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## Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

# LSM330DLC

## iNEMO inertial module: 3D accelerometer and 3D gyroscope

**Datasheet — production data**

## Features

- Analog supply voltage: 2.4 V to 3.6 V
- Digital supply voltage IOs: 1.8 V
- Low power mode
- Power-down mode
- 3 independent acceleration channels and 3 angular rate channels
- ±2 *g*/±4 *g*/±8 *g*/±16 *g* dynamically selectable full scale
- ±250/±500/±2000 dps dynamically selectable full scale
- SPI/$I^2C$ serial interface (16-bit data output)
- Programmable interrupt generator for free-fall and motion detection
- ECOPACK® RoHS and “Green” compliant

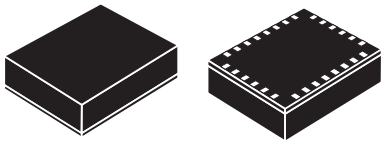
## Application

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

## Description

The LSM330DLC is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers.



**LGA-28L (4x5x1.1 mm)**

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330DLC has dynamically user-selectable full scale acceleration range of ±2 *g*/±4 *g*/±8 *g*/±16 *g* and angular rate of ±250/±500/±2000 deg/sec.

The accelerometer and gyroscope sensors can be either activated or separately put in Low power/Power-down mode for applications optimized for power saving.

The LSM330DLC is available in a plastic land grid array (LGA) package.

**Table 1. Device summary**

| Part number | Temperature range [°C] | Package | Packing |
|---|---|---|---|
| LSM330DLC | -40 to +85 | LGA-28L (4x5x1.1 mm) | Tray |
| LSM330DLCTR | -40 to +85 | | Tape and reel |

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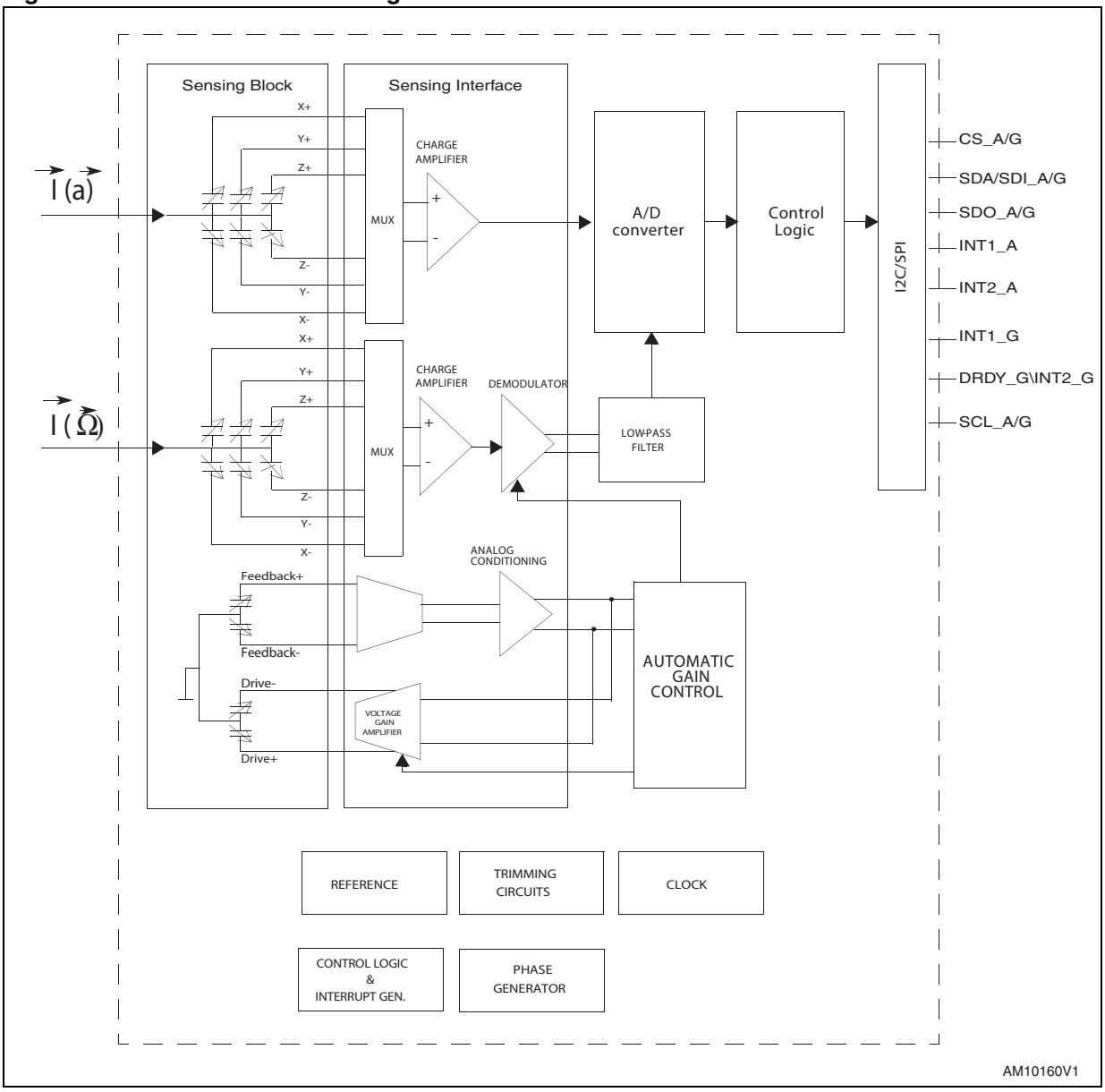
# 1 Block diagram and pin description

## 1.1 Block diagram

**Figure 1. LSM330DLC block diagram**



## 1.2 Pin description

**Figure 2. Pin connection**

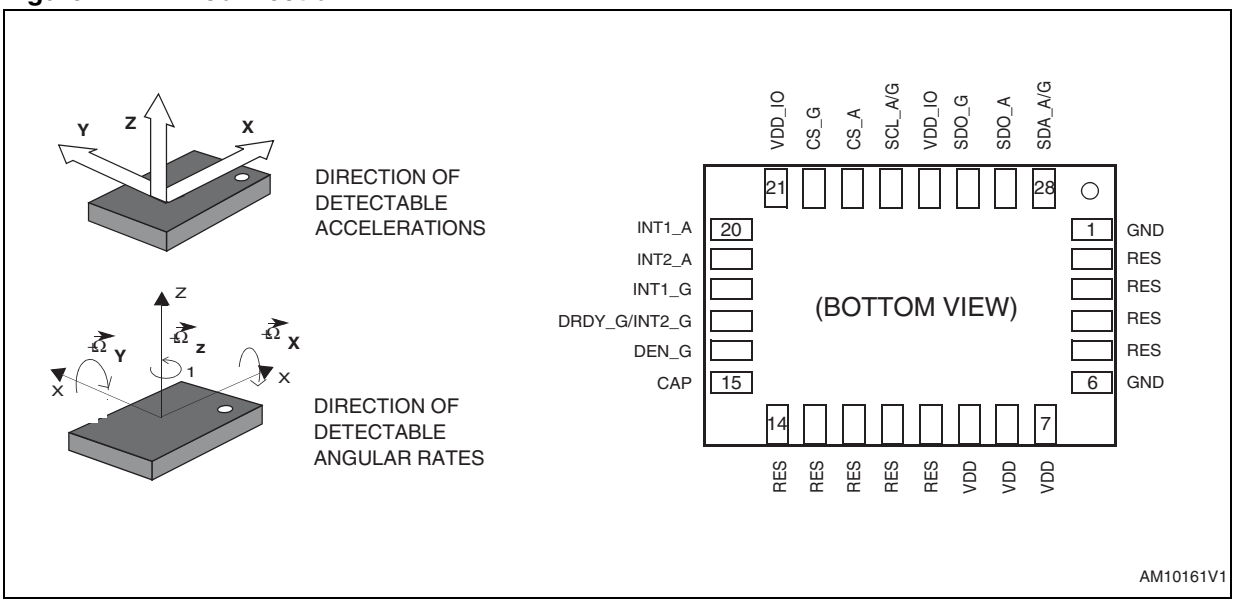



**Table 2. Pin description**

| Pin# | Name | Function |
|---|---|---|
| 1 | GND | 0 V supply |
| 2 | Res | Reserved. Connect to GND |
| 3 | Res | Reserved. Connect to GND |
| 4 | Res | Reserved. Connect to GND |
| 5 | Res | Reserved. Connect to GND |
| 6 | GND | 0 V supply |
| 7 | Vdd | Power supply |
| 8 | Vdd | Power supply |
| 9 | Vdd | Power supply |
| 10 | Res | Reserved. Connect to Vdd |
| 11 | Res | Reserved. Connect to Vdd |
| 12 | Res | Reserved. Connect to Vdd |
| 13 | Res | Reserved. Connect to Vdd |
| 14 | Res | Reserved. Connect to Vdd |
| 15 | Cap | Connect to GND with ceramic capacitor, 10 nF (+/-10%), 25 V |
| 16 | DEN_G | Gyroscope data enable |
| 17 | DRDY_G/ INT2_G | Gyroscope data ready/interrupt signal 2 |
| 18 | INT1_G | Gyroscope interrupt signal |

Table 2. Pin description (continued)

| Pin# | Name | Function |
|---|---|---|
| 19 | INT2_A | Accelerometer interrupt signal |
| 20 | INT1_A | Accelerometer interrupt signal |
| 21 | Vdd_IO | Power supply for IO pins |
| 22 | CS_G | Gyroscope: SPI enable<br>$I^2C$/SPI mode selection (1: SPI idle mode / $I^2C$ communication enabled; 0: SPI communication mode / $I^2C$ disabled) |
| 23 | CS_A | Accelerometer: SPI enable<br>$I^2C$/SPI mode selection (1: SPI idle mode / $I^2C$ communication enabled; 0: SPI communication mode / $I^2C$ disabled) |
| 24 | SCL_A/G | $I^2C$ serial clock (SCL)/SPI serial port clock (SPC) |
| 25 | Vdd_IO | Power supply for IO pins |
| 26 | SDO_G | Gyroscope:<br>SPI serial data output (SDO)<br>$I^2C$ least significant bit of the device address (SA0) |
| 27 | SDO_A | Accelerometer:<br>SPI serial data output (SDO)<br>$I^2C$ least significant bit of the device address (SA0) |
| 28 | SDA_A/G | $I^2C$ serial data (SDA)<br>SPI serial data input (SDI)<br>3-wire interface serial data output (SDO) |

# 2 Module specifications

## 2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [a]

**Table 3. Mechanical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| LA_FS | Linear acceleration measurement range(2) | User-selectable | | ±2 | | *g* |
| | | | | ±4 | | |
| | | | | ±8 | | |
| | | | | ±16 | | |
| G_FS | Angular rate measurement range(3) | User-selectable | | ±250 | | dps |
| | | | | ±500 | | |
| | | | | ±2000 | | |
| LA_So | Linear acceleration sensitivity | FS = ±2 *g* | | 1 | | m*g*/digit |
| | | FS = ±4 *g* | | 2 | | |
| | | FS = ±8 *g* | | 4 | | |
| | | FS = ±16 *g* | | 12 | | |
| G_So | Angular rate sensitivity | FS = ±250 dps | | 8.75 | | mdps/ digit |
| | | FS = ±500 dps | | 17.50 | | |
| | | FS = ±2000 dps | | 70 | | |
| LA_So | Linear acceleration sensitivity change vs. temperature | FS = ±2 *g* | | ±0.05 | | %/°C |
| G_SoDr | Angular rate sensitivity change vs. temperature | From -40 °C to +85 °C | | ±2 | | % |
| LA_TyOff | Linear acceleration typical zero-*g* level offset accuracy(3) | FS bit set to 00 | | ±60 | | m*g* |
| G_TyOff | Angular rate typical zero-rate level(4) | FS = 250 dps | | ±10 | | dps |
| | | FS = 500 dps | | ±15 | | |
| | | FS = 2000 dps | | ±25 | | |
| LA_TCOff | Linear acceleration zero-*g* level change vs. temperature | Max delta from 25 °C | | ±0.5 | | m*g*/°C |
| G_TCOff | Zero-rate level change vs. temperature | | | ±0.05 | | dps/°C |
| An | Acceleration noise density | FS = ±2 g, Normal mode *Table 9*, ODR bit set to 1001 *Table 19* | | 220 | | µg/√Hz |

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

**Table 3. Mechanical characteristics (continued)**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Rn | Rate noise density | FS = ±250 dps, BW = 50 Hz | | 0.03 | | dps/√Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.

## 2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted

**Table 4. Electrical characteristics**

| Symbol | Parameter | Test conditions | Min. | Typ.(1) | Max. | Unit |
|---|---|---|---|---|---|---|
| Vdd | Supply voltage | | 2.4 | | 3.6 | V |
| Vdd_IO | Power supply for I/O | | 1.71 | | Vdd+0.1 | V |
| LA_Idd | Accelerometer current consumption in Normal mode | ODR = 50 Hz | | 11 | | µA |
| | | ODR = 1 Hz | | 2 | | |
| LA_IddLowP | Accelerometer current consumption in Low power mode | ODR = 50 Hz | | 6 | | µA |
| LA_IddPdn | Accelerometer current consumption in Power-down mode | | | 0.5 | | µA |
| G_Idd | Gyroscope current consumption in Normal mode | | | 6.1 | | mA |
| G_IddLowP | Gyroscope supply current in Sleep mode(2) | | | 2 | | mA |
| G_IddPdn | Gyroscope current consumption in Power-down mode | | | 5 | | µA |
| VIH | Digital high level input voltage | | 0.8*Vdd_IO | | | V |
| VIL | Digital low level input voltage | | | | 0.2*Vdd_IO | V |
| VOH | High level output voltage | | 0.9*Vdd_IO | | | V |
| VOL | Low level output voltage | | | | 0.1*Vdd_IO | V |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to Power-down mode.

## 2.3 Temperature sensor characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [b]

**Table 5. Electrical characteristics**

| Symbol | Parameter | Test condition | Min. | Typ.[1] | Max. | Unit |
|---|---|---|---|---|---|---|
| TSDr | Temperature sensor output change vs. temperature | - | | -1 | | °C/digit |
| TODR | Temperature refresh rate | | | 1 | | Hz |
| Top | Operating temperature range | | -40 | | +85 | °C |

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

## 2.4 Communication interface characteristics

### 2.4.1 SPI - serial peripheral interface

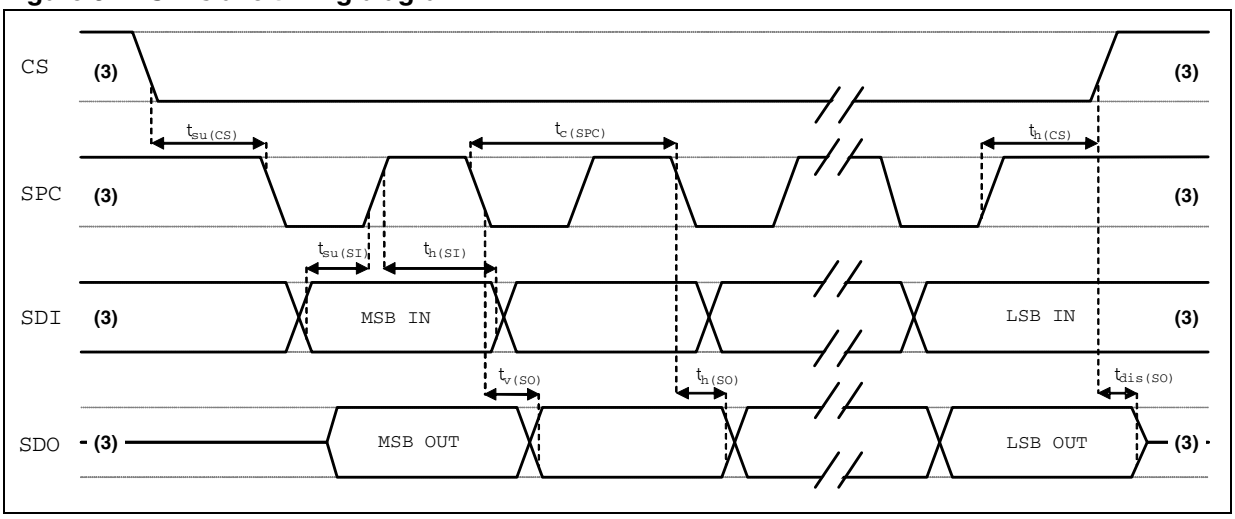
Subject to general operating conditions for Vdd and $T_{OP}$

**Table 6. SPI slave timing values**

| Symbol | Parameter | Value (1) | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| tc(SPC) | SPI clock cycle | 100 | | ns |
| fc(SPC) | SPI clock frequency | | 10 | MHz |
| tsu(CS) | CS setup time | 6 | | ns |
| th(CS) | CS hold time | 8 | | |
| tsu(SI) | SDI input setup time | 5 | | |
| th(SI) | SDI input hold time | 15 | | |
| tv(SO) | SDO valid output time | | 50 | |
| th(SO) | SDO output hold time | 9 | | |
| tdis(SO) | SDO output disable time | | 50 | |

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results. Not tested in production.

**Figure 3. SPI slave timing diagram(c)(d)**




3. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

c. The SDO output line features an internal pull-up.

d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

### 2.4.2 I²C - inter IC control interface

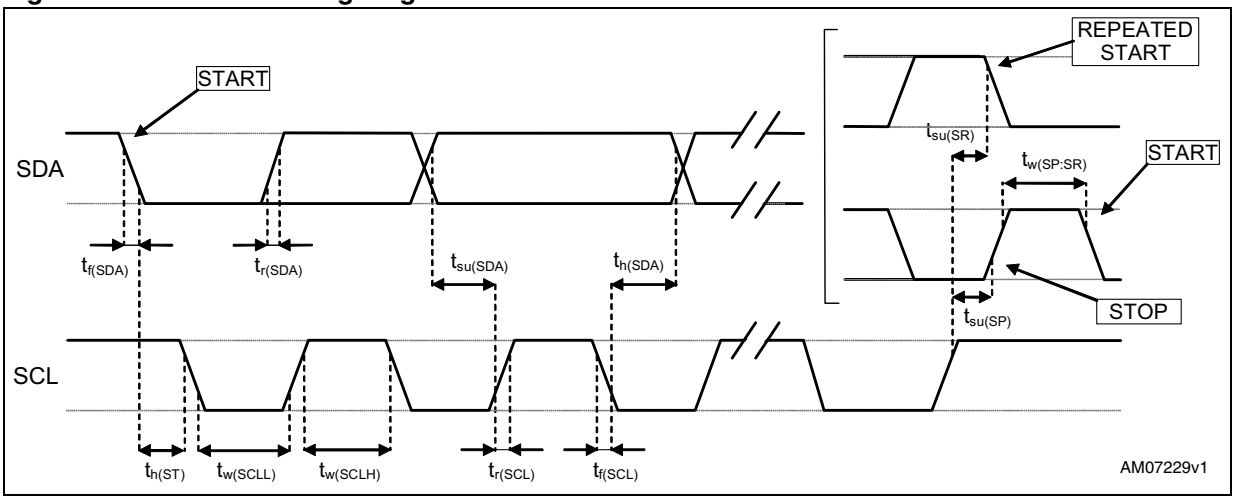
Subject to general operating conditions for Vdd and $T_{OP}$

**Table 7. I²C slave timing values**

| Symbol | Parameter(1) | I²C standard mode (1) | | I²C fast mode (1) | | Unit |
|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | |
| $f_{(SCL)}$ | SCL clock frequency | 0 | 100 | 0 | 400 | KHz |
| $t_{w(SCLL)}$ | SCL clock low time | 4.7 | | 1.3 | | µs |
| $t_{w(SCLH)}$ | SCL clock high time | 4.0 | | 0.6 | | |
| $t_{su(SDA)}$ | SDA setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0.01 | 3.45 | 0 | 0.9 | µs |
| $t_{r(SDA)}$ $t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | $20 + 0.1C_b$ (2) | 300 | ns |
| $t_{f(SDA)}$ $t_{f(SCL)}$ | SDA and SCL fall time | | 300 | $20 + 0.1C_b$ (2) | 300 | |
| $t_{h(ST)}$ | START condition hold time | 4 | | 0.6 | | µs |
| $t_{su(SR)}$ | Repeated START condition setup time | 4.7 | | 0.6 | | |
| $t_{su(SP)}$ | STOP condition setup time | 4 | | 0.6 | | |
| $t_{w(SP:SR)}$ | Bus free time between STOP and START condition | 4.7 | | 1.3 | | |

1. SCL (SCL_A/G pin), SDA (SDA_A/G pin)
2. Cb = total capacitance of one bus line, in pF

**Figure 4. I²C slave timing diagram(e)**




e. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports

## 2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

**Table 8. Absolute maximum ratings(1)**

| Symbol | Ratings | Maximum value | Unit |
|---|---|---|---|
| Vdd | Supply voltage | -0.3 to 4.8 | V |
| Vdd_IO | I/O pins supply voltage | -0.3 to 4.8 | V |
| Vin | Input voltage on any control pin (SCL_A/G, SDA_A/G, SDO_A, SDO_G, CS_A, CS_G, DEN_G) | -0.3 to Vdd_IO +0.3 | V |
| $A_{POW}$ | Acceleration (any axis, powered, Vdd = 3 V) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $A_{UNP}$ | Acceleration (any axis, unpowered) | 3000 *g* for 0.5 ms | |
| | | 10000 *g* for 0.1 ms | |
| $T_{OP}$ | Operating temperature range | -40 to +85 | °C |
| $T_{STG}$ | Storage temperature range | -40 to +125 | °C |
| ESD | Electrostatic discharge protection | 2 (HBM) | kV |

1. Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

# 3 Terminology

## 3.1 Sensitivity

Linear acceleration sensitivity can be determined e.g. by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

Angular Rate Sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and also very little over time.

## 3.2 Zero-*g* level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X axis and Y axes, whereas the Z axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as 2's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and over time.

# 4 Functionality

The LSM330DLC is a system-in-package featuring a 3D digital accelerometer and a 3D digital gyroscope.

The device includes specific sensing elements and two IC interfaces capable to measuring both the acceleration and angular rate applied to the module and to provide a signal to external applications through an SPI/$I^2C$ serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using a CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330DLC may also be configured to generate an inertial *wakeup* and *free-fall* interrupt signal according to a programmed acceleration event along the enabled axes.

## 4.1 Normal mode, Low power mode

The LSM330DLC provides two different operating modes: *Normal mode* and *Low power mode*. Normal mode guarantees high resolution, while Low power mode further reduces current consumption.

The table below summarizes how to select the operating mode and the corresponding characteristics.

**Table 9. Operating mode selection**

| Operating mode | CTRL_REG1[3] (LPen bit) | CTRL_REG4[3] (HR bit) | BW [Hz] | Turn-on time [ms] |
|---|---|---|---|---|
| Low power mode (8-bit) | 1 | 0 | ODR/2 | 1 |
| Normal mode (12-bit) | 0 | 1 | ODR/9 | 7/ODR(kHz) |

### 4.1.1 Self-test

Self-test allows the checking of sensor functionality without moving it. The self-test function is off when the self-test bit (ST) is programmed to '0'. When the self-test bit is programmed to '1' an actuation force is applied to the sensor, simulating a definite input acceleration. In this case, the sensor outputs exhibit a change in their DC levels which are related to the selected full scale through the device sensitivity. When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic test-force. If the output signals change within the amplitude specified in *Table 3*, then the sensor is working properly and the parameters of the interface chip are within the defined specifications.

### 4.1.2 6D/4D orientation detection

The LSM330DLC includes 6D/4D orientation detection. In this configuration the interrupt is generated when the device is stable in a known direction. In 4D configuration, Z axis position detection is disabled.

### 4.1.3 "Sleep-to-wake" and "Return to sleep"

The LSM330DLC can be programmed to automatically switch to Low power mode upon recognition of a determined event. Once the event condition is over, the device returns to the preset Normal mode.

To enable this function, the desired threshold value must be stored in the *Act_THS register*, while the duration value is written in the *Act_DUR register*.

When the internally high-pass filtered acceleration becomes lower than the threshold value on all the three axes, the device automatically switches to Low power mode (10Hz ODR). During this condition, the ODRx bits and LPen bit in the *CTRL_REG1_G register* and the HR bit in the *CTRL_REG3_G register* are not considered.

When the acceleration goes back over the threshold (on at least one axis), the system restores the operating mode and ODRs as per the *CTRL_REG1_G register* and *CTRL_REG3_G register* settings.

## 4.2 Linear acceleration digital main blocks

### 4.2.1 FIFO

The LSM330DLC embeds 32 slots of data FIFO for each of the three output channels: X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in four different modes: Bypass mode, FIFO mode, Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL_REG_A register*. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the INT1_A/INT2_A pin (configured through the *FIFO_CTRL_REG_A register*).

### 4.2.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

### 4.2.3 FIFO mode

In FIFO mode, data from the X, Y and Z channels are stored into the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in the *FIFO_CTRL_REG_A register* in order to be raised when the FIFO is filled to the level specified into the FIFO_WTMK_LEVEL bits of the *FIFO_CTRL_REG_A register*. The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO stops collecting data from the input channels.

### 4.2.4 Stream mode

In Stream mode, data from X, Y and Z measurement are stored into the FIFO. A watermark interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it is full (32 slots of data for X, Y and Z). When full, the FIFO discards the older data as the new data arrives.

### 4.2.5 Stream-to-FIFO mode

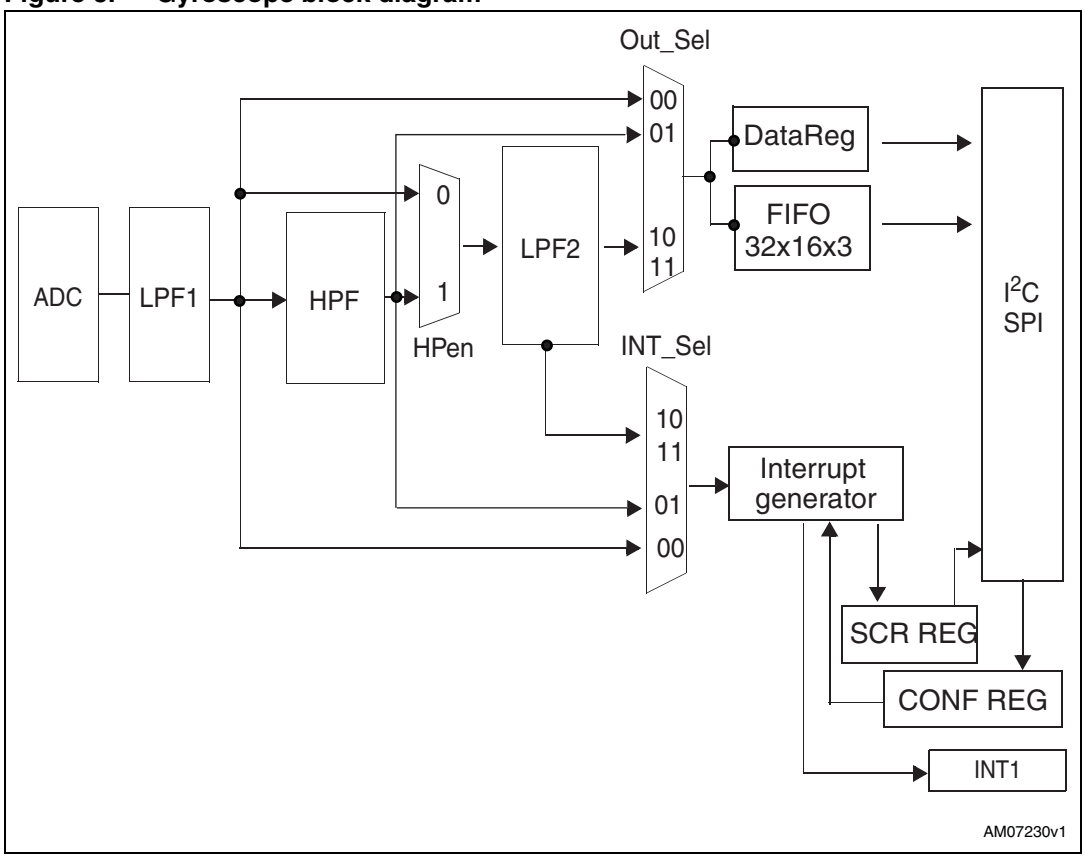
In Stream-to-FIFO mode, data from X, Y and Z measurement is stored in the FIFO. A watermark interrupt can be enabled (FIFO_WTMK_EN bit in the *FIFO_CTRL_REG_A register*) in order to be raised when the FIFO is filled to the level specified in the FIFO_WTMK_LEVEL bits of the *FIFO_CTRL_REG_A register*. The FIFO continues filling until it is full (32 slots of 8 -bit data for X, Y and Z). When full, the FIFO discards the older data as the data new arrives. Once trigger event occurs, the FIFO starts operating in FIFO mode.

### 4.2.6 Retrieve data from FIFO

FIFO data is read through *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* and *OUT_Z_L _A, OUT_Z_H_A*. When the FIFO is in Stream, Trigger or FIFO mode, a read operation to the *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* or *OUT_Z_L _A, OUT_Z_H_A* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A, OUT_X_H_A*, *OUT_Y_L_A, OUT_Y_H_A* and *OUT_Z_L _A, OUT_Z_H_A* registers and both single read and read_burst operations can be used.

## 4.3 Gyroscope digital main blocks

**Figure 5. Gyroscope block diagram**



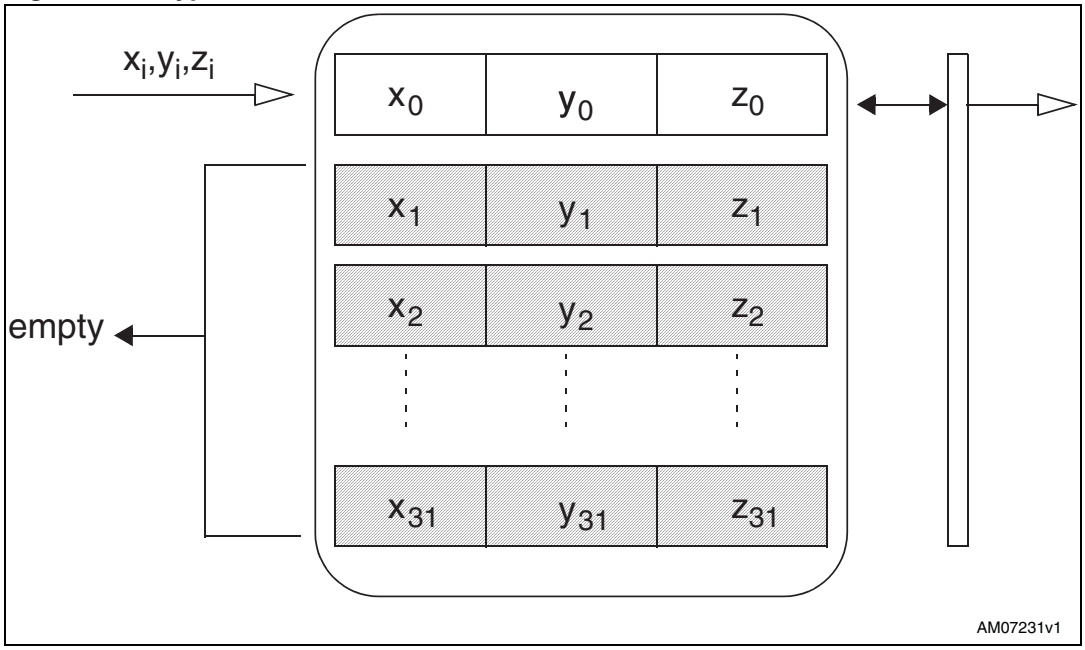
## 4.4 FIFO

The LSM330DLC embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but can wake up only when needed and burst the significant data out from the FIFO. This buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FIFO_MODE bits in the *FIFO_CTRL_REG_G register*. Programmable watermark level, FIFO_empty or FIFO_Full events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through the *CTRL_REG3_G register* and event detection information is available in the *FIFO_SRC_REG_G register*. Watermark level can be configured to WTM4:0 in the *FIFO_CTRL_REG_G register*.

### 4.4.1 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in *Figure 6* below, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available the old data is overwritten.

**Figure 6. Bypass mode**

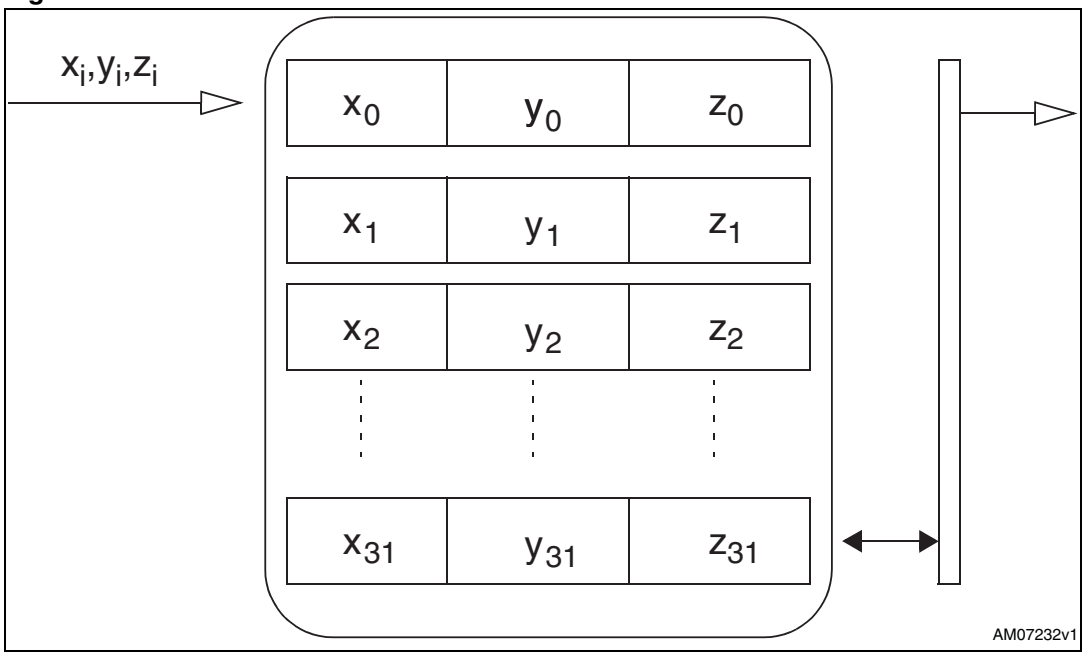



### 4.4.2 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels is stored in the FIFO. A watermark interrupt can be enabled (I2_WMK bit in the *CTRL_REG3_G register*) in order to be raised when the FIFO is filled to the level specified in the WTM 4:0 bits of the *FIFO_CTRL_REG_G register*. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart data collection, the *FIFO_CTRL_REG_G register* must be written back to Bypass mode.

FIFO mode is represented in *Figure 7: FIFO mode*.

**Figure 7. FIFO mode**




### 4.4.3 Stream mode

In Stream mode, data from yaw, pitch and roll measurement is stored in the FIFO. A watermark interrupt can be enabled and set as in FIFO mode.The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO discards the older data as the new data arrives. Programmable watermark level events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configured through the *CTRL_REG3_G register*.

Stream mode is represented in *Figure 8: Stream mode*.

**Figure 8. Stream mode**