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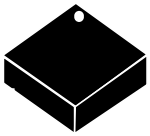
LSM330

iNEMO inertial module: 3D accelerometer and 3D gyroscope

Datasheet - production data



LGA-24L (3x3.5x1 mm)

Features

- Analog supply voltage: 2.4 V to 3.6 V
- Digital supply voltage IOs: 1.8 V
- Power-down and sleep modes
- 2 embedded programmable state machines
- 3 independent acceleration channels and 3 angular rate channels
- ±2/±4/±6/±8/±16 *g* selectable full scale
- ±250/±500/±2000 dps selectable full scale
- SPI/I^2C serial interface
- Embedded temperature sensor
- Embedded FIFO
- ECOPACK® RoHS and “Green” compliant

Applications

- GPS navigation systems
- Impact recognition and logging
- Gaming and virtual reality input devices
- Motion-activated functions
- Intelligent power saving for handheld devices
- Vibration monitoring and compensation
- Free-fall detection
- 6D orientation detection

Description

The LSM330 is a system-in-package featuring a 3D digital accelerometer with two embedded state machines that can be programmed to implement autonomous applications and a 3D digital gyroscope.

ST’s family of MEMS sensor modules leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

The LSM330 has a user-selectable full-scale acceleration range of ±2/±4/±6/±8/±16 *g* and an angular rate range of ±250/±500/±2000 dps. The accelerometer and gyroscope sensors can be either activated or separately put in power-down / sleep mode for applications optimized for power saving.

The LSM330 is available in a plastic land grid array (LGA) package.

Table 1. Device summary

Part number	Temperature range [°C]	Package	Packing
LSM330	-40 to +85	LGA-24L (3x3.5x1mm)	Tray
LSM330TR	-40 to +85		Tape and reel

Contents

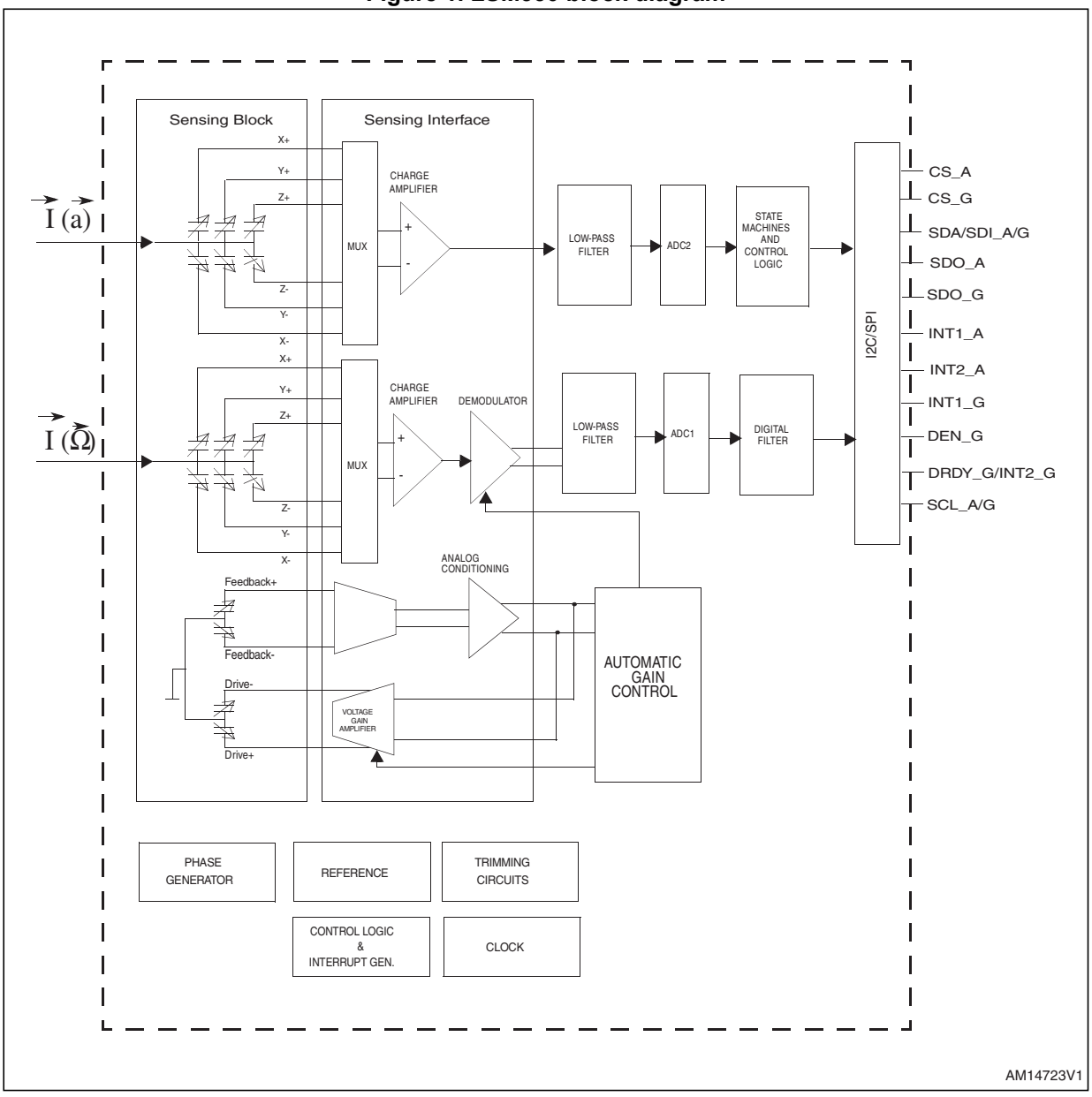
List of tables

List of figures

1 Block diagram and pin description

1.1 Block diagram

Figure 1. LSM330 block diagram



1.2 Pin description

Figure 2. Pin connections

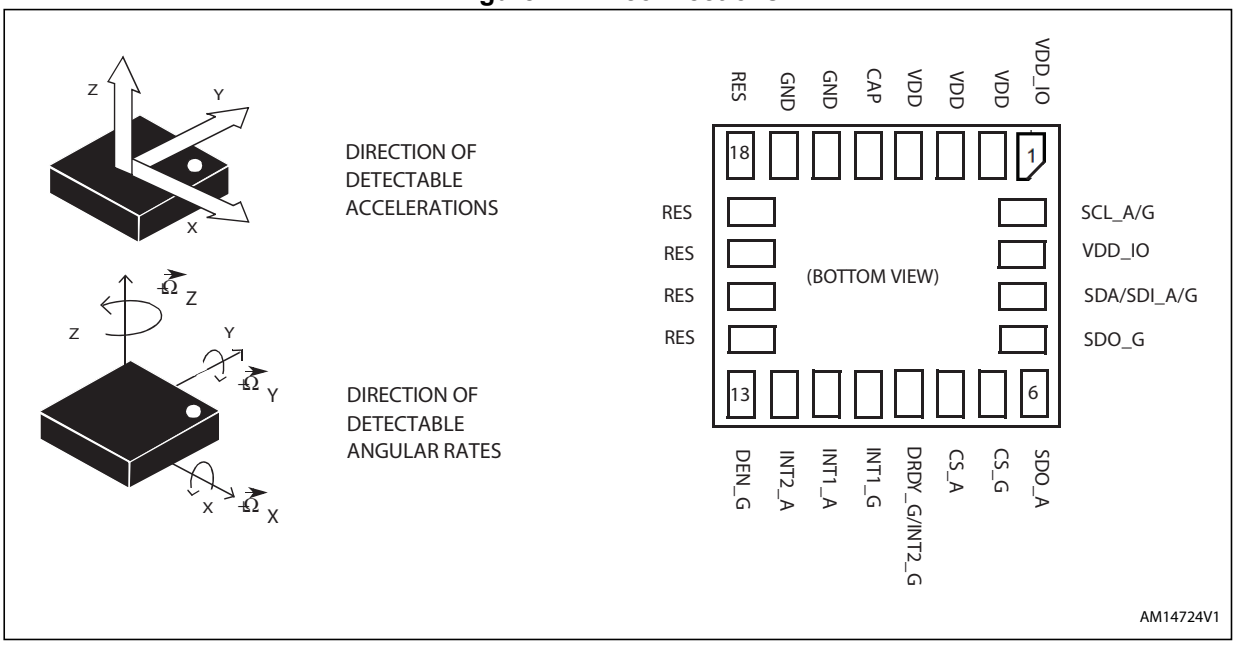


Table 2. Pin description

Pin #	Name	Function
1	Vdd_IO(1)	Power supply for IO pins
2	SCL_A/G	I^2C serial clock (SCL)/SPI serial port clock (SPC)
3	Vdd_IO(1)	Power supply for IO pins
4	SDA/SDI_A/G	I^2C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
5	SDO_G	Gyroscope: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
6	SDO_A	Accelerometer: SPI serial data output (SDO) I^2C least significant bit of the device address (SA0)
7	CS_G	Gyroscope: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
8	CS_A	Accelerometer: SPI enable I^2C/SPI mode selection (1: SPI idle mode / I^2C communication enabled; 0: SPI communication mode / I^2C disabled)
9	DRDY_G/ INT2_G	Gyroscope Data Ready/FIFO Interrupt (Watermark/Overrun/Empty)

Table 2. Pin description (continued)

Pin #	Name	Function
10	INT1_G	Gyroscope interrupt signal
11	INT1_A	Accelerometer interrupt1 signal
12	INT2_A	Accelerometer interrupt2 signal
13	DEN_G	Gyroscope Data Enable
14	Res	Reserved. Connect to GND
15	Res	Reserved. Connect to GND
16	Res	Reserved. Connect to GND
17	Res	Reserved. Connect to GND
18	Res	Reserved. Connect to GND
19	GND	0 V supply
20	GND	0 V supply
21	CAP	Connect to GND with ceramic capacitor(2)
22	Vdd(3)	Power supply
23	Vdd(3)	Power supply
24	Vdd(3)	Power supply

1. 100 nF filter capacitor recommended.
2. 10 nF (+/- 10%), 25 V. 1nF minimum value has to be guaranteed under 11 V bias condition1.
3. 100 nF plus 10 µF capacitors recommended.

2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [a]

Table 3. Mechanical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
LA_FS	Linear acceleration measurement range(2)	FS bit set to 000		±2.0		*g*
		FS bit set to 001		±4.0		
		FS bit set to 010		±6.0		
		FS bit set to 011		±8.0		
		FS bit set to 100		±16.0		
G_FS	Angular rate measurement range(3)	FS bit set to 00		±250		dps
		FS bit set to 01		±500		
		FS bit set to 10		±2000		
LA_So	Linear acceleration sensitivity	FS bit set to 000		0.061		mg/digit
		FS bit set to 001		0.122		
		FS bit set to 010		0.183		
		FS bit set to 011		0.244		
		FS bit set to 100		0.732		
G_So	Angular rate sensitivity	FS = ±250 dps		8.75		mdps/ digit
		FS = ±500 dps		17.50		
		FS = ±2000 dps		70		
LA_TyOff	Linear acceleration typical zero-*g* level offset accuracy(3)	FS bit set to 000		±60		m*g*
G_TyOff	Angular rate typical zero-rate level(4)	FS = 250 dps		±10		dps
		FS = 500 dps		±15		
		FS = 2000 dps		±25		
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Verified by wafer level test and measurement of initial offset and sensitivity.
3. Typical zero-*g* level offset value after MSL3 preconditioning.
4. Offset can be eliminated by enabling the built-in high-pass filter.

a. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.4 V to 3.6 V.

2.2 Electrical characteristics

@ Vdd = 3 V, T = 25 °C unless otherwise noted

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.(1)	Max.	Unit
Vdd	Supply voltage		2.4		3.6	V
Vdd_IO	Power supply for I/O		1.71		Vdd+0.1	V
LA_Idd	Accelerometer current consumption in normal mode	1.6 kHz ODR		250		µA
		3.125 Hz ODR		10		
LA_IddPdn	Accelerometer current consumption in power-down mode			1		µA
G_Idd	Gyroscope current consumption in Normal mode			6.1		mA
G_IddLowP	Gyroscope supply current in sleep mode(2)			2		mA
G_IddPdn	Gyroscope current consumption in power-down mode			5		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
VOH	High level output voltage		0.9*Vdd_IO			V
VOL	Low level output voltage				0.1*Vdd_IO	V
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Sleep mode introduces a faster turn-on time compared to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd = 3V, T = 25 °C unless otherwise noted [b]

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.(1)	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

b. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

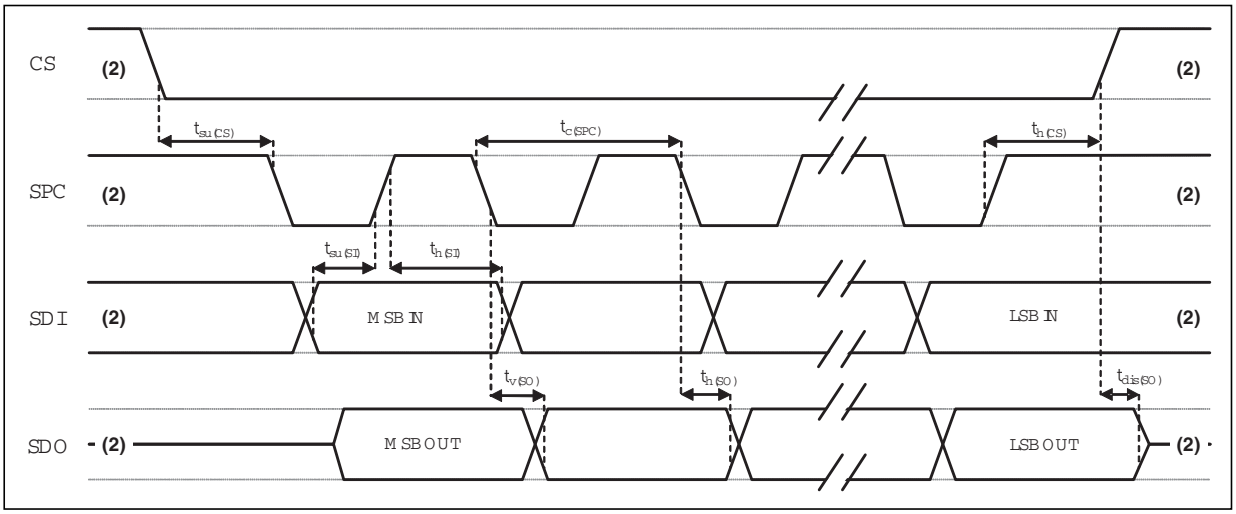
Subject to general operating conditions for Vdd and T_{OP}.

Table 6. SPI slave timing values

Symbol	Parameter(1)	Value(2)		Unit
		Min	Max	
$t_{c(SPC)}$	SPI clock cycle	100		ns
$f_{c(SPC)}$	SPI clock frequency		10	MHz
$t_{su(CS)}$	CS setup time	6		ns
$t_{h(CS)}$	CS hold time	8		
$t_{su(SI)}$	SDI input setup time	5		
$t_{h(SI)}$	SDI input hold time	15		
$t_{v(SO)}$	SDO valid output time		50	
$t_{h(SO)}$	SDO output hold time	9		
$t_{dis(SO)}$	SDO output disable time		50	

1. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.
2. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results. Not tested in production.

Figure 3. SPI slave timing diagram



2. Data on CS, SPC, SDI and SDO refer to pins: CS_A, CS_G, SCL_A/G, SDA_A/G, SDO_A / SDO_G.

Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both input and output ports.

2.4.2 I²C - inter-IC control interface

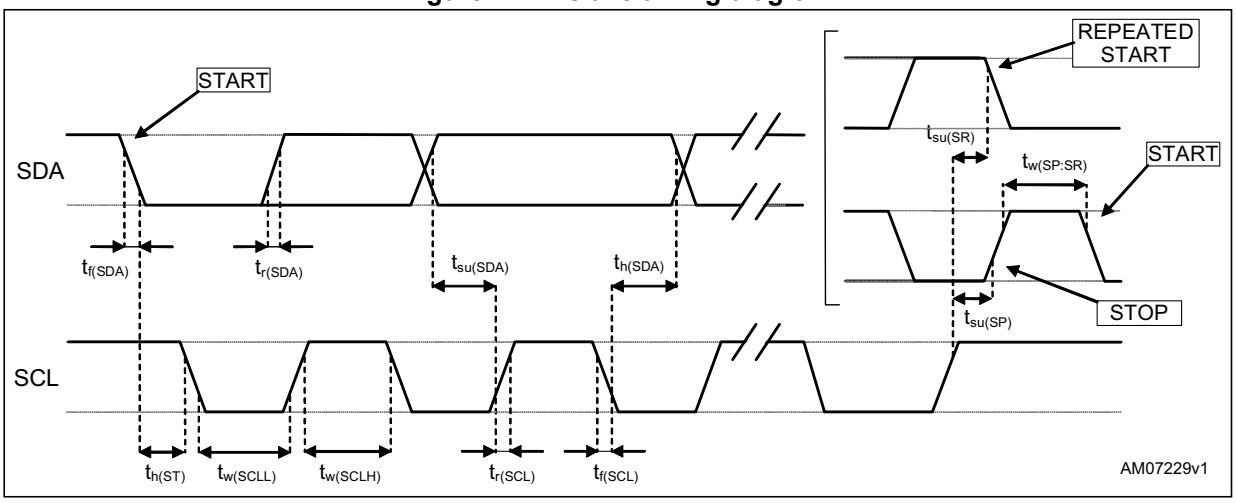
Subject to general operating conditions for Vdd and T_{OP}.

Table 7. I²C slave timing values

Symbol	Parameter(1)	I²C standard mode (1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		µs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0.01	3.45	0	0.9	µs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	20 + 0.1C_b (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	20 + 0.1C_b (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		µs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. SCL (SCL_A/G pin), SDA (SDA_A/G pin).
2. C_b = total capacitance of one bus line, in pF

Figure 4. I²C slave timing diagram



Note: Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings(1)

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
Vdd_IO	I/O pins supply voltage	-0.3 to 4.8	V
Vin	Input voltage on any control pin (SCL_A/G, SDA_A/G, SDO_A, SDO_G, CS_A, CS_G, DEN_G)	-0.3 to Vdd_IO +0.3	V
A_{POW}	Acceleration (any axis, powered, Vdd = 3 V)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
A_{UNP}	Acceleration (any axis, unpowered)	3000 *g* for 0.5 ms	
		10000 *g* for 0.1 ms	
T_{OP}	Operating temperature range	-40 to +85	°C
T_{STG}	Storage temperature range	-40 to +125	°C
ESD	Electrostatic discharge protection	2 (HBM)	kV

1. Supply voltage on any pin should never exceed 4.8 V.

This device is sensitive to mechanical shock, improper handling can cause permanent damage to the part.

This device is sensitive to electrostatic discharge (ESD), improper handling can cause permanent damage to the part.

3 Terminology

3.1 Sensitivity

Linear acceleration sensitivity can be determined by applying 1 *g* acceleration to the device. Because the sensor can measure DC accelerations, this can be done easily by pointing the selected axis towards the ground, noting the output value, rotating the sensor 180 degrees (pointing towards the sky) and noting the output value again. By doing so, ±1 *g* acceleration is applied to the sensor. Subtracting the larger output value from the smaller one, and dividing the result by 2, leads to the actual sensitivity of the sensor. This value changes very little over temperature and over time. The sensitivity tolerance describes the range of sensitivities of a large number of sensors.

Angular rate sensitivity describes the angular rate gain of the sensor and can be determined by applying a defined angular velocity to the device. This value changes very little over temperature and also very little overtime.

3.2 Zero-*g* and zero rate level

Linear acceleration zero-*g* level offset (TyOff) describes the deviation of an actual output signal from the ideal output signal if no acceleration is present. A sensor in a steady state on a horizontal surface will measure 0 *g* on both the X-axis and Y-axis, whereas the Z-axis will measure 1 *g*. Ideally, the output is in the middle of the dynamic range of the sensor (content of OUT registers 00h, data expressed as two's complement number). A deviation from the ideal value in this case is called zero-*g* offset.

Offset is to some extent a result of stress to MEMS sensor and therefore the offset can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. Offset changes little over temperature, see "Linear acceleration zero-*g* level change vs. temperature" in *Table 3*. The zero-*g* level tolerance (TyOff) describes the standard deviation of the range of zero-*g* levels of a group of sensors.

Angular rate zero-rate level describes the actual output value if there is no angular rate present. The zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore the zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress. This value changes very little over temperature and over time.

4 Functionality

The LSM330 is a system-in-package featuring a 3D digital accelerometer with two embedded state machines and a 3D digital gyroscope, together with two FIFO memory blocks available to manage linear acceleration and angular rate data.

The device includes specific sensing elements and two IC interfaces capable of measuring both the acceleration and angular rate applied to the module and providing a signal to external applications through an SPI/I^2C serial interface.

The various sensing elements are manufactured using specialized micromachining processes, while the IC interfaces are developed using CMOS technology that allows the design of a dedicated circuit which is trimmed to better match the sensing element characteristics.

4.1 Power modes

The linear acceleration sensor and the angular rate sensor can be either activated or separately set in power-down/ sleep mode for applications optimized for power saving.

The acceleration sensor operating modes can be selected between normal or power-down through *CTRL_REG5_A (20h)*. The angular rate sensor operating mode can be selected among normal power-down or sleep mode, through *CTRL_REG1_G (20h)*.

4.2 Linear acceleration sensor digital main blocks

4.2.1 State machine

The LSM330 embeds two state machines able to run a user-defined program.

The program is composed of a set of instructions that defines the transition to successive states. Conditional branches are possible.

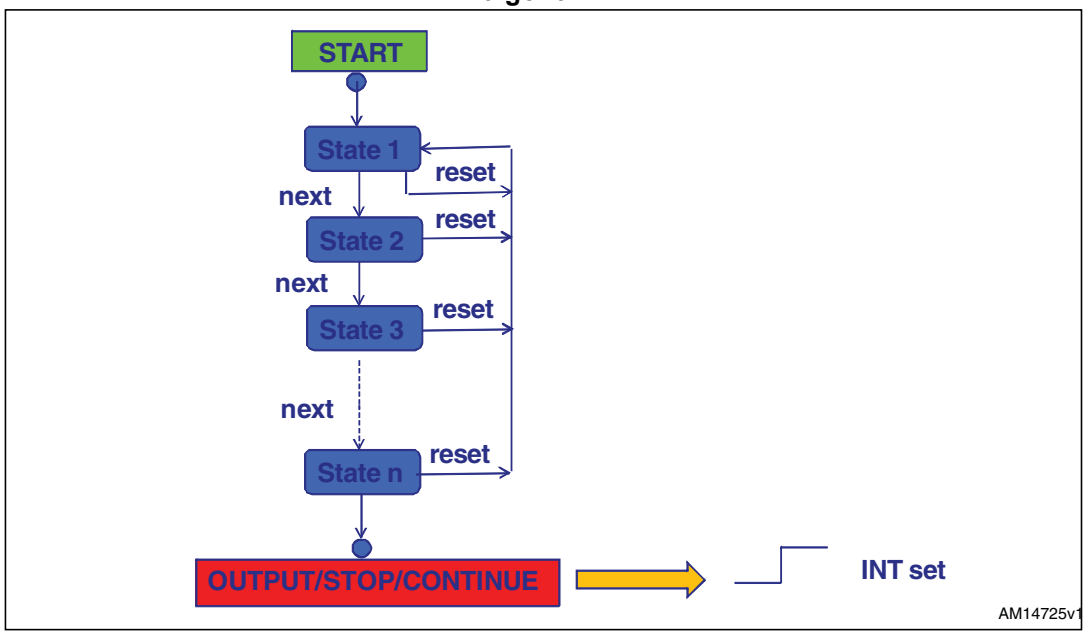
From each state (n) it is possible to have a transition to the next state (n+1) or to a reset state. The transition to the reset point happens when the “RESET condition” is true. The transition to the next step happens when the “NEXT condition” is true.

An interrupt is triggered when the Output/Stop/Continue state is reached.

Each State machine allows implementing, in a flexible way, gesture recognition, free-fall, wake-up, 4D/6D orientation, pulse counter and step recognition, click/double-click, shake/double-shake, face-up/face-down, turn/double-turn:

- Code and parameters are loaded by the host into dedicated memory areas for the state program
- State program with timing based on ODR or decimated time
- Possibility of conditional branches

Figure 5. LSM330 accelerometer state machines: sequence of state to execute an algorithm



4.2.2 FIFO

LSM330 embeds 32 slots of FIFO data for each of the three acceleration output channels X, Y and Z. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO. In order to use FIFO it is necessary to enable the FIFO_EN bit in the *CTRL_REG7_A (25h)* register.

The FIFO buffer can work accordingly in five different modes: Bypass mode, FIFO mode, Stream mode, Stream-to-FIFO mode and Bypass-to-Stream mode. Each mode is selected by the FMODE [2:0] bits in the *FIFO_CTRL_REG_A (2Eh)* register. Programmable watermark level, FIFO empty or FIFO overrun events can be enabled to generate dedicated interrupts on the INT1_A/INT2_A pin (configured through the INT2_EN and INT1_EN bits in the *CTRL_REG4_A (23h)* register).

When FIFO is empty, the EMPTY bit in *FIFO_SRC_REG_A (2Fh)* is equal to '1' and no samples are available.

If the application requires a lower number of samples, a programmable watermark level can be set. In *FIFO_SRC_REG_A (2Fh)* the WTM bit is high if new data arrives and the FSS [4:0] bit in *FIFO_SRC_REG_A (2Fh)* is greater than or equal to the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register. In *FIFO_SRC_REG_A (2Fh)* the WTM bit goes to '0' if reading X, Y, Z data slot from FIFO and the FSS [4:0] bit in *FIFO_SRC_REG_A (2Fh)* is less than or equal to the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register.

When FIFO is completely full, the OVRN_FIFO bit in the *FIFO_SRC_REG_A (2Fh)* is equal to '1' and the FIFO slot is overwritten.

4.2.3 Bypass mode

In Bypass mode, the FIFO is not operational and it remains empty. For each channel only the first address is used. The remaining FIFO slots are empty.

Bypass mode must be used in order to reset the FIFO buffer when a different mode is operating (i.e. FIFO mode).

4.2.4 FIFO mode

In FIFO mode, the buffer continues filling data from the X, Y and Z accelerometer channels until it is full (set of 32 samples stored). When the FIFO is full it stops collecting data from the input channels and the FIFO content remains unchanged.

An overrun interrupt can be enabled, P1_OVERRUN = '1' in the *CTRL_REG7_A (25h)* register, in order to be raised when the FIFO stops collecting data. When overrun interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

At the end of the reads it is necessary to transition from Bypass mode to reset FIFO content. After this reset command it is possible to restart FIFO mode by writing '001' to FMODE [2:0] in the *FIFO_CTRL_REG_A (2Eh)* register.

The FIFO buffer can memorize 32 levels of X, Y and Z data, but the depth of the FIFO can be reduced by a programmable watermark. In order to enable a FIFO watermark, the WTM_EN bit in *CTRL_REG7_A (25h)* is high and the FIFO depth is set by the WTMP [4:0] bits in the *FIFO_CTRL_REG_A (2Eh)* register. The watermark interrupt can be enabled on the INT1_A pad if the P1_WTM bit in the *CTRL_REG7_A (25h)* register is enabled.

4.2.5 Stream mode

In Stream mode FIFO continues filling data from the X, Y, and Z accelerometer channels. When the buffer is full (set of 32 samples stored) the FIFO buffer index restarts from the beginning and older data is replaced by the current. The oldest values continue to be overwritten until a read operation makes free FIFO slots available.

An overrun interrupt can be enabled, P1_OVERRUN = '1' in the *CTRL_REG7_A (25h)* register, in order to read the entire FIFO content at once. If in the application it is mandatory not to lose data and it is not possible to read at least one sample for each axis within one ODR period, a watermark interrupt can be enabled in order to read partially the FIFO and leave free memory slots for incoming data.

Setting the WTMP [4:0] bit in the *FIFO_CTRL_REG_A (2Eh)* register to value N, the number of X, Y and Z data samples that should be read at the rise of the watermark interrupt is up to (N+1).

In the latter case, reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in the previous burst, so the number of new data available in FIFO depends on the previous reading (see *FIFO_SRC_REG_A (2Fh)*).

At the end of the reads it is necessary to transition from Bypass mode to reset FIFO content.

4.2.6 Stream-to-FIFO mode

In Stream-to-FIFO mode FIFO behavior changes according to an interrupt generated by the configuration of the two state machines using the INT_SM1 and INT_SM2 bits in the *STAT (18h)* register.

When the INT_SM1, INT_SM2 bits in the *STAT (18h)* register are equal to '1', FIFO operates in FIFO mode. When the INT_SM1, INT_SM2 bits in the *STAT (18h)* register are equal to '0', FIFO operates in Stream mode.

4.2.7 Bypass-to-Stream mode

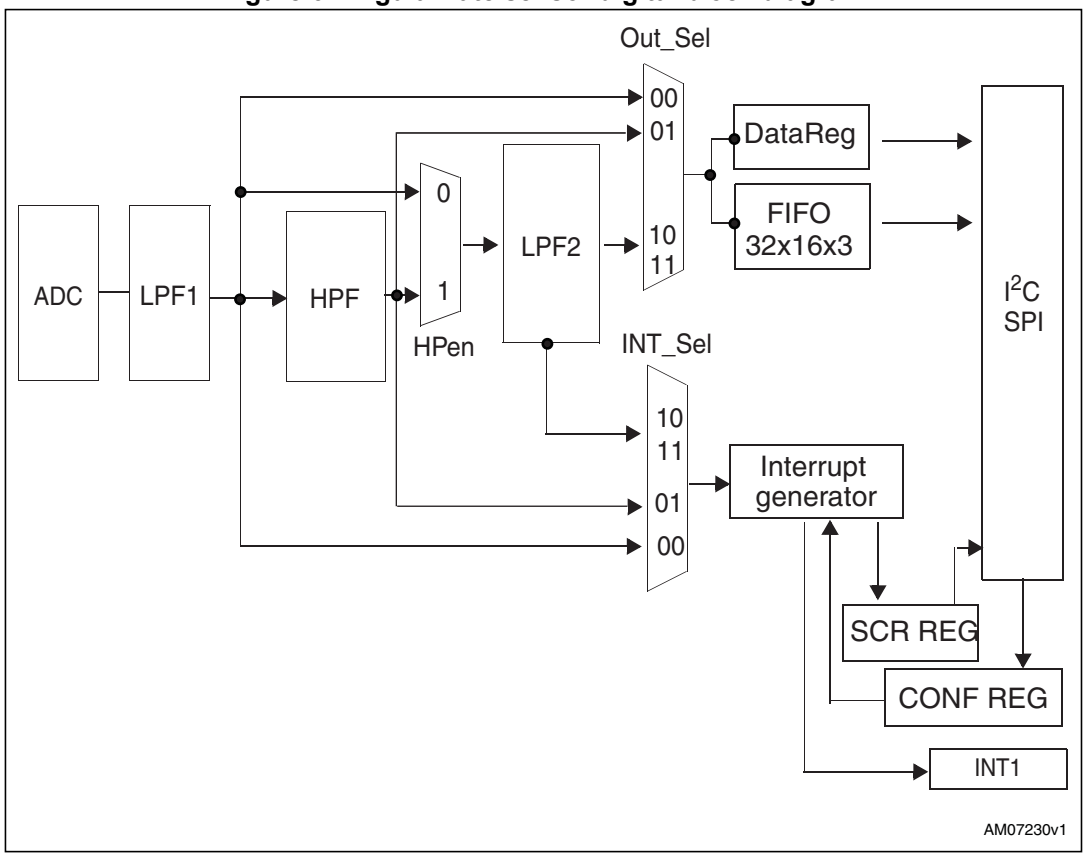
In Bypass-to-Stream mode, the FIFO starts operating in Bypass mode and once a trigger event occurs (*STAT (18h)*, the FIFO starts operating in Stream mode.

4.2.8 Retrieving data from FIFO

FIFO data is read from *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)*. When the FIFO is in Stream, Stream-to-FIFO mode or FIFO mode, a read operation from the *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* or *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)* registers provides the data stored in the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed in the *OUT_X_L_A (28h) and OUT_X_H_A (29h)*, *OUT_Y_L_A (2Ah) and OUT_Y_H_A (2Bh)* and *OUT_Z_L_A (2Ch) and OUT_Z_H_A (2Dh)* registers and both single read and read_burst operations can be used.

4.3 Angular rate sensor digital main blocks

Figure 6. Angular rate sensor digital block diagram



4.3.1 FIFO

The LSM330 embeds 32 slots of 16 bit data FIFO buffer for each of the three output channels, yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wake up only when needed and burst the significant data out from the FIFO.

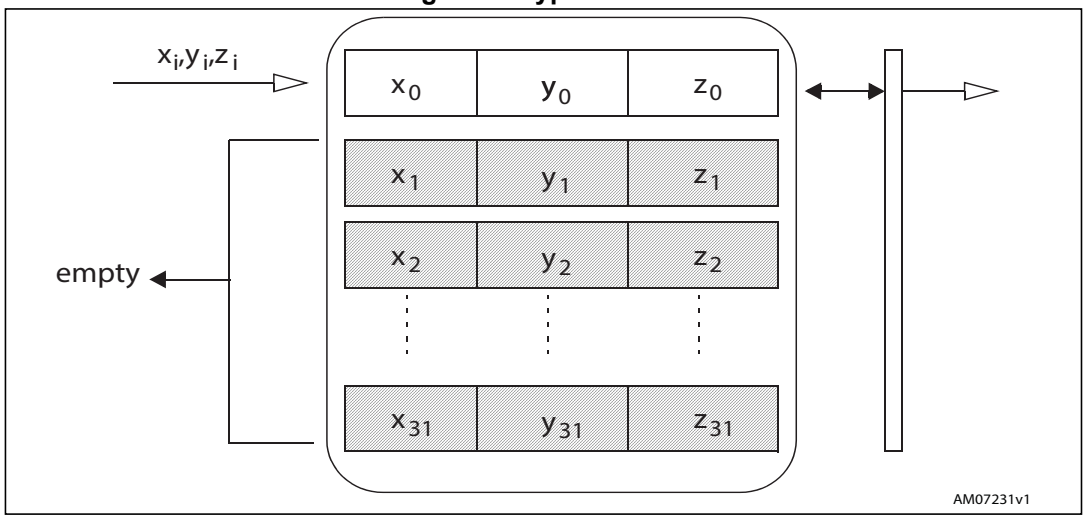
In order to use FIFO it is necessary to enable the FIFO_EN bit in the *CTRL_REG5_G (24h)* register. The FIFO buffer can work accordingly to five different modes: Bypass mode, FIFO mode, Stream mode, Bypass-to-Stream mode and Stream-to-FIFO mode. Each mode is selected by the FM[2:0] bits in the *FIFO_CTRL_REG_G (2Eh)* register.

Programmable watermark level, FIFO empty or FIFO full events can be enabled to generate dedicated interrupts on the DRDY_G/INT2_G pin (configuration through *CTRL_REG3_G (22h)*) and event detection information is available from *FIFO_SRC_REG_G (2Fh)*. The watermark level can be configured by the WTM[4:0] bits in *FIFO_CTRL_REG_G (2Eh)*.

4.3.2 Bypass mode

In Bypass mode, the FIFO is not operational and for this reason it remains empty. As described in the next figure, for each channel only the first address is used. The remaining FIFO slots are empty. When new data is available the previous data is overwritten.

Figure 7. Bypass mode



4.3.3 FIFO mode

In FIFO mode, data from the yaw, pitch and roll channels are stored in the FIFO. A watermark interrupt can be enabled (I2_WTM bit in *CTRL_REG3_G (22h)*) in order to be raised when the FIFO is filled to the level specified by the WTM[4:0] bits of the *FIFO_CTRL_REG_G (2Eh)* register. The FIFO continues filling until it is full (32 slots of 16-bit data for yaw, pitch and roll). When full, the FIFO stops collecting data from the input channels. To restart collecting data *FIFO_CTRL_REG_G (2Eh)* must be written back to Bypass mode. FIFO mode is represented in the following figure.

Figure 8. FIFO mode