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High Current Quad Output Regulator for TFT LCD Panels

FEATURES

- **4 Integrated Switches: 2.4A Buck, 2.6A Boost, 0.35A Boost, 0.35A Inverter (Guaranteed Minimum Current Limit)**
- **Fixed Frequency, Low Noise Outputs**
- **Soft-Start for all Outputs**
- **Externally Programmable V_{ON} Delay**
- Integrated Schottky Diode for V_{ON} Output
- PGOOD Pin for AV_{DD} Output Disconnect
- 4.5V to 22V Input Voltage Range
- PanelProtect™ Circuitry Disables V_{ON} Upon Fault
- Available in Thermally Enhanced 28-Lead TSSOP

APPLICATIONS

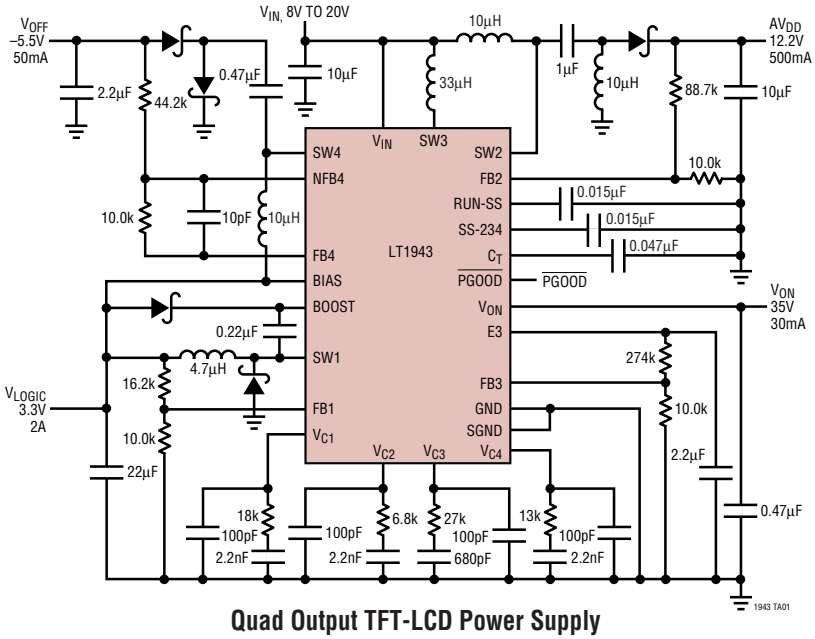
- Large TFT-LCD Desktop Monitors
- Flat Panel Televisions

DESCRIPTION

The LT®1943 quad output adjustable switching regulator provides power for large TFT LCD panels. The device, housed in a low profile 28 pin thermally enhanced TSSOP package, can generate a 3.3V or 5V logic supply along with the triple output supply required for the TFT LCD panel. Operating from an input range of 4.5V to 22V, a step-down regulator provides a low voltage output V_{LOGIC} with up to 2A current. A high-power step-up converter, a lower-power step-up converter and an inverting converter provide the three independent output voltages AV_{DD}, V_{ON} and V_{OFF} required by the LCD panel. A high-side PNP provides delayed turn-on of the V_{ON} signal and can handle up to 30mA. Protection circuitry ensures that V_{ON} is disabled if any of the four outputs are more than 10% below the programmed voltage.

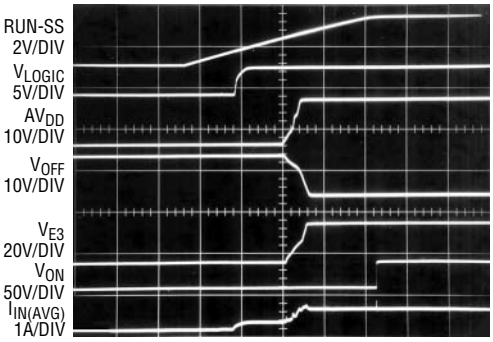
All switchers are synchronized to an internal 1.2MHz clock, allowing the use of low profile inductors and ceramic capacitors throughout. A current mode architecture provides excellent transient response. For best flexibility, all outputs are adjustable. Soft-start is included in all four channels. A PGOOD pin can drive an optional PMOS pass device to provide output disconnect for the AV_{DD} output.

TYPICAL APPLICATION



Quad Output TFT-LCD Power Supply

Startup Waveforms

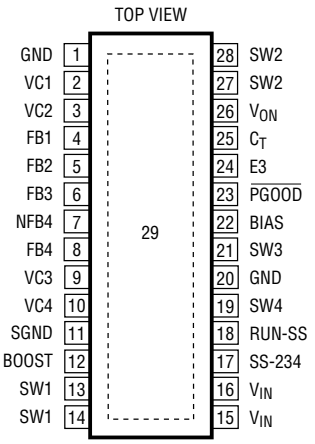


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} Voltage 25V
BOOST Voltage 36V
BOOST Voltage Above SW1 ..... 25V
BIAS Pin Voltage 18V
SW2, SW4 Pin Voltages 40V
SW3 Voltage 40V
FB1, FB2, FB3, FB4 Voltages 4V
NFB4 Voltage ..... +6V, –0.6V
VC1, VC2, VC3, VC4 Pin Voltages 6V
RUN-SS, SS-234 Pin Voltages 6V
PGOOD Pin Voltage 36V
E3 Pin Voltage 38V
V_{ON} Voltage 38V
C_T Pin Voltage 6V
Junction Temperature ..... 125°C
Operating Temperature Range (Note 2) ... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



FE PACKAGE
28-LEAD PLASTIC TSSOP
EXPOSED PAD (PIN 29) IS GROUND
(MUST BE SOLDERED TO PCB)

T_{JMAX} = 125°C, θ_{JA} = 25°C/W, θ_{JC} = 7.5°C/W

ORDER PART NUMBER
LT1943EFE
FE PART MARKING
1943E

Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●			4.5	V
Maximum Input Voltage					22	V
Quiescent Current	Not Switching RUN-SS = SS-234 = 0V			10 35	14 45	mA µA
RUN-SS, SS-234 Pin Current	RUN-SS, SS-234 = 0.4V			1.7		µA
RUN-SS, SS-234 Threshold				0.8		V
BIAS Pin Voltage to Begin SS-234 Charge		●	2.4	2.8	3.15	V
BIAS Pin Current	BIAS = 3.1V, All Switches Off			10.5	15	mA
FB Threshold Offset to Begin C_T Charge	(Note 3)		90	125	160	mV
C_T Pin Current Source	All FB Pins = 1.5V		16	20	25	µA
C_T Threshold to Power V_{ON}	All FB Pins = 1.5V		1.0	1.1	1.2	V
V_{ON} Switch Drop	V_{ON} Current = 30mA			180	240	mV
Maximum V_{ON} Current	V_{E3} = 30V	●	30	60		mA
PGOOD Threshold Offset			90	125	160	mV
PGOOD Sink Current			200			µA
PGOOD Pin Leakage	V_{PGOOD} = 36V				1	µA
Master Oscillator Frequency		 ●	1.1 1.0	1.2	1.35 1.46	MHz MHz
Foldback Switching Frequency	All FB Pins = 0V			250		kHz
Frequency Shift Threshold on FB	Δ200kHz			0.5		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH 1 (2.4A BUCK)						
FB1 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB1 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB1 Pin Bias Current	(Note 4)	●		100	600	nA
Error Amplifier 1 Voltage Gain				200		V/V
Error Amplifier 1 Transconductance	ΔI = 5μA			450		μmhos
Switch 1 Current Limit	Duty Cycle = 35% (Note 6)	●	2.4	3.2	4.3	A
Switch 1 V_{CESAT}	I_{SW} = 2A			310	470	mV
Switch 1 Leakage Current	FB1 = 1.5V			0.1	10	μA
Minimum BOOST Voltage Above SW1 Pin	I_{SW} = 1.5A (Note 7)			1.8	2.5	V
BOOST Pin Current	I_{SW} = 1.5A			30	50	mA
Maximum Duty Cycle (SW1)		●	82	92		%
SWITCH 2 (2.6A BOOST)						
FB2 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB2 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB2 Pin Bias Current	(Note 4)	●		220	1000	nA
Error Amplifier 2 Voltage Gain				200		V/V
Error Amplifier 2 Transconductance	ΔI = 5μA			450		μmhos
Switch 2 Current Limit		●	2.6	3.8	4.9	A
Switch 2 V_{CESAT}	I_{SW2} = 2A			360	540	mV
Switch 2 Leakage Current	FB2 = 1.5V			0.1	1	μA
BIAS Pin Current	I_{SW2} = 2A			45		mA
Maximum Duty Cycle (SW2)		●	85	92		%
SWITCH 3 (350mA BOOST)						
FB3 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB3 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB3 Pin Bias Current	(Note 4)	●		100	600	nA
Error Amplifier 3 Voltage Gain				200		V/V
Error Amplifier 3 Transconductance	ΔI = 5μA			450		μmhos
Switch 3 Current Limit		●	0.35	0.5	0.7	A
Switch 3 V_{CESAT}	I_{SW3} = 0.2A			180	280	mV
Switch 3 Leakage Current	FB3 = 1.5V			0.1	1	μA
BIAS Pin Current	I_{SW3} = 0.2A			14		mA
Maximum Duty Cycle (SW3)		 ●	84 83	88		% %
Schottky Diode Drop	I = 170mA			700		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. RUN-SS, SS-234 = 2.5V unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SWITCH 4 (350mA INVERTER)						
FB4 Voltage		 ●	1.23 1.22	1.25	1.27 1.27	V V
FB4 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
FB4 Pin Bias Current	(Note 4)	●		100	600	nA
NFB4 Voltage (V_{FB4}-V_{NFB4})		 ●	1.215 1.205	1.245	1.275 1.275	V V
NFB4 Voltage Line Regulation	4.5V < V_{IN} < 22V			0.01	0.03	%/V
NFB4 Pin Bias Current	(Note 5)			100	600	nA
Error Amplifier 4 Voltage Gain				200		V/V
Error Amplifier 4 Transconductance	ΔI = 5μA			450		μmhos
Switch 4 Current Limit		●	0.35	0.5	0.7	A
Switch 4 V_{CESAT}	I_{SW4} = 0.3A			260	390	mV
Switch 4 Leakage Current	FB4 = 1.5V			0.1	1	μA
BIAS Pin Current due to SW4	I_{SW4} = 0.3A			15		mA
Maximum Duty Cycle (SW4)		 ●	84 83	88		% %

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: The LT1943E is guaranteed to meet performance specifications from 0°C to 70°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization, and correlation with statistical process controls.

Note 3: The C_T pin is held low until FB1, FB2, FB3 and FB4 all ramp above the FB threshold offset.

Note 4: Current flows into FB1, FB2, FB3 and FB4 pins.

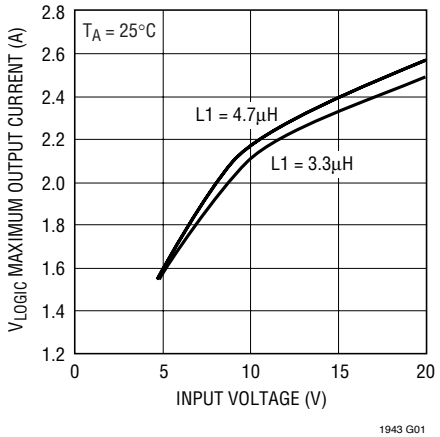
Note 5: Current flows out of NFB4 pin.

Note 6: Current limit is guaranteed by design and/or correlation to static test. Slope compensation reduces current limit at high duty cycle.

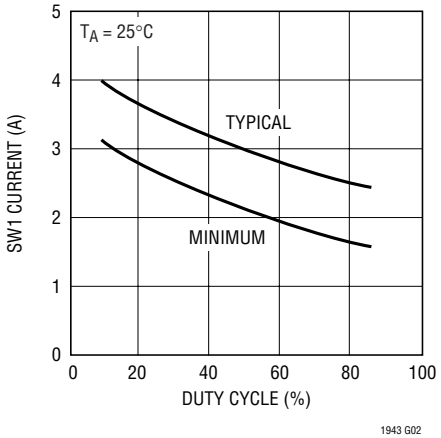
Note 7: This is the minimum voltage across the boost capacitor needed to guarantee full saturation of the internal power switch.

TYPICAL PERFORMANCE CHARACTERISTICS

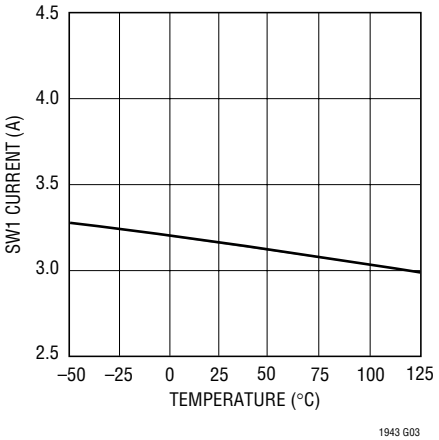
Maximum Output Current for V_{LOGIC} = 3.3V



SW1 Current Limit vs Duty Cycle

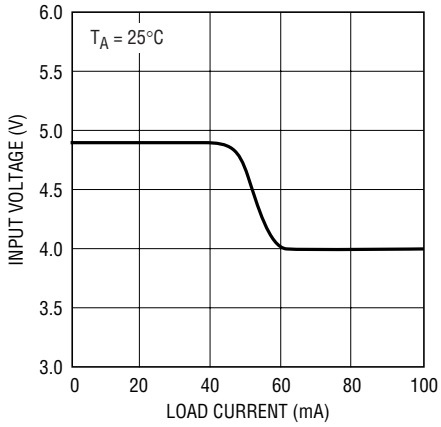


SW1 Current Limit



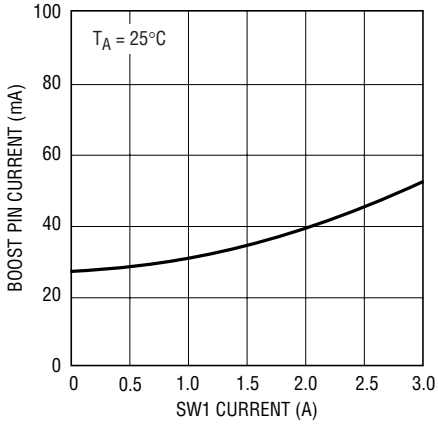
TYPICAL PERFORMANCE CHARACTERISTICS

MINIMUM Input Voltage to Start, V_{LOGIC} = 3.3V



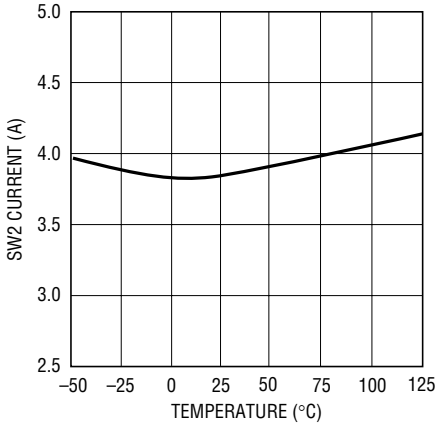
1943 G04

BOOST Pin Current



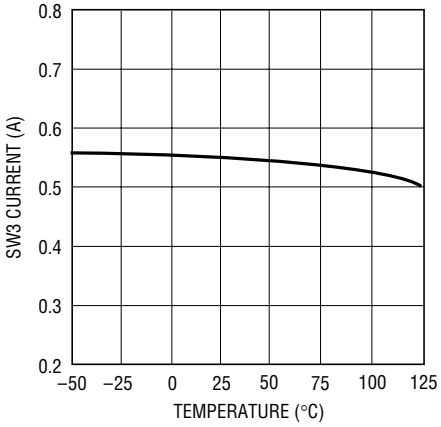
1943 G05

SW2 Current Limit



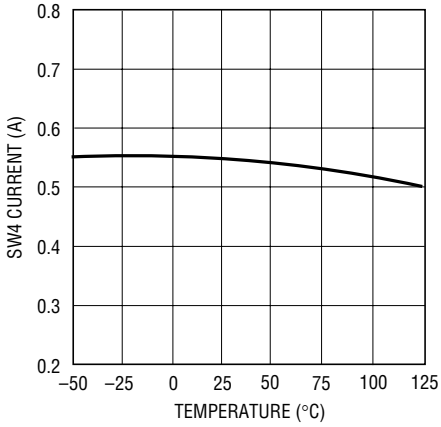
1943 G06

SW3 Current Limit



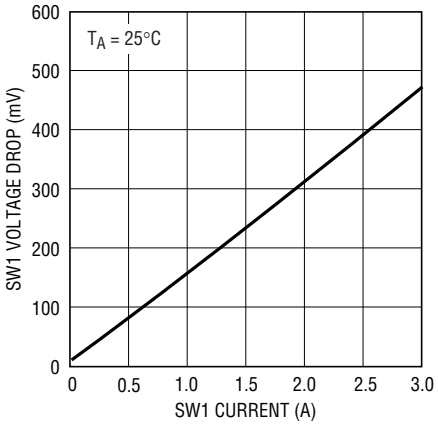
1943 G07

SW4 Current Limit



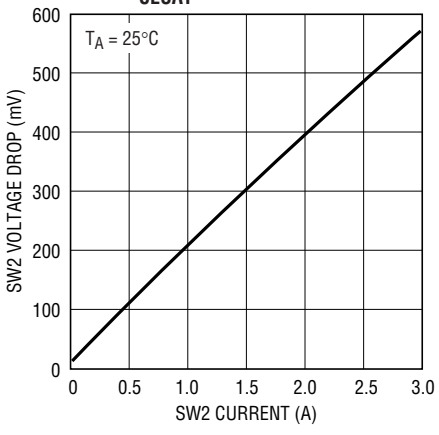
1943 G08

SW1 V_{CESAT}



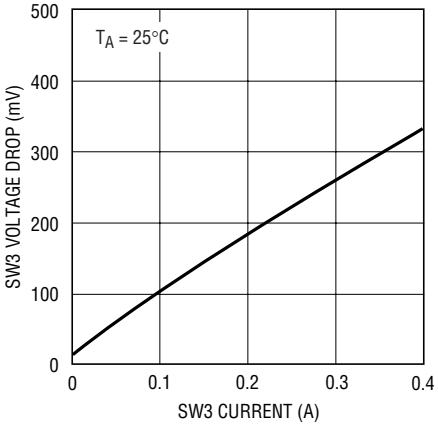
1943 G09

SW2 V_{CESAT}



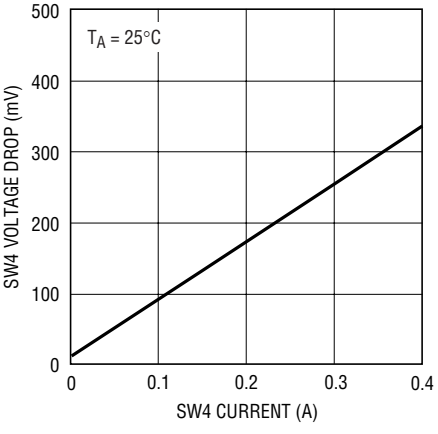
1943 G10

SW3 V_{CESAT}



1943 G11

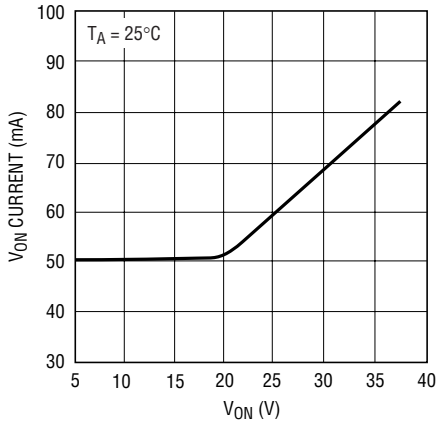
SW4 V_{CESAT}



1943 G12

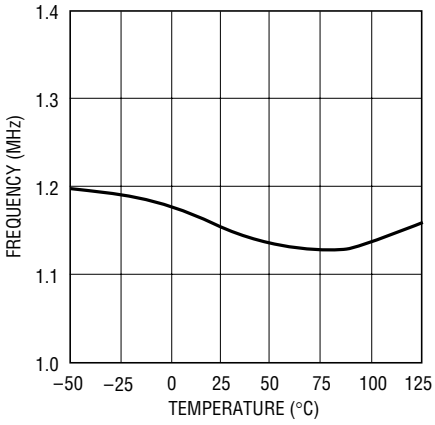
TYPICAL PERFORMANCE CHARACTERISTICS

V_{ON} Current Limit



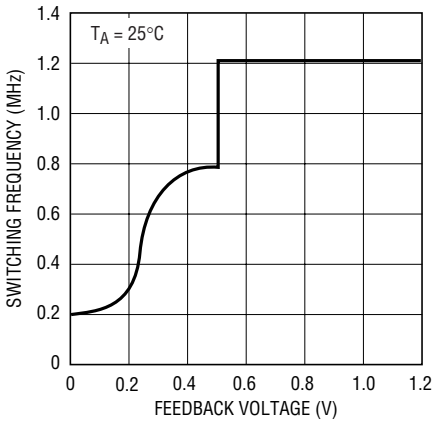
1943 G13

Oscillator Frequency



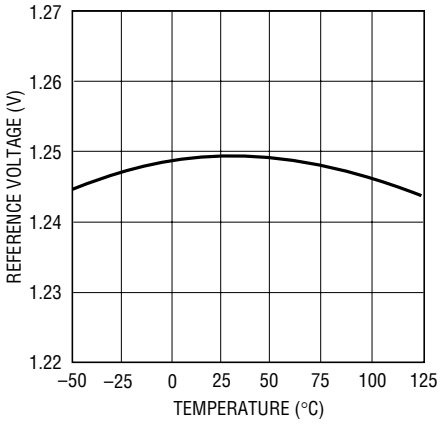
1943 G14

Frequency Foldback



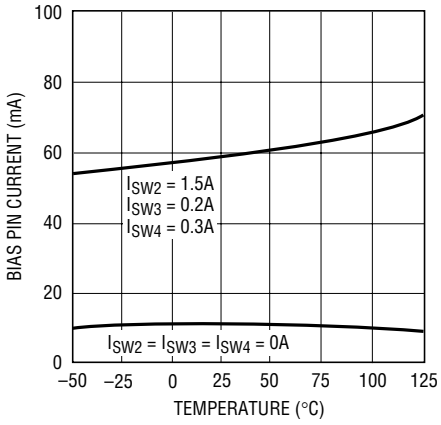
1943 G15

Reference Voltage



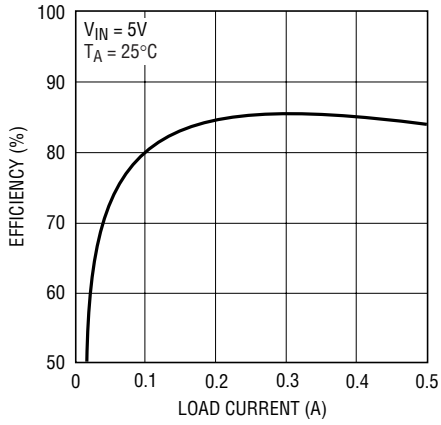
1943 G16

Bias Pin Current



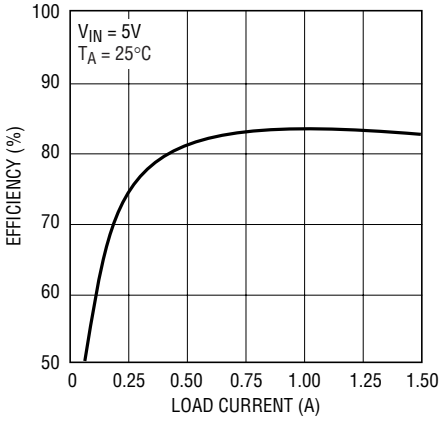
1943 G17

Efficiency, AV_{DD} = 13V



1943 G18

Efficiency, V_{LOGIC} = 3.3V



1943 G19

PIN FUNCTIONS

GND (Pins 1, 20, Exposed Pad Pin 29): Ground. Tie both GND pins and the exposed pad directly to a local ground plane. The ground metal to the exposed pad should be as wide as possible for better heat dissipation. Multiple vias (to ground plane under the ground backplane) placed close to the exposed pad can further aid in reducing thermal resistance.

VC1 (Pin 2): Switching Regulator 1 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

VC2 (Pin 3): Error Amplifier Compensation for Switcher 2. Connect a resistor/capacitor network in series with this pin.

FB1 (Pin 4): Switching Regulator 1 Feedback. Tie the resistor divider tap to this pin and set V_{LOGIC} according to $V_{LOGIC} = 1.25 \bullet (1 + R2/R1)$. Reference designators refer to Figure 1.

FB2 (Pin 5): Feedback for Switch 2. Tie the resistor divider tap to this pin and set AV_{DD} according to $AV_{DD} = 1.25 \bullet (1 + R6/R5)$.

FB3 (Pin 6): Switching Regulator 3 Feedback. Tie the resistor divider tap to this pin and set V_{ON} according to $V_{ON} = 1.25 \bullet (1 + R9/R8) – 150mV$.

NFB4 (Pin 7): Switching Regulator 4 Negative Feedback. Switcher 4 can be used to generate a positive or negative output. When regulating a negative output, tie the resistor divider tap to this pin. Negative output voltage can be set by the equation $V_{OFF} = –1.245 \bullet (R3/R4)$ with R4 set to 10k. Tie the NFB4 pin to FB4 for positive output voltages.

FB4 (Pin 8): Feedback for Switch 4. When generating a positive voltage from switch 4, tie the resistor divider tap to this pin. When generating a negative voltage, tie a 10k resistor between FB4 and NFB4 (R4).

VC3 (Pin 9): Switching Regulator 3 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

VC4 (Pin 10): Switching Regulator 4 Error Amplifier Compensation. Connect a resistor/capacitor network in series with this pin.

SGND (Pin 11): Signal Ground. Return ground trace from the FB resistor networks and V_C pin compensation components directly to this pin and then tie to ground.

BOOST (Pin 12): The BOOST pin is used to provide a drive voltage, higher than V_{IN}, to the switch 1 drive circuit.

SW1 (Pins 13, 14): The SW1 pins are the emitter of the internal NPN bipolar power transistor for switching regulator 1. These pins must be tied together for proper operation. Connect these pins to the inductor, catch diode and boost capacitor.

V_{IN} (Pins 15, 16): The V_{IN} pins supply current to the LT1943's internal regulator and to the internal power transistor for switch 1. These pins must be tied together and locally bypassed.

SS-234 (Pin 17): This is the soft-start pin for switching regulators 2, 3 and 4. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When the BIAS pin reaches 2.8V, a 1.7μA current source begins charging the capacitor. When the capacitor voltage reaches 0.8V, switches 2, 3 and 4 turn on and begin switching. For slower start-up, use a larger capacitor. When this pin is pulled to ground, switches 2, 3 and 4 are disabled. For complete shutdown, tie RUN-SS to ground.

RUN-SS (Pin 18): This is the soft-start pin for switching regulator 1. Place a soft-start capacitor here to limit start-up inrush current and output voltage ramp rate. When power is applied to the V_{IN} pin, a 1.7μA current source charges the capacitor. When the voltage at this pin reaches 0.8V, switch 1 turns on and begins switching. For slower start-up, use a larger capacitor. For complete shutdown, tie RUN-SS to ground.

SW4 (Pin 19): This is the collector of the internal NPN bipolar power transistor for switching regulator 4. Minimize metal trace area at this pin to keep EMI down.

PIN FUNCTIONS

SW3 (Pin 21): This is the collector of the internal NPN bipolar power transistor for switching regulator 3. Minimize metal trace area at this pin to keep EMI down.

BIAS (Pin 22): The BIAS pin is used to improve efficiency when operating at higher input voltages. Connecting this pin to the output of switching regulator 1 forces most of the internal circuitry to draw its operating current from V_{LOGIC} rather than V_{IN}. The drivers of switches 2, 3 and 4 are supplied by BIAS. Switches 2, 3 and 4 will not switch until the BIAS pin reaches approximately 2.8V. BIAS must be tied to V_{LOGIC}.

PGOOD (Pin 23): Power Good Comparator Output. This is the open collector output of the power good comparator and can be used in conjunction with an external P-Channel MOSFET to provide output disconnect for AV_{DD} as shown in the 5V Input, Quad Output TFT-LCD Power Supply on the last page of the data sheet. When switcher 2's output reaches approximately 90% of its programmed voltage, PGOOD will be pulled to ground. This will pull down on the gate of the MOSFET, connecting AV_{DD}. A 100k pull-up resistor between the source and gate of the P-channel MOSFET keeps it off when switcher 2's output is low.

E3 (Pin 24): This is switching regulator 3's output and the emitter of the output disconnect PNP. Tie the output capacitor and resistor divider here.

C_T (Pin 25): Timing Capacitor Pin. This is the input to the V_{ON} timer and programs the time delay from all four feedback pins reaching 1.125V to V_{ON} turning on. The C_T capacitor value can be set using the equation $C = (20\mu A \bullet t_{DELAY})/1.1V$.

V_{ON} (Pin 26): This is the delayed output for switching regulator 3. V_{ON} reaches its programmed voltage after the internal C_T timer times out. Protection circuitry ensures V_{ON} is disabled if any of the four outputs are more than 10% below normal voltage.

SW2 (Pins 27, 28): The SW2 pins are the collector of the internal NPN bipolar power transistor for switching regulator 2. These pins must be tied together. Minimize trace area at these pins to keep EMI down.

BLOCK DIAGRAM

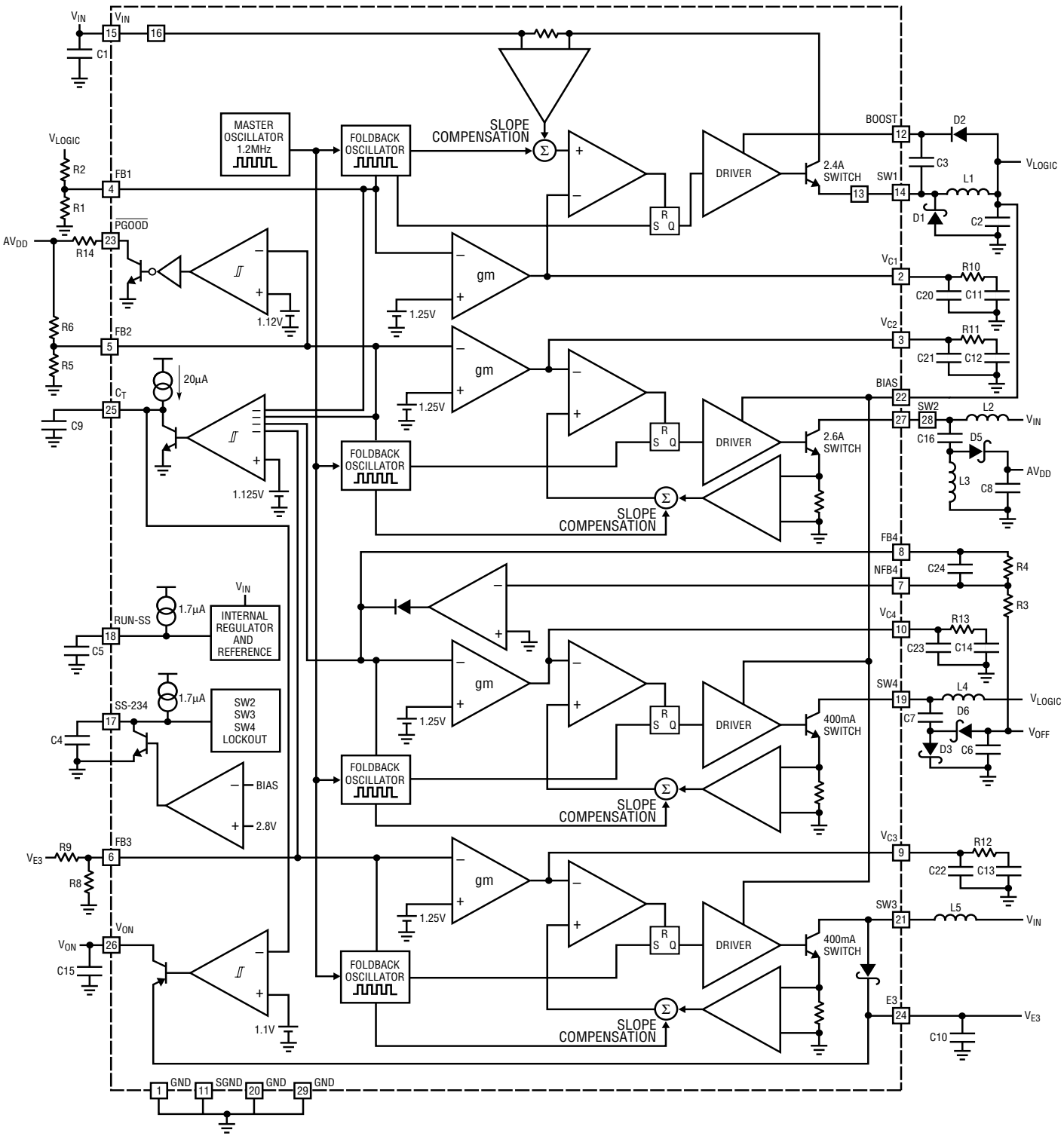


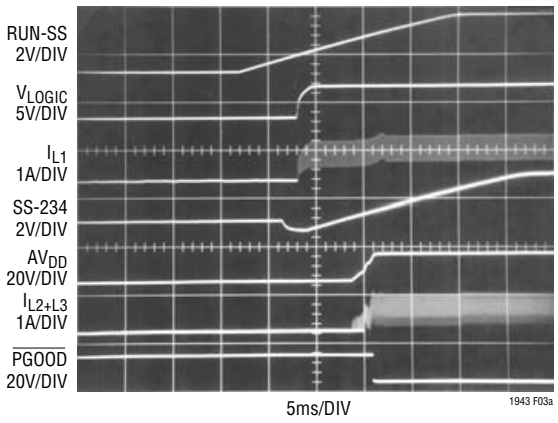
Figure 1. Block Diagram

OPERATION

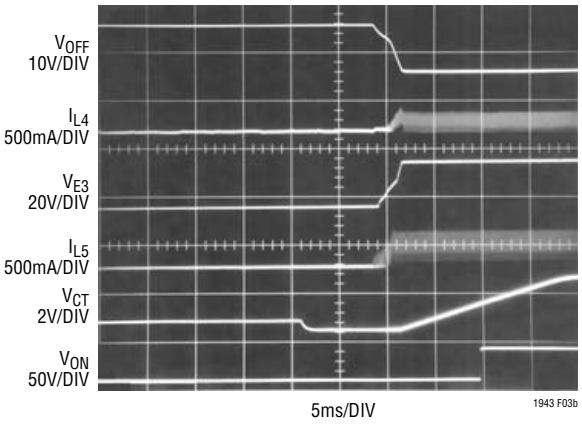
The LT1943 is a highly integrated power supply IC containing four separate switching regulators. All four switching regulators have their own oscillator with frequency foldback and use current mode control. Switching regulator 1 consists of a step-down regulator with a switch current limit of 2.4A. Switching regulator 2 can be configured as a step-up or SEPIC converter and has a 2.6A switch. Switching regulator 3 consists of a step-up regulator with a 0.35A switch as well as an integrated Schottky diode. Switching regulator 4 has two feedback pins (FB4 and NFB4) and can directly regulate positive or negative output voltages. The four regulators share common circuitry including input source, voltage reference, and master oscillator. Operation can be best understood by referring to the Block Diagram as shown in Figure 1.

If the RUN/SS pin is pulled to ground, the LT1943 is shut down and draws 35μA from the input source tied to V_{IN}. An internal 1.7μA current source charges the external soft-start capacitor, generating a voltage ramp at this pin. If the RUN/SS pin exceeds 0.6V, the internal bias circuits turn on, including the internal regulator, reference, and 1.1MHz master oscillator. The master oscillator generates four clock signals, one for each of the switching regulators. Switching regulator 1 will only begin to operate when the RUN/SS pin reaches 0.8V. Switcher 1 generates V_{LOGIC}, which must be tied to the BIAS pin. When BIAS reaches 2.8V, the NPN pulling down on the SS-234 pin turns off, allowing an internal 1.7μA current source to charge the external capacitor tied to the SS-234 pin. When the voltage on the SS-234 pin reaches 0.8V, switchers 2, 3 and 4 are enabled. AV_{DD} and V_{OFF} will then begin rising at a ramp rate determined by the capacitor tied to the SS-234 pin. When all the outputs reach 90% of their programmed voltages, the NPN pulling down on the C_T pin will turn off, and an internal 20μA current source will charge the external capacitor tied to the C_T pin. When the C_T pin reaches 1.1V, the output disconnect PNP turns on, connecting V_{ON}. In the event of any of the four outputs dropping below 10% of their programmed voltage, PanelProtect circuitry pulls the C_T pin to GND, disabling V_{ON}.

A power good comparator monitors AV_{DD} and turns on when the FB2 pin is at or above 90% of its regulated value.



(2a)



(2b)

Figure 2. LT1943 Power-Up Sequence. (Traces From Both Photos are Synchronized to the Same Trigger)

The output is an open collector transistor that is off when the output is out of regulation, allowing an external resistor to pull the pin high. This pin can be used with a P-channel MOSFET that functions as an output disconnect for AV_{DD}.

The four switchers are current mode regulators. Instead of directly modulating the duty cycle of the power switch, the feedback loop controls the peak current in the switch during each cycle. Compared to voltage mode control, current mode control improves loop dynamics and provides cycle-by-cycle current limit.

OPERATION

The control loop for the four switchers is similar. A pulse from the slave oscillator sets the RS latch and turns on the internal NPN bipolar power switch. Current in the switch and the external inductor begins to increase. When this current exceeds a level determined by the voltage at V_C, the current comparator resets the latch, turning off the switch. The current in the inductor flows through the Schottky diode and begins to decrease. The cycle begins again at the next pulse from the oscillator. In this way, the voltage on the V_C pin controls the current through the inductor to the output. The internal error amplifier regulates the output voltage by continually adjusting the V_C pin voltage. The threshold for switching on the V_C pin is 0.8V, and an active clamp of 1.8V limits the output current. The RUN/SS and SS-234 pins also clamp the V_C pin voltage. As the internal current source charges the external soft-start capacitor, the current limit increases slowly.

Each switcher contains an extra, independent oscillator to perform frequency foldback during overload conditions. This slave oscillator is normally synchronized to the master oscillator. A comparator senses when V_{FB} is less than 0.5V and switches the regulator from the master oscillator to a slower slave oscillator. The V_{FB} pin is less than 0.5V during startup, short-circuit, and overload conditions. Frequency foldback helps limit switch current and power dissipation under these conditions.

The switch driver for SW1 operates either from V_{IN} or from the BOOST pin. An external capacitor and diode are used to generate a voltage at the BOOST pin that is higher than the input supply. This allows the driver to saturate the internal bipolar NPN power switch for efficient operation.

STEP-DOWN CONSIDERATIONS

FB Resistor Network

The output voltage for switcher 1 is programmed with a resistor divider (refer to the Block Diagram) between the output and the FB pin. Choose the resistors according to:

$$R2 = R1(V_{OUT}/1.25V - 1)$$

R1 should be 10kΩ or less to avoid bias current errors.

Input Voltage Range

The minimum operating voltage of switcher 1 is determined either by the LT1943's undervoltage lockout of ~4V, or by its maximum duty cycle. The duty cycle is the fraction of time that the internal switch is on and is determined by the input and output voltages:

$$DC = (V_{OUT} + V_F)/(V_{IN} - V_{SW} + V_F)$$

where V_F is the forward voltage drop of the catch diode (~0.4V) and V_{SW} is the voltage drop of the internal switch (~0.3V at maximum load). This leads to a minimum input voltage of

$$V_{IN(MIN)} = (V_{OUT} + V_F)/DC_{MAX} - V_F + V_{SW}$$

with $DC_{MAX} = 0.82$.

Inductor Selection and Maximum Output Current

A good first choice for the inductor value is:

$$L = (V_{OUT} + V_F)/1.2$$

where V_F is the voltage drop of the catch diode (~0.4V) and L is in μH. The inductor's RMS current rating must be greater than the maximum load current and its saturation current should be at least 30% higher. For highest efficiency, the series resistance (DCR) should be less than 0.1Ω. Table 1 lists several vendors and types that are suitable.

The optimum inductor for a given application may differ from the one indicated by this simple design guide. A larger value inductor provides a higher maximum load current, and reduces the output voltage ripple. If your load is lower than the maximum load current, then you can relax the value of the inductor and operate with higher ripple current. This allows you to use a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that the maximum load current depends on input voltage. A graph in the Typical Performance section of this data sheet shows the maximum load current as a function of input voltage and inductor value for $V_{OUT} = 3.3V$. In addition, low inductance may result in discontinuous mode operation, which further reduces

OPERATION

maximum load current. For details of maximum output current and discontinuous mode operation, see Linear Technology's Application Note AN44. Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid subharmonic oscillations. See AN19.

The current in the inductor is a triangle wave with an average value equal to the load current. The peak switch current is equal to the output current plus half the peak-to-peak inductor ripple current. The LT1943 limits its switch current in order to protect itself and the system from overload faults. Therefore, the maximum output current that the LT1943 will deliver depends on the switch current limit, the inductor value, and the input and output voltages.

When the switch is off, the potential across the inductor is the output voltage plus the catch diode drop. This gives the peak-to-peak ripple current in the inductor:

$$\Delta I_L = (1 - DC)(V_{OUT} + V_F)/(L \bullet f),$$

where f is the switching frequency of the LT1943 and L is the value of the inductor. The peak inductor and switch current is

$$I_{SWPK} = I_{LPK} = I_{OUT} + \Delta I_L/2$$

To maintain output regulation, this peak current must be less than the LT1943's switch current limit of I_{LIM}. For SW1, I_{LIM} is at least 2.4A at DC = 0.35 and decreases linearly to 1.6A at DC = 0.8, as shown in the Typical Performance Characteristics section. The maximum output current is a function of the chosen inductor value:

$$I_{OUT(MAX)} = I_{LIM} - \Delta I_L/2$$
$$= 3A \bullet (1 - 0.57 \bullet DC) - \Delta I_L/2$$

Choosing an inductor value so that the ripple current is small will allow a maximum output current near the switch current limit.

One approach to choosing the inductor is to start with the simple rule given above, look at the available inductors, and choose one to meet cost or space goals. Then use these equations to check that the LT1943 will be able to deliver the required output current. Note again that these equations assume that the inductor current is continuous. Discontinuous operation occurs when I_{OUT} is less than $\Delta I_L/2$.

Table 1. Inductors.

Part Number	Value (µH)	I_{RMS} (A)	DCR (Ω)	Height (mm)
Sumida				
CR43-1R4	1.4	2.52	0.056	3.5
CR43-2R2	2.2	1.75	0.071	3.5
CR43-3R3	3.3	1.44	0.086	3.5
CR43-4R7	4.7	1.15	0.109	3.5
CDRH3D16-1R5	1.5	1.55	0.040	1.8
CDRH3D16-2R2	2.2	1.20	0.050	1.8
CDRH3D16-3R3	3.3	1.10	0.063	1.8
CDRH4D28-3R3	3.3	1.57	0.049	3.0
CDRH4D28-4R7	4.7	1.32	0.072	3.0
CDRH4D18-1R0	1.0	1.70	0.035	2.0
CDC5D23-2R2	2.2	2.50	0.03	2.5
CDRH5D28-2R6	2.6	2.60	0.013	3.0
Coilcraft				
DO1606T-152	1.5	2.10	0.060	2.0
DO1606T-222	2.2	1.70	0.070	2.0
DO1606T-332	3.3	1.30	0.100	2.0
DO1606T-472	4.7	1.10	0.120	2.0
DO1608C-152	1.5	2.60	0.050	2.9
DO1608C-222	2.2	2.30	0.070	2.9
DO1608C-332	3.3	2.00	0.080	2.9
DO1608C-472	4.7	1.50	0.090	2.9
MOS6020-222	2.2	2.15	0.035	2.0
MOS6020-332	3.3	1.8	0.046	2.0
MOS6020-472	4.7	1.5	0.050	2.0
D03314-222	2.2	1.6	0.200	1.4
1008PS-272	2.7	1.3	0.140	2.7
Toko				
(D62F)847FY-2R4M	2.4	2.5	0.037	2.7
(D73LF)817FY-2R2M	2.2	2.7	0.03	3.0

OPERATION

Output Capacitor Selection

For 5V and 3.3V outputs, a 10µF 6.3V ceramic capacitor (X5R or X7R) at the output results in very low output voltage ripple and good transient response. Other types and values will also work; the following discussion explores tradeoffs in output ripple and transient performance.

The output capacitor filters the inductor current to generate an output with low voltage ripple. It also stores energy in order satisfy transient loads and stabilizes the LT1943's control loop. Because the LT1943 operates at a high frequency, minimal output capacitance is necessary. In addition, the control loop operates well with or without the presence of output capacitor series resistance (ESR). Ceramic capacitors, which achieve very low output ripple and small circuit size, are therefore an option.

You can estimate output ripple with the following equations:

$V_{RIPPLE} = \Delta I_L/(8 \bullet f \bullet C_{OUT})$ for ceramic capacitors, and

$V_{RIPPLE} = \Delta I_L \bullet ESR$ for electrolytic capacitors (tantalum and aluminum);

where ΔI_L is the peak-to-peak ripple current in the inductor. The RMS content of this ripple is very low so the RMS current rating of the output capacitor is usually not of concern. It can be estimated with the formula:

$$I_{C(RMS)} = \Delta I_L/\sqrt{12}$$

Another constraint on the output capacitor is that it must have greater energy storage than the inductor; if the stored energy in the inductor transfers to the output, the resulting voltage step should be small compared to the regulation voltage. For a 5% overshoot, this requirement indicates:

$$C_{OUT} > 10 \bullet L \bullet (I_{LIM}/V_{OUT})^2$$

The low ESR and small size of ceramic capacitors make them the preferred type for LT1943 applications. Not all ceramic capacitors are the same, however. Many of the higher value capacitors use poor dielectrics with high temperature and voltage coefficients. In particular, Y5V and Z5U types lose a large fraction of their capacitance with applied voltage and at temperature extremes. Because loop stability and transient response depend on the value of C_{OUT}, this loss may be unacceptable. Use X7R and X5R types.

Electrolytic capacitors are also an option. The ESRs of most aluminum electrolytic capacitors are too large to deliver low output ripple. Tantalum and newer, lower ESR organic electrolytic capacitors intended for power supply use are suitable, and the manufacturers will specify the ESR. Chose a capacitor with a low enough ESR for the required output ripple. Because the volume of the capacitor determines its ESR, both the size and the value will be larger than a ceramic capacitor that would give similar ripple performance. One benefit is that the larger capacitance may give better transient response for large changes in load current. Table 2 lists several capacitor vendors.

Table 2. Low ESR Surface Mount Capacitors

Vendor	Type	Series
Taiyo Yuden	Ceramic	X5R, X7R
AVX	Ceramic Tantalum	X5R, X7R TPS
Kemet	Tantalum Ta Organic Al Organic	T491, T494, T495 T520 A700
Sanyo	Ta or Al Organic	POSCAP
Panasonic	Al Organic	SP CAP
TDK	Ceramic	X5R, X7R

Diode Selection

The catch diode (D1 from Figure 1) conducts current only during switch off time. Average forward current in normal operation can be calculated from:

$$I_{D(AVG)} = I_{OUT} (V_{IN} - V_{OUT})/V_{IN}$$

The only reason to consider a diode with a larger current rating than necessary for nominal operation is for the worst-case condition of shorted output. The diode current will then increase to the typical peak switch current.

Peak reverse voltage is equal to the regulator input voltage. Use a diode with a reverse voltage rating greater than the input voltage. Table 3 lists several Schottky diodes and their manufacturers.

OPERATION

Table 3. Schottky Diodes

Part Number	V_R (V)	I_{AVE} (A)	V_F at 1A (mV)	V_F at 2A (mV)
On Semiconductor				
MBRM120E	20	1	530	595
MBRM140	40	1	550	
Diodes Inc.				
B120	20	1	500	
B130	30	1	500	
B220	20	2		500
B230	30	2		500
B240	40	2		500
International Rectifier				
10BQ030	30	1	420	470
20BQ030	30	2		470

Boost Pin Considerations

The minimum operating voltage of an LT1943 application is limited by the undervoltage lockout ~4V and by the maximum duty cycle. The boost circuit also limits the minimum input voltage for proper start-up. If the input voltage ramps slowly, or the LT1943 turns on when the output is already in regulation, the boost capacitor may not be fully charged. Because the boost capacitor charges with the energy stored in the inductor, the circuit will rely on some minimum load current to get the boost circuit running properly. This minimum load will depend on input and output voltages. The Typical Performance Characteristics section shows a plot of the minimum load current to start as a function of input voltage for a 3.3V output. The minimum load current generally goes to zero once the circuit has started. Even without an output load current, in many cases the discharged output capacitor will present a load to the switcher that will allow it to start.

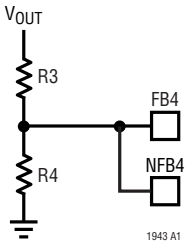
INVERTER/STEP-UP CONSIDERATIONS

Regulating Positive Output Voltages

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistors according to:

$$R3 = R4(V_{OUT}/1.25 - 1)$$

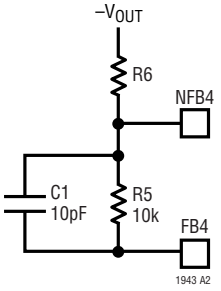
R4 should be 10kΩ or less to avoid bias current errors. If switcher 4 is used to generate a positive output voltage, NFB4 should be tied to FB4.



Regulating Negative Output Voltages

The LT1943 contains an inverting op amp with its non-inverting terminal tied to ground and its output connected to the FB4 pin. Use this op amp to generate a voltage at FB4 that is proportional to V_{OUT4}. Choose the resistors according to:

$$R6 = \frac{R5 \bullet |V_{OUT}|}{1.245V}$$



Use 10k for R5. Tie 10pF in parallel with R5.

Duty Cycle Range

The maximum duty cycle (DC) of the LT1943 switching regulator is 85% for SW2, and 83% for SW3 and SW4. The duty cycle for a given application using the step-up or charge pump topology is:

$$DC = \frac{|V_{OUT}| - V_{IN}}{|V_{OUT}|}$$

The duty cycle for a given application using the inverter or SEPIC topology is:

OPERATION

$$DC = \frac{|V_{OUT}|}{V_{IN} + |V_{OUT}|}$$

The LT1943 can still be used in applications where the duty cycle, as calculated above, is above the maximum. However, the part must be operated in discontinuous mode so that the actual duty cycle is reduced.

Inductor Selection

Several inductors that work well with the LT1943 regulator are listed in Table 4. Besides these, many other inductors will work. Consult each manufacturer for detailed information and for their entire selection of related parts. Use ferrite core inductors to obtain the best efficiency, as core losses at frequencies above 1MHz are much lower for ferrite cores than for powdered-iron units. A 10µH to 22µH inductor will be the best choice for most LT1943 step-up and charge pump designs. Choose an inductor that can carry the entire switch current without saturating. For inverting and SEPIC regulators, a coupled inductor, or two separate inductors is an option. When using coupled inductors, choose one that can handle at least the switch current without saturating. If using uncoupled inductors, each inductor need only handle approximately one-half of the total switch current. A 4.7µH to 15µH coupled inductor or two 10µH to 22µH uncoupled inductors will usually be the best choice for most LT1943 inverting and SEPIC designs.

Table 4. Inductors.

Part Number	Value (µH)	I_{RMS} (A)	DCR (Ω)	Height (mm)
Coiltronics				
TP3-4R7	4.7	1.5	0.181	2.2
TP4-100	10	1.5	0.146	3.0
Sumida				
CD73-100	10	1.44	0.080	3.5
CDRH5D18-6R2	6.2	1.4	0.071	2.0
CDRH4D28-100	10	1.3	0.048	3.0
CDRH4D28-100	10	1.0	0.095	3.0
Coilcraft				
DO3314-103	10	0.8	0.520	1.4
1008PS-103	10	0.78	0.920	2.8

Output Capacitor Selection

Use low ESR (equivalent series resistance) capacitors at the output to minimize the output ripple voltage. Multilayer ceramic capacitors are an excellent choice, as they have an extremely low ESR and are available in very small packages. X7R dielectrics are preferred, followed by X5R, as these materials retain their capacitance over wide voltage and temperature ranges. A 10µF to 22µF output capacitor is sufficient for most LT1943 applications. Even less capacitance is required for outputs with $|V_{OUT}| > 20V$ or $|I_{OUT}| < 100mA$. Solid tantalum or OS-CON capacitors will also work, but they will occupy more board area and will have a higher ESR than a ceramic capacitor. Always use a capacitor with a sufficient voltage rating.

Diode Selection

A Schottky diode is recommended for use with the LT1943 switcher 2 and switcher 4. The Schottky diode for switcher 3 is integrated inside the LT1943. Choose diodes for switcher 2 and switcher 4 rated to handle an average current greater than the load current and rated to handle the maximum diode voltage. The average diode current in the step-up, SEPIC, and inverting configurations is equal to the load current. Each of the two diodes in the charge pump configurations carries an average diode current equal to the load current. The maximum diode voltage in the step-up and charge pump configurations is equal to $|V_{OUT}|$. The maximum diode voltage in the SEPIC and inverting configurations is $V_{IN} + |V_{OUT}|$.

Input Capacitor Selection

Bypass the input of the LT1943 circuit with a 4.7µF or higher ceramic capacitor of X7R or X5R type. A lower value or a less expensive Y5V type will work if there is additional bypassing provided by bulk electrolytic capacitors or if the input source impedance is low. The following paragraphs describe the input capacitor considerations in more detail.

Step-down regulators draw current from the input supply in pulses with very fast rise and fall times. The input capacitor is required to reduce the resulting voltage ripple at the LT1943 input and to force this switching current into a tight local loop, minimizing EMI. The input capacitor

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must have low impedance at the switching frequency to do this effectively and it must have an adequate ripple current rating. The input capacitor RMS current can be calculated from the step-down output voltage and current, and the input voltage:

$$C_{INRMS} = I_{OUT} \bullet \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} < \frac{I_{OUT}}{2}$$

and is largest when V_{IN} = 2 V_{OUT} (50% duty cycle). The ripple current contribution from the other channels will be minimal. Considering that the maximum load current from switcher 1 is ~2.8A, RMS ripple current will always be less than 1.4A.

The high frequency of the LT1943 reduces the energy storage requirements of the input capacitor, so that the capacitance required is less than 10µF. The combination of small size and low impedance (low equivalent series resistance or ESR) of ceramic capacitors makes them the preferred choice. The low ESR results in very low voltage ripple. Ceramic capacitors can handle larger magnitudes of ripple current than other capacitor types of the same value. Use X5R and X7R types.

An alternative to a high value ceramic capacitor is a lower value along with a larger electrolytic capacitor, for example a 1µF ceramic capacitor in parallel with a low ESR tantalum capacitor. For the electrolytic capacitor, a value larger than 10µF will be required to meet the ESR and ripple current requirements. Because the input capacitor is likely to see high surge currents when the input source is applied, only consider a tantalum capacitor if it has the appropriate surge current rating. The manufacturer may also recommend operation below the rated voltage of the capacitor. Be sure to place the 1µF ceramic as close as possible to the V_{IN} and GND pins on the IC for optimal noise immunity.

A final caution is in order regarding the use of ceramic capacitors at the input. A ceramic input capacitor can combine with stray inductance to form a resonant tank circuit. If power is applied quickly (for example by plugging the circuit into a live power source), this tank can ring, doubling the input voltage and damaging the LT1943. The solution is to either clamp the input voltage or dampen the tank circuit by adding a lossy capacitor (an electrolytic) in parallel with the ceramic capacitor. For details, see Application Note 88.

Soft-Start and Shutdown

The RUN/SS (Run/Soft-Start) pin is used to place the switching regulators and the internal bias circuits in shutdown mode. It also provides a soft-start function, along with SS-234. If the RUN/SS is pulled to ground, the LT1943 enters its shutdown mode with all regulators off and quiescent current reduced to ~35µA. An internal 1.7µA current source pulls up on the RUN/SS and SS-234 pins. If the RUN/SS pin reaches ~0.8V, the internal bias circuits start and the quiescent currents increase to their nominal levels.

If a capacitor is tied from the RUN/SS or SS-234 pins to ground, then the internal pull-up current will generate a voltage ramp on these pins. This voltage clamps the V_C pin, limiting the peak switch current and therefore input current during start-up. The RUN/SS pin clamps V_{C1}, and the SS-234 pin clamps the V_{C2}, V_{C3}, and V_{C4} pins. A good value for the soft-start capacitors is C_{OUT}/10,000, where C_{OUT} is the value of the largest output capacitor.

To shut down SW2, SW3, and SW4, pull the SS-234 pin to ground with an open drain or collector.

If the shutdown and soft-start features are not used, leave the RUN/SS and SS-234 pins floating.

V_{ON} Pin Considerations

The V_{ON} pin is the delayed output for switching regulator 3. When the C_T pin reaches 1.1V, the output disconnect PNP turns on, connecting V_{ON} to E3. The V_{ON} pin is current limited, and will protect the LT1943 and input source from a shorted output. However, if the V_{ON} pin is charged to a high output voltage, and then shorted to ground through a long wire, unpredictable results can occur. The resonant tank circuit created by the inductance of the long wire and the capacitance at the V_{ON} pin can ring the V_{ON} pin several volts below ground. This can lead to large and potentially damaging currents internal to the LT1943. If the V_{ON} output may be shorted after being fully charged, there

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should be 5Ω of resistance between the V_{ON} pin and its connection to the load, as shown on Figure 3. The resistance will damp resonant tank circuit created by the output short. As the transient on the V_{ON} pin during a short-circuit condition will be highly dependent on the layout and the type of short, be sure to test the short condition and examine the voltage at the V_{ON} pin to check that it does not swing below ground.

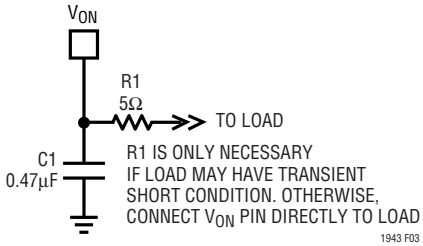

Figure 3. Transient Short Protection for V_{ON} Pin

Printed Circuit Board Layout

For proper operation and minimum EMI, care must be taken during printed circuit board (PCB) layout. Figure 4 shows the high-current paths in the step down regulator circuit. Note that in the step-down regulators, large, switched currents flow in the power switch, the catch diode, and the input capacitor. In the step-up regulators, large, switched currents flow through the power switch, the switching diode, and the output capacitor. In SEPIC and inverting regulators, the switched currents flow through the power switch, the switching diode, and the tank capacitor. The loop formed by the components in the switched current path should be as small as possible. Place these components, along with the inductor and output capacitor, on the same side of the circuit board, and connect them on that layer. Place a local, unbroken ground plane below these components, and tie this ground plane to system ground at one location, ideally at the ground terminal of the output capacitor C2. Additionally, keep the SW and BOOST nodes as small as possible.

Thermal Considerations

The PCB must provide heat sinking to keep the LT1943 cool. The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should be tied to other copper layers below with thermal vias; these layers will spread the heat dissipated by the LT1943. Place additional vias near the catch diodes. Adding more copper to the top and bottom layers and tying this copper to the internal planes with vias can reduce thermal resistance further. With these steps, the thermal resistance from die (or junction) to ambient can be reduced to θ_{JA} = 25°C or less. With 100LFPM airflow, this resistance can fall by another 25%. Further increases in airflow will lead to lower thermal resistance.

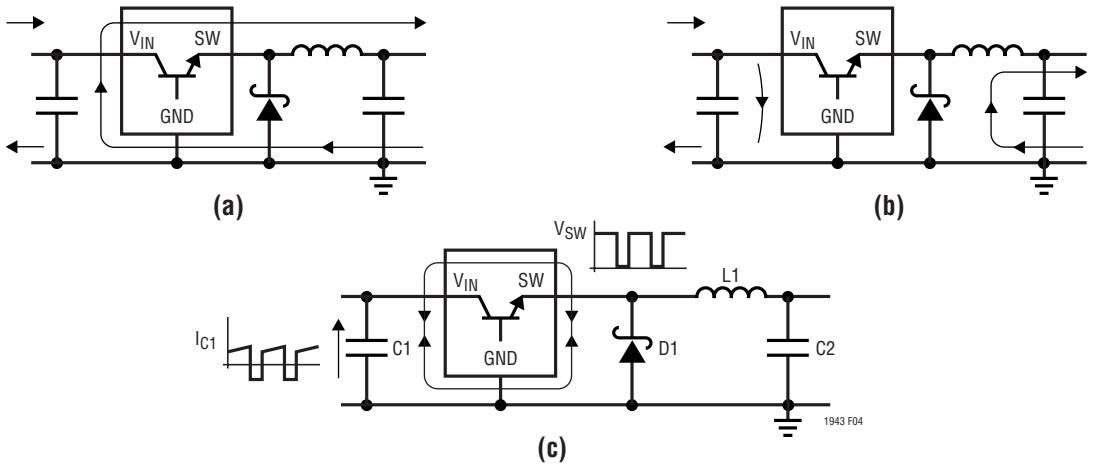

Figure 4. Subtracting the Current when the Switch is ON (a) From the Current when the Switch is OFF (b) Reveals the Path of the High Frequency Switching Current (c) Keep this Loop Small. The Voltage on the SW and BOOST Nodes will also be Switched; Keep these Nodes as Small as Possible. Finally, Make Sure the Circuit is Shielded with a Local Ground Plane

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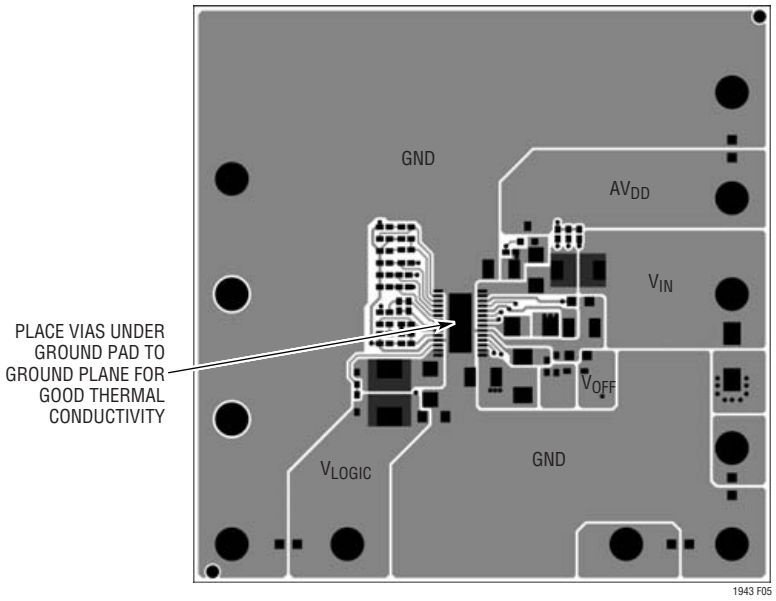
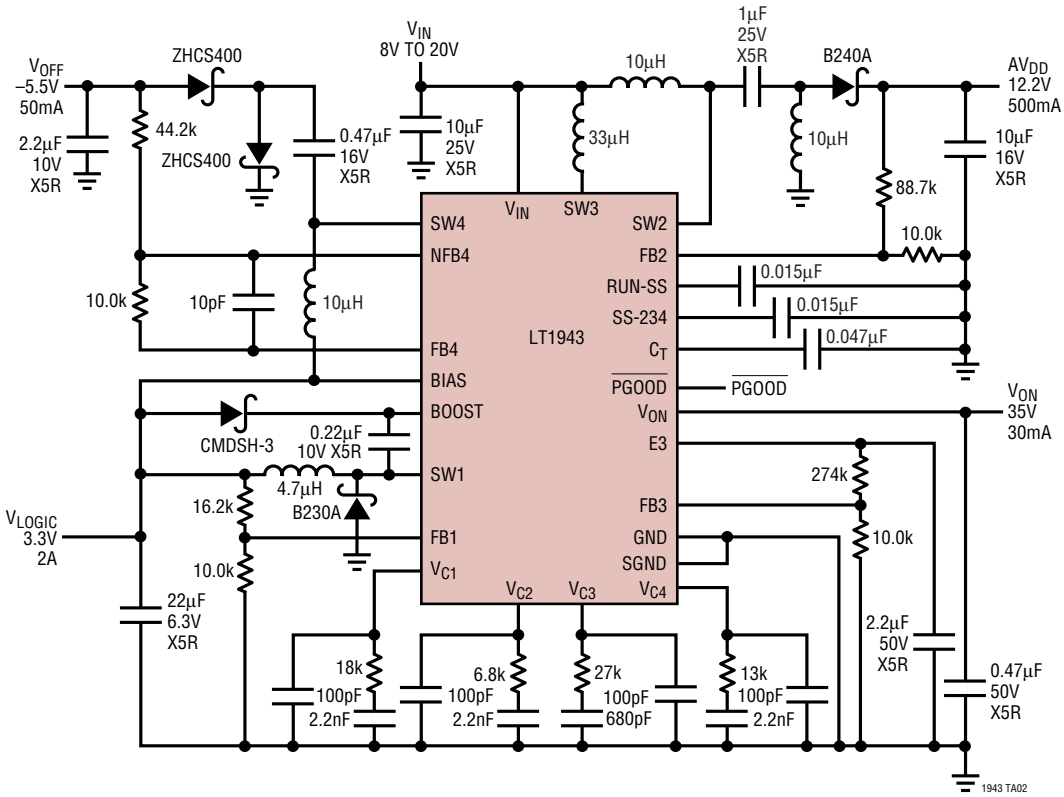


Figure 5. Top Side PCB Layout

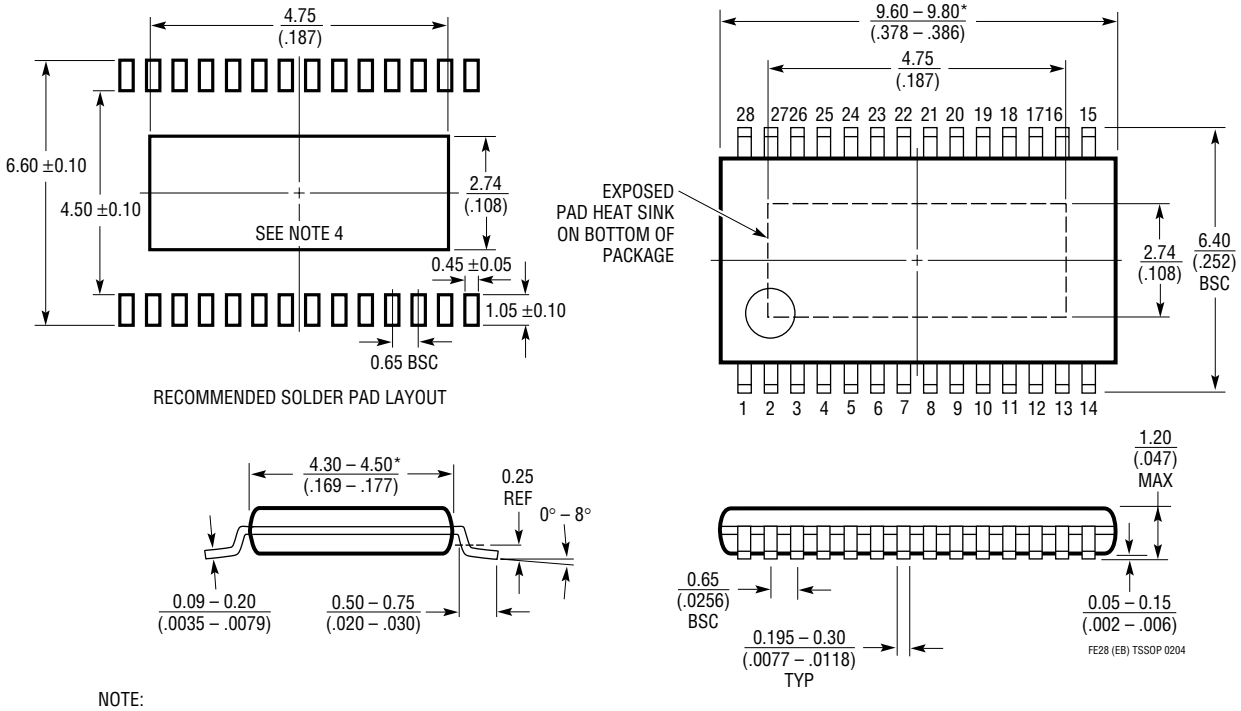
TYPICAL APPLICATIONS

8V to 20V Input, Quad Output TFT-LCD Power Supply



PACKAGE DESCRIPTION

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663)
Exposed Pad Variation EB

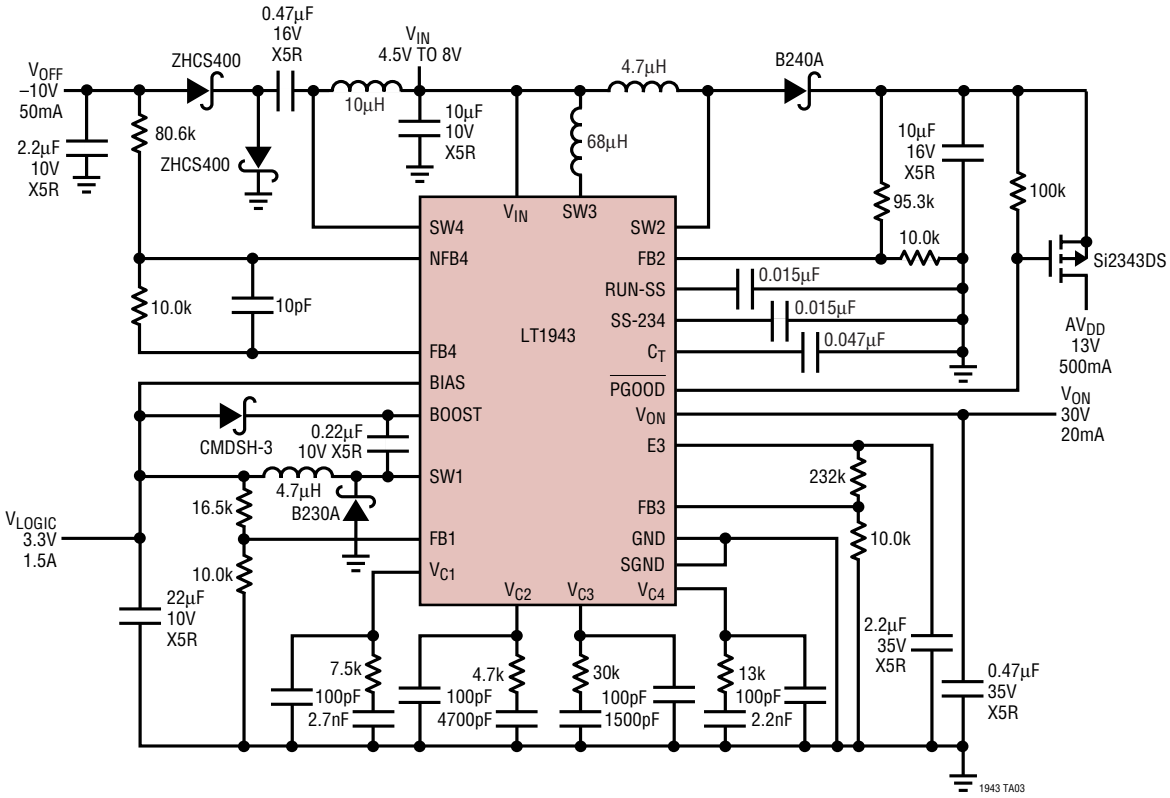


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN MILLIMETERS (INCHES)
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

TYPICAL APPLICATION

5V Input, Quad Output TFT-LCD Power Supply



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1615/LT1615-1	300mA/80mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converters	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, ThinSOT™ Package
LT1940	Dual Output 1.4A (I_{OUT}), Constant 1.1MHz, High Efficiency Step-Down DC/DC Converter	V_{IN}: 3V to 25V, $V_{OUT(MIN)}$: 1.2V, I_Q: 2.5mA, I_{SD}: <1µA, TSSOP-16E Package
LT1944/LT1944-1	Dual Output 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1945	Dual Output, Pos/Neg, 350mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter	V_{IN}: 1.2V to 15V, $V_{OUT(MAX)}$: ±34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1946/LT1946A	1.5mA (I_{SW}), 1.2MHz/2.7MHz, High Efficiency Step-Up DC/DC Converter	V_{IN}: 2.75V to 16V, $V_{OUT(MAX)}$: 34V, I_Q: 20µA, I_{SD}: <1µA, MS Package
LT1947	1.1A, 3MHz, TFT-LCD Triple Output Switching Regulator	V_{IN}: 2.7V to 8V, $V_{OUT(MAX)}$: 34V, I_Q: 9.5mA, I_{SD}: <1µA, MS Package
LT3464	85mA (I_{SW}), Constant Off-Time, High Efficiency Step-Up DC/DC Converter with Integrated Schottky and Output Disconnect PNP	V_{IN}: 2.3V to 10V, $V_{OUT(MAX)}$: 34V, I_Q: 25µA, I_{SD}: <0.5µA, ThinSOT Package

ThinSOT is a trademark of Linear Technology Corporation.

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