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LT1997-3

Precision, Wide Voltage Range Gain Selectable Amplifier

FEATURES

- Pin Configurable as a Difference Amplifier, Inverting Amplifier or Noninverting Amplifier
- 91dB Minimum DC CMRR (Gain = 1)
- 65dB AC CMRR (at 100kHz, Gain = 1)
- 0.006% (60ppm) Maximum Gain Error (Gain = 1)
- 1ppm/°C Maximum Gain Error Drift
- 2ppm Maximum Gain Nonlinearity
- ±160V Common Mode Voltage Range
- Wide Supply Voltage Range: 3.3V to 50V
- Rail-to-Rail Output
- 350µA Supply Current
- 60µV Maximum Op Amp Offset Voltage
- 1.1MHz –3dB Bandwidth (Gain = 1)
- Low-Power Shutdown: 20µA
- Space-Saving MSOP and DFN Packages

APPLICATIONS

- High Side or Low Side Current Sensing
- Bidirectional Wide Common Mode Range Current Sensing
- High Voltage to Low Voltage Level Translation
- Industrial Data-Acquisition Front-Ends
- Replacement for Isolation Circuits
- Differential to Single-Ended Conversion

DESCRIPTION

The LT®1997-3 combines a precision operational amplifier with highly-matched resistors to form a one-chip solution for accurately amplifying voltages. Gains from –13 to +14 with accuracy of 0.006% (60ppm) can be achieved using no external components. The LT1997-3 is particularly well suited for use as a difference amplifier, where the excellent resistor matching results in a common mode rejection ratio of greater than 91dB.

The amplifier features a 60µV maximum input offset voltage and a –3dB bandwidth of 1.1MHz (Gain = 1). The LT1997-3 operates from any supply voltage from 3.3V to 50V and draws only 350µA supply current. The output typically swings to within 100mV of either supply rail.

The resistors maintain their excellent matching over temperature; the matching temperature coefficient is guaranteed less than 1ppm/°C. The resistors are extremely linear with voltage, resulting in a gain nonlinearity of less than 2ppm.
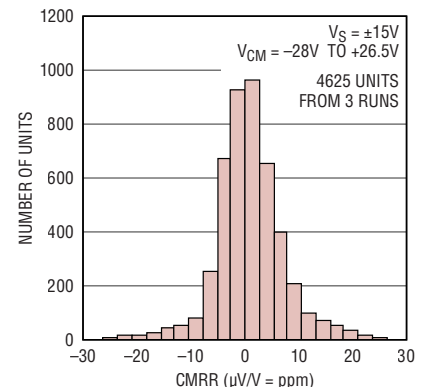
The LT1997-3 is fully specified at 5V and ±15V supplies and from –40°C to 125°C. The device is available in space saving 16-lead MSOP and 4mm × 4mm DFN14 packages.

TYPICAL APPLICATION

Gain = 1 Difference Amplifier

Typical Distribution of CMRR (G = 1)

19973f
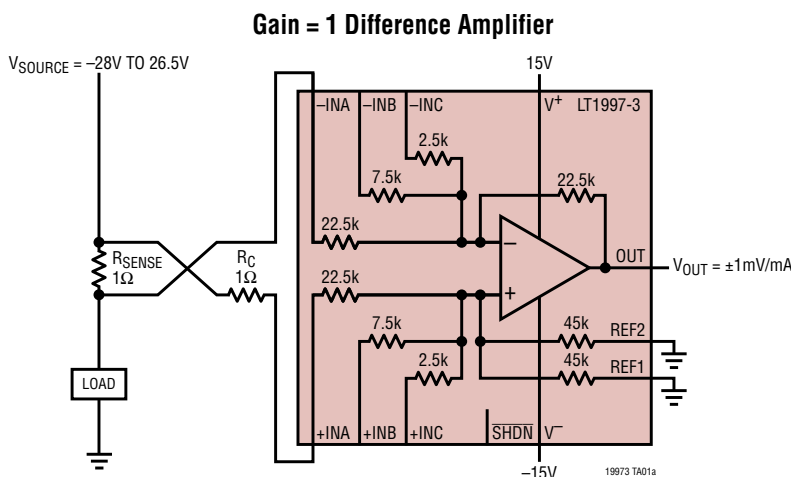
ABSOLUTE MAXIMUM RATINGS

(Note 1)

Supply Voltages (V$^+$ to V$^-$)......................................60V
+INA, −INA (Note 2) .... V$^-$ ±160V
+INB, −INB, +INC, −INC
   (Note 2) .... (V$^-$ + 80V) to (V$^-$ − 0.3V)
REF, REF1, REF2..................... (V$^-$ + 60V) to (V$^-$ − 0.3V)
$\overline{SHDN}$.................................... (V$^+$ + 0.3V) to (V$^-$ − 0.3V)
Output Current (Continuous) (Note 6)...................50mA

Output Short-Circuit Duration
   (Note 3) ....Thermally Limited
Temperature Range (Notes 4, 5)
   LT1997I-3 ....−40 to 85°C
   LT1997H-3 ....−40 to 125°C
Maximum Junction Temperature .... 150°C
Storage Temperature Range ....−65 to 150°C
MSOP Lead Temperature (Soldering, 10 sec)........300°C

PIN CONFIGURATION

TOP VIEW

+INA [1]   [14] −INA
+INB [3]   [12] −INB
NC [4]   [11] NC
     15
     V$^-$
+INC [5]   [10] −INC
$\overline{SHDN}$ [6]   [9] V$^+$
REF [7]   [8] OUT

DF PACKAGE
14(12)-LEAD (4mm × 4mm) PLASTIC DFN
T$_{JMAX}$ = 150°C, θ$_{JA}$ = 45°C/W , θ$_{JC}$ = 3°C/W
EXPOSED PAD (PIN 15) IS V$^-$, MUST BE SOLDERED TO PCB

TOP VIEW

+INA 1   16 −INA
+INB 3   14 −INB
+INC 5   12 −INC
REF1 6   11 V$^+$
REF2 7   10 $\overline{SHDN}$
V$^-$ 8   9 OUT

MS PACKAGE
VARIATION: MS16 (12)
16-LEAD PLASTIC MSOP
T$_{JMAX}$ = 150°C, θ$_{JA}$ = 130°C/W

ORDER INFORMATION

http://www.linear.com/product/LT1997-3#orderinfo
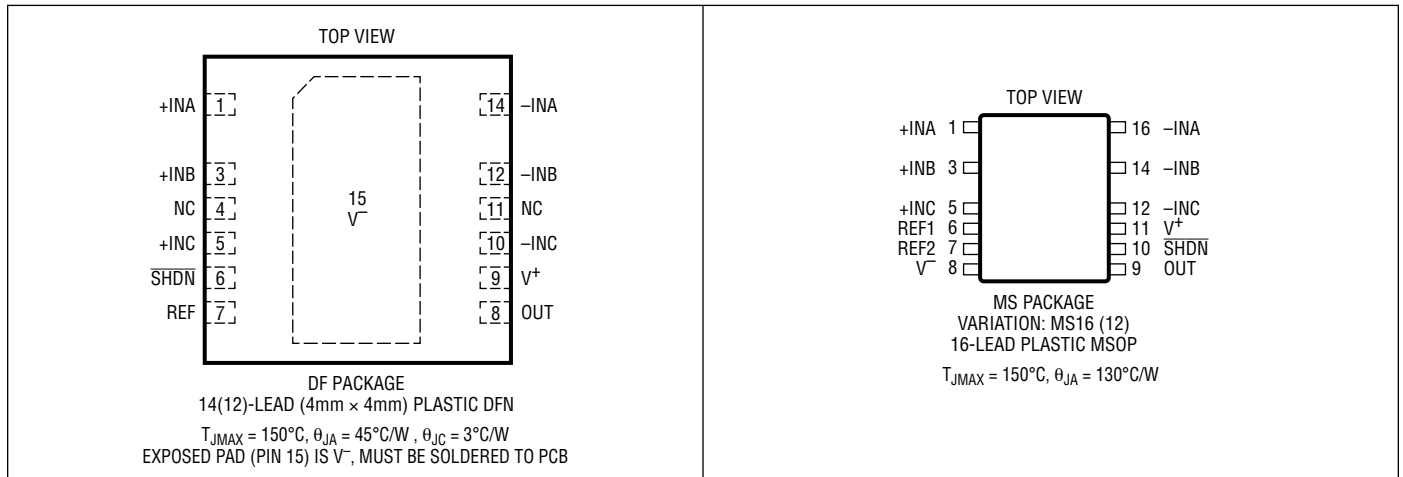
LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE
LT1997IDF-3#PBF	LT1997IDF-3#TRPBF	19973	14-Lead (4mm × 4mm) Plastic DFN	−40°C to 85°C
LT1997HDF-3#PBF	LT1997HDF-3#TRPBF	19973	14-Lead (4mm × 4mm) Plastic DFN	−40°C to 125°C
LT1997IMS-3#PBF	LT1997IMS-3#TRPBF	19973	16-Lead Plastic MSOP	−40°C to 85°C
LT1997HMS-3#PBF	LT1997HMS-3#TRPBF	19973	16-Lead Plastic MSOP	−40°C to 125°C

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges. Parts ending with PBF are RoHS and WEEE compliant.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, −40°C < T_A < 85°C for I-grade parts, −40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 15V, V^- = −15V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = 0V. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V_{OUT} = ±10V G = 1	 ●		±0.001	±0.006 ±0.012	% %
		G = 3	●		±0.001	±0.015 ±0.02	% %
		G = 9	●		±0.002	±0.03 ±0.04	% %
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = ±10V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = ±10V	 ●		±1	±2 ±3	ppm ppm
V_{OS}	Op Amp Offset Voltage (Note 9)	V^- < V_{CMOP} < V^+ − 1.75V	 ●		±20	±60 ±200	μV μV
$ΔV_{OS}/ΔT$	Op Amp Offset Voltage Drift (Note 6)	V^- < V_{CMOP} < V^+ − 1.75V	●		±0.5	±1.5	μV/°C
I_B	Op Amp Input Bias Current	V^- + 0.25V < V_{CMOP} < V^+ − 1.75V	 ●	−5 −15	±2	5 15	nA nA
I_{OS}	Op Amp Input Offset Current	V^- + 0.25V < V_{CMOP} < V^+ − 1.75V	 ●	−3 −10	±0.5	3 10	nA nA
R_{IN}	Input Impedance (Note 8)	Common Mode G = 1 G = 3 G = 9	 ● ● ●	 19 12.6 10.5	 22.5 15 12.5	 26 17.4 14.5	 kΩ kΩ kΩ
		Differential G = 1 G = 3 G = 9	 ● ● ●	 38 12.6 4.2	 45 15 5	 52 17.4 5.8	 kΩ kΩ kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	G = 1, V_{CM} = −28V to +26.5V	 ●	91 87	106		dB dB
		G = 3, V_{CM} = −15V to +17.6V	 ●	90 86	99		dB dB
		G = 9, V_{CM} = −15V to +14.7V	 ●	96 94	112		dB dB
CMRR	Common Mode Rejection Ratio, DF14 Package	G = 1, V_{CM} = −28V to +26.5V	 ●	91 87	101		dB dB
		G = 1, V_{CM} = −90V to +90V, +INB = −INB = 0V, V_S = ±25V	 ●	83 80	94		dB dB
		G = 1, V_{CM} = −120V to +120V, +INC = −INC = 0V, V_S = ±25V, T_A = −40°C to 125°C	 ●	81 77	91		dB dB
		G = 1, V_{CM} = −160V to +160V, +INC = −INC = 0V, V_S = ±25V, T_A = −40°C to 85°C	 ●	81 78	91		dB dB
		G = 3, V_{CM} = −15V to +17.6V	 ●	90 86	98		dB dB
		G = 9, V_{CM} = −15V to +14.7V	 ●	96 94	103		dB dB
V_{CM}	Input Voltage Range (Note 7)	+INA/−INA +INA/−INA, +INC/−INC Connected to Ground +INB/−INB +INC/−INC	● ● ● ●	−30 −160 −15 −15		26.5 160 17.6 14.7	V V V V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, −40°C < T_A < 85°C for I-grade parts, −40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 15V, V^- = −15V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = 0V. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔR/R	Reference Divider Matching Error $$\frac{\Delta R}{R} = \frac{R_{REF1} - R_{REF2}}{\left(\frac{R_{REF1} + R_{REF2}}{2}\right)}$$	Available in MS16 Package Only	●		±0.001	±0.006 ±0.012	% %
PSRR	Power Supply Rejection Ratio	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply (Note 9)	●	114	124		dB
e_{ni}	Input Referred Noise Voltage Density	f = 1kHz G = 1 G = 3 G = 9			50 30 22		nV/√Hz nV/√Hz nV/√Hz
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz G = 1 G = 3 G = 9			1.4 1 0.8		μV_{P-P} μV_{P-P} μV_{P-P}
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load I_{SINK} = 5mA	● ●		100 280	150 500	mV mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load I_{SOURCE} = 5mA	● ●		100 530	180 900	mV mV
I_{SC}	Short-Circuit Output Current	50Ω to V^+ 50Ω to V^-	● ●	10 10	28 30		mA mA
SR	Slew Rate	ΔV_{OUT} = ±5V	●	0.45	0.75		V/μs
BW	Small Signal −3dB Bandwidth	G = 1 G = 3 G = 9			1100 700 300		kHz kHz kHz
t_S	Settling Time	G = 1 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			14.6 95		μs μs
		G = 3 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			13.6 29		μs μs
		G = 9 0.1%, ΔV_{OUT} = 10V 0.01%, ΔV_{OUT} = 10V			13.8 29		μs μs
V_S	Supply Voltage		 ●	3 3.3		50 50	V V
t_{ON}	Turn-On Time				16		μs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			−2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	−1.2			V
I_{SHDN}	$\overline{SHDN}$ Pin Current		●		−10	−15	μA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$ Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	 ● ●		350 20	400 600 25 70	μA μA μA μA

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ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, −40°C < T_A < 85°C for I-grade parts, −40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ΔG	Gain Error	V_{OUT} = 1V to 4V G = 1			±0.001	±0.006	%
			●			±0.012	%
		G = 3			±0.001	±0.015	%
			●			±0.02	%
		G = 9			±0.002	±0.03	%
			●			±0.04	%
ΔG/ΔT	Gain Drift vs Temperature (Note 6)	V_{OUT} = 1V to 4V	●		±0.2	±1	ppm/°C
GNL	Gain Nonlinearity	V_{OUT} = 1V to 4V			±1		ppm
V_{OS}	Op Amp Offset Voltage (Note 9)	V^- < V_{CMOP} < V^+ − 1.75V			±20	±60	μV
			●			±200	μV
$ΔV_{OS}/ΔT$	Op Amp Offset Voltage Drift (Note 6)	V^- < V_{CMOP} < V^+ − 1.75V	●		±0.5	±1.5	μV/°C
I_B	Op Amp Input Bias Current	V^- + 0.25V < V_{CMOP} < V^+ − 1.75V		−5	±2	5	nA
			●	−15		15	nA
I_{OS}	Op Amp Input Offset Current	V^- + 0.25V < V_{CMOP} < V^+ − 1.75V		−3	±0.5	3	nA
			●	−10		10	nA
R_{IN}	Input Impedance (Note 8)	Common Mode G = 1 G = 3 G = 9	● ● ●	19 12.6 10.5	22.5 15 12.5	26 17.4 14.5	kΩ kΩ kΩ
		Differential G = 1 G = 3 G = 9	● ● ● ●	38 12.6 4.2	45 15 5	52 17.4 5.8	kΩ kΩ kΩ
CMRR	Common Mode Rejection Ratio, MS16 Package	G = 1, V_{CM} = −2.5V to +4.0V		90	100		dB
			●	88			dB
		G = 3, V_{CM} = 0V to +3.5V		90	103		dB
			●	87			dB
		G = 9, V_{CM} = 0V to +3.3V		96	108		dB
			●	94			dB
CMRR	Common Mode Rejection Ratio, DF14 Package	G = 1, V_{CM} = −2.5V to +4.0V		90	96		dB
			●	88			dB
		G = 3, V_{CM} = 0V to +3.5V		90	101		dB
			●	87			dB
		G = 9, V_{CM} = 0V to +3.3V		96	107		dB
			●	94			dB
ΔR/R	Reference Divider Matching Error $\dfrac{\Delta R}{R} = \dfrac{R_{REF1} - R_{REF2}}{\left(\dfrac{R_{REF1} + R_{REF2}}{2}\right)}$	Available in MS16 Package Only			±0.001	±0.006	%
			●			±0.012	%
PSRR	Power Supply Rejection Ratio	V_S = ±1.65V to ±25V, V_{CM} = V_{OUT} = Mid-Supply (Note 9)	●	114	124		dB
e_{ni}	Input Referred Noise Voltage Density	f = 1kHz G = 1 G = 3 G = 9			50 30 22		nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$ nV/$\sqrt{Hz}$

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5

LT1997-3

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, −40°C < T_A < 85°C for I-grade parts, −40°C < T_A < 125°C for H-grade parts, otherwise specifications are at T_A = 25°C. Difference Amplifier Configuration, V^+ = 5V, V^- = 0V, V_{CM} = V_{OUT} = V_{REF} = V_{REF1} = V_{REF2} = Mid-Supply. V_{CMOP} is the common mode voltage of the internal op amp.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Input Referred Noise Voltage	f = 0.1Hz to 10Hz					
		G = 1			1.4		μV_{P-P}
		G = 3			1		μV_{P-P}
		G = 9			0.8		μV_{P-P}
V_{OL}	Output Voltage Swing Low (Referred to V^-)	No Load	●		15	50	mV
		I_{SINK} = 5mA	●		280	500	mV
V_{OH}	Output Voltage Swing High (Referred to V^+)	No Load	●		15	50	mV
		I_{SOURCE} = 5mA	●		450	800	mV
I_{SC}	Short-Circuit Output Current	50Ω to V^+	●	10	27		mA
		50Ω to V^-	●	10	25		mA
SR	Slew Rate	ΔV_{OUT} = 3V	●	0.45	0.75		V/µs
BW	Small signal −3dB Bandwidth	G = 1			1100		kHz
		G = 3			700		kHz
		G = 9			300		kHz
t_S	Settling Time	G = 1					
		0.1%, ΔV_{OUT} = 2V			5.4		µs
		0.01%, ΔV_{OUT} = 2V			91		µs
		G = 3					
		0.1%, ΔV_{OUT} = 2V			6		µs
		0.01%, ΔV_{OUT} = 2V			21		µs
		G = 9					
		0.1%, ΔV_{OUT} = 2V			7		µs
		0.01%, ΔV_{OUT} = 2V			36		µs
V_S	Supply Voltage			3		50	V
			●	3.3		50	V
t_{ON}	Turn-On Time				22		µs
V_{IL}	$\overline{SHDN}$ Input Logic Low (Referred to V^+)		●			−2.5	V
V_{IH}	$\overline{SHDN}$ Input Logic High (Referred to V^+)		●	−1.2			V
$I_{\overline{SHDN}}$	$\overline{SHDN}$ Pin Current		●		−10	−15	µA
I_S	Supply Current	Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$			330	370	µA
		Active, $V_{\overline{SHDN}} \geq V^+ - 1.2V$	●			525	µA
		Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$			15	20	µA
		Shutdown, $V_{\overline{SHDN}} \leq V^+ - 2.5V$	●			40	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: See "Common Mode Voltage Range" and "High Common Mode Voltage Difference Amplifiers" in the Applications Information section of this data sheet for other considerations when taking +INA/–INA pins to ±160V and +INB/–INB/+INC/–INC pins to +80V.

Note 3: A heat sink may be required to keep the junction temperature below absolute maximum. This depends on the power supply, input voltages and the output current.

Note 4: The LT1997I-3 is guaranteed functional over the operating temperature range of –40°C to 85°C. The LT1997H-3 is guaranteed functional over the operating temperature range of –40°C to 125°C.

Note 5: The LT1997I-3 is guaranteed to meet specified performance from –40°C to 85°C. The LT1997H-3 is guaranteed to meet specified performance from –40°C to 125°C.

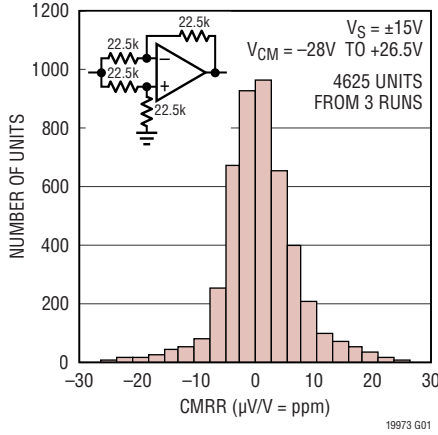**Note 6:** This parameter is not 100% tested.

Note 7: The Input Voltage Range numbers specified in the table guarantee that the internal op amp operates in its normal operating region. The Input voltage range can be significantly higher if the internal op amp operates in its Over-The-Top® operating region. See "Common Mode Voltage Range" in the Applications Information section to determine the valid input voltage range under various operating conditions.

Note 8: Input impedance is tested by a combination of direct measurements and correlation to the CMRR and gain error tests.
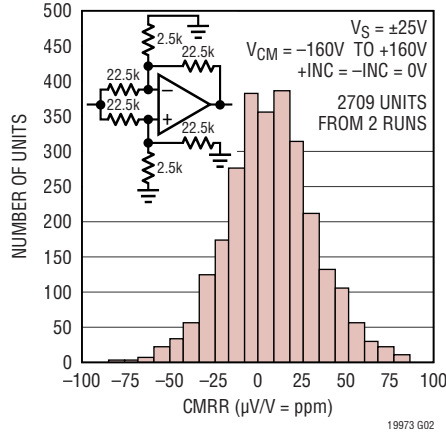
Note 9: Offset voltage, offset voltage drift and PSRR are defined as referred to the internal op amp. You can calculate output offset as follows. In the case of balanced source resistance, $V_{OS,OUT}$ = ($V_{OS} \cdot$ NOISEGAIN) + ($I_{OS} \cdot$ 22.5k) + ($I_B \cdot$ 22.5k $\cdot$ (1− R_P/R_N)) where R_P and R_N are the total resistance at the op amp positive and negative terminal, respectively.

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6

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, Difference Amplifier configuration, unless otherwise noted.

Typical Distribution of CMRR (G = 1)
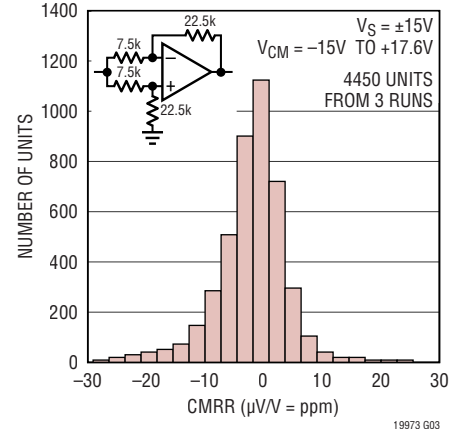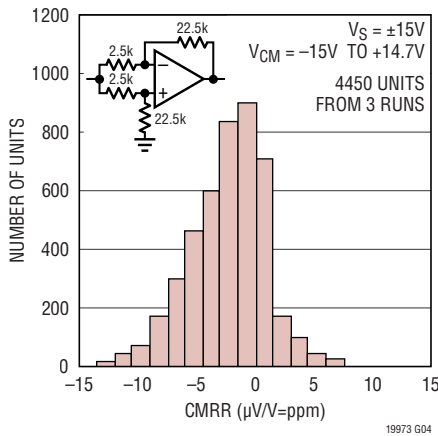
$V_S = ±15V$
$V_{CM} = -28V$ TO $+26.5V$
4625 UNITS FROM 3 RUNS

19973 G01

Typical Distribution of CMRR (G = 1)

$V_S = ±25V$
$V_{CM} = -160V$ TO $+160V$
$+INC = -INC = 0V$
2709 UNITS FROM 2 RUNS

19973 G02

Typical Distribution of CMRR (G = 3)

$V_S = ±15V$
$V_{CM} = -15V$ TO $+17.6V$
4450 UNITS FROM 3 RUNS

19973 G03

Typical Distribution of CMRR (G = 9)

$V_S = ±15V$
$V_{CM} = -15V$ TO $+14.7V$
4450 UNITS FROM 3 RUNS

19973 G04

Typical Distribution of Gain Error (G = 1)

$V_S = ±15V$
$V_{OUT} = ±10V$
4864 UNITS FROM 3 RUNS

19973 G05

Typical Distribution of Gain Error (G = 3)

$V_S = ±15V$
$V_{OUT} = ±10V$
4864 UNITS FROM 3 RUNS

19973 G06

Typical Distribution of Gain Error (G = 9)

$V_S = ±15V$
$V_{OUT} = ±10V$
4864 UNITS FROM 3 RUNS

19973 G07
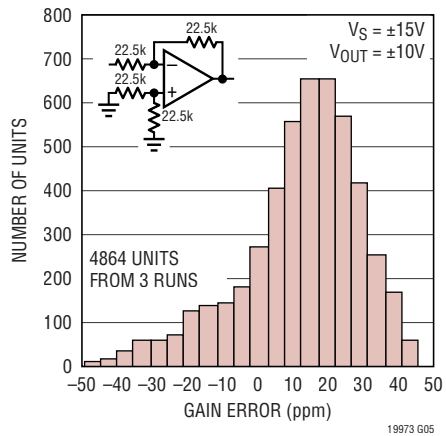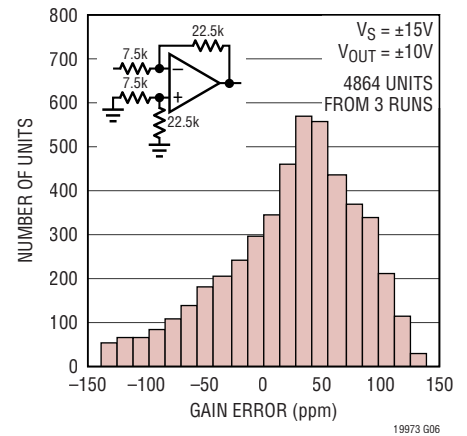
Typical Distribution of Gain Nonlinearity
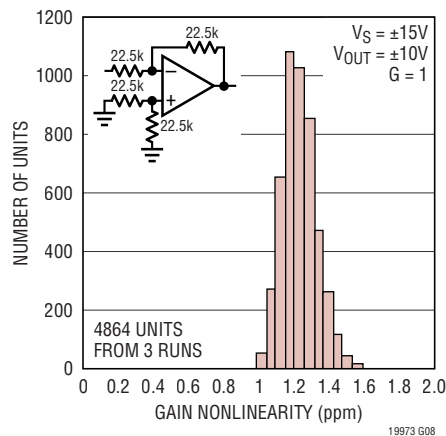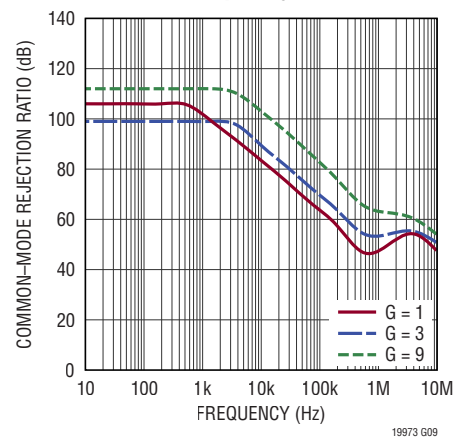
$V_S = ±15V$
$V_{OUT} = ±10V$
G = 1
4864 UNITS FROM 3 RUNS

19973 G08

CMRR vs Frequency

G = 1
G = 3
G = 9

19973 G09

19973f

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_S = ±15V, Difference Amplifier
configuration, unless otherwise noted.

Typical Distribution of Op Amp Offset Voltage

6360 UNITS FROM 3 RUNS
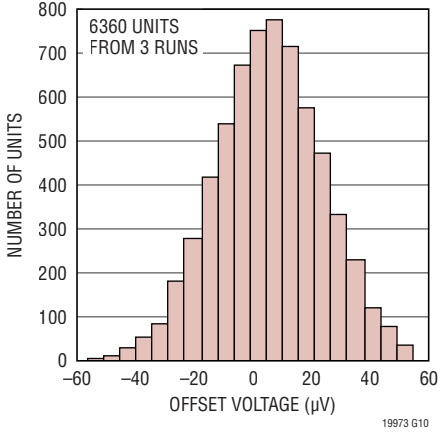
19973 G10

Typical Distribution of Op Amp PSRR

4864 UNITS FROM 3 RUNS

V_S = ±1.65V to ±25V
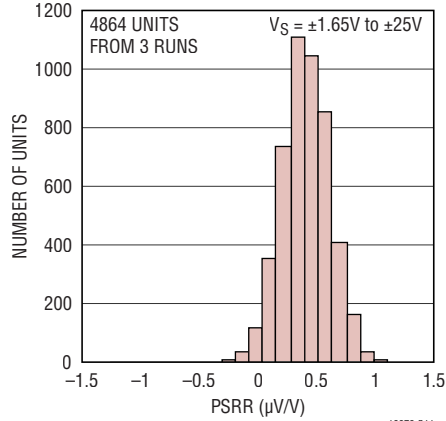
19973 G11

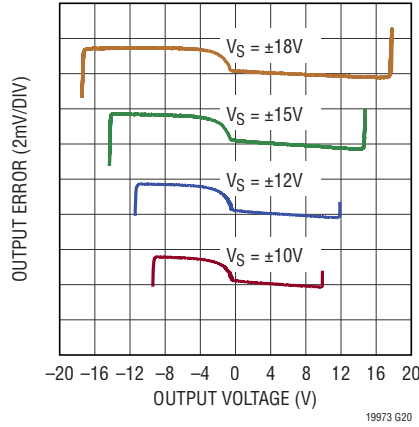**Typical Gain Error for R_L = 10kΩ G = 1 (Curves Offset for Clarity)**

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
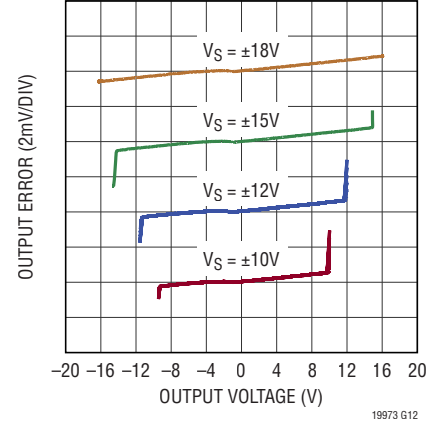
19973 G12

Typical Gain Error for R_L = 5kΩ G = 1 (Curves Offset for Clarity)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
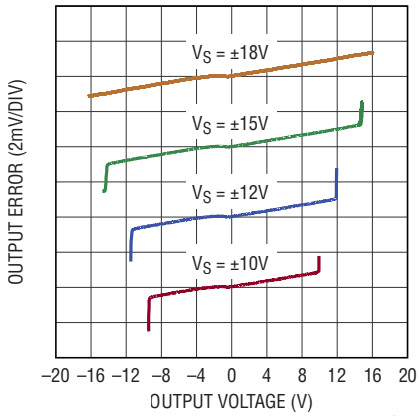
19973 G13

Typical Gain Error for R_L = 2kΩ G = 1 (Curves Offset for Clarity)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
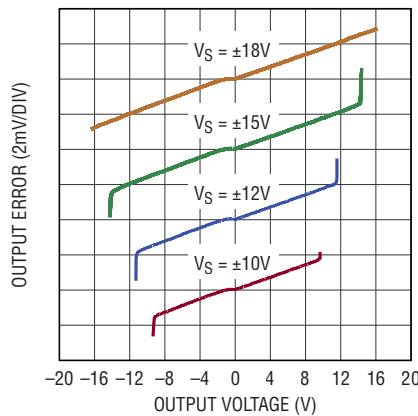
19973 G14

Typical Gain Error for Low Supply Voltages, G = 1 (Curves Offset for Clarity)

V_S = ±5V, R_L=10kΩ
V_S = ±5V, R_L=2kΩ
V_S = ±5V, R_L=1kΩ
V_S = ±2.5V, R_L=1kΩ
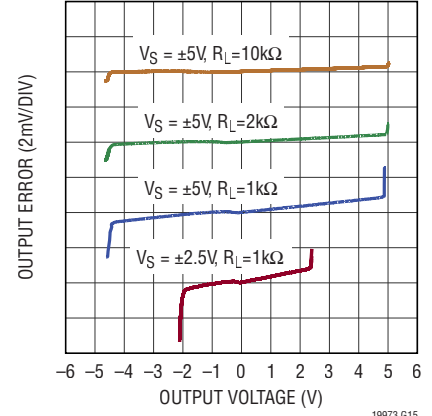
19973 G15

Typical Gain Error for R_L = 10kΩ G = 3 (Curves Offset for Clarity)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
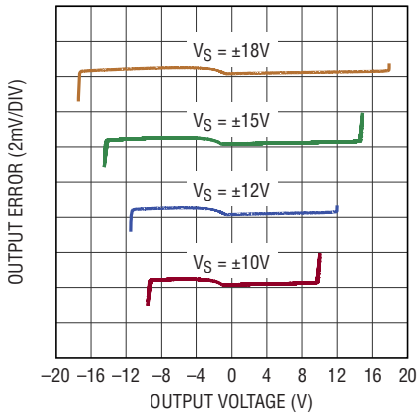
19973 G16

Typical Gain Error for R_L = 5kΩ G = 3 (Curves Offset for Clarity)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
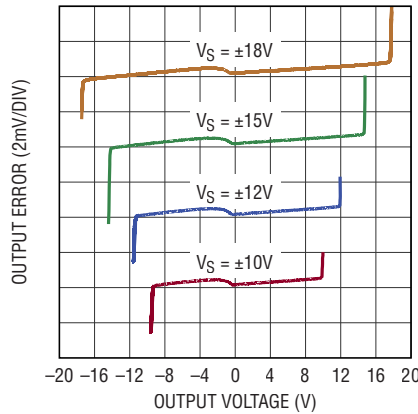
19973 G17

Typical Gain Error for R_L = 2kΩ G = 3 (Curves Offset for Clarity)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V
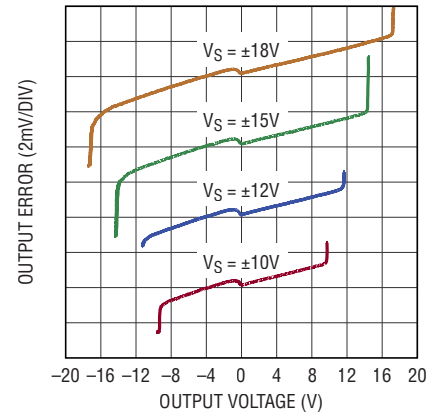
19973 G18

19973f

8

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_S = ±15V, Difference Amplifier
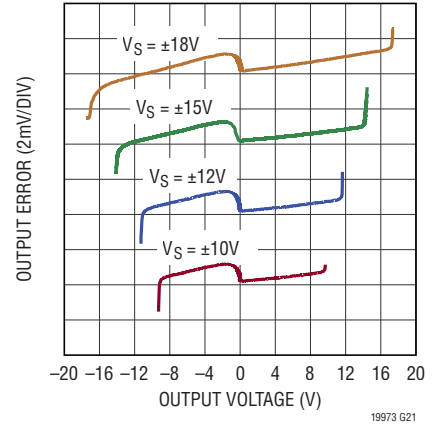configuration, unless otherwise noted.

Typical Gain Error for R_L = 10kΩ
G = 9 (Curves Offset for Clarity)
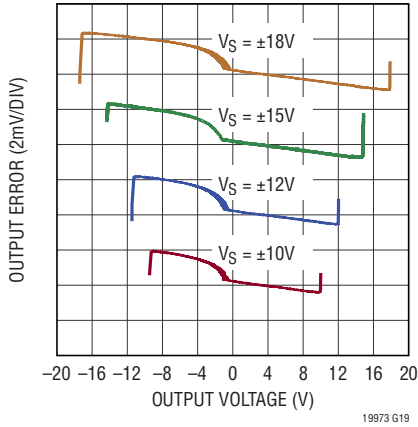
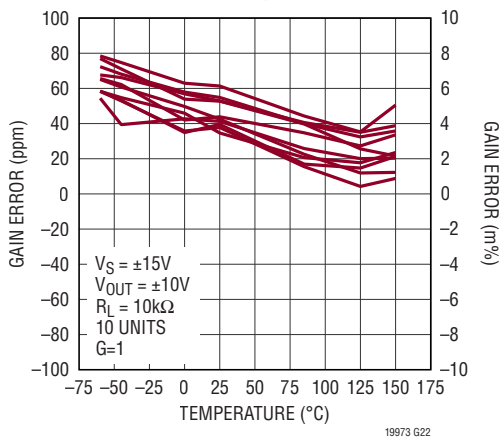OUTPUT ERROR (2mV/DIV)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V

OUTPUT VOLTAGE (V)

19973 G19

Typical Gain Error for R_L = 5kΩ
G = 9 (Curves Offset for Clarity)

OUTPUT ERROR (2mV/DIV)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V

OUTPUT VOLTAGE (V)

19973 G20

Typical Gain Error for R_L = 2kΩ
G = 9 (Curves Offset for Clarity)

OUTPUT ERROR (2mV/DIV)

V_S = ±18V
V_S = ±15V
V_S = ±12V
V_S = ±10V

OUTPUT VOLTAGE (V)

19973 G21

Gain Error vs Temperature

GAIN ERROR (ppm)
GAIN ERROR (m%)

V_S = ±15V
V_{OUT} = ±10V
R_L = 10kΩ
10 UNITS
G=1

TEMPERATURE (°C)

19973 G22

CMRR vs Temperature

CMRR (μV/V)

V_S = ±15V
10 UNITS,
G=1

TEMPERATURE (°C)

19973 G23
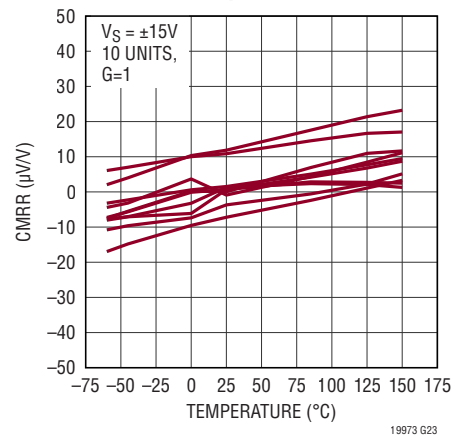
Output Voltage vs Load Current

OUTPUT VOLTAGE (V)

130°C
85°C
25°C
−45°C

OUTPUT CURRENT (mA)

19973 G24
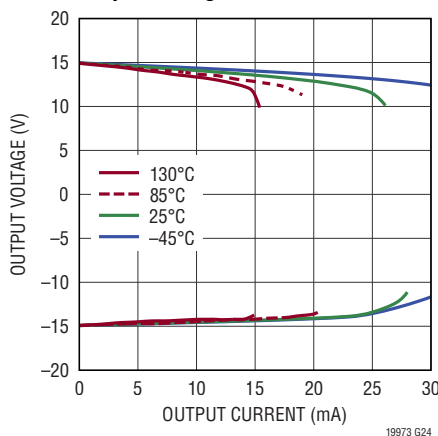
Maximum Power Dissipation vs Temperature
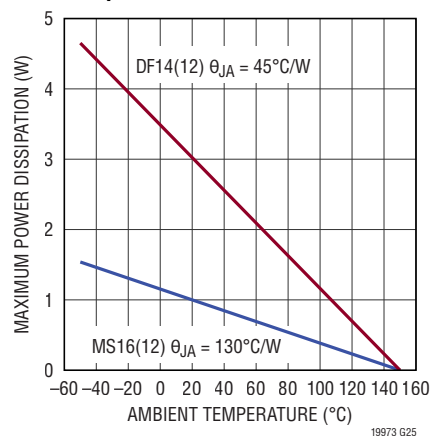
MAXIMUM POWER DISSIPATION (W)

DF14(12) θ_{JA} = 45°C/W

MS16(12) θ_{JA} = 130°C/W

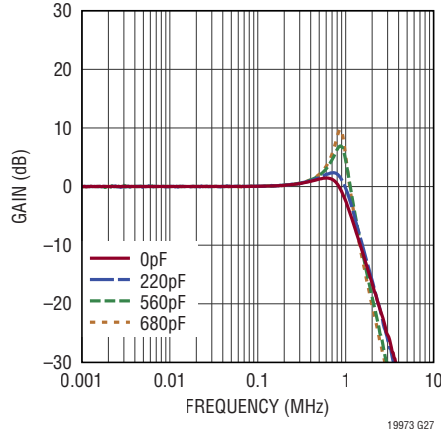AMBIENT TEMPERATURE (°C)

19973 G25

19973f

9

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_S = ±15V, Difference Amplifier
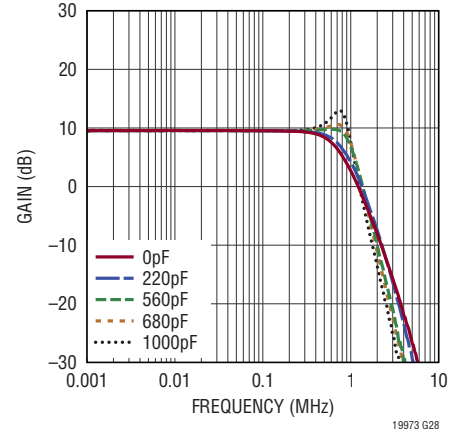configuration, unless otherwise noted.

Gain vs Frequency

19973 G26

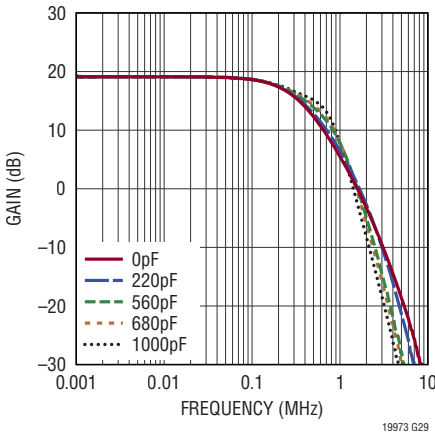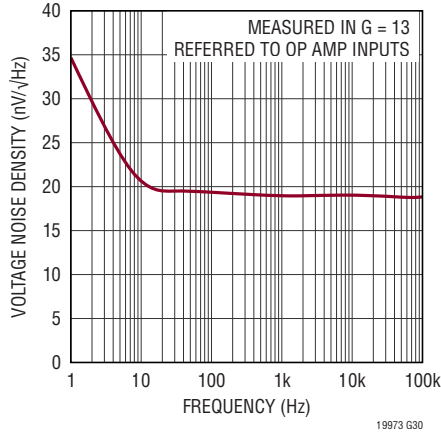**Frequency Response vs Capacitive Load (G = 1)**

19973 G27
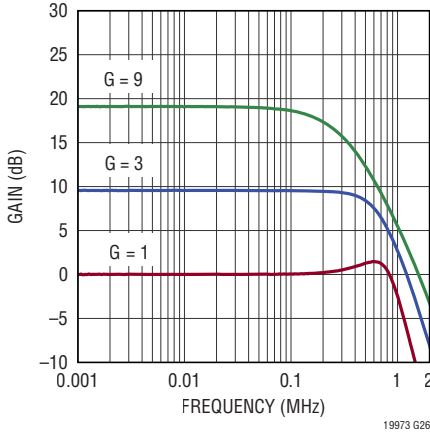
Frequency Response vs Capacitive Load (G = 3)

19973 G28

Frequency Response vs Capacitive Load (G = 9)

19973 G29

Op Amp Noise Density vs Frequency

19973 G30

0.1Hz to 10Hz Noise
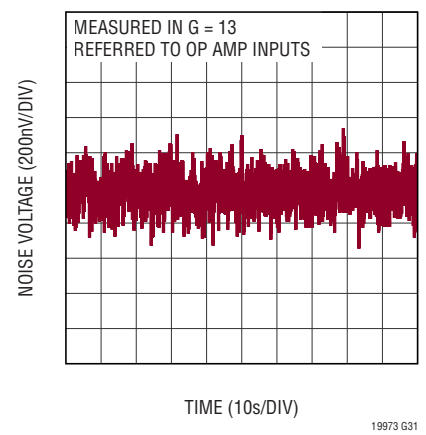
19973 G31

Positive PSRR vs Frequency
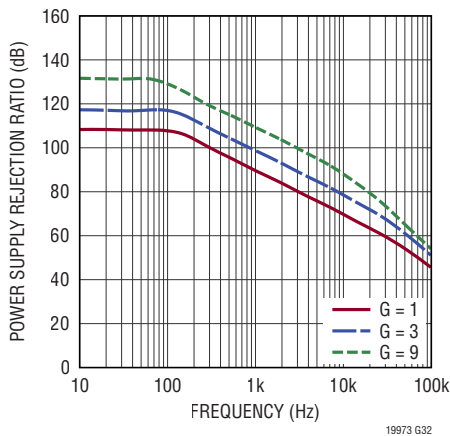
19973 G32

Negative PSRR vs Frequency
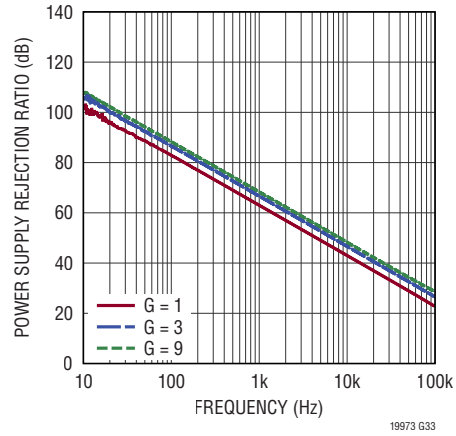
19973 G33

19973f

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_S = ±15V$, Difference Amplifier configuration, unless otherwise noted.

Slew Rate vs Temperature

$R_L = 10k\Omega$

RISING EDGE

FALLING EDGE
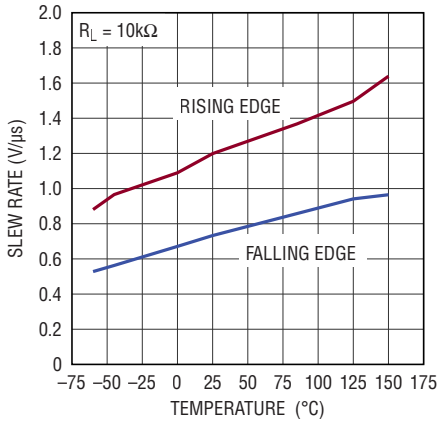
19973 G34

Large-Signal Step Response

G = 1
$R_L = 10k\Omega$
$C_L = 560pF$

19973 G35

Small-Signal Step Response

G = 1
$R_L = 10k\Omega$

$C_L = 680pF$

$C_L = 560pF$

$C_L = 0pF$
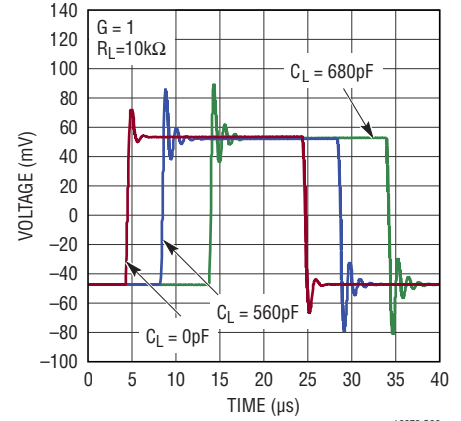
19973 G36

Small-Signal Step Response

G = 3
$R_L = 10k\Omega$

$C_L = 1000pF$

$C_L = 680pF$

$C_L = 0pF$

$C_L = 560pF$
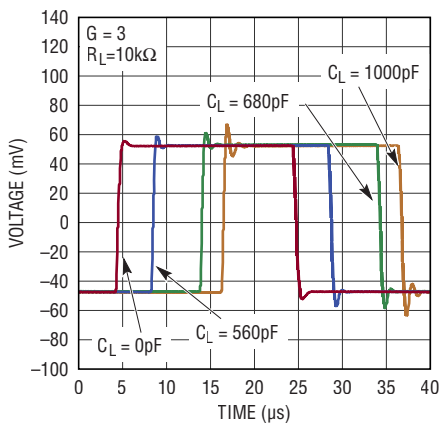
19973 G37

Small-Signal Step Response

G = 9
$R_L = 10k\Omega$

$C_L = 1000pF$

$C_L = 680pF$

$C_L = 0pF$

$C_L = 560pF$

19973 G38

Settling Time

OUTPUT VOLTAGE

G = 1

ERROR VOLTAGE

TIME (20µs/DIV)

19973 G39

Settling Time

G = 1

ERROR VOLTAGE

OUTPUT VOLTAGE

TIME (20µs/DIV)
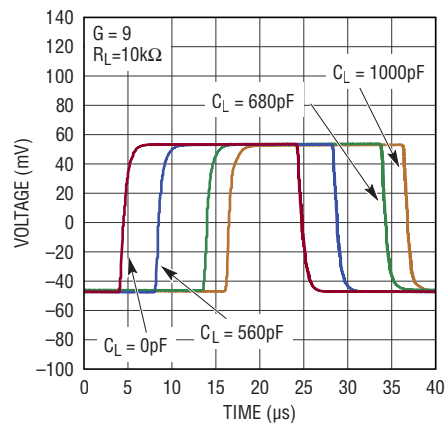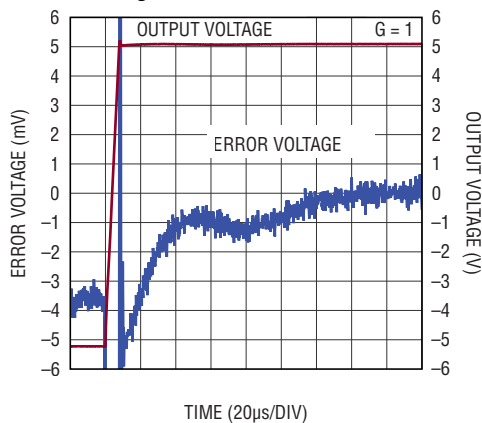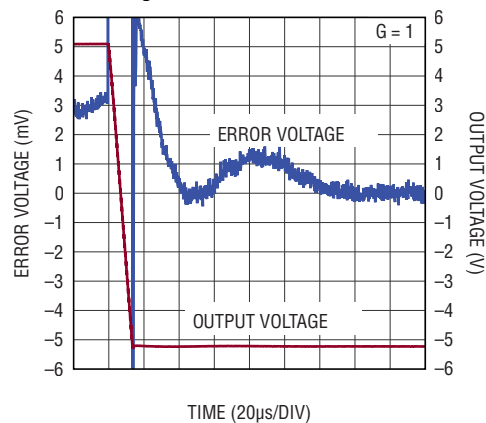
19973 G40

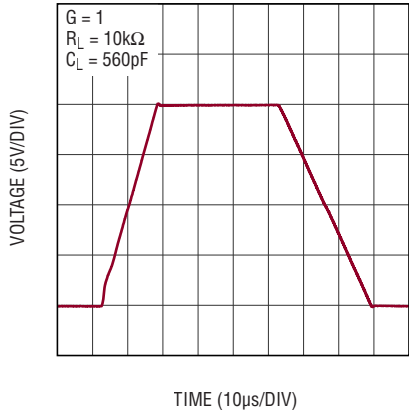# TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, V_S = ±15V, Difference Amplifier configuration, unless otherwise noted.

Op Amp Offset Voltage vs Temperature

20 UNITS
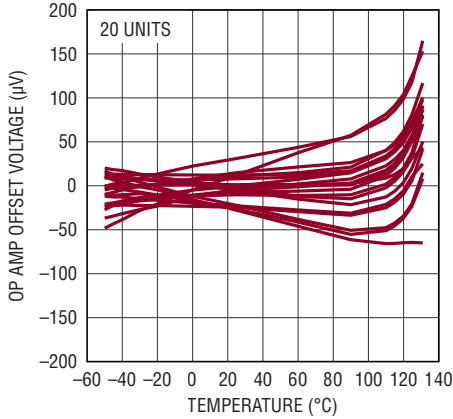
19973 G41

Quiescent Current vs Temperature

10 UNITS
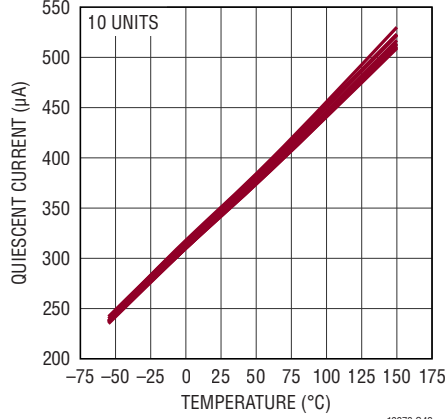
19973 G42

Thermal Shutdown vs Hysteresis
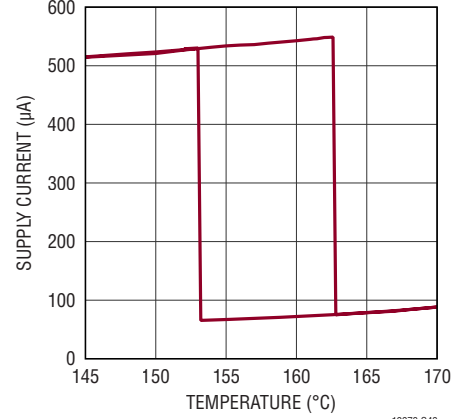
19973 G43

Quiescent Current vs Supply Voltage

PARAMETRIC SWEEP IN ~25°C INCREMENTS

T_A = 150°C

T_A = –55°C
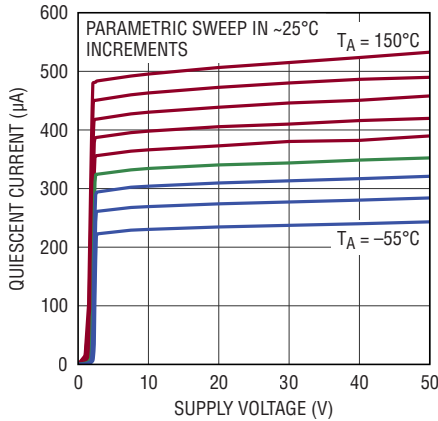
19973 G44

Shutdown Quiescent Current vs Supply Voltage

150°C   25°C
125°C   –40°C
85°C   –55°C

$V_{\overline{SHDN}}$ = 0V
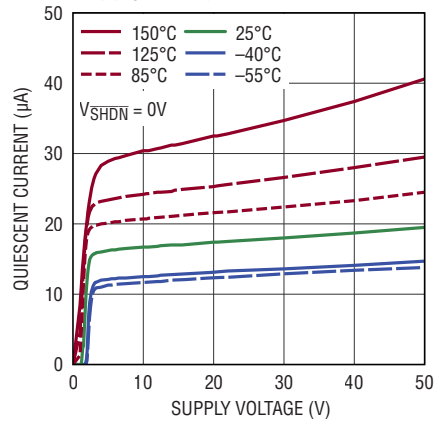
19973 G45

Quiescent Current vs $\overline{SHDN}$ Voltage

V_S = ±15V

150°C
125°C
85°C
25°C
–40°C
–55°C
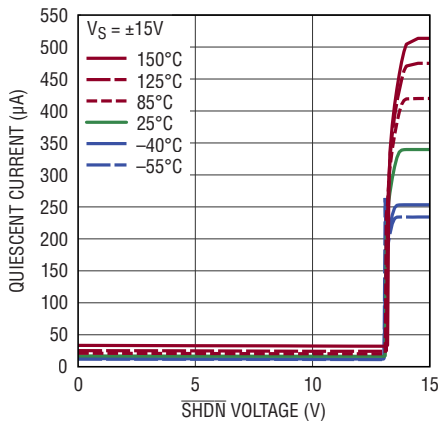
19973 G46

Minimum Supply Voltage

T_A = 125°C

T_A = 25°C

T_A = –45°C

19973 G47

19973f

12
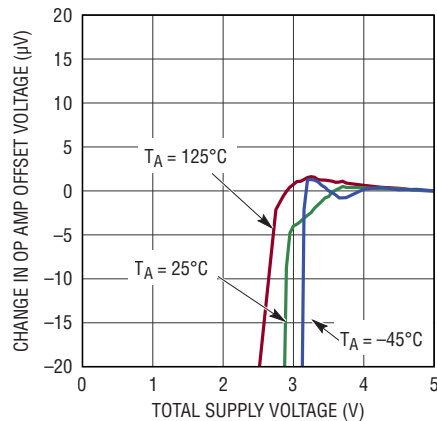
PIN FUNCTIONS (DFN/MSOP)

V+ (Pin 9/Pin 11): Positive Supply Pin.

V− (EXPOSED PAD Pin 15/Pin 8): Negative Supply Pin.

OUT (Pin 8/Pin 9): Output Pin.

+INA (Pin 1/Pin 1): Noninverting Gain-of-1 Input Pin. Connects a 22.5k internal resistor to the internal op amp's noninverting input.

+INB (Pin 3/Pin 3): Noninverting Gain-of-3 Input Pin. Connects a 7.5k internal resistor to the internal op amp's noninverting input.

+INC (Pin 5/Pin 5): Noninverting Gain-of-9 Input Pin. Connects a 2.5k internal resistor to the internal op amp's noninverting input.

−INA (Pin 14/Pin 16): Inverting Gain-of-1 input Pin. Connects a 22.5k internal resistor to the internal op amp's inverting input.

−INB (Pin 12/Pin 14): Inverting Gain-of-3 input Pin. Connects a 7.5k internal resistor to the internal op amp's inverting input.

−INC (Pin 10/Pin 12): Inverting Gain-of-9 input Pin. Connects a 2.5k internal resistor to the internal op amp's inverting input.

REF (Pin 7/NA): Reference Input Pin. Sets the output level when the difference between the inputs is zero.

REF1 (NA/Pin 6): Reference 1 Input Pin. With REF2, sets the output level when the difference between the inputs is zero.

REF2 (NA/Pin 7): Reference 2 Input. Pin. With REF1, sets the output level when the difference between the inputs is zero.

$\overline{\text{SHDN}}$ (Pin 6/Pin 10): Shutdown Pin. Amplifier is active when this pin is tied to V+ or left floating. Pulling the pin >2.5V below V+ causes the amplifier to enter a low power state.

BLOCK DIAGRAM

MSOP

DFN

19973 BD01

19973 BD02
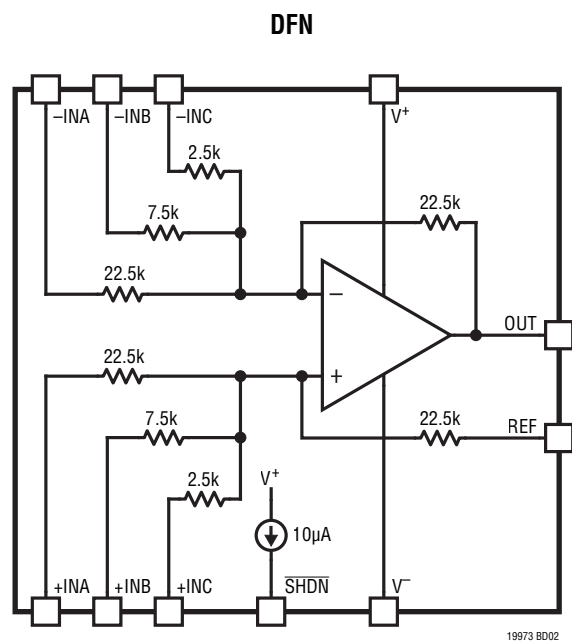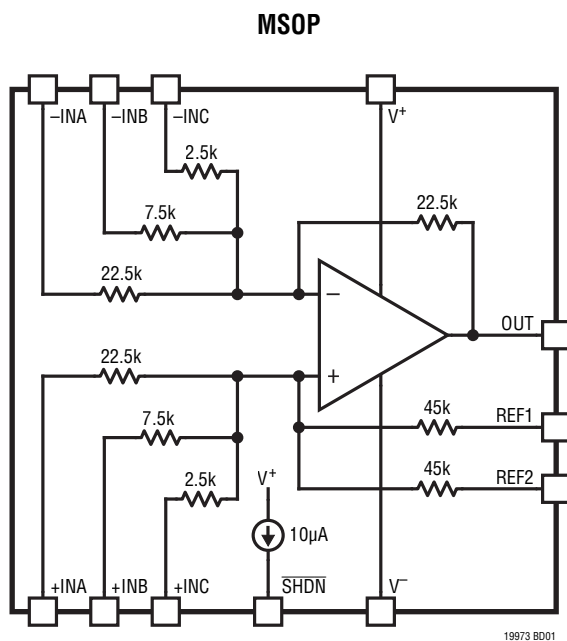
19973f

APPLICATIONS INFORMATION

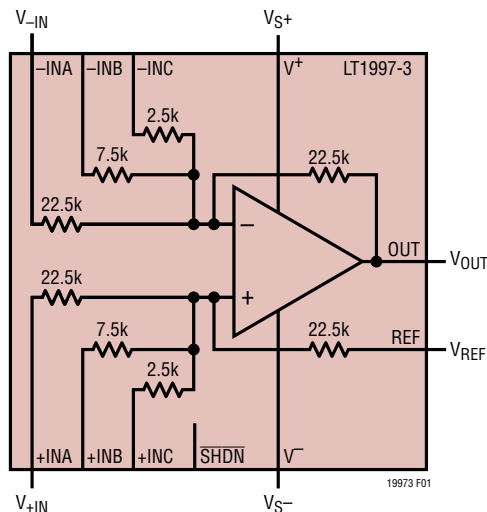**Figure 1. Difference Amplifier with Dual-Supply Operation (Gain = 1)**

Introduction

The LT1997-3 is a precision, high voltage general purpose op amp combined with a highly-matched resistor network. It can easily be configured into many different classical gain circuits without adding external components. The several pages of simple circuits in this data sheet demonstrate how easy the LT1997-3 is to use. It can be configured into a difference amplifier (Figure 1), as well as into inverting (Figure 7) and noninverting (Figure 3) single ended amplifiers. The LT1997-3 provides the resistors and op amp together in a small package in order to save board space and reduce complexity. Highly accurate measurement circuits can be easily constructed with the LT1997-3. The circuits can be tailored to specific measurement applications.

Common Mode Voltage Range

The common mode voltage range of the LT1997-3 is set by the voltage range allowed on the LT1997-3's input pins and by the input voltage range of the internal op amp.

The internal op amp of LT1997-3 has 2 operating regions: a) if the common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is between V^- and $V^+ - 1.75V$, the op amp operates in its normal region; b) If V_{CMOP} is between $V^+ - 1.75V$ and $V^- + 76V$, the op amp continues to operate, but in its Over-The-Top (OTT) region with degraded performance (see Over-The-Top Operation section of this data sheet for more detail).

The LT1997-3 will not operate correctly if the common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is below V^-, but the part will not be damaged as long as V_{CMOP} is greater than $V^- - 25V$ and the junction temperature of the LT1997-3 does not exceed 150°C.

The allowed voltage range on LT1997-3's input pins are as follows: The voltages at +INA and −INA input pins should never be higher than $V^- + 160V$ or lower than $V^- - 160V$ under any circumstances; The voltages at +INB, −INB, +INC and −INC input pins should not go below $V^- - 0.3V$ or above $V^- + 80V$.

The common-mode voltage at the inputs of the internal op amp (V_{CMOP}) is determined by the voltages on pins +INA, +INB, +INC and REF (see the "Calculating Input Voltage Range" section). This condition is true provided that the internal op amp's output is not clipped and feedback maintains the internal op amp's inputs at the same voltage.

In addition to the limits mentioned above, the common mode input voltage of the amplifier should be chosen so that the input resistors do not dissipate too much power. The power dissipated in a 22.5k resistor must be less than 1.5W. It must be less than 0.5W for the 7.5k resistor and less than 0.165W for the 2.5k resistor. For most applications, the pin voltage limitations will be reached before the resistor power limitation is reached.

Calculating Input Voltage Range

Figure 2 shows the LT1997-3 in the generalized case of a difference amplifier, with the inputs shorted for the common mode calculation. The values of R_F and R_G are dictated by how the positive inputs and REF pin are connected.

APPLICATIONS INFORMATION

By superposition we can write:

$$V_{CMOP} = V_{EXT} \bullet \frac{R_F}{R_F + R_G} + V_{REF} \bullet \frac{R_G}{R_F + R_G}$$

Or, solving for V_{EXT}:

$$V_{EXT} = V_{CMOP} \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$

But valid V_{CMOP} voltages are limited to $V_S+ - 1.75V$ ($V_S- + 76V$ OTT) on the high side and V_S- on the low side, so:

$$MAX\ V_{EXT} = \left(V_S+ -1.75\right) \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$

and:

$$MIN\ V_{EXT} = \left(V_S-\right) \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$
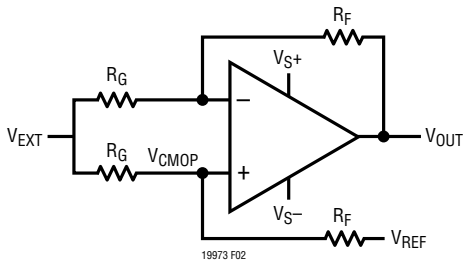

Figure 2. Calculating the Common Mode Input Voltage Range

Exceeding the MAX V_{EXT} limit will cause the amplifier to transition into the Over-The-Top region. The maximum input voltage for the Over-The-Top region is:

$$MAX\ V_{EXTOTT} = \left(V_S- +76\right) \bullet \left(1 + \frac{R_G}{R_F}\right) - V_{REF} \bullet \frac{R_G}{R_F}$$

Keep in mind that the above MAX and MIN values for input voltage range should not exceed the allowed voltage range specified earlier for LT1997-3's input pins.

The negative inputs are not limited by the internal op amp common mode range (V_{CMOP}) because they do not affect it.

They are limited by the output swing of the amplifier (and obviously by the allowed voltage range for the input pins).

Over-The-Top Operation

When the input common mode voltage of the internal op amp (V_{CMOP}) in the LT1997-3 is biased near or above the V+ supply, the op amp is operating in the Over-The-Top (OTT) region. The op amp continues to operate with an input common mode voltage of up to 76V above V− (regardless of the positive power supply voltage V+), but its performance is degraded. The op amp's input bias currents change from under ±2nA to 14µA. The op amp's input offset current rises to ±50nA, which adds ±1.1mV to the output offset voltage.

In addition, when operating in the Over-The-Top region, the differential input impedance decreases from 1MΩ in normal operation to approximately 3.7kΩ in Over-The-Top operation. This resistance appears across the summing nodes of the internal op amp and boosts noise and offset while decreasing speed. Noise and offset will increase by between 75% and 450% depending on the gain setting. The bandwidth will be reduced by 2X to 5.5X. For more detail on Over-The-Top operation, consult the LT6015 data sheet.

The Classical Noninverting Amplifier: High Input Z

A common op amp configuration enabled by the LT1997-3 is the noninverting amplifier. Figure 3 shows the textbook representation of the circuit on the top. The LT1997-3 is shown on the bottom configured in a precision gain of 5.5. One of the benefits of the noninverting op amp configuration is that the input impedance is extremely high. The LT1997-3 maintains this benefit. A large number of gains can be achieved with the LT1997-3 in the noninverting configuration. The complete list of such Hi-Z input noninverting gain configuration is shown in Table 1. Many of these are also represented in Figure 4 in schematic form. Note that the positive inputs are connected such that the source impedance seen by the positive and negative inputs of the internal op amp are equal. This minimizes the offset voltage due to the input bias current of the op amp. The noise gain and amplifier's gain in the noninverting configuration are identical.

APPLICATIONS INFORMATION

NONINVERTING OP AMP CONFIGURATION

$$V_{OUT} = GAIN \cdot V_{IN}$$
$$GAIN = 1 + R_F/R_G$$
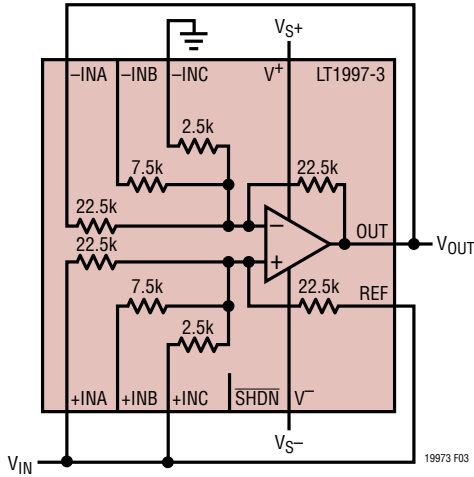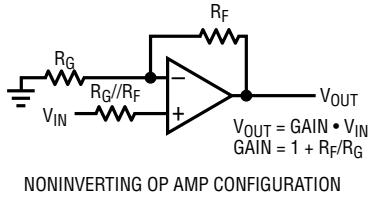
NONINVERTING OP AMP CONFIGURATION
IMPLEMENTED WITH THE LT1997-3, R_F = 11.25k, R_G = 2.5k, GAIN = 5.5

GAIN IS ACHIEVED BY GROUNDING, FLOATING OR FEEDING BACK
THE AVAILABLE RESISTORS TO ARRIVE AT THE DESIRED R_F AND R_G

Figure 3. The LT1997-3 Configured as a Noninverting Op Amp

Table 1. Configuring the Negative Pins for Noninverting Gains. The Positive Inputs Are Driven as Shown in the Examples in Figure 4

| Gain	Negative Input Connections		
	-INA	-INB	-INC
1	V_{OUT}	V_{OUT}	V_{OUT}
1.077	GND	V_{OUT}	V_{OUT}
1.1	GND	OPEN	V_{OUT}
1.25	GND	V_{OUT}	OPEN
1.273	V_{OUT}	GND	V_{OUT}
1.3	OPEN	GND	V_{OUT}
1.4	GND	GND	V_{OUT}
2	GND	OPEN	OPEN
2.5	V_{OUT}	GND	OPEN
2.8	V_{OUT}	V_{OUT}	GND
3.25	OPEN	V_{OUT}	GND
3.5	GND	V_{OUT}	GND
4	OPEN	GND	OPEN
5	GND	GND	OPEN
5.5	V_{OUT}	OPEN	GND
7	V_{OUT}	GND	GND
10	OPEN	OPEN	GND
11	GND	OPEN	GND
13	OPEN	GND	GND
14	GND	GND	GND

APPLICATIONS INFORMATION
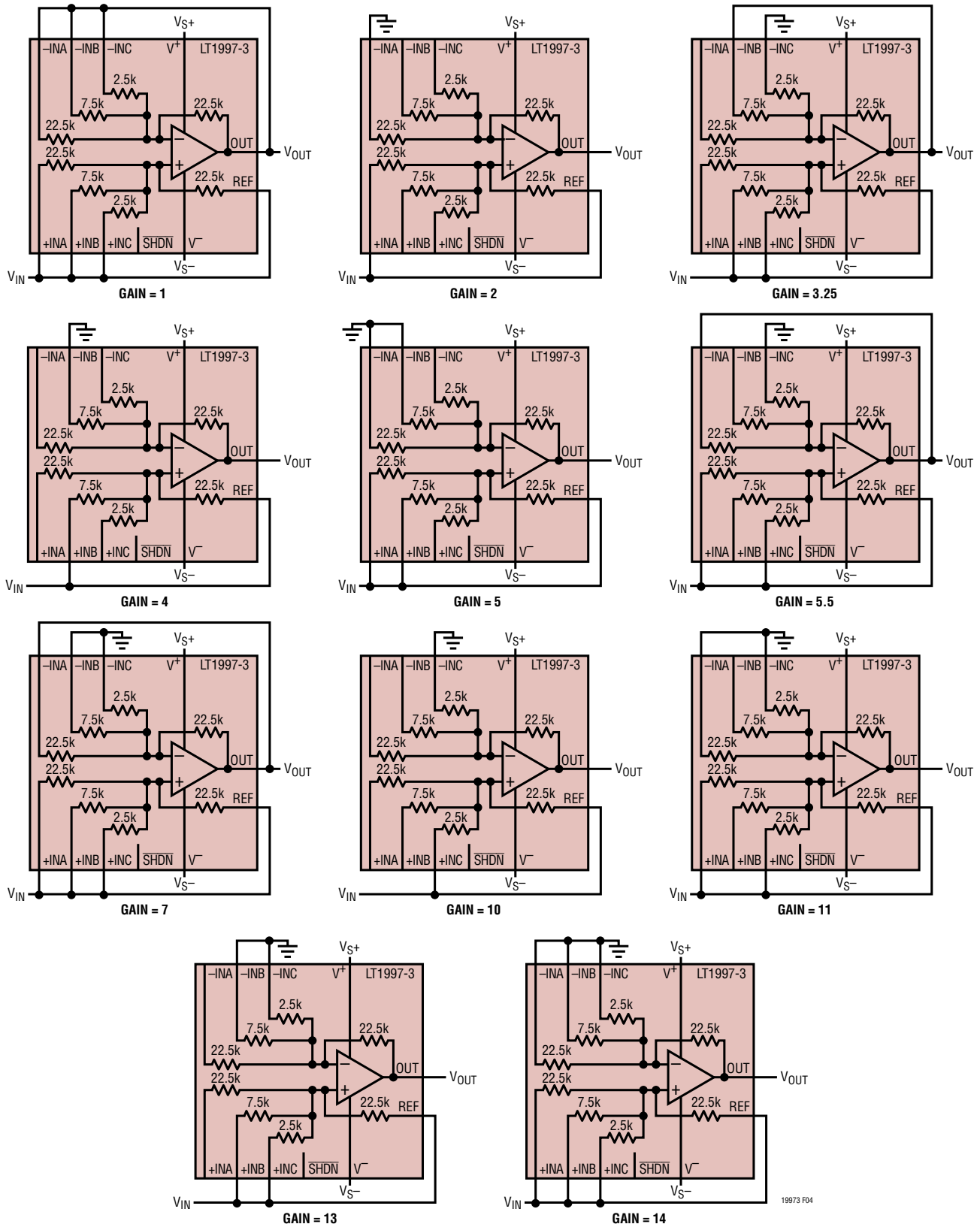
Figure 4. Some Implementations of Classical Noninverting Gains Using the LT1997-3. High Input Z is Maintained

APPLICATIONS INFORMATION

Attenuation

The positive input resistors can be configured to attenuate the input signal (Figure 5). This allows a trade-off to be made between input range and precision. Attenuating the input can prevent the op amp from entering the less precise Over-the-Top operating region at the cost of decreasing the output signal. The four positive resistors (R_{+INA}, R_{+INB}, R_{+INC}, R_{REF}) can be arranged to make many precise input attenuators. These are shown in Table 2.

ATTENUATOR

ATTENUATING THE POSITIVE INPUT
BY GROUNDING AN UNUSED INPUT
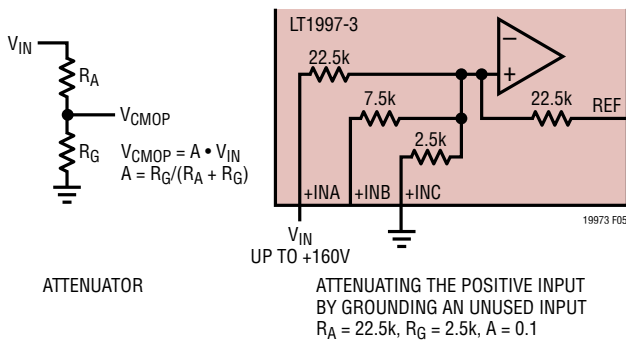R_A = 22.5k, R_G = 2.5k, A = 0.1

Figure 5. The Input of the LT1997-3 Can Be Attenuated to Increase the Usable Input Range. The +INA Input Can Be Taken to ±160V.

The attenuations and noninverting gains are set independently and can be combined to produce even more gain options. 346 unique gains between 0.0714 and 14 (Figure 6) can be realized. When using the positive side resistors as an attenuator, the benefit of canceling input bias current effects on offset voltage reduces. The impedance seen by the two op amp input nodes will not be identical.
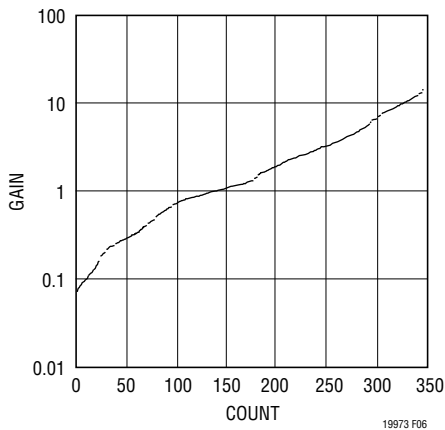
Figure 6. Many Unique Gains Can Be Achieved by Combining Attenuation with Noninverting Gain

Table 2. Configuring the Positive Pins for Various Attenuations

Gain	Positive Input Connections			
	+INA	+INB	+INC	REF
0.0714	V_{IN}	GND	GND	GND
0.0769	V_{IN}	GND	GND	OPEN
0.0909	V_{IN}	OPEN	GND	GND
0.1	V_{IN}	OPEN	GND	OPEN
0.143	V_{IN}	GND	GND	V_{IN}
0.182	V_{IN}	OPEN	GND	V_{IN}
0.2	V_{IN}	GND	OPEN	GND
0.214	GND	V_{IN}	GND	GND
0.231	OPEN	V_{IN}	GND	GND
0.25	V_{IN}	GND	OPEN	OPEN
0.286	V_{IN}	V_{IN}	GND	GND
0.308	V_{IN}	V_{IN}	GND	OPEN
0.357	V_{IN}	V_{IN}	GND	V_{IN}
0.4	V_{IN}	GND	OPEN	V_{IN}
0.5	V_{IN}	OPEN	OPEN	GND
0.6	GND	V_{IN}	OPEN	GND
0.643	GND	GND	V_{IN}	GND
0.692	OPEN	GND	V_{IN}	GND
0.714	V_{IN}	GND	V_{IN}	GND
0.75	OPEN	V_{IN}	OPEN	GND
0.769	V_{IN}	GND	V_{IN}	OPEN
0.786	V_{IN}	GND	V_{IN}	V_{IN}
0.8	V_{IN}	V_{IN}	OPEN	GND
0.818	GND	OPEN	V_{IN}	GND
0.857	GND	V_{IN}	V_{IN}	GND
0.9	OPEN	OPEN	V_{IN}	GND
0.909	V_{IN}	OPEN	V_{IN}	GND
0.923	OPEN	V_{IN}	V_{IN}	GND
0.929	V_{IN}	V_{IN}	V_{IN}	GND
1	V_{IN}	V_{IN}	V_{IN}	V_{IN}

APPLICATIONS INFORMATION

The Inverting Configuration

The inverting amplifier, shown in Figure 7, is another classical op amp configuration. The circuit is actually identical to the noninverting amplifier of Figure 3, except that V_{IN} and GND have been swapped. The list of available gains is shown in Table 3, and some of the circuits are shown in Figure 8. Noise gain is 1+|Gain|, as is the usual case for inverting amplifiers. For the best DC precision, match the source impedances seen by the op amp inputs.

INVERTING OP AMP CONFIGURATION

$$V_{OUT} = GAIN \cdot V_{IN}$$
$$GAIN = -R_F/R_G$$
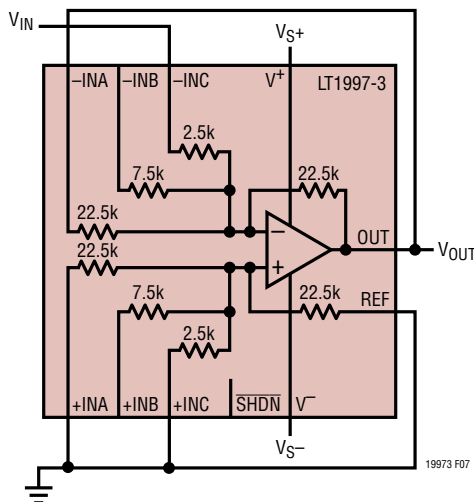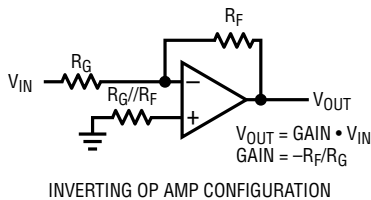
INVERTING OP AMP CONFIGURATION
IMPLEMENTED WITH THE LT1997-3, R_F = 11.25k, R_G = 2.5k, GAIN = –4.5

GAIN IS ACHIEVED BY GROUNDING, FLOATING OR FEEDING BACK
THE AVAILABLE RESISTORS TO ARRIVE AT THE DESIRED R_F AND R_G

Figure 7. The LT1997-3 Configured as an Inverting Op Amp

Table 3. Configuring the Negative Pins for Inverting Gains

Gain	Negative Input Connections		
	-INA	-INB	-INC
−0.077	V_{IN}	V_{OUT}	V_{OUT}
−0.1	V_{IN}	OPEN	V_{OUT}
−0.25	V_{IN}	V_{OUT}	OPEN
−0.273	V_{OUT}	V_{IN}	V_{OUT}
−0.3	OPEN	V_{IN}	V_{OUT}
−0.4	V_{IN}	V_{IN}	V_{OUT}
−1	V_{IN}	OPEN	OPEN
−1.5	V_{OUT}	V_{IN}	OPEN
−1.8	V_{OUT}	V_{OUT}	V_{IN}
−2.25	OPEN	V_{OUT}	V_{IN}
−2.5	V_{IN}	V_{OUT}	V_{IN}
−3	OPEN	V_{IN}	OPEN
−4	V_{IN}	V_{IN}	OPEN
−4.5	V_{OUT}	OPEN	V_{IN}
−6	V_{OUT}	V_{IN}	V_{IN}
−9	OPEN	OPEN	V_{IN}
−10	V_{IN}	OPEN	V_{IN}
−12	OPEN	V_{IN}	V_{IN}
−13	V_{IN}	V_{IN}	V_{IN}

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APPLICATIONS INFORMATION
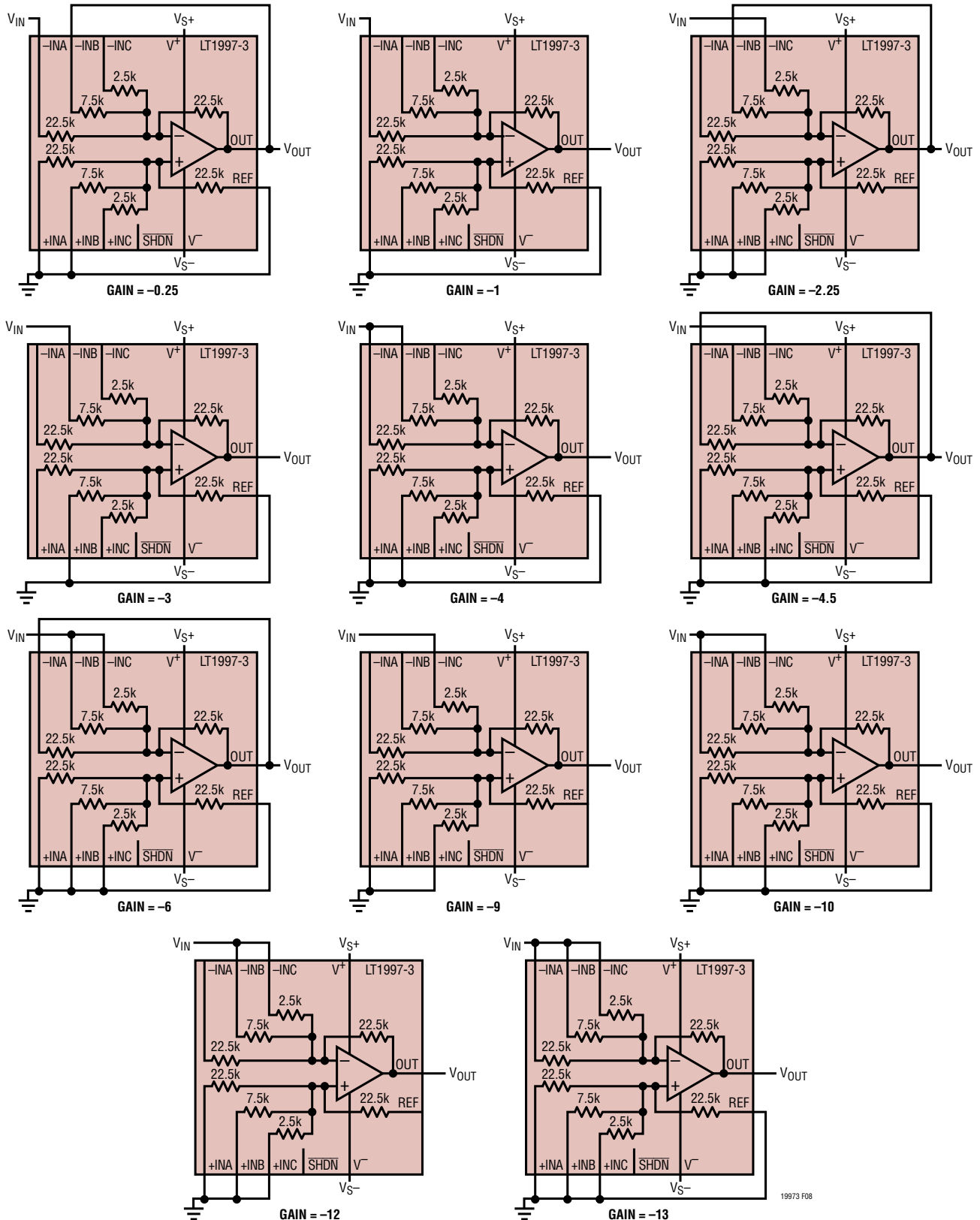

Figure 8. Inverting Gains with Input Impedance that Varies from 1.73kΩ (Gain = −13) to 22.5kΩ (Gain = −1)

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For more information www.linear.com/LT1997-3

APPLICATIONS INFORMATION

Difference Amplifiers

The LT1997-3 is ideally suited to be used as a difference amplifier. Figure 9 shows the basic 4-resistor difference amplifier and the LT1997-3. A difference gain of 3 is shown, but can be altered by additional dashed connections. By connecting the 22.5k resistors in parallel, the gain is reduced by a factor of 2. Of course there are many possible gains. Table 4 shows the difference gains and how they are achieved. Note that, as for inverting amplifiers, the noise gain is equal to the signal gain plus 1.
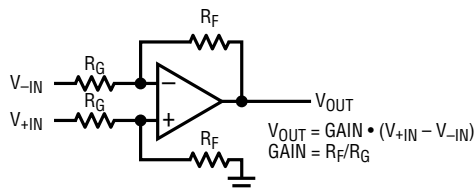
DIFFERENCE AMPLIFIER CONFIGURATION

$$V_{OUT} = GAIN \cdot (V_{+IN} - V_{-IN})$$
$$GAIN = R_F/R_G$$
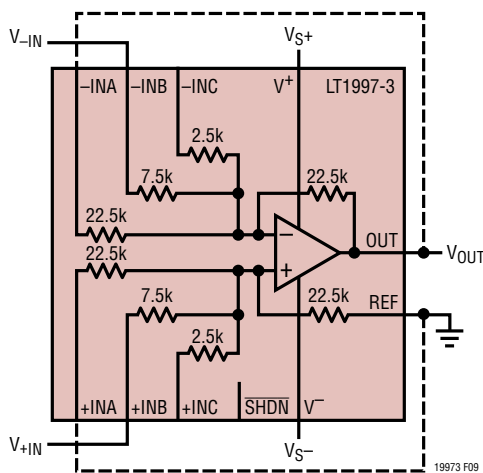
DIFFERENCE AMPLIFIER CONFIGURATION IMPLEMENTED WITH THE LT1997-3, R_F = 22.5k, R_G = 7.5k, GAIN = 3

ADDING THE DASHED CONNECTIONS CONNECT THE TWO 22.5k RESISTORS IN PARALLEL, SO R_F IS REDUCED TO 11.25k. THE GAIN BECOMES 11.25k/7.5k = 1.5

Figure 9. The LT1997-3 Configured as a Difference Amplifier. Gain Is Set by Connecting the Correct Resistors or Combinations of Resistors. Gain of 3 Is Shown, with Dashed Lines Modifying It to a Gain of 1.5

The Common Mode Voltage at the inputs of the internal op amp (V_{CMOP}) is set by the voltages at pins +INA, +INB, +INC and REF.

Table 4. Difference Amplifier Gains

Gain	V+IN	V−IN	OUT	GND (REF)
0.077	+INA	−INA	−INB, −INC	+INB, +INC
0.1	+INA	−INA	−INC	+INC
0.25	+INA	−INA	−INB	+INB
0.273	+INB	−INB	−INA, −INC	+INA, +INC
0.3	+INB	−INB	−INC	+INC
0.4	+INA, +INB	−INA, −INB	−INC	+INC
1	+INA	−INA		
1.5	+INB	−INB	−INA	+INA
1.8	+INC	−INC	−INA, −INB	+INA, +INB
2.25	+INC	−INC	−INB	+INB
2.5	+INA, +INC	−INA, −INC	−INB	+INB
3	+INB	−INB		
4	+INA, +INB	−INA, −INB		
4.5	+INC	−INC	−INA	+INA
6	+INB, +INC	−INB, −INC	−INA	+INA
9	+INC	−INC		
10	+INA, +INC	−INA, −INC		
12	+INB, +INC	−INB, −INC		
13	+INA, +INB, +INC	−INA, −INB, −INC		

APPLICATIONS INFORMATION

GAIN = 0.25

GAIN = 1

GAIN = 2.25

GAIN = 3

GAIN = 4

GAIN = 4.5

GAIN = 6

GAIN = 9

GAIN = 10

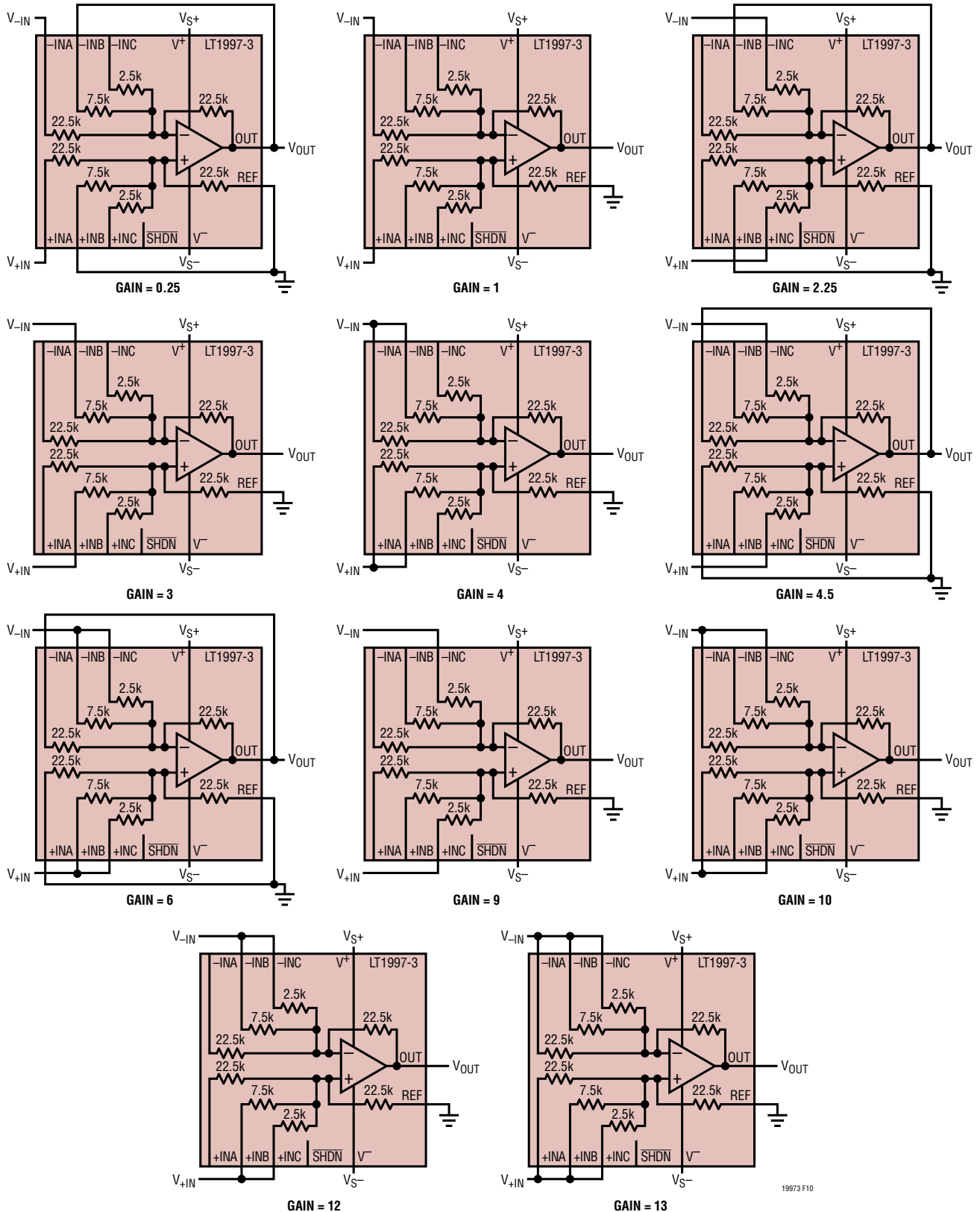**GAIN = 12**

GAIN = 13

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Figure 10. Many Difference Amplifier Gains Can Be Achieved by Strapping Pins
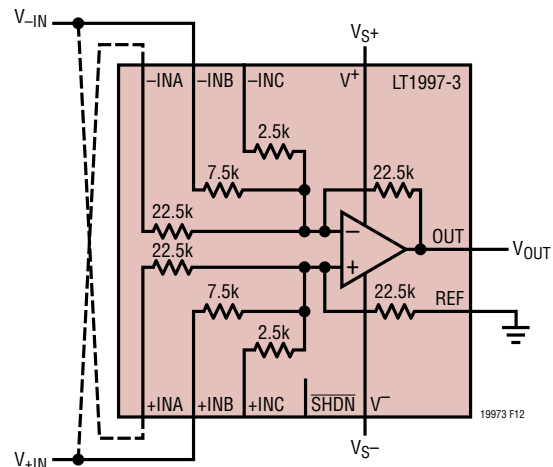
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22

APPLICATIONS INFORMATION

Difference Amplifier: Additional Integer Gains Using Cross-Coupling

Figure 11 shows the basic difference amplifier as well as the LT1997-3 with cross-coupled inputs. The additional dashed connections reduce the differential gain from 3 to 2. Using this method, additional integer gains are achievable, as shown in Table 5, so that all integer gains from 1 to 13 are achieved with the LT1997-3. Note that the equations can be written by inspection from the V_{+IN} connections, and that the V_{-IN} connections are simply the opposite (swap + for − and − for +). Noise gain, bandwidth, and input impedance specifications for the various cases are also shown. Schematics of the difference amplifiers using cross-coupling are shown in Figure 12. Additional non-integer gains produced with cross-coupling are listed in Table 6.
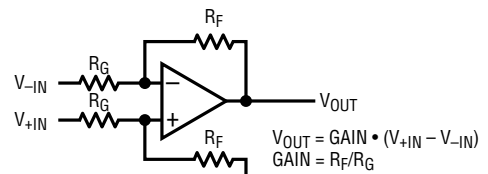
DIFFERENCE AMPLIFIER CONFIGURATION

$$V_{OUT} = GAIN \cdot (V_{+IN} - V_{-IN})$$
$$GAIN = R_F/R_G$$

DIFFERENCE AMPLIFIER CONFIGURATION
IMPLEMENTED WITH THE LT1997-3, R_F = 22.5k, R_G = 7.5k, GAIN = 3

GAIN CAN BE ADJUSTED BY CROSS-COUPLING THE INPUTS.
MAKING THE DASHED CONNECTIONS REDUCES THE GAIN FROM 3 TO 2

Figure 11. Cross-Coupling the Inputs of the LT1997-3 Allows Additional Integer Gains to Be Constructed. The LT1997-3 Provides All Integer Gains from 1 to 13

Table 5. Connections Using Cross-Coupling. Note that Equations Can Be Written by Inspection of the V_{+IN} Column

Gain	V_{+IN}	V_{-IN}	Equation	Noise Gain	−3dB BW (kHz)	Differential Input Impedance (kΩ)	Common Mode Input Impedance (kΩ)
2	+INB, −INA	−INB, +INA	3 − 1	5	540	11.25	14.1
5	+INC, −INB, −INA	−INC, +INB, +INA	9 − 3 − 1	14	222	3.5	12.1
7	+INC, +INA, −INB	−INC, −INA, +INB	9 + 1 − 3	14	222	3.5	12.1
8	+INC, −INA	−INC, +INA	9 − 1	11	277	4.5	12.4
11	+INC, +INB, −INA	−INC, −INB, +INA	9 + 3 − 1	14	222	3.5	12.1

Table 6. Additional Non-Integer Gains that Can Be Achieved Using Cross-Coupling

Gain	V_{+IN}	V_{-IN}	OUT	GND (REF)
0.143	+INA	−INA	+INB, −INC	−INB, +INC
0.2	−INA, +INB	+INA, −INB	−INC	+INC
0.333	+INB	−INB	+INA, −INC	−INA, +INC

APPLICATIONS INFORMATION

GAIN = 2

GAIN = 5
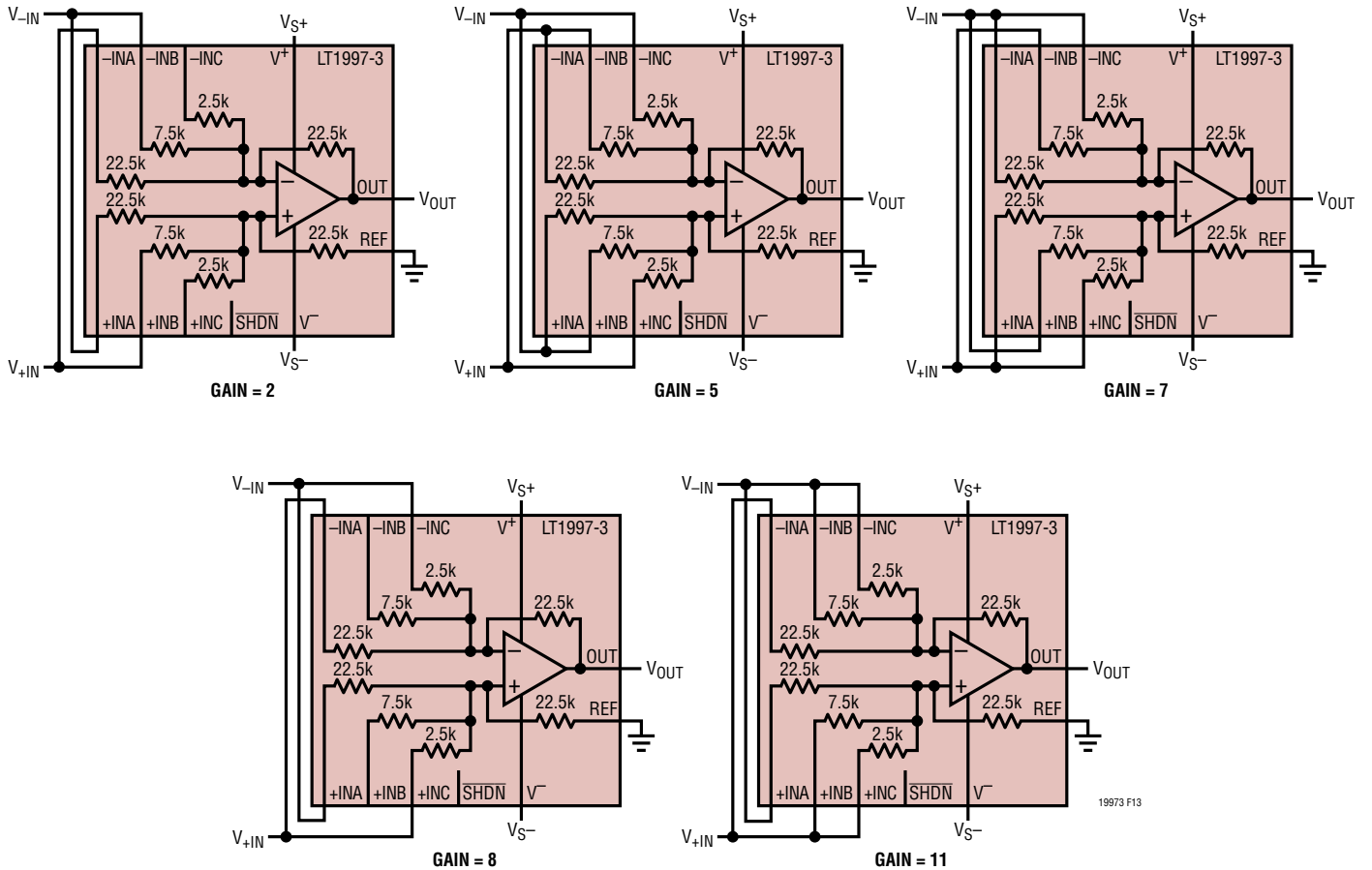
GAIN = 7

GAIN = 8

GAIN = 11

Figure 12. Integer Gain Difference Amplifiers Using Cross-Coupling

High Common Mode Voltage Difference Amplifiers

The input range of a difference amplifier can be extended by configuring the amplifier to divide the input common mode voltage. Figure 13 shows the basic circuit on the top. The effective input voltage range of the circuit is extended by the fact that resistors R_T attenuate the common mode (CM) voltage seen by the internal op amp inputs (V_{CMOP}). For the LT1997-3, the most useful resistors for R_G are the +INA and –INA 22.5kΩ resistors, because they do not have diode clamps to the V_S- supply and therefore can be taken beyond both rails. +INB, –INB, +INC and –INC pins can be taken 80V above V_S-, but not below V_S-. As before, the input common mode of the internal op amp is the limiting factor and is set by the voltage at the op amp's positive input (V_{CMOP}). By superposition we can write:

$$V_{CMOP} = V_{EXT} \bullet \frac{R_F \| R_T}{R_G + R_F \| R_T} + V_{REF} \bullet \frac{R_G \| R_T}{R_F + R_G \| R_T}$$
$$+ V_{TERM} \bullet \frac{R_F \| R_G}{R_T + R_F \| R_G}$$

Solving for V_{EXT}:

$$V_{EXT} = \left(1 + \frac{R_G}{R_F \| R_T}\right) \bullet \left(\begin{array}{l} V_{CMOP} - V_{REF} \bullet \dfrac{R_G \| R_T}{R_F + R_G \| R_T} \\[2ex] - V_{TERM} \bullet \dfrac{R_F \| R_G}{R_T + R_F \| R_G} \end{array} \right)$$

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APPLICATIONS INFORMATION

Given the values of the resistors in the LT1997-3, this equation has been simplified and evaluated, and the resulting equations are provided in Table 7. Substituting $V_{S+} - 1.75V$ and $V_{S}-$ for V_{LIM} will give the valid upper and lower common mode extremes respectively for the normal operating region of the op amp. Substituting $V_{S}- + 76V$ and $V_{S}-$ for V_{LIM} will give the valid upper and lower common mode extremes respectively for the Over-The-Top region of the op amp (see Over-The-Top Operation section of this data sheet for more detail). Following are sample calculations for the case shown in Figure 13. Note that +INC and −INC are terminated so row 3 of Table 7 provides the equation:

$$\text{MAX } V_{EXT} = 11 \bullet (V_{S}+ -1.75) - V_{REF} - 9 \bullet V_{TERM}$$
$$= 11 \bullet (10.25V) - 2.5 - 9 \bullet 12$$
$$= 2.25V$$

and:

$$\text{MIN } V_{EXT} = 11 \bullet (V_{S}-) - V_{REF} - 9 \bullet V_{TERM}$$
$$= 11 \bullet (0) - 2.5 - 9 \bullet 12$$
$$= -110.5V$$

If the calculated V_{EXT} voltage exceeds the 160V absolute maximum rating of the +INA, −INA pins, 160V or −160V would become the de facto common mode limit. Several more examples of high CM circuits are shown in Figure 14, Figure 15 and Figure 16 for various supplies.
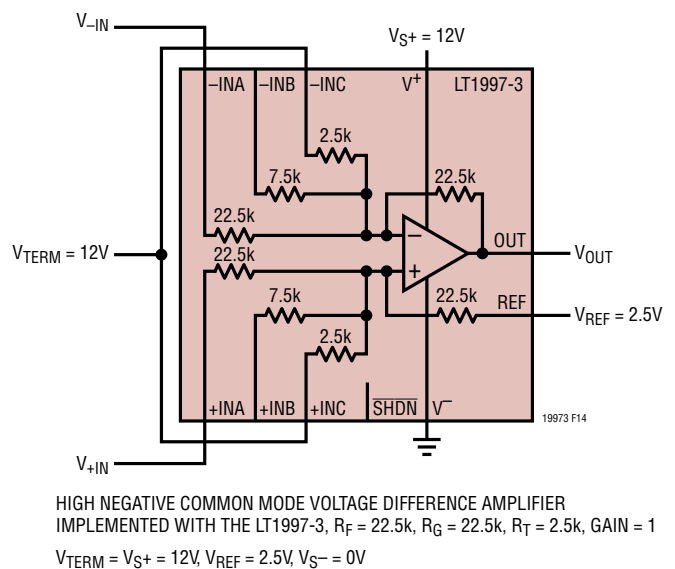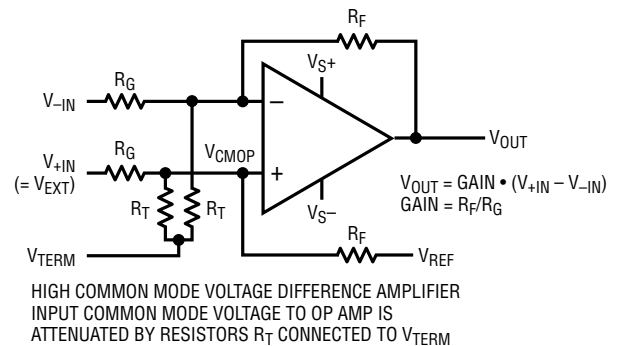

HIGH COMMON MODE VOLTAGE DIFFERENCE AMPLIFIER
INPUT COMMON MODE VOLTAGE TO OP AMP IS
ATTENUATED BY RESISTORS R_T CONNECTED TO V_{TERM}

$V_{OUT} = \text{GAIN} \bullet (V_{+IN} - V_{-IN})$
$\text{GAIN} = R_F/R_G$

HIGH NEGATIVE COMMON MODE VOLTAGE DIFFERENCE AMPLIFIER
IMPLEMENTED WITH THE LT1997-3, $R_F = 22.5k$, $R_G = 22.5k$, $R_T = 2.5k$, GAIN = 1
$V_{TERM} = V_{S}+ = 12V$, $V_{REF} = 2.5V$, $V_{S}- = 0V$

Figure 13. Extending Common Mode Input Range

Table 7. Input Common Mode Voltage Ranges for the LT1997-3 when Configured as a High Common Mode Voltage Difference Amplifier

Gain	V+IN	V−IN	R_T	Noise Gain	Max, Min V_{EXT} (Substitute $V_{S}-$ − 1.75 (Normal Region) or $V_{S}-$ + 76 (OTT), and $V_{S}-$ for V_{LIM})
1	+INA	−INA		2	$2 \bullet V_{LIM} - V_{REF}$
1	+INA	−INA	R_{+INB}, R_{-INB}	5	$5 \bullet V_{LIM} - V_{REF} - 3 \bullet V_{TERM}$
1	+INA	−INA	R_{+INC}, R_{-INC}	11	$11 \bullet V_{LIM} - V_{REF} - 9 \bullet V_{TERM}$
1	+INA	−INA	$R_{+INB}\|\|R_{+INC}$, $R_{-INB}\|\|R_{-INC}$	14	$14 \bullet V_{LIM} - V_{REF} - 12 \bullet V_{TERM}$