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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

–36V, 600mA Negative Linear Regulator with Programmable Current Limit

FEATURES

- **Output Current: 600mA**
- **Single Resistor Sets Output Voltage**
- **50µA SET Pin Current: ±1% Initial Accuracy**
- **Programmable Current Limit**
- **Positive or Negative Output Current Monitor**
- **Parallelable for Higher Current and Heat Spreading**
- **Low Dropout Voltage: 300mV**
- **Low Output Noise: 18µV_{RMS} (10Hz to 100kHz)**
- **Configurable as 3-Terminal Floating Regulator**
- **Wide Input Voltage Range: –1.5V to –36V**
- **Rail-to-Rail Output Voltage Range: 0V to –32V**
- Positive/Negative Shutdown Logic or UVLO
- Programmable Cable Drop Compensation
- Load Regulation: 1.2mV (1mA to 600mA)
- Stable with 4.7µF Minimum Output Capacitor
- Stable with Ceramic or Tantalum Capacitors
- Thermally Enhanced 12-Lead MSOP and 10-Lead 0.75mm × 3mm × 3mm DFN Packages

APPLICATIONS

- Post Regulator for Switching Supplies
- Low Noise Instrumentation and RF Supplies
- Rugged Industrial Supplies
- Precision Power Supplies

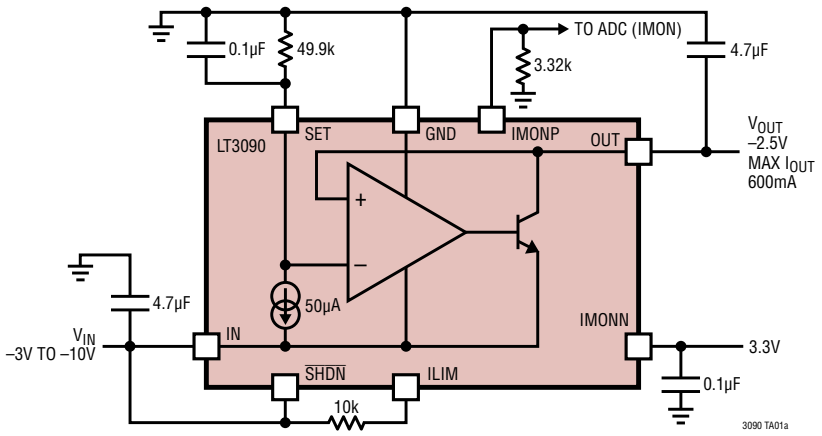
DESCRIPTION

The LT®3090 is a 600mA, low dropout negative linear regulator that is easily parallelable to increase output current or spread heat on surface mounted boards. Designed with a precision current reference followed by a high performance rail-to-rail voltage buffer, this regulator finds use in applications requiring precision output, high current with no heat sink, output adjustability to zero and low dropout voltage. The device can also be configured as a 3-terminal floating regulator.

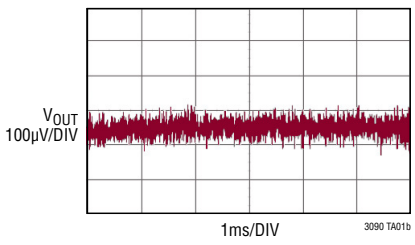
The LT3090 features fast transient response, high PSRR and output noise as low as 18µV_{RMS}. The LT3090 generates a wide output voltage range (0V to –32V) while maintaining unity gain operation. This yields virtually constant bandwidth, load regulation, PSRR and noise, regardless of the programmed output voltage.

The LT3090 supplies 600mA at a typical dropout voltage of 300mV. Operating quiescent current is nominally 1mA and drops to << 1µA in shutdown. A single resistor adjusts the LT3090's precision programmable current limit. The LT3090's positive or negative current monitor either sources a current (0.5mA/A) or sinks a current (1mA/A) proportional to output current. Built-in protection includes reverse output protection, internal current limit with foldback and thermal shutdown with hysteresis.

TYPICAL APPLICATION



Output Noise: 10Hz to 100kHz



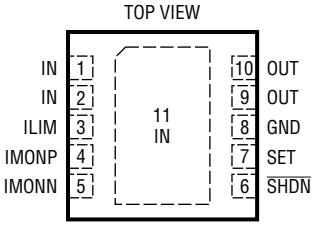
V_{IN}: –3.5V
V_{OUT}: –2V
C_{OUT}: 4.7µF, C_{SET}: 0.1µF
I_L: 600mA

ABSOLUTE MAXIMUM RATINGS

(Note 1)

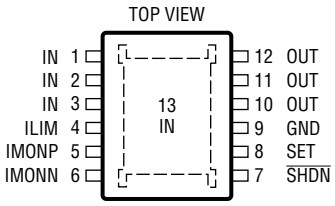
IN Pin Voltage (Note 3)
  with Respect to GND Pin .....0.3V, –40V
ILIM Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 0.7V
IMONP Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 40V
  with Respect to GND Pin .....–40V, 20V
  with Respect to IMONN Pin .....–40V, 20V
IMONN Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 40V
  with Respect to GND Pin .....–40V, 20V
$\overline{SHDN}$ Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 55V
  with Respect to GND Pin .....–40V, 20V
SET Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 36V
  with Respect to GND Pin .....±36V
SET Pin Current (Note 9).....±5mA
OUT Pin Voltage
  with Respect to IN Pin (Note 3) .....–0.3V, 36V
  with Respect to GND Pin .....±36V
Output Short-Circuit Duration ..... Indefinite
Operating Junction Temperature Range (Note 2)
  E-, I-Grade ..... –40°C to 125°C
  MP-Grade ..... –55°C to 150°C
  H-Grade ..... –40°C to 150°C
Storage Temperature Range .....–65°C to 150°C
Lead Temperature (Soldering, 10 Sec)
  MSE Package .....300°C

PIN CONFIGURATION



DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 34°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 11) IS IN, MUST BE SOLDERED TO PCB



MSE PACKAGE
12-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 33°C/W, θ_{JC} = 8°C/W
EXPOSED PAD (PIN 13) IS IN, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3090EDD#PBF	LT3090EDD#TRPBF	LGHJ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3090IDD#PBF	LT3090IDD#TRPBF	LGHJ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 125°C
LT3090HDD#PBF	LT3090HDD#TRPBF	LGHJ	10-Lead (3mm x 3mm) Plastic DFN	–40°C to 150°C
LT3090MPDD#PBF	LT3090MPDD#TRPBF	LGHJ	10-Lead (3mm x 3mm) Plastic DFN	–55°C to 150°C
LT3090EMSE#PBF	LT3090EMSE#TRPBF	3090	12-Lead Plastic MSOP	–40°C to 125°C
LT3090IMSE#PBF	LT3090IMSE#TRPBF	3090	12-Lead Plastic MSOP	–40°C to 125°C
LT3090HMSE#PBF	LT3090HMSE#TRPBF	3090	12-Lead Plastic MSOP	–40°C to 150°C
LT3090MPMSE#PBF	LT3090MPMSE#TRPBF	3090	12-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum IN Voltage (Note 11)	I_{LOAD} = 100mA I_{LOAD} = 600mA	 ●	 –1.9	–1.5 –1.5	 	V V
SET Pin Current (I_{SET})	V_{IN} = –1.9V, I_{LOAD} = 1mA, –36V < V_{IN} < –1.9V, 1mA < I_{LOAD} < 600mA (Note 5)	 ●	49.5 49	50 50	50.5 51	µA µA
Output Offset Voltage V_{OS} (V_{OUT} – V_{SET})	V_{IN} = –1.9V, I_{LOAD} = 1mA, –36V < V_{IN} < –1.9V, 1mA < I_{LOAD} < 600mA (Note 5)	 ●	–1 –2	 	1 2	mV mV
Line Regulation: $\Delta I_{SET}/\Delta V_{IN}$ Line Regulation: $\Delta V_{OS}/\Delta V_{IN}$	V_{IN} = –1.9V to –36V, I_{LOAD} = 1mA V_{IN} = –1.9V to –36V, I_{LOAD} = 1mA			1.5 2.5		nA/V µV/V
Load Regulation: ΔI_{SET} Load Regulation: ΔV_{OS}	I_{LOAD} = 1mA to 600mA I_{LOAD} = 1mA to 600mA, V_{IN} = –1.9V (Note 6)	 ●		0.5 1.2	 2.5	nA mV
Output Regulation with SET Pin Voltage Change: $\Delta I_{SET}/\Delta V_{SET}$ $\Delta V_{OS}/\Delta V_{SET}$	 V_{SET} = 0V to –32V, V_{IN} = –36V, I_{LOAD} = 1mA V_{SET} = 0V to –32V, V_{IN} = –36V, I_{LOAD} = 1mA	 ● ●		 0.2 2.5	 1 30	 nA/V µV/V
Dropout Voltage V_{IN} = $V_{OUT(NOMINAL)}$ (Note 7)	I_{LOAD} = 1mA I_{LOAD} = 1mA I_{LOAD} = 100mA I_{LOAD} = 100mA I_{LOAD} = 600mA I_{LOAD} = 600mA	 ● ● ●		185 195 300 	230 270 240 300 360 450	mV mV mV mV mV mV
GND Pin Current V_{IN} = $V_{OUT(NOMINAL)}$ (Note 8)	I_{LOAD} = 10µA I_{LOAD} = 1mA I_{LOAD} = 100mA I_{LOAD} = 600mA	● ● ● ●		1 1.05 2.6 11.5	1.4 1.4 5 22.5	mA mA mA mA
Error Amplifier RMS Output Noise (Note 12)	I_{LOAD} = 600mA, BW = 10Hz to 100kHz, C_{OUT} = 4.7µF, C_{SET} = 0.1µF			18		μV_{RMS}
Reference Current RMS Output Noise (Note 12)	BW = 10Hz to 100kHz			10		nA_{RMS}
Ripple Rejection V_{IN} – V_{OUT} = –1.5V (Avg)	V_{RIPPLE} = 500mV_{P-P}, f_{RIPPLE} = 120Hz, I_{LOAD} = 100mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 10kHz, I_{LOAD} = 600mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF V_{RIPPLE} = 50mV_{P-P}, f_{RIPPLE} = 1MHz, I_{LOAD} = 600mA, C_{OUT} = 4.7µF, C_{SET} = 0.47µF		70	85 50 20		dB dB dB
$\overline{SHDN}$ Pin Turn-ON Threshold	Positive $\overline{SHDN}$ Rising Negative $\overline{SHDN}$ Rising (in Magnitude)	● ●	1.14 –1.36	1.23 –1.27	1.32 –1.18	V V
$\overline{SHDN}$ Pin Hysteresis	Positive $\overline{SHDN}$ Hysteresis Negative $\overline{SHDN}$ Hysteresis			180 190		mV mV
$\overline{SHDN}$ Pin Current (Note 10)	$V_{\overline{SHDN}}$ = 0V $V_{\overline{SHDN}}$ = 15V $V_{\overline{SHDN}}$ = –15V		 –7	 21 –4.5	±1 30 	µA µA µA
Quiescent Current in Shutdown	V_{IN} = –6V, $V_{\overline{SHDN}}$ = 0V V_{IN} = –6V, $V_{\overline{SHDN}}$ = 0V	 ●		0.1 	1 10	µA µA
Internal Current Limit (Note 13)	V_{IN} = –1.9V, V_{OUT} = 0V V_{IN} = –13V, V_{OUT} = 0V V_{IN} = –36V, V_{OUT} = 0V V_{IN} = –1.9V, ΔV_{OUT} < 10mV	● ● ●	650 20 630	750 350 35 730	850 60 830	mA mA mA mA
Programmable Current Limit	Programming Scale Factor: –36V < V_{IN} < –1.9V, I_{OUT} > 50mA (Note 14) Max I_{OUT}: V_{IN} = –1.9V, R_{ILIM} = 20k Max I_{OUT}: V_{IN} = –1.9V, R_{ILIM} = 100k	 ● ●	 460 85	10 500 100	 540 115	A•kΩ mA mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Positive Current Monitor (Note 15)	Positive Current Monitoring (IMONP) Scale Factor			0.5		mA/A
	I_{OUT} = 600mA, V_{IN} = –2.5V, V_{IMONN} = 2V, V_{IMONP} = 0V	●	280	300	320	µA
	I_{OUT} = 100mA, V_{IN} = –2.5V, V_{IMONN} = 2V, V_{IMONP} = 0V	●	42.5	50	57.5	µA
Negative Current Monitor	Negative Current Monitoring (IMONN) Scale Factor			1		mA/A
	I_{OUT} = 600mA, V_{IN} = –2.5V, V_{IMONN} = 0V, V_{IMONP} = –2.5V	●	560	600	640	µA
	I_{OUT} = 100mA, V_{IN} = –2.5V, V_{IMONN} = 0V, V_{IMONP} = –2.5V	●	85	100	115	µA
Minimum Required Load Current (Note 4)	–36V < V_{IN} < –1.9V	●	10			µA
Thermal Regulation ISET	10ms Pulse			0.04		%/W

Note 1. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2. The LT3090 is tested and specified under pulsed load conditions such that $T_J \cong T_A$. The LT3090E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization, and correlation with statistical process controls. The LT3090I is guaranteed over the full –40°C to 125°C operating junction temperature range. The LT3090MP is 100% tested and guaranteed over the full –55°C to 150°C operating junction temperature range. The LT3090H is 100% tested at the 150°C operating junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 3. Parasitic diodes exist internally between the OUT, SET, ILIM, $\overline{SHDN}$, IMONP, IMONN, and GND pins and the IN pin. Do not drive OUT, SET, ILIM, $\overline{SHDN}$, IMONP, IMONN, and GND pins more than 0.3V below the IN pin during fault conditions. These pins must remain at a voltage more positive than IN during normal operation.

Note 4. The LT3090 may go out of regulation if the minimum output current requirement is not satisfied.

Note 5. Maximum junction temperature limits operating conditions. The regulated output voltage specification does not apply for all possible combinations of input voltage and output current, primarily due to the internal current limit foldback which decreases current limit at $V_{OUT} – V_{IN} \geq 7V$. If operating at maximum output current, limit the input voltage range. If operating at maximum input voltage, limit the output current range.

Note 6. Load regulation is Kelvin sensed at the package.

Note 7. Dropout voltage is the minimum output-to-input voltage differential needed to maintain regulation at a specified output current. In dropout, the output voltage is: $V_{IN} + V_{DROPOUT}$.

Note 8. GND pin current is tested with $V_{IN} = V_{OUT(NOMINAL)}$ and a current source load. Therefore, the device is tested while operating in dropout. This is the worst-case GND pin current. GND pin current decreases at higher input voltages.

Note 9. The SET pin is clamped to OUT with diodes through 12k resistors. These resistors and diodes only carry current under transient overloads or fault conditions.

Note 10. Positive $\overline{SHDN}$ pin current flows into the $\overline{SHDN}$ pin.

Note 11. The $\overline{SHDN}$ threshold must be met to ensure device operation.

Note 12. Output noise decreases by adding a capacitor across the voltage setting resistor. Adding this capacitor bypasses the voltage setting resistor's thermal noise as well as the reference current's noise. Output noise then equals the error amplifier noise (see Applications Information section).

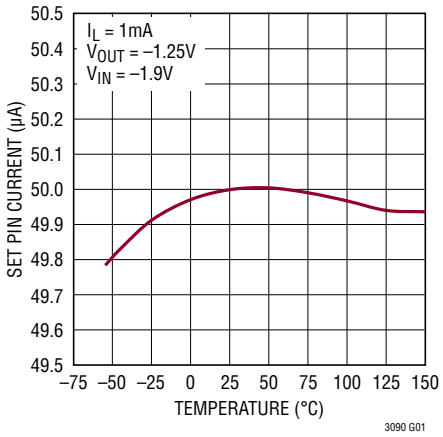
Note 13. The internal back-up current limit circuitry incorporates foldback protection that decreases current limit for $V_{OUT} – V_{IN} \geq 7V$. Some level of output current is provided at all $V_{OUT} – V_{IN}$ differential voltages. Please consult the Typical Performance Characteristic graph for current limit vs $V_{OUT} – V_{IN}$.

Note 14. The current limit programming scale factor is specified while the internal backup current limit is not active. Please note that the internal current limit has foldback protection for V_{OUT}-to-V_{IN} differentials greater than 7V.

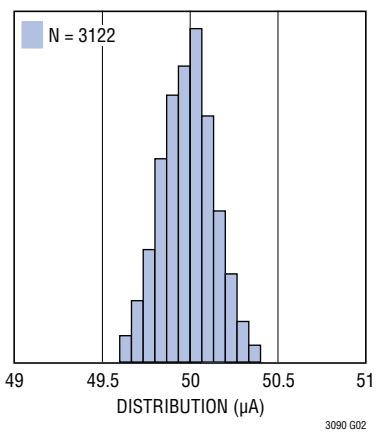
Note 15. For positive current monitoring, bias IMONN to ≥ 2V above IMONP.

TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

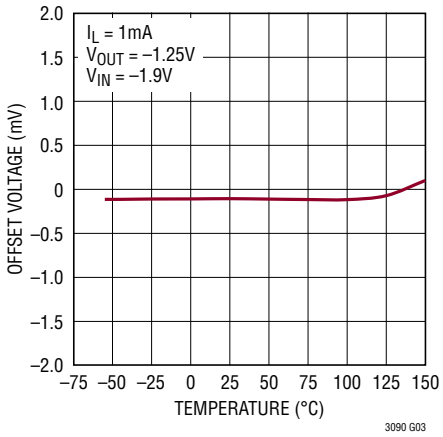
SET Pin Current



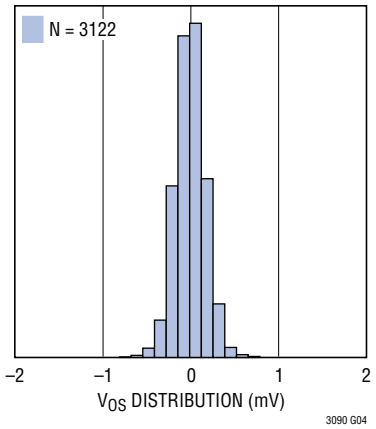
SET Pin Current



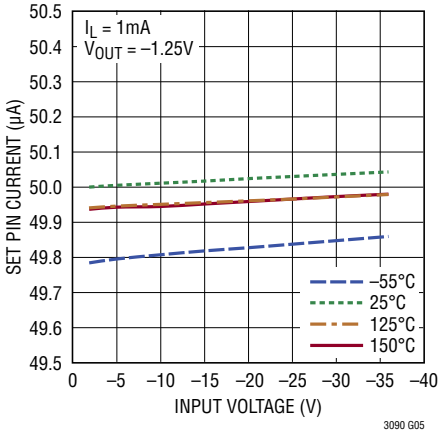
Offset Voltage (V_{OUT} – V_{SET})



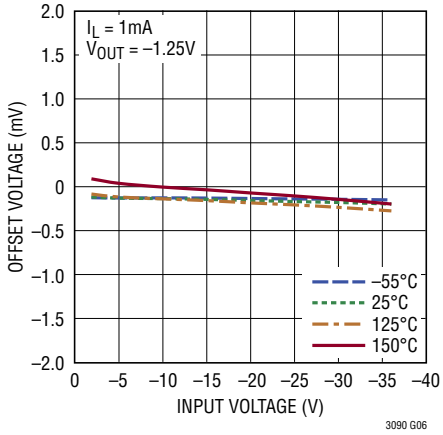
Offset Voltage



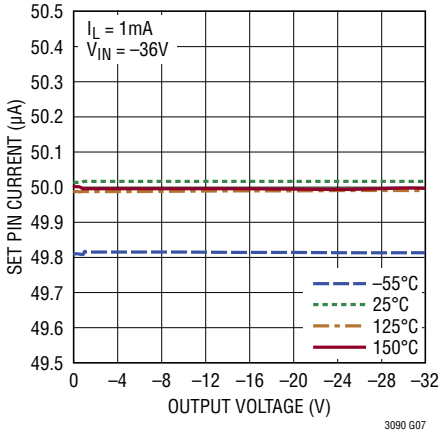
Set Pin Current



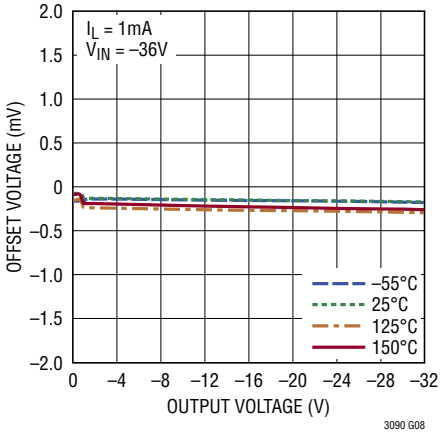
Offset Voltage (V_{OUT} – V_{SET})



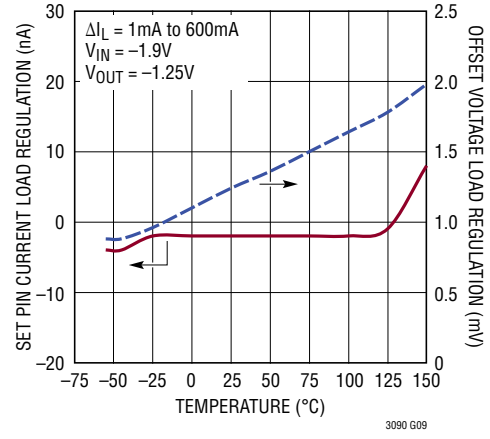
Set Pin Current



Offset Voltage (V_{OUT} – V_{SET})

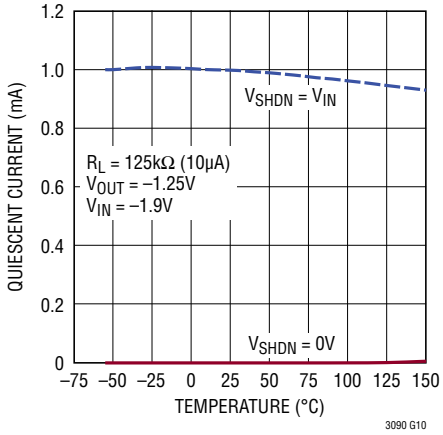


Load Regulation

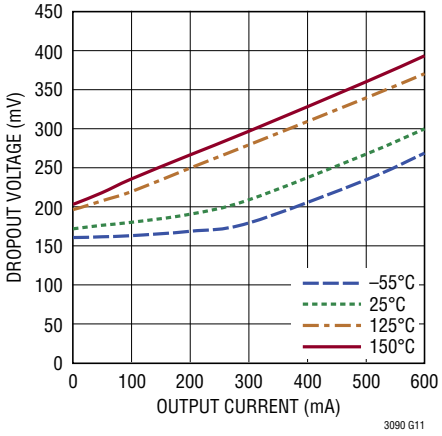


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

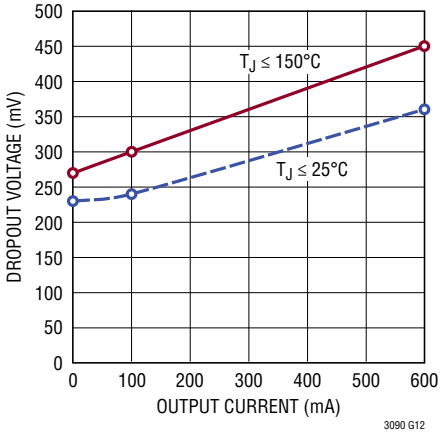
Quiescent Current



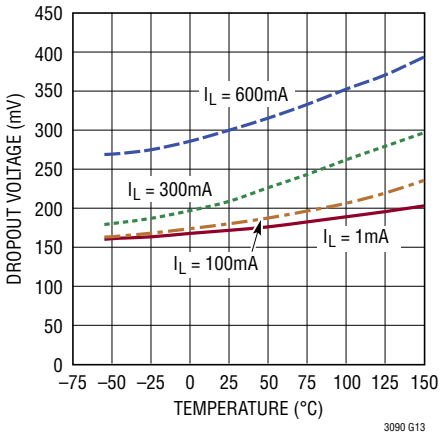
Typical Dropout Voltage



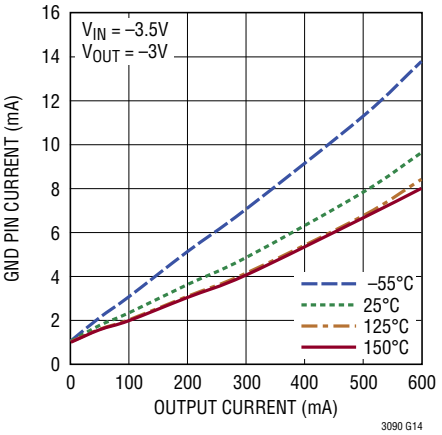
Guaranteed Dropout Voltage



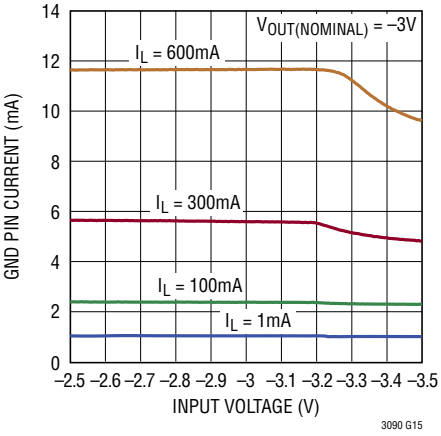
Dropout Voltage



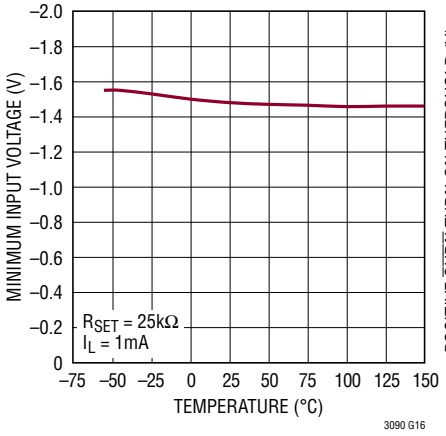
GND Pin Current



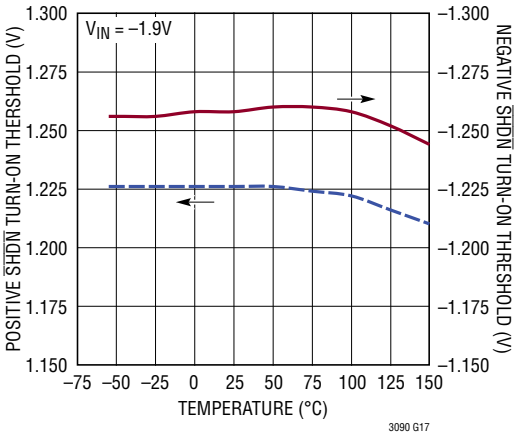
GND Pin Current Entering Dropout



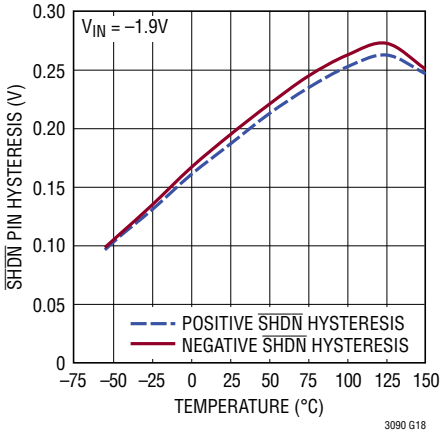
Minimum Input Voltage



$\overline{SHDN}$ Turn-On Threshold



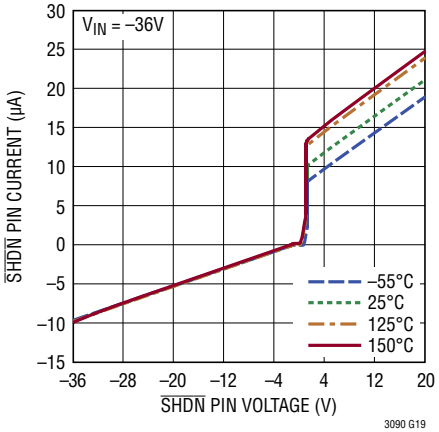
$\overline{SHDN}$ Pin Hysteresis



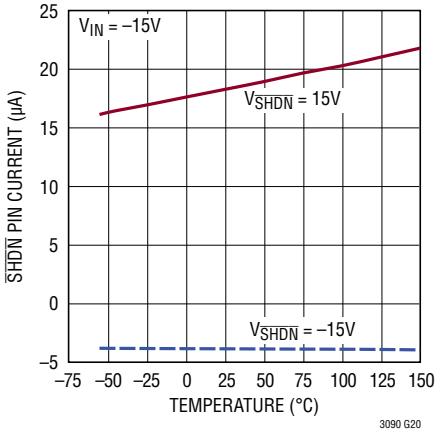
TYPICAL PERFORMANCE CHARACTERISTICS

T_J = 25°C, unless otherwise noted.

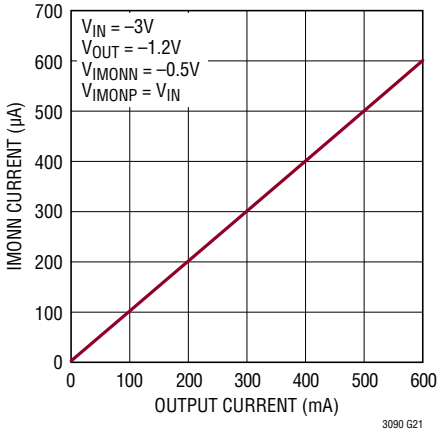
$\overline{SHDN}$ Pin Current



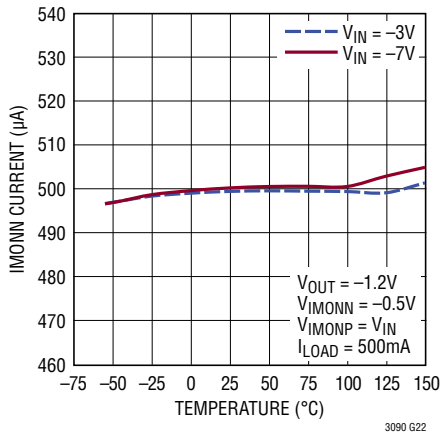
$\overline{SHDN}$ Pin Current



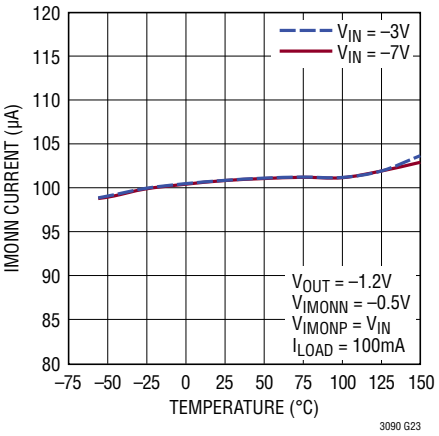
IMONN Pin Current



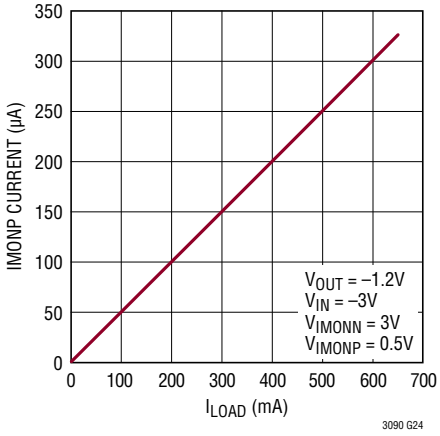
IMONN Pin Current at 500mA



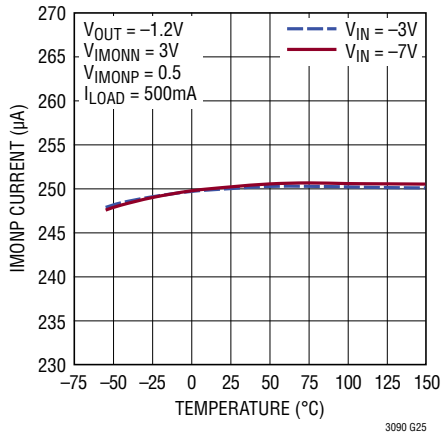
IMONN Pin Current at 100mA



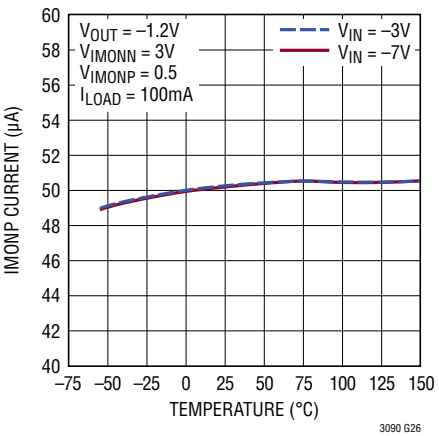
IMONP Pin Current



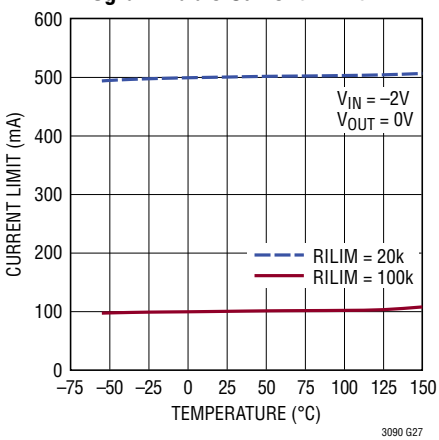
IMONP Pin Current at 500mA



IMONP Pin Current at 100mA

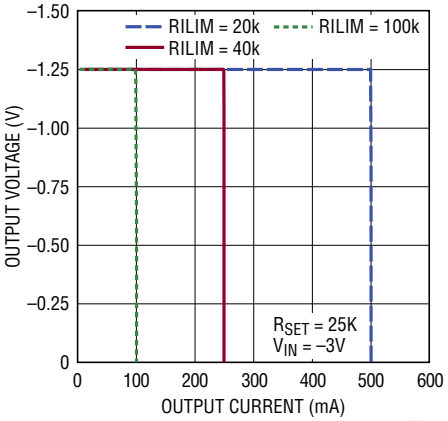


Programmable Current Limit

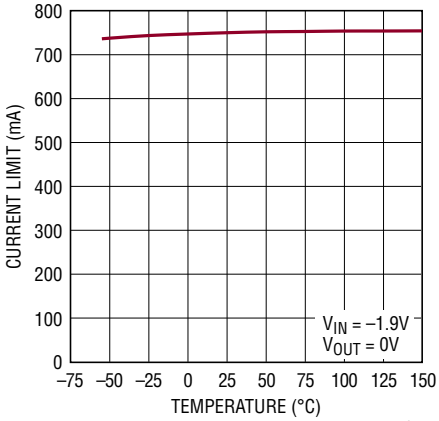


TYPICAL PERFORMANCE CHARACTERISTICS T_J = 25°C, unless otherwise noted.

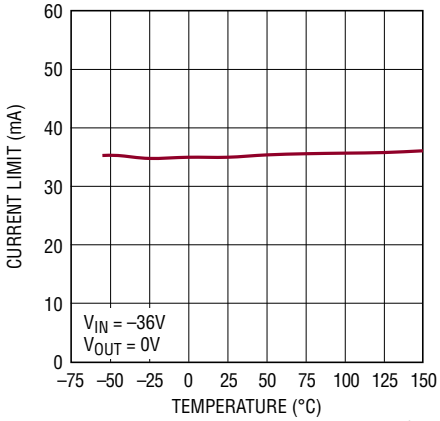
Programmable Brick-Wall Current Limit



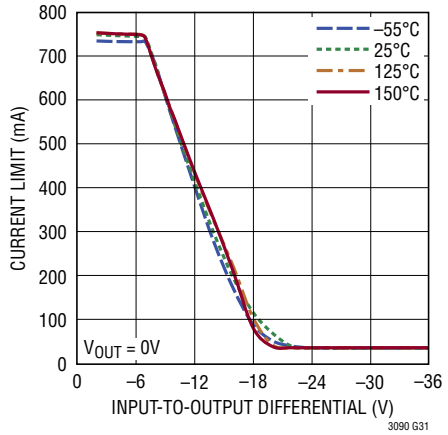
Internal Current Limit



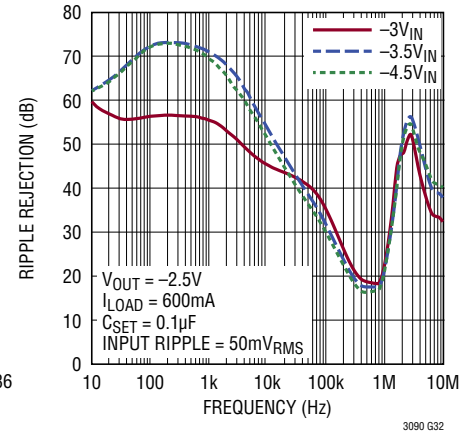
Internal Current Limit



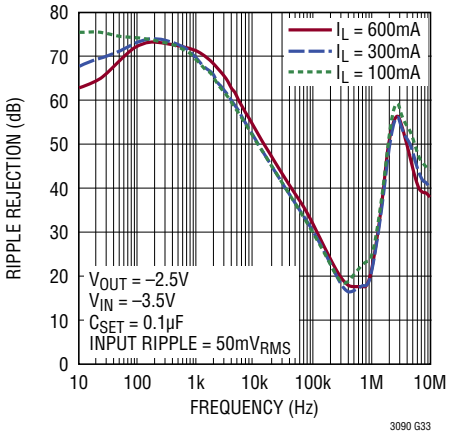
Internal Current Limit



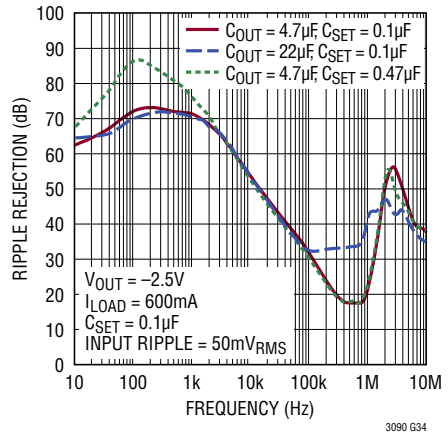
Input Ripple Rejection



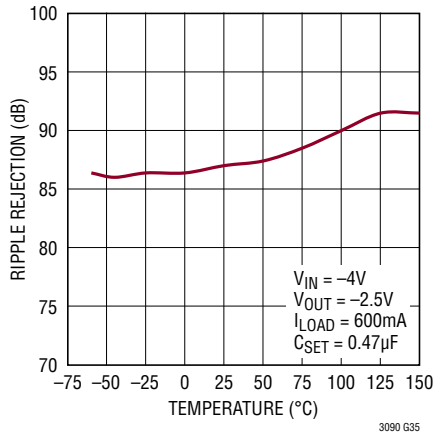
Input Ripple Rejection



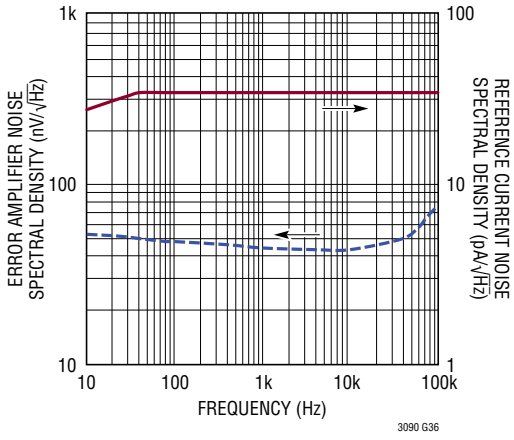
Input Ripple Rejection



Ripple Rejection (120Hz)



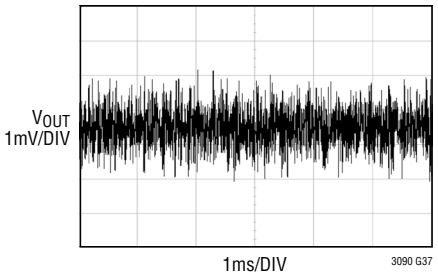
Noise Spectral Density



TYPICAL PERFORMANCE CHARACTERISTICS

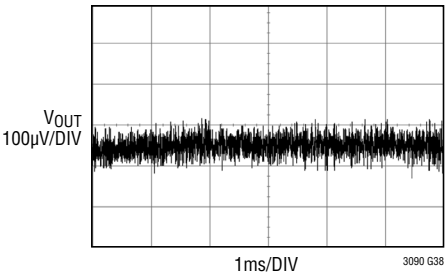
T_J = 25°C, unless otherwise noted.

Output Noise: 10Hz to 100kHz



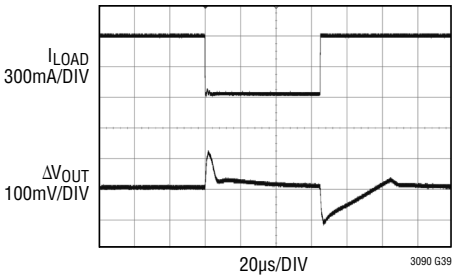
V_{IN}: –3.5V
C_{OUT}: 4.7µF, **C_{SET}: 20pF**
V_{OUT}: –2V
I_L: 600mA

Output Noise: 10Hz to 100kHz



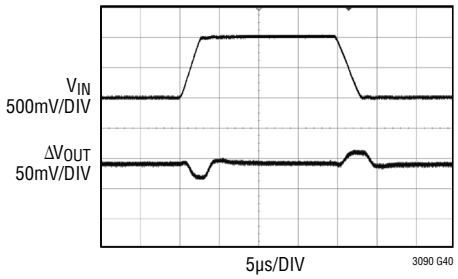
V_{IN}: –3.5V
C_{OUT}: 4.7µF, **C_{SET}: 0.1µF**
V_{OUT}: –2V
I_L: 600mA

Load Transient Response, $–3V_{OUT}$



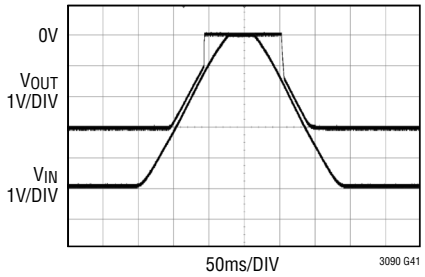
I_{LOAD}: 20mA TO 600mA
C_{OUT}: 4.7µF, C_{SET}: 0.1µF
V_{OUT}: –3V
V_{IN} = –4V, $\overline{SHDN}$ = IN

Line Transient Response



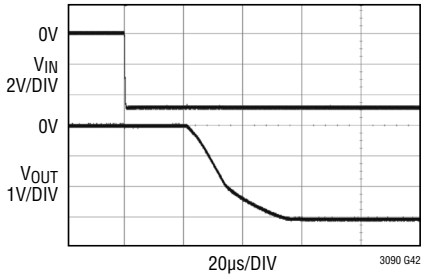
V_{IN}: –5V TO –4V
C_{OUT}: 4.7µF, C_{SET}: 0.1µF
V_{OUT}: –3V
I_L: 600mA, $\overline{SHDN}$ = IN

Slow Input Supply Ramp-Up and Ramp-Down



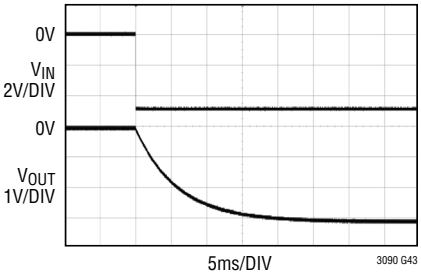
V_{IN}: –5V TO 0V
C_{OUT}: 4.7µF, C_{SET}: 0.1µF
V_{OUT}: –3V TO 0V
I_L: 600mA, $\overline{SHDN}$ = IN

Fast Input Supply Start-Up



V_{IN}: 0V TO –5V
C_{OUT}: 4.7µF, C_{SET}: 100pF
V_{OUT}: 0V TO –3V
I_L: 600mA, $\overline{SHDN}$ = IN

Fast Input Supply Start-Up



V_{IN}: 0V TO –5V
C_{OUT}: 4.7µF, C_{SET}: 0.1µF
V_{OUT}: 0V TO –3V
I_L: 600mA, $\overline{SHDN}$ = IN

PIN FUNCTIONS (DFN/MSOP)

IN (Pins 1, 2, Exposed Pad 11/1, 2, 3, Exposed Pad 13): Input. These pins supply power to the regulator. The exposed backside pad of the DFN and MSOP packages is an electrical connection to IN and the device's substrate. For proper electrical and thermal performance, tie all IN pins together and tie IN to the exposed backside of the package on the PCB. See the Applications Information section for thermal considerations and calculating junction temperature. The LT3090 requires a bypass capacitor at IN. In general, a battery's output impedance rises with frequency, so include a bypass capacitor in battery powered applications. An input bypass capacitor in the range of 2.2µF to 4.7µF generally suffices, but applications with large load transients or longer input lines may require higher input capacitance to prevent input supply droop or input ringing.

ILIM (Pin 3/4): Current Limit Programming Pin. Connecting an external resistor between the ILIM and IN pins programs the current limit set point. For best accuracy, Kelvin connect this resistor to the IN pins. The programming scale factor is nominally 10A • kΩ. Current limit is accurate to ±8% over temperature. If unused, tie ILIM to IN and the internal current limit protects the part. A parasitic substrate diode exists between the LT3090's ILIM and IN pins. Therefore, do not drive ILIM more than 0.3V below IN during normal operation or during a fault condition.

IMONP (Pin 4/5): Positive Current Monitoring Pin. For positive current monitoring, connect a resistor between IMONP and GND. IMONP sources current equal to 1/2000 of output current. For negative current monitoring, tie this pin to IN. For proper operation, IN and IMONP must be at least 2V below IMONN. If unused, tie IMONP to IN. A parasitic substrate diode exists between the LT3090's IMONP and IN pins. Therefore, do not drive IMONP more than 0.3V below IN during normal operation or during a fault condition.

IMONN (Pin 5/6): Negative Current Monitoring Pin. For negative current monitoring, connect a resistor between IMONN and GND. IMONN sinks current equal to 1/1000 of output current. For positive current monitoring, bias IMONN to a positive supply voltage (at least 2V above IMONP). If unused, tie IMONN to the GND pin. A parasitic substrate diode exists between the LT3090's IMONN and IN pins. Therefore, do not drive IMONN more than 0.3V below IN during normal operation or during a fault condition.

$\overline{\text{SHDN}}$ (Pin 6/7): Shutdown. Use the $\overline{\text{SHDN}}$ pin to put the LT3090 into a micropower shutdown state and to turn off the output voltage. The $\overline{\text{SHDN}}$ function is bidirectional, allowing either positive or negative logic to turn the regulator ON/OFF. The $\overline{\text{SHDN}}$ pin threshold voltages are referenced to GND. The output of the LT3090 is OFF if the $\overline{\text{SHDN}}$ pin is pulled within ±0.45V of GND. Driving the $\overline{\text{SHDN}}$ pin more than ±1.4V turns the LT3090 ON. Drive the $\overline{\text{SHDN}}$ pin with either a logic gate or with open collector/drain logic using a pull-up resistor. The resistor supplies the pull-up current of the open collector/drain gate. The maximum $\overline{\text{SHDN}}$ pin current is 7µA out of the pin (for negative logic) or 30µA into the pin (for positive logic). If the $\overline{\text{SHDN}}$ function is unused, connect the $\overline{\text{SHDN}}$ pin to V_{IN} or a positive bias voltage to turn the device ON. Do not float the $\overline{\text{SHDN}}$ pin. As detailed in the Applications Information section, the $\overline{\text{SHDN}}$ pin can also be used to set a programmable undervoltage lockout (UVLO) threshold. A parasitic diode exists between the LT3090's $\overline{\text{SHDN}}$ and IN pins. Therefore, do not drive $\overline{\text{SHDN}}$ more than 0.3V below IN during normal operation or during a fault condition.

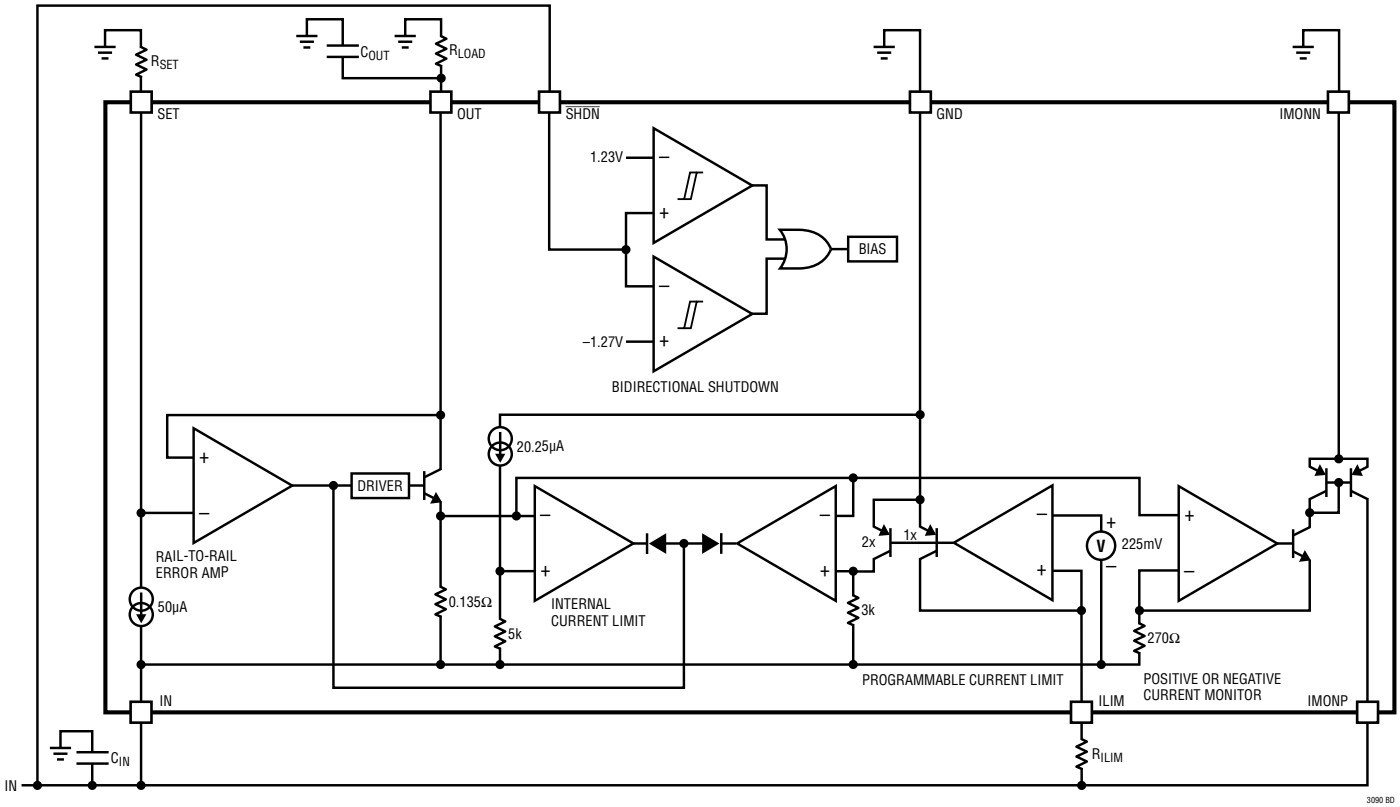
SET (Pin 7/8): SET. This pin is the inverting input to the error amplifier and the regulation setpoint for the device. A precision fixed current of 50µA flows into this pin. Connecting a resistor from SET to GND programs the LT3090's output voltage. Output voltage range is from zero to the –36V absolute maximum rating. Adding a bypass capacitor from SET to GND improves transient response, PSRR, noise performance and soft starts the output. Kelvin connect the GND side of the SET pin resistor to the load for optimum load regulation performance. A parasitic substrate diode exists between the LT3090's SET and IN pins. Therefore, do not drive SET more than 0.3V below IN during normal operation or during a fault condition.

PIN FUNCTIONS (DFN/MSOP)

GND (Pin 8/9): Ground. This pin supplies the LT3090's quiescent current and the drive current to the NPN pass transistor. The LT3090's GND pin is highly versatile. Depending on application's requirements, it can be tied to the system ground, a positive voltage, or the OUT pin. A parasitic substrate diode exists between the LT3090's GND and IN pins. Therefore, do not drive GND more than 0.3V below IN during normal operation or during a fault condition.

OUT (Pins 9, 10/10, 11, 12): Output. These pins supply power to the load. Tie all OUT pins together for best performance. Use a minimum output capacitor of 4.7µF with an ESR less than 0.5Ω to prevent oscillations. As mentioned in the Electrical Characteristics table, a minimum load current of 10µA is required to prevent instability. Large load transient applications require larger output capacitors to limit peak voltage transients. See the Applications Information section for more information on output capacitance. A parasitic substrate diode exists between OUT and IN pins of the LT3090. Therefore, do not drive OUT more than 0.3V below IN during normal operation or during a fault condition.

BLOCK DIAGRAM



APPLICATIONS INFORMATION

The LT3090 is a 600mA, rail-to-rail output, negative low dropout linear regulator featuring very low output noise, high bandwidth, precision programmable current limit, precision positive or negative current monitor, and bi-directional shutdown. The LT3090 supplies 600mA at a typical dropout voltage of 300mV. Unlike other devices, the LT3090 does not require a separate supply to achieve low dropout performance. The 1mA quiescent current drops to well below 1µA in shutdown.

The LT3090 is easy to use and incorporates all of the protection features expected in high performance regulators. Included are short circuit protection, safe operating area protection, as well as thermal shutdown with hysteresis. In bipolar supply applications where the regulator's load is returned to a positive supply, OUT can be pulled above GND up to 36V and still allow the LT3090 to safely startup.

Output Voltage

The LT3090 incorporates a zero TC 50µA reference current source that flows into the SET pin. The SET pin is the inverting input of the error amp. Connecting a resistor from SET to ground generates a voltage that becomes the reference point for the error amplifier (see Figure 1). The reference voltage is a straight multiplication of the SET pin current and the resistor value (Ohm's Law, V = I • R). The rail-to-rail error amp's unity gain configuration produces a low impedance voltage on its noninverting input, i.e. the OUT pin. Output voltage is programmable from 0V (using zero Ω resistor) to V_{IN} plus dropout. Table 1 lists many common output voltages and its corresponding 1% RSET resistance.

Table 1. 1% Resistor for Common Output Voltages

V_{OUT} (V)	R_{SET} (kΩ)
–2.5	49.9
–3	60.4
–3.3	66.5
–5	100
–12	243
–15	301

The benefits of using a current reference, as opposed to a voltage reference as in conventional regulators such as the LT1185, LT1175, LT1964 and LT3015, is that the device always operates in unity gain configuration – regardless of the programmed output voltage. This allows the LT3090 to have loop gain, frequency response, and bandwidth independent of the output voltage. Moreover, none of the error amp gain is needed to amplify the set pin voltage to a higher output voltage (in magnitude). As a result, output load regulation is specified in terms of millivolts and not a fixed percentage of the output voltage.

Since the zero TC current source is very accurate, the SET pin resistor is the limiting factor in achieving high accuracy; hence, it must be a precision resistor. Moreover, any leakage paths to and from the SET pin create errors in the output voltage. If necessary, use high quality insulation (e.g. Teflon, Kel-F); moreover, cleaning of all insulating surfaces to remove fluxes and other residues may be required. High humidity environments may require a surface coating at the SET pin to provide a moisture barrier.

Minimize board leakage by encircling the SET pin with a guard ring operated at a potential close to itself – ideally the guard ring should be tied to the OUT pin. Guarding both sides of the circuit board is required. Bulk leakage

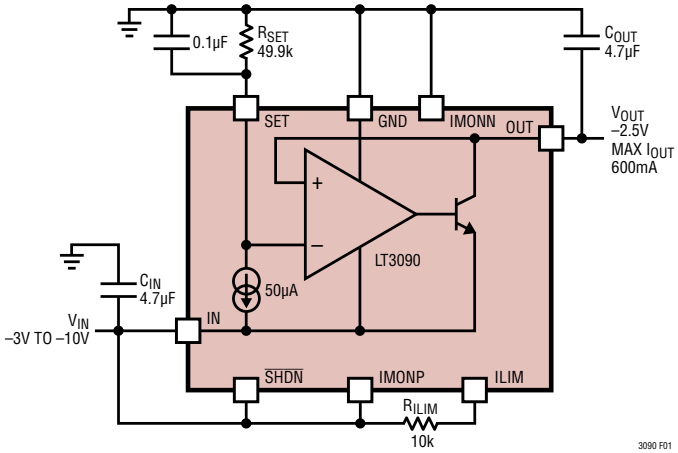


Figure 1. Basic Adjustable Regulator

APPLICATIONS INFORMATION

reduction depends on the guard ring width. Leakages as small as 50nA into or out of the SET pin creates a 0.1% error in the reference voltage. Leakages of this magnitude, coupled with other sources of leakage, can cause significant errors in the output voltage, especially over wide operating temperature range. Figure 2 illustrates a typical guard ring layout technique.

If guard ring techniques are used, then SET pin stray capacitance is practically eliminated. Since the SET pin is a high impedance node, unwanted signals may couple into the SET pin and cause erratic behavior. This is most noticeable when operating with a minimum output capacitor at light load currents. The simplest remedy is to bypass the SET pin with a small capacitance to ground – 100pF is generally sufficient.

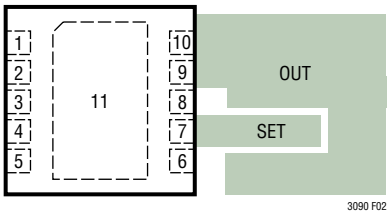


Figure 2. Guard Ring Layout for DFN

Stability and Input Capacitance

The LT3090 is stable with a minimum of 4.7µF capacitor placed at the IN pin. Low ESR ceramic capacitors can be used. However, in cases where long wires connect the power supply to the LT3090's input and ground, the use of low value input capacitors combined with a large output load current may result in instability. The resonant LC tank circuit formed by the wire inductance and the input capacitor is the cause and not because of LT3090 instability.

The self inductance, or isolated inductance, of a wire is directly proportional to its length. However, the wire diameter has less influence on its self inductance. For example, the self inductance of a 2-AWG isolated wire with a diameter of 0.26" is about half the inductance of a 30-AWG wire with a diameter of 0.01". One foot of 30-AWG wire has 465nH of self inductance.

Several methods exist to reduce a wire's self inductance. One method divides the current flowing towards the LT3090 between two parallel conductors. In this case, placing the wires further apart reduces the inductance; up to a 50% reduction when placed only a few inches apart. Splitting the wires connects two equal inductors in parallel. However, when placed in close proximity to each other, mutual inductance adds to the overall self inductance of the wires. The second and most effective technique to reduce overall inductance is to place the forward and return current conductors (the input wire and the ground wire) in close proximity. Two 30-AWG wires separated by 0.02" reduce the overall self inductance to about one-fifth of a single wire.

If a battery, mounted in close proximity, powers the LT3090, a 4.7µF input capacitor suffices for stability. However, if a distantly located supply powers the LT3090, use a larger value input capacitor. Use a rough guideline of 1µF (in addition to the 4.7µF minimum) per 8" of wire length. The minimum input capacitance needed to stabilize the application also varies with power supply output impedance variations. Placing additional capacitance on the LT3090's output also helps. However, this requires an order of magnitude more capacitance in comparison with additional LT3090 input bypassing. Series resistance between the supply and the LT3090 input also helps stabilize the application; as little as 0.1Ω to 0.5Ω suffices. This impedance dampens the LC tank circuit at the expense of dropout voltage. A better alternative is to use higher ESR tantalum or electrolytic capacitors at the LT3090 input in place of ceramic capacitors.

Stability and Output Capacitance

The LT3090 requires an output capacitor for stability. It is stable with low ESR capacitors (such as ceramic, tantalum or low ESR electrolytic). A minimum output capacitor of 4.7µF with an ESR of 0.5Ω or less is recommended to prevent oscillations. Larger values of output capacitance

APPLICATIONS INFORMATION

decrease peak output deviations during a load transient. The LT3090 requires a minimum 10µA load current to maintain stability under all operating conditions.

Give extra consideration to the use of ceramic capacitors. Ceramic capacitors are manufactured with a variety of dielectrics, each with different behavior across temperature and applied voltage. The most common dielectrics used are specified with EIA temperature characteristic codes of Z5U, Y5V, X5R and X7R. The Z5U and Y5V dielectrics are good for providing high capacitance in small packages, but they have strong voltage and temperature coefficients as shown in Figures 3 and 4. When used with a 5V regulator, a 16V 10µF Y5V capacitor can exhibit an effective value as low as 1µF to 2µF for the DC bias voltage applied over the operating temperature range.

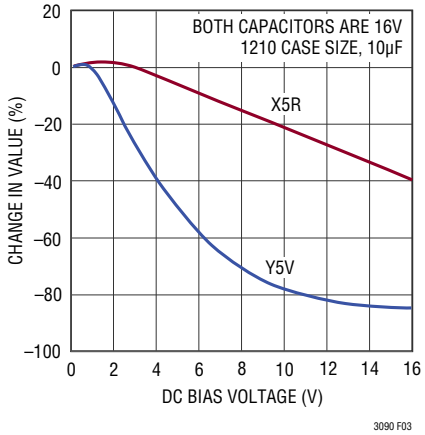


Figure 3. Ceramic Capacitor DC Bias Characteristics

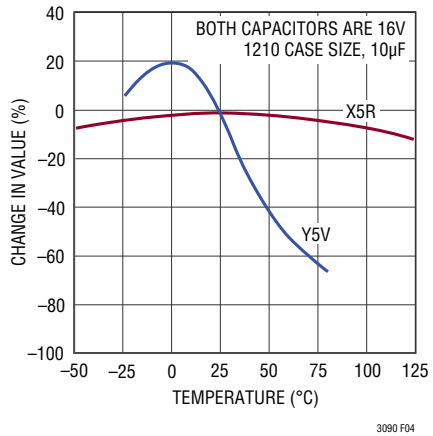


Figure 4. Ceramic Capacitor Temperature Characteristics

The X5R and X7R dielectrics result in more stable characteristics, and are thus more suitable for use as the regulator's output capacitor. The X7R dielectric has better stability across temperature, while X5R is less expensive and is available in higher values. Nonetheless, care must still be exercised when using X5R and X7R capacitors. The X5R and X7R codes only specify operating temperature range and the maximum capacitance change over temperature. While capacitance change due to DC bias for X5R and X7R is better than Y5V and Z5U dielectrics, it can still be significant enough to drop capacitance below sufficient levels. Capacitor DC bias characteristics tend to improve as component case size increases, but verification of expected capacitance at the operating voltage is highly recommended.

Voltage and temperature coefficients are not the only sources of problems. Some ceramic capacitors have a piezoelectric response. A piezoelectric device generates a voltage across its terminals due to mechanical stress upon it, similar to how a piezoelectric microphone works. For a ceramic capacitor the stress can be induced by mechanical vibrations within the system or due to thermal transients.

Output Noise Analysis

The LT3090 offers many advantages with respect to noise performance. Traditional linear regulators have several sources of noise. The most critical noise sources for an LDO are its voltage reference, the error amplifier, the noise of the resistors in the divider network setting output voltage and the noise gain created by this resistor divider.

Many low noise regulators pin out the voltage reference to allow for bypassing and noise reduction of the reference. Unlike other linear regulators, the LT3090 does not use a traditional voltage reference, but instead it uses a 50µA current source reference. That current operates with typical noise current levels of 31.6pA/$\sqrt{Hz}$ (10nA$_{RMS}$ over a 10Hz to 100kHz bandwidth). The voltage noise equals the noise current multiplied by the resistor value. The resistor itself generates spot noise equal to $\sqrt{4KTR}$ (whereby K = Boltzmann's constant, $1.38 \bullet 10^{-23}$ J/K and T is the absolute temperature) which is RMS summed with the reference current noise.

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One problem that conventional linear regulators face is that the resistor divider setting V_{OUT} gains up the reference noise. In contrast, the LT3090's unity gain follower architecture presents no gain from the SET pin to the output. Therefore, output noise is virtually independent of the output voltage setting if a capacitor bypasses the SET pin. Resultant output noise is then set by the error amplifier's noise, typically 57nV/$\sqrt{Hz}$ (18μV_{RMS} in a 10Hz to 100kHz bandwidth).

Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for both the reference current and the error amplifier over a 10Hz to 100kHz bandwidth.

Set Pin (Bypass) Capacitance: Output Noise, PSRR, Transient Response and Soft-Start

Bypassing the SET pin's voltage setting resistor with a capacitor lowers output noise. The Typical Performance Characteristics section illustrates that connecting a 0.1µF from SET to GND yields output noise as low as 18μV_{RMS}. Paralleling multiple LT3090s further reduces noise by $\sqrt{N}$, for N parallel regulators. Curves in the Typical Performance Characteristics section show noise spectral density and peak-to-peak noise characteristics for the error amplifier for different values of bypass capacitance.

Use of a SET pin bypass capacitor also improves PSRR and transient response performance. It is important to note that any bypass capacitor leakage deteriorates the LT3090's DC regulation. Capacitor leakage of even 50nA is a 0.1% DC error. Therefore, LTC recommends the use of a good quality low leakage capacitor.

The final benefit of using a SET pin bypass capacitor is that it soft starts the output and limits inrush current. The R-C time constant, formed by the SET pin resistor and capacitor, controls soft-start time. Ramp-up rate from 0 to 90% of nominal V_{OUT} is:

$$t_{SS} \approx 2.3 \bullet R_{SET} \bullet C_{SET}$$

For applications requiring higher accuracy or an adjustable output voltage, the SET pin may be actively driven by an external voltage source capable of sourcing 50µA – the application limitations are the creativity and ingenuity of the circuit designer. For instance, connecting a precision voltage reference to the SET pin removes any errors in output voltage due to the reference current and resistor tolerances.

Shutdown/UVLO

The $\overline{SHDN}$ pin is used to put the LT3090 into a micropower shutdown state. The LT3090 has an accurate –1.27V turn-ON threshold on the $\overline{SHDN}$ pin. This threshold can be used in conjunction with a resistor divider from the input supply to define an accurate undervoltage lockout (UVLO) threshold for the regulator. The $\overline{SHDN}$ pin current (at the threshold) needs to be considered when determining the resistor divider network. See the Typical Performance curves for $\overline{SHDN}$ pin current vs $\overline{SHDN}$ pin voltage.

Moreover, since the $\overline{SHDN}$ pin is bidirectional, it can be taken beyond ±1.4V to turn-ON the LT3090. In bipolar supply applications, the positive $\overline{SHDN}$ threshold can be used to sequence the turn-ON of LT3090 after the positive regulator has turned on.

Current Monitoring (IMONN and IMONP)

The LT3090 incorporates precision positive or negative current monitor. As illustrated in the Block Diagram, the negative current monitor pin (IMONN) sinks current proportional (1:1000) to the output current while the positive current monitor pin (IMONP) sources current proportional (1:2000) to the output current. For proper operation, ensure IMONN is at least 2V above IN and IMONP.

As highlighted in Figure 5, for a negative current monitor application, tie IMONP to IN and tie IMONN through a

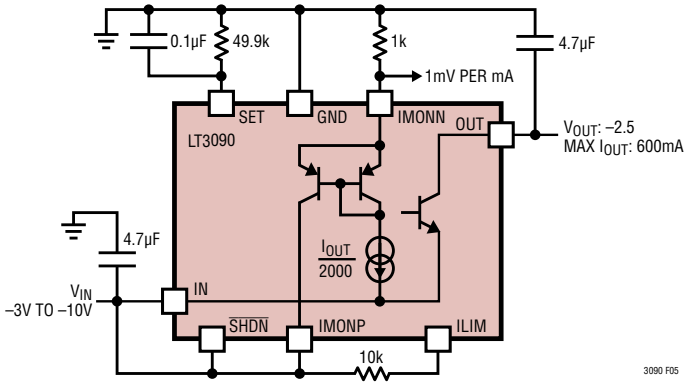

Figure 5: Negative Output Current Monitor

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resistor to GND – this generates a negative voltage (proportional to output current) on IMONN. Furthermore, as illustrated in Figure 6, the negative current monitor pin can also be used for cable drop compensation. Cable drop compensation corrects for load dependent voltage drop caused by a resistive connection between the LT3090's OUT pin and its load.

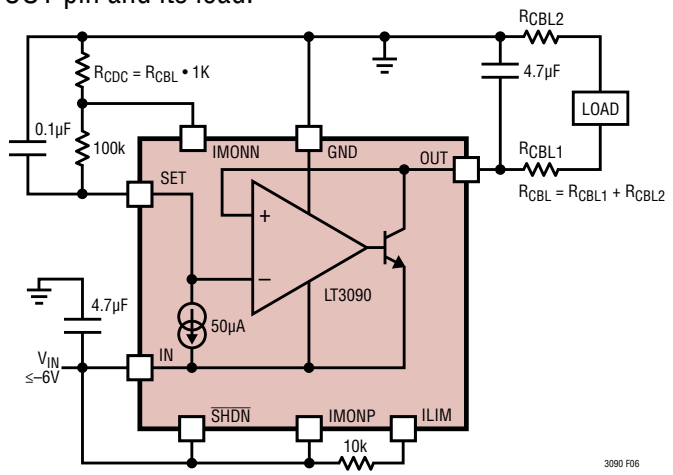

Figure 6. Simple Cable Drop Compensation

For a positive current monitor application, as illustrated in Figure 7, tie IMONP through a resistor to GND—this generates a positive voltage (proportional to output current) on IMONP. And tie IMONN to a supply at least 2V above the maximum operating IMONP voltage.

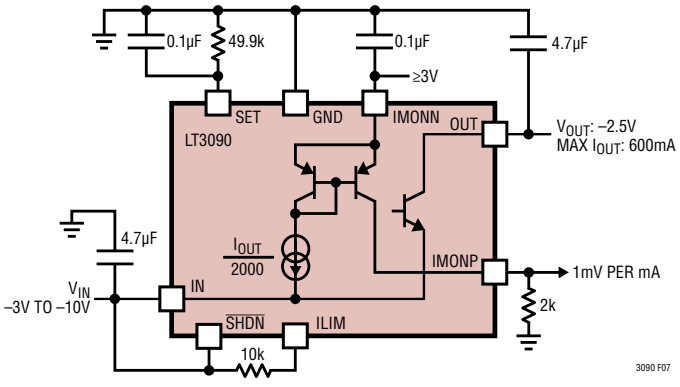

Figure 7. Positive Output Current Monitor

When unused, IMONN and IMONP pins can be left floating; however, this slightly reduces (~5%) the device's internal current limit. Hence, if the current monitor functionality is not used, as shown in Figure 1, it is recommended to tie IMONN to GND and IMONP to IN.

The LT3090's positive or negative current monitor circuitry is designed to remain accurate even under short circuit or dropout conditions.

Externally Programmable Current Limit

The ILIM pin internally regulates to 225mV above IN. Connecting a resistor from ILIM to IN sets the current flowing out of the ILIM pin, which in turn programs the LT3090's current limit. The programming scale factor is 10kΩ • A. For example, a 20k resistor between ILIM and IN programs current limit to 500mA. For good accuracy, Kelvin connect this resistor to the LT3090's IN pin.

In cases where the OUT-to-IN differential is greater than 7V, the LT3090's foldback circuitry decreases the internal current limit. Therefore, internal current limit may override the externally programmed current limit level to keep the LT3090 within its Safe-Operating-Area (SOA). See the Internal Current Limit vs Input-to-Output differential graph in the Typical Performance Characteristics section.

ILIM can be tied to IN if external programmable current limit is not needed. However, because the ILIM pin is internally regulated to 225mV above IN, if ILIM pin is shorted to IN, then this loop will current limit, thereby causing the LT3090's quiescent current to increase by about 300µA. Hence, when unused, it is recommended to tie ILIM to IN through a 10k resistor.

Load Regulation

The LT3090 does not have a separate Kelvin connection for sensing output voltage. Therefore, it is not possible to provide true remote load sensing. The connectivity resistance between the regulator and the load limits load regulation. The data sheet specification for load regulation is Kelvin sensed at the OUT pin of the package. GND side Kelvin sensing is a true Kelvin connection, with the top of the voltage setting resistor returned to the positive side of the load (see Figure 8). Connected as shown, system load regulation is the sum of the LT3090 load regulation and the parasitic line resistance multiplied by the output current. It is therefore important to keep the negative connection between the regulator and the load as short as possible and to use wide wires or PC board traces.

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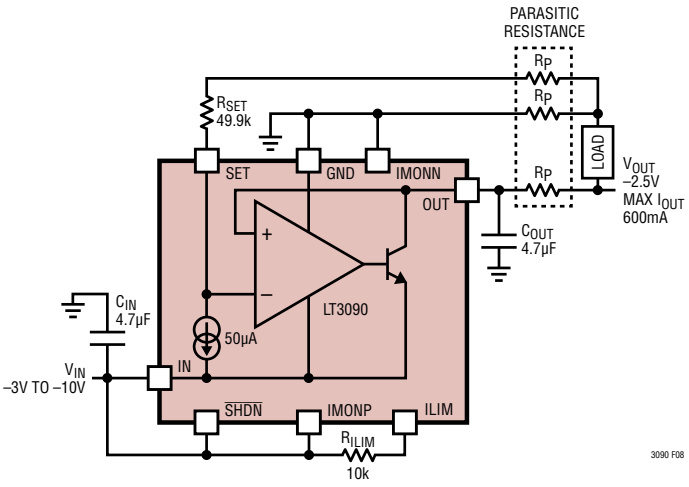


Figure 8. Connections for Best Load Regulation

Floating 3-Terminal Regulator

The LT3090's rail-to-rail error amp allows the LDO to be configured as a floating three-terminal regulator. With proper protection, the LT3090 can be used in arbitrarily high voltage applications. Figure 9 illustrates this configuration. In this mode, the GND pin current is supplied by the load; hence, a minimum 1mA load current is required to maintain regulation. If true zero output voltage operation is required, return the 1mA load current to a positive supply. Note that in three terminal operation, the minimum input voltage is now the device's dropout voltage. Furthermore, the ILIM pin is internally regulated to 225mV above IN. This servo loop will current limit if ILIM is shorted to IN, thereby causing LT3090's quiescent current to increase by about 300µA. Hence, when unused, it is recommended to tie ILIM to IN through a 10k resistor.

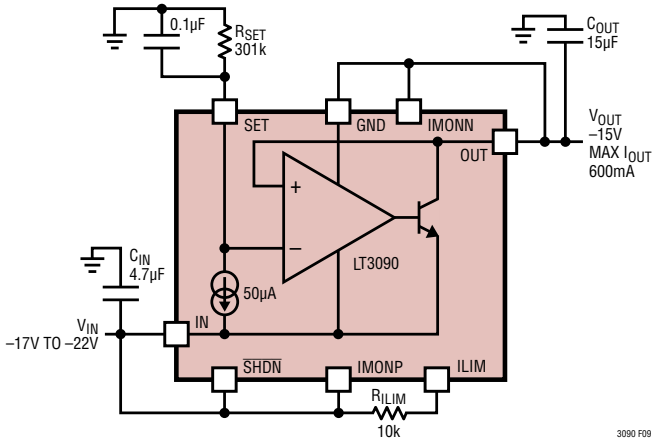
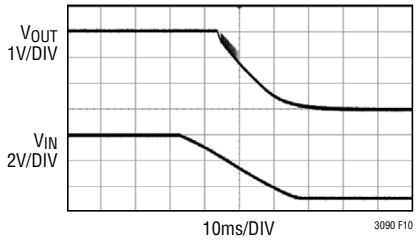


Figure 9. Floating 3-Terminal Adjustable Regulator

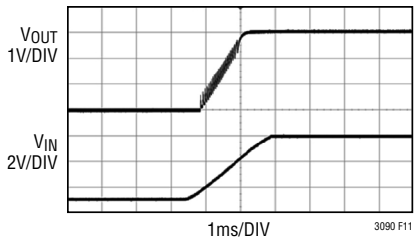
It is important to note that in a floating configuration and with slow V_{IN} ramp-up and ramp-down (as shown in Figures 10 and 11), the LT3090 may exhibit oscillations during start-up if $\overline{SHDN}$ is tied to V_{IN}. This occurs because the $\overline{SHDN}$ comparator's turn-ON and turn-OFF thresholds are referenced to the GND pin of LT3090. Since in floating configuration the GND pin of LT3090 is tied to the OUT pin, which is slowly increasing as V_{IN} is ramping up, the reference point for the $\overline{SHDN}$ comparator is changing; hence, it causes start-up oscillations. This oscillation can be minimized by placing at least 0.1µF and 15µF capacitor at the SET and OUT pins, respectively—although it won't be eliminated, as per Figures 10 and 11 below. For fast V_{IN} ramp-up and ramp-down the LT3090 does not oscillate.

If however, the $\overline{SHDN}$ pin is tied to a positive supply, 1.3V and above (as shown in Figure 12), then there are no start-up oscillations and a 4.7µF minimum output capacitor can be used—but having some SET pin capacitance is still recommended. In addition to tying the GND pin to the OUT pin (for floating configuration), the GND pin of LT3090 can also be tied to a positive voltage as shown in the next section.



V_{IN}: 0V TO –5V
C_{OUT}: 15µF, C_{SET}: 0.1µF
V_{OUT}: 0V TO –3V
I_L: 600mA, $\overline{SHDN}$ = IN

Figure 10. Floating Mode: Input Supply Ramp-Up



V_{IN}: –5V TO 0V
C_{OUT}: 15µF, C_{SET}: 0.1µF
V_{OUT}: –3V TO 0V
I_L: 600mA, $\overline{SHDN}$ = IN

Figure 11. Floating Mode: Input Supply Ramp-Down

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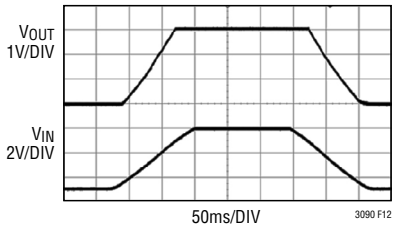

Figure 12. Floating Mode: Input Supply Ramp-Up and Down Using Positive SHDN

GND Pin Versatility of LT3090

For applications requiring very low output voltages such as below –1V, the minimum input voltage of –1.9V limits how low V_{IN} can drop before the device stops regulating. As shown in Figure 13, this results in a much higher dropout voltage set by the minimum V_{IN} specification rather than the actual dropout of the NPN pass device.

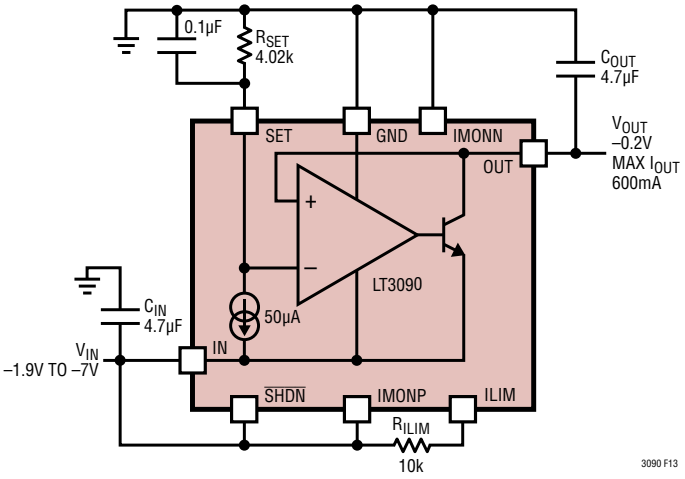

Figure 13. Generating Very Low Output Voltages

A solution to this problem is available from the LT3090 architecture and the flexibility in how its GND pin can be connected. The GND pin does not need to be connected to system ground! It can be connected to a positive voltage as well. If the GND pin of LT3090 is tied to a positive voltage that is at least 1.9V above V_{IN}, then V_{IN} can be set below the LT3090's –1.9V minimum input voltage. As long as there is 1.9V between IN and GND pins of LT3090, the minimum operating voltage is satisfied. Now it can operate with much lower dropout voltage, with the device dropout set by the pass device as illustrated in Figure 14.

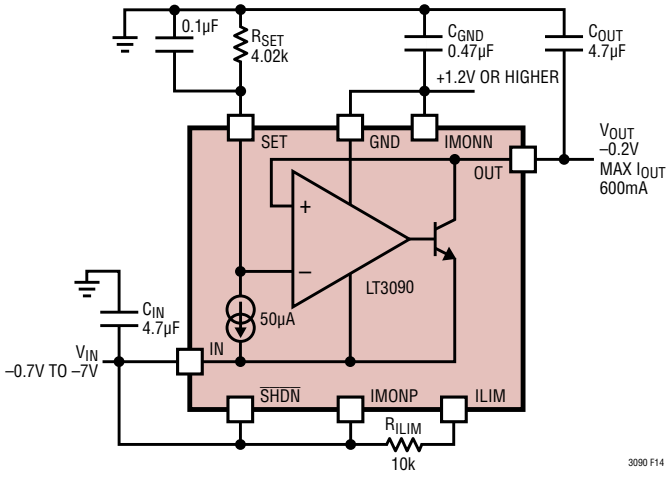

Figure 14. Low Dropout Operation for Very Low Output Voltages

Note that if the LT3090's $\overline{SHDN}$ capability is not desired, then tie the $\overline{SHDN}$ pin to V_{IN}. However, if it is desired to turn the device ON and OFF, then the $\overline{SHDN}$ logic signal needs to be referenced to the LT3090's GND pin. A simple way to achieve this is shown Figure 15, but the GND pin needs to be at least +1.4V.

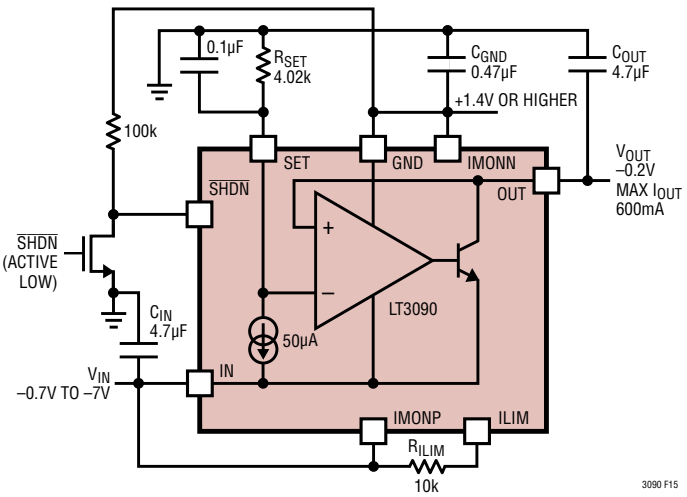

Figure 15. GND Pin Referenced $\overline{SHDN}$ Signal

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In summary, the GND pin of LT3090 is highly versatile and can be tied to different places depending on the application's requirements: a) It can be tied to the system GND for low dropout operation for output voltages greater than –1.6V, b) it can be tied to a positive voltage for low dropout operation for very low output voltages, and c) as illustrated in the Floating 3-Terminal Regulator section, the GND pin can be tied to the OUT pin for very high common mode voltage applications.

Direct Paralleling

Higher output current is obtained by paralleling multiple LT3090s. Tie all SET pins together and all IN pins together. Connect the OUT pins together using small pieces of PC trace (used as a ballast resistor) to equalize the currents in each LT3090. PC trace resistance in mΩ/inch is shown in Table 2. Ballasting requires only a tiny area.

Table 2. PC Board Trace Resistance

WEIGHT (oz)	10mil WIDTH*	20mil WIDTH*
1	54.3	27.1
2	27.1	13.6

*Trace resistance is measured in mΩ/in

The small worst-case offset of ±2mV for each paralleled LT3090 minimizes the value of required ballast resistance. Figure 16 illustrates that two LT3090s, each using a 20mΩ PCB trace ballast resistor, provide better than 80% output current sharing at full load. The 20mΩ external resistances (10mΩ for the two devices in parallel) only adds 12mV of output regulation drop with a 1.2A maximum load. With an output voltage as low as –1.2V, this only adds 1% to the regulation accuracy. If this additional load regulation error is intolerable, circuits shown in the Typical Applications section highlight how to correct this error using the output current monitor function or the master-slave configuration.

Finally, note that more than two LT3090s can be paralleled for higher output current. Paralleling multiple LT3090s is a useful technique for distributing heat on the PCB. For applications with high input-to-output voltage differential, either input series resistors or resistors in parallel with the LT3090s further spread heat.

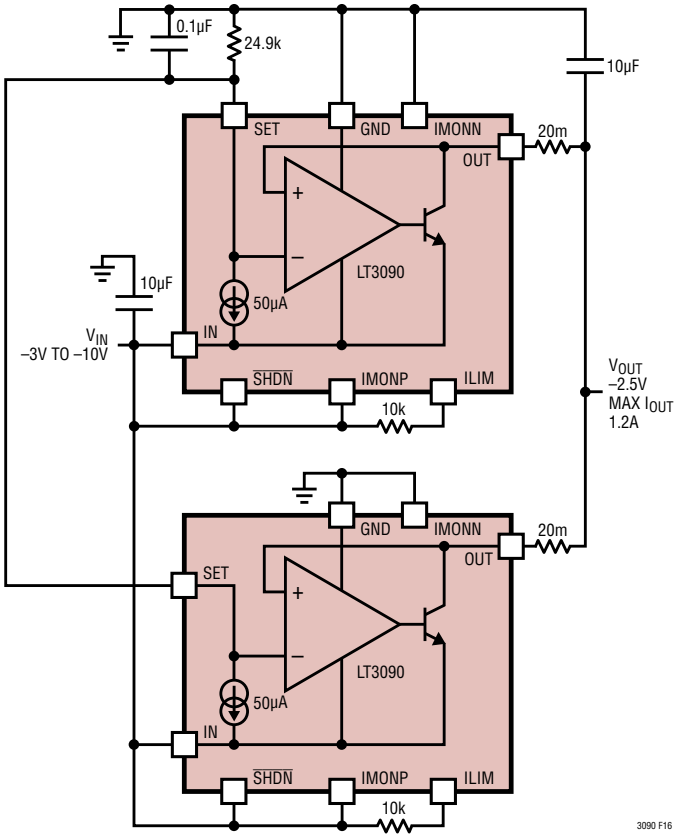

Figure 16. Parallel Devices

Thermal Considerations

The LT3090 has internal power and thermal limiting circuitry designed to protect it under overload conditions. The typical thermal shutdown temperature is 165°C with about 8°C of hysteresis. For continuous normal load conditions, do not exceed the maximum junction temperature. It is important to consider all sources of thermal resistance from junction to ambient. This includes junction-to-case, case-to-heat sink interface, heat sink resistance or circuit board-to-ambient as the application dictates. Additionally, consider all heat sources in close proximity to the LT3090.

The undersides of the DFN and MSOP packages have exposed metal from the lead frame to the die attachment. Both packages allow heat to directly transfer from the die junction to the PCB metal to limit the maximum operating

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junction temperature. The dual-in-line pin arrangement allows metal to extend beyond the ends of the package on the topside (component side) of the PCB. Connect this metal to IN on the PCB. The multiple IN and OUT pins of the LT3090 further assist in spreading heat to the PCB.

For surface mount devices, heat sinking is accomplished by using the heat spreading capabilities of the PCB and its copper traces. Copper board stiffeners and plated through-holes can also be used to spread the heat generated by power devices.

Table 3. Measured Thermal Resistance for DFN Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
Top Side*	Bottom Side		
2500mm^2	2500mm^2	2500mm^2	34°C/W
1000mm^2	2500mm^2	2500mm^2	34°C/W
225mm^2	2500mm^2	2500mm^2	35°C/W
100mm^2	2500mm^2	2500mm^2	36°C/W

*Device is mounted on topside

Table 4. Measured Thermal Resistance for MSOP Package

COPPER AREA		BOARD AREA	THERMAL RESISTANCE
Top Side*	Bottom Side		
2500mm^2	2500mm^2	2500mm^2	33°C/W
1000mm^2	2500mm^2	2500mm^2	33°C/W
225mm^2	2500mm^2	2500mm^2	34°C/W
100mm^2	2500mm^2	2500mm^2	35°C/W

*Device is mounted on topside

Tables 3 and 4 list thermal resistance as a function of copper area in a fixed board size. All measurements were taken in still air on a 4 layer FR-4 board with 1oz solid internal planes and 2oz top/bottom external trace planes with a total board thickness of 1.6mm. The four layers were electrically isolated with no thermal vias present. PCB layers, copper weight, board layout and thermal vias affect the resultant thermal resistance. For more information on thermal resistance and high thermal conductivity test boards, refer to JEDEC standard JESD51, notably JESD51-7 and JESD51-12. Achieving low thermal resistance necessitates attentions to detail and careful PCB layout.

Calculating Junction Temperature

Example: Given an output voltage of –2.5V and input voltage of –3.3V ± 5%, output current range from 1mA to 500mA, and a maximum ambient temperature of 85°C, what is the maximum junction temperature?

The LT3090's power dissipation is:

$$I_{OUT(MAX)} \bullet (V_{IN(MAX)} - V_{OUT}) + I_{GND} \bullet V_{IN(MAX)}$$

where:

$I_{OUT(MAX)} = –500mA$

$V_{IN(MAX)} = –3.465V$

I_{GND} (at $I_{OUT} = –500mA$ and $V_{IN} = –3.465V$) = –6.5mA

Thus:

$$P = (–0.5A) \bullet (–3.465V + 2.5V) + (–6.5mA) \bullet (– 3.465V) = 0.505W$$

Using a DFN package, the thermal resistance is in the range of 34°C/W to 36°C/W depending on the copper area. Therefore, the junction temperature rise above ambient approximately equals:

$$0.505W \bullet 35°C/W = 18°C$$

The maximum junction temperature equals the maximum ambient temperature plus the maximum junction temperature rise above ambient:

$$T_{JMAX} = 85°C + 18°C = 103°C$$

Overload Recovery

Like many monolithic power regulators, the LT3090 incorporates safe-operating-area (SOA) protection. The SOA protection activates at output-to-input differential voltage greater than 7V. The SOA protection decreases current limit as output-to-input differential increases and keeps the power transistor inside a safe operating region for all values of output-to-input voltage up to the LT3090's Absolute Maximum Ratings. The LT3090 provides some level of output current for all values of output-to-input differential. Refer to the Current Limit curve in the Typical Performance Characteristics section. When power is first

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applied and input voltage rises, the output follows the input and keeps the output-to-input differential low to allow the regulator to supply large output current and startup into high current loads.

Due to current limit fold back, however, at high input voltages, a problem can occur if the output voltage is low and the load current is high. Such situations occur after the removal of a short-circuit or if the shutdown pin is pulled high after the input voltage has already turn ON. The load line for such a load intersects the output current curve at two points. If this happens, the regulator has two stable output operating points. With this double intersection, the input power supply may need to be cycled down to zero and brought back up again to make the output recover. Other LTC negative linear regulators such as the LT3015, LT1964, and LT1175 also exhibit this phenomenon, so it is not unique to the LT3090.

Protection Features

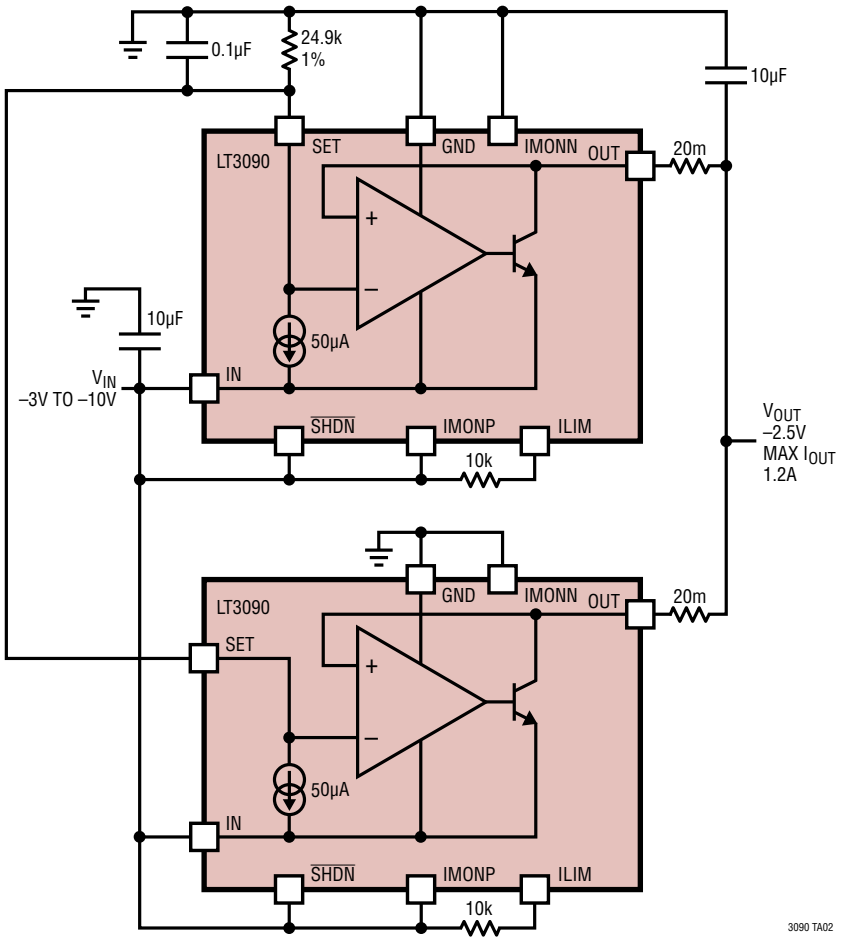
The LT3090 incorporates several protection features that make it ideal for use in battery-powered applications. In addition to the normal protection features associated with monolithic regulators, such as current limiting and thermal limiting, the device also protects itself against reverse output voltages.

Precision current limit and thermal overload protection protect the LT3090 against overload and fault conditions at the device's output. For normal operation, do not allow the junction temperature to exceed 125°C for E- and I-grades and 150°C for H- and MP-grades.

Pulling the LT3090's output above ground induces no damage to the part. If IN is left open circuited or grounded, OUT can be pulled 36V above GND. In this condition, a maximum current of 7mA flows into the OUT pin and out of the GND pin. If IN is powered by a voltage source, OUT sinks the LT3090's (fold back) short-circuit current and protects itself by thermal limiting. In this case, however, grounding the $\overline{\text{SHDN}}$ pin turns off the device and stops OUT from sinking the short-circuit current.

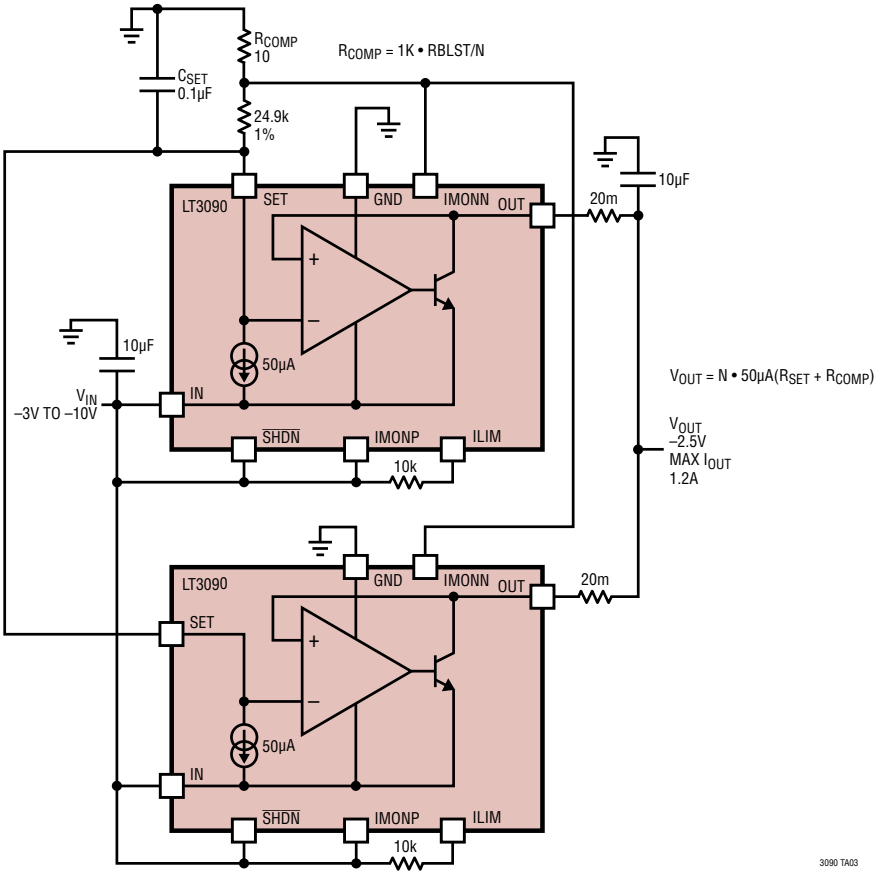
TYPICAL APPLICATIONS

Parallel Devices

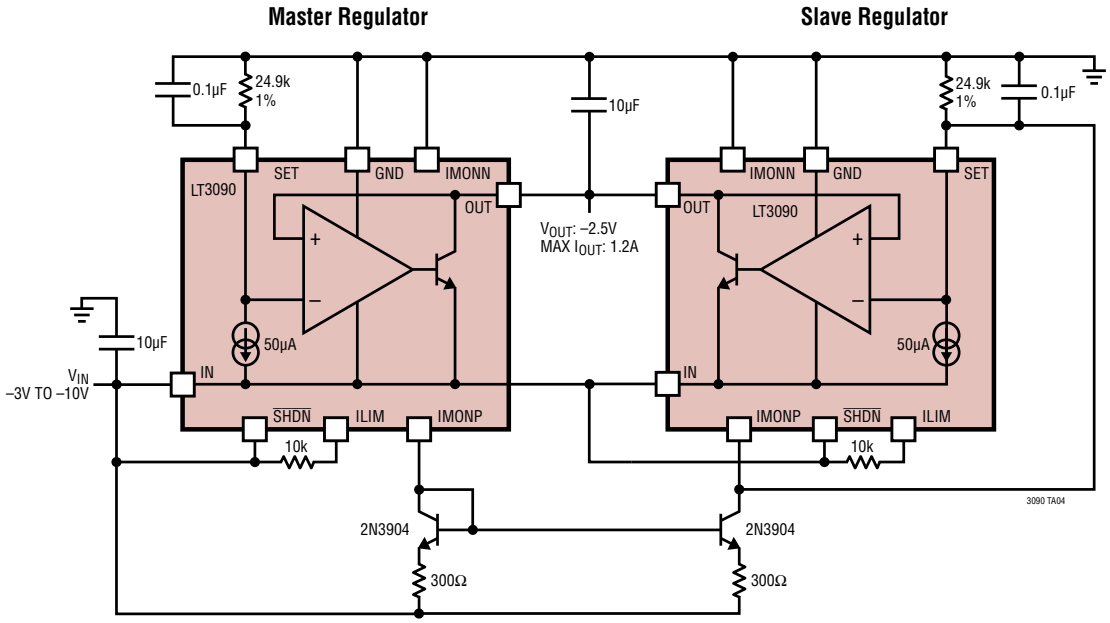


TYPICAL APPLICATIONS

Paralleling Devices Using IMONN to Cancel Ballast Resistor Drop

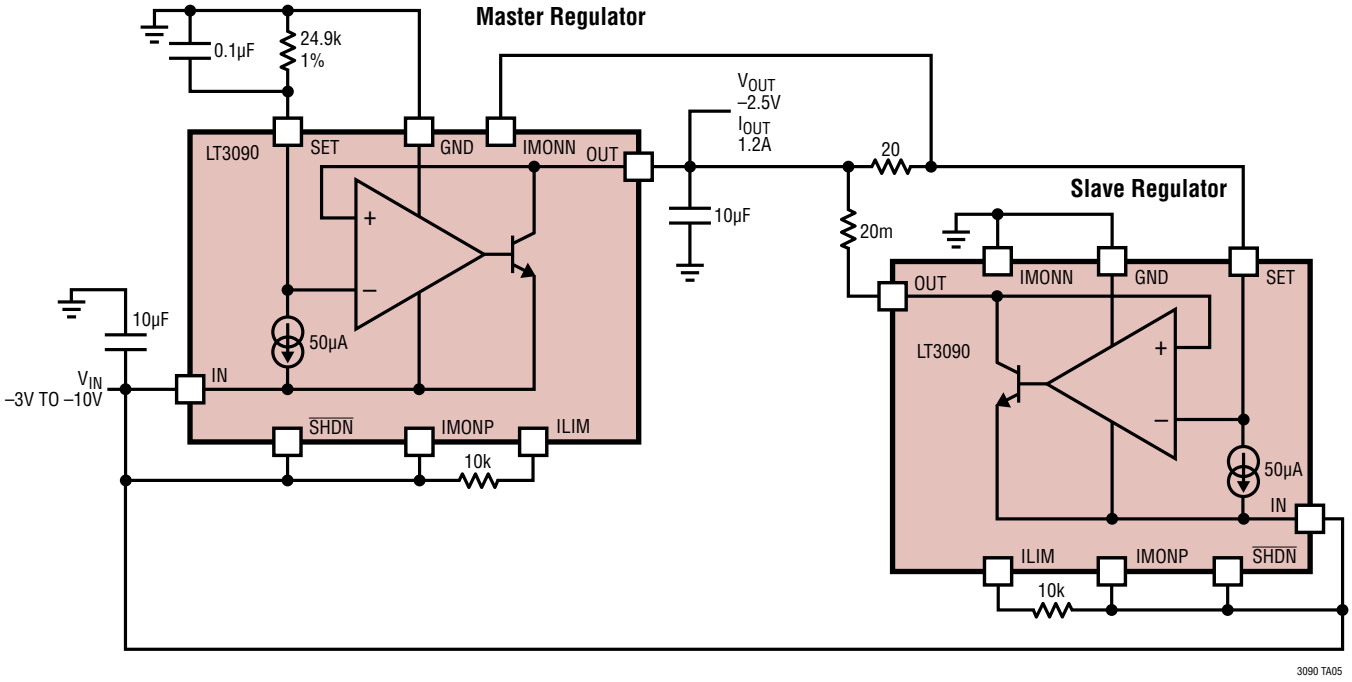


Load Sharing without Ballasting (Using IMONP)

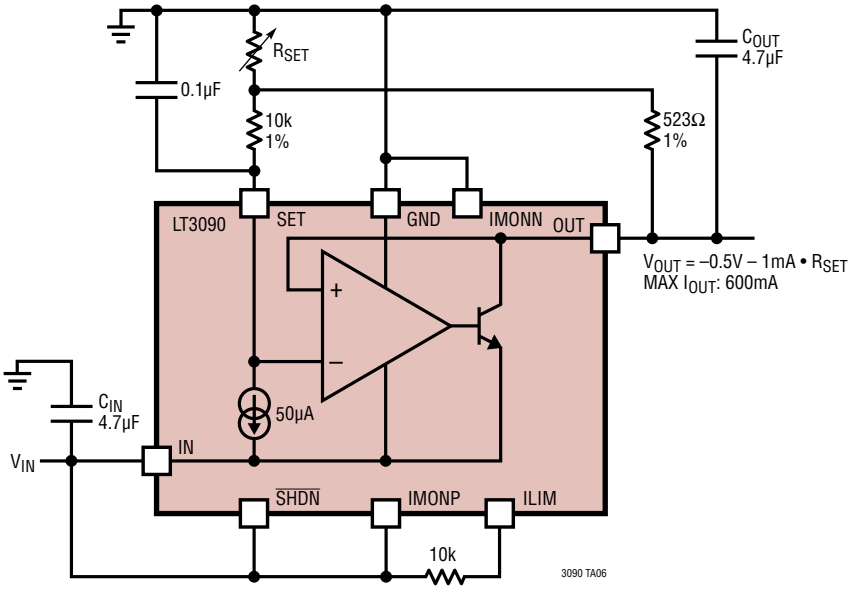


TYPICAL APPLICATIONS

Paralleling Devices without Ballasting (50mA Minimum Load)

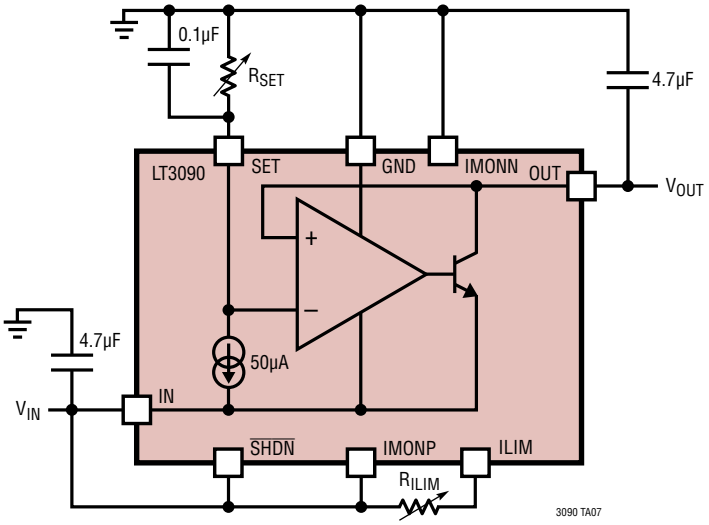


Using Lower Value RSET for Higher Output Voltages



TYPICAL APPLICATIONS

Constant-Current Constant-Voltage Lab Power Supply



Low Dropout Operation for Very Low Output Voltages