Active Clamp Synchronous Forward Controllers with Internal Housekeeping Controller

FEATURES

- **Input Voltage Range: LT3752: 6.5V to 100V, LT3752-1:Limited Only by External Components**
- **Internal Housekeeping DC/DC Controller**
- **Programmable Volt-Second Clamp**
- **High Efficiency Control: Active Clamp, Synchronous Rectification, Programmable Delays**
- Short-Circuit (Hiccup Mode) Overcurrent Protection
- Programmable Soft-Start/Stop
- Programmable OVLO and UVLO with Hysteresis
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an External Clock

APPLICATIONS

- Offline and HV Car Battery Isolated Power Supplies
- 48V Telecommunication Isolated Power Supplies
- Industrial, Automotive and Military Systems

DESCRIPTION

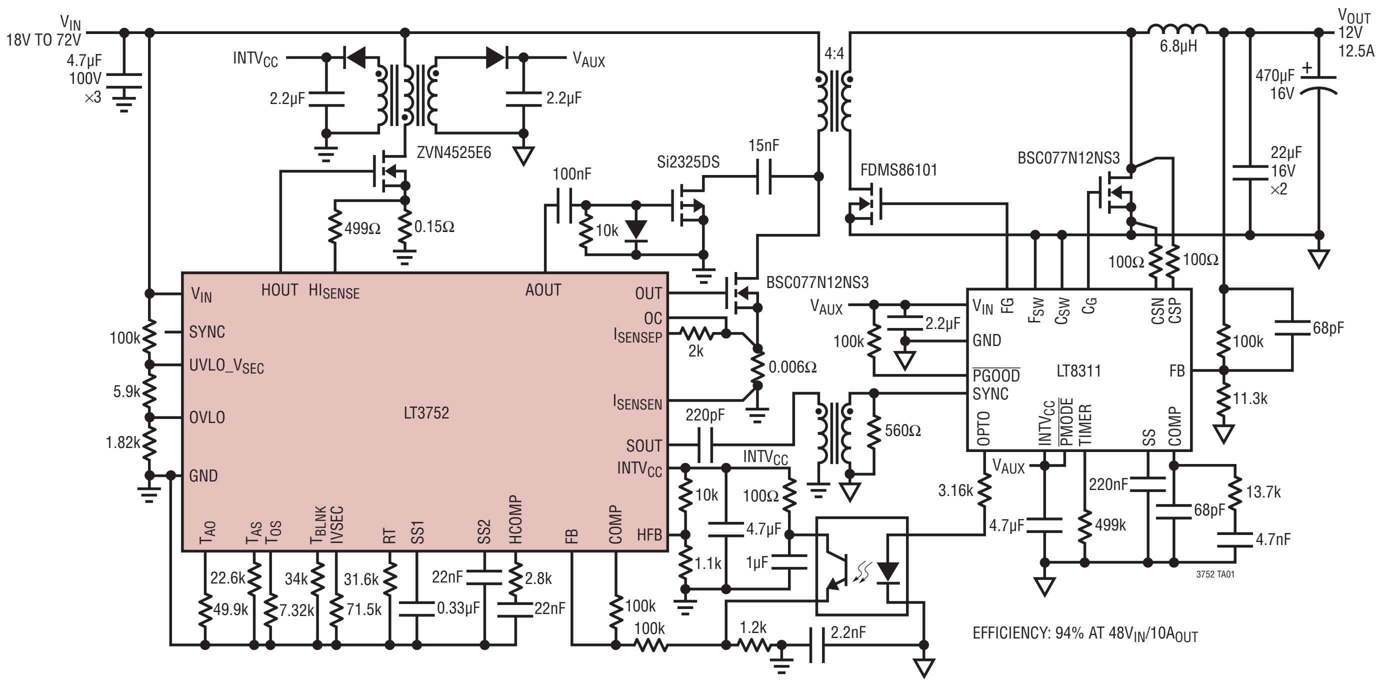
The LT®3752/LT3752-1 are current mode PWM controllers optimized for an active clamp forward converter topology. A DC/DC housekeeping controller is included for improved efficiency and performance. The LT3752 allows operation up to 100V input and the LT3752-1 is optimized for applications with input voltages greater than 100V.

A programmable volt-second clamp allows primary switch duty cycles above 50% for high switch, transformer and rectifier utilization. Active clamp control reduces switch voltage stress and increases efficiency. A synchronous output is available for controlling secondary side synchronous rectification.

The LT3752/LT3752-1 are available in a 38-lead plastic TSSOP package with missing pins for high voltage spacings.

TYPICAL APPLICATION

18V to 72V, 12V/12.5A, 150W Active Clamp Isolated Forward Converter



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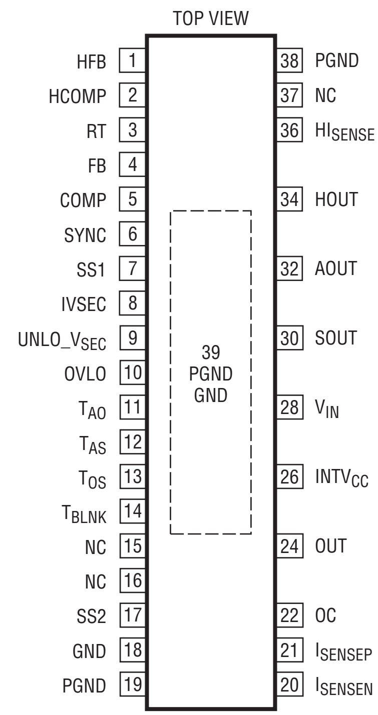
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN} (LT3752) 100V
UVLO_V_{SEC}, OVLO 20V
V_{IN} (LT3752-1) 16V, 8mA
$INTV_{CC}$, SS2 .... 16V
FB, SYNC 6V
SS1, COMP, HCOMP, HFB, RT 3V
I_{SENSEP}, I_{SENSEN}, OC, HI_{SENSE} 0.35V
IVSEC .... –250µA
Operating Junction Temperature Range (Notes 2, 3)
  LT3752EFE, LT3752EFE-1 .... –40°C to 125°C
  LT3752IFE, LT3752IFE-1 .... –40°C to 125°C
  LT3752HFE, LT3752HFE-1 .... –40°C to 150°C
  LT3752MPFE, LT3752MPFE-1 .... –55°C to 150°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 Sec) .... 300°C

PIN CONFIGURATION



FE PACKAGE
VARIATION: FE38(31)
38-LEAD PLASTIC TSSOP
θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS PGND AND GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3752EFE#PBF	LT3752EFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT3752IFE#PBF	LT3752IFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	–40°C to 125°C
LT3752HFE#PBF	LT3752HFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	–40°C to 150°C
LT3752MPFE#PBF	LT3752MPFE#TRPBF	LT3752FE	38-Lead Plastic TSSOP	–55°C to 150°C
LT3752EFE-1#PBF	LT3752EFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	–40°C to 125°C
LT3752IFE-1#PBF	LT3752IFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	–40°C to 125°C
LT3752HFE-1#PBF	LT3752HFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	–40°C to 150°C
LT3752MPFE-1#PBF	LT3752MPFE-1#TRPBF	LT3752FE-1	38-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Operational Input Voltage (LT3752)		●	6.5		100	V
Operational Input Voltage (LT3752-1)		●	10.5		16	V
$V_{IN(ON)}$ (LT3752)		●		5.8	6.4	V
$V_{IN(OFF)}$ (LT3752)				5.5	5.9	V
$V_{IN(ON/OFF)}$ Hysteresis (LT3752)		●	0.1	0.3	0.5	V
$V_{IN(ON)}$ (LT3752-1)		●		9.5	10.4	V
$V_{IN(OFF)}$ (LT3752-1)				7.6		V
$V_{IN(ON/OFF)}$ Hysteresis (LT3752-1)		●	1.61	1.9	2.19	V
V_{IN} Start-Up Current (LT3752-1)	(Notes 6, 7)	●		170	265	µA
V_{IN} Quiescent Current (Housekeeping Controller Only) (LT3752)	HCOMP = 1V (Housekeeping Not Switching), HFB = 0.85V	●		4	6.2	mA
V_{IN} Quiescent Current (Housekeeping Controller Only) (LT3752-1)	HCOMP = 1V (Housekeeping Not Switching), HFB = 0.85V	●		3	4.6	mA
V_{IN} Quiescent Current (Housekeeping Controller + Forward Controller)	HCOMP = 1V (Housekeeping Not Switching), HFB = 1.35V, FB = 1.5V (Main Loop Not Switching)			7.5	9.5	mA
UVLO_V_{SEC} Micropower Threshold (V_{SD})	I_{VIN} < 20µA	●	0.2	0.4	0.6	V
V_{IN} Shutdown Current (Micropower)	UVLO_V_{SEC} = 0.2V			20	40	µA
UVLO_V_{SEC} Threshold (V_{SYS_UV})		●	1.180	1.250	1.320	V
V_{IN} Shutdown Current (After Soft-Stop)	UVLO_V_{SEC} = 1V			165	220	µA
UVLO_V_{SEC} (ON) Current	UVLO_V_{SEC} = V_{SYS_UV} + 50mV			0		µA
UVLO_V_{SEC} (OFF) Current Hysteresis Current With One-Shot Communication Current	UVLO_V_{SEC} = V_{SYS_UV} – 50mV (Note 15)	● 	4.0	5 25	6.0	µA µA
OVLO (Rising) (No Switching, Reset SS1)		●	1.220	1.250	1.280	V
OVLO (Falling) (Restart SS1)				1.215		V
OVLO Hysteresis		●	23	35	47	mV
OVLO Pin Current (Note 10)	OVLO = 0V OVLO = 1.5V (SS1 = 2.7V) OVLO = 1.5V (SS1 = 1.0V)			5 0.9 5	100 100	nA mA nA
Oscillator (Forward Controller: OUT, SOUT, AOUT)						
Frequency: f_{OSC} = 100kHz	R_T = 82.5k		94	100	106	kHz
Frequency: f_{OSC} = 300kHz	R_T = 24.9k	●	279	300	321	kHz
Frequency: f_{OSC} = 500kHz	R_T = 14k		470	500	530	kHz
f_{OSC} Line Regulation	R_T = 24.9k 6.5V < V_{IN} < 100V (LT3752) 10.5V < V_{IN} < 16V (LT3752-1)			 0.05 0.05	 0.1 0.1	 %/V %/V
Frequency and D_{VSEC} Foldback Ratio (LT3752) (Fold)	SS1 = V_{SSACT} + 25mV, SS2 = 2.7V			4		
Frequency and D_{VSEC} Foldback Ratio (LT3752-1) (Fold)	SS1 = V_{SS1ACT} + 25mV, SS2 = 2.7V			2		
SYNC Input High Threshold	(Note 4)	●		1.2	1.8	V
SYNC Input Low Threshold	(Note 4)	●	0.6	1.025		V
SYNC Pin Current	SYNC = 6V			75		µA
SYNC Frequency/Programmed f_{OSC}			1.0		1.25	kHz/kHz
Linear Regulator ($INTV_{CC}$) (LT3752)						
$INTV_{CC}$ Regulation Voltage			6.6	7	7.2	V
Dropout (V_{IN}-$INTV_{CC}$)	V_{IN} = 6.5V, I_{INTVCC} = 10mA			0.8		V
$INTV_{CC}$ UVLO(+)	(Start Switching)			4.75	5	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ UVLO(–)	(Stop Switching)			4.6	4.85	V
$INTV_{CC}$ UVLO Hysteresis			0.075	0.15	0.24	V
Linear Regulator ($INTV_{CC}$) (LT3752-1)						
$INTV_{CC}$ Regulation Voltage			9.4	10	10.4	V
Dropout (V_{IN}-$INTV_{CC}$)	V_{IN} = 8.75V, I_{INTVCC} = 10mA			0.6		V
$INTV_{CC}$ UVLO(+)	(Start Switching)			7	7.4	V
$INTV_{CC}$ UVLO(–)	(Stop Switching)			6.8	7.2	V
$INTV_{CC}$ UVLO Hysteresis			0.1	0.2	0.3	V
Linear Regulator ($INTV_{CC}$) (LT3752/LT3752-1)						
$INTV_{CC}$ OVLO(+)	(Stop Switching)		15.9	16.5	17.2	V
$INTV_{CC}$ OVLO(–)	(Start Switching)		15.4	16	16.7	V
$INTV_{CC}$ OVLO Hysteresis			0.38	0.5	0.67	V
$INTV_{CC}$ Current Limit	$INTV_{CC}$ = 0V $INTV_{CC}$ = 5.75V (LT3752) $INTV_{CC}$ = 8.75V (LT3752-1)	 ● ●	17 35 35	23 50 50	29 60 60	mA mA mA
Error Amplifier						
FB Reference Voltage		●	1.220	1.250	1.275	V
FB Line Reg	6.5V < V_{IN} < 100V (LT3752) 10.5V < V_{IN} < 16V (LT3752-1)			0.1 0.1	0.3 0.3	mV/V mV/V
FB Load Reg	COMP_SW – 0.1V < COMP < COMP_V_{OH} – 0.1V			0.1	0.3	mV/V
FB Input Bias Current	(Note 10)			50	200	nA
Open-Loop Voltage Gain				85		dB
Unity-Gain Bandwidth	(Note 8)			2.5		MHz
COMP Source Current	FB = 1V, COMP = 1.75V (Note 10)		6	11		mA
COMP Sink Current	FB = 1.5V, COMP = 1.75V		6.5	11.5		mA
COMP Output High Clamp	FB = 1V			2.6		V
COMP Switching Threshold				1.25		V
Current Sense (Main Loop)						
I_{SENSEP} Maximum Threshold	FB = 1V, OC = 0V		180	220	260	mV
COMP Current Mode Gain	$\Delta V_{COMP}/\Delta V_{ISENSEP}$			6.1		V/V
I_{SENSEP} Input Current (D = 0%)	(Note 10)			2		µA
I_{SENSEP} Input Current (D = 80%)	(Note 10)			33		µA
I_{SENSEN} Input Current	FB = 1.5V (COMP Open) (Note 10) FB = 1V (COMP Open) (Note 10)			20 90	30 135	µA µA
OC Overcurrent Threshold		●	82.5	96	107.5	mV
OC Input Current				200	500	nA
AOUT Driver (Active Clamp Switch Control) (LT3752 External PMOS; LT3752-1 External NMOS)						
AOUT Rise Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			23		ns
AOUT Fall Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			19		ns
AOUT Low Level				0.1		V
AOUT High Level	$INTV_{CC}$ = 12V		11.9			V
AOUT High Level in Shutdown (LT3752)	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{AOUT} = 1mA Out of the Pin		7.8			V
AOUT Low Level in Shutdown (LT3752-1)	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 12V, I_{AOUT} = 1mA Into the Pin			0.25		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
AOUT Edge to OUT (Rise): (t_{AO})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 44.2k R_{TAO} = 73.2k (Note 11)		 168 253	 218 328	 268 403	 ns ns
OUT (Fall) to AOUT Edge: (t_{OA})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 44.2k R_{TAO} = 73.2k (Note 12)		 150 214	 196 295	 250 376	 ns ns
SOUT Driver (Synchronous Rectification Control)						
SOUT Rise Time	C_{OUT} = 1nF, $INTV_{CC}$ = 12V (Note 5)			21		ns
SOUT Fall Time	C_{OUT} = 1nF, $INTV_{CC}$ = 12V (Note 5)			19		ns
SOUT Low Level				0.1		V
SOUT High Level	$INTV_{CC}$ = 12V		11.9			V
SOUT High Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{SOUT} = 1mA Out of the Pin		7.8			V
AOUT Edge to SOUT (Fall): (t_{AS})	C_{AOUT} = C_{SOUT} = 1nF, $INTV_{CC}$ = 12V R_{TAS} = 44.2k (Note 13) R_{TAS} = 73.2k		 168 253	 218 328	 268 403	 ns ns
SOUT (Fall) to OUT (Rise): (t_{SO} = t_{AO} – t_{AS})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TAO} = 73.2k, R_{TAS} = 44.2k (Notes 11, 13) R_{TAO} = 44.2k, R_{TAS} = 73.2k		 70 –70	 110 –110	 132 –132	 ns ns
OUT (Fall) to SOUT (Rise): (t_{OS})	C_{SOUT} = 1nF, C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V R_{TOS} = 14.7k R_{TOS} = 44.2k (Note 14)		 52 102	 68 133	 84 164	 ns ns
OUT Driver (Main Power Switch Control)						
OUT Rise Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 5)			19		ns
OUT Fall Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 5)			20		ns
OUT Low Level				0.1		V
OUT High Level	$INTV_{CC}$ = 12V		11.9			V
OUT Low Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 8V, I_{OUT} = 1mA Into the Pin			0.25		V
OUT (Volt-Sec) Max Duty Cycle Clamp D_{VSEC} (1 • System Input (Min)) × 100 D_{VSEC} (2 • System Input (Min)) × 100 D_{VSEC} (4 • System Input (Min)) × 100	R_T = 24.9k, R_{IVSEC} = 51.1k, FB = 1V, SS1 = 2.7V UVLO_V_{SEC} = 1.25V UVLO_V_{SEC} = 2.50V UVLO_V_{SEC} = 5.00V		 68.5 34.3 17.5	 72.5 36.5 18.6	 76.2 38.7 19.7	 % % %
OUT Minimum ON Time	C_{OUT} = 3.3nF, $INTV_{CC}$ = 12V (Note 9) R_{TBLNK} = 14.7k R_{TBLNK} = 73.2k (Note 16)			 325 454		 ns ns
SS1 Pin (Soft-Start: Frequency and D_{VSEC}) (Soft-Stop: COMP Pin, Frequency and D_{VSEC})						
SS1 Reset Threshold ($V_{SS1(RTH)}$)				150		mV
SS1 Active Threshold ($V_{SS1(ACT)}$)	(Allow Switching)			1.25		V
SS1 Charge Current (Soft-Start)	SS1 = 1.5V (Note 10)		7	11.5	16	µA
SS1 Discharge Current (Soft-Stop)	SS1 = 1V, UVLO_V_{SEC} = V_{SYS_UV} – 50mV		6.4	10.5	14.6	µA
SS1 Discharge Current (Hard Stop) OC > OC Threshold $INTV_{CC}$ < $INTV_{CC}$ UVLO(–) OVLO > OVLO(+)	SS1 = 1V			 0.9 0.9 0.9		 mA mA mA
SS2 Pin (Soft-Start: Comp Pin)						
SS2 Discharge Current	SS1 < $V_{SS(ACT)}$, SS2 = 2.5V			2.8		mA
SS2 Charge Current	SS1 > $V_{SS(ACT)}$, SS2 = 1.5V		11	21	28	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, UVLO_V_{SEC} = 2.5V.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Error Amplifier (Housekeeping Controller)						
HFB Reference Voltage			0.90	1.000	1.10	V
HFB Line Reg	6.5V < V_{IN} < 100V (LT3752) 10.5V < V_{IN} < 16V (LT3752-1)			0.1 0.1		mV/V mV/V
HFB Load Reg	HCOMP V_{SW} – 0.1V < HCOMP < HCOMP V_{OH} – 0.1V			–6		mV/V
HFB Input Bias Current	HFB = 1.1V (Note 10)			85	170	nA
Transconductance	ΔI_{HCOMP} ±5µA			250		µS
Voltage Gain				175		V/V
Power Good(+) (HFB Level)				0.96		V
Power Good(–) (HFB Level)				0.92		V
HFB OVLO(+)	(Disable HOUT Switching)			1.206		V
HFB OVLO(–)	(Enable Housekeeping Operation)			1.150		V
HCOMP Source Current	HCOMP = 1.75V (Note 10)		11	15	19	µA
HCOMP Sink Current	HCOMP = 1.75V		13	18	23	µA
HCOMP Output High Clamp				2.9		V
HCOMP Switching Threshold				1.28		V
Current Sense (Housekeeping Controller)						
HI_{SENSE} Peak Current Threshold	HFB = 0.8V		69	79	86.5	mV
HCOMP Current Mode Gain	$\Delta V_{HCOMP}/\Delta V_{HISENSE}$			9.1		V/V
HI_{SENSE} Input Current (D = 0%) HI_{SENSE} Input Current (D = 80%)	(Note 10)			2 52		µA µA
HI_{SENSE} Overcurrent Threshold			84.6	98	105.4	mV
HOUT Driver (Housekeeping Controller)						
HOUT Rise Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			13		ns
HOUT Fall Time	C_L = 1nF (Note 5), $INTV_{CC}$ = 12V			12		ns
HOUT Low Level				0.1		V
HOUT High Level LT3752 LT3752-1	$INTV_{CC}$ = 12V		 11.9 11.9			 V V
HOUT Low Level in Shutdown	UVLO_V_{SEC} = 0V, $INTV_{CC}$ = 12V, I_{HOUT} = 1mA Into the Pin			0.25		V
HOUT Maximum Duty Cycle	HCOMP = 2.7V, R_T = 24.9k		90	95		%
HOUT Minimum ON Time	C_L = 1nF (Note 9), $INTV_{CC}$ = 12V			350		ns
Soft-Start (HSS) (Housekeeping Controller)						
HSS (Internal) Ramp Time (t_{HSS})	HCOMP SW ≥ HCOMP V_{OH} – 0.1V			2.2	4	ms
Oscillator (Housekeeping Controller)						
Frequency (f_{HOUT}) (f_{OSC} Folded Back) (LT3752)	HFB = 0.8V, R_T = 24.9k, SS1 = 0V		55	65	75	kHz
Frequency (f_{HOUT}) (f_{OSC} Folded Back) (LT3752-1)	HFB = 0.8V, R_T = 24.9k, SS1 = 0V		119	141	163	kHz
Frequency (f_{HOUT}) (Full-Scale f_{OSC})	HFB = 1.15V, HCOMP = 2.7V	●	279	300	321	kHz

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LT3752EFE/LT3752EFE-1 are guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3752IFE/LT3752IFE-1 are guaranteed to meet performance specifications from –40°C to 125°C junction temperature. The LT3752HFE/LT3752HFE-1 are guaranteed to meet performance specifications from –40°C to 150°C junction temperature. The LT3752MPFE/LT3752MPFE-1 are tested and guaranteed to meet performance specifications from –55°C to 150°C junction temperature.

Note 3: For maximum operating ambient temperature, see the Thermal Calculations section in the Applications Information section.

Note 4: SYNC minimum and maximum thresholds are guaranteed by SYNC frequency range test using a clock input with guard banded SYNC levels of 0.7V low level and 1.7V high level.

Note 5: Rise and fall times are measured between 10% and 90% of gate driver supply voltage.

Note 6: Guaranteed by correlation to static test.

Note 7: V_{IN} start-up current is measured at $V_{IN} = V_{IN(ON)}$ – 0.25V and then scaled by 1.18× to correlate to worst-case V_{IN} current required for part start-up at $V_{IN} = V_{IN(ON)}$.

Note 8: Guaranteed by design.

Note 9: ON times are measured between rising and falling edges at 50% of gate driver supply voltage.

Note 10: Current flows out of pin.

Note 11: Guaranteed by correlation to R_{TAS} = 73.2k test.

Note 12: t_{OA} timing guaranteed by design based on correlation to measured t_{AO} timing.

Note 13: Guaranteed by correlation to R_{TAO} = 44.2k test.

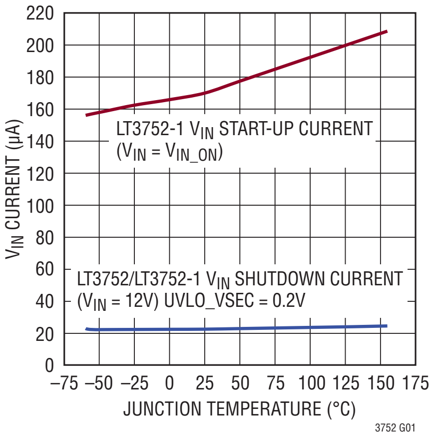
Note 14: Guaranteed by correlation to R_{TOS} = 14.7k test.

Note 15: A 2µs one-shot of 20µA from the UVLO_V_{SEC} pin allows communication between ICs to begin shutdown (useful when stacking supplies for more power (= inputs in parallel/outputs in series)). The current is tested in a static test mode. The 2µs one-shot is guaranteed by design.

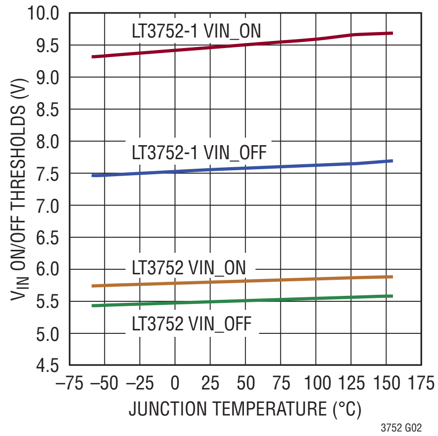
Note 16: Guaranteed by correlation to R_{TBLNK} = 14.7k test.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

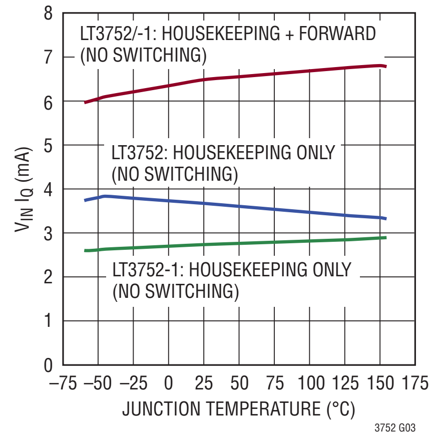
V_{IN} Start-Up and Shutdown Current vs Junction Temperature



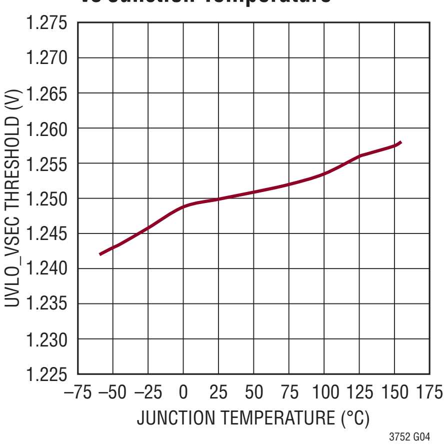
$V_{IN(ON)}$, $V_{IN(OFF)}$ Thresholds vs Junction Temperature



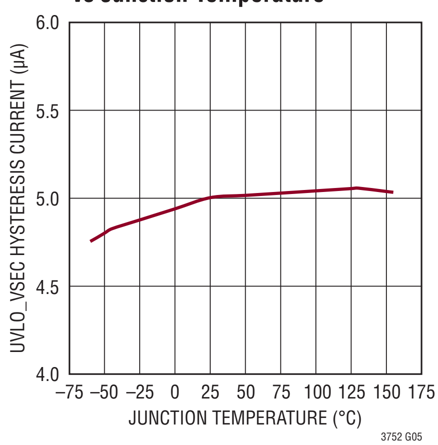
V_{IN} Quiescent Current vs Junction Temperature



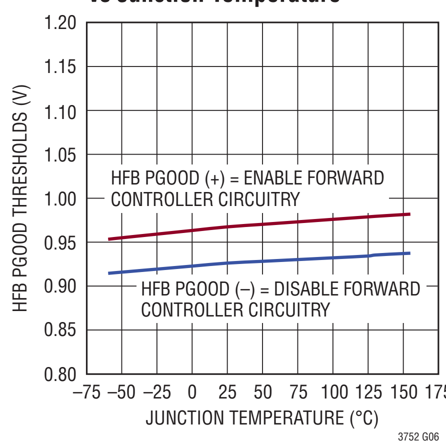
UVLO_VSEC Turn-On Threshold vs Junction Temperature



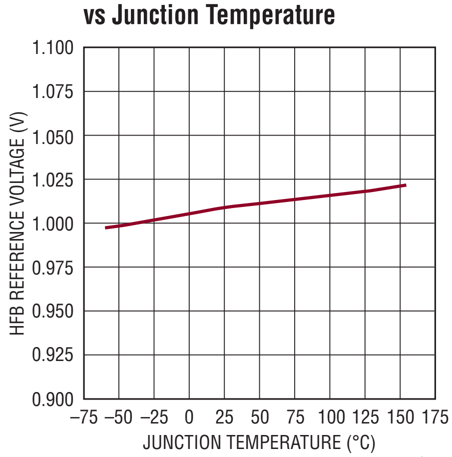
UVLO_V_{SEC} Hysteresis Current vs Junction Temperature



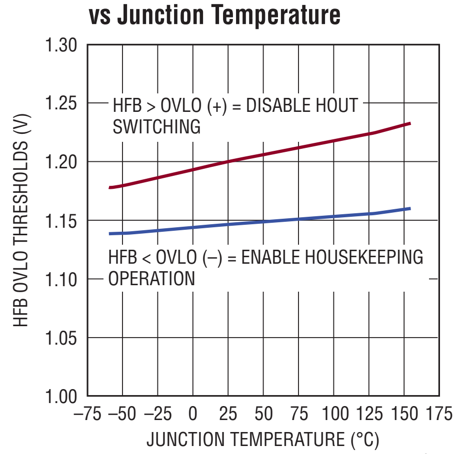
HFB PGOOD Thresholds vs Junction Temperature



HFB Reference Voltage vs Junction Temperature

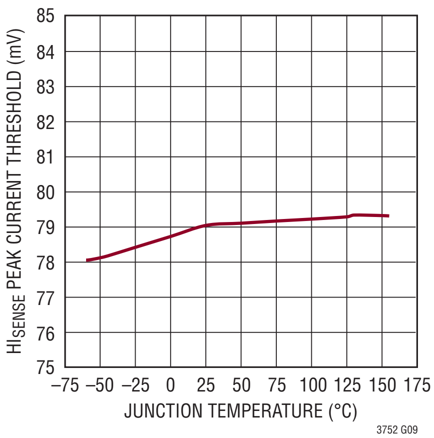


HFB OVLO Thresholds vs Junction Temperature

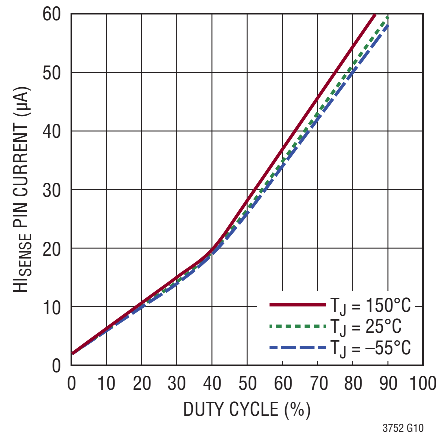


TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

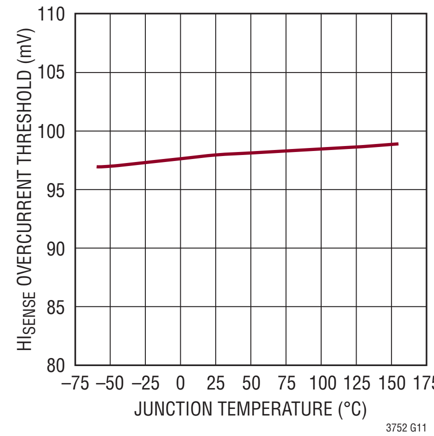
HI_{SENSE} Peak Current Threshold vs Junction Temperature



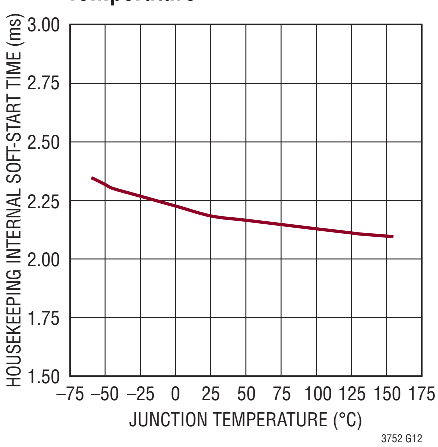
HI_{SENSE} Pin Current vs Duty Cycle



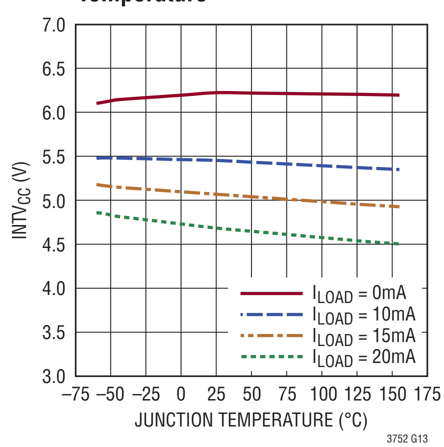
HI_{SENSE} Overcurrent (Hiccup Mode) Threshold vs Junction Temperature



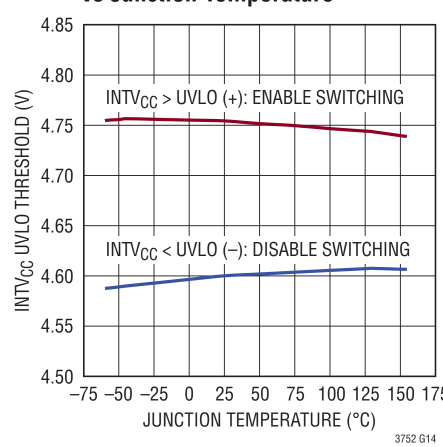
Housekeeping Internal Soft-Start Time (HSS) vs Junction Temperature



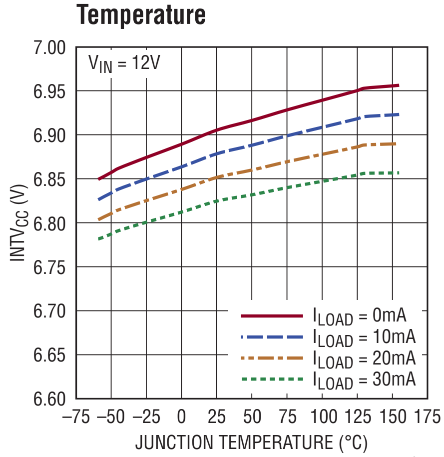
LT3752: $INTV_{CC}$ in Dropout at $V_{IN} = 6.5V$ vs Current, Junction Temperature



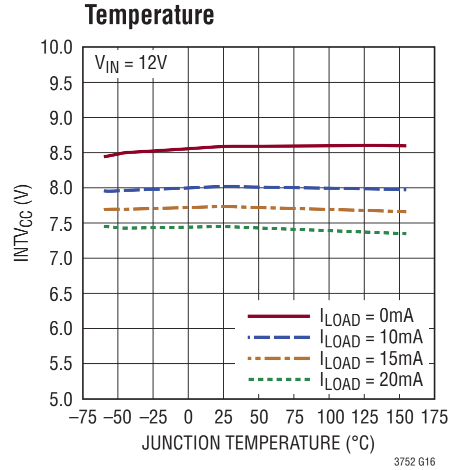
LT3752: $INTV_{CC}$ UVLO Thresholds vs Junction Temperature



LT3752: $INTV_{CC}$ Regulation Voltage vs Current, Junction Temperature

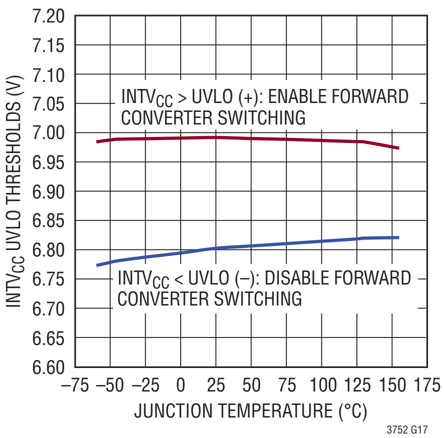


LT3752-1: $INTV_{CC}$ in Dropout at $V_{IN} = 8.75V$ vs Current, Junction Temperature

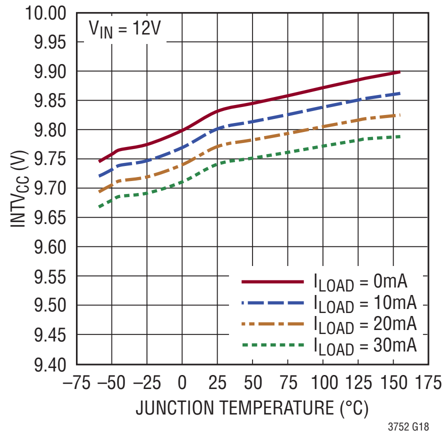


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

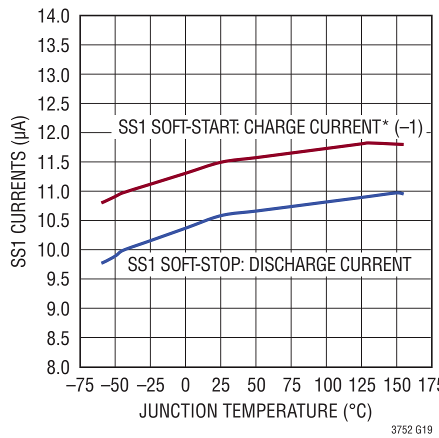
LT3752-1: $INTV_{CC}$ UVLO Thresholds vs Junction Temperature



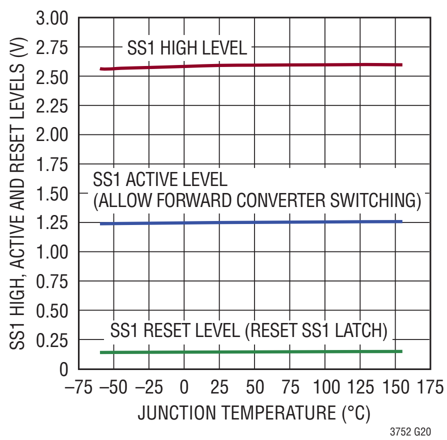
LT3752-1: $INTV_{CC}$ Regulation Voltage vs Current, Junction Temperature



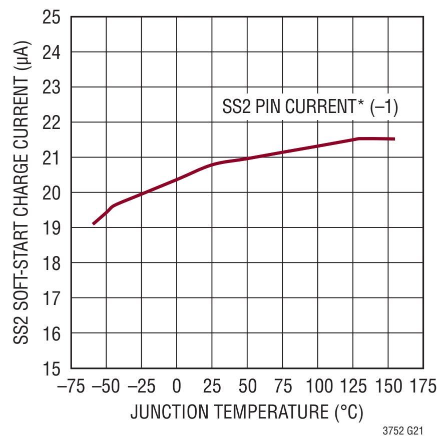
SS1 Soft-Start/Soft-Stop Pin Currents vs Junction Temperature



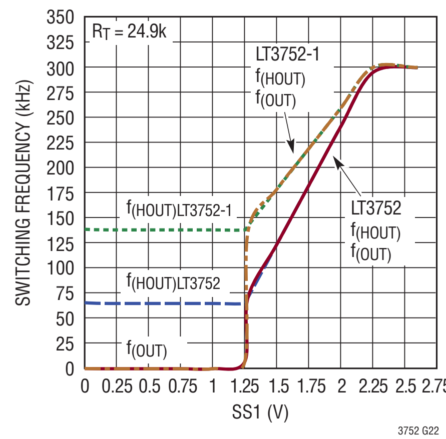
SS1 High, Active and Reset Levels vs Junction Temperature



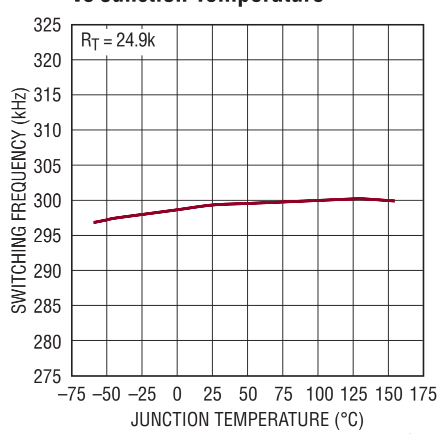
SS2 Soft-Start Charge Current vs Junction Temperature



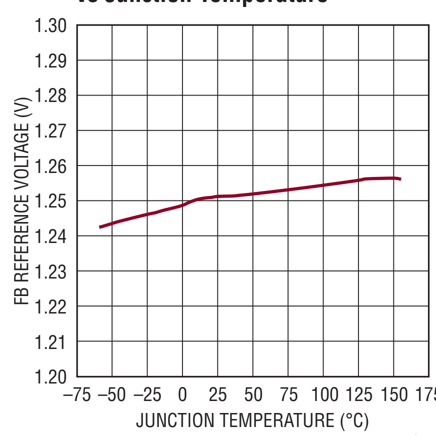
Switching Frequency vs SS1 Pin Voltage



Switching Frequency vs Junction Temperature

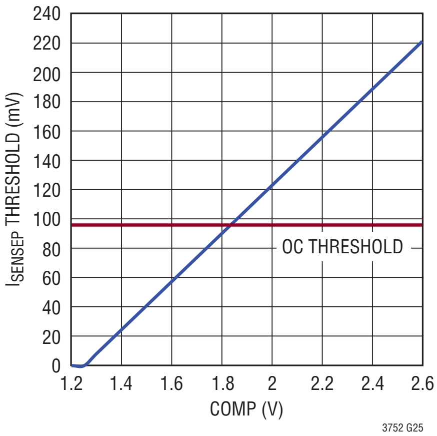


FB Reference Voltage vs Junction Temperature

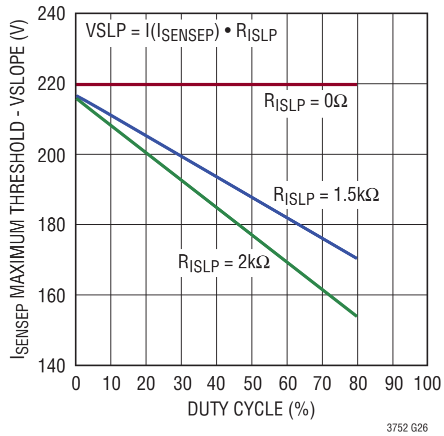


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

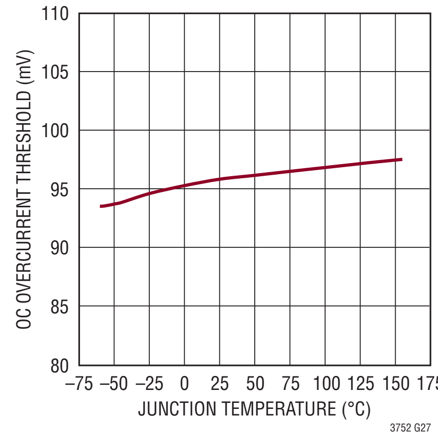
I_{SENSEP} Maximum Threshold vs COMP



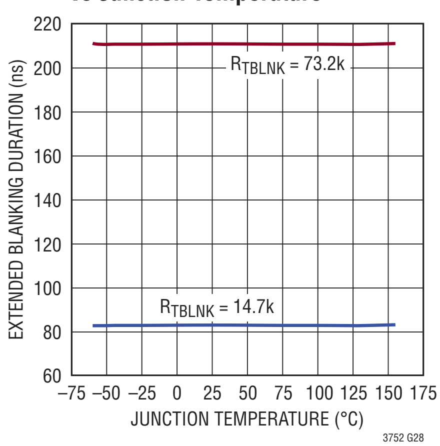
I_{SENSEP} Maximum Threshold – VSLP vs Duty Cycle (Programming Slope Compensation)



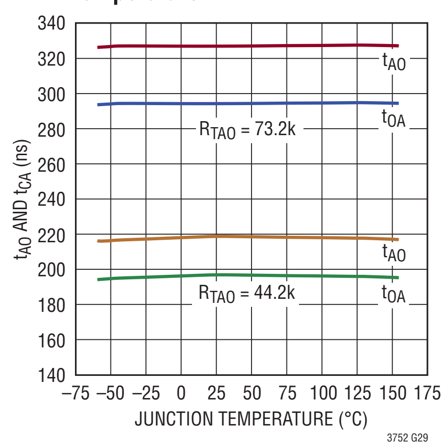
OC Overcurrent (Hiccup Mode) Threshold vs Junction Temperature



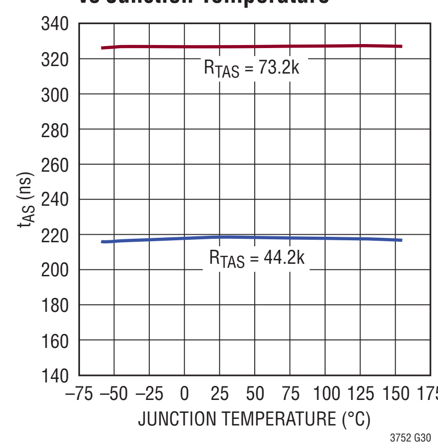
Extended Blanking Duration vs Junction Temperature



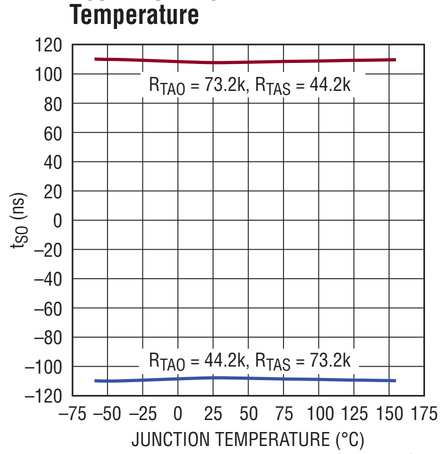
AOUT to OUT Delay (t_{AO}) and OUT to AOUT Delay (t_{OA}) vs Junction Temperature



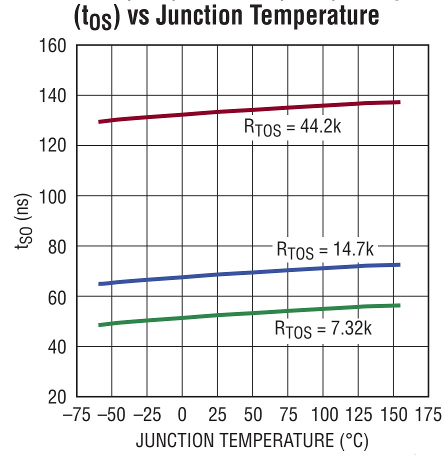
AOUT to SOUT Delay (t_{AS}) vs Junction Temperature



SOUT (Fall) to OUT (Rise) Delay ($t_{SO} = t_{AO} – t_{AS}$) vs Junction Temperature



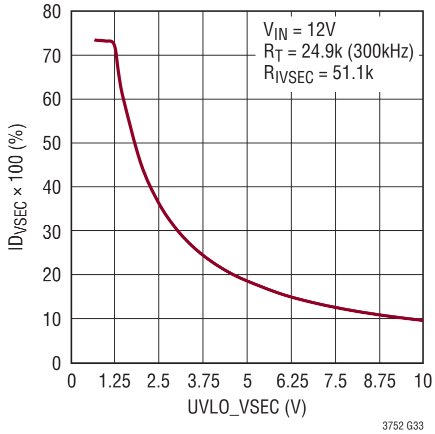
OUT (Fall) to SOUT (Rise) Delay (t_{OS}) vs Junction Temperature



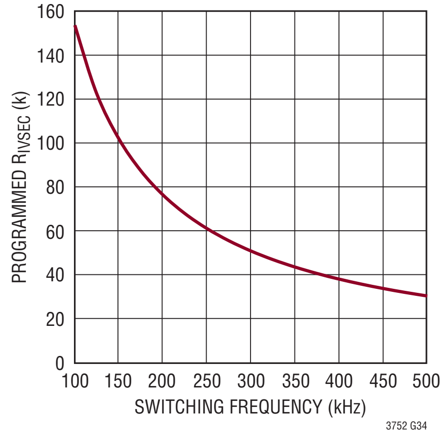
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

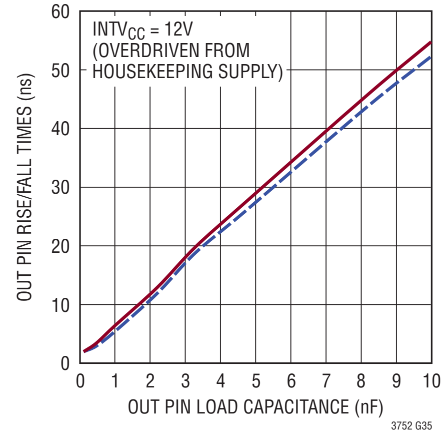
OUT Maximum Duty Cycle Clamp (D_{VSEC}) vs UVLO_V_{SEC}



Required R_{IVSEC} vs Switching Frequency (for D_{VSEC} × 100 = 72.5%, UVLO_VSEC = 1.25V)



OUT Pin Rise/Fall Times vs OUT Pin Load Capacitance



PIN FUNCTIONS

HFB (Pin 1): Housekeeping Supply Error Amplifier Inverting Input.

HCOMP (Pin 2): Housekeeping Supply Error Amplifier Output and Compensation Pin.

RT (Pin 3): A resistor to ground programs switching frequency.

FB (Pin 4): Error Amplifier Inverting Input.

COMP (Pin 5): Error Amplifier Output. Allows various compensation networks for nonisolated applications.

SYNC (Pin 6): Allows synchronization of internal oscillator to an external clock. f_{SYNC} equal to f_{OSC} allowed.

SS1 (Pin 7): Capacitor controls soft-start/stop of switching frequency and volt-second clamp. During soft-stop it also controls the COMP pin.

IVSEC (Pin 8): Resistor Programs OUT Pin Maximum Duty Cycle Clamp (D_{VSEC}). This clamp moves inversely proportional to system input voltage to provide a volt-second clamp.

UVLO_V_{SEC} (Pin 9): A resistor divider from system input allows switch maximum duty cycle to vary inversely proportional with system input. This volt-second clamp prevents transformer saturation for duty cycles above 50%. Resistor divider ratio programs undervoltage lockout (UVLO) threshold. A 5μA pin current hysteresis allows programming of UVLO hysteresis. Pin below 0.4V reduces V_{IN} currents to microamps.

OVLO (Pin 10): A resistor divider from system input programs overvoltage lockout (OVLO) threshold. Fixed hysteresis included.

T_{AO} (Pin 11): A resistor programs nonoverlap timing between AOUT rise and OUT rise control signals.

T_{AS} (Pin 12): Resistors at T_{AO} and T_{AS} define delay between SOUT fall and OUT rise (= $t_{AO} - t_{AS}$).

T_{OS} (Pin 13): Resistor programs delay between OUT fall and SOUT rise.

T_{BLNK} (Pin 14): Resistor programs extended blanking of I_{SENSEP} and OC signals during MOSFET turn-on.

NC (Pins 15, 16, 37): No Connect Pins. These pins are not connected inside the IC. These pins should be left open.

SS2 (Pin 17): Capacitor controls soft-start of COMP pin. Alternatively can connect to OPTO to communicate start of switching to secondary side. If unused, leave the pin open.

GND (Pin 18): Analog Signal Ground. Electrical connection exists inside the IC to the exposed pad (Pin 39).

PIN FUNCTIONS

PGND (Pins 19, 38, 39): The Power Grounds for the IC. The package has an exposed pad (Pin 39) underneath the IC which is the best path for heat out of the package. Pin 39 should be soldered to a continuous copper ground plane under the device to reduce die temperature and increase the power capability of the LT3752/LT3752-1.

I_{SENSEN} (Pin 20): Negative input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET.

I_{SENSEP} (Pin 21): Positive input for the current sense comparator. Kelvin connect to the sense resistor in the source of the power MOSFET. A resistor in series with I_{SENSEP} programs slope compensation.

OC (Pin 22): An accurate 96mV threshold, independent of duty cycle, for detection of primary side MOSFET over-current and trigger of hiccup mode. Connect directly to sense resistor in the source of the primary side MOSFET.

Missing Pins 23, 25, 27, 29, 31, 33, 35: Pins removed for high voltage spacings and improved reliability.

OUT (Pin 24): Drives the gate of an N-channel MOSFET between 0V and $INTV_{CC}$. Active pull-off exists in shutdown.

$INTV_{CC}$ (Pin 26): A linear regulator supply generated from V_{IN}. LT3752 supplies 7V for AOUT, SOUT, OUT and HOUT gate drivers. LT3752-1 supplies 10V for AOUT,SOUT, and OUT gate drivers (HOUT supplied from V_{IN}). $INTV_{CC}$ must be bypassed with a 4.7µF capacitor to power ground. Can be externally driven by the housekeeping supply to remove power from within the IC.

V_{IN} (Pin 28): Input Supply Pin. Bypass with 1µF to ground.

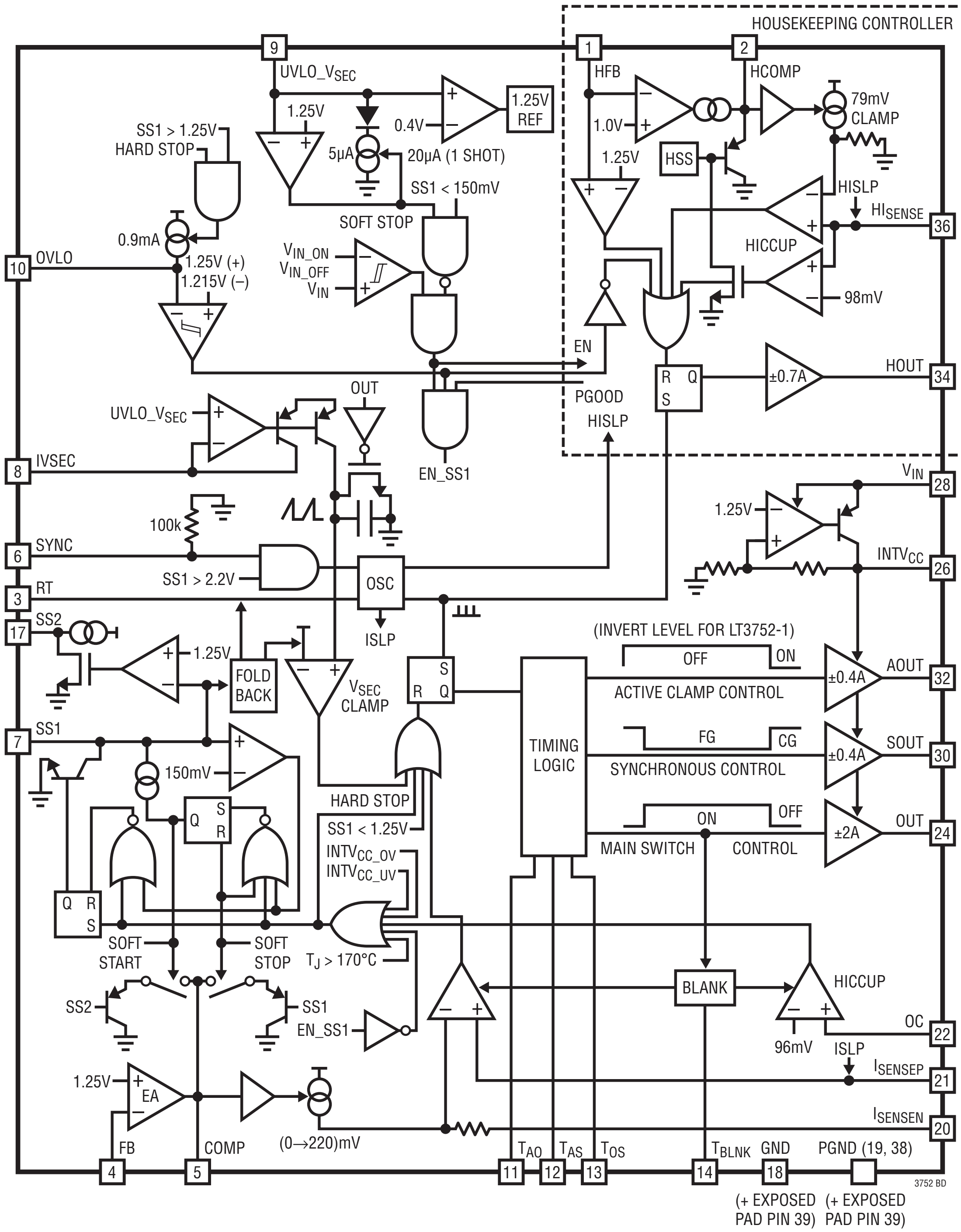
SOUT (Pin 30): Sync signal for secondary side synchronous rectifier controller.

AOUT (Pin 32): Control signal for external active clamp switch. (P-channel LT3752, N-channel LT3752-1).

HOUT (Pin 34): Drives the gate of an N-channel MOSFET used for the housekeeping supply. Active pull-off exists in shutdown.

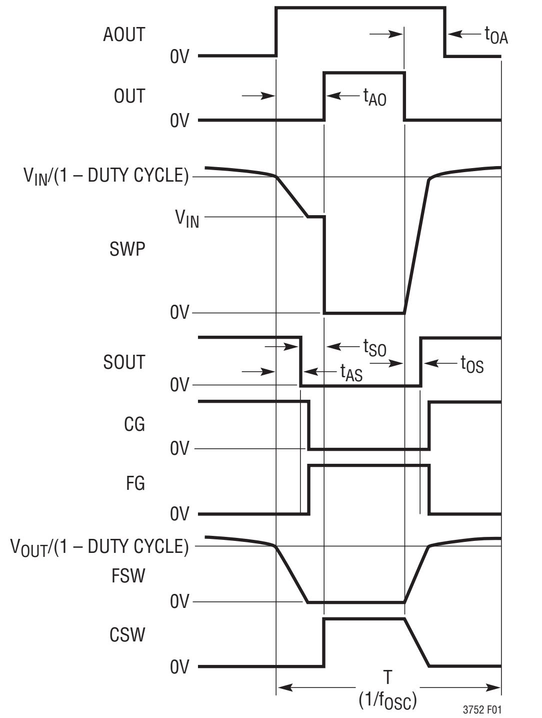
HI_{SENSE} (Pin 36): Current sense input for the house keeping supply. Connect to sense resistor in the source of the power MOSFET. A resistor in series with HI_{SENSE} programs slope compensation.

BLOCK DIAGRAM



PART	SYSTEM INPUT MAX	V_{IN} PIN MAX	V_{IN} ON/OFF	$INTV_{CC}$ UVLO(+)/(REG)	AOUT PHASING
LT3752	100V	100V	5.8V/5.5V	4.75V/7V	for External PMOS
LT3752-1	Limited Only by External Components	16V, 8mA (Internal V_{IN} Clamp)	9.5V/7.6V	7V/10V	for External NMOS

TIMING DIAGRAMS



t_{AO} PROGRAMMED BY R_{TAO}, t_{AS} PROGRAMMED BY R_{TAS}
t_{OS} PROGRAMMED BY R_{TOS}, $t_{OA} = 0.9 \bullet t_{AO}$, $t_{SO} = t_{AO} - t_{AS}$

Figure 1. LT3752 Timing Diagram (LT3752-1 Inverts AOUT Phase for N-Channel Control)

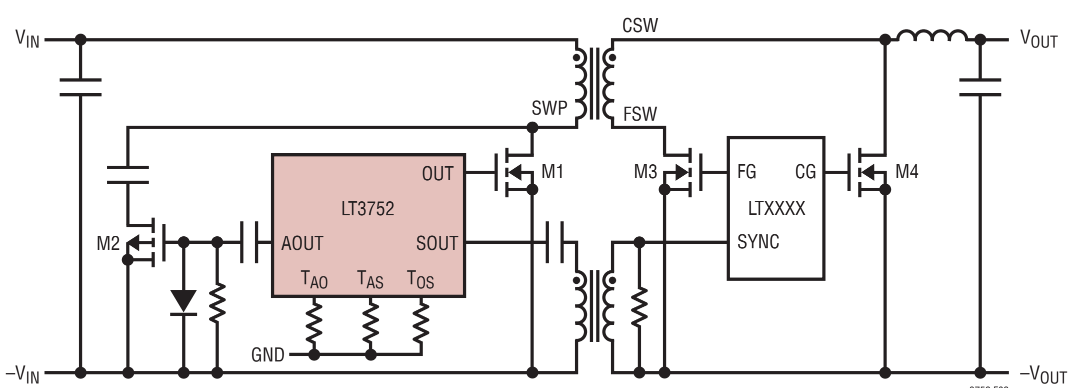


Figure 2. Timing Reference Circuit

TIMING DIAGRAMS

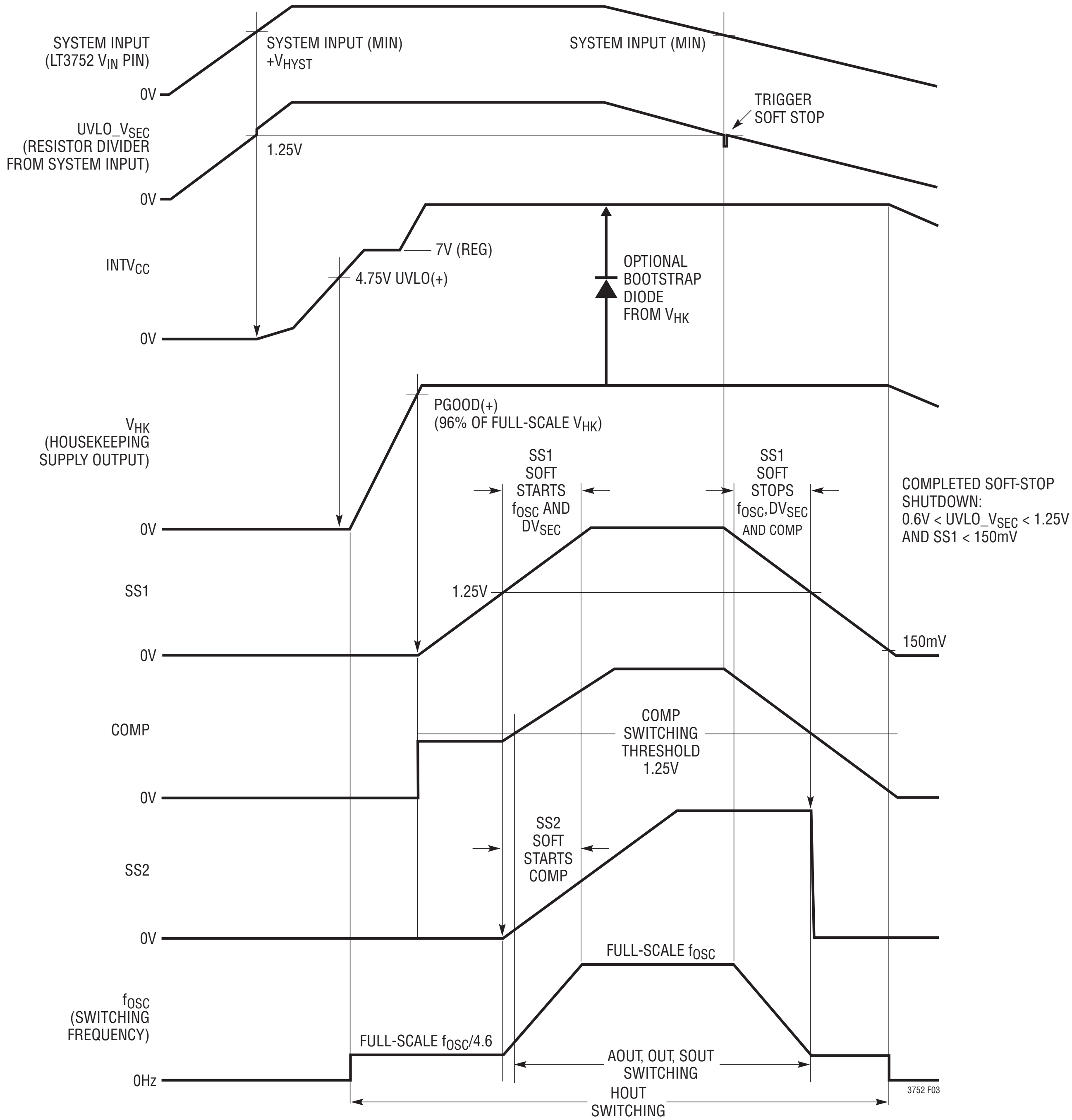


Figure 3. LT3752 Start-Up and Shutdown Timing Diagram

TIMING DIAGRAMS

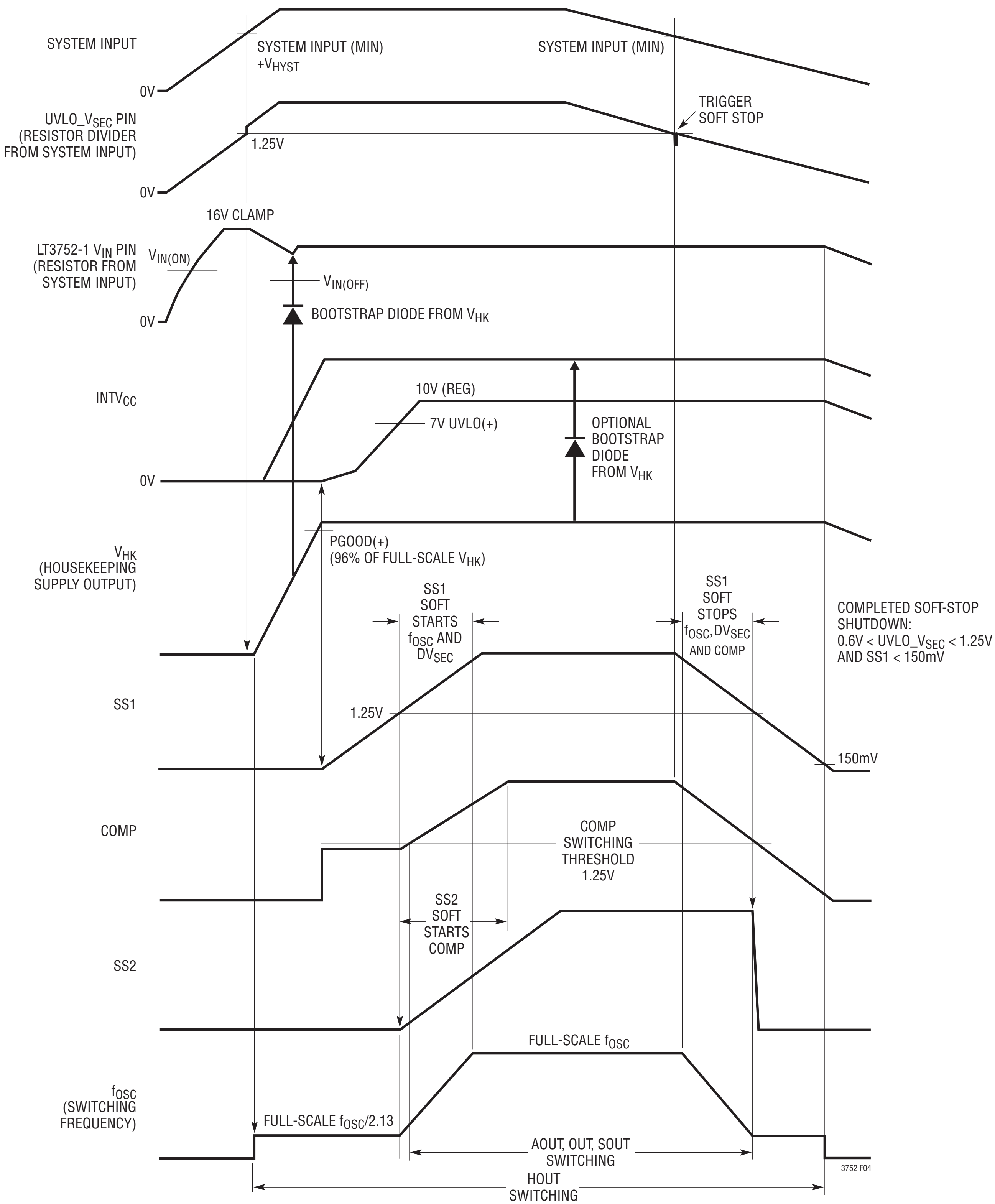


Figure 4. LT3752-1 Start-Up and Shutdown Timing Diagram

OPERATION

Introduction

The LT3752/LT3752-1 are primary side, current mode, PWM controllers optimized for use in a synchronous forward converter with active clamp reset. Combined with an integrated housekeeping controller, each IC provides a compact, versatile, and highly efficient solution. The LT3752 allows V_{IN} pin operation between 6.5V and 100V. For applications with system input voltages greater than 100V, the LT3752-1 allows RC start-up from input voltage levels limited only by external components. The LT3752 and LT3752-1 based forward converters are targeted for power levels up to 400W and are not intended for battery charger applications. For higher power levels the converter outputs can be stacked in series. Connecting UVLO_V_{SEC} pins, OVLO pins, SS1 pins and SS2 pins together allows blocks to react simultaneously to all fault modes and conditions.

Each IC contains an accurate programmable volt-second clamp. When set above the natural duty cycle of the converter, it provides a duty cycle guardrail to limit primary switch reset voltage and prevent transformer saturation during load transients. The accuracy and excellent line regulation of the volt-second clamp provides V_{OUT} regulation for open-loop conditions such as no opto-coupler, reference or error amplifier on the secondary side.

For applications not requiring isolation but requiring high step-down ratios, each IC contains a voltage error amplifier to allow a very simple nonisolated, fully regulated synchronous forward converter.

The integrated housekeeping controller reduces the complexity and size of the main power transformer by avoiding the need for extra windings to create bias supplies. Secondary side ICs no longer require start-up circuitry and can operate even when output voltage is 0V.

A range of protection features include programmable overcurrent (OC) hiccup mode, programmable system input undervoltage lockout (UVLO), programmable system input overvoltage lockout (OVLO) and built-in thermal shutdown. Programmable slope compensation and switching frequency allow the use of a wide range of output inductor values and transformer sizes.

LT3752 Part Start-Up

LT3752 start-up is best described by referring to the Block Diagram and to the start-up waveforms in Figure 3. For part start-up, system input voltage must be high enough to drive the UVLO_V_{SEC} pin above 1.25V and the V_{IN} pin must be greater than 6.5V. An internal linear regulator is activated and provides a 7V $INTV_{CC}$ supply for all gate drivers. The housekeeping controller starts up before the forward controller. An internal soft-start (HSS) ramps the housekeeping HCOMP pin to allow switching at the gate driver output HOUT to drive an external N-channel MOSFET. The housekeeping controller output voltage V_{HK} is regulated when the HFB pin reaches 1.0V. V_{HK} can be used to override $INTV_{CC}$ to reduce power in the part, increase efficiency and to optimize the $INTV_{CC}$ level. During start-up the housekeeping controller switches at the programmed switching frequency (f_{OSC}) folded back by 1/4.6. The SS1 pin of the forward controller is allowed to start charging when V_{HK} reaches 96% of its target value (PGOOD). When SS1 reaches 1.25V, the SS2 pin begins to charge, controlling COMP pin rise and the soft-start of output inductor peak current. The SS1 pin independently soft starts switching frequency and a volt-second clamp. As SS1 charges towards 2.6V the switching frequencies of both controllers remain equal, synchronized and soft started towards full-scale f_{OSC}.

If secondary side control already exists for soft starting the converter output voltage then the SS2 pin can still be used to control initial inductor peak current rise. Simply programming the primary side SS2 soft-start faster than the secondary side allows the secondary side to take over. If SS2 is not needed for soft-start control, its pull-down strength and voltage rating also allow it to drive the input of an opto-coupler connected to $INTV_{CC}$. This allows the option of communicating to the secondary side that switching has begun.

LT3752-1 Part Start-Up

The LT3752-1 start-up of housekeeping supply and forward converter are similar to the LT3752 except for a small change in architecture and V_{IN} pin level. LT3752-1 start-up is best described by referring to the Block Diagram and to

OPERATION

the start-up waveforms in Figure 4. The LT3752-1 starts up by using a high valued resistor from system input to charge up the input capacitor at the V_{IN} pin. If system input is already high enough to generate UVLO_V_{SEC} above 1.25V, then the part turns on once V_{IN} pin charges past $V_{IN(ON)}$ (9.5V). If system input is not high enough to generate UVLO_V_{SEC} above 1.25V, the V_{IN} pin charges towards system input until it reaches an internal 16V, 8mA clamp. The part turns on when system input becomes high enough to generate UVLO_V_{SEC} above 1.25V. As the supply current of the part discharges the V_{IN} capacitor a bootstrap supply must be generated to prevent V_{IN} pin from falling below $V_{IN(OFF)}$ (7.6V).

The LT3752-1 uses the housekeeping controller to provide the bootstrap bias to the V_{IN} pin during RC start-up instead of waiting for the forward converter to also start. This method is more efficient, requires a smaller V_{IN} input capacitor and avoids the need for an auxiliary winding in the main transformer. The part's low start-up current at the V_{IN} pin allows the use of a large start-up resistor to minimize power loss from system input. The V_{IN} capacitor value required for proper start-up is minimized by providing a large $V_{IN(ON)}$-$V_{IN(OFF)}$ hysteresis, a low V_{IN} I_Q and a fast start-up time for the housekeeping controller. In contrast to the LT3752, the LT3752-1 housekeeping gate driver (HOUT) runs from the V_{IN} pin instead of $INTV_{CC}$. This avoids having to use current from the V_{IN} pin to charge the $INTV_{CC}$ capacitor during initial start-up. This means the regulated 10V $INTV_{CC}$ on the LT3752-1 does not wake up until the housekeeping supply is valid. Start-up from this point is similar to the LT3752. The housekeeping supply and forward converter switch together with a soft-started frequency and volt-second clamp. The forward converter peak inductor current is also soft started similar to the LT3752.

APPLICATIONS INFORMATION

Programming System Input Undervoltage Lockout (UVLO) Threshold and Hysteresis

The LT3752/LT3752-1 have an accurate 1.25V shutdown threshold at the UVLO_V_{SEC} pin. This threshold can be used in conjunction with an external resistor divider to define the falling undervoltage lockout threshold (UVLO(–)) for the converter's system input voltage (V_S) (Figure 5). A pin hysteresis current of 5µA allows programming of the UVLO(+) threshold.

V_S (UVLO(–)) [begin SOFT-STOP then shut down]

$$=1.25\left[1+\left(\frac{R1}{R2+R3}\right)\right]$$

V_S (UVLO(+)) [begin SOFT-START]
= V_S (UVLO(–)) + (5µA • R1)

It is important to note that the part enters soft-stop when the UVLO_V_{SEC} pin falls back below 1.25V. During soft-stop the converter continues to switch as it folds back switching frequency, volt-second clamp and COMP pin voltage. See Soft-Stop in the Applications Information section. When the SS2 pin is finally discharged below its 150mV reset threshold both the housekeeping supply and forward converter are shut down.

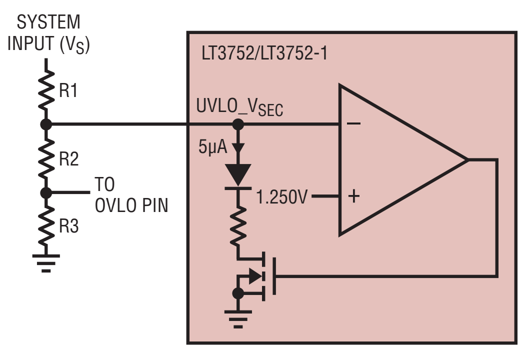


Figure 5. Programming Undervoltage Lockout (UVLO)

Soft-Stop Shutdown

Soft-stop shutdown (similar to system undervoltage) can be commanded by an external control signal. A MOSFET with a diode (or diodes) in series with the drain should be used to pull down the UVLO_V_{SEC} pin below 1.25V but not below the micropower shutdown threshold of 0.6V(max). Typical V_{IN} quiescent current after soft-stop is 165µA.

Micropower Shutdown

If a micropower shutdown is required using an external control signal, an open-drain transistor can be directly connected to the UVLO_V_{SEC} pin. The LT3752/LT3752-1 have a micropower shutdown threshold of typically 0.4V at the UVLO_V_{SEC} pin. V_{IN} quiescent current in micropower shutdown is 20µA.

Programming System Input Overvoltage Lockout (OVLO) Threshold

The LT3752/LT3752-1 have an accurate 1.25V overvoltage shutdown threshold at the OVLO pin. This threshold can be used in conjunction with an external resistor divider to define the rising overvoltage lockout threshold (OVLO(+)) for the converter's system input voltage (V_S) (Figure 6). When OVLO(+) is reached, the part stops switching immediately and a hard stop discharges the SS1 and SS2 pins. The falling threshold OVLO(–) is fixed internally at 1.215V and allows the part to restart in soft-start mode. A single resistor divider can be used from system input supply (V_S) to define both the undervoltage and overvoltage thresholds for the system. Minimum value for R3 is 1k. If OVLO is unused, place a 10k resistor from OVLO pin to ground.

V_S OVLO(+) [stop switching; HARD STOP]

$$=1.25\left[1+\left(\frac{R1+R2}{R3}\right)\right]$$

V_S OVLO(–) [begin SOFT-START]

$$=V_S\ OVLO(+)\bullet\frac{1.215}{1.25}$$

APPLICATIONS INFORMATION

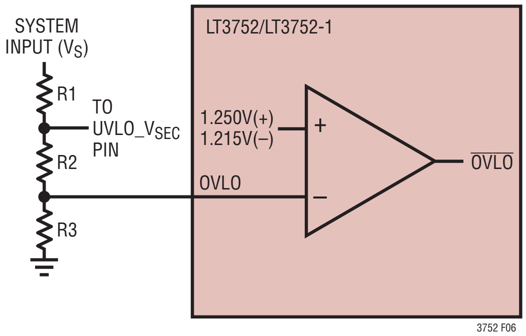


Figure 6. Programming Overvoltage Lockout (OVLO)

LT3752-1 Micropower Start-Up from High System Input Voltages

The LT3752-1 starts up from system input voltage levels limited only by external components (Figure 7). The low start-up current of the LT3752-1 allows a large start-up resistor (R_{START}) to be connected from system input voltage (V_S) to the V_{IN} pin.

When system input voltage is applied, the start-up capacitor (C_{START}) begins charging at the V_{IN} pin. Once the V_{IN} pin exceeds 9.5V (and UVLO_V_{SEC} > 1.25V) the housekeeping controller will start to switch and V_{IN} supply current will begin to discharge C_{START}. The C_{START} capacitor value should be chosen high enough to prevent the V_{IN} pin from falling below 7.6V before the housekeeping supply can provide a bootstrap bias to the V_{IN} pin. The LT3752-1 start-up architecture minimizes the value of C_{START} by activating only the house keeping controller for providing drive back to the V_{IN} pin. The forward controller only operates once the housekeeping supply is established. (If a bootstrap diode is used from the housekeeping supply back to $INTV_{CC}$, this only uses current from system input and not from the V_{IN} pin).

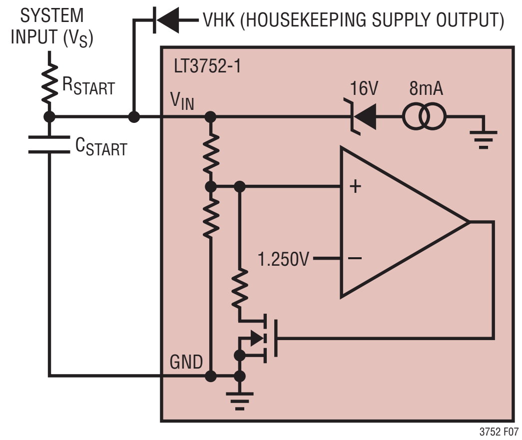


Figure 7. Micropower Start-Up from High System Input

The start-up capacitor can be calculated as:

$$C_{START(MIN)} = \left(I_{HKEEP} + I_{DRIVE}\right)_{(MAX)} \bullet \frac{t_{HSS(MAX)}}{V_{DROOP(MIN)}}$$

where:

I_{HKEEP} = Housekeeping I_Q (not switching)

I_{DRIVE} = $(f_{OSC}/2.13) \bullet Q_G)$

f_{OSC} = full-scale controller switching frequency

Q_G = gate charge (V_{GS} = V_{IN})(HOUT MOSFET)

t_{HSS} = housekeeping output voltage soft-start time

V_{DROOP} = 16V(clamp) – $V_{IN(OFF)}$ or $V_{IN(ONOFFHYST)}$

The start-up resistor can be calculated as:

$$R_{START(MAX)} = \frac{V_{S(MAX)} - V_{IN(ON)(MAX)}}{I_{START(MAX)} \bullet k}$$

where:

$V_{S(MAX)}$ = Maximum system input voltage

$V_{IN(ON)(MAX)}$ = Maximum V_{IN} pin turn on threshold

$I_{START(MAX)}$ = Maximum V_{IN} I_Q for part start-up

k > 1.0 reduces R_{START} and V_{IN} charge-up time

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Worst-case values should be used to calculate the C_{START} and R_{START} required to guarantee start-up and to turn on in the time required.

Example: (LT3752-1)

For $V_{S(MIN)}$ = 75V, $V_{IN(ON)(MAX)}$ = 10.4V

$I_{START(MAX)}$ = 265µA, $I_{HKEEP(MAX)}$ = 4.6mA

Q_G = 8nC (at V_{IN} = 10V), f_{OSC} = 150kHz

$t_{HSS(MAX)}$ = 4ms, $V_{DROOP(MIN)}$ = 1.61V

$$C_{START(MIN)} = (4.6mA + 71kHz \bullet 8nC) \bullet \frac{4ms}{1.61V}$$

$$= 12.8\mu F \ (\text{Choose } 14.7\mu F)$$

$$R_{START(MAX)} = \frac{75V - 10.4V}{265\mu A \bullet k} = 243k \ (\text{for } k = 1.0)$$

The $R_{START(MAX)}$ value should be chosen with higher k values until the charge-up time for C_{START} is acceptable. In most cases, C_{START} will be charged to the 16V clamp on the LT3752-1 V_{IN} pin before system input reaches its UVLO(+) threshold (Figure 4). This will allow an extra 5.6V for V_{DROOP} in the C_{START} equation, allowing a smaller C_{START} value and hence a faster start-up time.

The trade-off of lower R_{START} is greater power dissipation, given by:

$P_{RSTART} = (V_S - V_{IN})^2/R_{START}$

for R_{START} = 200k, $V_{S(MAX)}$ = 150V, V_{IN} = 10V (back driven from housekeeping supply)

$P_{RSTART} = (150 - 10)^2/200k$ = 98mW.

Programming Switching Frequency

The switching frequency for the housekeeping supply and the main forward converter are programmed using a resistor, R_T, connected from analog ground (Pin 18) to the RT pin. Table 1 shows typical f_{OSC} vs R_T resistor values. The value for R_T is given by:

$R_T = 8.39 \bullet X \bullet (1 + Y)$

where,

$X = (10^9/f_{OSC}) - 365$

$Y = (300kHz - f_{OSC})/10^7 \quad (f_{OSC} < 300kHz)$

$Y = (f_{OSC} - 300kHz)/10^7 \quad (f_{OSC} > 300kHz)$

Example: For f_{OSC} = 200kHz,

$R_T = 8.39 \bullet 4635 \bullet (1 + 0.01)$ = 39.28k (choose 39.2k)

The LT3752/LT3752-1 include frequency foldback at start-up (see Figures 3 and 4). In order to make sure that a SYNC input does not override frequency foldback during start-up, the SYNC function is ignored until SS1 pin reaches 2.2V. Both the housekeeping and forward controllers run synchronized to each other and in phase, with or without the SYNC input.

Table 1. R_T vs Switching Frequency (f_{OSC})

SWITCHING FREQUENCY (kHz)	R_T (kΩ)
100	82.5
150	53.6
200	39.2
250	30.9
300	24.9
350	21
400	18.2
450	15.8
500	14

Synchronizing to an External Clock

The LT3752 / LT3752-1 internal oscillator can be synchronized to an external clock at the SYNC pin. SYNC pin high level should exceed 1.8V for at least 100ns and SYNC pin low level should fall below 0.6V for at least 100ns. The SYNC pin frequency should be set equal to or higher than the typical frequency programmed by the RT pin. An f_{SYNC}/f_{OSC} ratio of x (1.0 < x < 1.25) will reduce the externally programmed slope compensation by a factor of 1.2x. If required, the external resistor R_{ISLP} can be reprogrammed higher by a factor of 1.2x. (see Current Sensing and Programmable Slope Compensation).

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The part injection locks the internal oscillator to every rising edge of the SYNC pin. If the SYNC input is removed at any time during normal operation the part will simply change switching frequency back to the oscillator frequency programmed by the R_T resistor. This injection lock method avoids the possible issues from a PLL method which can potentially cause a large drop in frequency if SYNC input is removed.

During soft-start the SYNC input is ignored until SS1 exceeds 2.2V. During soft-stop the SYNC input is completely ignored. If the SYNC input is to be used, recall that the programmable duty cycle clamp D_{VSEC} is dependent on the switching frequency of the part (see section Programming Duty Cycle Clamp). R_{IVSEC} should be reprogrammed by 1/x for an f_{SYNC}/f_{OSC} ratio of x.

$INTV_{CC}$ Regulator Bypassing and Operation

The $INTV_{CC}$ pin is the output of an internal linear regulator driven from V_{IN} and provides the supply for onboard gate drivers. The LT3752 $INTV_{CC}$ provides a regulated 7V supply for gate drivers AOUT, SOUT, OUT and HOUT. The LT3752-1 $INTV_{CC}$ provides a regulated 10V supply for gate drivers AOUT, SOUT and OUT. $INTV_{CC}$ should be bypassed with a 4.7µF low ESR, X7R or X5R ceramic capacitor to power ground to ensure stability and to provide enough charge for the gate drivers.

The $INTV_{CC}$ regulator has a minimum 35mA output current limit. This current limit should be considered when choosing the switching frequency and capacitance loading on each gate driver. Average current load on the $INTV_{CC}$ pin for a single gate driver driving an external MOSFET is given as :

$$I_{INTVCC} = f_{OSC} \cdot Q_G$$

where:

f_{OSC} = controller switching frequency

Q_G = gate charge ($V_{GS} = INTV_{CC}$)

While the $INTV_{CC}$ 50mA output current limit is sufficient for LT3752/LT3752-1 applications, efficiency and internal power dissipation should also be considered. $INTV_{CC}$ can be externally overdriven by the housekeeping supply to improve efficiency, remove power dissipation from within the IC and provide more than 35mA output current capability. Any overdrive level should exceed the regulated $INTV_{CC}$ level but not exceed 16V.

In the case of a short-circuit fault from $INTV_{CC}$ to ground, each IC reduces the $INTV_{CC}$ output current limit to typically 23mA. The $INTV_{CC}$ regulator has an undervoltage lockout rising threshold, UVLO(+), which prevents gate driver switching until $INTV_{CC}$ reaches 4.75V (7V for LT3752-1) and maintains switching until $INTV_{CC}$ falls below a UVLO(–) threshold of 4.6V (6.8V for LT3752-1).

For V_{IN} levels close to or below the $INTV_{CC}$ regulated level, the $INTV_{CC}$ linear regulator may enter dropout. The resulting lower $INTV_{CC}$ level will still allow gate driver switching as long as $INTV_{CC}$ remains above $INTV_{CC}$ UVLO(–) levels. See the Typical Performance Characteristics section for $INTV_{CC}$ performance vs V_{IN} and load current.

HOUSEKEEPING CONTROLLER

The LT3752/LT3752-1 include an internal constant frequency, current mode, PWM controller for creating a housekeeping supply (see the Block Diagram and Figure 8). Connected as a flyback converter with multiple outputs, the housekeeping supply is able to efficiently provide bias to both primary and secondary ICs. It eliminates the need to generate bias supplies from auxiliary windings in the main forward transformer, reducing the complexity, size and cost of the transformer.

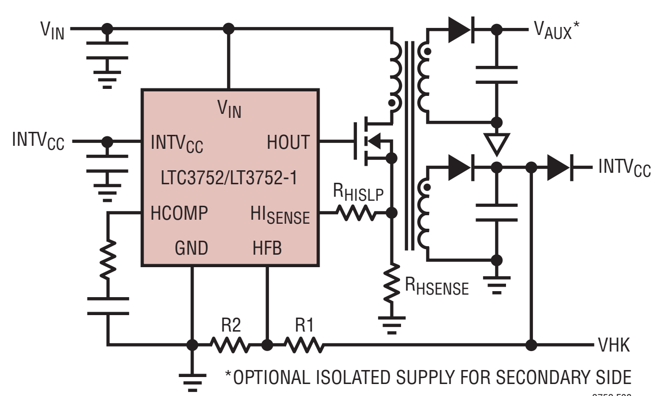

Figure 8. Housekeeping Supply

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Integrating the housekeeping controller saves cost and space and allows switching frequency to be inherently synchronized to the main forward converter.

The housekeeping supply can be used to overdrive the $INTV_{CC}$ pin to take power outside of the part, improve efficiency, provide more drive current and optimize the $INTV_{CC}$ level. It can also be used as a bootstrap bias to the V_{IN} pin as described in the section LT3752-1 Part Start-Up. The housekeeping supply also allows bias to any secondary side IC before the main forward converter starts switching. This removes the need for external start-up circuitry on the secondary side. Alternative methods involve powering secondary side ICs directly from the output voltage of the forward converter. This can cause issues depending on the minimum and maximum allowed input voltages for each IC.

Housekeeping: Operation

The LT3752/LT3752-1 housekeeping controller operation is best described by referring to the Block Diagram and Figure 8. The housekeeping controller uses a ±0.7A gate driver at HOUT to control an external N-channel MOSFET. When current in the primary winding of the flyback transformer exceeds a level commanded by HCOMP and sensed at the HI_{SENSE} pin, the duty cycle of the HOUT is terminated. Stored energy in the transformer is delivered to the output during the off time of HOUT. The housekeeping output voltage is programmed using a resistor divider to the HFB pin. A transconductance amplifier monitors the error signal between HFB pin and a 1.0V reference to control HCOMP level and hence peak switch current. A simple RC network from HCOMP pin to ground provides compensation. Overcurrent protection exists for the external switch when 98mV is sensed at the HI_{SENSE} pin. This causes a low power hiccup mode (repeated retry cycles' of shutdown followed by soft-start) until the overcurrent condition is removed.

Housekeeping: Soft-Start/Shutdown

During start-up of the LT3752/LT3752-1, the housekeeping controller has a built-in soft-start of approximately 2.2ms. The time will vary depending on the HCOMP level needed to achieve regulation. The housekeeping controller is shut down and the internal soft-start capacitor is discharged for any of the following conditions (typical values):

(1) $UVLO\_V_{SEC}$ < 1.25V (and SS1 < 0.15V) :Soft-Stop Shutdown
(2) $UVLO\_V_{SEC}$ < 0.4V :Micropower Shutdown
(3) OVLO > 1.250V :System Input OVLO
(4) HI_{SENSE} > 98mV :Housekeeping Overcurrent
(5) $INTV_{CC}$ < X, > 16.5V :$INTV_{CC}$ UVLO, OVLO
(6) T_J > 170°C :Thermal Shutdown
(7) V_{IN} < Y :V_{IN} Pin UVLO

(X = 4.6V, Y = 5.5V for LT3752)

(X = 6.8V, Y = 7.6V for LT3752-1)

Housekeeping: Programming Output Voltage

The output voltage, V_{HK}, of the housekeeping controller is programmed using a resistor divider between V_{HK} and the HFB pin (Figure 8) using the equation:

$$V_{HK} = 1V \bullet \left(1 + \frac{R1}{R2}\right)$$

The HFB pin bias current is typically 85nA.

Housekeeping: Programming Cycle-by-Cycle Peak Inductor Current and Slope Compensation

The housekeeping controller limits cycle-by-cycle peak current in the external switch and primary winding of the flyback transformer by sensing voltage at a resistor ($R_{HISENSE}$) connected in the source of the external N-channel MOSFET (Figure 8). This sense voltage is compared to a sense threshold at the HI_{SENSE} pin, controlled by HCOMP with an upper limit of 79mV. Since there is only one sense line from the positive terminal of the sense resistor, any parasitic resistance in ground side will increase its effective value and reduce available peak switch current. For operation in continuous mode and above 50% duty cycle, required slope compensation can be programmed by adding a resistor R_{HISLP} in series with the HI_{SENSE} pin. A ramped current always flows out of the HI_{SENSE} pin. The current starts from 2µA at 0% duty cycle and ramps to 52µA at 100% duty cycle. Minimize capacitance on this pin.