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Triple Output LED Driver Controller

FEATURES

- **Three Independent LED Driver Channels**
- **Wide Input Voltage Range: 2.5V to 40V**
- **V_{IN} Transient Ride-Through Up to 60V**
- **Rail-to-Rail LED Current Sense: 0V to 100V**
- **3000:1 PWM Dimming**
- **TG Drivers for PMOS LED Disconnection**
- Operates in Boost, Buck Mode, Buck-Boost Mode, SEPIC or Flyback Topology
- Open-LED Protection
- Short-Circuit Protected Boost Capable
- Fault Flags for Independent Channels
- Programmable V_{IN} Undervoltage and Overvoltage Lockout
- Adjustable Switching Frequency: 100kHz to 1MHz
- Synchronizeable to an External Clock
- CTRL Pins Provide Analog Dimming
- Programmable Soft-Start
- 52-Lead QFN Package

APPLICATIONS

- Automotive and Industrial Lighting
- RGB Lighting
- Billboards and Large Displays

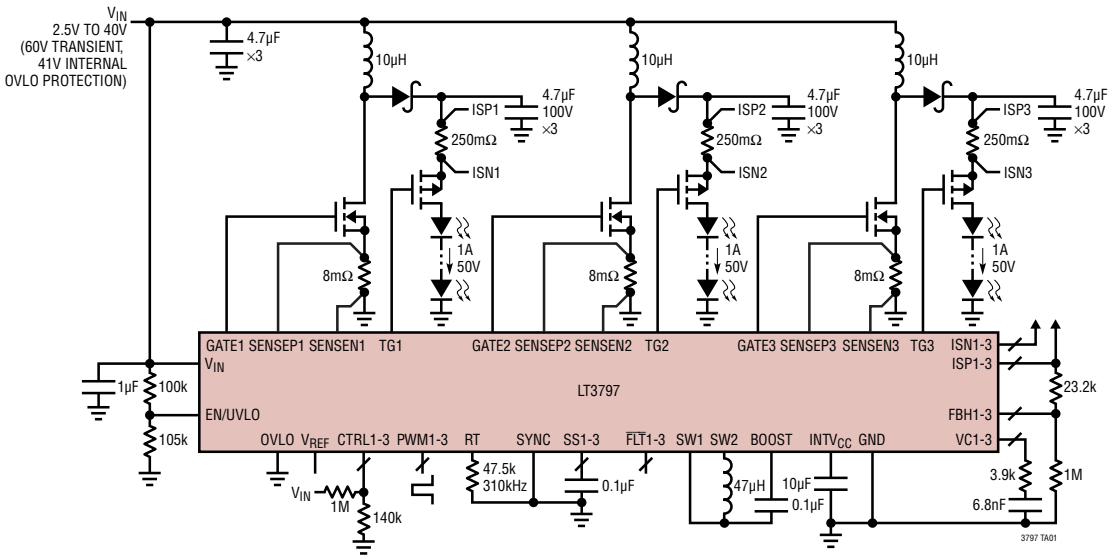
DESCRIPTION

The LT®3797 is a triple output DC/DC controller designed to drive three strings of LEDs. The fixed frequency, current mode architecture results in stable operation over a wide range of supply and output voltages. The LT3797 includes an integrated DC/DC converter to produce a regulated 7.5V supply for the N-channel MOSFET gate drivers of the three channels. This high efficiency converter enables the part to operate from a wide input voltage range from 2.5V to 40V.

The LT3797 is designed so that each converter can use the most suitable configuration to drive its LED load, whether step-up, step-down or a combination. Two key features enable this flexibility: first the LT3797 can sense output current at the high side of the LED string; and second, the voltage feedback pin, FBH, is referred to the ISP current sensing input. The CTRL inputs provide output current analog dimming capability. The TG drivers level shift the PWM signals to drive the gates of external LED-disconnect P-channel MOSFETs, allowing high PWM dimming range, and providing LED overcurrent protection and short-circuit protected boost capability.

TYPICAL APPLICATION

Triple Boost LED Driver

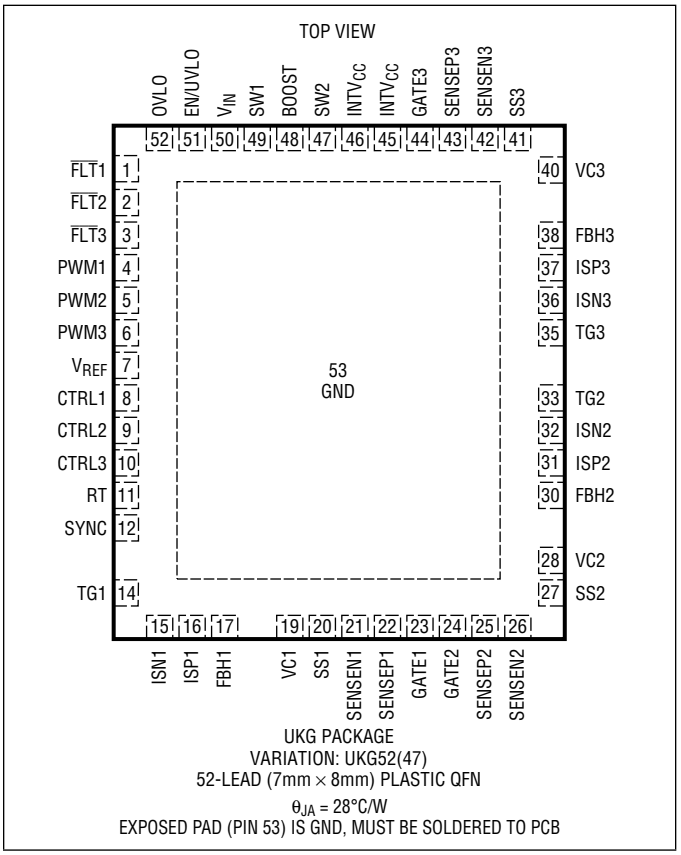


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, EN/UVLO.....60V
$INTV_{CC}$, SYNC, OVLO, PWM1, PWM2, PWM3.....8V
ISN1.....ISP1-1.5V, 100V
ISN2.....ISP2-1.5V, 100V
ISN3.....ISP3-1.5V, 100V
FBH1.....ISP1 ±6V, 100V
FBH2.....ISP2 ±6V, 100V
FBH3.....ISP3 ±6V, 100V
VC1, VC2, VC3, V_{REF}, SS1, SS2, SS3.....3V
CTRL1, CTRL2, CTRL3, $\overline{FLT1}$, $\overline{FLT2}$, $\overline{FLT3}$.....12V
RT.....1.5V
SENSEP1, SENSEP2, SENSEP3, SENSEN1, SENSEN2, SENSEN3,.....±0.3V
SW1, SW2, BOOST, TG1, TG2, TG3, GATE1, GATE2, GATE3 .....(Note 2)
Operating Ambient Temperature Range (Note 3).....–40 to 125°C
Maximum Junction Temperature .....125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UKG PACKAGE
VARIATION: UKG52(47)
52-LEAD (7mm × 8mm) PLASTIC QFN
θ_{JA} = 28°C/W
EXPOSED PAD (PIN 53) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT3797#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3797EUKG#PBF	LT3797EUKG#TRPBF	LT3797UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C
LT3797IUKG#PBF	LT3797IUKG#TRPBF	LT3797UKG	52-Lead (7mm × 8mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; EN/UVLO = 24V; CTRL1, CTRL2, CTRL3, PWM1, PWM2, PWM3 = 2V; SENSEN1, SENSEN2, SENSEN3 = 0V, OVLO = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Minimum Operation Voltage		●			2.5	V
V_{IN} Overvoltage Lockout	Rising V_{IN} Falling Hysteresis	●	40	41 1	42.5	V V
V_{IN} Shutdown I_Q	EN/UVLO = 0V EN/UVLO = 1.15V			0.1	1 15	µA µA
V_{IN} Operating I_Q (Not Switching)	PWM1, PWM2, PWM3 = 0V, $INTV_{CC}$ = 8V			0.5	0.75	mA
$INTV_{CC}$ Operating I_Q (Not Switching)	PWM1, PWM2, PWM3 = 0V, $INTV_{CC}$ = 8V			2.4	3	mA
V_{REF} Voltage	0µA ≤ I_{VREF} ≤ 450µA, $INTV_{CC}$ = 8V	●	1.955	2.00	2.035	V
V_{REF} Line Regulation	2.5V ≤ V_{IN} ≤ 40V, $INTV_{CC}$ = 8V			0.001		%/V
SENSEP1-SENSEN1, SENSEP2-SENSEN2, SENSEP2-SENSEN2 Current Limit Threshold		●	100	110	120	mV
SENSEP1, SENSEP2, SENSEP3 Input Bias Current	Current Out of Pin, SENSEP1, SENSEP2, SENSEP3 = 0V			55		µA
SENSEN1, SENSEN2, SENSEN3 Input Bias Current	Current Out of Pin			210		µA
Integrated $INTV_{CC}$ Power Supply (Note 7)						
$INTV_{CC}$ Regulation Voltage		●	7.15	7.5	7.75	V
$INTV_{CC}$ Undervoltage Lockout Threshold	Falling $INTV_{CC}$ Hysteresis		5.15	5.25 0.4	5.4	V V
$INTV_{CC}$ Line Regulation ($\Delta V_{INTVCC}/\Delta V_{IN}$)	2.5V < V_{IN} < 40V			0.001	0.02	%
Error Amplifiers						
LED Current Sense Threshold (ISP1-ISN1, ISP2-ISN2, ISP3-ISN3)	ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V ISN1, ISN2, ISN3, FBH1, FBH2, FBH3 = 0V	● ●	243 238	250 250	257 272	mV mV
8/10th LED Current Sense Threshold (ISP1-ISN1, ISP2-ISN2, ISP3-ISN3)	CTRL1, CTRL2, CTRL3=1.1V, ISP1, ISP2, ISP3 = 48V CTRL1, CTRL2, CTRL3=1.1V, ISN1, ISN2, ISN3 = 0V	● ●	194.5 192	200 200	203.5 218	mV mV
1/10th LED Current Sense Threshold (ISP1-ISN1, ISP2-ISN2, ISP3-ISN3)	CTRL1, CTRL2, CTRL3=0.3V, ISP1, ISP2, ISP3 = 48V CTRL1, CTRL2, CTRL3=0.3V, ISN1, ISN2, ISN3 = 0V	● ●	17 15	25 25	29 34	mV mV
CTRL1, CTRL2, CTRL3 Range for Linear Current Sense Threshold Adjustment		●	0.2		1.2	V
CTRL1, CTRL2, CTRL3 Input Bias Current	Current Out of Pin, CTRL1, CTRL2, CTRL3 = 0.3V			50	100	nA
CTRL1, CTRL2, CTRL3 Idle Mode Threshold	Falling Hysteresis		135	150 20	170	mV mV
LED Current Sense Amplifier Input Common Mode Range (ISN1, ISN2, ISN3)		●	0		100	V
LED Overcurrent Protection Threshold (ISP1-ISN1, ISP2-ISN2, ISP3-ISN3)	ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V			1000		mV
ISP1, ISP2, ISP3 Input Bias Current (Active)	ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 0V			630 –100		µA nA
ISP1, ISP2, ISP3 Input Bias Current (Idle)	PWM1, PWM2, PWM3=0V , ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V			2		µA
	PWM1, PWM2, PWM3, ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 0V			–40		nA
ISN1, ISN2, ISN3 Input Bias Current (Active)	ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 0V			20 –100		µA nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; EN/UVLO = 24V; CTRL1, CTRL2, CTRL3, PWM1, PWM2, PWM3 = 2V; SENSEN1, SENSEN2, SENSEN3 = 0V, OVLO = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
ISN1, ISN2, ISN3 Input Bias Current (Idle)	PWM1, PWM2, PWM3=0V , ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V			0	1	µA
	PWM1, PWM2, PWM3, ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 0V			–20		nA
LED Current Sense Amplifier g_m	ISP1-ISN1, ISP2-ISN2, ISP3-ISN3 = 250mV			250		µS
FBH1, FBH2, FBH3 Regulation Voltage "FBH(REG)" (|ISP1-FBH1, ISP2-FBH2, ISP3-FBH3|)	ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V	●	1.225	1.250	1.275	V
FBH1, FBH2, FBH3 Pin Input Bias Current	ISP1-FBH1, ISP2-FBH2, ISP3-FBH3 = 1.25V ISP1-FBH1, ISP2-FBH2, ISP3-FBH3 = –1.25V		 2	40 2.4	100 3	nA µA
FBH1, FBH2, FBH3 Amplifier g_m	|ISP1-FBH1|, |ISP2-FBH2|, |ISP3-FBH3| = 1.25V			480		µS
FBH1, FBH2, FBH3 Open-LED Threshold (|ISP1-FBH1|, |ISP2-FBH2|, |ISP3-FBH3|) Voltage	Rising (Note 4) ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V		FBH(REG) – 0.07	FBH(REG) – 0.05	FBH(REG) – 0.04	V
	Hysteresis			20		mV
FBH1, FBH2, FBH3 Overvoltage Threshold (|ISP1-FBH1|, |ISP2-FBH2|, |ISP3-FBH3|) Voltage	Rising (Note 4) ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V		FBH(REG) + 0.05	FBH(REG) + 0.06	FBH(REG) + 0.085	V
	Hysteresis			25		mV
VC1, VC2, VC3 Output Impedance				10		MΩ
VC1, VC2, VC3 Standby Input Bias Current	PWM1, PWM2, PWM3 = 0V CTRL1, CTRL2, CTRL3 = 0V		–20 –20		20 20	nA nA
VC1, VC2, VC3 Current Mode Gain $-\Delta V_{VC}/\Delta V_{SENSE}$				4		V/V
VC1, VC2, VC3 Source Current	ISP1, ISP2, ISP3, ISN1, ISN2, ISN3, FBH1, FBH2, FBH3 = 48V, Current Out of Pin			10.5		µA
VC1, VC2, VC3 Sink Current	ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V, ISN1, ISN2, ISN3 = 47.7V			12		µA
	ISP1, ISP2, ISP3, ISN1, ISN2, ISN3 = 48V, FBH1, FBH2, FBH3 = 46.7V			32		µA
Oscillator						
Switching Frequency	R_T = 154kΩ R_T = 35.7kΩ R_T = 12.4kΩ	 ● 	95 375 950	100 400 1000	107 425 1050	kHz kHz kHz
RT Voltage				1.05		V
GATE1, GATE2, GATE3 Minimum Off-Time	C_{GATE} = 3300pF			200	270	ns
GATE1, GATE2, GATE3 Minimum On-Time	C_{GATE} = 3300pF			220	300	ns
SYNC Input Low		●			0.4	V
SYNC Input High		●	1.5			V
SYNC Resistance to GND				200		kΩ
Logic Inputs/Outputs						
EN/UVLO Threshold Voltage Falling		●	1.180	1.220	1.250	V
EN/UVLO Rising Hysteresis				20		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA				0.4	V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V	●	1.5	2	2.6	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.33V			40	100	nA
OVLO Pin Input Bias Current				20	100	nA
OVLO Threshold Voltage	Rising Hysteresis	●	1.225	1.250 125	1.275	V mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 24V; EN/UVLO = 24V; CTRL1, CTRL2, CTRL3, PWM1, PWM2, PWM3 = 2V; SENSEN1, SENSEN2, SENSEN3 = 0V, OVLO = 0V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PWM1, PWM2, PWM3 Input High Voltage		●		1.1	1.4	V
PWM1, PWM2, PWM3 Input Low Voltage		●	0.6	0.9		V
PWM1, PWM2, PWM3 Resistance to GND				200		kΩ
$\overline{FLT}$1, $\overline{FLT}$2, $\overline{FLT}$3 Output Low	$I_{\overline{FLT}}$ =1mA				300	mV
SS1, SS2, SS3 Sourcing Current	SS1, SS2, SS3 = 1V, Current Out of Pin			28		µA
SS1, SS2, SS3 Sinking Current	SS1, SS2, SS3 = 1V, OVLO =1.3V			2.8		µA
SS1, SS2, SS3 Soft-Start Reset Threshold	Falling, Measured on SS1, SS2, SS3 Hysteresis			160 30		mV mV
SS1, SS2, SS3 Fault Reset Threshold	Measured on SS1, SS2, SS3			1.7		V
NMOS Gate Drivers						
GATE1, GATE2, GATE3 Output Rise Time (t_r)	C_{GATE} = 3300pF (Note 5)			25		ns
GATE1, GATE2, GATE3 Output Fall Time (t_f)	C_{GATE} = 3300pF (Note 5)			25		ns
Gate Output Low (V_{OL})					0.1	V
Gate Output High (V_{OH})			$INTV_{CC}$ – 0.05			V
PMOS Gate Drivers						
TG1, TG2, TG3 Turn-On Time	C_{TG} = 1000pF, ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V (Note 6)			200		ns
TG1, TG2, TG3 Turn-Off Time	C_{TG} = 1000pF, ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V (Note 6)			70		ns
PMOS Gate On Voltage (ISP1-TG1, ISP2-TG2, ISP3-TG3)	ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V			6.5		V
PMOS Gate Off Voltage (ISP1-TG1, ISP2-TG2, ISP3-TG3)	ISP1, ISP2, ISP3, FBH1, FBH2, FBH3 = 48V				0.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not apply a positive or negative voltage or current source to SW1, SW2, GATE1, GATE2, GATE3, TG1, TG2, TG3 pins, otherwise permanent damage may occur.

Note 3: The LT3797E is guaranteed to meet performance specifications from the 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT3797I is guaranteed over the full –40°C to 125°C operating junction temperature range.

Note 4: FBH(REG) denotes the regulation voltage (|ISP-FBH|) of the corresponding FBH pin.

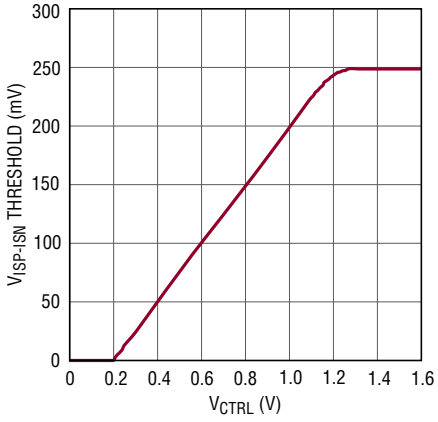
Note 5: Rise and fall times are measured at 10% and 90% levels.

Note 6: Gate turn-on/turn-off time is measured from 50% level of PWM voltage to 90% level of gate on/off voltage.

Note 7: The $INTV_{CC}$ regulation voltage is tested in an open loop. Closed loop operation is guaranteed by design and process controls.

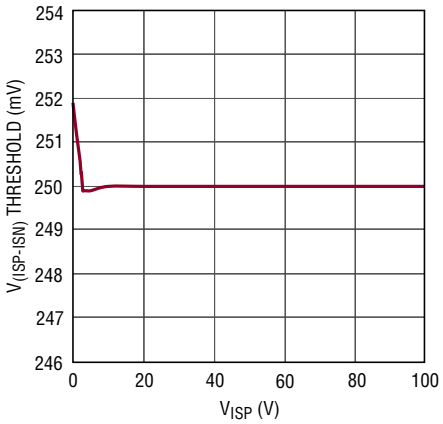
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

$V_{ISP-ISN}$ Threshold vs V_{CTRL}



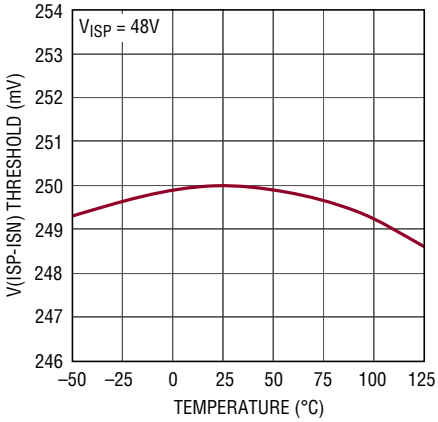
3797 G01

$V_{ISP-ISN}$ Threshold vs V_{ISP}



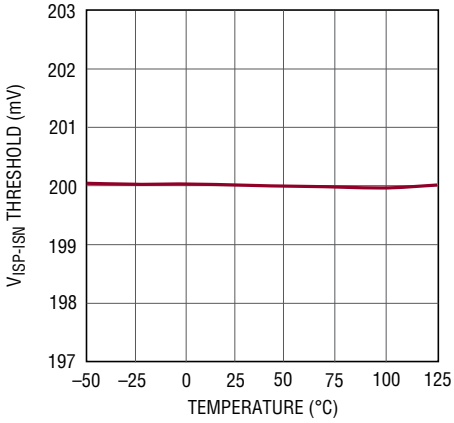
3797 G02

$V_{ISP-ISN}$ Full-Scale Threshold vs Temperature



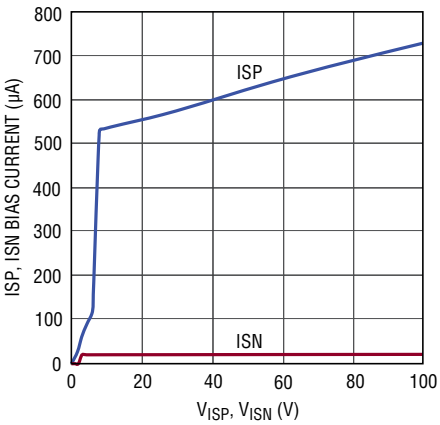
3797 G03

$V_{ISP-ISN}$ Threshold at CTRL = 0.7V vs Temperature



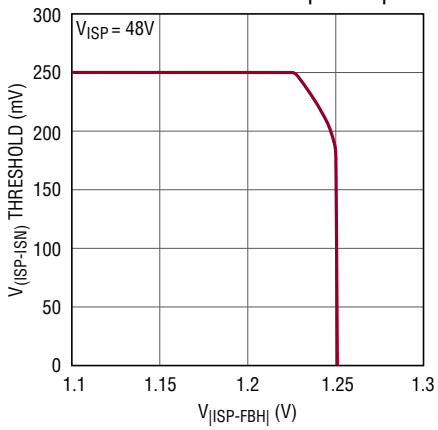
3797 F04

ISP/ISN Input Bias Current vs V_{ISP}, V_{ISN}



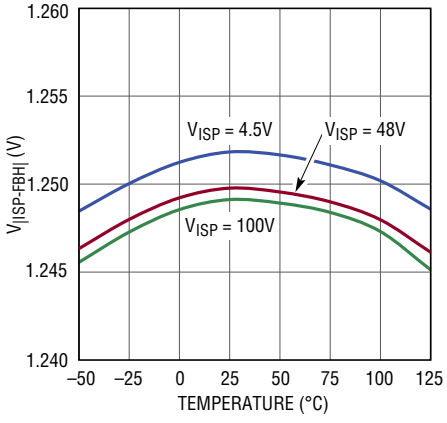
3797 G05

$V_{ISP-ISN}$ Threshold vs $V_{|ISP-FBH|}$



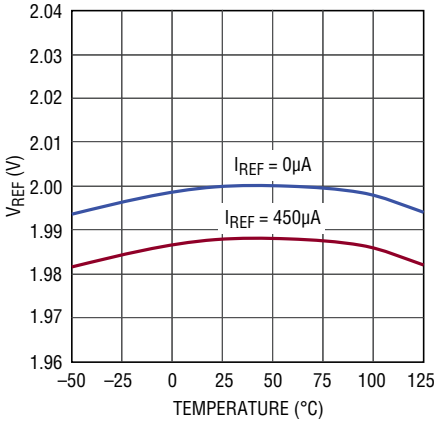
3797 G06

|ISP-FBH| Regulation Voltage vs Temperature, V_{ISP}



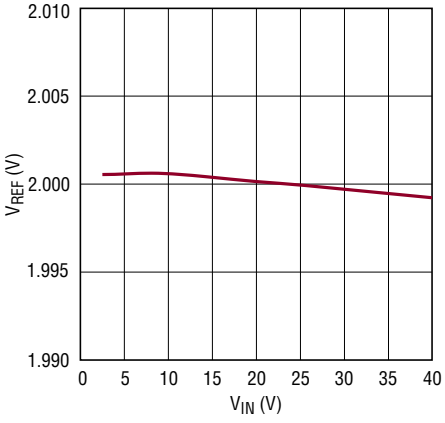
3797 G07

V_{REF} Voltage vs Temperature



3797 G08

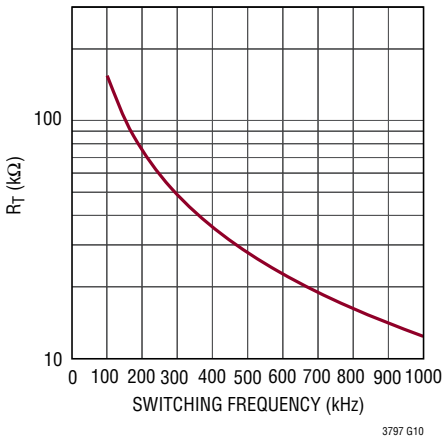
V_{REF} Voltage vs V_{IN}



3797 G09

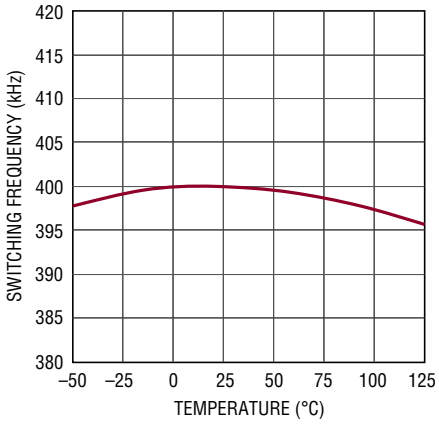
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

R_T vs Switching Frequency



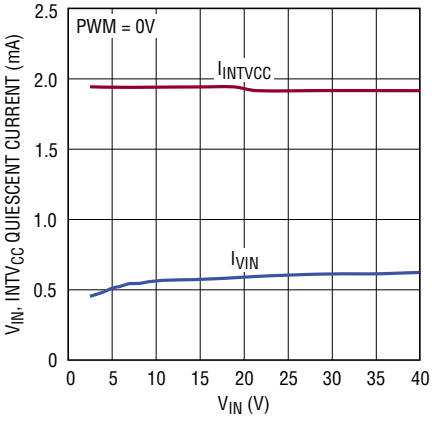
3797 G10

Switching Frequency vs Temperature



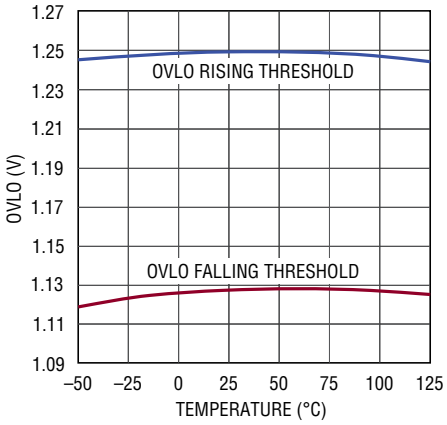
3797 G11

V_{IN}, $INTV_{CC}$ Quiescent Current vs V_{IN}



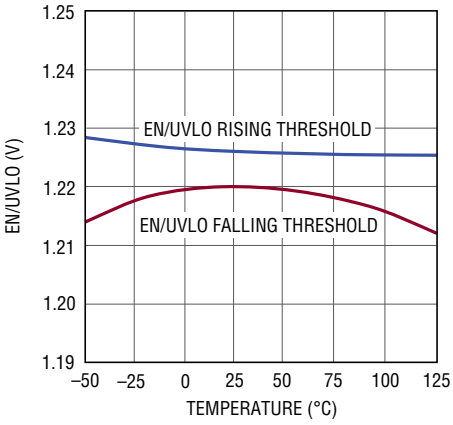
3797 G12

OVLO Threshold vs Temperature



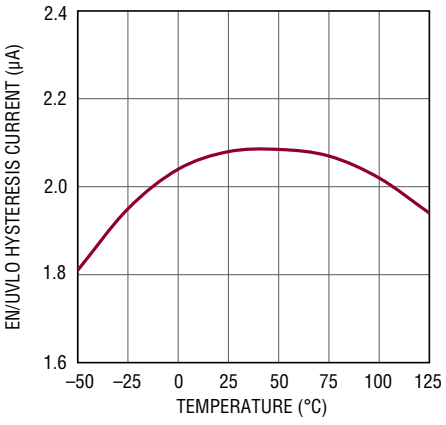
3797 G13

EN/UVLO Falling/Rising Threshold vs Temperature



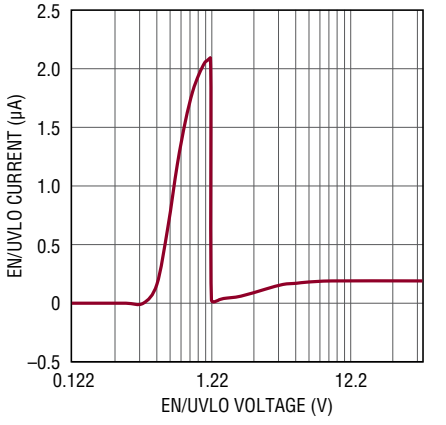
3797 G14

EN/UVLO Hysteresis Current vs Temperature



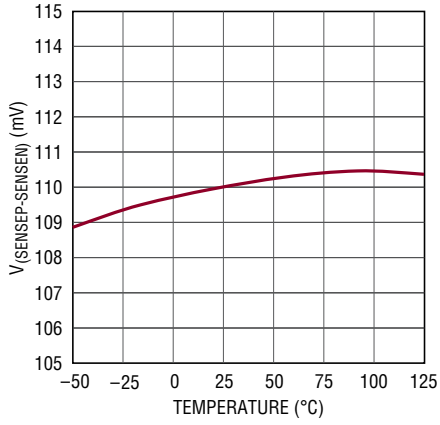
3797 G15

EN/UVLO Current vs Voltage



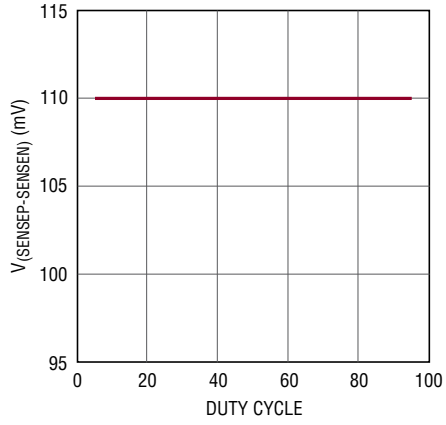
3797 G16

SENSE Current Limit Threshold vs Temperature



3797 G17

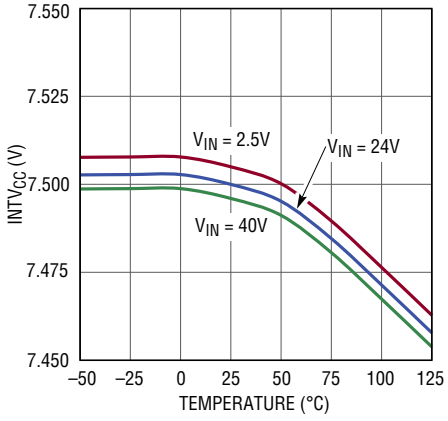
SENSE Current Limit Threshold vs Duty Cycle



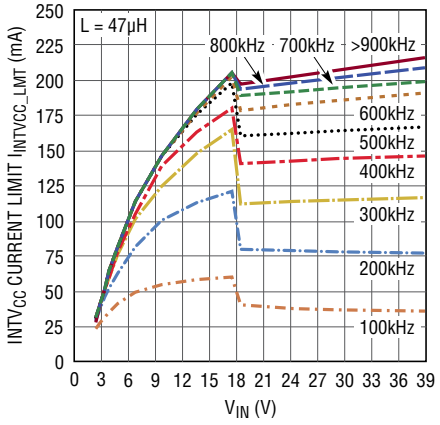
3797 G18

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

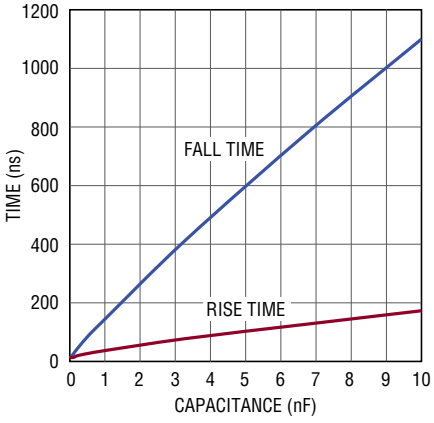
$INTV_{CC}$ vs Temperature, V_{IN}



$INTV_{CC}$ Current Limit vs V_{IN}, f_{SW}



Top Gate (PMOS) Rise/Fall Time vs Capacitance



PIN FUNCTIONS

$\overline{FLT1}$, $\overline{FLT2}$, $\overline{FLT3}$ (Pins 1, 2, 3): Open-Collector Pull-Downs on $\overline{FLT}$ Pins Report The Fault Conditions:

1. V_{IN} > 41V (typical)
2. Overtemperature (T_J > 165°C)
3. $INTV_{CC}$ < 5.2V (typical)
4. OVLO > 1.25V (typical)
5. LED Overcurrent
6. Open LED
7. Output Overvoltage

PWM1, PWM2, PWM3 (Pins 4, 5, 6): Pulse Width Modulated Input Pins. Signal low causes the respective converter to go into idle mode which means it stops switching, the TG pin transitions high, the quiescent currents are reduced, and the VC becomes high impedance. If not used, connect to the REF pin.

V_{REF} (Pin 7): Reference Output Pin. Can supply up to 450µA. This pin drives a resistor divider for the CTRL1, CTRL2, CTRL3 pins, either for analog dimming or for temperature limit/compensation of LED loads. The normal output voltage is 2V.

CTRL1, CTRL2, CTRL3 (Pins 8, 9, 10): Current Sense Threshold Adjustment Pins. Sets voltage across external sense resistor between ISP and ISN pins of the respective converter:

$V_{ISP-ISN}$ = 0V, when V_{CTRL} < 0.2V

$V_{ISP-ISN}$ = (V_{CTRL} – 0.2V)/4, when 0.2V < V_{CTRL} < 1.2V

$V_{ISP-ISN}$ = 250mV, when V_{CTRL} >1.2V

Connect CTRL pins to V_{REF} for the 250mV default threshold. When V_{CTRL} < 150mV (typical), the respective converter goes into idle mode, which is the same as PWM pin being pulled low. Do not leave these pins open.

RT (Pin 11): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND. Do not leave the RT pin open.

SYNC (Pin 12): The SYNC pin is used to synchronize the internal oscillator to an external logic-level signal. The R_T resistor should be chosen to program an internal switching frequency 20% slower than the SYNC pulse frequency. Gate turn-on occurs at a 0.2µs (typical) delay after the rising edge of SYNC. Tie SYNC to GND if not used.

PIN FUNCTIONS

TG1, TG2, TG3 (Pins 14, 33, 35): Top Gate Driver Output Pins for Driving LED Loads Disconnect P-Channel MOSFETs (PMOSs). One for each channel. An inverted PWM signal drives an external PMOS gate of the respective converter between V_{ISP} and (V_{ISP} – 6.5V). Leave TG pins unconnected if not used.

ISN1, ISN2, ISN3 (Pins 15, 32, 36): Connection Points for the Negative Terminals of the Current Feedback Resistors.

ISP1, ISP2, ISP3 (Pins 16, 31, 37): Connection Points for the Positive Terminals of the Current Feedback Resistors. Also serves as positive rails for TG pin drivers and the reference point for FBH.

FBH1, FBH2, FBH3 (Pins 17, 30, 38): Voltage Loop Feedback Pins. The output feedback voltage V_{FB} is measured between the ISP pin and the FBH pin (absolute value): V_{FB} = |ISP – FBH|. The FBH pin is intended for constant-voltage regulation or for LED protection/open-LED detection for each channel. In an open-LED event, the internal amplifier with output VC regulates V_{FB} to 1.25V (typical) through the respective converter. If V_{FB} is above the overvoltage threshold (typical 1.3V), the TG pin of the same channel is driven high to disconnect the external PMOS to protect the LEDs from an overvoltage event. Either open-LED or overvoltage event signals a fault condition. Do not leave the FBH pins open. It requires ISP to be no less than 4.5V to maintain an accurate V_{FB1} voltage sense. If ISP falls below 4.5V, the voltage regulation is deactivated and the ISP-ISN current regulation dominates regardless of the |ISP-FBH| value. If not used, connect the FBH pin to the ISP pin of the same channel.

VC1, VC2, VC3 (Pins 19, 28, 40): Error Amplifier Compensation Pins. Connect a series RC from each VC pin to GND. In each channel, the VC pin is high impedance when the PWM pin is low, or the CTRL pin is below 150mV. This feature allows the VC pin to store the demand current state variable for the next PWM or CTRL high transition.

SS1, SS2, SS3 (Pins 20, 27, 41): Soft-Start Pins. Each SS pin modulates compensation VC pin voltage of the respective channel. Each of the soft-start intervals is set with an external capacitor.

SENSEN1, SENSEN2, SENSEN3 (Pins 21, 26, 42): The Negative Current Sense Inputs for the Control Loops. Kelvin connect the SENSEN pin to the negative terminal of the switch current sense resistor (which connects to the GND plane) of the respective converter.

SENSEP1, SENSEP2, SENSEP3 (Pins 22, 25, 43): The Positive Current Sense Inputs for the Control Loops. Kelvin connect the SENSEP pin to the positive terminal of the switch current sense resistor in the source of the external N-channel MOSFET (NMOS) switch of the respective converter.

GATE1, GATE2, GATE3 (Pins 23, 24, 44): N-Channel MOSFET Gate Driver Outputs. Switch between $INTV_{CC}$ and GND. Driven to GND during shutdown, fault or idle states.

$INTV_{CC}$ (Pins 45, 46): $INTV_{CC}$ pins are the integrated power supply output voltage nodes that provide supply for control circuits and NMOS gate drivers. The two $INTV_{CC}$ pins are internally shorted. Must be bypassed with a 10µF ceramic capacitor placed close to the pins.

SW2 (Pin 47): Integrated Power Supply Switch Node. Connect this pin to one side of the integrated power supply inductor.

BOOST (Pin 48): Connect this pin to SW1 pin through a 0.1µF ceramic capacitor.

SW1 (Pin 49): Integrated Power Supply Switch Node. Connect this pin to the other side of the integrated power supply inductor, and to the BOOST pin with a 0.1µF ceramic capacitor.

V_{IN} (Pin 50): Input Supply Pin. If V_{IN} is over 41V (typical), the integrated $INTV_{CC}$ power supply is turned off. All three channels are also turned off (including pulling the GATE pins to GND and TG pins to ISP) and the soft-starts are reset. Must be locally bypassed with low ESR capacitors placed close to the pin.

PIN FUNCTIONS

EN/UVLO (Pin 51): Enable and Undervoltage Lockout Pin. An accurate 1.22V falling threshold with externally programmable hysteresis detects when power is OK to enable the integrated $INTV_{CC}$ power supply and each channel switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 2µA pull-down current. Above the 1.24V (typical) rising threshold (but below 2.5V), EN/UVLO input bias current is sub-µA. Below the 1.22V (typical) falling threshold, a 2µA pull-down current is enabled so the user can define the hysteresis with the external resistor selection. An undervoltage condition turns off the integrated $INTV_{CC}$ power supply and all the three channels and resets the soft-starts. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

OVLO (Pin 52): Overvoltage Lockout Pin. An accurate 1.25V rising threshold with 125mV hysteresis detects an overvoltage condition. An overvoltage condition turns off all three channels (including pulling the GATE pins to GND and TG pins to ISP) and resets the soft-starts. Tie OVLO to GND if not used.

GND (Exposed Pad Pin 53): Ground. Solder the exposed pad directly to ground plane.

BLOCK DIAGRAM

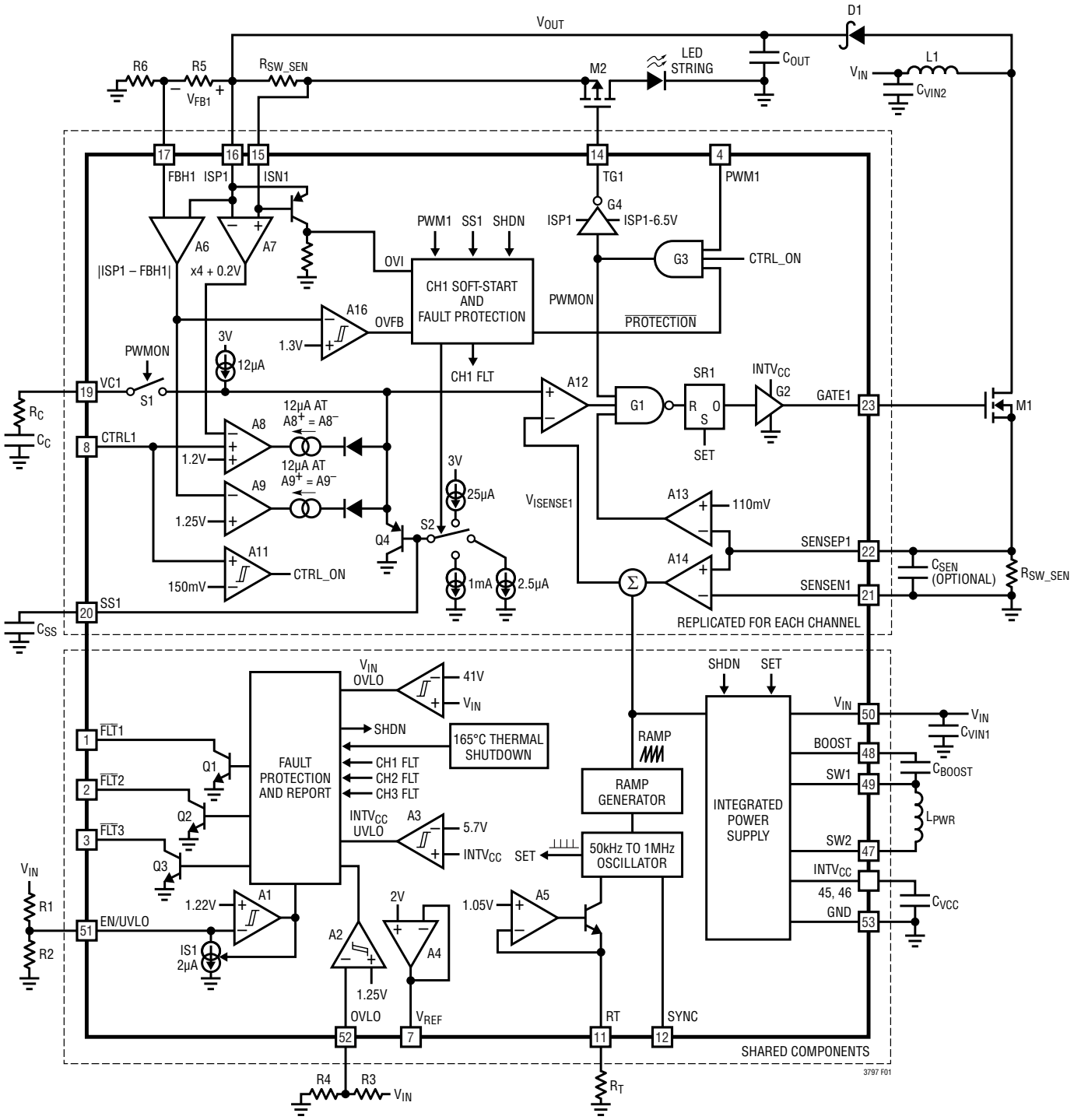


Figure 1. LT3797 Block Diagram Working in Boost Configuration (for Simplicity, Only Channel 1 Is Shown)

OPERATION

The LT3797 uses a fixed frequency, current mode control scheme to provide excellent line and load regulation. It contains three independent switching regulators. Operation can be best understood by referring to the Block Diagram in Figure 1. The oscillator, internal power supply etc., are shared among the three converters. The LED current control circuitry, gate drivers etc., are replicated for each of the three converters. For simplicity, Figure 1 shows the shared circuits and the channel specific circuits for converter 1.

The LED current regulation can be understood by following the operation of converter 1. The start of each oscillator cycle sets the SR latch SR1 and turns on the external power MOSFET switch M1 through gate driver G2 (the three converters share the same oscillator, which means if all the three channels are enabled the GATE pins of all the three channels transition high at the same instant). The switch current flows through the external current sensing resistor R_{SW_SEN1} and generates a voltage proportional to the switch current. This current sense voltage (amplified by A14) is added to a stabilizing slope compensation ramp and the resulting sum $V_{ISENSE1}$ is fed into the negative terminal of the PWM comparator A12. The current in the external inductor L1 increases steadily during the time the switch is on. When $V_{ISENSE1}$ exceeds the level at the negative input of A12 (VC1), SR1 is reset, turning off the power switch. During the switch-off phase, L1 current decreases.

Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current in the LED string. The VC1 voltage is set by the error amplifier A8 and is an amplified version of the difference between the LED current sense voltage, measured between ISP1 and ISN1, and the target difference voltage set by the CTRL1 pin. In this manner, the error amplifier sets the correct switch peak current level to keep the LED current in regulation.

The LT3797 has a switch current limit function. The switch current sense signal is input to the current limit comparator A13. If the current sense voltage is higher than the sense current limit threshold, $V_{SENSE(MAX)}$ (typical 110mV), A13 will reset SR1 and turn off M1 immediately.

The LT3797 provides the constant voltage regulation mode to allow the users to accurately program the output regulation voltage in an open-LED event. In voltage regulation mode, the operation is similar to that described above, except the VC1 voltage is set by A9 and is an amplified version of the difference between the internal reference of 1.25V (typical) and the output feedback voltage, V_{FB1}, which is measured between ISP1 and FBH1 (the absolute value):

$$V_{FB1} = |ISP1\text{-}FBH1|$$

The LED current sense feedback interacts with the FBH1 voltage feedback so that the sense voltage between ISP1 and ISN1 does not exceed the threshold set by the CTRL1 pin, and V_{FB1} does not exceed 1.25V (typical).

For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions, the appropriate loop is dominant. To deactivate the voltage loop entirely, FBH1 can be connected to ISP1. To deactivate the LED current loop entirely, the ISP1 and ISN1 should be tied together and the CTRL1 input tied to V_{REF}.

It requires ISP to be no less than 4.5V to maintain an accurate V_{FB1} voltage sense. If ISP falls below 4.5V, the voltage regulation is deactivated and the current regulation dominates regardless of the |ISP1-FBH1| value.

Two LED driver specific functions featured on the LT3797 are controlled by the voltage feedback pin FBH1. First, when the V_{FB1} exceeds a voltage 50mV lower (–4%) than the V_{FB1} regulation voltage (typical 1.25V), it indicates that the LED may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. $\overline{FLT}$1 is pulled low to report a fault condition. Second, when V_{FB1} exceeds the V_{FB1} regulation voltage by 60mV (5% typical), it indicates an output overvoltage fault. In this condition, TG1 pin is driven high by G3 and G4, turning off the external PMOS M2. This action disconnects the LED load from the power path, preventing excessive current from damaging the LEDs. $\overline{FLT}$1 is kept low to report the fault condition.

APPLICATIONS INFORMATION

Switching Frequency and Synchronization

The RT frequency adjust pin allows the user to program the switching frequency (f_{SW}) from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives higher efficiency, achieves higher maximum duty cycle or lower minimum duty cycle at the cost of larger external component size. An external resistor from the RT pin to GND is required—do not leave this pin open. For an appropriate R_T resistor value see Table 1.

Table 1. Switching Frequency (f_{SW}) vs R_T Value

f_{SW} (kHz)	R_T (kΩ)	f_{SW} (kHz)	R_T (kΩ)
100	154	600	22.6
150	102	650	20.5
200	75.0	700	17.4
250	59.0	750	19.1
300	48.7	800	16.2
350	41.2	850	15.0
400	35.7	900	14.0
450	31.6	950	13.3
500	28.0	1000	12.4
550	24.9		

The operating frequency of the LT3797 can be synchronized to an external clock source. By providing a digital clock signal into the SYNC pin, the LT3797 will operate at the SYNC clock frequency. If this feature is used, an R_T resistor should be chosen to program a switching frequency 20% slower than SYNC pulse frequency. Tie the SYNC pin to GND if this feature is not used.

Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The minimum duty cycle of the switch is limited by the fixed minimum on-time (200ns maximum) and the switching frequency (f_{SW}). The maximum duty cycle of the switch is limited by the fixed minimum off-time (200ns maximum) and f_{SW}. The following equations express the minimum/maximum duty cycle:

Minimum Duty Cycle = 200ns • f_{SW}

Maximum Duty Cycle = 1 – 200ns • f_{SW}

Besides the limitation by the minimum off-time, it is also recommended to choose the maximum duty cycle below 95%.

PWM Dimming Control

The LED of each channel can be dimmed with pulse width modulation using the PWM pin. Figure 1 shows the channel 1 driver. If the PWM1 pin is pulled high, M2 is turned on by G3 and G4. Converter 1 operates normally. G4 limits ISP1-TG1 to 6.5V to protect the gate of M2. If the PWM1 pin is pulled low, the external NMOS M1 is turned off through G1 etc, and converter 1 stops operating. M2 is turned off through the TG1 pin, disconnecting LED1 and stopping current drawing from output capacitor, C_{OUT}. The VC1 pin is also disconnected from the internal circuitry through S1. The capacitors C_C and C_{OUT} store the state of the LED string current until PWM1 is pulled up again. This leads to a highly linear relationship between PWM duty cycle and output light (brightness), and allows for a large and accurate dimming range. The PWM dimming range can be maximized by using the PWM pin for dimming and the CTRL pin for linearly adjusting the current sense threshold.

In the applications where the operation frequency of the LT3797 is synchronized to an external clock source applied to the SYNC pin, it is recommended to synchronize the rising edge of the external clock and the rising edge of the PWM signal of each of the three channels, as shown in Figure 2.

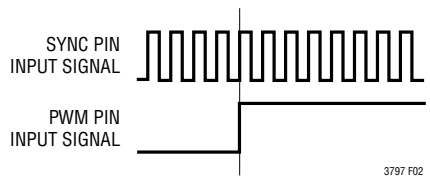


Figure 2. Synchronize the SYNC Pin Input Signal and the PWM Pin Input Signal

APPLICATIONS INFORMATION

Besides analog dimming, the CTRL pin can also be used for PWM dimming control. Refer to Figure 1 for channel 1 operation. If CTRL1 falls below 150mV, the CTRL_ON signal is pulled low by comparator A11. Since CTRL_ON is connected to one of G3's inputs, channel 1 has the same operation as PWM1 being pulled low (such as disconnecting LED1 from C_{OUT} and disconnecting C_C from VC1, etc). Therefore, the CTRL pin can be used for a combination of linear and PWM dimming control if it is connected to a PWM signal whose low level is below 150mV and high level is between 0.2V and 1.3V. Connect the PWM pins to the V_{REF} pin if the CTRL pins are used for PWM dimming or no PWM dimming is used.

Do not use a low V_{TH} PMOS for LED disconnection. The PMOS with a minimum V_{TH} of –1V to –2V is recommended. In the applications where accurate PWM dimming is not required, the P-channel MOSFETs can be omitted to reduce cost. In these conditions, the TG pins should be left open.

Programming the LED Current

The LED current of each channel is programmed by connecting an external sense resistor, R_{LED_SEN}, in series with the LED load, and setting the voltage regulation threshold across R_{LED_SEN} using CTRL input. The ISP and ISN sense node traces should run parallel to each other to a Kelvin connection on the positive and negative terminals of R_{LED_SEN}. Typically, sensing of the current should be done at the top of the LED string. If this option is not available, then the current may be sensed at the bottom of the LED string. The CTRL pin should be tied to a voltage higher than 1.3V to get the full-scale 250mV (typical) threshold across the sense resistor. The CTRL pin can also be used to dim the LED current from full scale to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the CTRL pin voltage is less than 1.1V and higher than 0.2V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 200mV}{R_{LED\_SEN} \bullet 4}$$

When the CTRL pin voltage is between 1.1V and 1.3V the LED current varies with CTRL, but departs from the equation above by an increasing amount as CTRL voltage increases. Ultimately, above CTRL = 1.3V the LED current no longer varies with CTRL. The typical (ISP-ISN) threshold vs CTRL voltage when CTRL is close to 1.2V is listed in Table 2.

Table 2. (ISP-ISN) Threshold vs CTRL When CTRL Is Close to 1.2V

V_{CRTL} (V)	(ISP-ISN) THRESHOLD (mV)
1.1	225
1.15	236
1.2	244.5
1.25	248.5
1.3	250

When CTRL is higher than 1.3V, the LED current is regulated to:

$$I_{LED} = \frac{250mV}{R_{LED\_SEN}}$$

The LED current is regulated to 0A when CTRL is lower than 200mV (typical).

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and limit peak switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor. Some level of ripple signal is acceptable: the compensation capacitor on the VC pin filters the signal so the average difference between ISP and ISN is regulated to the user-programmed value. Ripple voltage amplitude (peak-to-peak) in excess of 50mV should not cause misoperation, but may lead to noticeable offset between the average value and the user-programmed value.

APPLICATIONS INFORMATION

Programming Output Regulation Voltage for the Open-LED Event

The output voltage of each channel in the open-LED event can be programmed by selecting two external sense resistors. Figure 3 shows the sense resistor connection of channel 1. In the open-LED event, V_{FB1} is regulated to 1.25V, therefore the output regulation voltage can be set according to the following equation:

$$V_{OUT} = 1.25V \bullet \frac{R5+R6}{R5}$$

Since the output voltage is directly measured between ISP1 and LED1⁻, the Figure 3 approach works well for the converter topologies where LED1⁻ is connected to GND (such as boost, SEPIC, flyback), as well as the topologies where LED1⁻ is connected to an inductor (such as buck mode, buck-boost mode LED drivers).

Typically, the current sense resistor R_{LED_SEN1} and disconnect PMOS M2 are connected to the top of the LED string (LED1⁺), as shown in Figure 3. If this option is not available (for example some multi-string LED modules are built with a common anode configuration), then the current may be sensed at the bottom of the LED string as shown in Figure 4. In this configuration, the FBH pin draws 2µA (typical) current. Therefore, the output regulation voltage in the open-LED event can be set according to the following equation:

$$V_{OUT} = 1.25V \bullet \frac{R5+R6}{R5} + 2\mu A \bullet R6$$

Under normal operating conditions, the LED current regulation loop is dominant. Therefore, the output regulation voltage (V_{OUT}) in the open-LED event should be programmed so that V_{FB1} (V_{FB1} = |ISP1-FBH1|) should never exceed 1.1V when LED1 is connected. The only way for V_{FB1} to be within 50mV of the regulation voltage (1.25V) is for an open-LED event to occur.

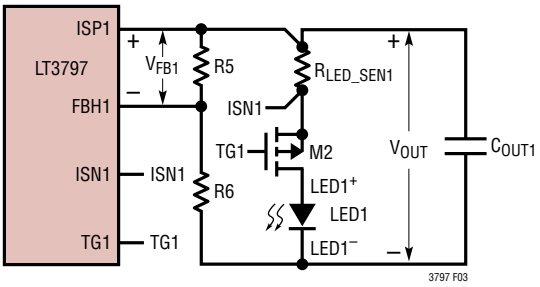


Figure 3. Output Voltage Sense Resistor Connection

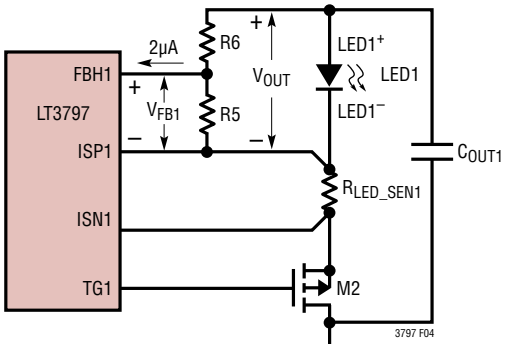


Figure 4. Output Voltage Sense Resistor Connection When R_{LED_SEN1} and M2 Are Connected to the Bottom of the LED String

Programming Enable and Undervoltage Lockout with the EN/UVLO Pin

EN/UVLO pin controls whether the LT3797 is enabled or is in shutdown state. As shown in Figure 1, a 1.22V reference, a comparator, A1, and a controllable current source, IS1, allow the user to accurately program the supply voltage at which the IC turns on and off. The falling value can be accurately set by the resistor divider R1 and R2. When EN/UVLO is above 0.4V and below the 1.22V threshold, the small pull-down current source, IS1 (typical 2µA), is active. The purpose of this current is to allow the user to program the rising hysteresis. The falling threshold voltage and rising threshold voltage can be calculated by the following equations:

$$V_{IN(FALLING)} = 1.22V \bullet \frac{R1+R2}{R2}$$

$$V_{IN(RISING)} = V_{IN(FALLING)} + 2\mu A \bullet R1$$

APPLICATIONS INFORMATION

For applications where the EN/UVLO pin is to be used only as a logic input, the EN/UVLO pin can be connected directly to the input voltage, V_{IN}, for "always on" operation.

Programming Overvoltage Lockout Threshold with the OVLO Pin

The LT3797 provides an OVLO pin that allows user-programmable overvoltage lockout. A 1.25V (typical) rising threshold with 125mV hysteresis detects the overvoltage condition. The OVLO pin can be used to monitor V_{IN} or other voltages against overvoltage conditions.

Figure 1 shows OVLO connecting to V_{IN} through a voltage divider to protect against V_{IN} overvoltage. The rising threshold voltage and falling threshold voltage can be calculated by the following equations:

$$V_{OV(RISING)} = 1.25V \bullet \frac{R3+R4}{R4}$$

$$V_{OV(FALLING)} = 1.125V \bullet \frac{R3+R4}{R4}$$

An overvoltage condition turns off all three channels (including pulling the GATE pins to GND and TG pins to ISP) and resets the soft-starts.

Loop Compensation

Loop compensation determines the stability and transient performance. The LT3797 uses current mode control to regulate the output which simplifies loop compensation. The optimum values depend on the converter topology, the component values and the operating conditions (including the input voltage, LED current switching frequency). To compensate the feedback loop of the LT3797, a series resistor-capacitor network is usually connected from the VC pin to GND. Figure 1 shows the typical VC compensation network. For most applications, the capacitor should be in the range of 2.2nF to 22nF, and the resistor should be in the range of 2k to 25k. A practical approach to designing the compensation network is to start with one of the circuits in this data sheet that is similar to your application, and tune the compensation network to optimize the performance. Stability should then be checked across all operating conditions, including LED current, input voltage and temperature. Application Note 76 is a good reference for loop compensation.

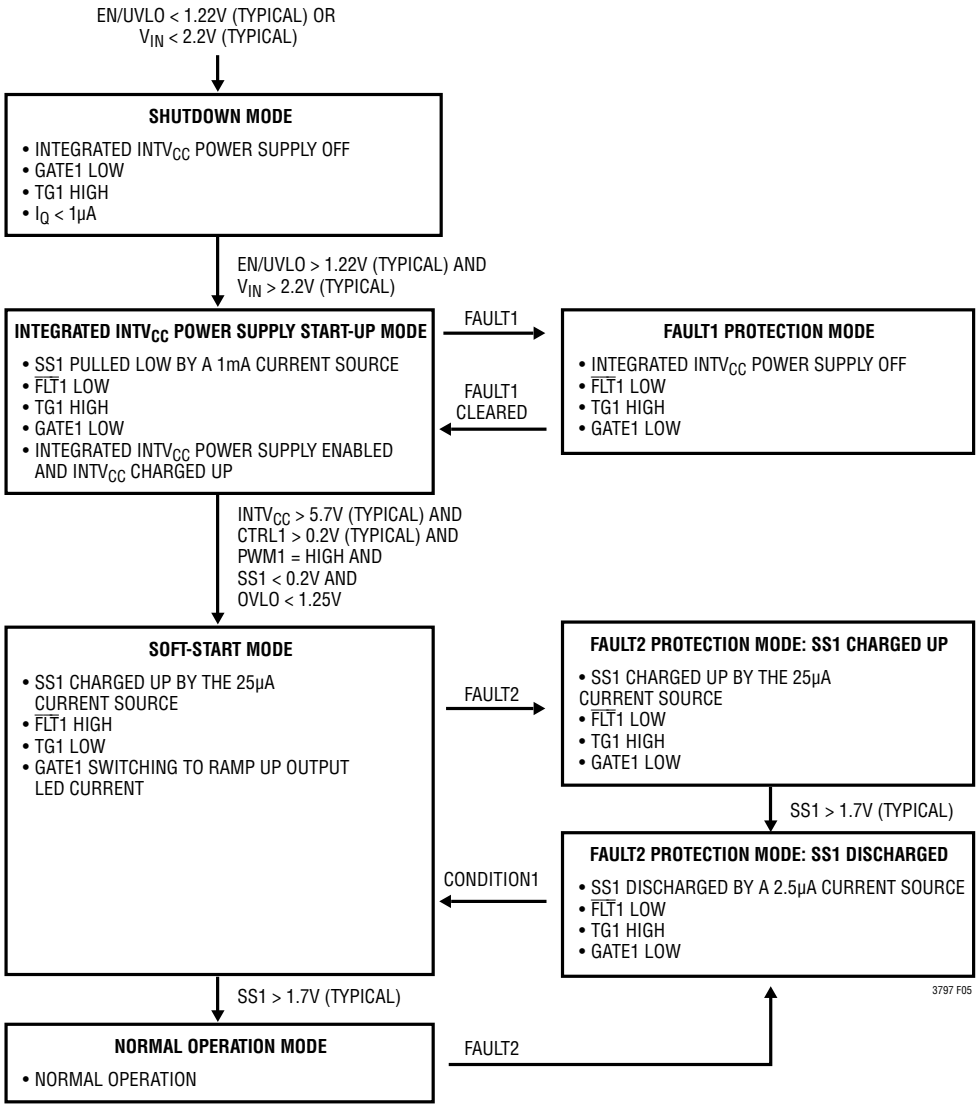
Soft-Start and Fault Protection

The LT3797 has identical soft-start and fault protection functions for each channel. The soft-start feature is designed to limit peak switch currents and output voltage (V_{OUT}) overshoot during start-up or recovery from a fault condition. Figure 4 shows the state diagram of the soft-start and fault protection of channel 1. Also refer to Figure 1 for channel 1 operation. In soft-start mode, the soft-start capacitor is charged up by the 25µA current source. The SS1 pin gradually increases the peak switch current allowed in M1 by clamping the VC1 voltage through Q4. In this way the SS1 pin allows the output capacitor, C_{OUT}, voltage to be charged gradually toward its final value while limiting M1 current overshoot. The soft-start interval is set by the soft-start capacitor selection according to the following equation:

$$t_{SS} = \frac{1.2V}{25\mu A} \bullet C_{SS}$$

The discharge time of the soft-start capacitor is controlled by a 2.5µA current source. Therefore, the SS1 pin is also used as an adjustable timer in the FAULT2 protection modes (see Figure 5) to prevent thermal runaway problems on the external components and/or the LEDs. In some fault conditions, the soft-start capacitor is charged and discharged repetitively, referred to as the hiccup mode operation. A typical hiccup mode operation occurs when an LT3797 LED driver has an output short-circuit fault. Figure 5 shows that if an output short-circuit fault causes LT3797 overcurrent (sensed by ISP1-ISN1) in the normal operation mode, the LT3797 moves to FAULT2 protection mode, where TG1 is pulled high, turning off the external PMOS and isolating the output. As a result, the overcurrent condition is cleared. When SS1 is discharged below 200mV, the LT3797 moves to soft-start mode, where TG1 is pulled low to turn on the external PMOS. If the short-circuit fault still exists, the LT3797 senses an overcurrent fault again and moves to FAULT2 protection mode: SS1 charged up and a new cycle starts. In this manner, the soft-start capacitor is kept charging and discharging between 200mV and 1.7V until the short-circuit fault is cleared.

APPLICATIONS INFORMATION



NOTES:

FAULT1 = V_{IN} > 41V (TYPICAL) OR
OVER TEMPERATURE (T_J > 165°C)

FAULT2 = V_{IN} > 41V (TYPICAL) OR
OVER TEMPERATURE (T_J > 165°C) OR
$INTV_{CC}$ < 5.2V (TYPICAL) OR
OVLO > 1.25V OR
OUTPUT OVER CURRENT

CONDITION1 = FAULT2 CLEARED AND
CTRL1 > 0.2V (TYPICAL) AND
PWM1 = HIGH AND
SS1 < 0.2V

Figure 5. State Diagram of the Soft-Start and Fault Protection of Channel 1

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The LT3797 fault protection can be configured as the latch-off mode by connecting a 470k resistor between the SS pin and V_{REF} pin. The FAULT2 conditions (see Figure 4) cause the LT3797 latch off. The LT3797 does not retry a soft-start even if the fault condition is cleared, since the SS pin is not able to fall below 0.2V by the 2.5µA pull-down current to reset the latch, due to the pulling up of the 470k resistor. The latch-off can only be cleared by toggling the EN/UVLO pin low to high.

The open-LED fault and the output overvoltage fault are not included in FAULT2 in Figure 5. These two faults do not affect the soft-start status. The open-LED fault in channel 1 causes $\overline{FLT}1$ low. The output overvoltage fault in channel 1 causes $\overline{FLT}1$ low and TG1 high to disconnect the LED load from power path.

APPLICATION CIRCUIT DESIGN GUIDELINE

The LT3797 contains three independent switching regulators. The following sections describe the LT3797 LED driver design guideline for the key parameters calculation and external components selection. The design guideline applies to each of the switching regulators.

Switch Duty Cycle

The LT3797 can be configured with different topologies. The boost LED driver is used for the applications where the LED voltage is higher than the input voltage. The LT3797 can be configured as a buck mode LED driver for the applications where the LED voltage is lower than the input voltage. The buck-boost mode and the SEPIC LED driver allow for the input voltage to be higher, equal to or lower than the LED voltage. The switch duty cycles of different topologies in continuous conduction mode (CCM) are:

$$D_{BOOST} = \frac{V_{LED} - V_{IN}}{V_{LED}}$$

$$D_{BUCK} = \frac{V_{LED}}{V_{IN}}$$

$$D_{BUCK\text{-}BOOST} = \frac{V_{LED}}{V_{LED} + V_{IN}}$$

$$D_{SEPIC} = \frac{V_{LED}}{V_{LED} + V_{IN}}$$

The maximum duty cycle (D_{MAX}) occurs when the converter has the minimum input voltage ($V_{IN(MIN)}$).

Inductor Selection

Figure 6 shows a typical inductor current waveform when the LED driver has maximum output current at the minimum input voltage. ΔI_L and $I_{L\_AVG(MAX)}$ denote the inductor ripple current and the maximum average inductor current respectively.

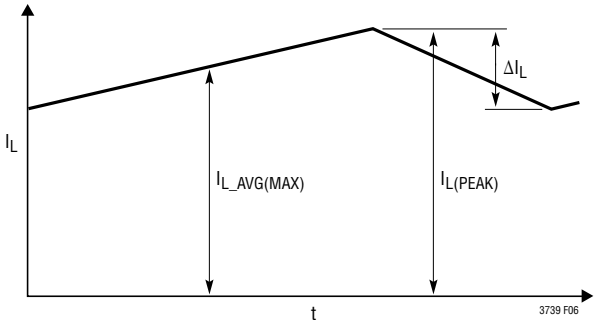

Figure 6. A Typical Inductor Waveform

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The $I_{L\_AVG(MAX)}$ of boost, buck mode, and buck-boost mode LED drivers in CCM are:

$$I_{L\_AVG(MAX)\_BUCK} = I_{LED(MAX)}$$

$$I_{L\_AVG(MAX)\_BOOST} = I_{LED(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

$$I_{L\_AVG(MAX)\_BUCK\text{-}BOOST} = I_{LED(MAX)} \bullet \frac{1}{1-D_{MAX}}$$

The primary and secondary maximum average inductor current of the SEPIC LED driver are:

$$I_{L1\_AVG(MAX)\_SEPIC} = I_{LED(MAX)} \bullet \frac{D_{MAX}}{1-D_{MAX}}$$

$$I_{L2\_AVG(MAX)\_SEPIC} = I_{LED(MAX)}$$

where $I_{LED(MAX)}$ is the maximum LED current.

The inductor ripple current ΔI_L has a direct effect on the choice of the inductor value. Choosing smaller values of ΔI_L requires large inductances and reduces the current loop gain (the converter will approach voltage mode). Accepting larger values of ΔI_L provides fast transient response and allows the use of low inductances, but results in higher input current ripple and greater core losses.

The inductor ripple percentage of the boost, buck mode, and buck-boost mode LED drivers is:

$$\frac{\Delta I_L}{I_{L(MAX)}}$$

For the SEPIC converter, ΔI_L of the primary inductor is equal to ΔI_L of the secondary inductor. The inductor ripple percentage can be calculated as:

$$\frac{2 \bullet \Delta I_L}{I_{L1(MAX)} + I_{L2(MAX)}}$$

The user should choose an appropriate ΔI_L based on the trade-offs to optimize the LED driver performance. It is recommended that the ripple current percentage fall within the range of 20% to 60% at D_{MAX}.

Given an operating input voltage range, and having chosen the operating frequency, f, and ripple current ΔI_L in the inductor, the inductor values of the boost, buck mode, and buck-boost mode LED drivers can be determined using the following equations:

$$L_{BUCK} = \frac{V_{LED}}{\Delta I_L \bullet f} \bullet \left(1-D_{MAX}\right)$$

$$L_{BOOST} = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

$$L_{BUCK\text{-}BOOST} = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

The primary and secondary inductor values of the SEPIC LED driver are:

$$L1 = L2 = \frac{V_{IN(MIN)}}{\Delta I_L \bullet f} \bullet D_{MAX}$$

By making L1 = L2, and winding them on the same core, the value of inductance in the preceding equation is replaced by 2L, due to mutual inductance:

$$L = \frac{V_{IN(MIN)}}{2 \bullet \Delta I_L \bullet f} \bullet D_{MAX}$$

The inductor peak current and RMS current in continuous mode operation can be calculated based on $I_{L(MAX)}$ and ΔI_L.

$$I_{L(PEAK)} = I_{L(MAX)} + 0.5 \bullet \Delta I_L$$

$$I_{L(RMS)} \approx I_{L(MAX)}$$

Based on the preceding equations, the user should choose the inductors having sufficient saturation and RMS current ratings.

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Switch Current Sense Resistors Selection

The LT3797 measures each channel's power N-channel MOSFET current by using a sense resistor (see R_{SW_SEN} in Figure 1) between GND and the MOSFET source. Figure 7 shows a typical waveform of the sense voltage (V_{SW_SENSE}) across the sense resistor in CCM. The placement of the sense resistor R_{SW_SEN} should be close to the source of the MOSFET and GND. The SENSEP and SENSEN sense node traces should run parallel to each other to a Kelvin connection on the positive and negative terminals of R_{SW_SEN}.

Due to the current limit function of the power switch current control, R_{SW_SEN} should be selected to guarantee that the peak current sense voltage $V_{SW\_SENSE(PEAK)}$ during steady-state normal operation is lower than the SENSE current limit threshold (100mV minimum). It is recommended to give a 20% margin and set $V_{SW\_SENSE(PEAK)}$ to be 80mV. Then, the switch current sense resistor value can be calculated as:

$$R_{SW\_SEN} = \frac{80mV}{I_{SW(PEAK)}}$$

where $I_{SW(PEAK)}$ is the peak switch current. $I_{SW(PEAK)}$ of the boost, buck mode and buck-boost mode LED driver is:

$$I_{SW(PEAK)} = I_{L(PEAK)}$$

$I_{SW(PEAK)}$ of the SEPIC LED driver is:

$$I_{SW(PEAK)} = I_{L1(PEAK)} + I_{L2(PEAK)}$$

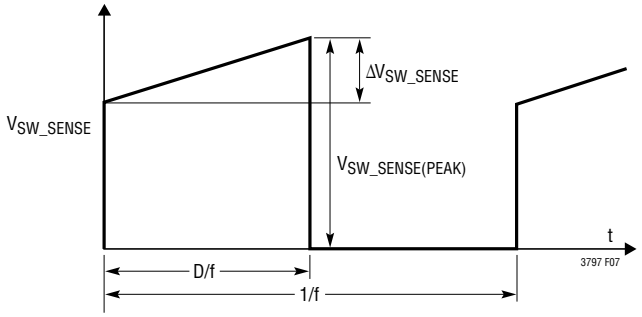

Figure 7. The Sense Voltage Across the Sense Resistor in CCM

Sense Voltage Ripple Verification

After the inductor ripple current and the switch current sense resistor value have been selected according to the previous sections, the sense voltage ripple ΔV_{SW_SENSE} (refer to Figure 7) of the boost, buck, and buck-boost LED drivers can be determined using the following equation:

$$\Delta V_{SW\_SENSE} = \Delta I_L \bullet R_{SW\_SEN}$$

ΔV_{SW_SENSE} of the SEPIC LED driver can be determined using the following equation:

$$\Delta V_{SW\_SENSE} = 2 \bullet \Delta I_L \bullet R_{SW\_SEN}$$

The LT3797 has internal slope compensation to stabilize the control loop against sub-harmonic oscillation. When the LT3797 operates at a duty cycle greater than 0.66 in CCM, the sense voltage ripple, ΔV_{SW_SENSE} (refer to Figure 7), needs to be limited to ensure the internal slope compensation is sufficient to stabilize the control loop. Figure 8 shows the maximum ΔV_{SW_SENSE} over the duty cycle. It is recommended to check and ensure ΔV_{SW_SENSE} is below this curve at the highest duty cycle. If ΔV_{SW_SENSE} is above the maximum ΔV_{SW_SENSE} curve at the highest duty cycle, the ΔI_L needs to be reduced and the parameters in the previous two sections need to be recalculated until the optimized values are obtained.

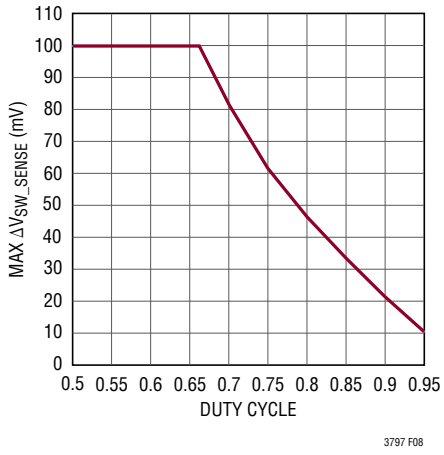

Figure 8. The Maximum Sense Voltage Ripple vs Duty Cycle for CCM

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Power MOSFET Selection

The selection criteria for the power MOSFET includes the drain-source breakdown voltage (BV_{DSS}), the threshold voltage ($V_{GS(TH)}$), the on-resistance ($R_{DS(ON)}$), the total gate charge (Q_G), the maximum drain current ($I_{D(MAX)}$) and the MOSFET's thermal resistances ($R_{\theta JC}$ and $R_{\theta JA}$), etc.

The required power MOSFET BV_{DSS} rating of different topologies can be estimated using the following equations. Add a diode forward voltage, and any additional ringing across its drain-to-source during its off-time.

$BV_{DSS\_BOOST} > V_{LED}$

$BV_{DSS\_BUCK} > V_{IN(MAX)}$

$BV_{DSS\_BUCK\text{-}BOOST} > V_{IN(MAX)} + V_{LED}$

$BV_{DSS\_SEPIC} > V_{IN(MAX)} + V_{LED}$

The power dissipated by the MOSFET in a boost, buck mode, or buck-boost mode LED driver is:

$$P_{FET} = I_{L(MAX)}^2 \bullet R_{DS(ON)} \bullet D_{MAX} + 2 \bullet V_{SW(PEAK)} \bullet I_{L(MAX)} \bullet C_{RSS} \bullet f/1.5A$$

The power dissipated by the MOSFET in a SEPIC LED driver is:

$$P_{FET} = (I_{L1(MAX)} + I_{L2(MAX)})^2 \bullet R_{DS(ON)} \bullet D_{MAX} + 2 \bullet V_{SW(PEAK)} \bullet (I_{L1(MAX)} + I_{L2(MAX)}) \bullet C_{RSS} \bullet f/1.5A$$

The first terms in the preceding equations represent the conduction losses in the devices, and the second terms, the switching losses. C_{RSS} is the reverse transfer capacitance, which is usually specified in the MOSFET characteristics. For maximum efficiency, $R_{DS(ON)}$ and Q_G should be minimized. From a known power dissipated in the power MOSFET, its junction temperature can be obtained using the following equation:

$$T_J = T_A + P_{FET} \bullet \theta_{JA} = T_A + P_{FET} \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

Schottky Rectifier Selection

The power Schottky diode conducts current during the interval when the switch is turned off. In an LT3797 LED driver, the Schottky diode should have the same voltage rating as the power N-channel MOSFET in the same channel. Refer to the power MOSFET BV_{DSS} rating in the previous section for the peak reverse voltage rating selection. If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Choose a Schottky diode with sufficiently low leakage current.

The power dissipated by the diode in a boost, buck, or buck-boost converter in CCM is:

$$P_D = I_{L\_AVG(MAX)} \bullet V_D \bullet (1 - DMAX)$$

where V_D is the diode forward voltage drop.

The power dissipated by the diode in a SEPIC converter is:

$$P_D = (I_{L1\_AVG(MAX)} + I_{L2\_AVG(MAX)}) \bullet V_D \bullet (1 - D_{MAX})$$

and the diode junction temperature is:

$$T_J = T_A + P_D \bullet (\theta_{JC} + \theta_{CA})$$

T_J must not exceed the diode maximum junction temperature rating.

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High Side PMOS Disconnect Switch Selection

A PMOS with a minimum $V_{GS(TH)}$ of –1V to –2V is recommended for the high side disconnect switch in most LT3797 applications to improve the PWM dimming ratio and protect the LED array from excessive heating during fault conditions. The PMOS BV_{DSS} rating must be higher than the open-LED regulation voltage set by the FBH pin. The maximum continuous drain current $I_{D(MAX)}$ rating should be higher than the maximum LED current.

Input Capacitor Selection

The input capacitor C_{IN} supplies the AC ripple current to the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the required capacitor value. The X5R or X7R type ceramic capacitors are usually good choices since they have small variation with temperature and DC bias. Typically, the boost or SEPIC converter requires a lower value input capacitor than the buck mode or buck-boost mode converter, due to the fact that its inductor is in series with the input, and the input current waveform is continuous. The input capacitor value can be estimated based on the inductor ripple ΔI_L (refer to Inductor Selection section), the switching frequency, and the acceptable input voltage ripple ΔV_{IN} on C_{IN}. C_{IN} value of the boost and SEPIC converter can be calculated by:

$$C_{IN} = 0.125 \bullet \frac{\Delta I_L}{\Delta V_{IN} \bullet f}$$

C_{IN} value of the buck mode and buck-boost mode LED driver can be calculated by:

$$C_{IN} = I_{LED} \bullet \frac{V_{LED} \bullet \left(V_{IN(MIN)} - V_{LED}\right)}{V_{IN(MIN)}^2 \bullet \Delta V_{IN} \bullet f}$$

Output Capacitor Selection

The output filter capacitors should be sized to attenuate the LED current ripple. Use of X5R or X7R type ceramic capacitors is recommended. To achieve the same LED ripple current, the required filter capacitor is smaller in the buck mode applications than that in the boost, buck-boost mode and SEPIC applications. This is due to the fact that, in the buck converter, the inductor is in series with the output and the ripple current flowing through the output capacitor is continuous. Lower operating frequencies will require proportionately higher capacitor values.

The DC Coupling Capacitor Selection for SEPIC LED Driver

The DC voltage rating of the DC coupling capacitor, C_{DC}, connected between the primary and secondary inductors should be larger than the maximum input voltage:

$$V_{CDC} > V_{IN(MAX)}$$

C_{DC} has nearly a rectangular current waveform in CCM. During the switch off-time, the current through C_{DC} is I_{VIN}, while approximately $–I_{LED}$ flows during the on-time. The C_{DC} voltage ripple causes distortions on the primary and secondary inductor current waveforms. The C_{DC} should be sized to limit its voltage ripple. The power loss on the C_{DC} ESR reduces the LED driver efficiency. Therefore, the sufficient low ESR ceramic capacitors should be selected. The X5R or X7R ceramic capacitor is recommended for C_{DC}.

Integrated $INTV_{CC}$ Power Supply

The LT3797 includes an internal switch mode DC/DC converter to generate a regulated 7.5V $INTV_{CC}$ power supply to power the NMOS gate drivers of the three channels (I_{DRIVE}). This $INTV_{CC}$ power supply can also be used to drive external circuits (I_{EXT}). This $INTV_{CC}$ power supply

APPLICATIONS INFORMATION

has two major advantages over the traditional internal LDO regulators. It is able to generate 7.5V $INTV_{CC}$ voltage from a V_{IN} voltage as low as 2.5V, allowing the LT3797 to drive high threshold MOSFETs in the low V_{IN} applications. It is also able to deliver large current from a V_{IN} voltage as high as 40V without overheating the package, due to its high efficiency (over 70% at full load). This integrated DC/DC converter requires three external components (C_{VCC}, C_{BOOST} and L_{PWR}) for operation, as shown in Figure 1. Select these three components based on the following guidelines:

- C_{VCC} is a 10µF/10V ceramic capacitor used to bypass $INTV_{CC}$ to GND immediately adjacent to the pins.
- C_{BOOST} is a 0.1µF/10V ceramic capacitor connected between the BOOST pin and the SW1 pin.
- Select a 47µH inductor with the saturation current rating of 0.6A or greater and RMS current rating of 0.4A or greater for L_{PWR}.

The $INTV_{CC}$ power supply has an output current limit function to protect itself from excessive electrical and thermal stress. Figure 9 shows the $INTV_{CC}$ output limit (I_{INTVCC_LMT}) vs V_{IN} and switching frequency. Make sure the sum of the I_{DRIVE} and I_{EXT} is always lower than the I_{INTVCC_LMT} across the whole V_{IN} range of the application circuit:

$$I_{DRIVE} + I_{EXT} < I_{INTVCC\_LMT}$$

where:

$$I_{DRIVE} = (Q_{G\_CH1} + Q_{G\_CH2} + Q_{G\_CH3}) \bullet f_{SW}$$

Q_{G_CH1-3} is the total gate charge of the NMOS of the three channels at V_{GS} = 0V to 7.5V.

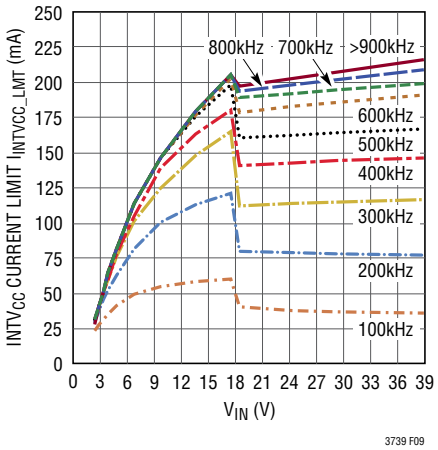

Figure 9. $INTV_{CC}$ Current Limit vs V_{IN}, f_{SW}

Board Layout

The high speed operation of the LT3797 demands careful attention to board layout and component placement. The exposed pad of the package is the only GND terminal of the IC, and is important for thermal management of the IC. Therefore, it is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground planes of the board. For the LT3797 to deliver its full output power, it is imperative that a good thermal path be provided to dissipate the heat generated within the package. It is recommended that multiple vias in the printed circuit board be used to conduct heat away from the IC and into copper planes with as much area as possible.

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Due to the highly compact integration of the three switching channels within the LT3797, careful consideration must be given to possible noise coupling between channels. To reduce noise coupling, the compensation network components connected to the VC1-3 pins and the DC control signal components connected to the SS1-3, RT, EN/UVLO, and CTRL1-3 pins must be connected to signal ground (SGND). The signal ground (SGND) and power ground (PGND) connection should only occur at the LT3797 exposed GND pad (pin 53). Further, board traces for high impedance signals such as FBH1-3 and VC1-3 should be kept to the shortest length possible to avoid unwanted noise pick up. Also, the decoupling capacitors that connect V_{IN} to PGND and $INTV_{CC}$ to PGND should be physically located close to their respective pins. Finally, for high voltage and/or high current applications, an effective approach to attenuate possible switch noise coupling into each channel's control loop is to add a small footprint size 0.1µF ceramic capacitor between each SENSEP pin and the corresponding SENSEN pin. When used, these noise filtering capacitors should be physically located near their respective pins. Figure 10 provides an example of a PCB layout of the decoupling capacitors, compensation networks and ground separation.

To reduce electromagnetic interference (EMI) and high frequency resonance problems, proper layout of the LT3797 LED driver power stage is essential, especially the power paths with high di/dt. Figures 11-14 show the simplified power stage circuits of boost, buck mode, buck-boost mode and SEPIC topologies with the high di/dt loops highlighted. The high di/dt loops of different topologies should be kept as tight as possible to reduce inductive ringing. Figures 15-16 shows the examples of the high di/dt loop layout of the different topologies shown in Figures 11-14.

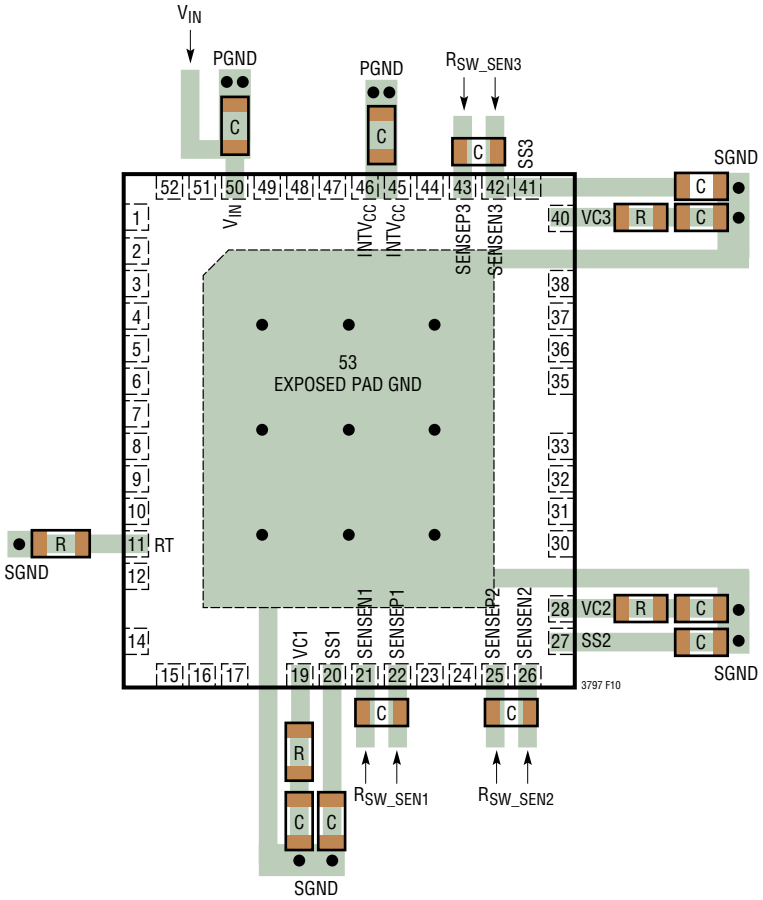

Figure 10. Decoupling Capacitors and Ground Separation

APPLICATIONS INFORMATION

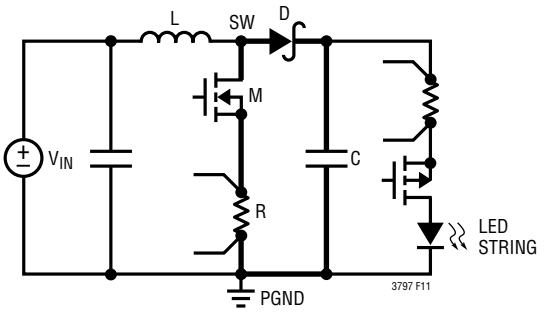

Figure 11. The Simplified Boost LED Driver Power Stage with the High di/dt Loop Highlighted

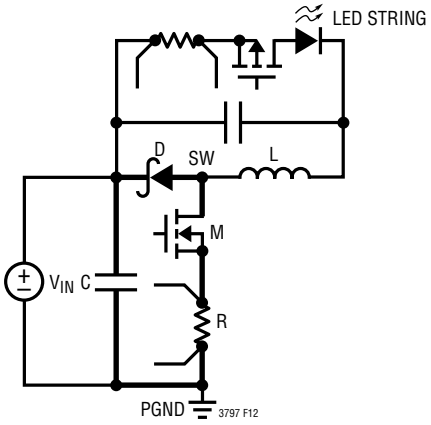

Figure 12. The Simplified Buck Mode LED Driver Power Stage with the High di/dt Loop Highlighted

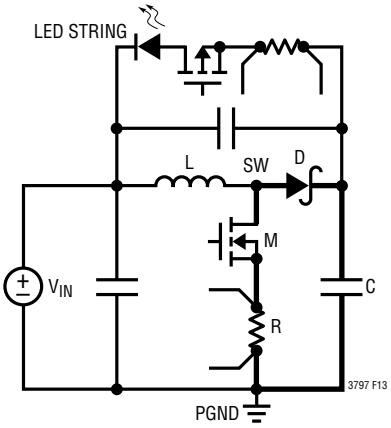

Figure 13. The Simplified Buck-Boost Mode LED Driver Power Stage with the High di/dt Loop Highlighted