Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

GC3021A

3.3V MIXER AND CARRIER REMOVAL CHIP

DATASHEET

October 2002

This datasheet contains information which may be changed at any time without notice.

REVISION HISTORY

This datasheet is revised from the GC3021 datasheet to reflect the changes in the GC3021A replacement.

Revision	Date	Description
1.0	9 Sept2002	First GC3021A datasheet. Major changes in specifications to reflect 3.3volt operation.

0.1 GC3021A TO GC3021 COMPARISON

The GC3021A is designed to be a functional and footprint compatible replacement for the GC3021 chip. The timing specifications for the GC3021A meet and exceed the timing specifications for the GC3021. Electrically the GC3021A is a 3.3 volt only part, making it incompatible with the GC3021's 5 volt mode. The GC3021A does not support the PECL high speed interface from the GC3021. Except for this change, the GC3021A is fully compatible with the GC3021's 3.3 volt mode, but at a lower power consumption. See Section 5 for timing and electrical specifications. NOTE: The GC3021A inputs are NOT 5 volt tolerant; chip damage may occur if the input voltages exceed Vcc + 0.5V (3.8 volts). Designs using the GC3021 at 5 volts will need to add a 3.3 volt supply and voltage level translators to use the GC3021A.

The function of the GC3021A has been slightly enhanced, but any enhancements are "backward" compatible with the GC3021 with the exception of the power down control. In the GC3021A the user must set bit 15 of control register 1. Highlights of the enhancements follow.

0.1.1 Clock Loss Detect and Power Down Modes

The GC3021 chip used a slow internal clock to power down the chip or to put it into a low power mode if the clock is stopped. The slow clock has been removed in the GC3021A and replaced with a mode that will put the chip in a fully static mode if the clock has stopped. The fully static mode powers down the chip and reduces the power consumption down to a few microwatts until the clock resumes. The user can also force the power down state if desired. Two control bits (address 13 bits 6 and 7) are used to control the clock loss detect and power down modes. One control bit turns off the clock loss detect circuit, the other forces the power down mode. Both bits are cleared at power up to keep GC3021 compatibility. THE USER MUST SET POWER DOWN TO A "2" TO OPERATE THE CHIP.

See Section 2.9 for details.

0.1.2 Control Interface

The control interface has been enhanced to use either the R/$\overline{W}$ and $\overline{CS}$ strobes of the original GC3021, or to use the $\overline{RE}$, $\overline{WE}$ and $\overline{CE}$ strobes used by most memory interfaces. If the $\overline{RE}$ pin is grounded, then the interface behaves in the R/$\overline{W}$ and $\overline{CS}$ mode, where the $\overline{WE}$ pin becomes the R/$\overline{W}$ pin and the $\overline{CE}$ pin becomes the $\overline{CS}$ pin. The $\overline{RE}$ pin on the GC3021A chip is a ground pin (pin 58) on the GC3021 chip, so that a GC3021A chip soldered into a GC3021 socket will automatically operate in the GC3021 R/$\overline{W}$ and $\overline{CS}$ mode.

See Section 2.1 for details.

GC3021A DATASHEET

1.0 KEY FEATURES

CARRIER REMOVAL MODE

- 100 Million Complex Samples per second (CSPS) input data
- 12 bit input and output data
- 12 bit by 12 bit complex multiplier
- 4K bit phase error lookup RAM
- Phase error feedback loop for carrier and phase offset removal
- 32 bit numerically controlled oscillator (NCO)
- Snapshot memory for adaptive filtering

MIXER MODE

- 200 MSPS real input data (even/odd data at 100MSPS)
- 100 MSPS complex input data (TTL level inputs)
- 12 bit inputs and outputs
- 32 bit NCO phase control
- NCO generates 12 bit sines and cosines

OVERALL

- Microprocessor interface for control, output, and diagnostics
- Built in diagnostics
- 500 mW power at 100 MHz, 3.3 volts
- 160 pin plastic quad flat pack package

1.1 BLOCK DIAGRAM

A block diagram illustrating the major functions of the chip is shown in Figure 1

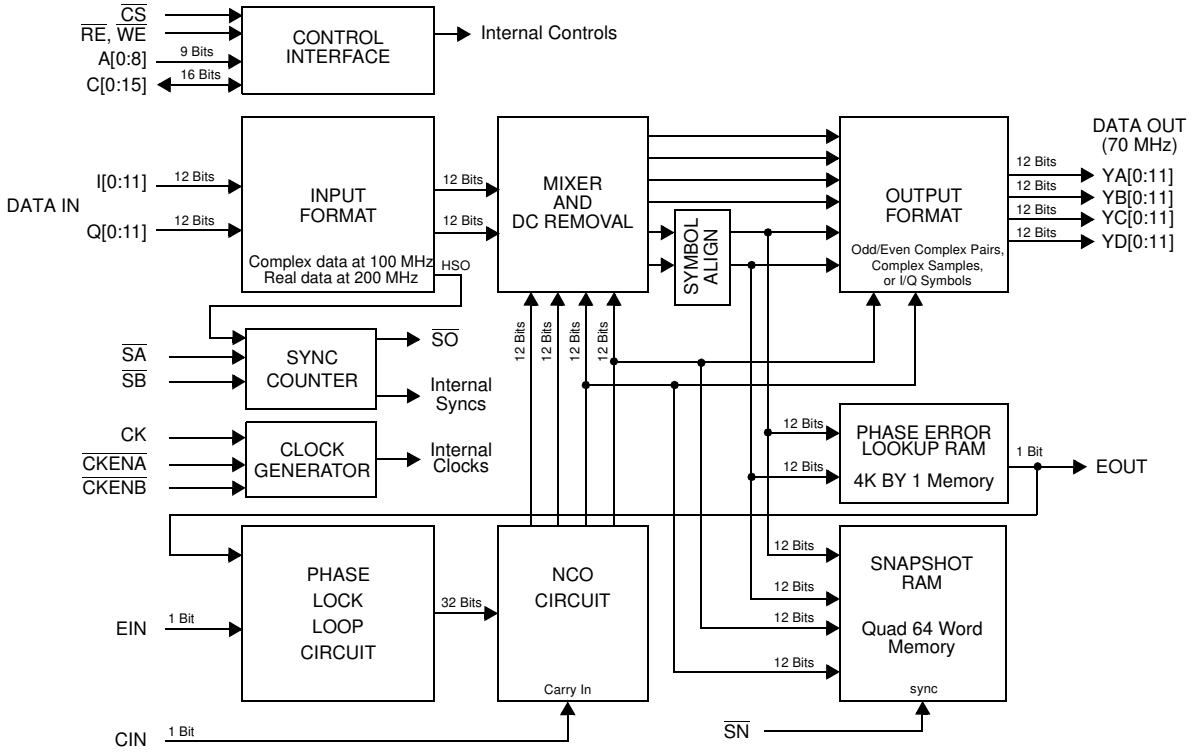


Figure 1. GC3021A BLOCK DIAGRAM

2.0 FUNCTIONAL DESCRIPTION

Fabricated in 0.5 micron CMOS technology, the GC3021A chip is designed to mix input data with an internally generated sine/cosine sequence. The chip can be used as a signal mixer, or if the phase error lookup and phase lock loop (PLL) circuitry is enabled, as a carrier removal circuit for signal demodulation. The mixer accepts complex data at rates up to 100 MHz , or real samples at rates up to 200 MHz in the real input mode . The chip mixes the input with a complex sinusoid, and outputs the results at a 100 MHz rate.

The input data in the real mode is assumed to be even/odd sample pairs. The 200 MHz input data is split into even and odd samples streams, each at a rate of 100 million samples per second. The even and odd time sample data streams are mixed with sines and cosines which have also been split into even and odd time streams. The complex results are then output as two complex pairs at 100 MHz, one for the even time samples and one for the odd time samples.

The frequency of the sine/cosine sequence is specified as a 32 bit phase word which drives a phase accumulator. A carry input to the phase accumulator allows the user to extend the tuning resolution with an external accumulator.

The GC3021A chip's carrier removal mode allows the chip to be used as part of a QPSK/QAM demodulator using decision error feed back to achieve carrier lock. A phase error feedback circuit uses the upper 7 bits of the I and Q mixer outputs to lookup a one bit phase error term. The phase error lookup is performed by mapping the I/Q pair into a single quadrant so that the lookup table address is only 12 bits (6 bits of I and 6 bits of Q). The 4096 bit lookup table is programmed by the user to output the sign of the phase error for each possible I/Q pair. This phase error feeds a phase-lock-loop (PLL) circuit which adjusts the sinusoid frequency to drive the average phase error to zero.

A snapshot RAM is included to store blocks of I/Q symbol outputs and the sine/cosine pairs used to generate them. This information is used by an external DSP chip or microprocessor to lookup the symbol error, to rotate the error by the sine/cosine phase, and then update equalizer coefficients.

On chip diagnostic circuits are provided to simplify system debug and maintenance.

The chip receives configuration and control information over a microprocessor compatible bus consisting of a 16 bit data I/O port, a 9 bit address port, a read enable, a write enable, and a chip enable strobe. The control registers, coefficient registers, phase error RAM and snapshot memory are mapped into the 512 word address space of the control port.

A detailed description of the major circuits within the chip follows.

2.1 CONTROL INTERFACE

The control interface allows an external processor to configure the chip, to capture and read samples from the chip and to perform diagnostics.

The chip is configured by writing control information into control registers within the chip. The registers are written to or read from using the **C[0:15]**, **A[0:8]**, $\overline{\textbf{RE}}$, $\overline{\textbf{WE}}$, and $\overline{\textbf{CE}}$ pins. Each control register has been assigned a unique address within the chip. An external processor (a microprocessor, computer,

or DSP chip) can write into a register by setting **A[0:8]** to the desired register address, setting the **$\overline{CE}$** pin low, setting **C[0:15]** to the desired value and then pulsing **$\overline{WE}$** low. **$\overline{RE}$** must remain high.

To read from a control register the processor must set **A[0:8]** to the desired address, set **$\overline{CE}$** low, and then set **$\overline{RE}$** low. The chip will then drive **C[0:15]** with the contents of the selected register. After the processor has read the value from **C[0:15]** it should set **$\overline{RE}$** and **$\overline{CE}$** high. The **C[0:15]** pins are turned off (high impedance) whenever **$\overline{CE}$** is high or **$\overline{WE}$** is low. The chip will only drive these pins when both **$\overline{CE}$** and **$\overline{RE}$** are low and **$\overline{WE}$** is high.

If **$\overline{RE}$** is held low, then the interface will behave in the GC3021 mode, where **$\overline{CE}$** is **$\overline{CS}$**, and **$\overline{WE}$** is **R/$\overline{W}$**.

The chip's control address space is divided into fourteen control registers, a test port, four DC offset registers, 256 phase error memory words, and 256 snapshot memory words. The 14 control registers are MODE_REG, SYNC_REG0, SYNC_REG1, DELAY_REG, COUNTER_REG, PLL_REG, FREQ_REG0, FREQ_REG1, OUTPUT_REGA, OUTPUT_REGB, OUTPUT_REGC, OUTPUT_REGD, SNAP_REG, and PHASE_REG. The control registers are mapped to addresses 0 to 13. See Section 4.0 for details about the contents of these registers.

Address 14 is used to generate a one-shot pulse. This pulse, $\overline{OS}$, which is one clock cycle wide, can be output from the chip on the $\overline{SO}$ pin or used to synchronize internal circuits. Address 15 is a read only port used to monitor the power-down and keepalive clock functions for test. Addresses 16 through 19 are the DC offset registers DC_I_IN, DC_Q_IN, DC_I_OUT, DC_Q_OUT.

Addresses 20 through 255 are unused.

Addresses 256 through 511 are shared between the phase error memory and the snapshot memory. Reading from these addresses accesses the contents of the snapshot memory. Writing to these addresses loads the phase error lookup memory.

2.2 SYNC COUNTER

The sync counter circuit is used to generate sync pulses for the chip. The circuit accepts two sync inputs ($\overline{SA}$ and $\overline{SB}$) and generates internal syncs and a sync out ($\overline{SO}$) pulse. The circuit contains a 20 bit counter which can be set to count in cycles of 16*(COUNT+1) clocks, where COUNT ranges from 0 to 2^{16}-1. The counter's terminal count ($\overline{TC}$) can be used as a synchronization pulse. The lower 12 bits from the counter are used as input data during diagnostics.

The circuit can generate a one-shot pulse (OS) which can be used as a synchronization pulse.

The input syncs $\overline{SA}$ and $\overline{SB}$ can be delayed by up to 258 clock cycles. The delayed syncs ($\overline{DSA}$ and $\overline{DSB}$) can be used to adjust the sync timing to meet system requirements.

The internal syncs are used to synchronize the counter, the symbol align circuit, the snapshot memory, the phase lock loop circuit and NCO circuit. Each circuit can be independently synchronized to $\overline{SA}$, $\overline{SB}$, $\overline{DSA}$, $\overline{DSB}$, $\overline{TC}$, $\overline{OS}$, or left to free run. The sync output can also be chosen from these syncs.

2.3 CLOCK GENERATOR

The clock generator generates the internal clocks from the clock input (CK). Two clock enable inputs ($\overline{\text{CKENA}}$ and $\overline{\text{CKENB}}$) are used to enable or disable the clock. Both enables must be low for internal clocks to be generated. The enables are clocked into the chip and are used to enable or disable the following clock edge. The enables are designed to be used with the data valid strobes from the GC3021A digital resampler and GC2011Adigital filter chips.

2.4 INPUT FORMAT

The input format circuit accepts complex data at the clock rate of the chip, or real data at twice the clock rate of the chip. The input format circuit outputs pairs of samples to the mixer circuit where the pair is either a complex data pair, or an even and odd time sample pair. A block diagram of the input circuit is shown in Figure 2.

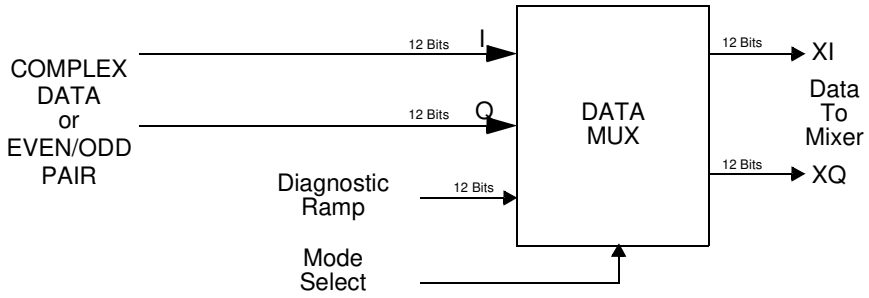


Figure 2. INPUT FORMAT CIRCUIT

The even/odd data inputs share pins with the I/Q complex data inputs. The I input pins are used as the even time inputs and the Q pins are used as the odd time inputs. The even samples are assumed to preceed the odd time samples. I.E., (X0, X2, X4, ...) are the even time samples, (X1, X3, X5,..) are the odd time samples.

2.5 MIXER

The mixer multiplies the pairs of samples from the input format circuit by sines and cosines and outputs the results to the output format and the symbol offset circuits. A block diagram of the mixer circuit is shown in Figure 3.

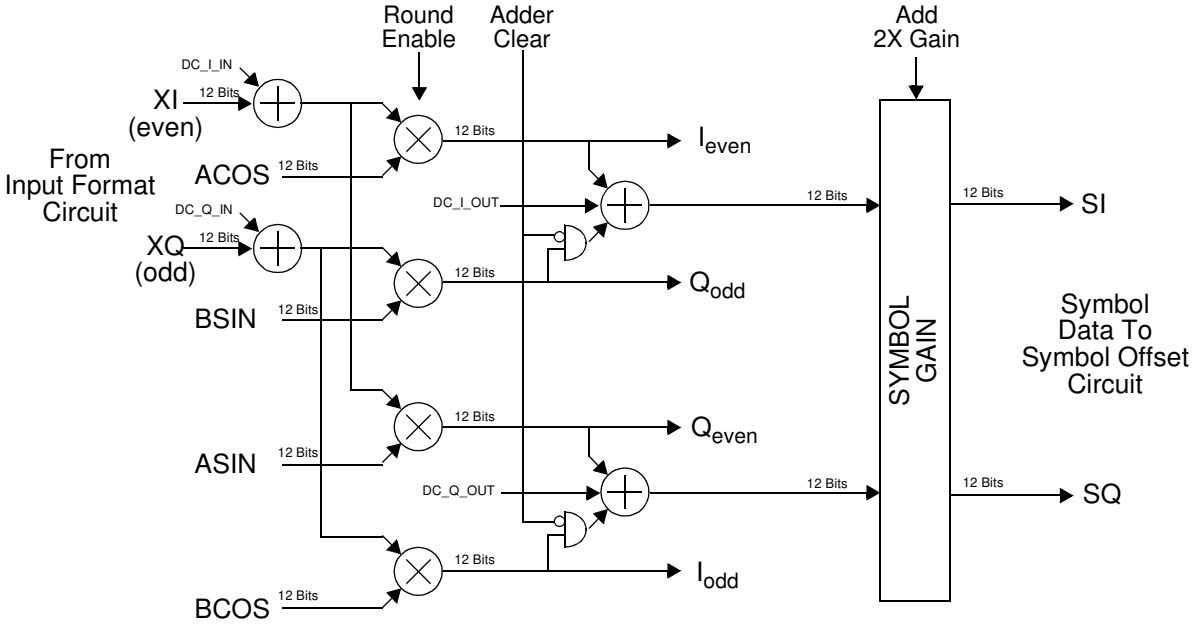


Figure 3. MIXER

The ACOS, BCOS, ASIN and BSIN values are generated by the NCO circuit. In the complex mode BCOS will equal ACOS and BSIN will equal minus ASIN. In the high speed mode the ASIN and ACOS values are the even time sine/cosine pairs and the BCOS and BSIN values are the odd time pairs. The lower 11 bits of the 23 bit multiplier products are either rounded off or truncated depending upon the state of the round enable control. The rounding is performed using the "round to even" technique[1]. The 12 bit products are passed to the output format circuit.

The adders sum the individual products to generate complex products. The adder outputs are saturated to 12 bits if the add causes overflow. The adder outputs pass through a gain circuit and then to the symbol offset circuit. The gain circuit, if it is enabled, doubles the data values. The gain outputs are saturated to plus or minus full scale if the gain causes overflow[2]. The adder clear control allows the I_{even} and Q_{even} mixer outputs, instead of the complex products, to be passed to the symbol gain circuit. This permits the user to capture the high speed mode's even outputs in the snapshot RAM, or to use them in the phase error lookup circuit.

DC components before or after the mixer can be removed by adjusting the DC_I_IN, DC_Q_IN, DC_I_OUT and the DC_Q_OUT values. These values are added to the input and output data as shown in

1. When the fraction to be rounded is exactly 1/2, the round to even technique rounds up when the integer portion is odd and rounds down when it is even. This removes any DC bias in the rounding.
2. The input samples of QAM signals have an extra sign bit before the carrier is removed. The extra sign bit is needed because the square QAM constellation is spinning. Once carrier has been removed the extra sign bit can be removed by the gain circuit. This increases the resolution of the phase error RAM and simplifies the symbol mapping.

Figure 3. The outputs from these adders are saturated to plus or minus full scale (12 bits) if overflow is detected.

2.6 SYMBOL ALIGN

The symbol align circuit is used in the carrier removal mode to process offset (or staggered) QPSK signals. The offset is removed by delaying the SI sample by one clock cycle so that it is paired with the next SQ sample. Every other SI and SQ pair is held for two clock cycles, effectively decimating the sample rate by two. The symbol offset circuit is controlled by the OFFSET and OFFSET_HOLD control bits described in Section 4.1 The symbol offset circuit is synchronized by the OFFSET_SYNC described in Section 4.2.

2.7 PHASE ERROR RAM

The the I and Q samples are passed to the phase error RAM. The phase error RAM uses the upper 7 bits of the I and Q values to look up the sign of the phase error for the sample. The phase error RAM contents are downloaded through the control interface. The phase error RAM outputs a 1 or a 0 depending upon whether the phase angle of the (I, Q) complex pair is greater than or smaller than the nearest decision point for the signal's constellation pattern. A "0" means that the phase angle needs to be increased to match the decision point and a "1" means it needs to be decreased. A block diagram of the phase error RAM circuit is shown in Figure 4.

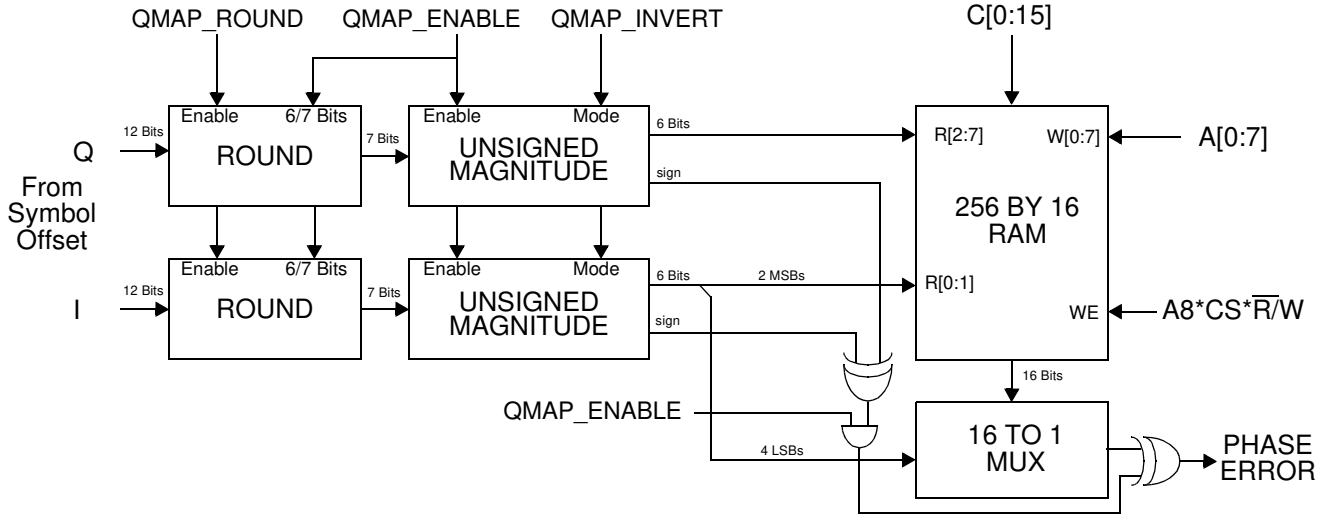


Figure 4. PHASE ERROR RAM

The round circuit rounds the 12 bit I and Q samples into the upper 6 or 7 bits, or, if rounding is disabled, truncates them. If the quadrant map (Qmap) mode is enabled the circuit rounds to 7 bits, otherwise it rounds to 6 bits. The rounding is performed using the round to even technique.

The rounded bits are passed to the unsigned magnitude circuit where, if Qmap is enabled, they are converted from 7 bit 2's complement signed numbers to 6 bit unsigned numbers. The conversion is performed using 2's complement negation unless the invert control is set. If the invert control is set, then the negation is performed by inverting the data bits (i.e., a 1's complement negation is used).

If Qmap is enabled the circuit outputs the 6 bit magnitude and the sign bit. If Qmap is turned off the circuit outputs the 6 bit signed number from the round circuit.

The Qmap mode is used to map the I, Q complex pair into one quadrant for looking up the phase error. This is possible when the signal's constellation pattern has quadrant symmetry. If the pattern does not exhibit symmetry, then the quadrant map mode should not be used.

The 6 bit I and Q values are used to lookup the phase error in a 4096 by 1 bit memory. In the Qmap mode the phase error is inverted as necessary to map it back into the proper quadrant.

The memory is implemented using a 256 word by 16 bit RAM as shown in Figure 4. The RAM is loaded as 256 sixteen bit words mapped to addresses 256 to 511 of the control interface. The RAM is a write only memory.

The phase error is passed to the phase lock loop (PLL) circuit. The phase error is also output on the EOUT pin of the chip for external use.

2.8 PHASE LOCK LOOP

The phase error drives the PLL circuit shown in Figure 5.

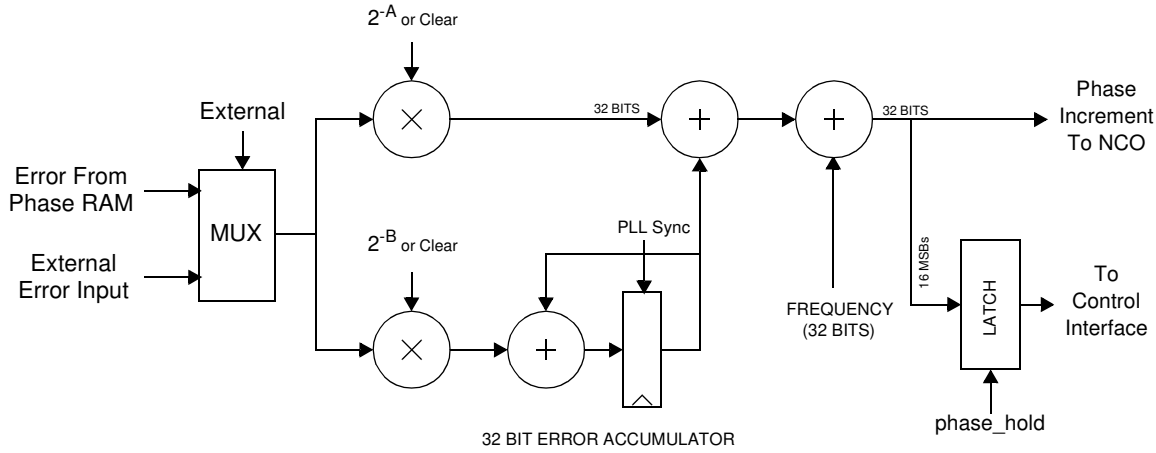


Figure 5. PLL CIRCUIT

The phase error can either come from an input pad or from the phase error RAM. The error is multiplied by the two constants 2^{-A} and 2^{-B}. These multipliers treat a phase error of "0" as +1 and a phase error of "1" as -1. The multipliers also have a clear mode so that 2^{-A} or 2^{-B} can be set to zero.

The tracking bandwidth and damping of the of the phase lock loop filter are set using the constants A and B. The filter will be critically damped when A is approximately one-half of B. When critically damped the tracking bandwidth and residual phase jitter of the loop are set by B. A small value for B results in a wide bandwidth with lots of jitter, but fast acquisition. A large value of B narrows the bandwidth and reduces the residual jitter, but increases the initial acquisition time. Values of B between 24 and 31 are suggested. Use 24 for initial acquisition and 31 for final tracking. The values of A and B are double buffered so that the loop bandwidth can be changed synchronous to an external sync signal.

Initial acquisition can be greatly aided by presetting the PLL to an estimated frequency offset. This is done by loading the frequency register with the estimated frequency.

In the mixer mode the PLL is turned off by clearing 2^{-A} and 2^{-B}, clearing the accumulator and setting the frequency register to the desired tuning frequency. The 32 bit frequency word is set to the desired frequency using the formula: $FREQ = \frac{Frequency}{Clock\ Rate} 2^{32}$, where "Frequency" is the desired

frequency and “Clock Rate” is the chip’s clock rate. The frequency register is double buffered so that frequency changes can be made synchronous to external sync signals.

The upper 16 bits of the current phase increment is monitored by the phase increment register. The register tracks the current phase increment when the “hold” control is low and holds the last value when “hold” is high. The user may wish to monitor the phase increment in order to reinitialize the PLL after a loss of signal, or to determine when carrier lock has been achieved.

2.9 NCO

The PLL circuit generates a phase increment word which is used by the NCO to generate a sine/cosine sequence at the desired tuning frequency. The NCO circuit accumulates the phase and uses the upper 13 bits of the 32 bit accumulator to lookup 12 bit sines and cosines. A block diagram of the NCO circuit is shown in Figure 6.

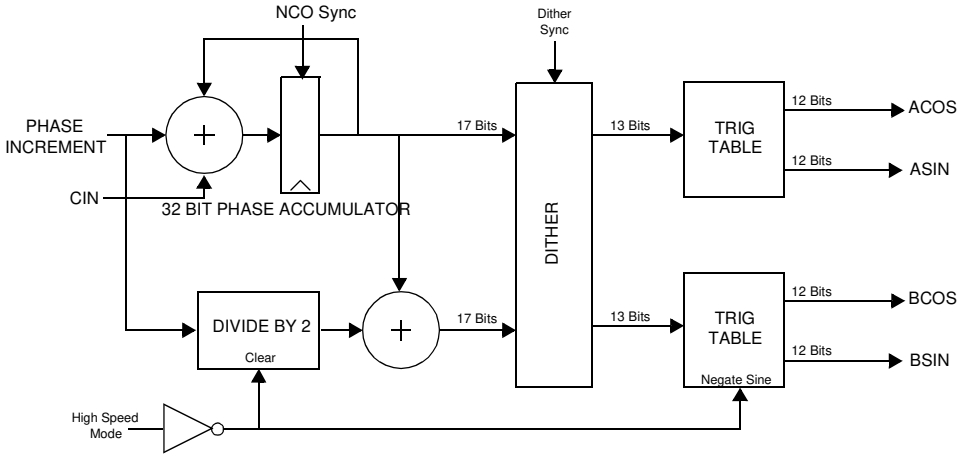


Figure 6. NCO CIRCUIT

The accumulator output plus one half the phase increment is used in the high speed mode[1] to look up the BCOS and BSIN values. This generates the proper “odd time” sine/cosine values needed in the high speed mode. The tuning range in the high speed mode is limited to +/- $F_{IN}/4$, where F_{IN} is thehigh speed input data rate. To tune to frequencies above $F_{IN}/4$, the user must negate the odd-time output samples (both I and Q). This mixes the output down by $F_{IN}/2$. For example, to mix down the frequency 0.3_{IN}, the user should set the tuning frequency to $+0.2F_{IN}$, and then negate the odd-time output data to give a final tuning of $(0.2F_{IN} - 0.5F_{IN}) = -0.3F_{IN}$.

The dither circuit adds a random value to the upper 17 bits of the accumulator output. The random number sequence is initialized to zero by the dither sync input. The dithering can be turned off by forcing the sync to be active. The BSIN output is negated if the high speed mode is not enabled.

2.10 SNAPSHOT RAM

The snapshot RAM is used to store blocks of 64 mixer and NCO outputs. The mixer outputs are the SI and SQ outputs shown in Figure 3. The NCO samples are the ACOS and ASIN values shown in Figure 3. The NCO samples are delayed to match the pipeline delay from the XI and XQ inputs to the SI and SQ

1. The high speed mode is the double rate real input mode, see Section 2.4

outputs. The snapshot can be programmed to store every sample, every other sample, every third sample, or every fourth sample. The rate control is primarily used when capturing samples of offset-QPSK data which is processed by the chip at twice the baud rate. Only every other sample of the offset-QPSK sample is of interest.

The snapshot can be triggered by the input syncs, the delayed input syncs, the sync counter's terminal count or the snap sync input. Once triggered, the snapshot start time can be delayed by up to 256 sample clocks, where the sample clock rate is dependant upon the snapshot rate control.

The snapshot RAM is a read only memory which is read using addresses 256 through 511 of the control interface. Addresses 256 through 319 read SI, addresses 320 through 383 read SQ, addresses 384 through 447 read ASIN, and addresses 448 through 511 read ACOS. The 12 bit values are sign extended to 16 bits in the control interface.

2.11 OUTPUT FORMAT

The chip has four 12 bit output ports labeled YA, YB, YC, and YD. Each port can be individually configured to output mixer results (I_{even}, Q_{even}, I_{odd}, Q_{odd}), or symbol and NCO samples. The symbol and NCO samples are the snapshot RAM inputs (SI, SQ, sine, cosine). The output selection is shown in Table 1 below:

Table 1: OUTPUT SELECTION

OUTPUT PORT	OUTPUT SELECT	
	0	1
YA	I_{even}	SI
YB	Q_{even}	SQ
YC	I_{odd}	cosine
YD	Q_{odd}	sine

The YA, YB, YC and YD outputs can be rounded to 12, 10 or 8 bits and can be masked to a desired number of bits through the use of four 12 bit mask words. The masks are bitwise ANDed with the output words to selectively clear the output bits.

Output enable controls are provided to individually turn off these outputs.

2.12 DATA DELAYS

The data delay through the chip in input clock cycles is shown in Table 2 below.

Table 2: DATA DELAYS

FROM	TO	DELAY	MODE
I, Q	SI, SQ	15	OUTSEL=1
I, Q	I, Q (even/odd)	13	OUTSEL=0

2.13 POWER DOWN MODES

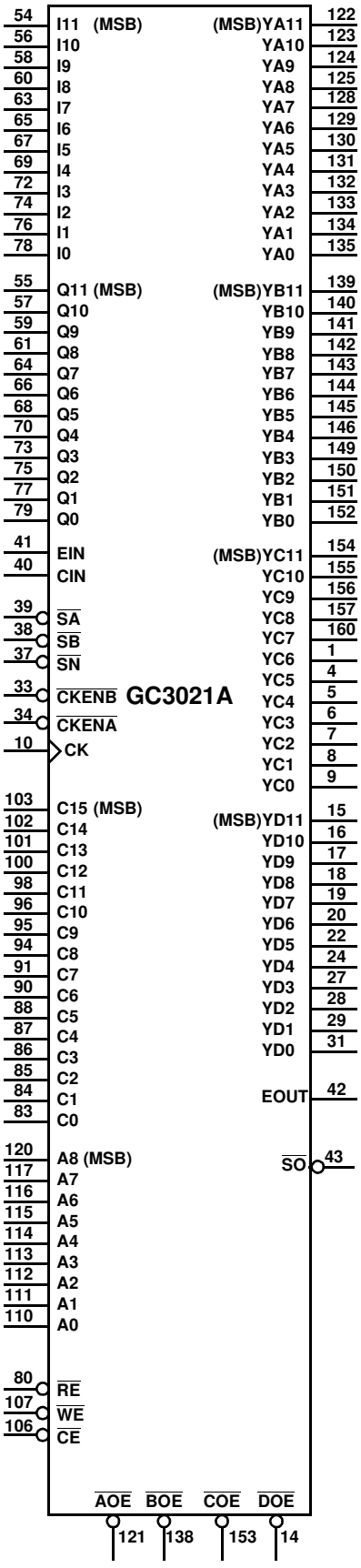
The chip has a power down and clock loss detect circuit. This circuit detects if the clock is absent long enough to cause dynamic storage nodes to lose state. If clock loss is detected, an internal reset state is entered to force the dynamic nodes to become static. The control registers are not reset and will retain their values, but any data values within the chip will be lost. When the clock returns to normal the chip will automatically return to normal. In the reset state the chip consumes only a small amount of standby power. The user can select whether this circuit is in the automatic clock-loss detect mode, is always on (power down mode), or is disabled (the clock reset never kicks in) using the POWER_DOWN control bits in address 1.

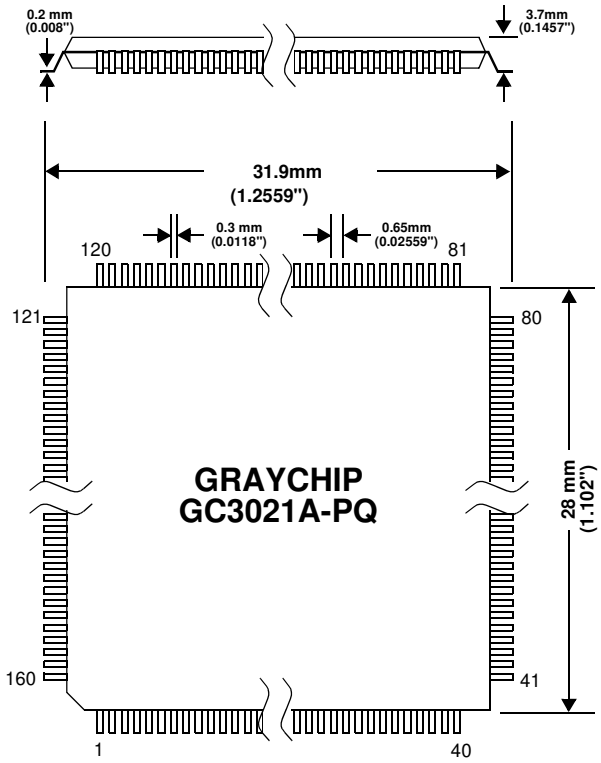
NOTE: The chip is in the power down mode when power is applied, and must be enabled by setting the power down mode to "2" in register 1.

2.14 DIAGNOSTICS

The sync counter can be used as an input sync and data source in order to perform diagnostics. The diagnostic outputs are captured in the snapshot RAM and compared with predicted results. The whole chip except for the I/O pads, the high speed input circuit and the output format circuit can be checked this way. Section 6.6 tabulates the diagnostic configurations and their expected snapshot outputs.

3.0 PACKAGING





160 PIN PLASTIC QUAD FLAT PACK CHIP CARRIER

VCC PINS: 3,12,13,23,26,32,36,44,47, 48,81,89,93,97,104,108,118,126,136,147,158

GND PINS: 2,11,21,25,30,35,45,46,82,92,99,105,109,119,127,137,148,159

UNUSED PINS: 53, 62, 71, 49, 50, 51, 52

NOTE: 0.01 to 0.1 μf DECOUPLING CAPACITORS SHOULD BE PLACED AS CLOSE AS POSSIBLE TO THE MIDDLE OF EACH SIDE OF THE CHIP

3.1 PIN DESCRIPTIONS

SIGNAL	DESCRIPTION
I[0:11]	**IN-PHASE INPUT DATA.** *Active high* The 12 bit two's complement input samples for the I half of the complex input. New samples are clocked into the chip on the rising edge of the clock.
Q[0:11]	**QUADRATURE INPUT DATA.** *Active high* The 12 bit two's complement input samples for the Q-half of the complex input. New samples are clocked into the chip on the rising edge of the clock.
CIN	**NCO CARRY INPUT.** *Active high* The carry input to the phase accumulator in the NCO. The CIN input can be used to increase the tuning resolution of the NCO. This signal is clocked into the chip on the rising edge of the clock. The CIN input is cleared by the chip during diagnostics.
EIN	**PHASE ERROR INPUT.** *Active high* This input can be used as the error input into the PLL circuit. This signal is clocked into the chip on the rising edge of the clock.
$\overline{\text{SA}}$,$\overline{\text{SB}}$	**SYNC INPUTS**. *Active low* The sync inputs to the chip. All timers, accumulators, and control counters are, or can be, synchronized to these syncs. The syncs are clocked into the chip on the rising edge of the clock.
$\overline{\text{SN}}$	**SNAPSHOT SYNC**. *Active low* The snapshot sync is provided to synchronously start the data snapshot. This signal is clocked into the chip on the rising edge of the clock.
CK	**CLOCK INPUT.** *Active high* The clock input to the chip. The **I**, **Q**, **$\overline{\text{SA}}$**, **$\overline{\text{SB}}$**, **$\overline{\text{SN}}$**, **$\overline{\text{CKENA}}$**, **$\overline{\text{CKENB}}$**, **EIN** and **CIN** signals are clocked into the chip on the rising edge of this clock. The **YA**, **YB**, **YC**, **YD**, **EOUT** and **$\overline{\text{SO}}$** signals are clocked out on the rising edge of this clock.
$\overline{\text{CKENA}}$, $\overline{\text{CKENB}}$	**CLOCK ENABLE INPUTS.** *Active low* The clock enable inputs to the chip. These signals are gated with **CK** to generate the chip's internal clock. **$\overline{\text{CKENA}}$** and **$\overline{\text{CKENB}}$** are clocked into the chip on the rising edge of **CK** and will enable or disable the following clock edge. A low level on both **$\overline{\text{CKENA}}$** and **$\overline{\text{CKENB}}$** enables the clock edge.
YA[0:11] **YB[0:11]** **YC[0:11]** **YD[0:11]**	**YA OUTPUT DATA**. *Active high* **YB OUTPUT DATA**. *Active high* **YC OUTPUT DATA**. *Active high* **YD OUTPUT DATA**. *Active high* These pins output the complex mixer or symbol outputs. The bits are clocked out on the rising edge of the clock.
$\overline{\text{AOE}}$,$\overline{\text{BOE}}$,$\overline{\text{COE}}$,$\overline{\text{DOE}}$	**OUTPUT ENABLES**. *Active low* The **YA, YB, YC** and **YD** output pins are put into a high impedance state when these pins are high. **$\overline{\text{AOE}}$** controls the **YA** output pins. **$\overline{\text{BOE}}$** controls the **YB** output pins. **$\overline{\text{COE}}$** controls the **YC** output pins. **$\overline{\text{DOE}}$** controls the **YD** output pins.

EOUT	**PHASE ERROR OUT**. *Active high* The phase error RAM output is clocked out of the chip on this pin. This signal is made available mostly for diagnostic purposes.
$\overline{\text{SO}}$	**SYNC OUT**. *Active low* This signal is either one of the input syncs, the one shot sync **$\overline{\text{OS}}$**, or the internal counter's terminal count strobe **$\overline{\text{TC}}$**.
C[0:15]	**CONTROL DATA I/O BUS**. *Active high* This is the 16 bit control data I/O bus. Control register contents are loaded into the chip or read from the chip through these pins. The chip will only drive these pins when **$\overline{\text{CE}}$** and **$\overline{\text{RE}}$** are low and **$\overline{\text{WE}}$** is high.
A[0:8]	**CONTROL ADDRESS BUS**. *Active high* These pins are used to address the control registers, phase error RAM and the snapram memory within the chip.
$\overline{\text{WE}}$, **$\overline{\text{RE}}$**	**READ/$\overline{\text{WRITE}}$ CONTROL**. *Active low* These pin determines if the control bus cycle is a read or write operation.
$\overline{\text{CE}}$	**CHIP ENABLE**. *Active low* This control strobe enables the chip for read or write operations.
VCC	**SUPPLY VOLTAGE.** *Fixed voltage* The power supply pins.
GND	**CHIP GROUND.** *Fixed voltage* The power supply ground pins.

4.0 CONTROL REGISTERS

The chip is configured and controlled through the use of 14 sixteen bit control registers. These registers are accessed for reading or writing using the control bus pins (**$\overline{\text{CS}}$**, **R/$\overline{\text{W}}$**, **A[0:8]**, and **C[0:15]**) described in the previous section. The register names and their addresses are:

ADDRESS	NAME	ADDRESS	NAME
0	MODE_REG	8	OUTPUT_REGA
1	SYNC_REG0	9	OUTPUT_REGB
2	SYNC_REG1	10	OUTPUT_REGC
3	DELAY_REG	11	OUTPUT_REGD
4	COUNTER_REG0	12	SNAP_REG
5	PLL_REG	13	PHASE_REG
6	FREQ_REG0	14	ONE_SHOT
7	FREQ_REG1	15	TEST_OUT
16	DC_I_IN		
17	DC_Q_IN		
18	DC_I_OUT		
19	DC_Q_OUT		

20 to 255	unused
256 to 511	Snapshot memory (read only)
256 to 511	Phase Error memory (write only)

The DC offset registers contain two's complement values. Only the 12 LSBs are used.

The following sections describe each of these registers. The type of each register bit is either R or R/W indicating whether the bit is read only or read/write. All bits are active high.

Suggested default settings for using the chip in carrier removal applications is given for each register.

4.1 MODE CONTROL REGISTER

This register contains the mode control bits. The suggested default value is 5280 (HEX).

ADDRESS 0: MODE_REG

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSBs)	R/W	INPUT[0:1]	This two bit field controls the input data selection. The input modes are: INPUT DESCRIPTION 0 Complex data input 1 High speed real data input 2 Diagnostic ramp input 3 Zero input
2-6	R/W	-	unused
7	R/W	MIXER_ROUND	Round the mixer multiplier products to 12 bits. The products are truncated to 12 bits if this control is low.
8	R/W	ADDER_CLEAR	Clears one input to the adder in the mixer circuit to allow the I_{even} and Q_{even} outputs to be routed to the symbol offset circuitry. See Section 2.5.
9	R/W	2X_GAIN	Enables the 2X gain circuit in the mixer circuit.
10	R/W	OFFSET	Delays the I sample in the symbol offset circuit by one clock cycle relative to the Q sample.
11	R/W	OFFSET_HOLD	Samples and holds every other I,Q pair in the symbol offset circuit. The OFFSET_SYNC mode (See Section 4.2) determines how the sample and hold timing is synchronized to the input data.
12	R/W	QMAP_ENABLE	Enables the quadrant map mode. This mode maps the I,Q pairs into the first quadrant for phase error lookup when this mode is selected. The error is then mapped back to the correct quadrant after it is looked up in the phase error memory.
13	R/W	QMAP_ROUND	Round instead of truncate the I,Q samples in the phase error circuit. If QMAP_ENABLE is set the values are rounded into the 7 MSBs, otherwise they are rounded to the 6 MSB.
14	R/W	QMAP_INVERT	Convert negative numbers to positive numbers in the Qmap mode by inverting the data bits (1's complement negation) rather than negating them.
15	R/W	NCO_MODE	Turns on the high speed NCO mode. Must be high for the high speed double rate input mode, low otherwise.

4.2 SYNC CONTROL REGISTERS

Control registers SYNC_REG0 and SYNC_REG1 determine how the circuits within the chip are synchronized. Each circuit which requires synchronization can be configured to be synchronized to the sync inputs **(SA** and **SB**), to the delayed versions of these syncs (**DSA** and **DSB**), to the terminal count of the internal counter (**TC**), or to the one-shot strobe (**OS**). The sync to each circuit can also be set to be always on or always off. Each circuit is given a three bit sync mode control which is defined as:

Table 3: SYNC MODES

MODE	SYNC DESCRIPTION
0	"0" (never asserted)
1	SA
2	SB
3	DSA
4	DSB
5	TC
6	OS
7	"1" (always asserted)

NOTE: the internal syncs are active high. The **$\overline{\text{SA}}$** and **$\overline{\text{SB}}$** inputs have been inverted to be the active high syncs **SA** and **SB**.

The suggested default setting for SYNC_REG0 is to sync everything to SA, value = 0249 (HEX).

ADDRESS 1: SYNC_REG0

BIT	TYPE	NAME	DESCRIPTION
0-2 (LSBs)	R/W	COUNT_SYNC	The counter sync selection
3-5	R/W	OUTPUT_SYNC	The selected sync is inverted and output on the **$\overline{\text{SO}}$** pin.
6-8	R/W	OFFSET_SYNC	The symbol offset sync.
9-11	R/W	SNAP_SYNC	The snapshot memory can be triggered by this sync.
12	R/W	-	unused
13	R/W	USE_CLK_EN	The clock enables **$\overline{\text{CKENA}}$** and **$\overline{\text{CKENB}}$** are ignored when this bit is low.
14,15	R/W	POWER_DOWN	These bits control the power down and keep alive circuit. POWER_DOWN — MODE 0,1 — Power down 2 — Clock loss detect mode 3 — Clock loss detect off

The USE_CLK_EN and POWER_DOWN bits initialize to zero upon power up. This puts the chip in the power down mode to prevent a current surge if there is no clock provided. See Section 2.13 for details.

The suggested default value for SYNC_REG1 is 7DF7 (HEX) which is to always sync AB_SYNC, FREQ_SYNC and DITHER_SYNC (turns dithering off) and to sync PLL_SYNC and NCO_SYNC with the oneshot strobe.

ADDRESS 2: SYNC_REG1

BIT	TYPE	NAME	DESCRIPTION
0-2 (LSBs)	R/W	AB_SYNC	The PLL circuit accepts new A and B values when the sync is asserted.
3-5	R/W	PLL_SYNC	The PLL accumulator is cleared by this sync.
6-8	R/W	FREQ_SYNC	The PLL accepts the new FREQ value from the FREQ registers when this sync is asserted.
9-11	R/W	NCO_SYNC	The NCO accumulator is cleared by this sync.
12-14	R/W	DITHER_SYNC	The dither value circuit is cleared by this sync.
15 (MSB)	R/W	-	unused

4.3 DELAY CONTROL REGISTER

The **DSA** and **DSB** syncs are generated by delaying the **SA** and **SB** sync inputs by (2+DELAY) clocks where DELAY ranges from 0 to 255. The suggested default is zero.

ADDRESS 3: DELAY_REG

BIT	TYPE	NAME	DESCRIPTION
0-7 (LSBs)	R/W	DELAY_A	The DELAY value for **DSA**.
8-15 (MSBs)	R/W	DELAY_B	The DELAY value for **DSB**.

4.4 COUNTER CONTROL REGISTER

The internal counter counts in cycles of 16*(COUNT+1) clocks by counting down from (16*COUNT+15) to zero and starting over again. The counter emits a terminal count (TC) each time it reaches zero. The suggested default is 00FF (HEX) which sets a counter cycle of 4096.

ADDRESS 4: COUNT_REG

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	COUNT	The counter period is 16*(COUNT+1) clocks.

4.5 PLL CONTROL REGISTER

The phase lock loop (PLL) phase hold control and filter coefficients are stored in this register. The suggested default is 028A (HEX) which sets A=10 and B=20 for acquisition, and 038e (HEX) which sets A=14 and B=28 for tracking.

ADDRESS 5: PLL_REG

BIT	TYPE	NAME	DESCRIPTION
0-4	R/W	A[0:4]	The 5 bit "A" coefficient. See Figure 5. The phase error is multiplied by 2^{-A} for A equal to 1 through 31, and is multiplied by 0 for A equal to 0.
5-9	R/W	B[0:4]	The 5 bit "B" coefficient. See Figure 5. The phase error is multiplied by 2^{-B} for B equal to 1 through 31, and is multiplied by 0 for B equal to 0.
10	R/W	EXT_ERROR	Use the **EIN** input as the error input to the PLL circuit. **EIN** = 0 adds to the phase, **EIN** = 1 subtracts.
11-14	R/W	-	unused
15 (MSB)	R/W	PHASE_HOLD	The phase register tracks the value of the phase increment when this bit is low and holds the last value when this bit is high.

The A and B coefficients stored in this register are not used until the AB_SYNC is asserted as described in Section 4.2.

4.6 FREQUENCY WORD REGISTERS

Registers 6 and 7 contain the 32 bit frequency tuning word. The frequency word is added into the PLL output as shown in Figure 4. Bit 0 is the LSB, bit 31 is the MSB. The suggested default is zero.

ADDRESS 6: FREQ_REG0

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	FREQ[0:15]	16 LSBs of the frequency word

ADDRESS 7: FREQ_REG1

BIT	TYPE	NAME	DESCRIPTION
0-15	R/W	FREQ[15:31]	16 MSBs of the frequency word

The tuning frequency is specified using the formula:

$$\text{FREQ} = \frac{\text{Frequency}}{\text{Clock Rate}} 2^{32}$$

where "Frequency" is the desired tuning frequency, and "clock rate" is the chip's clock rate. The FREQ value stored in these registers are transferred to the PLL circuit when the FREQ_SYNC is asserted as described in Section 4.2.

4.7 OUTPUT CONTROL REGISTERS

Registers 8, 9, 10 and 11 contain the four output format control words. Each register is identical. OUTPUT_REGA controls output YA, OUTPUT_REGB controls output YB, OUTPUT_REGC controls output YC and OUTPUT_REGD controls output YD. The suggested default is 1FFF.

ADDRESS 8: OUTPUT_REGA
ADDRESS 9: OUTPUT_REGB
ADDRESS 10: OUTPUT_REGC
ADDRESS 11: OUTPUT_REGD

BIT	TYPE	NAME	DESCRIPTION
0-11	R/W	MASK	12 Bit output mask. MASK is bitwise anded with the output sample. Bit 0 is the LSB, bit 11 is the MSB.
12	R/W	OUTPUT_SEL	Selects which signal is output on this port. See Table 2 in Section 2.11.
13	R/W	RND_8	Round to 8 bits
14	R/W	RND_10	Round to 10 bits
15	R/W	-	Unused

The RND_8 and RND_10 controls are used to round the 12 bit output values to 8 or 10 bits. Only one control should be high.

4.8 SNAPSHOT CONTROL REGISTER

Registers 12 controls the snapshot memory. The suggested default is 0002 (HEX).

ADDRESS 12: SNAP_REG

BIT	TYPE	NAME	DESCRIPTION
0,1 (LSB)	R/W	TRIGGER	This control sets the trigger condition which will start a snapshot once the ARMED bit is set. The trigger conditions are to start: TRIGGER DESCRIPTION 0 immediately, 1 when the **$\overline{SN}$** strobe is received, 2 when the SNAP_SYNC is received (See Section 4.2), 3 never
2	R/W	ARMED	The user sets this bit to arm the snapshot memory so that it will start on the next trigger condition. The chip clears this bit when the trigger occurs.
3	R/W	DONE	This bit goes high when the snapshot is complete.
4,5	R/W	SNAP_RATE	Determines the rate at which samples are stored according to: SNAP_RATE DESCRIPTION 0 every clock, full rate samples 1 every other clock, half rate samples 2 every 3rd clock, third rate samples 3 every 4th clock, quarter rate samples.
6,7	R/W	-	unused
8-15 (MSB)	R/W	SNAP_DELAY	Delay from snapshot trigger until the start of snapshot. The delay is: SNAP_DELAY*(SNAP_RATE+1) clock cycles where SNAP_DELAY ranges from 0 to 255.

4.9 PHASE REGISTER

Register 13 is a read only register used to monitor the upper 16 bits of the NCO's phase increment. See PHASE_HOLD in Section 4.5.

4.10 ONE SHOT ADDRESS

The one shot pulse is generated on the **$\overline{OS}$** pin by writing to address 14. This is a write-only address. The data written to it is irrelevant.

4.11 TEST OUTPUT REGISTER

Register address 15 is a read only port used to monitor the powerdown and clock loss modes. Bit 0 is low if the chip is in power down, and bit 1 is low if clock loss has been detected. Normally both bits will read as 1.

5.0 SPECIFICATIONS

5.1 ABSOLUTE MAXIMUM RATINGS

Table 4: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	-0.3	4.0	V	
Input voltage (undershoot and overshoot)	V_{IN}	-0.7	V_{CC}+0.7	V	
Storage Temperature	T_{STG}	-65	150	°C	
Lead Soldering Temperature (10 seconds)			300	°C	
Clock Rate	F_{CK}	1		KHz	1

Notes:

1. Below 1 KHz the clock loss detect circuit may power down the chip. If the clock loss detect circuit is disabled (address 1, bits 14 and 15) and the clock is stopped, the chip may draw up to one Amp of power supply current for approximately 10 seconds. After 10 seconds the current will go down to below 50 mAmps.

5.2 RECOMMENDED OPERATING CONDITIONS

Table 5: Recommended Operating Conditions

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
DC Supply Voltage	V_{CC}	3.0	3.6	V	
Temperature Ambient, no air flow	T_A	-40	+85	°C	1
Junction Temperature	T_J		125	°C	1

Notes:

1. Thermal management is required to keep T_J below MAX for full rate operation. See Table 3 below.

5.3 THERMAL CHARACTERISTICS

Table 6: Thermal Data

THERMAL CONDUCTIVITY	SYMBOL	GC3021A-PQ	UNITS
		0.5 Watts	
Theta Junction to Ambient	θja	30	°C/W
Theta Junction to Case	θjc	10	°C/W

Note: Air flow will reduce **θja** and is highly recommended.

5.4 DC CHARACTERISTICS

All parameters are industrial temperature range of 0 to 85 ^{o}C ambient unless noted.:

Table 7: DC Operating Conditions

PARAMETER	SYMBOL	Vcc = 3.3V		UNITS	NOTES
		MIN	MAX		
Voltage input low	V_{IL}		0.8	V	1
Voltage input high	V_{IH}	2.0		V	2
Input current (V_{IN} = 0V)	I_{IN}	Typical +/- 50		uA	2
Voltage output low (I_{OL} = 2mA)	V_{OL}		0.5	V	2
Voltage output high (I_{OH} = -2mA)	V_{OH}	2.4	3.3	V	2
Data input capacitance (All inputs except **CK** and **C[0:15]**)	C_{IN}	Typical 4		pF	1
Clock input capacitance (**CK** input)	C_{CK}	Typical 10		pF	1
Control data capacitance (**C[0:7]** I/O pins)	C_{CON}	Typical 6		pF	1

Notes:

1. Controlled by design and process and not directly tested. Verified on initial parts evaluation.
2. Each part is tested at 85^{o}C for the given specification.