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## FEATURES

- **Input Voltage Range: 6V to 100V**
- **Duty Mode Control Regulates an Isolated Output without an Opto**
- High Efficiency Synchronous Control
- Short-Circuit (Hiccup Mode) Overcurrent Protection
- Programmable OVLO and UVLO with Hysteresis
- Programmable Frequency (100kHz to 500kHz)
- Synchronizable to an External Clock
- Positive or Negative Polarity Output Voltage Feedback with a Single FBX Pin
- Programmable Soft-Start
- Low Shutdown Current < 1μA
- Available in FE20 TSSOP with HV Pin Spacing

## APPLICATIONS

- Industrial, Automotive and Military Systems
- 48V Telecommunication Isolated Power Supplies
- Isolated and Nonisolated DC/DC Converters

## DESCRIPTION

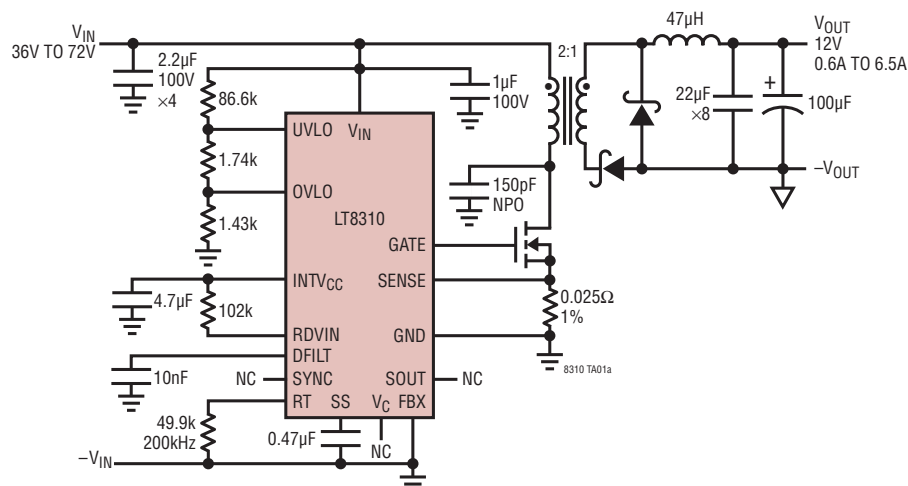
The **LT<sup>®</sup>8310** is a simple-to-use resonant reset forward converter controller that drives the gate of a low side N-channel MOSFET from an internally regulated 10V supply. The LT8310 features duty mode control that generates a stable, regulated, isolated output using a single power transformer. With the addition of output voltage feedback, via opto-coupler (isolated) or directly wired (nonisolated), current mode regulation is activated, improving output accuracy and load response. The flexibility to choose transformer turns ratio makes high step-down or step-up ratios possible without operating at duty cycle extremes.

The user can program the switching frequency from 100kHz to 500kHz to optimize efficiency, performance or external component size. A synchronous output is available for controlling secondary side synchronous rectification to improve efficiency. User programmable protection features include monitors on input voltage (UVLO and OVLO) and switch current (overcurrent limit). The LT8310 soft-start feature helps protect the transformer from flux saturation.

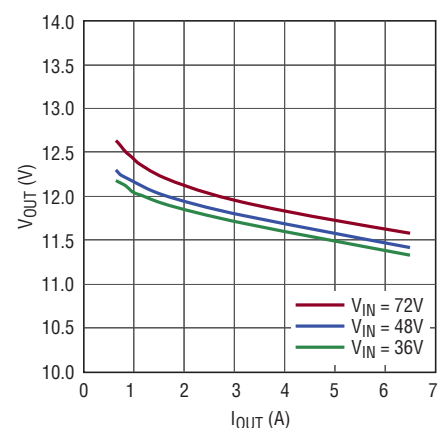
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## TYPICAL APPLICATION

**78 Watt Isolated Forward Converter, ±8% V<sub>OUT</sub>**



**Output Voltage Load Regulation**



8310 TA01b

# LT8310

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

$V_{IN}$ , UVLO .....	100V
INTV <sub>CC</sub> , RDVIN, SYNC .....	20V
DFILT.....	8V
$V_C$ , OVLO, SS, RT.....	3V
FBX .....	-3V to 3V
SENSE.....	-0.3V to 0.3V
GATE, SOUT .....	Note 3

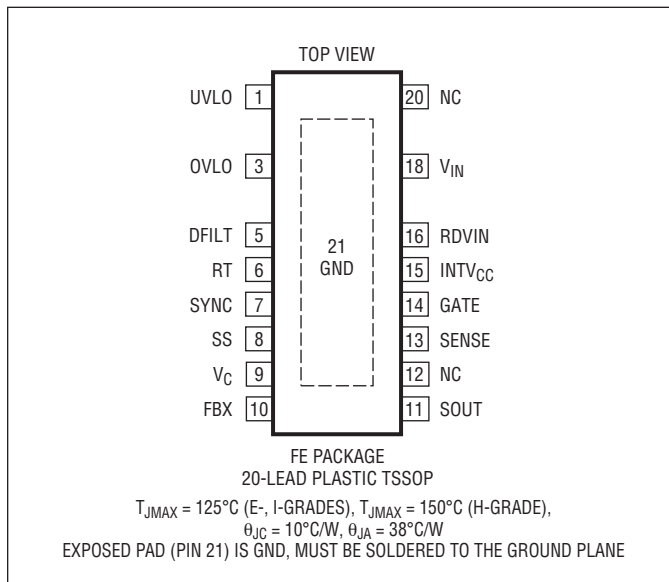
Operating Junction Temperature Range (Notes 4, 5)

LT8310E.....	-40°C to 125°C
LT8310I.....	-40°C to 125°C
LT8310H .....	-40°C to 150°C
LT8310MP .....	-55°C to 150°C

Storage Temperature Range .....

Lead Temperature Range (Soldering, 10 sec).....

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8310EFE#PBF	LT8310EFE#TRPBF	LT8310FE	20-Lead Plastic TSSOP	-40°C to 125°C
LT8310IFE#PBF	LT8310IFE#TRPBF	LT8310FE	20-Lead Plastic TSSOP	-40°C to 125°C
LT8310HFE#PBF	LT8310HFE#TRPBF	LT8310FE	20-Lead Plastic TSSOP	-40°C to 150°C
LT8310MPFE#PBF	LT8310MPFE#TRPBF	LT8310FE	20-Lead Plastic TSSOP	-55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>



**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 24\text{V}$ ,  $UVLO = 24\text{V}$ ,  $OVLO = 0\text{V}$ ,  $SYNC = 0\text{V}$ ,  $SENSE = 0\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Supply</b>						
Operating Input Voltage		●	6		100	V
$V_{IN}$ Supply Current in Shutdown	UVLO = 0V UVLO = 1.15V			0.3 5	1 7	$\mu\text{A}$ $\mu\text{A}$
$V_{IN}$ Operating Current	Not Switching			3.8	4.6	mA
<b>UVLO</b>						
UVLO Threshold Voltage	UVLO Falling	●	1.196	1.220	1.250	V
UVLO Threshold Hysteresis	UVLO Rising			40		mV
UVLO Low Quiescent Current Threshold	$I_{VIN} < 1\mu\text{A}$	●	0.36	0.62	0.85	V
UVLO Pin Input Current	UVLO = 1.15V UVLO = 1.30V		4.5	5.7 20	6.8 150	$\mu\text{A}$ nA
<b>OVLO</b>						
OVLO Threshold Voltage	OVLO Rising	●	1.225	1.250	1.275	V
OVLO Threshold Hysteresis	OVLO Falling			-33		mV
OVLO Pin Input Current	OVLO = 1.17V OVLO = 1.32V			10 120	150 400	nA nA
<b>Linear Regulator</b>						
INTV <sub>CC</sub> Regulation Voltage	$I_{INTVCC} = 0\text{mA to } 20\text{mA}$	●	9.6	10.0	10.3	V
Regulator Dropout Voltage ( $V_{IN} - \text{INTV}_{CC}$ )	$V_{IN} = 9\text{V}$ , $I_{INTVCC} = 20\text{mA}$			600		mV
INTV <sub>CC</sub> Undervoltage Lockout Threshold	INTV <sub>CC</sub> Falling		4.60	4.75	4.90	V
INTV <sub>CC</sub> Undervoltage Hysteresis				0.45		V
INTV <sub>CC</sub> Overvoltage Lockout Threshold	INTV <sub>CC</sub> Rising		17.0	17.4	17.8	V
INTV <sub>CC</sub> Overvoltage Hysteresis				-0.65		V
INTV <sub>CC</sub> Current Limit	$V_{IN} = 12\text{V}$	●	25	33	39	mA
INTV <sub>CC</sub> Current in Shutdown	UVLO = 0V, INTV <sub>CC</sub> = 10V			125		$\mu\text{A}$
INTV <sub>CC</sub> Line Regulation	$10.8\text{V} \leq V_{IN} \leq 100\text{V}$			0.001	0.01	%/V
INTV <sub>CC</sub> Load Regulation	$0\text{mA} \leq I_{INTVCC} \leq 20\text{mA}$		-3.0	-0.4		%
<b>Duty Cycle Control</b>						
Minimum GATE On-Time				190		ns
Maximum Duty Cycle	$V_{IN} = 12\text{V}$	●	75	78	82	%
RDVIN Pin Input Current		●	19.7	20.0	20.3	$\mu\text{A}$
Duty Control Transconductance (Note 6) ( $\Delta I_{DFILT} / \Delta V_{SET}$ )	$V_{SET} = 1\text{V}$		22.5	25.0	27.5	$\mu\text{A/V}$
Duty Mode Control Gain (Notes 6, 7), Gain = $V_{IN} / V_{SET}$ at $I_{DFILT} = 0\mu\text{A}$	$V_{SET} = 0.5\text{V to } 6\text{V}$	●	11.76	12.00	12.24	V/V
Duty Cycle Foldback, Foldback = Duty at $V_{SS} = 1.15\text{V} / \text{Duty (Nom)}$	$SS = 1.15\text{V}$			0.14		%/%
<b>Error Amplifier</b>						
FBX Error Amp Reference Voltage	FBX > 0V FBX < 0V	● ●	1.568 -0.820	1.600 -0.800	1.632 -0.780	V V
FBX Overvoltage Threshold	FBX > 0V FBX < 0V		6 5.5	7.5 7.5	9 10	% %

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 24\text{V}$ ,  $UVLO = 24\text{V}$ ,  $OVLO = 0\text{V}$ ,  $SYNC = 0\text{V}$ ,  $SENSE = 0\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Feedback Mode Threshold Voltage (Below = Duty Mode/Above = Current Mode)	FBX > 0V	0.2	0.3	0.4	V
	FBX < 0V	-0.3	-0.2	-0.13	V
Feedback Mode Threshold Hysteresis	FBX > 0V		20		mV
	FBX < 0V		20		mV
FBX Pin Input Current	FBX = 1.6V		70	100	nA
	FBX = -0.8V	-100	0	100	nA
Transconductance ( $\Delta I_{VC}/\Delta V_{FBX}$ )			250		$\mu\text{A}/\text{V}$
$V_C$ Source Current	$V_{FBX} = 0\text{V}$ , $V_{VC} = 1.3\text{V}$		-14		$\mu\text{A}$
$V_C$ Sink Current	$V_{FBX} = 1.7\text{V}$ , $V_{VC} = 1.3\text{V}$		13		$\mu\text{A}$
	$V_{FBX} = -0.85\text{V}$ , $V_{VC} = 1.3\text{V}$		11		$\mu\text{A}$
$V_C$ Pin Output Impedance			3.3		$\text{M}\Omega$
$V_C$ Pin Current Mode Gain			5		V/V
<b>Gate Driver</b>					
GATE Rise Time	$C_{\text{GATE}} = 3.3\text{nF}$		30		ns
GATE Fall Time	$C_{\text{GATE}} = 3.3\text{nF}$		27		ns
GATE Low Voltage				0.05	V
GATE High Voltage		$\text{INTV}_{\text{CC}}$ - 0.05			V
<b>Current Sense</b>					
SENSE Pin Maximum Current Threshold		● 115	125	135	mV
SENSE Pin Input Current			-200		$\mu\text{A}$
<b>Oscillator</b>					
Switching Frequency	$R_T = 100\text{k}$ to GND, $V_{\text{SS}} \geq 2.9\text{V}$	● 95	100	105	kHz
	$R_T = 33.2\text{k}$ to GND, $V_{\text{SS}} \geq 2.9\text{V}$	● 285	300	315	kHz
	$R_T = 20\text{k}$ to GND, $V_{\text{SS}} \geq 2.9\text{V}$	● 475	500	525	kHz
Switching Frequency Line Regulation	$V_{\text{IN}} = 6\text{V}$ to 100V		0.01		%
RT Pin Voltage	$V_{\text{SS}} = 3\text{V}$	0.8	1.0	1.3	V
Frequency Foldback Foldback = $(f_{\text{OSC}}$ at $V_{\text{SS}} = 1.15\text{V})/f_{\text{OSC(NOM)}}$	$V_{\text{SS}} = 1.15\text{V}$	0.15	0.20	0.25	Hz/Hz
SYNC Pin Input High Threshold Voltage		●		2.00	V
SYNC Pin Input Low Threshold Voltage		● 1.00			V
SYNC Pin Input Resistance	SYNC = 2V		200		$\text{k}\Omega$
SYNC Frequency Operating Range	$R_T = 33.2\text{k}$	● 260		400	kHz
Minimum SYNC High Setup Time	$f_{\text{SW}} = 400\text{kHz}$	●		250	ns
Minimum SYNC Low Hold Time	$f_{\text{SW}} = 400\text{kHz}$	●		250	ns
<b>SOUT Driver</b>					
SOUT Rise Time	$C_{\text{SOUT}} = 1\text{nF}$		20		ns
SOUT Fall Time	$C_{\text{SOUT}} = 1\text{nF}$		25		ns
SOUT Low Voltage				0.05	V
SOUT High Voltage		$\text{INTV}_{\text{CC}}$ - 0.05			V

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = 24\text{V}$ ,  $UVLO = 24\text{V}$ ,  $OVLO = 0\text{V}$ ,  $SYNC = 0\text{V}$ ,  $SENSE = 0\text{V}$ , unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SOUT-to-GATE Delay ( $t_{PRE}$ )	SOUT Falling to GATE Rising (Note 8)	●	190	240	300	ns
GATE-to-SOUT Delay ( $t_{POST}$ )	GATE Falling to SOUT Rising (Note 8)	●	0	12	25	ns
<b>Soft-Start</b>						
SS Active Switching Level (GATE Switches)			0.95	1.00	1.05	V
SS Frequency Foldback Complete	$f_{OSC}$ within Specified Limits	●			2.5	V
SS Pin Current (Note 8)	Soft-Up	●	-60	-50	-40	$\mu\text{A}$
	Slow Wake	●	-6	-5	-4	$\mu\text{A}$
	Hard-Down, $V_{SS} = 0.4\text{V}$			6		$\text{mA}$
SS Reset Threshold Voltage				0.27		V

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltages are relative to GND unless otherwise noted. All pin currents are defined positive into the pin unless otherwise noted.

**Note 3:** Do not apply a positive or negative voltage or current source to the GATE or SOUT pins, otherwise permanent damage may occur.

**Note 4:** The LT8310E is guaranteed to meet performance specifications from the  $0^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8310I is guaranteed over the full  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range. The LT8310H is guaranteed over the full  $-40^\circ\text{C}$  to  $150^\circ\text{C}$  operating junction temperature range. The LT8310MP is guaranteed over the full  $-55^\circ\text{C}$  to  $150^\circ\text{C}$  operating junction temperature range. Operating lifetime is derated at junction temperatures greater than  $125^\circ\text{C}$ .

**Note 5:** The LT8310 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum junction temperature may impair device reliability.

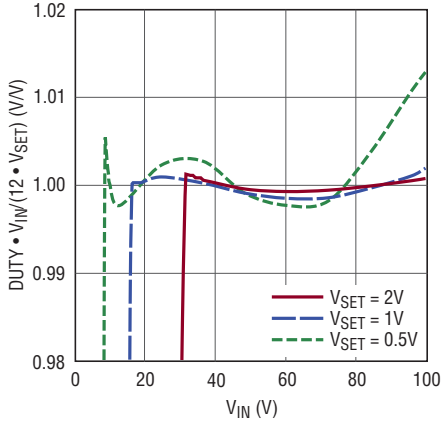
**Note 6:**  $V_{SET} = V_{INTVCC} - V_{RDVIN}$ .

**Note 7:** Line regulation in duty mode control applications is constrained by the accuracy of the RDVIN pin input current, the duty mode control gain, and the external set resistor,  $R_{SET}$ .  $R_{SET}$  should be specified to 1% or better.

**Note 8:** See the Timing Diagrams section.

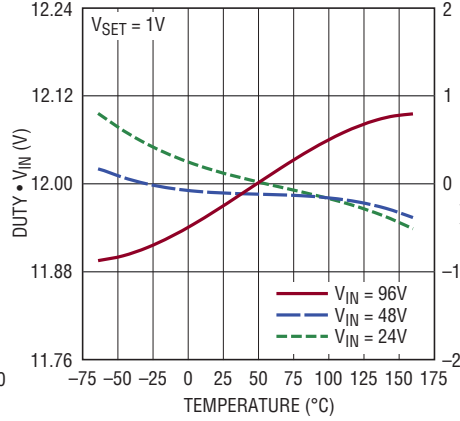
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**DUTY •  $V_{IN}$  Line Regulation (Normalized)**



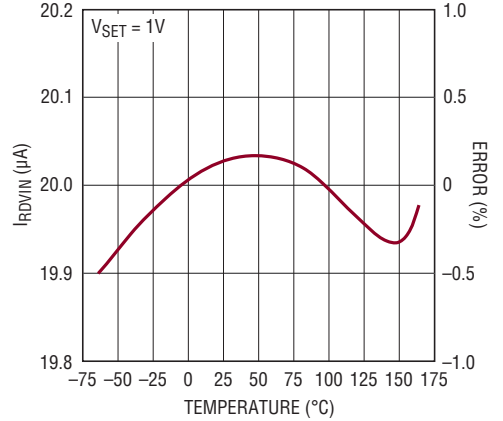
8310 G01

**Duty •  $V_{IN}$  Temperature Regulation**



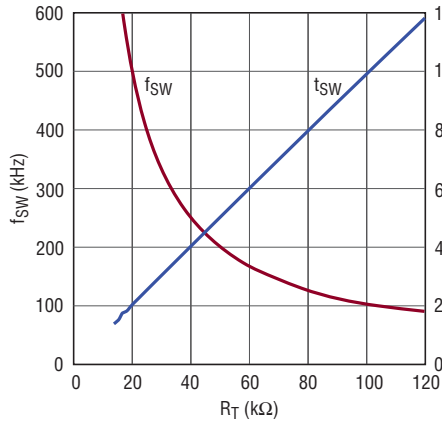
8310 G02

**Duty Set Current vs Temperature**



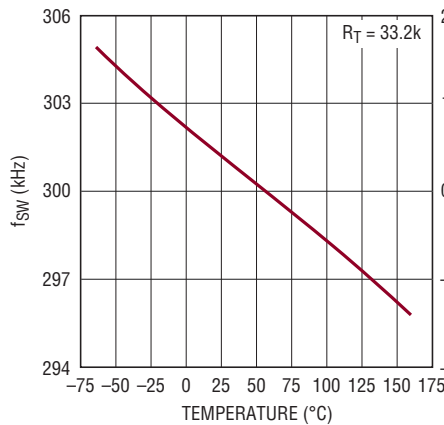
8310 G03

**Switching Frequency and (Period) vs Programming Resistance**



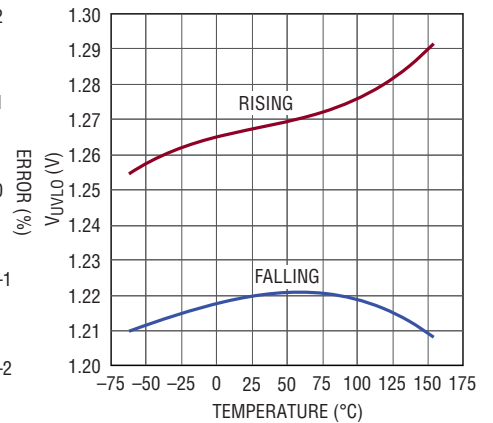
8310 G04

**Switching Frequency vs Temperature**



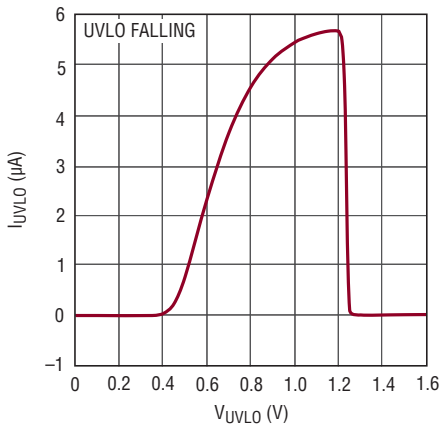
8310 G05

**UVLO Threshold vs Temperature**



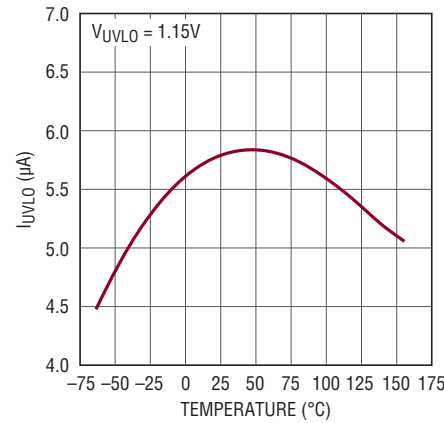
8310 G06

**UVLO Hysteresis Current vs UVLO Voltage**



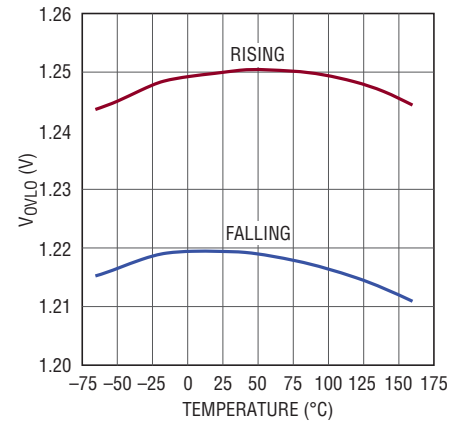
8310 G07

**UVLO Hysteresis Current vs Temperature**



8310 G08

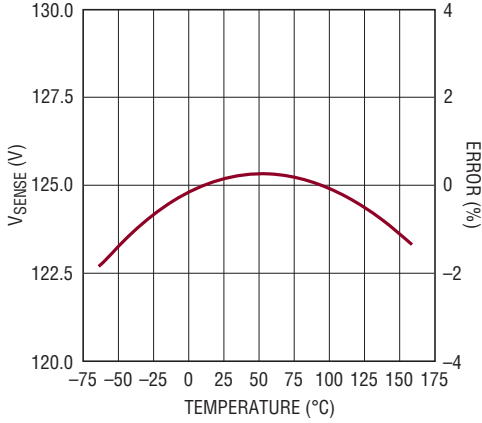
**OVLO Threshold Voltage vs Temperature**



8310 G09

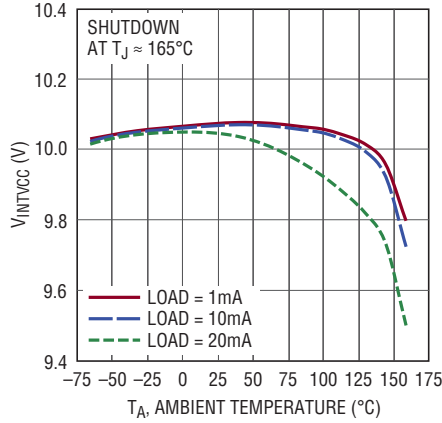
**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**SENSE Overcurrent Threshold Voltage vs Temperature**



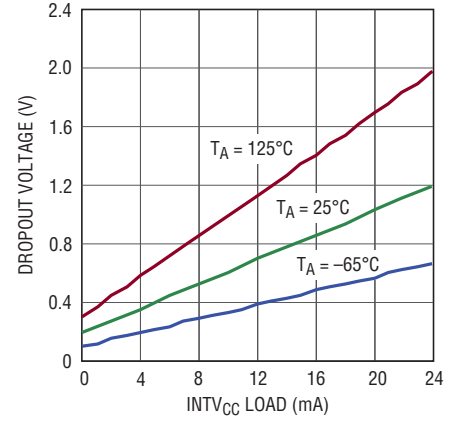
8310 G10

**INTV<sub>CC</sub> Voltage vs Temperature and Load Current**



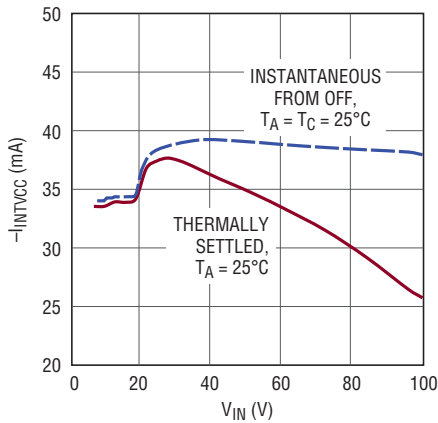
8310 G11

**INTV<sub>CC</sub> Dropout Voltage vs Load Current, Temperature**



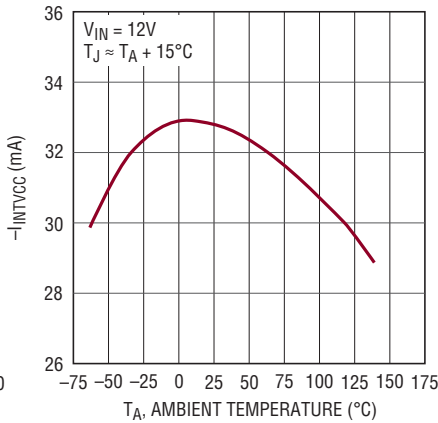
8310 G12

**INTV<sub>CC</sub> Current Limit vs Input Voltage**



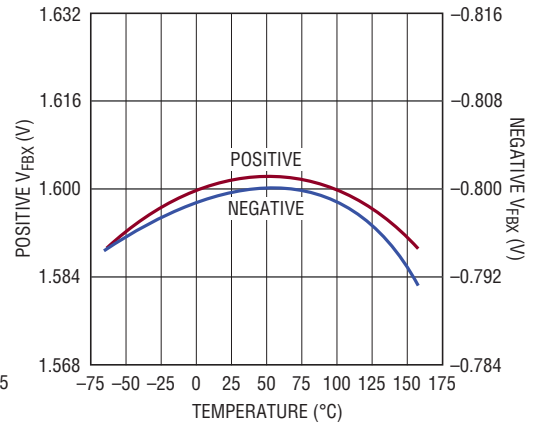
8310 G13

**INTV<sub>CC</sub> Current Limit vs Temperature**



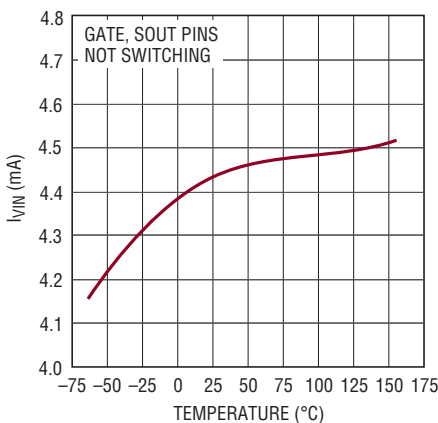
8310 G14

**FBX Regulation Voltage vs Temperature**



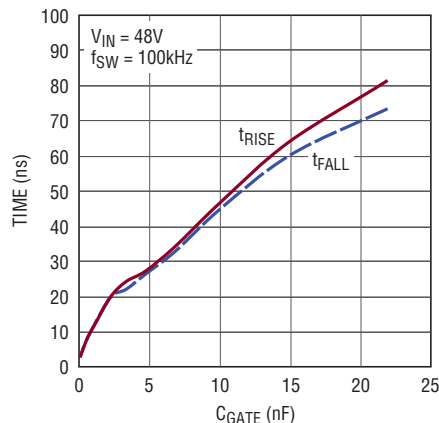
8310 G15

**V<sub>IN</sub> Quiescent Current vs Temperature**



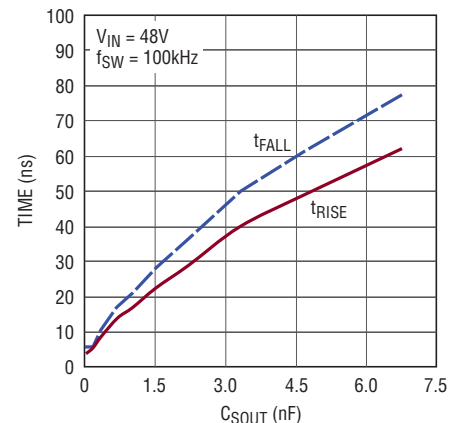
8310 G16

**GATE Driver Transition Time vs Capacitance**



8310 G17

**SOUT Driver Transition Time vs Capacitance**

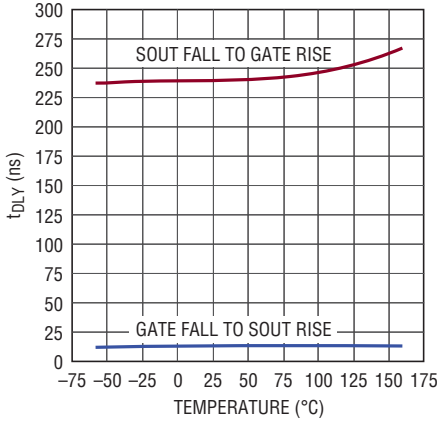


8310 G18



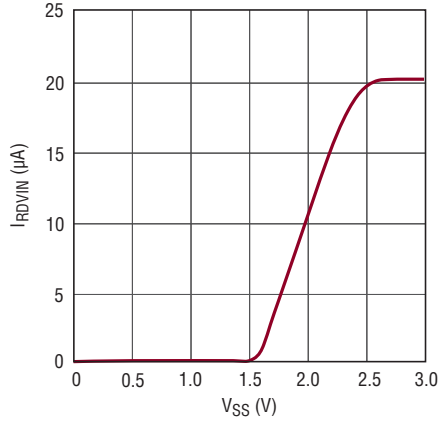
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , unless otherwise noted.

**Driver Nonoverlap Delays vs Temperature**



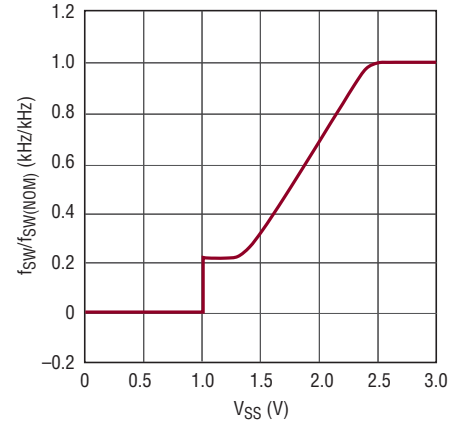
8310 G19

**Set Current vs Soft-Start Voltage**



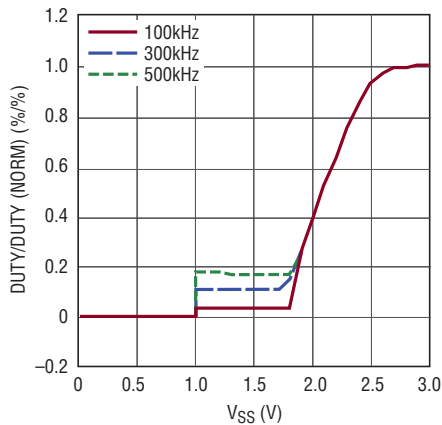
8310 G20

**Switching Frequency (Normalized) vs Soft-Start Voltage**



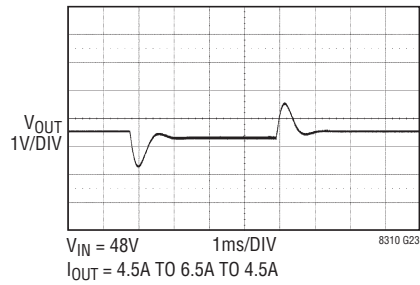
8310 G21

**GATE Duty Cycle (Normalized) vs Soft-Start Voltage**



8310 G22

**Output Voltage Transient Response (Typical Applications, Pages 1 and 31)**



8310 G23

## PIN FUNCTIONS

**UVLO (Pin 1):** System Undervoltage Lockout Input. Program the system falling UVLO threshold (minimum  $V_{IN}$  voltage) with a resistive voltage divider from  $V_{IN}$  to this pin. The pin voltage is compared internally to an accurate 1.22V threshold. Program the system rising UVLO hysteresis via this pin's 5.7 $\mu$ A hysteretic current and the values of the external resistors. The device is shut down below the UVLO threshold and draws 1 $\mu$ A or less from  $V_{IN}$  when  $V_{UVLO} \leq 0.36V$  (min). The UVLO pin can withstand 100V maximum.

**OVLO (Pin 3):** System Overvoltage Lockout Input. Program the system rising OVLO threshold (maximum  $V_{IN}$  voltage) with a resistive voltage divider from  $V_{IN}$  to this pin. The pin voltage is compared internally to an accurate 1.25V threshold. Exceeding the OVLO threshold sets the fault latch and forces a system shutdown.

**DFILT (Pin 5):** Duty Cycle Loop Filter Pin. Set the duty cycle loop filter pole by connecting a capacitor to GND from this pin in both duty mode and current mode applications. Consult the Applications Information section to choose the capacitor value to reduce load step ringing in duty mode control applications. Do not float this pin, a capacitor is required.

**RT (Pin 6):** Switching Period Set Input. Set the oscillator switching period (frequency) via a resistor to GND from this pin, typically 20k to 100k for 2 $\mu$ s to 10 $\mu$ s (500kHz to 100kHz). In applications where an external clock drives the SYNC pin, program the switching period to the expected SYNC frequency value. Place the resistor close to the pin and minimize stray capacitance. Do not leave the RT pin open.

**SYNC (Pin 7):** External Clock Input. Drive this pin with an external fixed-frequency clock signal to synchronize switching to it. The SYNC falling edge is automatically detected and converted to a pulse that starts the minimum off-time of the duty cycle. The SYNC pulse low and high times must both be  $\geq 250ns$ . Select an  $R_T$  resistor that programs the internal switch frequency to the external SYNC frequency to keep the maximum duty cycle limit accurate. When  $V_{SS} < 1V$ , the SYNC pin is ignored.

**SS (Pin 8):** Soft-Start Input. Program start and hiccup timing by tying an external capacitor between SS and GND. During normal soft-start this pin sources 50 $\mu$ A. During faults and initial start, a 6mA (typ) current sink discharges this pin to 0.27V (typ). The GATE pin is shut off until  $V_{SS} \geq 1V$ . After an overcurrent shutdown, the pin sources only 5 $\mu$ A until  $V_{SS} \geq 1V$ , which provides an extended wake-up period that reduces power dissipation during repeated start-up retries (hiccup mode). Switching frequency and duty cycle are folded back until  $SS > 2.5V$ . Above 1V, the pin sources 50 $\mu$ A until charged to an internal 3V clamp.

**V<sub>C</sub> (Pin 9):** Transconductance Error Amp Output. Compensate the converter loop at this pin with an external series resistor and capacitor to GND in feedback applications. In opto-isolated feedback applications, compensation is generally done on the secondary side (see the Applications Information section). In duty mode control applications that have no output voltage feedback, leave this pin unconnected.

**FBX (Pin 10):** Feedback Input and Mode Control. Standard input for nonisolated applications that require voltage feedback. Program output voltage with a resistive voltage divider to compare to the internal 1.6V reference for positive output applications, or to the -0.8V reference for negative output applications. When  $-0.2V < V_{FBX} < 0.3V$ , duty mode controls the GATE pin, otherwise FBX is assumed to be in control. FBX exceeding its reference by 7.5% ends the switching cycle in progress without triggering a system reset. Tie FBX to GND if duty mode only is desired.

**SOUT (Pin 11):** Synchronization Output. Pulse transformer driver for applications with synchronous secondary-side control, complementary to GATE. The SOUT falling edge leads GATE turn-on by 240ns (typ), and the rising edge trails GATE turn off by 12ns (typ). Actively pulled to  $INTV_{CC}$  during shutdown.

**NC (Pin 12):** No Internal Connection. Connect to GND.

## PIN FUNCTIONS

**SENSE (Pin 13):** Switch Current Sense Input. Positive input of the low side current sense to the control loops and the overcurrent comparator. Kelvin-connect this pin to the sense resistor at the source of the N-channel MOSFET switch. Exceeding 125mV at this pin triggers an overcurrent fault, and sends the system into fast shutdown, slow wake-up, and soft-start.

**GATE (Pin 14):** Switch Control Output. Low side switch drive (GND to INTV<sub>CC</sub>) for external N-channel MOSFET. The maximum duty cycle is limited to 78% (typ) because resonant reset forward converters require time for transformer flux to reset. Actively pulled to GND during shutdown.

**INTV<sub>CC</sub> (Pin 15):** Regulated Supply Output. A 10V LDO supply generated from V<sub>IN</sub> and capable of supplying the GATE pin. Must be bypassed with a 4.7μF capacitor or higher. The regulator voltage can be externally driven up to 17V, as long as V<sub>IN</sub> ≥ V<sub>INTVCC</sub>, to reduce internal power dissipation from V<sub>IN</sub> or to accommodate more than 10V gate drive for high voltage N-channel MOSFETs.

**RDVIN (Pin 16):** Duty Cycle Control Input. This pin sinks a precise 20μA in normal operation, but less during soft-start, when the duty cycle is folded back. Connect a resistor R<sub>SET</sub> between the INTV<sub>CC</sub> and RDVIN pins to program the desired (no opto) application output voltage:

$$R_{SET} = \left( \frac{N_p}{N_s} \right) \cdot \left( \frac{V_{OUT}}{12} \right) \frac{1}{20\mu A}$$

Resistor value accuracy contributes directly to the output voltage accuracy, choose appropriate tolerance. In current mode applications, feedback sets V<sub>OUT</sub>, therefore program R<sub>SET</sub> to set a maximum duty cycle guardrail that constrains the volt-seconds of flux in the transformer during transients. This pin must be connected to INTV<sub>CC</sub> by a resistor.

**V<sub>IN</sub> (Pin 18):** Supply Input and System Input Voltage Sense. Input supply for the part; operational from 6V to 100V. Accurate duty cycle requires accurate sensing of the V<sub>IN</sub> voltage, so keep the connection to the transformer primary short to minimize resistive voltage drops. Bypass to GND with 1μF.

**NC (Pin 20):** No Internal Connection. Connect to V<sub>IN</sub>.

**GND (Exposed Pad Pin 21):** Ground. This pin also senses the negative terminal of the current sense resistor. Solder the exposed pad directly to the ground plane.

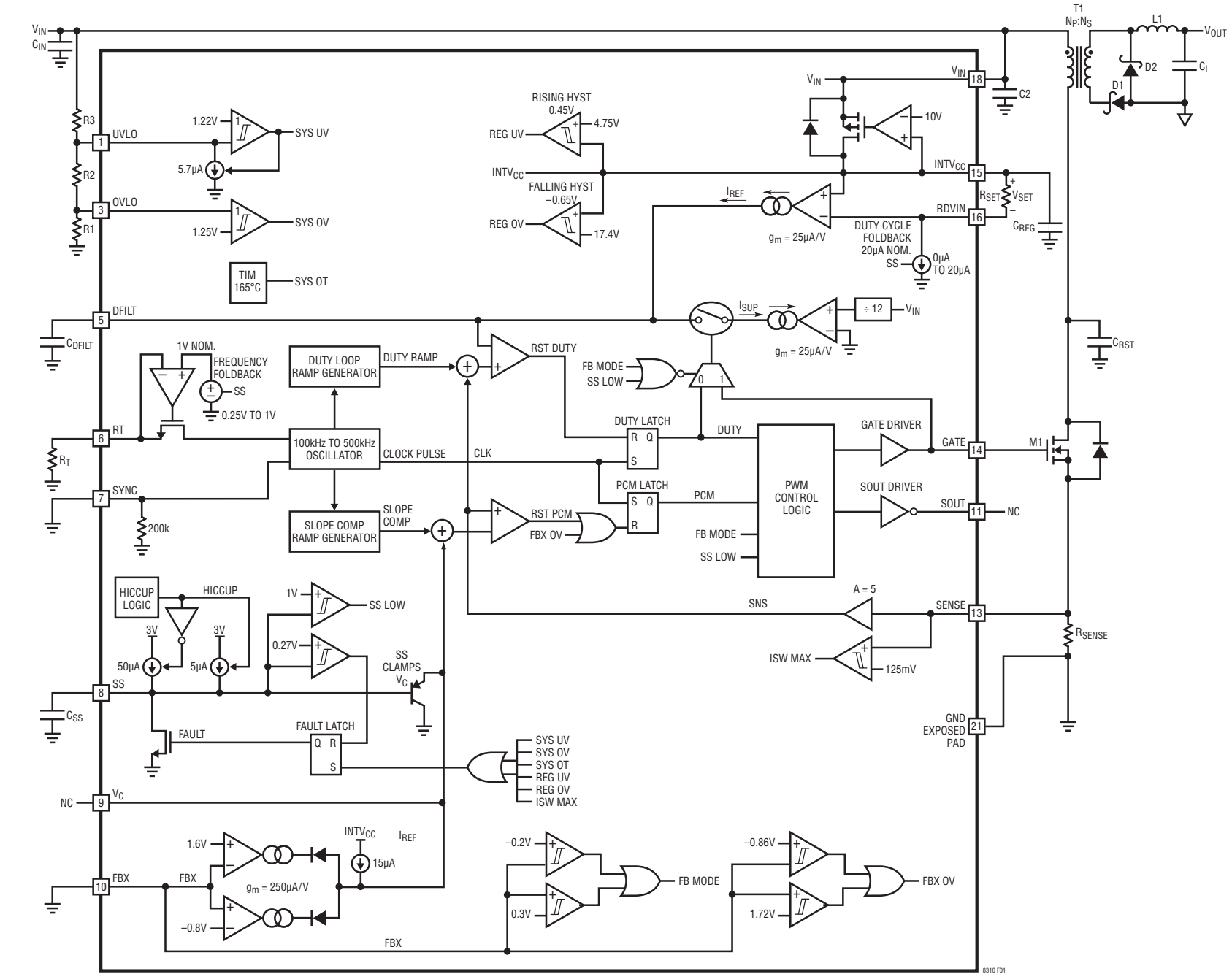
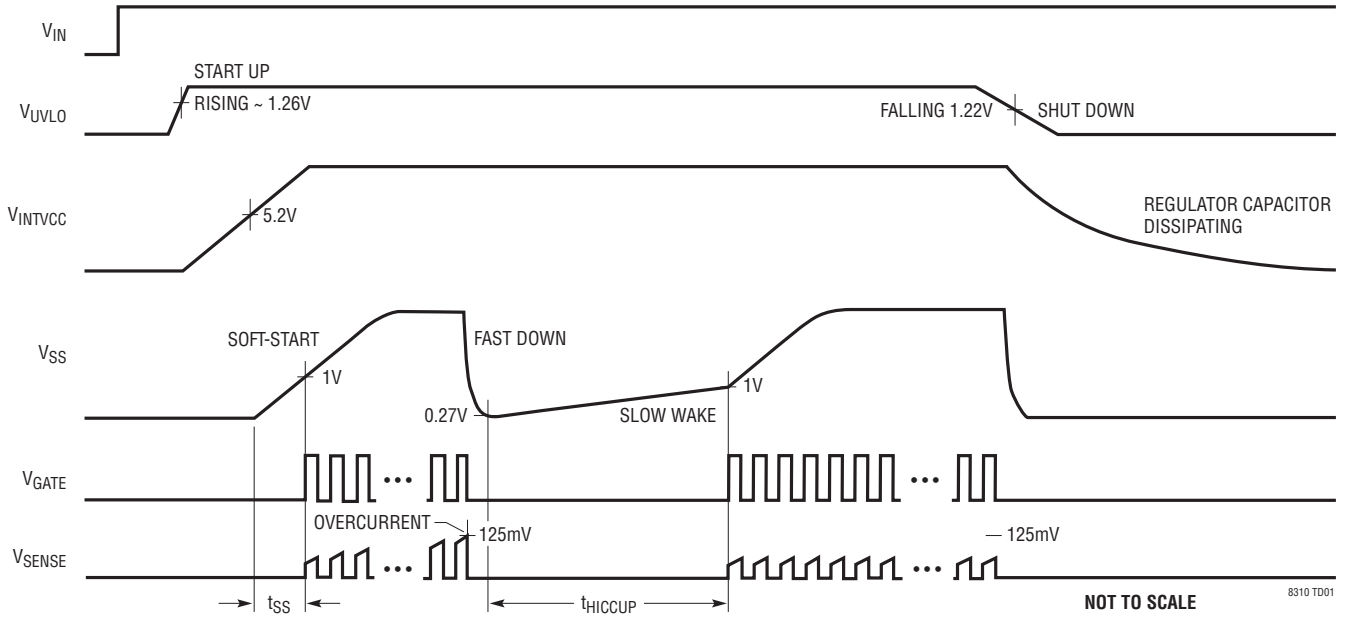


Figure 1. LT8310 Block Diagram Configured as a Nonsynchronous Duty Mode Converter

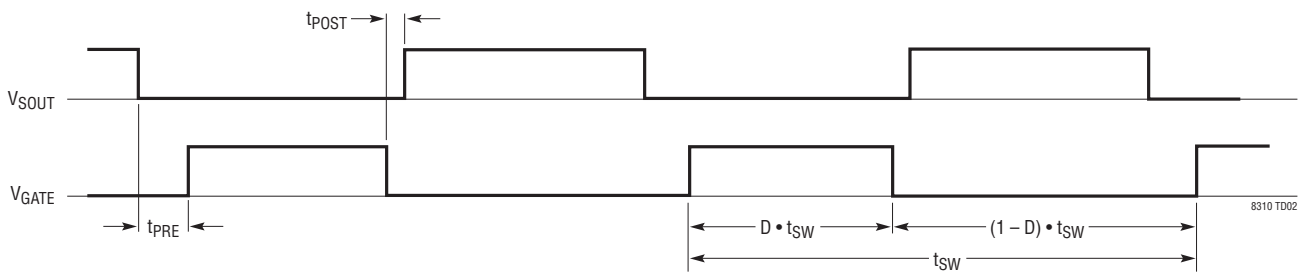
**BLOCK DIAGRAM**

## TIMING DIAGRAMS

### Start-Up/Soft-Start/Fault/Shutdown/Restart



### Nonoverlapping GATE/SOUT





## OPERATION

### INTRODUCTION

The LT8310 is a constant-frequency forward converter controller with a low side N-channel MOSFET gate driver and low side switch current sensing that offers two operating modes: duty mode control and peak current mode control. Duty mode control that requires no output voltage feedback is targeted for (but not limited to) isolated duty mode control applications, to which it brings a simple schematic, low parts count, and only one isolation element, a transformer. In current mode control applications, feedback determines the output voltage, but the duty control loop enforces a programmable relative maximum duty cycle that clamps the volt-seconds of core flux to avoid transformer saturation during transients. At all times the LT8310 also enforces an absolute maximum duty cycle that provides time to reset the core each switching period. With a patent pending architecture, the LT8310's duty control loop imposes volt-second accuracy over the span of input voltage that translates into both accurate output voltage without feedback and protection from transformer saturation.

### Duty Mode Control

The duty mode control loop compels a PWM duty cycle that is inversely proportional to the system input voltage,  $D(V_{IN}) \propto 1/V_{IN}$ , which is the correct function for a buck (or buck derived) converter to generate a constant output regardless of the line input. For a given scaling constant  $K_D$ ,

$$D(V_{IN}) = \frac{K_D [V]}{V_{IN}} \quad [1]$$

In a forward converter with transformer turns ratio  $N_P/N_S$ ,

$$V_{OUT} = \frac{D(V_{IN}) \cdot V_{IN}}{N_P / N_S} = \frac{K_D}{N_P / N_S} \quad [2]$$

In the discussion that follows it will be helpful to refer to the Block Diagram in Figure 1. Duty mode control governs operation when the feedback pin (FBX) is tied to GND. It serves as an accurate volt-second clamp when current mode control governs operation because feedback is present. The system clock starts the PWM duty cycle by driving the GATE pin high to close the external MOSFET switch and initiating a timing ramp in the duty loop ramp generator. While GATE is high, current proportional to  $V_{IN}$  discharges a capacitor ( $C_{DFILT}$ ) between the DFILT pin and GND; when GATE is pulled low, a fixed current charges it. The duty cycle ends when the ramp voltage plus some switch current feedback exceeds the DFILT voltage, at which point GATE falls and shuts off the primary-side switch until the start of the next period.

The condition of the main switch (on or off, as indicated by GATE pin voltage) controls the sourcing and sinking of current at the DFILT pin. The voltage imposed between the INTV<sub>CC</sub> and RDVIN pins,  $V_{SET}$ , establishes an internal reference current ( $I_{REF}$ ). During the switch on-time,  $D \cdot t_{SW}$ , a current proportional to the system input voltage  $V_{IN}$  (which is sensed at the  $V_{IN}$  supply pin) is subtracted from the reference current and driven at DFILT. During the switch off-time,  $(1-D) \cdot t_{SW}$ , only the reference current is driven. The external capacitor to GND at DFILT ( $C_{DFILT}$ ) integrates the current. In steady-state operation with sufficient load, the feedback loop forces the net cycle current to zero, which produces a duty cycle inversely proportional to  $V_{IN}$  (Equation 3), and ultimately a constant output voltage (Equation 4). An external resistor ( $R_{SET}$ ) between INTV<sub>CC</sub> and RDVIN and a precise 20 $\mu$ A sink at RDVIN program  $V_{SET}$  and thus,  $V_{OUT}$ .

$$D = \frac{12 \cdot V_{SET}}{V_{IN}} \quad [3]$$

$$V_{OUT} = \frac{12 \cdot V_{SET}}{N_P / N_S} \quad [4]$$

## OPERATION

With no output voltage feedback, the secondary-side LC filter might freely ring (depending on load resistance and parasitics) in response to load current steps; the primary-side switch current that feeds into the duty mode control loop limits the ringing. During the switch on-time, inductor current translates to switch current that is scaled and added to the timing ramp. Constant current is absorbed into the DC level of the DFILT voltage, which does not affect duty cycle, but changing current dynamically adjusts the duty cycle to dampen the ringing. The DFILT capacitor is chosen with respect to the output LC time constant ( $\sqrt{L_1 \cdot C_L}$ ) to track out the oscillation. The selection of this capacitor is discussed in the section, Compensating the Duty Mode Control Loop.

Duty mode control operation requires a minimum load in steady-state to balance the sum of the transformer magnetization current and output inductor ripple current, see the section, Minimum Load Requirements.

### Current Mode Control

To serve applications that require tighter output voltage regulation and faster load response, the LT8310 offers standard constant-frequency peak current mode control when output voltage feedback (opto-isolated or nonisolated) is connected. The system clock starts the PWM duty cycle by driving the GATE pin high to close the external MOSFET switch. The switch current flows through the external current sensing resistor  $R_{SENSE}$  and generates a voltage proportional to the switch current. The current sense voltage is amplified and added to a stabilizing slope compensation ramp. When the resulting sum exceeds the control pin ( $V_C$ ) voltage, the duty cycle ends, and the main switch is opened. The  $V_C$  pin level is set by the error amplifier, which amplifies the difference between the reference voltage (1.6V or -0.8V, depending on the configuration) and the feedback pin (FBX) voltage. In this manner, the error amplifier sets the correct peak switch current level to keep the output in regulation.

Several system operation and protection features are exclusive to current mode control. When the load is light, automatic pulse skipping allows the effective switching period to extend, which lowers the duty cycle without necessitating impractically narrow GATE pulses. If FBX pin overvoltage is detected during a cycle, the duty cycle ends, GATE falls, and the switch turns off, which allows the output voltage to coast down. When current mode control governs operation, the duty loop circuitry acts as a relative maximum duty cycle clamp that protects the transformer from developing excessive volt-seconds of flux during transients and it limits the output voltage. This feature also allows the system to revert to duty mode control if FBX is grounded. The duty cycle clamp margin is user-programmable.

### Common Operation and Protection Features

A programmable soft-start pin (SS) controls the power-up time and folds back the switching frequency and the duty cycle during start-up to protect the transformer and to limit inrush current. A minimum on-time of 190ns (typ) ensures that the MOSFET switch has enough time to turn on reliably, and a maximum duty cycle of 78% guarantees time for core reset each cycle. The SYNC pin allows an external pulse signal to override the LT8310's oscillator and set the switching period. The SOUT pin supplies a non-overlapping signal complementary to the GATE that may be used for synchronous converter applications. The SOUT pin driver has about 40% of the GATE pin's drive strength, and may be used to drive a pulse transformer (isolated) for forced continuous mode (FCM) operation.

Other protection mechanisms end the normal switching cycle or force system shutdown to protect the application circuit. The minimum and maximum  $V_{IN}$  operating thresholds are programmed at the UVLO and OVLO pins, respectively. Input voltages outside of the set limits shut down the system. Shutdown also occurs when the  $INTV_{CC}$  regulator voltage goes above or below its operating range, and when the die temperature exceeds 165°C. The switch

## OPERATION

overcurrent limit threshold is programmed at the SENSE pin. If the maximum current limit is reached, a fault latch is set and the system shuts down. Upon restart the system will operate in hiccup mode, which extends the soft-start time and thus reduces average power dissipated in the MOSFET during repeated retries.

### Forward Converter Basics

A forward converter is a buck-derived topology that comprises a transformer, a primary-side PWM-controlled switch, secondary-side switches, an inductor, and a capacitor, as shown in Figure 3. The secondary-side switches may be nonsynchronous (diodes), synchronous (MOSFETs), or a combination thereof. The transformer provides galvanic isolation for isolated applications.

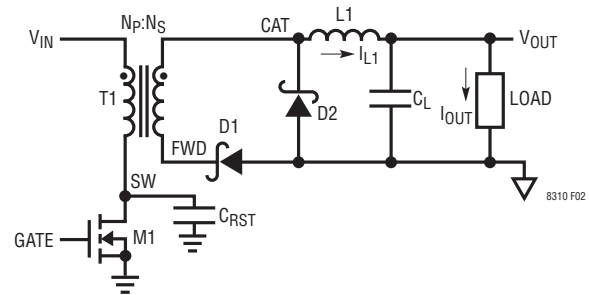


Figure 3. Forward Converter Architecture (Nonsynchronous)

Refer to Figure 2 in the following discussion of signals in a forward converter. When the GATE signal goes high, the primary winding sees the full input voltage, and the secondary winding voltage has a value scaled by the turns ratio,  $V_{IN}/(N_P/N_S)$ . During this period the forward diode

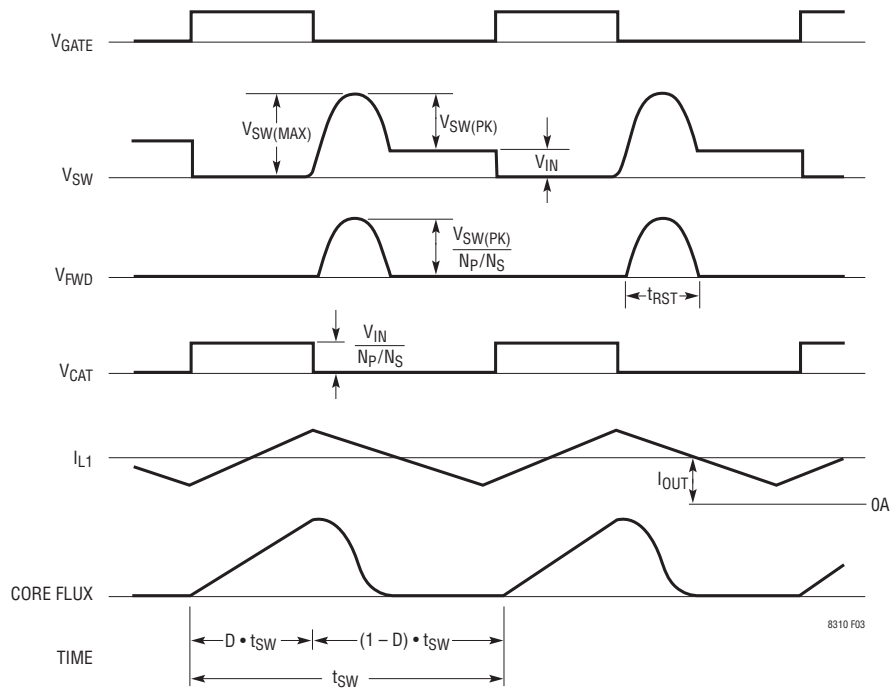


Figure 2. Typical Signals in a Forward Converter

## OPERATION

D1 conducts, which imposes  $V_{IN}/(N_P/N_S) - V_{OUT}$  across inductor L1 (ignoring voltage drop across the diode), for the switch on-time,  $D \cdot t_{SW}$ . When the GATE signal goes low, the switch turns off, and the primary winding voltage collapses as the primary current charges the reset resistor  $C_{RST}$ . The switch node voltage ( $V_{SW}$ ) resonates past  $V_{IN}$ , which takes the primary winding voltage negative. The secondary winding voltage also goes negative, forward diode D1 turns off, and the inductor current flows through the catch diode, D2, which imposes  $-V_{OUT}$  (again ignoring diode drop) across inductor L1 for the switch off-time,  $(1 - D) \cdot t_{SW}$ . The output voltage may be calculated by considering the volt-second balance in the inductor under steady-state conditions (Equation 5), and then solving for  $V_{OUT}$ . Equation 6 makes it clear that forcing the duty cycle to be inversely proportional to the input voltage would create a constant output voltage as desired.

$$\left( \frac{V_{IN}}{N_P / N_S} - V_{OUT} \right) \cdot D \cdot T_{SW} + (-V_{OUT}) \cdot (1 - D) \cdot T_{SW} = 0 \quad [5]$$

$$V_{OUT} = \frac{D \cdot V_{IN}}{N_P / N_S} \quad [6]$$

To keep the transformer from saturating, its core flux must be reset periodically. The LT8310 relies on resonant reset each cycle uses a capacitor between the switch node, SW, and ground (see Figure 2). When the main switch turns off at the end of the duty cycle,  $V_{SW}$  ramps up to and beyond  $V_{IN}$ , which cuts off secondary-side current and forces primary-side current to charge the switching node. Node SW resonates for half a sine wave until the transformer voltage and current are both zero, which leaves  $V_{SW} = V_{IN}$  until the next switch activation. Note that (1) the maximum voltage on the primary switch exceeds the input voltage, and may be well above it, and (2) ideally, the flux reset completes within the switch off-time before the next cycle begins. The LT8310 controller imposes an absolute maximum duty cycle that provides a predictable minimum off-time (at a given switching frequency) in which to reset the core.

## APPLICATIONS INFORMATION

### INTV<sub>CC</sub> Regulator Bypassing and Operation

The GATE and SOUT pin drivers and other chip loads are powered from the INTV<sub>CC</sub> pin, which is an internally regulated supply. The internal low dropout regulator requires a capacitor from the INTV<sub>CC</sub> pin to GND for stable operation and to store the charge for the large GATE and SOUT switching currents; a 4.7μF capacitor is adequate for most applications. Choose a 16V rated low ESR, X7R ceramic capacitor for best performance. Place the capacitor close to the LT8310 to minimize the trace length both to the INTV<sub>CC</sub> pin and to the chip ground. In shutdown, the INTV<sub>CC</sub> pin sinks 125μA (typical) until the pin voltage falls below 4.75V.

An internal current limit on the INTV<sub>CC</sub> output protects the LT8310 from excessive on-chip power dissipation. The minimum specified current limit should be considered when choosing the switching N-channel MOSFET and the operating frequency. Careful selection of a lower Q<sub>G</sub> MOSFET allows higher GATE switching frequencies, which leads to smaller magnetics. SOUT switching current must be accounted for when that pin drives a MOSFET gate, but in typical applications where SOUT is unused or drives an AC-coupled pulse transformer, GATE switching dominates the steady-state regulator load and the SOUT current may be ignored. The MOSFET gate drive switching current required may be calculated using Equation 7, see the Thermal Considerations section for further information.

$$I_{DRIVE} = Q_G \cdot f_{SW} \quad [7]$$

The INTV<sub>CC</sub> voltage tracks a few hundred millivolts below the supply voltage until the regulation loop closes when V<sub>IN</sub> exceeds about 10.5V. The INTV<sub>CC</sub> pin has its own undervoltage disable set to 4.75V (typical) that protects the external MOSFET from excessive power dissipation caused by not being fully enhanced. If the INTV<sub>CC</sub> pin drops below its undervoltage threshold, the GATE pin will be forced to GND, the SOUT pin will follow the INTV<sub>CC</sub> voltage, and the soft-start pin will be reset.

The regulator may be overdriven from external circuitry to reduce switching power dissipation in the LT8310 package, or to drive a MOSFET switch with a high threshold. The overdriven INTV<sub>CC</sub> pin voltage must be less than the IC supply to avoid back-driving the V<sub>IN</sub> pin. The INTV<sub>CC</sub> pin

has its own overvoltage threshold set to 17.4V (typical) that disables the system to protect MOSFETs rated for V<sub>GS(MAX)</sub> = 20V, a common specification. As with undervoltage shutdown, the GATE pin will be forced to GND, the SOUT pin will follow the INTV<sub>CC</sub> voltage, and the soft-start pin will be reset. A 4.7μF 25V rated low ESR, X7R capacitor is recommended when INTV<sub>CC</sub> is overdriven.

### Programming the System Turn-On and Turn-Off Thresholds

The system undervoltage and overvoltage thresholds are programmed by a resistive voltage divider from V<sub>IN</sub> to UVLO and OVLO, respectively (Figure 4). The falling UVLO threshold, 1.22V (nom), accurately sets the minimum operating V<sub>IN</sub> (Equation 8), below which the system goes into low power mode. A 5.7μA (typical) pull-down current that is active when the UVLO pin is below its falling threshold provides rising hysteresis that sets the minimum start-up V<sub>IN</sub> (Equation 9). The built-in comparator hysteresis contributes a small amount to the rising threshold as well.

$$V_{IN(UVLO \text{ FALLING})} = 1.22V \cdot \left( \frac{R3 + R2 + R1}{R2 + R1} \right) \quad [8]$$

$$V_{IN(UVLO \text{ RISING})} = V_{IN(UVLO \text{ FALLING})} + 5.7\mu A \cdot R3 + 40mV \cdot \left( \frac{R3 + R2 + R1}{R2 + R1} \right) \quad [9]$$

The rising OVLO threshold, 1.25V (nom), accurately sets the maximum operating V<sub>IN</sub> (Equation 10), above which the system stops switching and awaits soft-start. The built-in comparator hysteresis provides falling hysteresis that sets the maximum restart V<sub>IN</sub> (Equation 11).

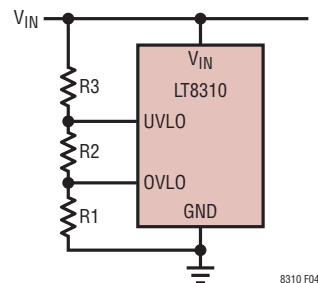


Figure 4. Resistor Connections for System UVLO and OVLO Threshold Programming



**APPLICATIONS INFORMATION**

$$V_{IN(OVLO\ RISING)} = 1.25V \cdot \left( \frac{R3 + R2 + R1}{R1} \right) \quad [10]$$

$$V_{OUT(TARG)} = \frac{D \cdot V_{IN}}{N_P / N_S} \quad [12]$$

$$V_{IN(OVLO\ FALLING)} = V_{IN(OVLO\ RISING)} - 33mV \cdot \left( \frac{R3 + R2 + R1}{R1} \right) \quad [11]$$

Selecting the resistor values best proceeds as follows:

1. Choose  $V_{IN(UVLO\ FALLING)}$  and  $V_{IN(OVLO\ RISING)}$  for the system
2. Choose a rising hysteresis voltage,  $V_{HYST(UVLO\ RISING)}$ , and calculate  $R3 = V_{HYST(UVLO\ RISING)} / 5.7\mu A$
3. Calculate the sum of  $R2 + R1$  from Equation 8
4. Calculate  $R1$  from Equation 10, which then determines  $R2$ , and
5. Recheck the thresholds using actual resistor values.

**Programming the Duty Cycle Loop Output Voltage Target**

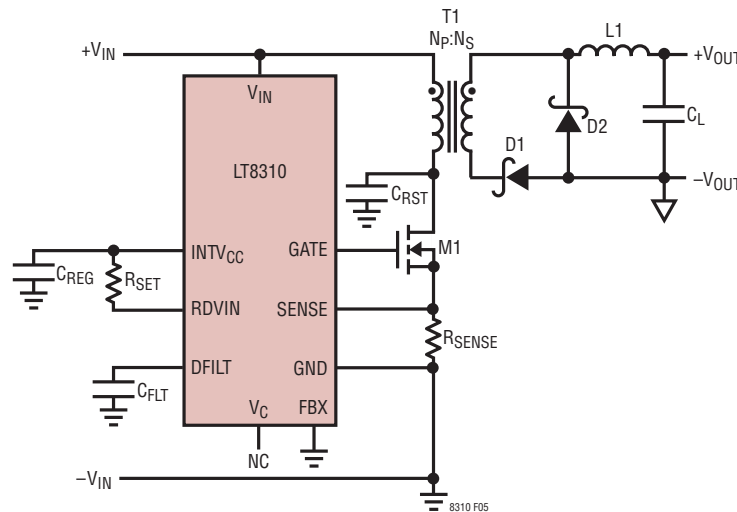
In all applications, the LT8310 duty mode control loop must have a programmed output voltage target,  $V_{OUT(TARG)}$ , that is the value the converter would produce, without output voltage feedback, using ideal components. For the forward converter, this is characterized by Equation 6 (here recast with the target output).

This is accomplished by setting the scaling factor ( $K_D$ ) of the duty cycle versus  $V_{IN}$  function and choosing the transformer turns ratio ( $N_P/N_S$ ). In applications without output voltage feedback, the target voltage minus any voltage drops (e.g., diode thresholds, ohmic losses) yields the nominal output voltage,  $V_{OUT}$ . In applications using an opto-coupler, the target is used as an upper guard rail level to the nominal output voltage that is set by feedback, and it is a measure of the relative duty cycle clamp margin.

First consider the transformer turns ratio in the core schematic in Figure 5. Since duty mode control forces the duty cycle to be inversely proportional the input voltage, the largest duty cycle occurs at the lowest operating input voltage. For a given target output voltage and minimum input voltage, the LT8310's maximum duty cycle limit, 75% (min), constrains the turns ratio per Equation 13.

$$\frac{N_P}{N_S} < \frac{0.75 \cdot V_{IN(MIN)}}{V_{OUT(TARG)}} \quad [13]$$

After fixing the turns ratio, consider the duty cycle. In general, the highest operating duty cycle should be maximized to best utilize the MOSFET each switching period, and to reduce the effect of switching losses each in cycle. The



**Figure 5. Forward Nonsynchronous Converter Core Schematic**

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duty cycle should be checked for feasibility and margin over the full  $V_{IN}$  operating range. The minimum input voltage produces the maximum duty cycle, which must not exceed the LT8310's minimum-specified maximum duty cycle limit (75%). The maximum input voltage produces the minimum duty cycle, which must be greater than duty cycle of the minimum GATE pulse width,  $f_{sw} \cdot t_{ON(MIN)}$ , as in Equation 14.

$$f_{sw} \cdot t_{ON(MIN)} < \frac{V_{OUT(TARG)}}{V_{IN}} \cdot \frac{N_P}{N_S} < 0.75 \quad [14]$$

Finally, the duty cycle scaling must be programmed. As discussed in the latter part of the section, Duty Mode Control, the voltage difference between the  $INTV_{CC}$  and RDVIN pins,  $V_{SET}$ , and an accurate internal gain of 12V/V sets the duty mode loop scaling constant,  $K_D$ . The RDVIN pin sinks a precise 20 $\mu$ A that permits a single resistor,  $R_{SET}$ , to program the voltage difference.

$$K_D = \frac{12V}{V} \cdot V_{SET} = \frac{12V}{V} \cdot (20\mu A \cdot R_{SET}) \quad [15]$$

Resistor  $R_{SET}$  may be chosen to achieve the desired  $V_{OUT(TARG)}$  based on Equation 16.

$$R_{SET} = \frac{\frac{V_{OUT(TARG)}}{12V/V} \cdot \frac{N_P}{N_S}}{20\mu A} \quad [16]$$

The tolerance of the set resistor contributes directly to the accuracy of the target output voltage, which is especially important to the accuracy of converters operating without output voltage feedback, so always use a 1% or better resistor. Keep  $R_{SET}$  close to the RDVIN and  $INTV_{CC}$  pins of the chip to minimize trace length and avoid cross-coupling with other signals.

During soft-start, the RDVIN sinking current is reduced to fold back the duty cycle while the clock frequency is also reduced. This protects the transformer by limiting the volt-seconds of flux generated when the clock period is made longer. Take care to consider the flux conditions during soft-start if external currents are employed for trimming or margining.

### Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 500kHz to optimize efficiency and performance or external component size. Higher frequency operation yields smaller component size, but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. It also decreases magnetization current, which reduces the minimum load requirement under duty cycle mode control. Lower frequency operation gives better performance at the cost of larger external component size. Table 1 shows the  $R_T$  values for several frequencies that match the design equation, Equation 17.

**Table 1. Resistor Selection Guidance for Some Common Switching Frequencies**

FREQUENCY ( $f_{sw}$ ) (kHz)	PERIOD ( $t_{sw}$ ) ( $\mu$ s)	CLOSEST 1% RESISTOR ( $R_T$ ) (k $\Omega$ )
100	10.0	100
150	6.67	66.5
200	5.00	49.9
250	4.00	40.2
300	3.33	33.2
350	2.86	28.7
400	2.50	24.9
450	2.22	22.1
500	2.00	20.0

$$R_T = \frac{1000kHz}{f_{sw}} \cdot 10k = \frac{t_{sw}}{1\mu s} \cdot 10k \quad [17]$$

Minimize stray-coupling to the adjacent DFILT and SYNC pins by keeping the traces short. An external resistor from the RT pin to GND is required—do not leave this pin open.

### Programming the Current Sense

The LT8310 features primary-side switch current sensing that protects the system from excessive load current, damps output ringing when duty mode control dominates, and sets the duty cycle when current mode control dominates. When  $V_{SENSE}$  exceeds 125mV (nom), the maximum switch current threshold, the system shuts down and attempts a restart after a slow wake-up period (see Programming the Soft-Start Interval and Hiccup Period). In converter

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applications operating without output voltage feedback, current sense information is fed back to the duty cycle loop to reduce output voltage ringing due to load current steps that excite the output LC tank. In supply applications, each cycle ends when the amplified SENSE voltage exceeds the  $V_C$  pin control level. In all cases, during the cycle on-time, the switch sees the rippling inductor current ( $I_{L1}$ ), scaled by the transformer turns ratio (Equation 18) plus the transformer's primary magnetizing current,  $I_{\mu,p}$ . Applying  $V_{IN}$  across the magnetizing inductance generates a peak magnetizing current of approximately  $12 \cdot V_{SET} \cdot t_{SW} / L_{\mu,p}$ .

$$I_{SWITCH} = \frac{I_{L1}}{N_p / N_s} + I_{\mu,p} \quad [18]$$

Resistor  $R_{SENSE}$  connected between the SENSE and GND pins converts the switch current to a voltage. It should be selected to provide the maximum switch current required by the application, including inductor ripple current, without exceeding the SENSE pin's overcurrent threshold. A good rule of thumb is to allow 10% margin on the minimum overcurrent threshold of 115mV.

During steady-state operation, the average inductor current equals the load current. In applications under duty mode control, which require a minimum load, less inductor ripple means a lower minimum load current, so peak inductor current might be 10% or less above the maximum load current. Output voltage ring damping operates best with a strong average current signal, so  $R_{SENSE}$  should be chosen as large as allowed by the SENSE pin threshold. Equation 19 provides a good value for  $R_{SENSE}$  that accounts for the minimum SENSE threshold:

$$R_{SENSE} \leq \frac{115mV}{1.1 \cdot I_{SWITCH(MAX)}} \quad [19]$$

In applications with output voltage feedback, current mode control is most agile with a steep slope to the ripple, so peak inductor current might be 20% or more above the average load current. Equation 20 provides a good value for  $R_{SENSE}$  that accounts for the minimum SENSE threshold:

$$R_{SENSE} \leq \frac{115mV}{1.4 \cdot I_{SWITCH(MAX)}} \quad [20]$$

It is always prudent to verify the peak inductor current in the application to ensure the sense resistor selection provides margin to the SENSE overcurrent limit threshold. The placement of  $R_{SENSE}$  should be close to the source of the N-channel MOSFET and GND of the LT8310. The SENSE input to LT8310 should be a Kelvin connection to the positive terminal of  $R_{SENSE}$ . Verify the power in the resistor to ensure that it does not exceed its rated maximum.

### Programming the Soft-Start Interval and Hiccup Period

The built-in soft-start circuit significantly reduces the inrush current spike and output voltage overshoot at start-up. Please refer to Figure 6 and the Timing Diagrams section for the following discussion of soft-start behavior. The soft-start interval is programmed by a capacitor connected from the SS pin to GND. In a normal start-up, after the  $INTV_{CC}$  voltage exceeds its rising threshold of about 5.2V, the SS pin sources 50 $\mu$ A (typical), which ramps the capacitor voltage. Switching commences when the 1.00V switching threshold is exceeded (EN\_GATE high).

Assuming the SS pin starts fully discharged, the soft-start time,  $t_{SS}$ , may be programmed by choosing  $C_{SS}$  using Equation 21. A 100nF soft-start capacitor produces about 2ms of delay, which suits many applications.

$$C_{SS} = 50nF \cdot \frac{t_{SS} [ms]}{1ms} \quad [21]$$

The SS pin voltage is discharged when the fault latch is set under any of the following conditions: the UVLO pin voltage falls below its threshold (SYS\_UV high), the OVLO pin voltage exceeds its threshold (SYS\_OV high), the die temperature exceeds 165°C (SYS\_OT high), the  $INTV_{CC}$  voltage falls below or rises above its operating range (REG\_UV or REG\_OV high), or the SENSE pin voltage exceeds its maximum threshold because the switch current is too large (ISW\_MAX high). When the fault condition ceases and  $V_{SS} < 0.27V$ , the fault latch clears, which brings about restart as SS rises through the 1V threshold.

Exceeding maximum switch current sets the hiccup latch, which extends the soft-start time by reducing the pull-up current to 5 $\mu$ A (typical). After the fault latch is reset, the



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### Compensating the Direct-Wired Current Mode Control Loop

When output voltage feedback is directly wired to the FBX pin, the LT8310 uses current mode control to regulate the output. To compensate the current mode feedback loop of the LT8310, a series resistor-capacitor network is usually connected from the  $V_C$  pin to GND (Figure 7).

For most applications, a capacitor ( $C_C$ ) in the range of 1nF to 22nF is suitable, with 4.7nF being typical. The resistor ( $R_Z$ ) should fall in the range of 10k to 50k, with 20k being typical. An estimate for  $R_Z$  based on the output voltage, the output capacitance ( $C_L$ ), the compensation capacitance ( $C_C$ ), the sense resistor ( $R_{SENSE}$ ), the turns ratio ( $N_P/N_S$ ), and the absolute value of the feedback reference ( $|V_{REF}| = 1.6V$  or  $0.8V$ ) is:

$$R_Z = \sqrt{R_{SENSE} \cdot 100k \cdot \frac{C_L}{C_C} \cdot \frac{(N_P / N_S) \cdot V_{OUT}}{|V_{REF}|}} \quad [26]$$

A small capacitor is sometimes connected in parallel with the  $R_C$  compensation network to attenuate the  $V_C$  voltage ripple induced from the output voltage ripple through the internal error amplifier. The parallel capacitor usually ranges in value from 10pF to 100pF.

A practical approach to design the compensation network is to start with the typical  $C_C = 4.7nF$  and  $R_Z = 20k$ , calculate a new  $R_Z$  when all the component values in Equation 26 are available, then tune the compensation network to optimize the performance. Stability should be checked across all operating conditions, including load current, input voltage and temperature.

### Minimum Load Requirements

In standard current mode converters, the controller senses rising output voltage and activates pulse-skipping mode that reduces the power delivered to the load as the output current demand decreases, until there is no load and the main switch is turned off. With no output voltage sensing to command pulse skipping and a  $V_{IN}$ -based control loop that operates continuously, LT8310 nonsynchronous duty mode control applications require a minimum load in steady state operation to dissipate transformer magnetization and inductor ripple currents. Failure to provide the minimum load current results in an increased steady-state output voltage, which peaks at  $V_{IN}/(N_P/N_S)$  when  $I_{OUT} = 0A$ .

In Equation 27, given an output voltage ( $V_{OUT}$ ), the minimum load current is expressed as a function of (1) the

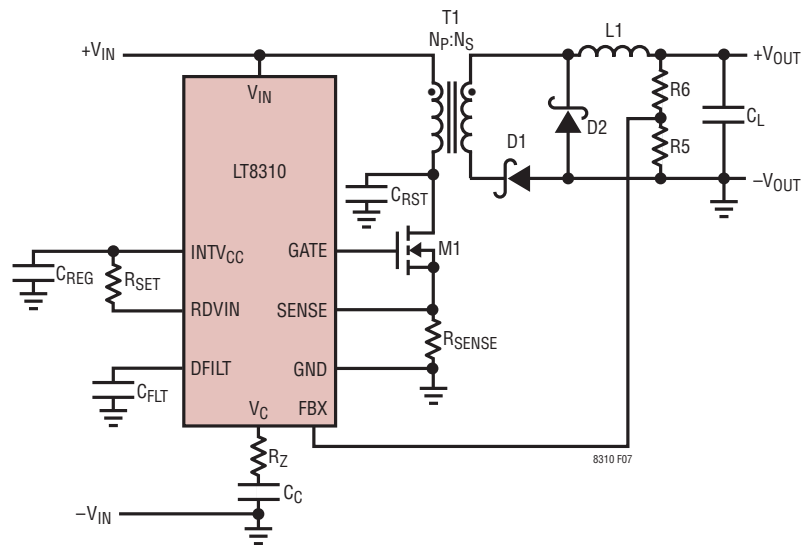


Figure 7. Forward Nonsynchronous Direct-Wired Nonisolated Basic Schematic



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switching frequency ( $f_{SW}$ ), (2) the transformer's primary magnetizing inductance ( $L_{\mu}$ ) as seen on the secondary-side through the turns ratio ( $N_P/N_S$ ), and (3) the ripple current in the inductor ( $L1$ ) during the off-time portion of the duty cycle ( $1 - D_{MIN}$ ).

$$I_{OUT(MIN)} = \frac{V_{OUT}}{2 \cdot f_{SW}} \cdot \left( \frac{(N_P / N_S)^2}{L_{\mu}} + \frac{(1 - D_{MIN})}{L1} \right) \quad [27]$$

The minimum load current may be reduced in three ways, given a fixed output voltage. First, the switching frequency,  $f_{SW}$ , may be increased while keeping the same transformer and output inductor. Operating at higher frequency tends to decrease efficiency as switching transients account for a higher percentage of the period. Some power transfer lost to lower efficiency generally outweighs power spent on burning dummy load current if the natural load is too light. Second, the transformer magnetizing inductance may be increased by using more turns to reduce the magnetizing current. Within the same family of transformers, an 8:4 transformer will have more magnetizing inductance than a 2:1 transformer, but more turns also means more winding resistance losses. Third, the output inductor may be increased, which directly reduces the output ripple current, and thus the minimum load.

If an application's natural load is not sufficient, a dedicated load resistor that guarantees the minimum current for a given output voltage may be selected using Equation 28. Consider the power dissipation when choosing the rating and type of resistor  $R_{OUT}$ .

$$R_{OUT} < 2 \cdot f_{SW} \cdot \left( \frac{L_{\mu}}{(N_P / N_S)^2} \parallel \frac{L1}{(1 - D_{MIN})} \right) \quad [28]$$

### Ohmic Loss Matters

Before a more specific discussion of component selection, a general note about DC resistance in the power path is warranted. For duty mode control applications, no voltage feedback exists to compensate for voltage drops in the system. Contributors include the on-resistance of all

switches, the current sense resistor, and the DCR's of the transformer and inductor. Take care to select components for their low ohmic losses to control both the absolute accuracy of the output voltage and the load regulation effect. Once ohmic losses are estimated or measured for a given application, the output voltage target may be adjusted upward, and a new value of set resistor chosen to compensate, see Programming the Duty Cycle Loop Output Voltage Target.

### Transformer Selection

Important parameters that guide the choice of transformer include the primary-to-secondary turns ratio, the presence or absence of auxiliary windings and their turns ratios, the power rating, the operating frequency, the magnetizing inductance, the leakage inductance, the DC winding resistances of the primary and secondary and the isolation voltage rating.

An application's input voltage range and output voltage target drive the choice of turns ratio between the primary and secondary windings (see Equation 12). DC/DC power transformer winding ratios should be specified to  $\pm 1\%$ , a variation that directly affects the accuracy of converters without output voltage feedback, but that only influences the duty cycle range in circuits with output voltage feedback.

Some application circuits require auxiliary primary- or secondary-side rails to accommodate the supply limits of other external devices. Switching power dissipation in the LT8310 may be reduced by driving the  $INTV_{CC}$  regulator externally from a third winding.

Rather than stipulate a maximum current and core flux limit for DC/DC converter transformers, most vendors specify a power rating, an operating frequency range and a minimum magnetizing inductance.

While flux capability (saturation) is important, most manufacturers specify a power rating.

For a lower minimum load current, choose less magnetizing current/more magnetizing inductance.

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Table 2 provides some recommended transformer vendors.

**Table 2. Recommended Transformer Manufacturers**

MANUFACTURER	WEB ADDRESS
Champs Technologies	www.champs-tech.com
Coilcraft	www.coilcraft.com
Cooper-Coiltronics	www.cooperet.com
Pulse Electronics	www.pulseelectronics.com
Würth-Midcom	www.we-online.com

### Resonant Reset Capacitor Selection

The reset capacitor value must be sized to allow a half period of a sine wave to complete during the shortest off-time the switch normally experiences, namely when  $V_{IN}$  is lowest and the duty cycle is greatest. The LT8310's maximum duty cycle clamp of 78% typical/82% maximum (see the Electrical Characteristics section) sets a lower bound on the off-time of 18% of the period. Minimum input voltage, turns ratio, and output voltage target determine the largest duty cycle in steady state operation,  $D_{MAX}$ . The resonant reset time,  $t_{RST}$ , must fall between the two:

$$0.18 \cdot t_{SW} < t_{RST} < (1 - D_{MAX}) \cdot t_{SW} \quad [29]$$

The maximum switch node voltage,  $V_{SW(MAX)}$ , occurs at the peak of the resonance when the input voltage is greatest. In practical circuits, the switch node might slew beyond  $V_{IN}$  before resonating, it might initially spike, and then have a high frequency ripple, or it might not complete resonance if the available reset time is too short—all of which change the peak voltage. Estimate the maximum switch voltage with Equation 30, and increase it by at least 20% when choosing the voltage rating of the reset capacitor.

$$V_{SW(MAX)} = V_{IN(MAX)} + V_{OUT(TARG)} \cdot \left(\frac{N_P}{N_S}\right) \cdot \frac{\pi}{2} \cdot \frac{t_{SW}}{t_{RST}} \quad [30]$$

A COG/NPO type capacitor is the best choice for the resonant reset capacitor—first, for its negligible microphonic action that would otherwise cause electronic or audio interference, and second, for its excellent voltage linearity and flatness over temperature, which makes for consistent timing across operating conditions and less margining of other components and specifications.

An initial design value for the resonant reset capacitor requires estimates of the transformer's magnetizing inductance ( $L_\mu$ ) and MOSFET output capacitance ( $C_{OSS}$ ), in addition to the reset time target (Equation 31).

$$C_{RST} = \left(\frac{t_{RST}}{\pi}\right)^2 \cdot \frac{1}{L_\mu} - C_{OSS} \quad [31]$$

Board layout, transformer windings, and the forward diodes also contribute to the total switch node capacitances, and may be subtracted from the resonant capacitor value as required. Keep the resonant reset capacitor close to the MOSFET's drain at one terminal and well grounded with a short trace at the other terminal. Prototyping to characterize the actual reset behavior is highly recommended.

In step-up applications (where  $N_P/N_S < 1$ ), splitting the capacitance between the primary-side switch node and the secondary-side forward node may help reduce switch node ringing. The secondary-side capacitor value reflects to the primary-side by a factor of  $(N_S/N_P)^2$ .

### Primary Switch MOSFET Selection

Important parameters for the primary N-channel MOSFET switch include the maximum drain-source voltage rating ( $V_{DS}$ ), the gate-source threshold voltage ( $V_{GS}$ ), the on-resistance ( $R_{DS(ON)}$ ), the gate charge ( $Q_G$ ), the maximum drain current ( $I_D$ ), and the thermal resistances ( $\theta_{JC}$  and  $\theta_{JA}$ ).

The drain-source breakdown voltage ( $BV_{DSS}$  or  $V_{DS(MAX)}$ ) is the key to MOSFET selection because the primary switch experiences a maximum voltage significantly above the input (see Figure 3), which was estimated in Equation 30. Many available power MOSFETs are avalanche-rated, and will easily withstand occasional overvoltage, but regular avalanching is inefficient, and can be destructive depending on energy, frequency, and temperature. Derating the result of Equation 30 by at least 20% and prototyping the circuit are recommended design procedures.

An internal current limit on the  $INTV_{CC}$  output protects the LT8310 from excessive on-chip power dissipation. The minimum value of this current should be considered when choosing the main N-channel MOSFET and the operating frequency. Selection of a lower  $Q_G$  MOSFET allows higher

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switching frequencies, which leads to smaller magnetics. The required switching current,  $I_{GATE}$ , can be calculated using Equation 32, see the Thermal Considerations section for further details.

$$I_{GATE} = Q_G \cdot f_{SW} \quad [32]$$

The power dissipated in the primary MOSFET in a forward converter is described by Equation 33. The first term represents the conduction loss in the device, and the second term represents the switching loss.  $C_{RSS}$  is the reverse-transfer capacitance, which is usually specified in the MOSFET characteristics. For maximum efficiency,  $R_{DS(ON)}$  and  $C_{RSS}$  should be minimized.

$$P_{SW} = I_{L(MAX)}^2 \cdot R_{DS(ON)} \cdot D_{MAX} + 2 \cdot V_{IN}^2 \cdot C_{RSS} \cdot f_{SW} \cdot \frac{I_{L(MAX)}}{1A} \quad [33]$$

From the known power dissipated in the main MOSFET, its junction temperature can be obtained using Equation 34.  $T_J$  must not exceed the MOSFET maximum junction temperature rating. It is recommended to measure the MOSFET temperature in steady state to ensure that absolute maximum ratings are not exceeded.

$$T_J = T_A + P_{SW} \cdot \theta_{JA} = T_A + P_{SW} \cdot (\theta_{JC} + \theta_{CA}) \quad [34]$$

### Input Capacitor Selection

The input capacitor supplies the transient input current through to the transformer and main switch, so it must be sized according to transient current requirements. Forward converters experience discontinuous input currents on par with the load current divided by the transformer turns ratio. The switching frequency, output current, and tolerable input voltage ripple are key inputs to estimating the capacitor value required to limit input voltage ripple to a specified level. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and DC bias. Low ESR and ESL at the switching frequency are necessary to avoid excess spiking of the input voltage.

To achieve RMS input ripple of  $V_{IN(RIPPLE)}$ , the input capacitor for a forward converter can be estimated using Equation 35. For example, 15 $\mu$ F is an appropriate selection for 100mV RMS ripple on a 350kHz converter with 2A maximum load current and a transformer turns ratio of  $N_P/N_S = 2$ .

$$C_{IN} = \frac{0.5 \cdot I_{L(MAX)}}{f_{SW} \cdot V_{IN(RIPPLE)} \cdot (N_P / N_S)} \quad [35]$$

Table 3 provides some recommended ceramic capacitor vendors.

**Table 3. Recommended Ceramic Capacitor Manufacturers**

MANUFACTURER	WEB ADDRESS
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
TDK	www.tdk.com

### Inductor Selection

The inductor used with the LT8310 should have a saturation current rating appropriate to the maximum load current, and thus appropriate to the switch current rating and  $R_{SENSE}$  resistor. For applications with no output voltage feedback, choose an inductor value that keeps ripple current low in support of the minimum load current target,  $I_{L(MIN)}$ . If the contribution of the output inductor equals that of the reflected transformer magnetizing inductance ( $L\mu$ ), a first cut for the inductor value based on operating frequency, output voltage, and minimum duty cycle is:

$$L1 = \frac{V_{OUT} \cdot (1 - D_{MIN})}{f_{SW} \cdot I_{L(MIN)}} \quad [36]$$

Once both the transformer and inductor are chosen, the minimum load current estimate in Equation 27 should be re-evaluated, and the component selections modified if necessary.