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LINEAR TECHNOLOGY

High Voltage, High Current Buck-Boost Battery Charge Controller with Maximum Power Point Tracking (MPPT)

FEATURES

- V_{IN} Range: 6V to 80V
- V_{BAT} Range: 1.3V to 80V
- Single Inductor Allows V_{IN} Above, Below, or Equal to V_{BAT}
- Automatic MPPT for Solar Powered Charging
- Automatic Temperature Compensation
- No Software or Firmware Development Required
- Operation from Solar Panel or DC Supply
- Input and Output Current Monitor Pins
- Four Integrated Feedback Loops
- Synchronizable Fixed Frequency: 100kHz to 400kHz
- 64-Lead (7mm × 11mm × 0.75mm) QFN Package

APPLICATIONS

- Solar Powered Battery Chargers
- Multiple Types of Lead-Acid Battery Charging
- Li-Ion Battery Charger
- Battery Equipped Industrial or Portable Military Equipment

DESCRIPTION

The LT®8490 is a buck-boost switching regulator battery charger that implements a constant-current constant-voltage (CCCV) charging profile used for most battery types, including sealed lead-acid (SLA), flooded, gel and lithium-ion. The device operates from input voltages above, below or equal to the output voltage and can be powered by a solar panel or a DC power supply. On-chip logic provides automatic maximum power point tracking (MPPT) for solar powered applications. The LT8490 can perform automatic temperature compensation by sensing an external thermistor thermally coupled to the battery. STATUS and FAULT pins containing charger information can be used to drive LED indicator lamps. The device is available in a low profile (0.75mm) 7mm × 11mm 64-lead QFN package.
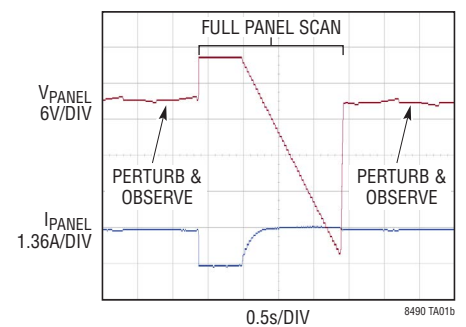
TYPICAL APPLICATION

Simplified Solar Powered Battery Charger Schematic

Maximum Power Point Tracking

BACK PAGE APPLICATION
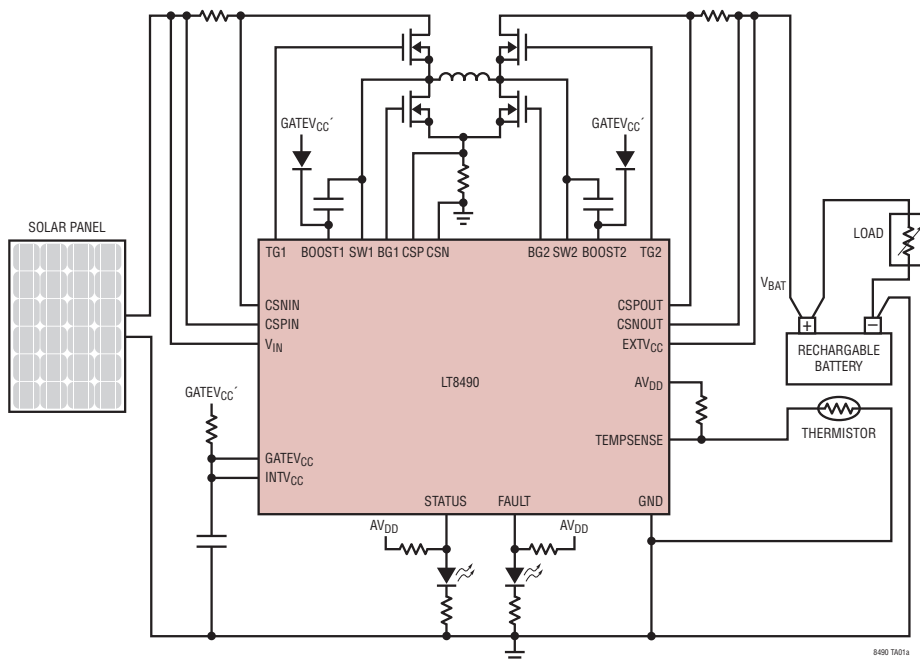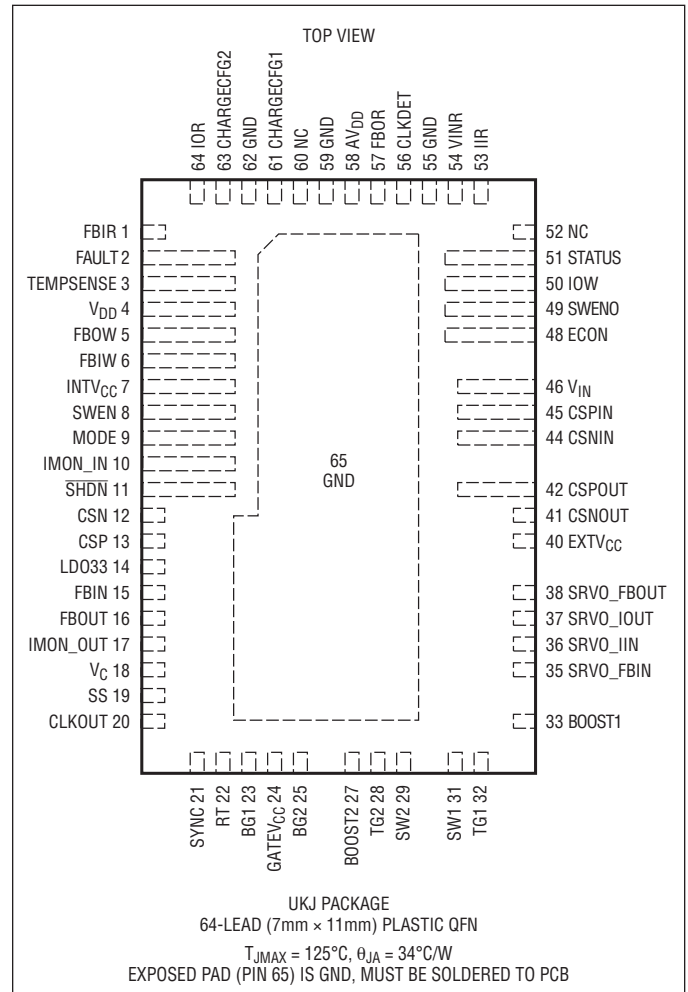
ABSOLUTE MAXIMUM RATINGS

(Note 1)

$V_{CSP} - V_{CSN}$, $V_{CSPIN} - V_{CSNIN}$,
$V_{CSPOUT} - V_{CSNOUT}$ .... −0.3V to 0.3V
SS, CLKOUT, CSP, CSN Voltage .... −0.3V to 3V
V_C Voltage (Note 2) .... −0.3V to 2.2V
LDO33, V_{DD}, AV_{DD} Voltage .... −0.3V to 5V
RT, FBOUT Voltage .... −0.3V to 5V
IMON_IN, IMON_OUT Voltage .... −0.3V to 5V
SYNC Voltage .... −0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage .... −0.3V to 7V
$V_{BOOST1} - V_{SW1}$, $V_{BOOST2} - V_{SW2}$ .... −0.3V to 7V
SWEN, MODE Voltage .... −0.3V to 7V
SRVO_FBIN, SRVO_FBOUT Voltage .... −0.3V to 30V
SRVO_IIN, SRVO_IOUT Voltage .... −0.3V to 30V
FBIN, $\overline{SHDN}$ Voltage .... −0.3V to 30V
CSNIN, CSPIN, CSPOUT, CSNOUT Voltage .. −0.3V to 80V
V_{IN}, $EXTV_{CC}$ Voltage .... −0.3V to 80V
SW1, SW2 Voltage .... 81V (Note 5)
BOOST1, BOOST2 Voltage .... −0.3V to 87V
BG1, BG2, TG1, TG2 .... (Note 4)
IOW, ECON, CLKDET Voltage .... −0.3V to V_{DD} + 0.5V
SWENO, STATUS Voltage .... −0.3V to V_{DD} + 0.5V
FBOW, FBIW, FAULT Voltage .... −0.3V to V_{DD} + 0.5V
VINR, FBOR, IIR, IOR Voltage .... −0.3V to V_{DD} + 0.5V
TEMPSENSE Voltage .... −0.3V to V_{DD} + 0.5V
CHARGECFG2,
CHARGECFG1 Voltage .... −0.3V to V_{DD} + 0.5V

Operating Junction Temperature Range
    LT8490E (Notes 1, 3) .... −40°C to 125°C
    LT8490I (Notes 1, 3) .... −40°C to 125°C
Storage Temperature Range .... −65°C to 150°C

PIN CONFIGURATION

TOP VIEW

Pins (left side, top to bottom): FBIR 1, FAULT 2, TEMPSENSE 3, V_{DD} 4, FBOW 5, FBIW 6, $INTV_{CC}$ 7, SWEN 8, MODE 9, IMON_IN 10, $\overline{SHDN}$ 11, CSN 12, CSP 13, LDO33 14, FBIN 15, FBOUT 16, IMON_OUT 17, V_C 18, SS 19, CLKOUT 20

Pins (top, left to right): 64 IOR, 63 CHARGECFG2, 62 GND, 61 CHARGECFG1, 60 NC, 59 GND, 58 AV_{DD}, 57 FBOR, 56 CLKDET, 55 GND, 54 VINR, 53 IIR

Pins (right side, top to bottom): 52 NC, 51 STATUS, 50 IOW, 49 SWENO, 48 ECON, 46 V_{IN}, 45 CSPIN, 44 CSNIN, 42 CSPOUT, 41 CSNOUT, 40 $EXTV_{CC}$, 38 SRVO_FBOUT, 37 SRVO_IOUT, 36 SRVO_IIN, 35 SRVO_FBIN, 33 BOOST1

Pins (bottom, left to right): SYNC 21, RT 22, BG1 23, $GATEV_{CC}$ 24, BG2 25, BOOST2 27, TG2 28, SW2 29, SW1 31, TG1 32

65 GND

UKJ PACKAGE
64-LEAD (7mm × 11mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8490EUKJ#PBF	LT8490EUKJ#TRPBF	LT8490UKJ	64-Lead (7mm × 11mm) Plastic QFN	−40°C to 125°C
LT8490IUKJ#PBF	LT8490IUKJ#TRPBF	LT8490UKJ	64-Lead (7mm × 11mm) Plastic QFN	−40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supply and Regulators						
V_{IN} Operating Voltage Range (Note 7)		●	6		80	V
V_{IN} Quiescent Current	Not Switching, V_{EXTVCC} = 0, V_{DD} = AV_{DD} = Float			2.65	4.2	mA
V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
V_{DD} Quiescent Current	I_{AVDD} + I_{VDD}, V_{DD} = AV_{DD} = 3.3V	●	2.5	4	6.5	mA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.18		V
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			−0.25	−1	%
LDO33 Pin Current Limit		●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device	●	1.184	1.234	1.284	V
$\overline{SHDN}$ Input Voltage High Hysteresis				50		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current	●			0.35	V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 11	1 22	µA µA
SWEN Rising Threshold Voltage		●	1.156	1.206	1.256	V
SWEN Threshold Voltage Hysteresis				22		mV
MODE Pin Thresholds	Discontinuous Mode Forced Continuous Mode	● ●	 0.4		2.3 	V V
IMON_OUT Rising threshold for CCM Operation	MODE = 0V	●	168	195	224	mV
IMON_OUT Falling threshold for DCM	MODE = 0V	●	95	122	150	mV
Voltage Regulation						
Regulation Voltage for FBOUT	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.193	1.207	1.222	V
Regulation Voltage for FBIN	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.184	1.205	1.226	V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBIN Pin Bias Current	Current Out of Pin			10		nA
Current Regulation						
Regulation Voltage for IMON_IN and IMON_OUT	V_C = 1.2V, $EXTV_{CC}$ = 0V	●	1.187	1.208	1.229	V
IMON_IN Output Current	$V_{CSPIN} - V_{CSNIN}$ = 50mV, V_{CSPIN} = 5.025V $V_{CSPIN} - V_{CSNIN}$ = 50mV, V_{CSPIN} = 5.025V $V_{CSPIN} - V_{CSNIN}$ = 0mV, V_{CSPIN} = 5V	 ● ●	54 53 2.5	57 57 7	60 61 11.5	µA µA µA
IMON_IN Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_OUT Output Current	$V_{CSPOUT} - V_{CSNOUT}$ = 50mV, V_{CSPOUT} = 5.025V $V_{CSPOUT} - V_{CSNOUT}$ = 50mV, V_{CSPOUT} = 5.025V $V_{CSPOUT} - V_{CSNOUT}$ = 5mV, V_{CSPOUT} = 5.0025V $V_{CSPOUT} - V_{CSNOUT}$ = 5mV, V_{CSPOUT} = 5.0025V	 ● ●	47.5 47 3.25 2.75	50 50 5 5	52.5 54.25 6.75 8	µA µA µA µA
IMON_OUT Overvoltage Threshold		●	1.55	1.61	1.67	V

ELECTRICAL CHARACTERISTICS
The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{DD} = AV_{DD} = 3.3V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator Oscillator (OSC1)						
Switch Frequency Range	Syncing or Free Running		100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365k	●	102	120	142	kHz
	R_T = 215k	●	170	202	235	kHz
	R_T = 124k	●	310	350	400	kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Min SYNC Ratio, f_{SYNC}/f_{OSC}				3/4		
CLKOUT Output Voltage HIGH	1mA Out of CLKOUT Pin		2.3	2.45	2.55	V
CLKOUT Output Voltage LOW	1mA into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = −40°C			22.7		%
	T_J = 25°C			44.1		%
	T_J = 125°C			77		%
Charging Control						
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output Low Voltage	I_{OL} = 5mA	●		0.22	0.5	V
STATUS, FBOW, FBIW, SWENO, IOW, ECON Output High Voltage	I_{OH} = −5mA	●	2.7	3.0		V
FAULT Output Voltage Low	I_{OL} = 0.5mA	●		0.1	0.25	V
FAULT Output Voltage High	I_{OH} = −0.1mA	●	1.7	2.2		V
Power Supply Mode Detection Threshold (Note 6)	VINR Pin Falling	●	155	174		mV
Power Supply Mode Detection Threshold Hysteresis (Note 6)	VINR Pin			29		mV
Minimum VINR Voltage for Start-Up (Note 6)	Not in Power Supply Mode					
	Low Power Mode Enabled	●	380	395	410	mV
	Low Power Mode Disabled	●	213	225	237	mV
High Charging Current Threshold on IOR (Note 6)	IOR Rising → ECON Rising	●	168	195	224	mV
Low Charging Current Threshold on IOR (Note 6)	IOR Falling → ECON Falling	●	95	122	150	mV
Minimum CHARGECFG1 % of AV_{DD} to Disable Stage 3 (Note 6)	Temperature Compensation Enabled	●	94	95	96	%
Maximum CHARGECFG1 % of AV_{DD} to Disable Stage 3 (Note 6)	Temperature Compensation Disabled	●	4	5	6	%
Minimum CHARGECFG2 % of AV_{DD} to Disable Time Limits (Note 6)	Wide Valid Temperature Range	●	94	95	96	%
Maximum CHARGECFG2 % of AV_{DD} to Disable Time Limits (Note 6)	Narrow Valid Temperature Range	●	4	5	6	%
Minimum TEMPSENSE % of AV_{DD} to Detect Battery Disconnected (Note 6)		●	94.5	96	97.5	%
$V_{CSPOUT} - V_{CSNOUT}$ Threshold for C/5 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		9	10	11	mV
$V_{CSPOUT} - V_{CSNOUT}$ Threshold for C/10 Detection (Note 6)	V_{CSxOUT} Common Mode = 5.0V, IOR Falling, R_{TOTAL} from IMON_OUT to Ground = 24.3kΩ		4.25	5	5.75	mV
FBIW, FBOW PWM Frequency (OSC2)				31.25		kHz
FBIW, FBOW PWM Resolution				8		Bits
STATUS UART Bit Rate		●	2160	2400	2640	Baud
Internal A/D Resolution				10		Bits

8490fa

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8490E is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8490I is guaranteed over the full –40°C to 125°C junction temperature range.

Note 4: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

Note 5: Negative voltages on the SW1 and SW2 pins are limited in the applications by the body diodes of the external NMOS devices M2 and M3 or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

Note 6: These thresholds are measured by the internal A-D converter. The A-D reference voltage is AV_{DD}. AV_{DD}, V_{DD} and an additional 2.8mA load are regulated by LDO33 to create the AV_{DD} reference for these measurements. The absolute threshold voltages will shift with corresponding changes in the AV_{DD} voltage.

Note 7: 10V minimum V_{IN} required for solar powered start-up if low power mode is enabled.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

Solar Powered Charging Lead Acid Battery "A"

PARTLY CLOUDY

V_{BAT}

I_{BAT}

SUNSET

SOME TRANSIENTS FROM FULL PANEL SCANS REMOVED FOR CLARITY.

STAGE

V_{BAT} (V) AND I_{BAT} (A)

CHARGING STAGE

9AM   TIME OF DAY   6PM
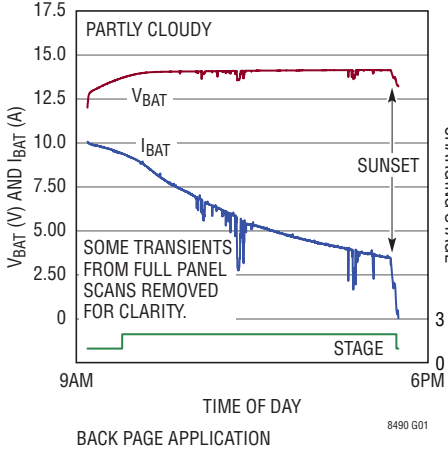
BACK PAGE APPLICATION

8490 G01

Solar Powered Charging Lead Acid Battery "B"

CLOUDY DAY

V_{BAT}

SOME TRANSIENTS FROM FULL PANEL SCANS REMOVED FOR CLARITY.

SUNSET

I_{BAT}

STAGE

V_{BAT} (V) AND I_{BAT} (A)

CHARGING STAGE

10AM   TIME OF DAY   6PM
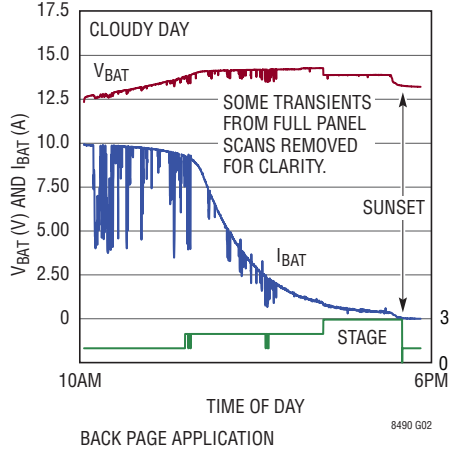
BACK PAGE APPLICATION

8490 G02

Solar Powered Charging Lithium Ion Battery

PARTLY CLOUDY

STAGE 1   STAGE 2

V_{BAT}

SOME TRANSIENTS FROM FULL PANEL SCANS REMOVED FOR CLARITY.

I_{BAT}

UART AND STATUS INDICATE < C/10

V_{BAT} (V)

I_{BAT} (A)

1PM   TIME OF DAY   5PM
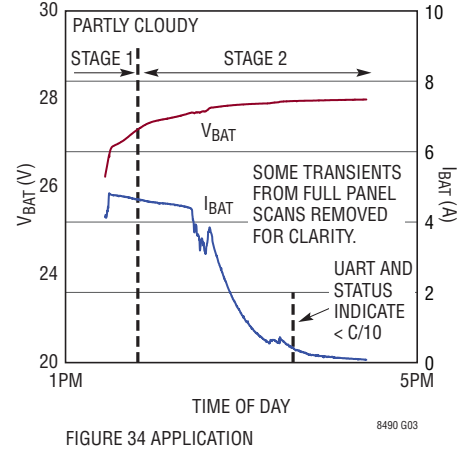
FIGURE 34 APPLICATION

8490 G03

Power Supply Mode Charging Lead Acid Battery "B"

V_{BAT}

STAGE 1   STAGE 2   STAGE 3

I_{BAT}

V_{IN} = 36V

V_{BAT} (V) AND I_{BAT} (A)

0   CHARGING TIME (HOURS)   12
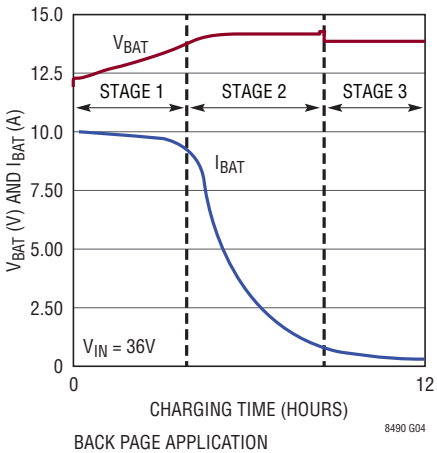
BACK PAGE APPLICATION

8490 G04

STATUS V_{OH} and V_{OL} ($V_{DD} = AV_{DD} = 3.3V$)

V_{OH}

−40°C

125°C   25°C

125°C   25°C

V_{OL}

−40°C

V_{STATUS} (V)

$|I_{STATUS}|$ (mA)
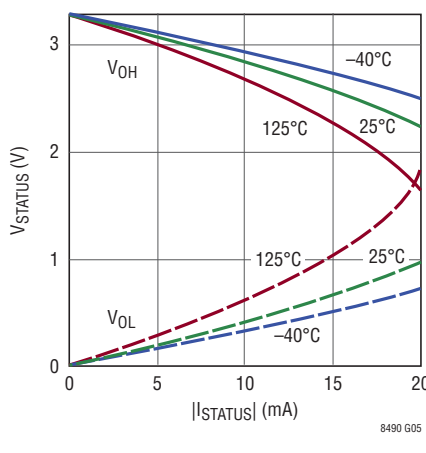
8490 G05

FAULT V_{OH} and V_{OL} ($V_{DD} = AV_{DD} = 3.3V$)

V_{OH}

−40°C   25°C

125°C

25°C

125°C

V_{OL} −40°C

V_{FAULT} (V)

$|I_{FAULT}|$ (mA)
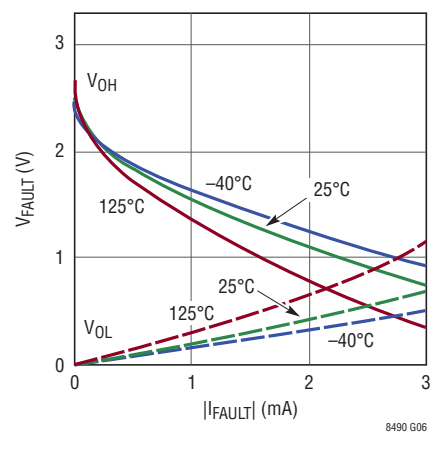
8490 G06

LDO33 Load Regulation (Not Connected to AV_{DD} and V_{DD})

25°C

125°C

−40°C

LDO33 (V)

LOAD CURRENT (mA)
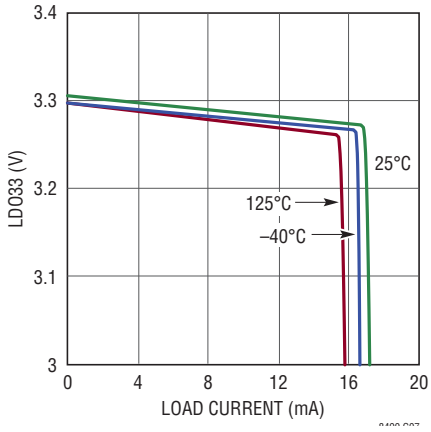
8490 G07

IMON Output Currents

IMON_IN

IMON_OUT

PIN CURRENT (µA)

CSxIN-CSxOUT (mV)
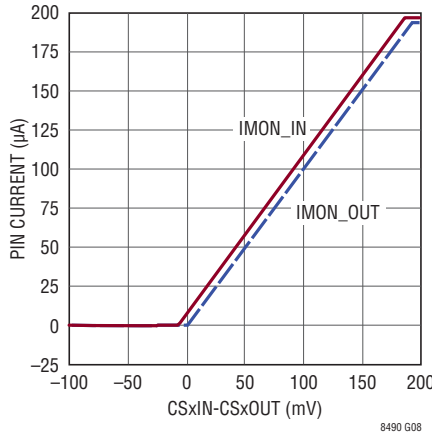
8490 G08

FBOUT, FBIN, IMONIN, IMONOUT Voltage Rise vs Power

$INTV_{CC}$ REGULATED FROM V_{IN}

$INTV_{CC}$ REGULATED FROM $EXTV_{CC}$

VOLTAGE RISE (%)

$INTV_{CC}$ REGULATOR POWER (W)
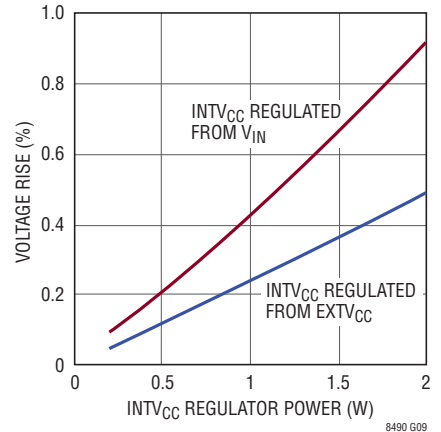
8490 G09

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, unless otherwise noted.

Maximum Power Point Tracking
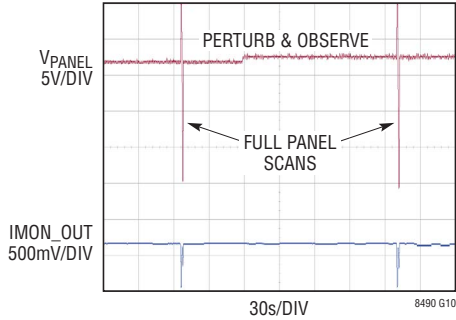
V_{PANEL} 5V/DIV

PERTURB & OBSERVE

FULL PANEL SCANS

I_{MON_OUT} 500mV/DIV

30s/DIV
8490 G10
FIGURE 34 APPLICATION

Perturb and Observe

V_{PANEL} 5V/DIV

I_{MON_OUT} 200mV/DIV

0.5s/DIV
8490 G11
FIGURE 34 APPLICATION

Perturb and Observe

V_{PANEL} 5V/DIV

IMON_OUT 100mV/DIV

0.5s/DIV
8490 G12
FIGURE 34 APPLICATION
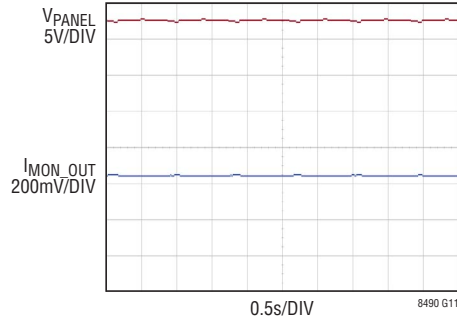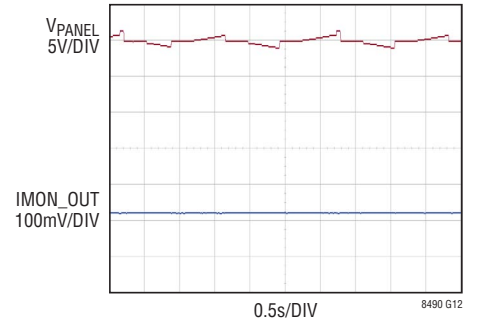
Perturb and Observe Maximum Power Point Tracking

V_{PANEL} 6V/DIV

ROTATE PANEL TOWARDS THE SUN. PANEL VOLTAGE AND CURRENT ARE AUTOMATICALLY ADJUSTED TO NEW MAX.

IMON_OUT 100mV/DIV
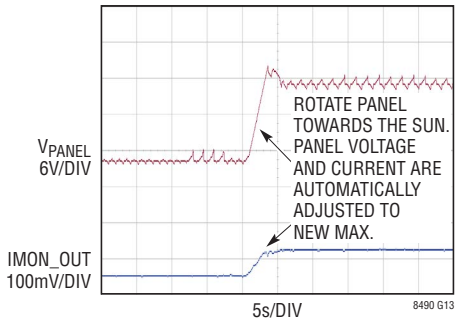
5s/DIV
8490 G13
FIGURE 34 APPLICATION

Full Panel Scan Single Power Peak

V_{PANEL} 10V/DIV

POWER PEAK

IMON_OUT 500mV/DIV

IMON_IN 500mV/DIV
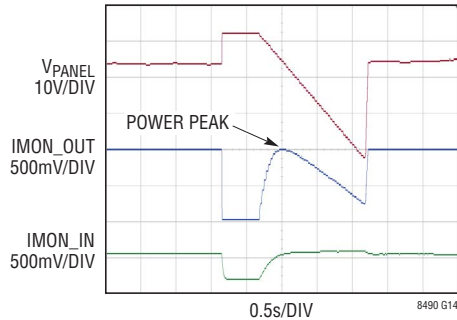
0.5s/DIV
8490 G14
FIGURE 34 APPLICATION

Full Panel Scan—Partially Shaded with Dual Power Peaks
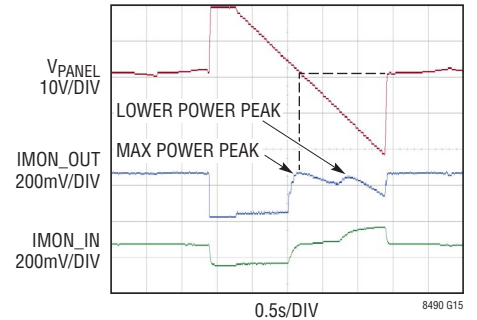
V_{PANEL} 10V/DIV

LOWER POWER PEAK

MAX POWER PEAK

IMON_OUT 200mV/DIV

IMON_IN 200mV/DIV

0.5s/DIV
8490 G15
FIGURE 34 APPLICATION

Panel Voltage in Low Power Mode

IMON_OUT 50mV/DIV

10.6mV

V_{PANEL} 5V/DIV

17.6V

10.4V

SWEN 5V/DIV

3.3V

40ms/DIV
8490 G16
FIGURE 34 APPLICATION

Panel Voltage in Low Power Mode

IMON_OUT 50mV/DIV

10.6mV

V_{PANEL} 5V/DIV

10.1V

SWEN 5V/DIV

3.3V
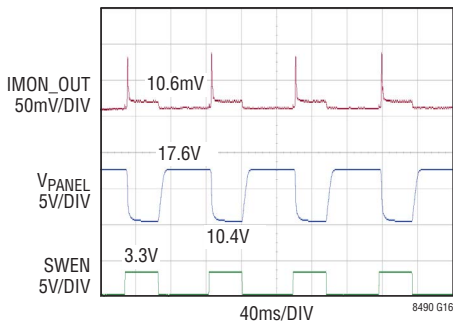
40ms/DIV
8490 G17
FIGURE 34 APPLICATION

PIN FUNCTIONS

FBIR (Pin 1): A/D Input Pin. Connects to FBIN pin to measure input feedback voltage.

FAULT (Pin 2): FAULT Pin. This pin generates an active high digital output that, when used with an LED, provides a visual indication of a fault event.

TEMPSENSE (Pin 3): A/D Input Pin. Connects to a thermistor divider network for sensing battery temperature or a resistor divider if unused. This pin is frequently monitored for temperature compensation and enforcing temperature limits.

V_{DD} (Pin 4): Control Logic Power Supply Pin. Connect this pin to LDO33 and AV_{DD}.

FBOW (Pin 5): PWM Digital Output Pin. Connects to FBOUT through an RCR network to temperature compensate the battery voltage.

FBIW (Pin 6): PWM Digital Output Pin. Connects to FBIN through an RCR network to adjust the solar panel voltage for MPPT.

$INTV_{CC}$ (Pin 7): Internal 6.35V Regulator Output Pin. Connects to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{IN}. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor. See Switching Configuration - MODE Pin for additional details.

SWEN (Pin 8): Switch Enable Pin. Tie to the SWENO pin.

MODE (Pin 9): Mode Pin. The voltage applied to this pin sets the operating mode of the switching regulator. Tie this pin to $INTV_{CC}$ to make discontinuous current mode active. Tie this pin to ground to operate in discontinuous current mode for low battery charging currents and continuous current mode for high battery charging currents. Do not float this pin. See Switching Configuration - MODE Pin for additional details.

IMON_IN (Pin 10): Input Current Monitor Pin. The current out of this pin is proportional to the input current. See the Applications Information section for more information.

SHDN (Pin 11): Shutdown Pin. In conjunction with the UVLO (undervoltage lockout) circuit, this pin is used to enable/disable the chip. Do not float this pin.

CSN (Pin 12): The (−) Input to the Inductor Current Sense and Reverse Current Detect Amplifier.

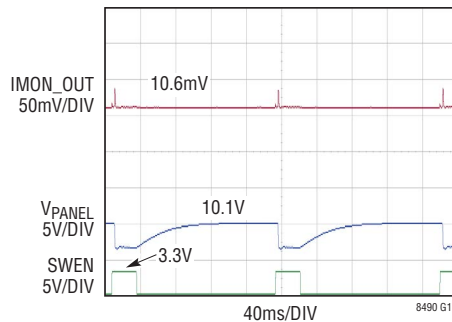**CSP (Pin 13):** The (+) Input to the Inductor Current Sense and Reverse Current Detect Amplifier. The V_C pin voltage and built-in offsets between the CSP and CSN pins set the current trip threshold.

LDO33 (Pin 14): 3.3V Regulator Output. This supply provides power to the V_{DD} and AV_{DD} pins. Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

FBIN (Pin 15): Input Feedback Pin. This pin is connected to the input error amplifier input.

FBOUT (Pin 16): Output Feedback Pin. This pin connects the error amplifier input to an external resistor divider from the output.

IMON_OUT (Pin 17): Output Current Monitor Pin. The current out of this pin is proportional to the average output current. See the Applications Information section for more information.

V_C (Pin 18): Error Amplifier Output Pin. Tie the external compensation network to this pin.

SS (Pin 19): Soft-Start Pin. Place 100nF of capacitance from this pin to ground. Upon start-up, this pin will be charged by an internal resistor to 2.5V.

CLKOUT (Pin 20): Switching Regulator Clock Output Pin. CLKOUT will toggle at the same frequency as the switching regulator oscillator (OSC1 on the Block Diagram) or as the SYNC pin, but is approximately 180° out-of-phase. CLKOUT can also be used as a temperature monitor of the switching regulator since the CLKOUT duty cycle varies linearly with the junction temperature of the switching regulator. It is connected to CLKDET through an RC filter. The CLKOUT pin can drive capacitive loads up to 200pF.

SYNC (Pin 21): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock (OSC1 in the Block Diagram).

PIN FUNCTIONS

RT (Pin 22): Timing Resistor Pin. Adjusts the switching regulator frequency (OSC1) when SYNC is not driven by a clock. Place a resistor from this pin to ground to set the free-running frequency of OSC1. Do not float this pin.

BG1, BG2 (Pin 23/Pin 25): Bottom Gate Drive. Drives the gates of the bottom N-channel MOSFETs between ground and GATEV$_{CC}$.

GATEV$_{CC}$ (Pin 24): Power Supply for Gate Drivers. Must be connected to the INTV$_{CC}$ pin. Do not power from any other supply. Locally bypass to ground.

BOOST1, BOOST2 (Pin 33/Pin 27): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below GATEVcc up to V$_{IN}$ + GATEV$_{CC}$. The BOOST2 pin swings from a diode voltage below GATEV$_{CC}$ up to V$_{BAT}$ + GATEV$_{CC}$.

TG1, TG2 (Pin 32/Pin 28): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to GATEV$_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pin 31/Pin 29): Switch Nodes. The (–) terminal of the bootstrap capacitors connect here.

SRVO_FBIN (Pin 35): Open-Drain Logic Output. This pin is pulled to ground when the input voltage feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_IIN (Pin 36): Open-Drain Logic Output. This pin is pulled to ground when the input current feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_IOUT (Pin 37): Open-Drain Logic Output. This pin is pulled to ground when the output current feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

SRVO_FBOUT (Pin 38): Open-Drain Logic Output. This pin is pulled to ground when the output voltage feedback loop is active. This pin is unused for most LT8490 applications and can be floated.

EXTV$_{CC}$ (Pin 40): External V$_{CC}$ Input. When EXTV$_{CC}$ exceeds 6.4V (typical), INTV$_{CC}$ will be powered from this pin. When EXTV$_{CC}$ is lower than 6.22V (typical), INTV$_{CC}$ will be powered from V$_{IN}$. See Switching Configuration - MODE Pin for additional details.

CSNOUT (Pin 41): The (–) Input to the Output Current Sense Amplifier.

CSPOUT (Pin 42): The (+) Input to the Output Current Sense Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor to provide the output current signals.

CSNIN (Pin 44): The (–) Input to the Input Current Sense Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor to provide the instantaneous input current signals.

CSPIN (Pin 45): The (+) Input to the Input Current Sense Amplifier.

V$_{IN}$ (Pin 46): Main Input Supply Pin. Must be bypassed to local ground plane.

ECON (Pin 48): Digital Output Pin. Optional control output signal used to disconnect EXTV$_{CC}$ from the battery when the average charge current drops below a predetermined threshold.

SWENO (Pin 49): Digital Output Pin. Connect to SWEN. Enables the switching regulator. A 200kΩ pull-down resistor is required from this pin to ground.

IOW (Pin 50): Digital Output Pin. Connects to IMON_OUT through a resistor. By switching the pin between logic low and high impedance, the total R$_{IMON\_OUT}$ changes, which changes the output current limit.

STATUS (Pin 51): Digital Output Pin. When used with an LED, this signal provides a visual indication of the progress of the charging algorithm. In addition, STATUS transmits two UART bytes (8 bits, no parity, one stop bit, 2400 baud) every 3.5 seconds (typical), which indicates status and fault information.

IIR (Pin 53): A/D Input Pin. Connects to IMON_IN to read input current. Used to manage MPPT.

PIN FUNCTIONS

VINR (Pin 54): A/D Input Pin. Connects to resistive divider on VIN to measure input voltage. Used to manage MPPT and start-up.

CLKDET (Pin 56): A/D Input Pin. Connects to CLKOUT through an RC filter to detect the duty cycle of CLKOUT. Used to manage start-up.

FBOR (Pin 57): A/D Input Pin. Connects to FBOUT pin to read charger output voltage. Used to manage the charging algorithm.

AV$_{DD}$ (Pin 58): A/D Positive Reference Pin. Tie this pin to V$_{DD}$ and LDO33.

CHARGECFG1 (Pin 61): A/D Input Pin. Used to configure the float voltage, temperature compensation and enable stage 3 charging.

CHARGECFG2 (Pin 63): A/D Input Pin. Used to configure time limits and the valid battery temperature range.

IOR (Pin 64): A/D Input Pin. Connects to IMON_OUT pin to read the charger output current. Used to manage the charging algorithm.

GND (Exposed Pad 65 and Pins 55, 59, 62): Ground. Tie directly to local ground plane.

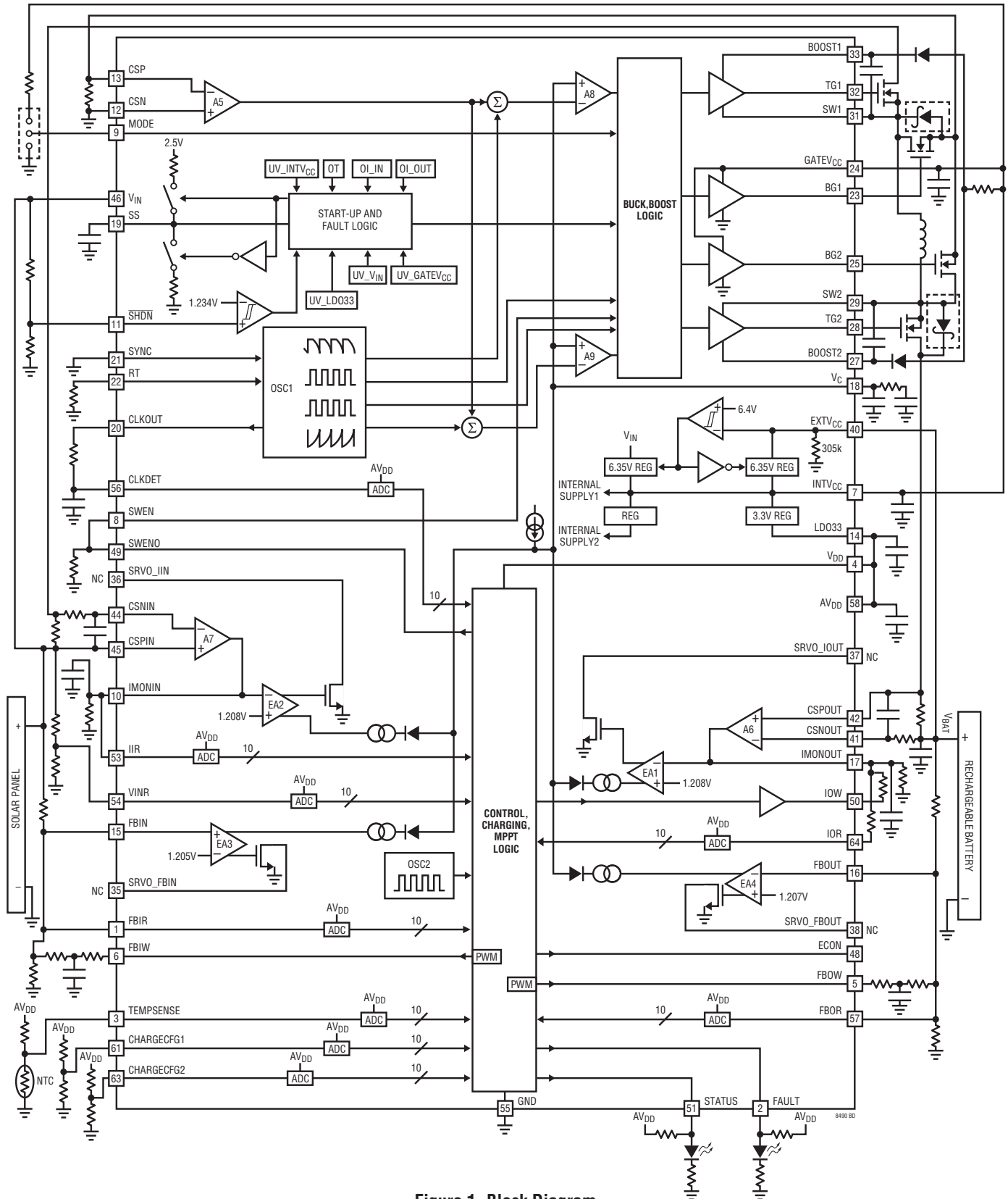**NC (Pins 52, 60):** Not connected.

BLOCK DIAGRAM

Figure 1. Block Diagram

OPERATION

Overview

The LT8490 is a powerful and easy to use battery charging controller with automatic maximum power point tracking (MPPT) and temperature compensation. The LT8490 is based on the LT8705 buck-boost controller with additional battery charging and MPPT control functions. Refer to the LT8705 data sheet for more detailed information about the switching regulator portions of the LT8490. Several reference applications are included in this data sheet to simplify system design. Many battery charging applications can be implemented using one of the reference applications with little or no modification required. Configuration for the various charging parameters is implemented in the hardware. No software or firmware development is required.

The LT8490 includes four different forms of regulation: output current, input current, input voltage and output voltage (EA1-EA4 respectively as shown in Figure 1). Whichever form of regulation requires the lowest voltage on the V_C pin limits the commanded inductor current. When powered by a solar panel, the MPPT function uses input voltage regulation to locate and track the maximum power point of the panel. Input current regulation is used to limit the maximum current drawn from the input supply. The output current regulation limits the battery charging current, and the output voltage regulation is used to set the maximum battery charging voltage.

The LT8490 offers user configurable timers that can be enabled with the appropriate resistor divider on the CHARGECFG2 pin. If a timer has been set and expires, the LT8490 will halt charging and communicate this through the STATUS and FAULT pins. Options for automatic restart of the charge cycle are discussed later in the Automatic Charger Restart and Fault Recovery section.

The LT8490 also includes a TEMPSENSE pin, which can be connected to an NTC resistor divider network thermally coupled to the battery pack. When connected, the TEMPSENSE pin can provide temperature compensated charging and/or can be used to disable charging when the battery is outside of safe temperature limits. The presence of the NTC resistor can also give an indication to the charger if the battery is connected or not.

The LT8490 also provides charging status and fault indicators through the STATUS and FAULT pins. The behavior of these pins is described in the STATUS and FAULT Indicators section.

Battery Charging Algorithm

The LT8490 implements a CCCV charging algorithm. The idealized charging profile is shown in Figure 2 and assumes constant temperature and adequate input power. As battery temperature and illumination conditions on the panel change, the actual current and voltage seen by the battery will vary accordingly.

After start-up, the LT8490 frequently measures the battery voltage and charging current to determine the proper charging stage.
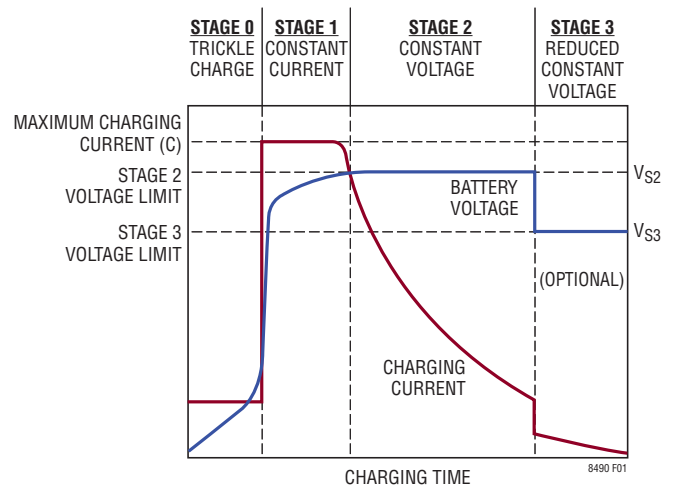

Figure 2. Typical Battery Charging Cycle

OPERATION

STAGE 0: In Stage 0 (reduced constant-current/trickle charge) the LT8490 charges the battery with a hardware configurable reduced constant current. This trickle charge stage occurs for battery voltages between 35% to 70% (typical) of the Stage 2 voltage limit (V_{S2}).

STAGE 1: In Stage 1 (full constant-current) the LT8490 charges the battery with a hardware configurable constant current equal to or higher than in Stage 0. This constant current stage occurs for battery voltages between 70% to 98% (typical) of the Stage 2 voltage limit. This charging stage is often referred to as bulk charging. This charging stage will be called Stage 1 for the remainder of this document.

STAGE 2: In Stage 2 (constant-voltage) the LT8490 charges the battery with a hardware configurable constant voltage. This constant voltage stage occurs for battery voltages above 98% (typical) of the Stage 2 voltage limit. This charging stage is often referred to as float charging for lithium-ion batteries and absorption charging for lead-acid batteries. To avoid confusion, this charging stage will be called Stage 2 for the remainder of this document.

If the optional Stage 3 is enabled, the LT8490 will proceed from Stage 2 to Stage 3 when the charging current drops below C/10. Other conditions for exiting Stage 2 depend on whether time limits are enabled for the charger. See the Charging Time Limits section for more details about Stage 2 termination.

STAGE 3 (OPTIONAL): Stage 3 is optional as configured with the CHARGECFG1 pin. In Stage 3 the LT8490 charges the battery with a hardware configurable reduced constant voltage. This charging stage is often referred to as float charging in lead-acid battery charging. This charging stage will be called Stage 3 for the remainder of this document.

Charging will automatically restart if, during Stage 3, the charging current exceeds C/5 or the battery voltage falls below 96% (typical) of the Stage 3 voltage limit (V_{S3}). In addition, an optional time limit can be enabled to terminate charging in Stage 3. See the Charging Time Limits section for more details about Stage 3 termination.

Table 1. Description of LT8490 Charging Stages

STAGE	NAME	METHOD	DURATION
0	Trickle Charge	Constant Current at a Configured Fraction of Full Charge Current	Until Battery Voltage Rises Above V_{S0} (70% of Stage 2 Voltage Limit)
			Optional Max Time Limit
1	Constant Current	Constant Full Charge Current	Until Battery Voltage Rises Above V_{S1} (98% of Stage 2 Voltage Limit)
			Optional Max Time Limit for Stage 1 + Stage 2
2	Constant Voltage	Constant Voltage	Until Charging Current Falls Below C/10 or Optional Indefinite Charging
			Optional Max Time Limit for Stage 1 + Stage 2
3 (Optional)	Reduced Constant Voltage	Constant Voltage at a Configured Fraction of Stage 2 Constant Voltage	Until Battery Voltage Falls below 96% of V_{S3} (Stage 3 Voltage Limit - Configurable) or Charging Current Rises Above C/5
			Optional Max Time Limit. The same duration as the Stage 1 + Stage 2 Time Limit.

Maximum Power Point Tracking

When powered by a solar panel, the LT8490 employs a proprietary Perturb and Observe algorithm for identifying the maximum power point. This algorithm provides accurate MPPT for slow to moderate changes in panel illumination. The panel is also scanned periodically to avoid settling on a false maximum power point for long periods of time, in the case of non-uniform panel illumination.

Fault Conditions

The LT8490 can indicate the presence of a fault condition through the STATUS and FAULT pins. These faults include: battery undervoltage, battery overtemperature, battery under temperature and timer expiration. Following a fault, the LT8490 will discontinue charging until the fault condition is removed, at which point it will continue or restart the charging cycle. See the Automatic Charger Restart and Fault Recovery section for more information.

APPLICATIONS INFORMATION

Input Voltage Sensing and Modulation Network

The passive component network shown in Figure 3 is required to properly measure and modulate the input supply voltage. This network is required whether the supply is a solar panel or a DC voltage source.
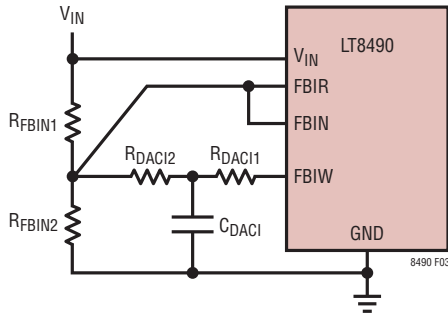

Figure 3. Input Feedback Resistor Network

Choosing the components requires knowing the maximum panel open-circuit voltage (V_{OCMAX}) as well as the maximum DC input supply voltage (V_{DCMAX}) desired (see the DC Supply Powered Charging section for more information). V_{OCMAX} typically occurs at cold temperatures and should be specified in the panel manufacturer's data sheet. Use the following equations to determine proper component values:

$$R_{FBIN1} = 100k \cdot \left[\frac{1 + \left(\frac{4.470V}{V_{MAX} - 6V} \right)}{1 + \left(\frac{5.593}{V_{MAX} - 6V} \right)} \right] \Omega$$

$$R_{DACI2} = 2.75 \cdot \left(\frac{R_{FBIN1}}{V_{MAX} - 6V} \right) \Omega$$

$$R_{FBIN2} = \frac{1}{\left(\frac{1}{100k - R_{FBIN1}} \right) - \left(\frac{1}{R_{DACI2}} \right)} \Omega$$

$$R_{DACI1} = 0.2 \cdot R_{DACI2} \Omega$$

$$C_{DACI} = \frac{1}{1000 \cdot R_{DACI1}} F$$

where V_{MAX} is the greater of V_{OCMAX} and V_{DCMAX} with some additional margin. These resistors should have a 1% tolerance or better.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to more closely match the calculated results. Otherwise, use standard resistor values and check the final results with the following equations:

$$V_{X2} = 1.205 \cdot \left[\frac{R_{FBIN1}}{R_{DACI1} + R_{DACI2}} + \left(\frac{R_{FBIN1}}{R_{FBIN2}} \right) + 1 \right]$$

V_{X2} indicates the actual V_{MAX} using the selected resistors. Make sure this result is greater than or equal to the desired V_{MAX} for the application.

$$V_{X1} = V_{X2} - 3.3 \cdot \left(\frac{R_{FBIN1}}{R_{DAC1} + R_{DAC2}} \right)$$

V_{X1} should be as close to 6V as possible. Iterations may be required to determine the best standard resistor values.

Table 2 shows good sets of standard value components for maximum input voltages of 20V, 40V, 60V and 80V. Iterative calculations were required to select these values that achieve the best overall results.

Table 2. Input Feedback Network vs Panel Voltage

V_{MAX} (V)	R_{FBIN1} (kΩ)	R_{FBIN2} (kΩ)	R_{DACI1} (kΩ)	R_{DACI2} (kΩ)	C_{DACI} (nF)
20	95.3	8.45	3.4	19.1	270
40	107	4.87	1.69	8.66	560
60	105	3.24	1.05	5.36	1000
80	133	3.09	1.05	4.87	1000

As discussed later in DC Supply Powered Charging, arbitrarily setting V_{MAX} to 80V may not result in the best operation of the LT8490 for all conditions, particularly at low input voltages. Be sure to give proper consideration to the required voltage range for each application.

Solar Powered Charging

VINR DIVIDER NETWORK: The LT8490 can be powered by a solar panel or a DC power supply. As discussed later in DC Supply Powered Charging, the VINR pin must be pulled low when being powered by a DC supply. Otherwise, VINR must be connected to the resistor divider network as shown in Figure 4.
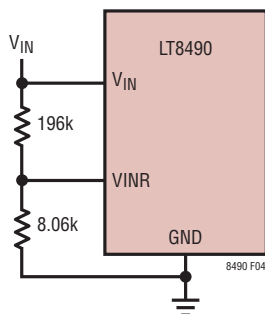
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APPLICATIONS INFORMATION

Figure 4. VINR Resistor Divider Circuit

The LT8490 uses this divider network to measure absolute panel voltage (as part of its maximum power point calculations) and to check for adequate input voltage to operate the charger. These resistors should have a 1% tolerance or better.

TIMER TERMINATION DISABLED: When powered by a solar panel, the timer termination option (see the Charging Time Limits section for more detail) is automatically disabled. This is due to the inability to guarantee full charging current during the entire charging cycle in cases where the panel illumination conditions change. In addition, the timers can reset if all power to the charger is lost due to insufficient lighting. This makes the use of timer termination potentially unreliable in solar powered applications.

C/10 DETECTION: When powered by a solar panel, charging current may drop below C/10 because the battery is approaching full charge, or because the solar panel has insufficient lighting. If sufficient panel power is available, the LT8490 can determine if the charging current has dropped below C/10 due to the battery approaching full charge. In this case, the charger will proceed from Stage 2 to the next appropriate stage. If the LT8490 is able to determine that the charging current has dropped below C/10 due to insufficient panel power, the charger will continue operating in Stage 2.

MINIMUM PANEL VOLTAGE REQUIREMENT: A minimum panel voltage of 6V is required to operate the charger. However, higher panel voltages are required in various other cases.

1. LOW POWER MODE ENABLED: Low power mode allows additional power to be recovered from the solar panel under very weak lighting conditions. When low power mode is enabled, the panel voltage must initially exceed 10V (typical – as measured through the VINR pin) before the charger will attempt to charge the battery. Read the Optional Low Power Mode section for more details.

2. LOW POWER MODE DISABLED: If low power mode is disabled the charger will attempt to charge the battery as long as the panel is above 6V. However, if sufficient panel current is not detected the LT8490 will temporarily stop charging. The charger will check for sufficient panel current at 30 second intervals (typical) or will check sooner if the LT8490 detects either a significant rise in panel voltage or a significant fall in battery voltage.

3. LOW INPUT VOLTAGE EFFECTS: Figure 5 shows the minimum input voltage, below which the maximum charging current can be reduced. This limit is a function of the input V_{MAX} as discussed previously in the Input Voltage and Modulation Network section. Maximum charging current can reduce as FBIN gets closer to its regulation voltage of 1.205V (typical). This is not normally a significant issue unless 1) the charger is powered by a low voltage DC power supply or 2) a low voltage panel is used with a charger that was configured for a much higher voltage panel. The farther that V_{IN} is below the Normal Configuration line in Figure 5 the more the current can reduce.
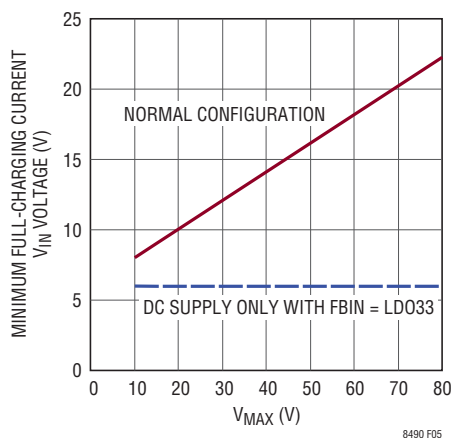

Figure 5. Minimum Full Charging Current V_{IN} Voltage

APPLICATIONS INFORMATION

When V_{IN} is powered by a DC voltage supply, maintain V_{IN} higher than the Normal Configuration line in Figure 5. Operating V_{IN} below this line can reduce the maximum charging current and the V_{S2} and V_{S3} charging voltages. If V_{IN} is never going to be supplied by a solar panel then FBIN can be disconnected from FBIR (see Figure 3) and reconnected to the LDO33 pin. This allows the charger to operate with V_{IN} as low as 6V with no charging current or voltage reduction.

When using a solar panel supply, choose a panel having a maximum open-circuit voltage (V_{OC}) close to V_{MAX} (discussed in the prior Input Voltage Sensing and Modulation Network section). The maximum power point voltage is typically well above the voltage limit in Figure 5 and current limiting is rarely an issue. Avoid using solar panels that operate dramatically below V_{MAX}, particularly if the maximum power point voltage is typically below the Normal Configuration line in Figure 5.

DC Supply Powered Charging

SELECTING POWER SUPPLY MODE: When powered by a DC voltage source, the VINR pin must be pulled below 174mV (typical) to activate power supply mode. This disables unnecessary solar panel functions and allows the LT8490 to operate properly from a DC voltage source. If the application is never powered by a solar panel, VINR can be grounded. If the application is only powered by a solar panel, then connect VINR as shown in Figure 4. Otherwise, see the Optional DC Supply Detection Circuit section for a method to pull down the VINR pin when a DC supply is detected.

MINIMUM INPUT VOLTAGE REQUIREMENT: When power supply mode is enabled, the LT8490 will operate from an input as low as 6V. However, charging current capability can become limited at low input voltages depending on the V_{MAX} voltage used to select the input voltage sensing network (see previous Input Voltage Sensing and Modulation Network section). Figure 5 shows the minimum input supply voltage required, below which charging current can become less than the maximum output current limit. If the LT8490 is powered by a DC supply only, the minimum input voltage shown in Figure 5 can be reduced to 6V by

(1) disconnecting FBIN from FBIR and (2) connecting the FBIN pin directly to LDO33.

INPUT CURRENT LIMITING: Input current limiting should be considered when using DC power supplies. This is discussed later in the Input Current Limiting section.

In Situ Battery Charging

The LT8490 can be used to charge a battery while the battery is powering a load. The load should be directly connected to the battery terminals as shown in Figure 6. The variable nature of some loads can make charging times unpredictable. Due to this unpredictability it is recommended that charging time limits be disabled (see Charger Configuration – CHARGECFG2 Pin section for more information).

Because a load connected to the battery may draw more power than provided by the charger, the battery may discharge while the LT8490 is charging the battery. If this case occurs and the battery voltage falls below 31% (typical) of the Stage 2 voltage limit, the undervoltage fault will become active and the charger will halt until the battery voltage rises above 35% (typical) of the Stage 2 voltage limit. Consider automatically disabling the load if the battery depletes below an unacceptably low voltage.

The arrow in Figure 6 shows the proper disconnect point if removing the battery from the charger in an in situ battery charging application. This disconnect point is specified because the LT8490 is not designed to provide power directly to a load without the presence of a battery.
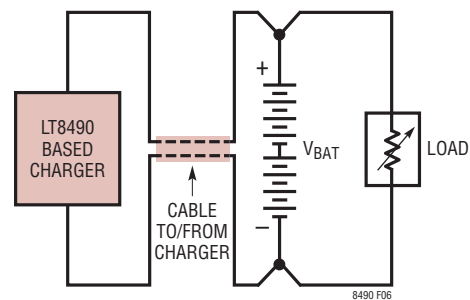

Figure 6. Load Connection to Battery in LT8490 Application

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LINEAR TECHNOLOGY

APPLICATIONS INFORMATION

Stage Voltage Limits

The Stage 2 voltage limit (V_{S2}) is the maximum battery charging voltage. The voltage limits for Stages 0, 1 and 3 are all related to the Stage 2 limit as shown in Table 3 and Figure 11. If temperature compensated charging is enabled, then V_{S2} will change with temperature as shown in Figure 13. As such, the limits for the other stages will also change with temperature since they are a constant proportion of V_{S2}.

Table 3. Typical Charging Stage Voltage Thresholds

STAGE TRANSITION	V_{BAT} RISING OR FALLING	TYPICAL V_{BAT}/V_{S2}	TYPICAL V_{BAT}/V_{S3}
V_{BAT} Undervoltage Fault → STAGE 0	Rising	35%	–
STAGE 0 → STAGE 1	Rising	70%	–
STAGE 1 → STAGE 2	Rising	98%	–
STAGE 3 → STAGE 0	Falling	–	96%
STAGE 2 → STAGE 1	Falling	95%	–
STAGE 1 → STAGE 0	Falling	66%	–
STAGE 0 → V_{BAT} Undervoltage Fault	Falling	31%	
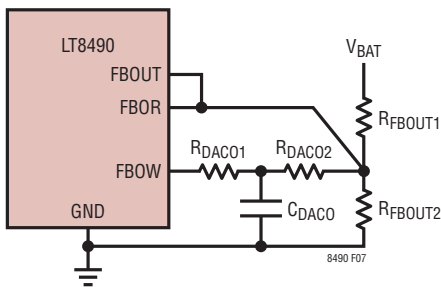
Figure 7. Output Feedback Resistor Network

SETTING THE STAGE 2 VOLTAGE LIMIT: The resistor network shown in Figure 7 is used to set the Stage 2 voltage limit. Battery manufacturers typically call for a higher Stage 2 voltage limit than the nominal battery voltage. For example, a 12V lead-acid battery used in automotive applications commonly has a Stage 2 charging voltage limit of 14.2V. If temperature compensated charging will be used (see Temperature Measurement, Compensation and Fault section) then use the 25°C value for V_{S2} in the equations below.

R_{FBOUT2} is often chosen between 4.99kΩ and 49.9kΩ. Choosing higher values for R_{FBOUT2} reduces the amount of current draw from the battery through the feedback network.

$$R_{FBOUT1} = R_{FBOUT2} \bullet \left[V_{S2} \bullet \left(\frac{1.241}{1.211} - 0.128 \right) - 1 \right] \Omega$$

$$R_{DACO2} = \frac{R_{FBOUT1} \bullet R_{FBOUT2} \bullet 0.833}{\left(R_{FBOUT2} \bullet V_{S2} \bullet \frac{1.241}{1.211} \right) - R_{FBOUT2} - R_{FBOUT1}} \Omega$$

$$R_{DACO1} = 0.2 \bullet R_{DACO2} \Omega$$

$$C_{DACO} = \frac{1}{500 \bullet R_{DACO1}} F$$

For greater charging voltage accuracy, it is recommended that 0.1% tolerance resistors be used for the output feedback resistor network.

Due to the granularity of standard resistor values, simply rounding the calculated results to their nearest standard values may result in unwanted errors. Consider using multiple resistors in series to match the calculated results. Otherwise, use standard resistor values and check the final results with the following equations.

$$V_{X3} = \left(\frac{R_{FBOUT1}}{R_{DACO1} + R_{DACO2}} \right) \bullet (X - 1.89)$$

where

$$X = 1.211 \bullet \left[1 + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT2}} \right) + \left(\frac{R_{DACO1} + R_{DACO2}}{R_{FBOUT1}} \right) \right]$$

V_{X3} indicates the actual 25°C V_{S2} voltage using the selected resistors.

$$N1 = \frac{X - 1.89}{X - 3.3}$$

N1 should be as close as possible to 1.22.

$$N2 = 1 - \frac{1.89}{X}$$

N2 should be as close as possible to 0.805. Iterations may be required to determine best standard resistor values.

APPLICATIONS INFORMATION

Table 4 shows good sets of standard value components for charging nominal battery voltages of 12V, 24V, 36V, 48V and 60V. Iterative calculations were required to select these values that achieve the best overall results.

Table 4. Standard Value Output Feedback Network vs Output Regulation Voltage

BATTERY VOLTAGE	TARGET V_{S2} (V)	R_{FBOUT1} (kΩ)	R_{FBOUT2} (kΩ)	R_{DACO1} (kΩ)	R_{DACO2} (kΩ)	C_{DACO} (nF)
12	14.2	274	23.2	26.1	124	82
24	28.4	487	20	28	107	68
36	42.6	787	21	22.6	121	100
48	56.8	1000	20	22.6	115	100
60	71.0	866	13.7	13.3	80.6	150

SETTING THE STAGE 3 VOLTAGE LIMIT: When enabled, Stage 3 charging maintains the battery voltage at 85% to 99% of V_{S2}. This proportion is adjustable and is discussed in the Charger Configuration – CHARGECFG1 Pin section.

BATTERY UNDERVOLTAGE LIMIT: Upon start-up, the LT8490 checks for battery voltage above 35% (typical) of the Stage 2 voltage limit. If the battery voltage is less than this, charging will not start and a battery undervoltage fault will be indicated on the FAULT pin. Charging will begin after the battery voltage rises above 35% (typical) of the Stage 2 voltage limit. If the battery voltage subsequently falls below 31% (typical), charging will again stop and the fault will be indicated on the FAULT and STATUS pins.

Charge Current Limiting

The maximum charging current is configured with the output current limiting circuit. The output current is sensed through R_{SENSE2} and converted to a proportional current flowing out of the IMON_OUT pin (see Figure 8).

IMON_OUT voltages above 1.208V (typical) cause V_C to reduce due to EA1, and thus limit the output current. IOW is either driven to ground or floated depending on charging conditions. This allows the current limit for Stage 0 ($I_{OUT(MAXS0)}$) to be set independently of the remaining Stages ($I_{OUT(MAX)}$) with proper selection of R_{IOW} and R_{IMON_OUT}. Use the following equations to configure the charging current limits:

$$R_{SENSE2} = \frac{0.0497}{I_{OUT(MAX)}}\,\Omega$$

$$R_{IMON\_OUT} = \frac{1208}{I_{OUT(MAXS0)} \bullet R_{SENSE2}}\,\Omega$$

$$R_{IOW} = \frac{24.3k \bullet R_{IMON\_OUT}}{R_{IMON\_OUT} - 24.3k}\,\Omega$$

$$R_{IOR} = 3.01k\Omega$$

$$C_{IMON\_OUT} = \text{read below}$$

where $I_{OUT(MAX)}$ is the maximum charging current in Amps, $I_{OUT(MAXS0)}$ is the maximum trickle charging current in Stage 0 and $I_{OUT(MAXS0)}$ is no greater than $I_{OUT(MAX)}$. For cases where $I_{OUT(MAX)} = I_{OUT(MAXS0)}$, it is OK to exclude R_{IOW} and float the I_{OW} pin. $I_{OUT(MAXS0)}$ must be at least 20% of $I_{OUT(MAX)}$.
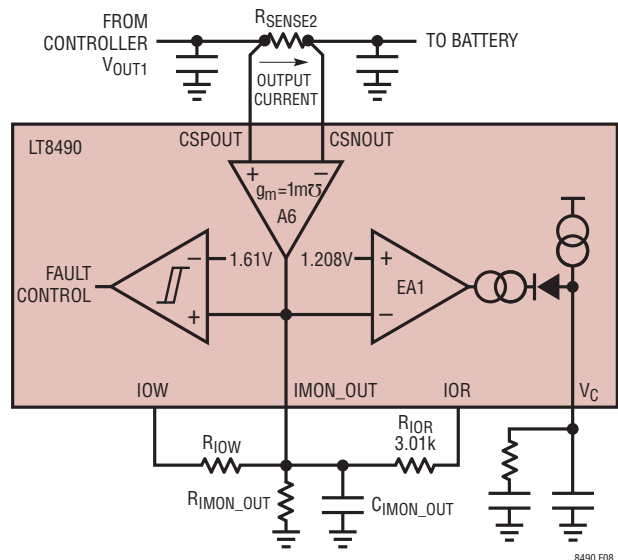

Figure 8. Output Current Regulation Loop

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C_{IMON_OUT} reduces IMON_OUT ripple and stabilizes the constant charging current control loop. Reducing C_{IMON_OUT} improves stability and minimizes inductor current overshoot that can occur if a discharged battery is quickly disconnected then reconnected to the charger. However, this is at the expense of increased IMON_OUT ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_OUT must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_OUT} capacitor in the range of 4.7nF to 22nF is adequate for most applications.

Input Current Limiting

SOLAR PANEL SUPPLY: Solar panels are inherently current limited and may not be able to provide maximum charging power at the lowest input voltages. The LT8490 uses its MPPT algorithm to sweep the panel voltage as low as 6V to find the maximum power point. Make sure that the input current limit is set higher than the maximum panel current capability, plus at least 20% to 30% margin, in order to achieve the maximum charging capability of the system.

In addition, note that the LT8490 uses the same circuit (shown in Figure 9) to measure the input current as to limit it. The input current is measured by an A/D conversion of the IIR pin voltage which is connected to IMON_IN and is proportional to input current. The digitized input current is used to locate the maximum power point of the solar panel. Setting a higher input current limit reduces the resolution of the digitized reading of the input current. Avoid setting the input current limit dramatically higher than necessary, as this may affect the accuracy of the maximum power point calculations.

DC POWER SUPPLY: When charging a battery at maximum current, and thus power, a low voltage supply must provide more current than a high voltage supply. This can be seen by equating output power to input power, less some efficiency loss.

$$V_{IN} \bullet I_{IN} \bullet \eta = V_{BAT} \bullet I_{BAT}$$

or

$$I_{IN(MAX)} = \frac{V_{BAT} \bullet I_{BAT(MAX)}}{V_{IN(MIN)} \bullet \eta}$$

where the efficiency factor η is typically between 0.95 and 0.99.

When powered by a DC supply, appropriate input current limiting is recommended for supplies that might (1) become overloaded as the supply ramps up or down through 6V or (2) provide more input current than the charger components can tolerate.

SETTING THE INPUT CURRENT LIMIT: The input current is sensed through R_{SENSE1} as shown in Figure 9. The current through R_{SENSE1} is converted to a voltage on the IMON_IN pin according to the following equation:

$$V_{IMON\_IN} = \left[\left(\frac{I_{IN} \bullet R_{SENSE1}}{1000} + 7\mu A \right) \bullet R_{IMON\_IN} \right] V$$

IMON_IN voltages exceeding 1.208V (typical) cause the V_C voltage to reduce, thus limiting the input current. R_{IMON_IN} should be 21kΩ ± 1% or better. Using this information, the appropriate value for R_{SENSE1} can be calculated using the following equation:

$$R_{SENSE1} = \frac{1000 \bullet \left(\frac{1.208V}{21k\Omega} - 7\mu A \right)}{I_{IN(MAX)}} = \frac{0.0505}{I_{IN(MAX)}} \Omega$$

where $I_{IN(MAX)}$ is the maximum input current limit in Amps. R_{SENSE1} values greater than 25mΩ are not recommended.

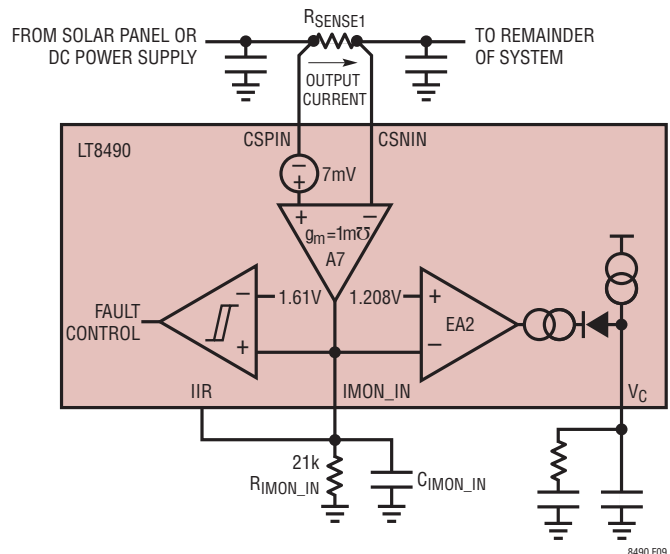**Figure 9. Input Current Regulation Loop**

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C_{IMON_IN} reduces IMON_IN ripple and stabilizes the input current limit control loop. Reducing C_{IMON_IN} improves stability and minimizes possible inductor current overshoot. However, this is at the expense of increased IMON_IN ripple that can introduce more noise into the ADC measurements. The higher frequency pole created at IMON_IN must be adequately separated from the lower frequency pole at the V_C pin for proper stability. A C_{IMON_IN} capacitor of 4.7nF to 22nF is adequate for most applications.

Input and Output Current Sense Filtering

The C_{SX} and R_{SX} current sense filtering shown in Figure 10 can improve the accuracy of the input and output current measurements at low average current levels. Amplifiers A7 and A8 (Figures 8 and 9) can only amplify positive R_{SENSE} voltages. Although the average R_{SENSE} voltage is always positive, the voltage ripple at low average current levels may contain negative components that are averaged out by the filter. Recommended values for R_{S1}, R_{S2} and C_{S1}, C_{S2} are 10Ω and 470nF.

C_{C1} and C_{C2} may be required, depending on board layout, to reduce common mode noise that may reach the LT8490 pins. 100nF ceramic capacitors, with the appropriate voltage ratings, work well in most cases. Be sure to place all of the filter components (C_{SX}, R_{SX}, C_{CX}) close to the LT8490 for best performance.

Finally, note that a small voltage drop (typically ~0.25mV per 10Ω) will occur across R_{S1} and R_{S2} due to the input bias currents of CSNOUT and CSNIN. This represents a ~0.5% reduction in the maximum current limit which typically occurs with ~50mV across R_{SENSE}. The C/10 threshold (typically when 5mV is measured across CSPOUT and CSNOUT) will also reduce to C/10.5 due to the 0.25mV drop across R_{S2}.
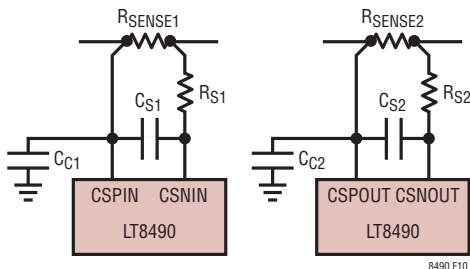

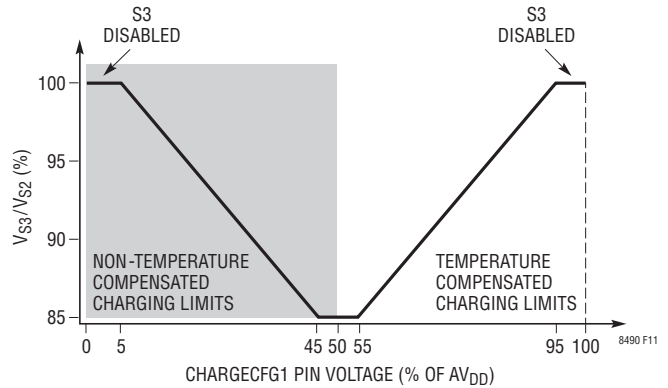**Figure 10. Recommended Current Sense Filter**

Figure 11. CHARGECFG1 Pin Configuration

Charger Configuration – CHARGECFG1 Pin

The CHARGECFG1 pin is a multifunctional pin as shown in Figure 11. Set this pin using a resistor divider totaling no less than 100kΩ to the AV_{DD} pin (see the Typical Applications section for examples). The voltage on CHARGECFG1, as a percentage of AV_{DD}, makes the selections discussed below. Avoid setting the divider ratio directly at any of the inflection points on Figure 11 (e.g. 5%, 45%, 50%, 55% or 95%)

ENABLE/DISABLE TEMPERATURE COMPENSATED VOLTAGE LIMITS: Setting the CHARGECFG1 pin in the upper half of the voltage range (> 50%) enables battery voltage temperature compensation, while using the bottom half (< 50%) disables the temperature compensation, even if a thermistor is coupled to the battery pack. The next section provides more detailed information.

DISABLE STAGE 3: Setting the CHARGECFG1 pin to AV_{DD} or 0V disables Stage 3. When the CHARGECFG1 pin is set in this manner, the charging algorithm will never proceed to Stage 3. Stage 3 is commonly used for lead-acid battery charging but is not typically used for lithium-ion battery charging.

ENABLE STAGE 3: Setting the CHARGECFG1 pin between 5% to 95% of AV_{DD} enables Stage 3 charging and sets the Stage 3 voltage limit (V_{S3}) as a percentage of the Stage 2 voltage limit (V_{S2}) according to the following formulas.

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When temperature compensated charging and Stage 3 are enabled, use:

$$CHARGECFG1\% = \left[\left(2.67 \cdot \left(\frac{V_{S3}}{V_{S2}} - 0.85\right)\right) + 0.55\right] \cdot 100\%$$

When temperature compensated charging is disabled and Stage 3 is enabled, use:

$$CHARGECFG1\% = \left[2.72 - \left(2.67 \cdot \left(\frac{V_{S3}}{V_{S2}}\right)\right)\right] \cdot 100\%$$

where V_{S3}/V_{S2} should be between 0.86 to 0.99.

For example, to enable temperature compensated charging with V_{S3} set to 93% of V_{S2}, choose a divider that puts CHARGECFG1 at 76% of AV_{DD}. For best accuracy use resistors that have a 1% tolerance or better.

Temperature Measurement, Compensation and Fault

The LT8490 can measure the battery temperature using an NTC (negative temperature coefficient) thermistor thermally coupled to the battery pack. The temperature monitoring function is enabled by connecting a 10kΩ, ß = 3380 NTC thermistor from the TEMPSENSE pin to ground and an 11.5kΩ (1% tolerance or better) resistor from AV_{DD} to TEMPSENSE (as shown in Figure 12). If battery temperature monitoring is not required, then use a 10kΩ resistor in place of the thermistor. This will indicate to the LT8490 that the battery is always at 25°C.
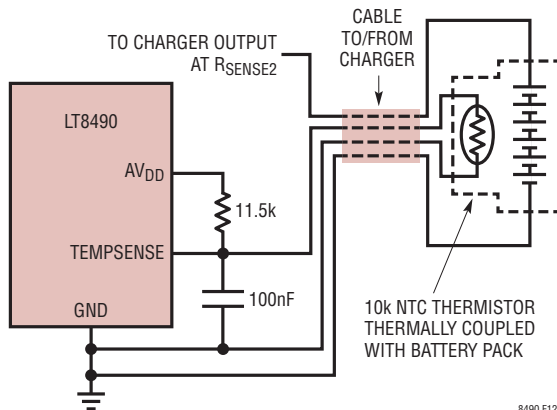
The LT8490 monitors the voltage on the TEMPSENSE pin to determine the battery temperature and also to detect if the thermistor is connected or not. A TEMPSENSE voltage greater than 96% of AV_{DD} (typical) indicates that the thermistor has been disconnected. Three charger functions rely on the TEMPSENSE information.

1. INVALID BATTERY TEMPERATURE FAULT: A temperature fault occurs when the battery temperature is outside of the valid range as configured on the CHARGECFG2 pin (−20°C to 50°C or 0°C to 50°C). The temperature fault condition remains until the temperature returns within −15°C to 45°C or 5°C to 45°C (5°C of hysteresis). During a temperature fault, charging is halted and the STATUS and FAULT pins follow the pattern described in Table 6. If timer termination is enabled with the CHARGECFG2 pin, the timer count is paused during the temperature fault and resumes when the fault state is exited.

2. BATTERY VOLTAGE TEMPERATURE COMPENSATION: Some battery chemistries charge best when the voltage limit is adjusted with battery temperature. Lead-acid batteries, in particular, experience a significant change in the ideal charging voltage as temperature changes. If enabled with the CHARGECFG1 pin, the battery charging voltage and all related voltage thresholds are automatically adjusted with battery temperature. As the voltage on the TEMPSENSE pin changes, the PWM duty cycle from the FBOW pin changes such that the voltage limits of the LT8490 follow the curve shown in Figure 13.
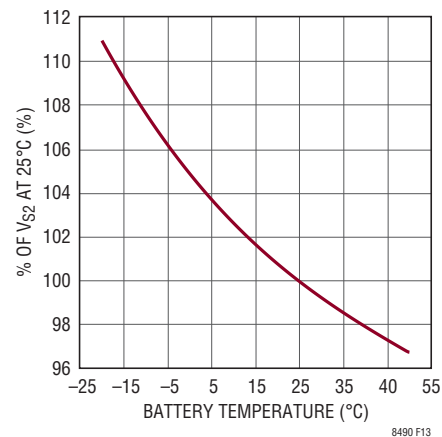

Figure 12. Battery Temperature Sensing Circuit

Figure 13. Stage 2 Voltage Limit vs Temperature When Temperature Compensation Is Enabled

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3. BATTERY DISCONNECT SENSING: The LT8490 detects if the battery and thermistor have been disconnected from the charger by monitoring the TEMPSENSE pin voltage. When the connection to the battery is severed, as shown by the arrow in Figure 12, the connection to the thermistor is also severed and the TEMPSENSE voltage rises up to AV_{DD} through the 11.5kΩ resistor. During the time when the battery is not present, the LT8490 halts charging. The charger automatically restarts the charging at Stage 0 when a battery (along with integrated thermistor or resistor) is sensed through the TEMPSENSE pin.

Charger Configuration – CHARGECFG2 Pin

The CHARGECFG2 pin is a multifunctional pin as shown in Figure 14. Set this pin using a resistor divider totaling no less than 100kΩ to the AV_{DD} pin (see the Typical Applications section for examples). The voltage on CHARGECFG2, as a percentage of AV_{DD}, makes the selections discussed below. Avoid setting the divider ratio directly at any of the inflection points on Figure 14 (e.g. 5%, 10%, 45%, 50%, 55%, 90% or 95%)
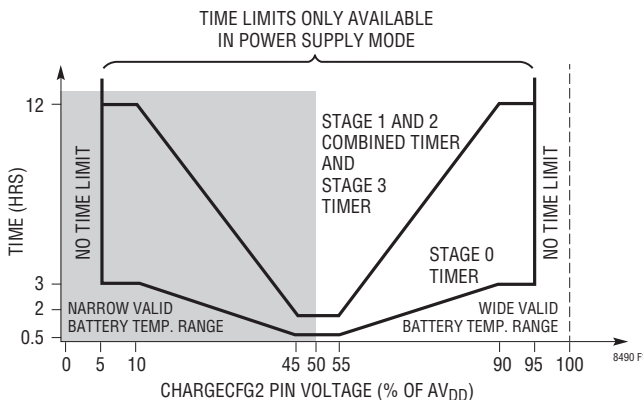

Figure 14. CHARGECFG2 Pin Voltage Settings

ENABLE/DISABLE CHARGING TIME LIMITS: The LT8490 supports charging time limits only when power supply mode is enabled (see the DC Supply Powered Charging section). When power supply mode is disabled, any finite time limit setting on CHARGECFG2 is interpreted as no time limit. This section discusses how to configure the time limits using the CHARGECFG2 pin. For more information about the operation of the time limits see the Charging Time Limits section.

Setting the CHARGECFG2 pin between 5% to 95% of AV_{DD} allows for time limit settings between 0.5 hours to 3 hours for Stage 0, 2 hours to 12 hours for Stage 1 and 2 combined and 2 hours to 12 hours for Stage 3. The Stage 0 time limit is always 1/4th of the Stage 1 + Stage 2 time limit and the Stage 3 time limit is always the same length as the Stage 1 + Stage 2 limit. When choosing a Stage 1 + Stage 2 time limit of 12 hours, choose a divider ratio very close to 7.5% or 92.5%. When choosing a Stage 1 + Stage 2 time limit of 2 hours, choose a divider ratio very close to 47.5% or 52.5%. For time limits in between, use one of the following formulas.

When the wide valid battery temperature range (–20°C to 50°C) is desired use:

$$CHARGECFG2\% = 3.5\% \cdot (T_{S1S2} - 2) + 55\%$$

where T_{S1S2} is the desired Stage 1 + Stage 2 time limit in hours between 2.1 and 11.9.

When the narrow valid battery temperature range (0°C to 50°C) is desired use:

$$CHARGECFG2\% = 45\% - 3.5\% \cdot (T_{S1S2} - 2)$$

where T_{S1S2} is the desired Stage 1 + Stage 2 time limit in hours between 2.1 and 11.9.

Setting CHARGECFG2 below 4% (i.e., ground) or above 96% of AV_{DD} (i.e., tie to AV_{DD}) disables the time limits, allowing the charging to run indefinitely in lieu of any fault conditions.

SELECT THE VALID BATTERY TEMPERATURE RANGE: Setting the CHARGECFG2 pin in the top half of the voltage range (> 50%) selects a wider valid battery temperature range (–20°C to 50°C), while using the bottom half of the voltage range (< 50%) selects a narrower valid battery temperature range (0°C to 50°C). Generally, lead-acid batteries would use the wide range, while lithium-ion batteries would use the narrow range. See the Temperature Measurement, Compensation and Fault section for more information about the invalid battery temperature fault.

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Charging Time Limits

Charging time limits can be enabled only in power supply mode by properly configuring the CHARGECFG2 pin (see the Charger Configuration – CHARGECFG2 Pin section). Charging time limits are not recommended for use when a load is present on the battery due to the unpredictable amount of time that may be required to achieve full charge.

When enabled, the appropriate timers start at the beginning of Stages 0, 1 and 3. If the timer expires while operating in its respective stage or the LT8490 returns to a charging stage after its respective timer has expired, charging stops immediately. As shown in Table 5, expiration of a timer is treated as either a fault or as done charging depending on the timer that expired and the configuration of the charger. In any case, when charging stops, the fault or done charging status is indicated on the STATUS and FAULT pins as described in the STATUS and FAULT Indicators section.

Table 5. Charger Conditions and Timer Expiration Results

CHARGING STAGE WHEN TIMER EXPIRES	STAGE 3 ENABLED?	TIMER USED	RESULT OF TIMER EXPIRATION
0	–	Stage 0	Fault
1	–	Stage 1 + Stage 2	Fault
2	–	Stage 1 + Stage 2	Fault
3	Yes	Stage 3	Done Charging

STAGE 2 TERMINATION (TIME LIMITS ENABLED): Timer expiration in Stage 2 causes a fault and charging stops immediately with a fault indication on the STATUS and FAULT pins. If the Stage 2 output current drops below C/10 before the timer expires and Stage 3 is disabled then charging stops and done charging is indicated on the STATUS pin.

STAGE 2 TERMINATION (TIME LIMITS DISABLED): If time limits are disabled, Stage 2 can only terminate if Stage 3 is also enabled. After charging current falls below C/10, charging will proceed to Stage 3. If Stage 3 is also disabled then the charger will operate in Stage 2 indefinitely unless the battery voltage falls enough for charging to revert back to Stage 1. During the indefinite Stage 2 charging, the STATUS pin will indicate if Stage 2 current is below C/10 or above C/5 (as shown in Tables 6 and 7).

STAGE 3 TERMINATION CONDITIONS: If Stage 3 is enabled and time limits are disabled, the LT8490 will remain in Stage 3 forcing reduced constant-voltage indefinitely unless the battery voltage falls below 96% of V_{S3} or charging current rises above C/5 causing the charger to revert back to Stage 0. If Stage 3 is enabled and time limits are enabled, timer expiration in Stage 3 will stop charging and communicate the done charging state through the STATUS pin (as shown in Tables 6 and 7).

Lithium-Ion Battery Charging

The LT8490 is well suited to charge lithium-ion batteries. Connecting the CHARGECFG1 and CHARGECFG2 pins to ground puts the LT8490 into a typical configuration for lithium-ion battery charging (0°C to 50°C valid battery temperature, Stage 3 disabled, no temperature compensation, no time limits). Figure 15 shows a typical lithium-ion charging cycle in this configuration.

If no timer termination has been selected, the LT8490 will charge the lithium-ion battery stack to the desired Stage 2 voltage limit, maintaining that limit indefinitely. When the charging current is < C/10, the STATUS pin will go high as described in Table 6.

NOTE: When solar charging a Li-Ion battery without time limits it is recommended that the Stage 2 voltage limit not exceed 95% of the lithium-ion maximum cell voltage. Since this configuration can charge indefinitely, following this guideline keeps the lifetime of the batteries from degrading quickly.
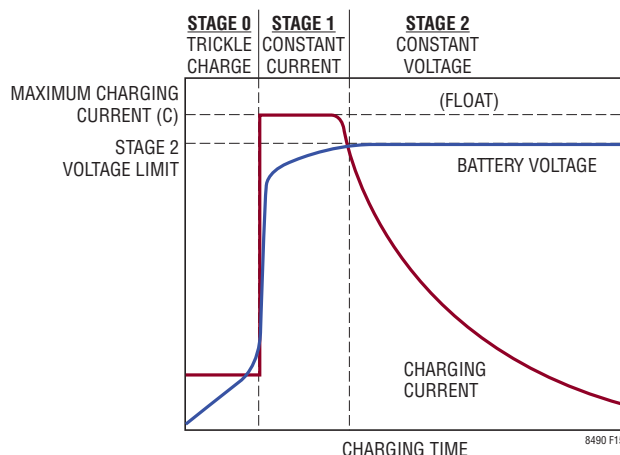
Figure 15. Lithium-Ion Battery Charging Cycle

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Lead-Acid Battery Charging

The LT8490 can be used to charge lead-acid batteries. Setting the CHARGECFG1 pin to 87.6% of AV_{DD} and CHARGECFG2 pin equal to AV_{DD} configures the LT8490 for typical lead-acid battery charging (–20°C to 50°C valid battery temperature, Stage 3 enabled with $V_{S3}/V_{S2} = 97.2\%$, temperature compensated voltage limits, no time limits). Figure 16 shows a typical lead-acid charging cycle.

If time limits have been disabled, the LT8490 will charge the lead-acid battery stack to the desired Stage 3 voltage limit and restart the charging cycle if 1) the battery voltage falls below 96% of the Stage 3 voltage limit (V_{S3}) or 2) the charging current rises above C/5.
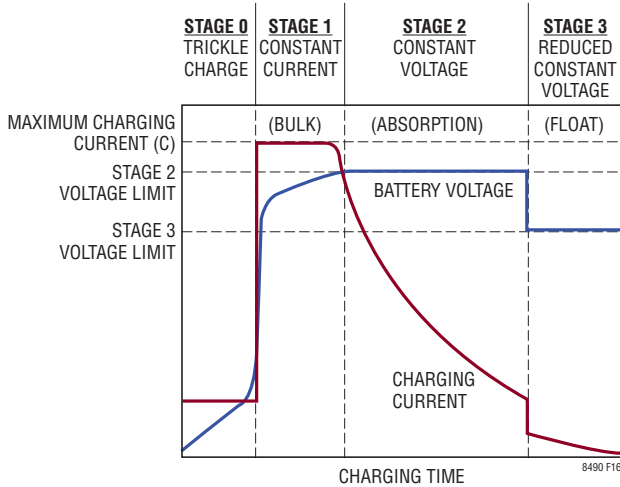
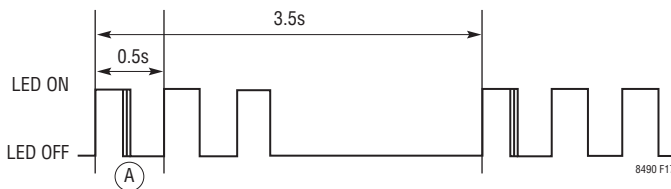

Figure 16. Lead-Acid Battery Charging Cycle

Figure 17. Example Waveform for STATUS Pin in STAGE 3

STATUS and FAULT Indicators

The LT8490 reports charger status through two outputs, the STATUS and FAULT pins. These pins can be used to drive LEDs for user feedback. In addition, the STATUS pin doubles as a UART output to send status information to a peripheral device. Table 6 describes the LED behavior of these pins in relationship to the charger status.

While the LT8490 is operating, the STATUS pin toggles on a 3.5 sec (typical) interval as shown in Figure 17. The three pulses shown in Figure 17 represent the charger operating in Stage 3. The STATUS and FAULT pins pull up to turn the LEDs on and drive to ground to turn the LEDs off.

Table 6. STATUS and FAULT LED INDICATORS

CHARGER STATUS	LED PULSES/3.5s, APPROXIMATE ON-TIME PER PULSE		FOR MORE INFORMATION SEE SECTION
	STATUS	FAULT	
Stage 0	1, 10ms	OFF	Battery Charging Algorithm
Stage 1	1, 250ms	OFF	Battery Charging Algorithm
Stage 2 and (Stage 3 Enabled or Time Limits Enabled or I_{OUT} Rising Above C/5)	2, 250ms	OFF	Battery Charging Algorithm and Charger Configuration Sections
Stage 2 and Stage 3 Disabled and Time Limits Disabled and I_{OUT} Falling Below C/10	ON	OFF	Battery Charging Algorithm and Charger Configuration Sections
Stage 3	3, 250ms	OFF	Battery Charging Algorithm
Done Charging	ON	OFF	Charging Time Limits
Battery Present Detection Fault	1, 10ms	1, 250ms	Temperature Measurement, Compensation and Fault
Invalid Battery Temperature Fault	1, 10ms	2, 250ms	Temperature Measurement, Compensation and Fault
Timer Expiration Fault	1, 10ms	3, 250ms	Charging Time Limits
Battery Undervoltage Fault	1, 10ms	4, 250ms	Stage Voltage Limits

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Driving LEDs with the STATUS and FAULT Pins

The STATUS and FAULT pins on the LT8490 can be used to drive LED indicators. Figure 18 shows the simplest configuration for driving LEDs from these two pins.

The STATUS pin can drive up to 2.5mA into an LED. Choose R_{DSA} to limit the LED current to 2.5mA or less when STATUS is driven close to 3.3V. Choose R_{DSB} to conduct a current equivalent to the LED current when STATUS is driven close to ground and R_{DSB} has ~3.3V across the terminals. D_S, in Figure 18, conducts ~2.5mA when STATUS is driven high. R_{DSB} conducts ~2.5mA when the STATUS is driven low.

The FAULT pin has a weak pull up in comparison to the STATUS pin (see the Typical Performance Characteristics section). The LED current is typically self-limited to less than 1mA by the FAULT pin driver. R_{DFB} in Figure 18 is typically 3.32kΩ and increases the FAULT LED current. When configured as shown in Figure 18, the D_F LED current should be limited to less than 1.5mA.

For driving higher current LEDs, the circuit in Figure 19 can be used. Note that the LED current for D_F is provided by the INTV$_{CC}$ regulator in this case. Excessive LED current can overload the INTV$_{CC}$ regulator and/or cause excessive heating in the LT8490. 7.5mA is a good starting point when using this circuit. Higher currents can be possible

with careful board evaluation. Transistor Q2 must have a collector-emitter breakdown voltage greater than INTV$_{CC}$. The MMBT3646 has a breakdown voltage of 15V and is well suited for this application.

The LED current for D_S is provided by V_{IN} in this case. Do not draw current for D_S from INTV$_{CC}$ since this increases power dissipation in the LT8490. Transistor Q1 must have a collector-emitter breakdown greater than V_{IN}. The MMBT5550L has a breakdown voltage of 140V and is suitable for most applications.
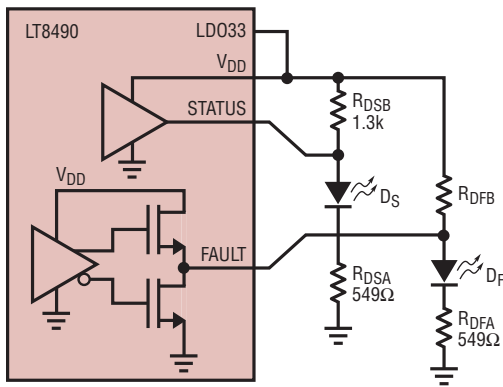
To properly set the resistors shown in Figure 19, use the following equations:

$$R_{E1} \cong \frac{2.6}{I_D}\Omega$$

$$R_{C1} \cong \left(\frac{I_{NTVCC} - V_F}{I_D}\right)\Omega$$

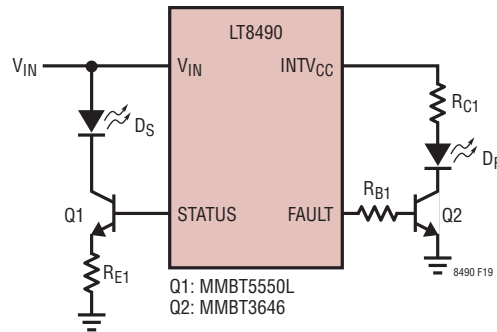$$R_{B1} = \frac{50}{I_D}\Omega$$

where INTV$_{CC}$ is typically 6.35V, V_F is the forward voltage of the LED (often about 1.7V) and I_D is the desired bias current through the LED.

D_S: OSRAM, LGL29KF2J124Z
D_F: OSRAM, LGL29K-H1J2-1-Z

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Figure 18. Default STATUS/FAULT LED Indicators

Q1: MMBT5550L
Q2: MMBT3646

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Figure 19. Higher Current Drive for STATUS/FAULT LEDs