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# 42V, Low $I_Q$ , Quad Output Triple Monolithic Buck Converter and Boost Controller

## FEATURES

- Flexible Power Supply System Capable of Four Regulated Outputs with  $V_{BATT} \ll V_{OUT}$
- Two High Voltage Synchronous Buck Regulators
  - 3V to 42V Input Voltage Range
  - Output Currents Up to 2.5A and 1.5A
- One Low Voltage Synchronous Buck Regulator
  - 2.6V to 5.5V Input Voltage Range
  - Output Currents Up to 1.8A
- One Boost Controller Allows Buck Converters to Regulate with  $V_{BATT} \ll V_{OUT}$
- Selectable Burst Mode® Operation Allows Low  $28\mu A I_Q$  with High Voltage Channels Active
- Programmable Power-On Reset
- Individual Channel Power Good Indicators
- Step-Down Switching Frequency: 250kHz to 2.2MHz
- Available in 40-Lead QFN (6mm × 6mm) Package

## APPLICATIONS

- Automotive Stop-Start and Cold Crank Ride Through
- Last-Gasp CPU Power Hold-Up
- Industrial Controls and Power Supplies

## DESCRIPTION

The **LT®8603** is a highly flexible, quad output regulator combining two high input voltage capable monolithic step-down switching regulators, one low input voltage capable monolithic step-down regulator, and a boost controller to satisfy a wide range of applications while occupying minimal board space.

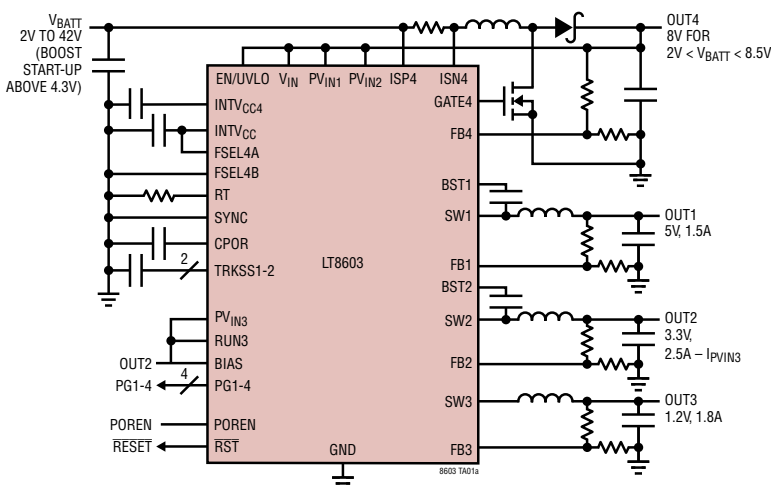
With the boost controller configured to supply the chip  $V_{IN}$  supply, the LT8603 produces three precisely regulated outputs even when the boost input voltage falls significantly below the regulated output voltages, such as during an automotive cold crank scenario. Alternatively, with the boost controller driven from one of the step-down regulator outputs or configured as a SEPIC, the LT8603 provides four precisely regulated outputs over a wide input voltage range.

The LT8603 provides robust regulation by including a cycle-by-cycle current limit for all step-down regulators, thermal shutdown, and a boost controller that can tolerate reverse battery connections and negative transient input voltages down to  $-42V$ .

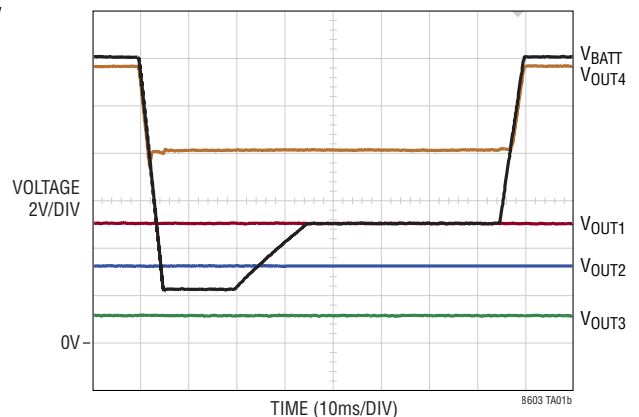
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## TYPICAL APPLICATION

Cold Crank Tolerant Automotive Triple Output Supply



LT8603 Response to a Cold Crank Automotive Input Waveform



# LT8603

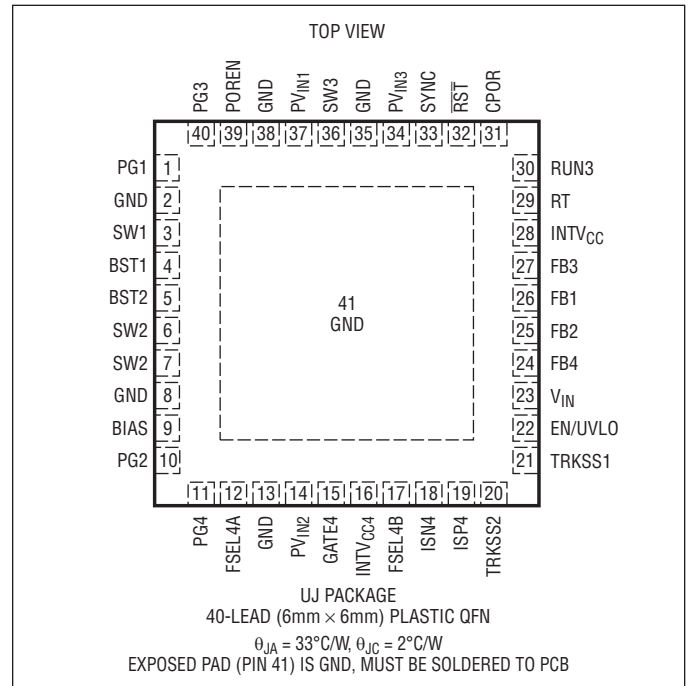
## ABSOLUTE MAXIMUM RATINGS

(Note 1)

### Supply Voltages

$V_{IN}$ , $PV_{IN1,2}$ .....	-0.3V to 42V
$PV_{IN3}$ .....	-0.3V to 6V
EN/UVLO .....	42V
ISP4, ISN4 .....	-42V to 42V
TRKSS1-2, RUN3, FB4, PG1-4, SYNC .....	6V
FSEL4A, FSEL4B, RST .....	6V
FB1-3, CPOR, POREN .....	3.6V
BIAS .....	-0.3V to 15V
Operating Junction Temperature (Notes 2, 5)	
LT8603E .....	-40°C to 125°C
LT8603I .....	-40°C to 125°C
Storage Temperature Range .....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LT8603#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8603EUJ#PBF	LT8603EUJ#TRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	-40°C to 125°C
LT8603IUJ#PBF	LT8603IUJ#TRPBF	LT8603UJ	40-Lead (6mm × 6mm) Plastic QFN	-40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ , EN/UVLO = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Bias and Internal Regulators</b>						
Minimum Operating $V_{IN}$ for Channels 1, 2 and 3		●		2.7	3.0	V
Minimum $V_{IN}$ to Start for Channels 1, 2 and 3		●		3.1	3.3	V
Minimum Operating $V_{IN}$ for Channel 4		●		3.0	3.2	V
Minimum $V_{IN}$ to Start for Channel 4		●		4.0	4.15	V
$V_{IN}$ Quiescent Current, Shutdown	$V_{BIAS} = 0\text{V}$ , EN/UVLO = 0.4V			0.1	1	$\mu\text{A}$
Total Operating Current $V_{BATT}$	$V_{BATT} = 12\text{V}$ , Channels 1 and 2 Active, No-Load (Note 4)			28		$\mu\text{A}$
	$V_{BATT} = 12\text{V}$ , All Channels Active, No-Load (Note 4)			50		$\mu\text{A}$
EN/UVLO Threshold	EN/UVLO Rising	●	1.15	1.2	1.25	V
	EN/UVLO Falling	●	1.1	1.15	1.2	V
EN/UVLO Input Current	EN/UVLO = 1.2V		-50		50	nA
INTV <sub>CC4</sub> Regulated Voltage	$V_{BIAS} = 0\text{V}$	●	4.4	4.6	4.8	V
	$V_{BIAS} = 6\text{V}$	●	4.7	5	5.2	V
INTV <sub>CC4</sub> Regulator Load Regulation	INTV <sub>CC4</sub> at 1mA – INTV <sub>CC4</sub> at 40mA			70		mV
<b>Oscillator</b>						
Switching Frequency	$R_T = 28.7\text{k}\Omega$	●	1.8	2	2.2	MHz
	$R_T = 243\text{k}\Omega$	●	0.224	0.25	0.284	MHz
SYNC Input Frequency Range		●	0.25		2.2	MHz
SYNC Input Voltage Low		●			0.3	V
SYNC Input Voltage High		●	1.2			V
SYNC Input Current			-100		100	nA
FSEL4A, FSEL4B Input Voltage Low		●			0.4	V
FSEL4A, FSEL4B Input Voltage High		●	2			V
FSEL4A, FSEL4B Input Current		●	-100		100	nA
<b>Channel 1</b>						
Feedback Voltage FB1		●	0.985	1	1.015	V
Input Current FB1		●	-100		100	nA
FB1 Line Regulation	$V_{IN} = 3\text{V}$ to 42V			0.002	0.01	%/V
SW1 Peak Current Limit (Note 3)			2.0	2.7	3.7	A
SW1 Leakage Current				0.1	1	$\mu\text{A}$
SW1 Top On-Resistance	$I_{SW1} = 1\text{A}$			240		m $\Omega$
SW1 Bottom On-Resistance	$I_{SW1} = 1\text{A}$			170		m $\Omega$
Lower FB1 Power Good Threshold	Percentage of $V_{FB1}$ , $V_{FB1}$ Falling	●	89	92	95	%
Upper FB1 Power Good Threshold	Percentage of $V_{FB1}$ , $V_{FB1}$ Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.8		%
PG1 Output Voltage Low	$I_{PG1} = 350\mu\text{A}$	●		0.13	0.3	V
PG1 Leakage Current	PG1 = 5V, FB1 = 1V	●			6	$\mu\text{A}$
TRKSS1 Pull-Up Current	TRKSS1 = 0.2V		1.5	2.4	3.1	$\mu\text{A}$

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ ,  $EN/UVLO = 3\text{V}$  unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Channel 2</b>						
Feedback Voltage FB2		●	0.985	1	1.015	V
Input Current FB2		●	-100		100	nA
FB2 Line Regulation	$V_{IN} = 3\text{V to } 42\text{V}$			0.002	0.01	%/V
SW2 Peak Current Limit (Note 3)			3.2	4.0	5.3	A
SW2 Leakage Current				0.1	1	$\mu\text{A}$
SW2 Top On-Resistance	$I_{SW2} = 1\text{A}$			150		$\text{m}\Omega$
SW2 Bottom On-Resistance	$I_{SW2} = 1\text{A}$			100		$\text{m}\Omega$
Lower FB2 Power Good Threshold	Percentage of $V_{FB2}$ , $V_{FB2}$ Falling	●	89	92	95	%
Upper FB2 Power Good Threshold	Percentage of $V_{FB2}$ , $V_{FB2}$ Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.8		%
PG2 Output Voltage Low	$I_{PG2} = 350\mu\text{A}$	●		0.13	0.3	V
PG2 Leakage Current	$PG2 = 5\text{V}$ , $FB2 = 1\text{V}$	●			6	$\mu\text{A}$
TRKSS2 Pull-Up Current	$TRKSS2 = 0.2\text{V}$		1.5	2.4	3.1	$\mu\text{A}$
<b>Channel 3</b>						
$PV_{IN3}$ Operating Voltage	$PV_{IN3}$ Falling	●	2.6		5.5	V
$PV_{IN3}$ Undervoltage Lockout	$PV_{IN3}$ Falling	●		2.35	2.6	V
Feedback Voltage FB3		●	788	800	812	mV
FB3 Line Regulation	$V_{IN} = 3\text{V to } 42\text{V}$			0.002	0.01	%/V
Input Current FB3		●	-100		100	nA
SW3 Leakage Current				0.1	1	$\mu\text{A}$
SW3 Peak Current Limit (Note 3)			2.6	3.2	3.8	A
SW3 PMOS On-Resistance	$I_{SW3} = 1\text{A}$			150		$\text{m}\Omega$
SW3 NMOS On-Resistance	$I_{SW3} = 1\text{A}$			100		$\text{m}\Omega$
Lower FB3 Power Good Threshold	Percentage of $V_{FB3}$ , $V_{FB3}$ Falling	●	89	92	95	%
Upper FB3 Power Good Threshold	Percentage of $V_{FB3}$ , $V_{FB3}$ Rising	●	104	107	110	%
Power Good Threshold Hysteresis				0.2		%
PG3 Output Voltage Low	$I_{PG3} = 350\mu\text{A}$	●		0.13	0.3	V
PG3 Leakage Current	$PG3 = 5\text{V}$ , $FB3 = 0.8\text{V}$	●			6	$\mu\text{A}$
RUN3 Threshold Voltage		●	1.15	1.20	1.25	V
RUN3 Input Current			-100		100	nA
Soft-Start Time			0.7	1	1.3	ms

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{IN} = 12\text{V}$ ,  $EN/UVLO = 3\text{V}$  unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Channel 4</b>						
Feedback Voltage FB4		●	788	800	812	mV
FB4 Line Regulation	$V_{IN} = 3.2\text{V to } 42\text{V}$			0.002	0.01	%/V
Input Current FB4		●	-100		100	nA
Soft-Start Time				1		ms
Current Comparator Limit Threshold	$V_{ISP4} \text{ to } V_{ISN4}, V_{CM} = 2\text{V to } 42\text{V}$	●	43	50	57	mV
Current Comparator Input Common Mode Range			2		42	V
ISP4, ISN4 Input Currents, Sleep	$V_{ISP4} = V_{ISN4} = 2\text{V to } 42\text{V}, \text{FB4} = 1\text{V}, \text{SYNC} = 0\text{V}$				200	nA
ISP4, ISN4 Input Currents, Active	$V_{ISP4} = V_{ISN4} = 2\text{V to } 42\text{V}, \text{FB4} = 0\text{V}, \text{SYNC} = 0\text{V}$			34	44	$\mu\text{A}$
ISP4, ISN4 Input Currents	$V_{ISP4} = V_{ISN4} = -42\text{V}$			7	10	mA
GATE4 High Side PMOS On-Resistance				2.5		$\Omega$
GATE4 Low Side NMOS On-Resistance				1.25		$\Omega$
FB4 Power Good Threshold	Percentage of $V_{FB4}$ , $V_{FB4}$ Falling	●	89	92	95	%
Power Good Threshold Hysteresis				0.2		%
PG4 Output Voltage Low	$I_{PG4} = 350\mu\text{A}$	●		0.13	0.3	V
PG4 Leakage Current	$PG4 = 5\text{V}, \text{FB4} = 0.8\text{V}$	●			6	$\mu\text{A}$
<b>Power-On Reset</b>						
POR Delay Time	$CPOR = 1000\text{pF}$	●	31	35.2	39.4	ms
RST Output Voltage Low	$I_{RST} = 100\mu\text{A}$	●		0.1	0.2	V
RST Pull-Up Current	POR Timed Out, $RST = 0\text{V}$			20		$\mu\text{A}$
RST Leakage Current	POR Timed Out, $RST = 6\text{V}$		-100		100	nA
POREN Threshold		●	1.15	1.2	1.25	V
POREN Pull-Up Current	$POREN = 0\text{V}$		0.6	1.0	1.4	$\mu\text{A}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** The LT8603E is guaranteed to meet performance specifications from  $0^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. Specifications over the  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8603I is guaranteed to meet performance specifications from  $-40^\circ\text{C}$  to  $125^\circ\text{C}$  junction temperature. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures above  $125^\circ\text{C}$ .

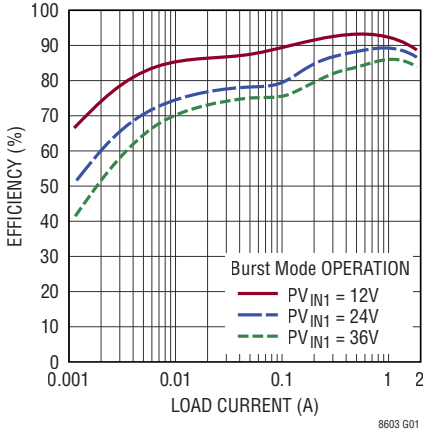
**Note 3:** Current limit is assured by design and/or correlation to static test. Slope compensation reduces current limit at higher duty cycles.

**Note 4:** Measurement made using the circuit titled, "Details of Front Page Application" in the Typical Applications section.

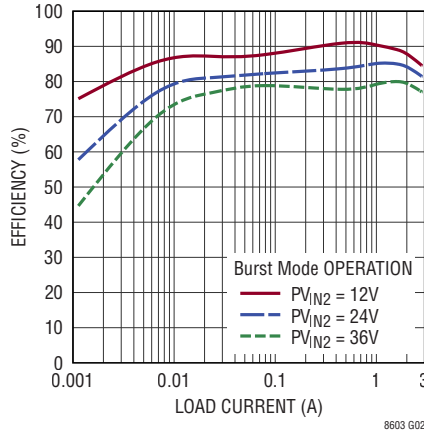
**Note 5:** This IC includes overtemperature protection that is intended to protect the device during overload conditions. Junction temperature will exceed  $150^\circ\text{C}$  when overtemperature protection is active. Continuous operation above the specified maximum junction temperature will reduce lifetime.

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = PV_{IN1} = PV_{IN2} = 12\text{V}$ ,  $EN/UVLO = 3\text{V}$  and  $PV_{IN3} = 3.3\text{V}$  unless otherwise noted.

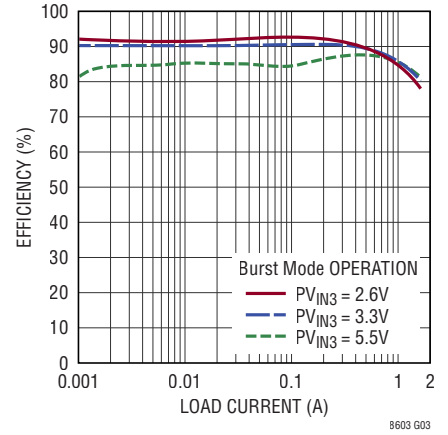
**Channel 1 Efficiency vs Load**  
 $V_{OUT1} = 5\text{V}$ ,  $f_{SW} = 1\text{MHz}$



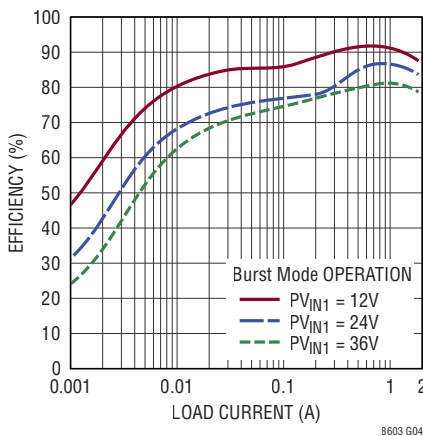
**Channel 2 Efficiency vs Load**  
 $V_{OUT2} = 3.3\text{V}$ ,  $f_{SW} = 1\text{MHz}$



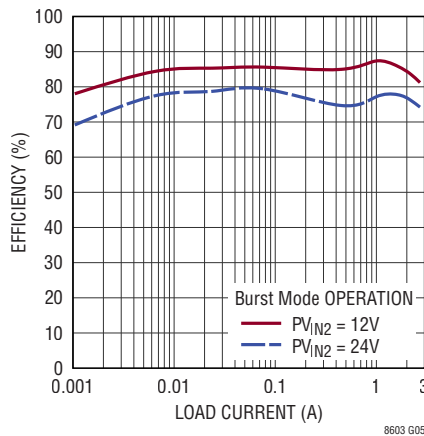
**Channel 3 Efficiency vs Load**  
 $V_{OUT3} = 1.2\text{V}$ ,  $f_{SW} = 1\text{MHz}$



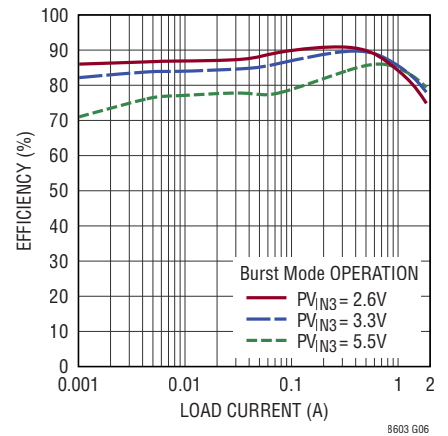
**Channel 1 Efficiency vs Load**  
 $V_{OUT1} = 5\text{V}$ ,  $f_{SW} = 2\text{MHz}$



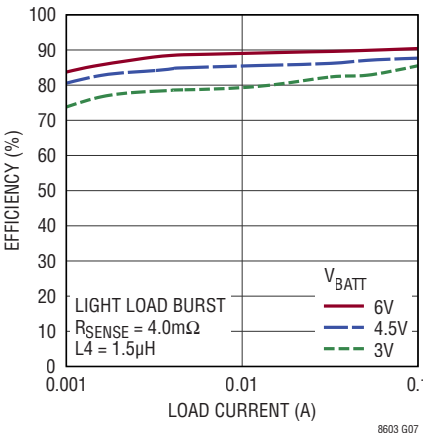
**Channel 2 Efficiency vs Load**  
 $V_{OUT2} = 3.3\text{V}$ ,  $f_{SW} = 2\text{MHz}$



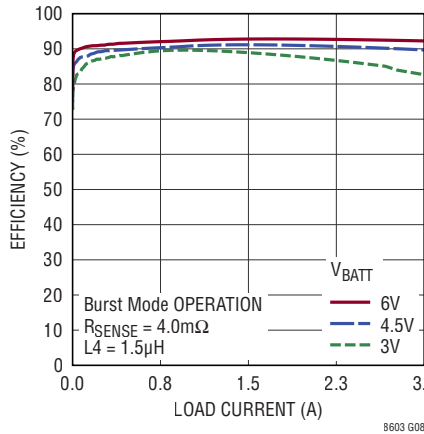
**Channel 3 Efficiency vs Load**  
 $V_{OUT3} = 1.2\text{V}$ ,  $f_{SW} = 2\text{MHz}$



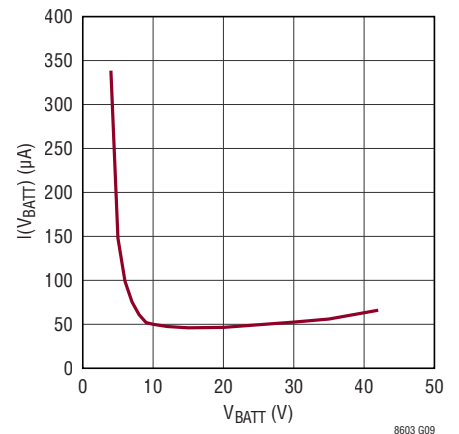
**Channel 4 Efficiency vs Load**  
 $V_{OUT4} = 8\text{V}$ ,  $f_{SW} = 1\text{MHz}$



**Channel 4 Efficiency vs Load**  
 $V_{OUT4} = 8\text{V}$ ,  $f_{SW} = 1.0\text{MHz}$

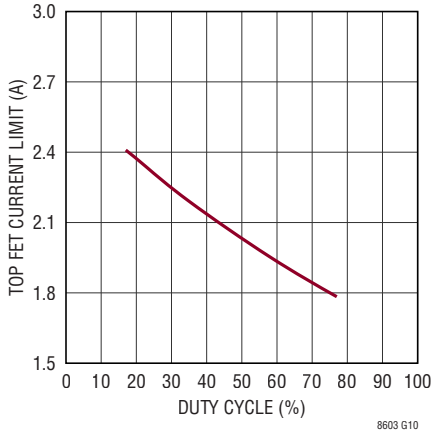


**No-Load I (V<sub>IN</sub>) vs V<sub>IN</sub>**  
All Channels Enabled (Note 4)

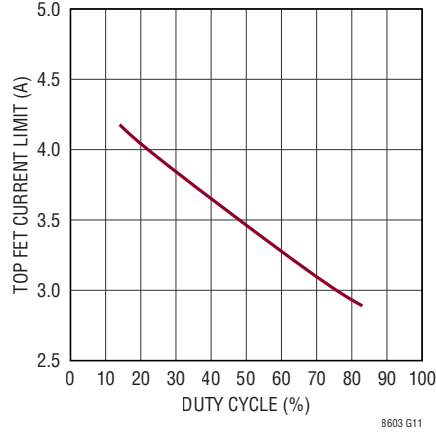


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = PV_{IN1} = PV_{IN2} = 12\text{V}$ ,  $EN/UVLO = 3\text{V}$  and  $PV_{IN3} = 3.3\text{V}$  unless otherwise noted.

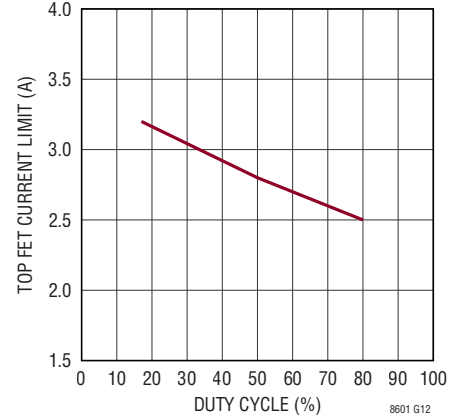
**Channel 1  
Peak Current Limit vs Duty Cycle**



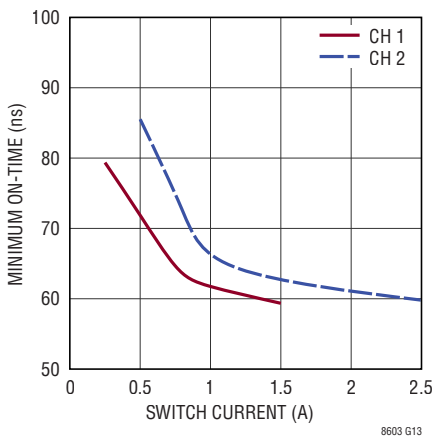
**Channel 2  
Peak Current Limit vs Duty Cycle**



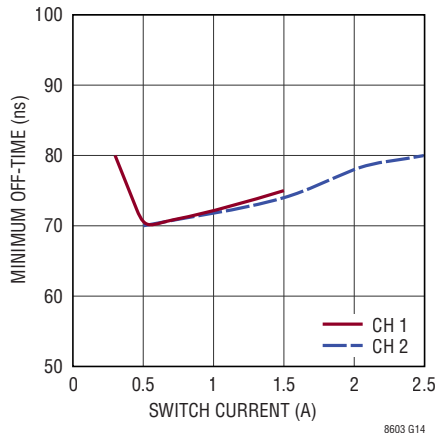
**Channel 3  
Peak Current Limit vs Duty Cycle**



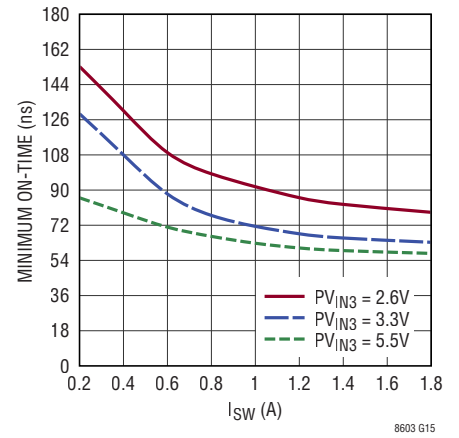
**Channels 1, 2  
Minimum On-Time vs  $I_{SW}$**



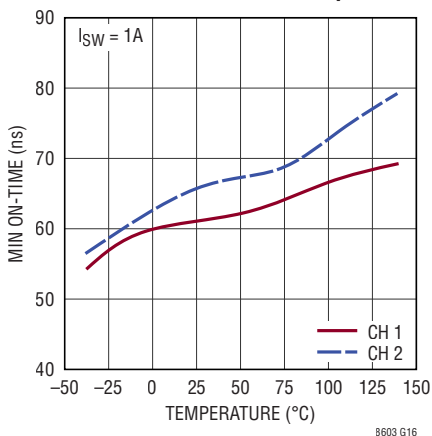
**Channels 1, 2  
Minimum Off-Time vs  $I_{SW}$**



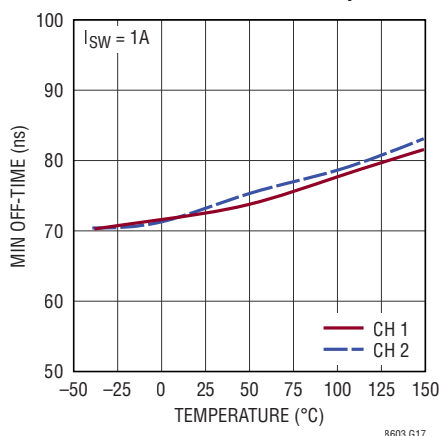
**Channel 3  
Minimum On-Time vs  $I_{SW}$**



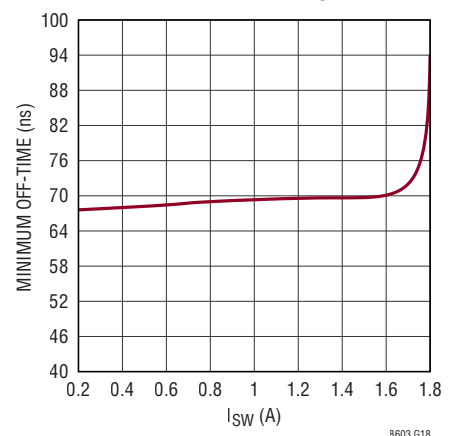
**Channels 1, 2  
Minimum On-Time vs Temperature**



**Channels 1, 2  
Minimum Off-Time vs Temperature**

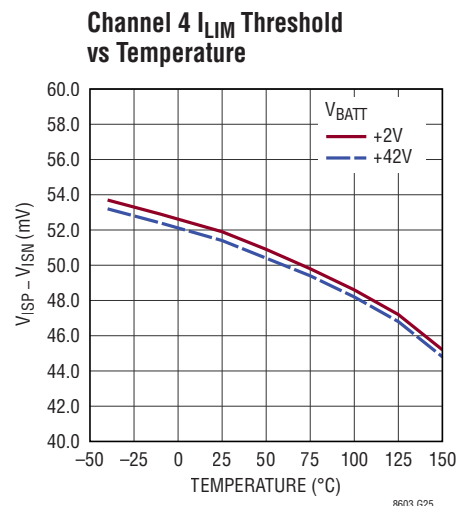
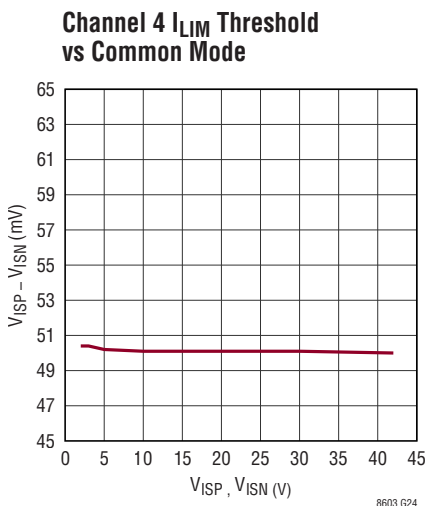
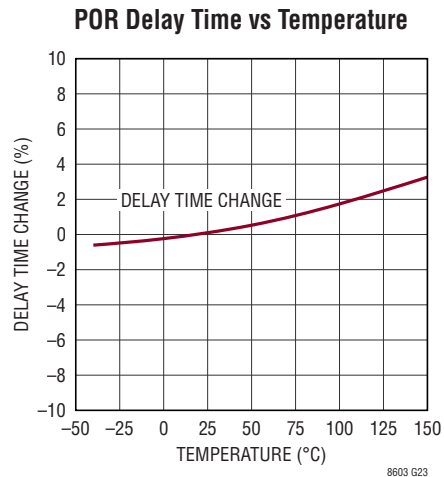
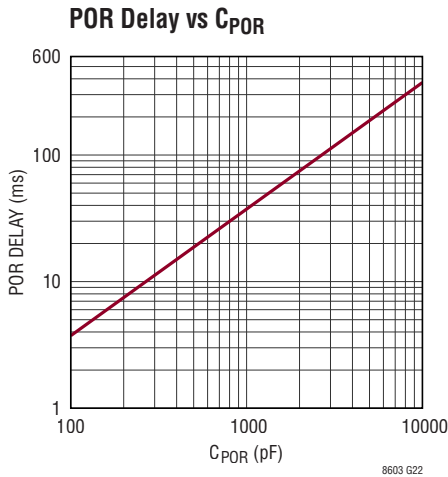
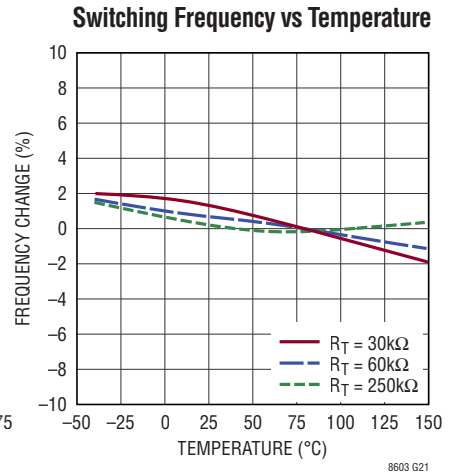
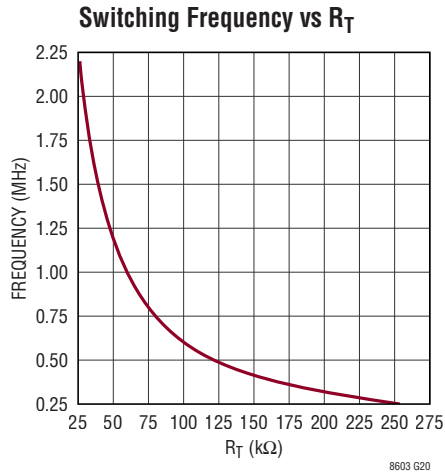
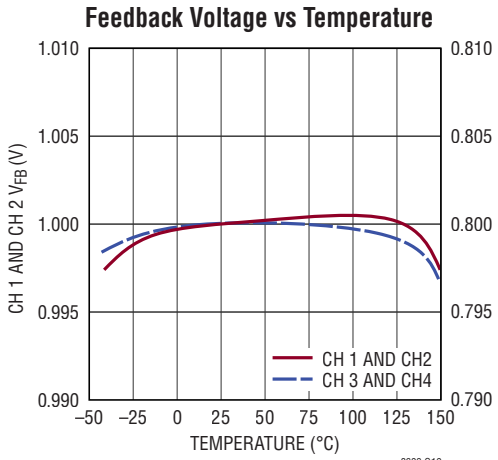


**Channel 3  
Minimum Off-Time vs  $I_{SW}$**



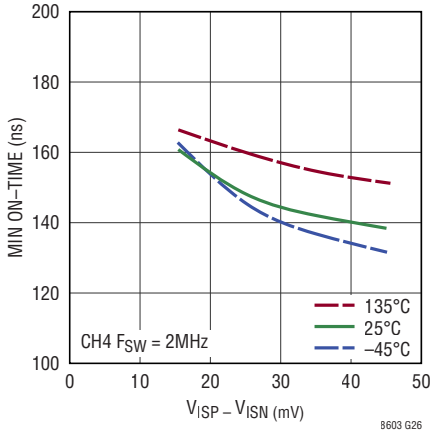


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{IN} = PV_{IN1} = PV_{IN2} = 12\text{V}$ , $EN/UVLO = 3\text{V}$ and $PV_{IN3} = 3.3\text{V}$ unless otherwise noted.

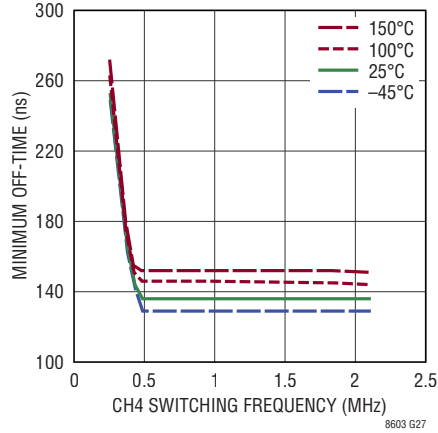


**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{IN} = PV_{IN1} = PV_{IN2} = 12\text{V}$ ,  $EN/UVLO = 3\text{V}$  and  $PV_{IN3} = 3.3\text{V}$  unless otherwise noted.

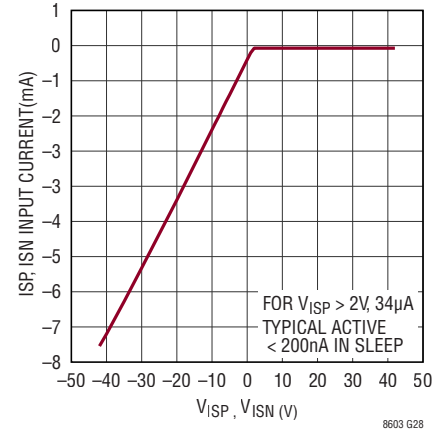
**Channel 4 Minimum On-Time vs  $V_{ISP} - V_{ISN}$**



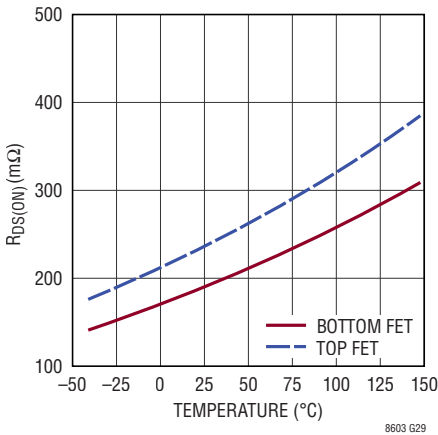
**Channel 4 Minimum Off-Time vs  $V_{ISP} - V_{ISN}$**



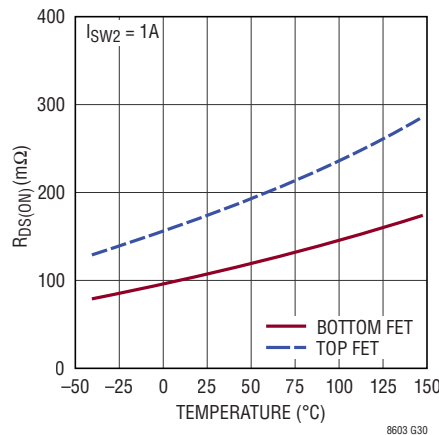
**Channel 4 ISP, ISN Input Current vs  $V_{ISP}$ ,  $V_{ISN}$**



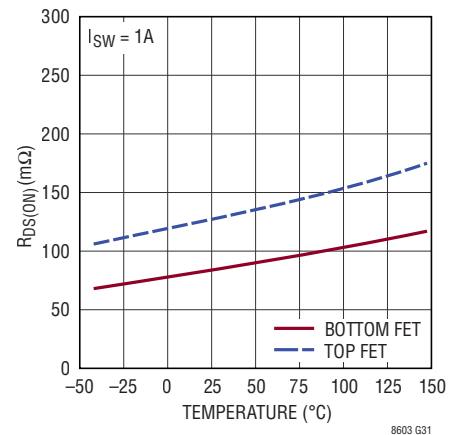
**Channel 1  $R_{DS(ON)}$  vs Temperature**



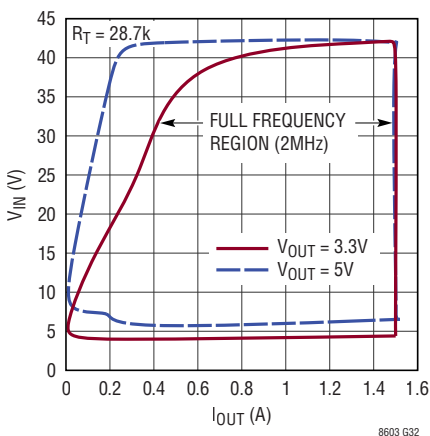
**Channel 2  $R_{DS(ON)}$  vs Temperature**



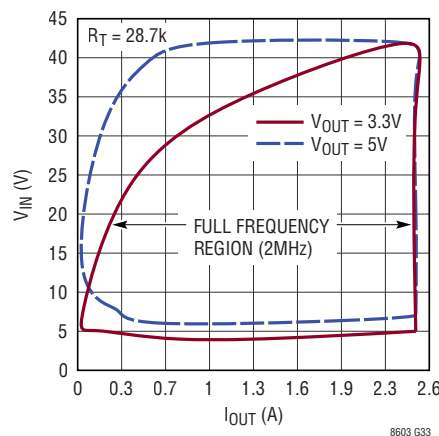
**Channels 3  $R_{DS(ON)}$  vs Temperature**



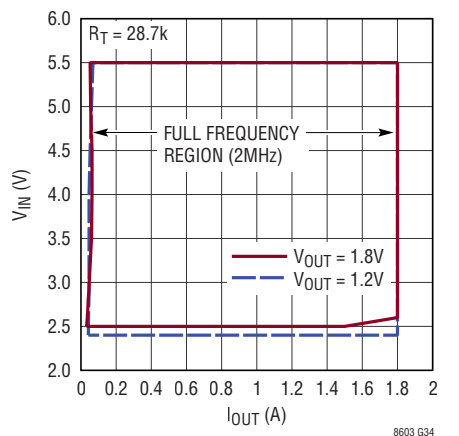
**Channel 1 Full Frequency  $V_{IN}$  vs Load Current**



**Channel 2 Full Frequency  $V_{IN}$  vs Load Current**

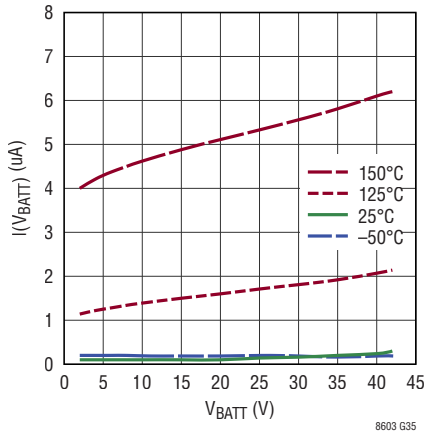


**Channel 3 Full Frequency  $V_{IN}$  vs Load Current**

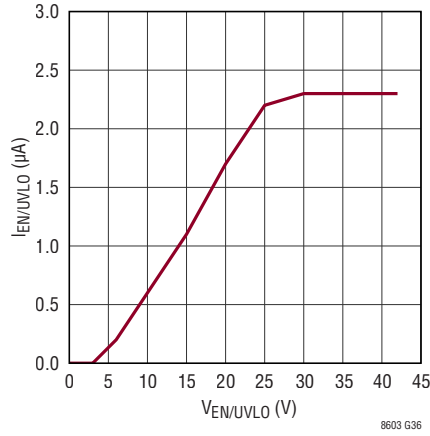


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{IN} = PV_{IN1} = PV_{IN2} = 12\text{V}$ , $EN/UVLO = 3\text{V}$ and $PV_{IN3} = 3.3\text{V}$ , unless otherwise noted.

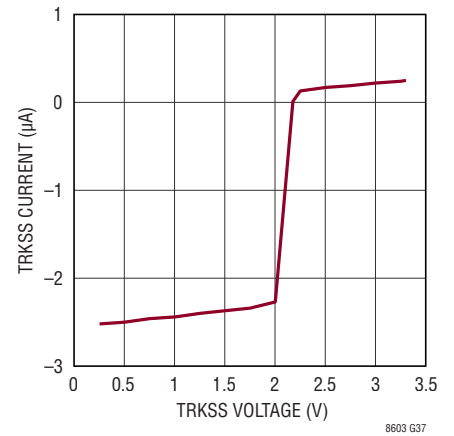
**Shutdown  $I_Q$  from the Battery  
Overvoltage/Temperature**



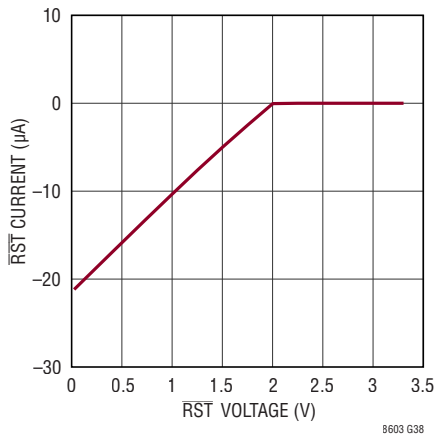
**EN/UVLO Current vs Voltage**



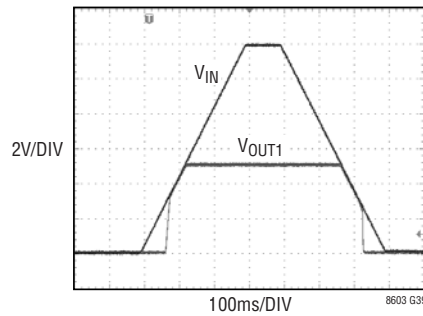
**TRKSS Pull-Up Current vs Voltage**



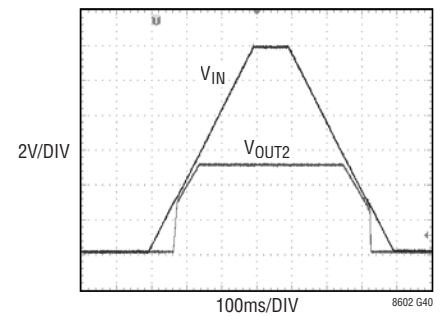
**RST Pull-Up Current vs Voltage**



**Channel 1 Start-Up and Dropout,  
 $R_L = 20\Omega$**

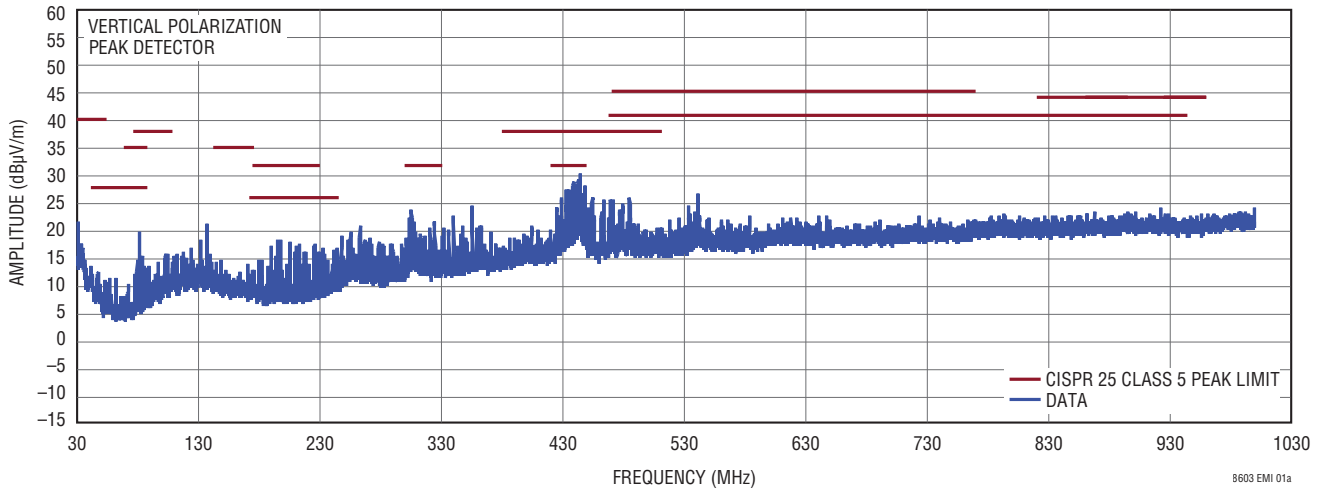


**Channel 2 Start-Up and  
Dropout,  $R_L = 2\Omega$**



**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$

**Radiated EMI Performance, CISPR 25 Radiated Emission Tests with Class 5 Peak Limits**



DC2114A DEMO BOARD  
 (WITH EMI FILTER INSTALLED)  
 $V_{BATT} = 14\text{V}$ ,  $V_{OUT1} = 5\text{V}$ ,  $V_{OUT2} = 3.3\text{V}$ ,  $V_{OUT3} = 1.8\text{V}$ ,  $I_{OUT1,2,3} = 1\text{A}$   
 $f_{SW} = 2\text{MHz}$ ,  $FSELA = INTV_{CC}$ ,  $FSELB = \text{Ground}$

## PIN FUNCTIONS

**PG1, PG2, PG3 (Pins 1, 10, 40):** Power Good Indicators for Channels 1, 2 and 3, respectively. These pins are open-drain outputs that pull down until the associated FB pin is within  $\pm 8\%$  of the target regulation voltage.

**GND (Pins 2, 8, 13, 35, 38, Exposed Pad 41):** Ground. All ground pins and the exposed pad must be soldered to PCB ground. See the Applications Information section for PCB layout recommendations.

**SW1 (Pin 3):** High Voltage Converter 1 Switch Node. This is the output of the internal power switches for Channel 1.

**BST1, BST2 (Pins 4, 5):** Boost Voltage for High Voltage Converters. These pins provide the drive voltage required by the internal power MOSFETs. A capacitor should be connected from BST to the associated SW pin.

**SW2 (Pins 6, 7):** High Voltage Converter 2 Switch Node. This is the output of the internal power switches for Channel 2. These pins should be soldered to the same PCB trace for even current distribution.

**BIAS (Pin 9):** Alternate Power Source for  $INTV_{CC}$  and  $INTV_{CC4}$  Regulators. If  $BIAS > 3.1V$  for  $INTV_{CC}$  or  $> 4.6V$  for  $INTV_{CC4}$  the internal regulators will draw their power from BIAS. This will reduce the on-chip power dissipation during full frequency operation and reduce the effective no-load sleep current at the input.

**PG4 (Pin 11):** Power Good Indicator Channel 4. This pin is an open-drain output that pulls low until the Channel 4 feedback voltage is greater than 92% of its reference voltage.

**FSEL4A, FSEL4B (Pins 12, 17):** Boost Converter Frequency Select and RUN Control. These pins are logic inputs. When both pins are low, the boost controller is shut down. The boost controller switching frequency is controlled using these pins according to Table 2 in the Applications Information section.

**GATE4 (Pin 15):** External MOSFET Gate Drive Output. This pin switches from GND to  $V_{INTV_{CC4}}$  to turn on the low side power MOSFET in the BOOST converter. See

the Applications Information section for information on MOSFET selection.

**$INTV_{CC4}$  (Pin 16):** Internal Boost Regulator Output. Do not load the  $INTV_{CC4}$  pin with external circuitry.  $INTV_{CC4}$  is 4.6V when  $BIAS < 4.6V$ , 5V when  $BIAS > 5V$ , and equal to BIAS when BIAS is between 4.6V and 5V. Decouple to ground with a low ESR 4.7 $\mu$ F capacitor.

**ISP4, ISN4 (Pins 19, 18):** Boost Controller Current Sense Inputs. Connect a current sense resistor of appropriate value between these pins with ISP4 connected to the input supply and ISN4 to the application inductor. See the Applications Information section for sense resistor selection details.

**TRKSS1, TRKSS2 (Pins 21, 20):** Track/Soft-Start Inputs for the High Voltage Converters. When this pin is below 1V, the converter regulates the FB pin to the TRKSS voltage instead of the internal reference. The TRKSS pin has a 2.4 $\mu$ A pull-up current. Connect a capacitor between either of these pins to ground to program a soft-start time for the associated channel.

**EN/UVLO (Pin 22):** Enable/Undervoltage Lockout Input. The LT8603 is in low power shutdown when this pin is below 0.4V. Between 0.4V and 1.1V, the part will turn on the internal reference. A precision threshold at 1.2V (rising) enables the switching regulators. The precision threshold allows the EN/UVLO pin to be used as an input undervoltage lockout by connecting to resistor divider between  $V_{IN}$  and GND. When the EN/UVLO voltage is between 0.4V and 1.2V, the LT8603 input current will depend on the mode selected, the  $V_{IN}$  voltage and EN/UVLO voltage.

**$V_{IN}$  (Pin 23):** Power Supply to Internal Functions. This pin provides power to the LT8603 internal circuitry. This pin must reach 4V for the boost converter to complete its internal soft-start delay of 1ms.

**FB4 (Pin 24):** Feedback Input Pin for the Boost Converter. The converter regulates FB4 to 0.8V.

**FB1, FB2 (Pins 26, 25):** Feedback Input Pins for the High Voltage Converters. The converters regulate the

## PIN FUNCTIONS

corresponding feedback pin to the lesser of 1V or the voltage on the associated TRKSS pin.

**FB3 (Pin 27):** Feedback Input Pin for the Low Voltage Converter. The converter regulates FB3 to 0.8V.

**INTV<sub>CC</sub> (Pin 28):** Internal Regulator Bypass. Do not load the INTV<sub>CC</sub> pin with external circuitry. INTV<sub>CC</sub> is 3.1V when BIAS < 3.1V, 3.4V when BIAS > 3.4V, and equal to BIAS when BIAS is between 3.1V and 3.4V. Decouple to ground with a low ESR 4.7 $\mu$ F capacitor.

**RT (Pin 29):** Frequency Programming Resistor. Connect a resistor between this pin and ground to set the internal oscillator frequency. This pin should not be left open.

**RUN3 (Pin 30):** Enable Input For Low Voltage Channel 3. Channel 3 is enabled when the voltage on this pin exceeds 1.2V. The RUN3 pin has a precise threshold so it can be used to create a UVLO function or be sequenced from another channel. There is an internal soft-start timer which ramps the output up in approximately 1ms.

**CPOR (Pin 31):** Power-On Reset Timing Capacitor. A capacitor from this pin to ground sets the period of the power-on reset oscillator timer. See the Applications Information Section for details.

**RST (Pin 32):** Active Low Reset Output. This pin is the output of the power-on reset function. This pin is an open-drain output with a weak pull-up to approximately 2V. This pin is held low until the power on reset timer times out.

**SYNC (Pin 33):** Clock Synchronization and Mode Select Input. This pin allows the LT8603 to synchronize its switching frequency to an external clock. When an external clock is applied, the LT8603 will operate in pulse-skipping mode. If clock synchronization is not used, connect this pin to ground to enable low ripple Burst Mode operation or connect high to enable pulse-skipping operation.

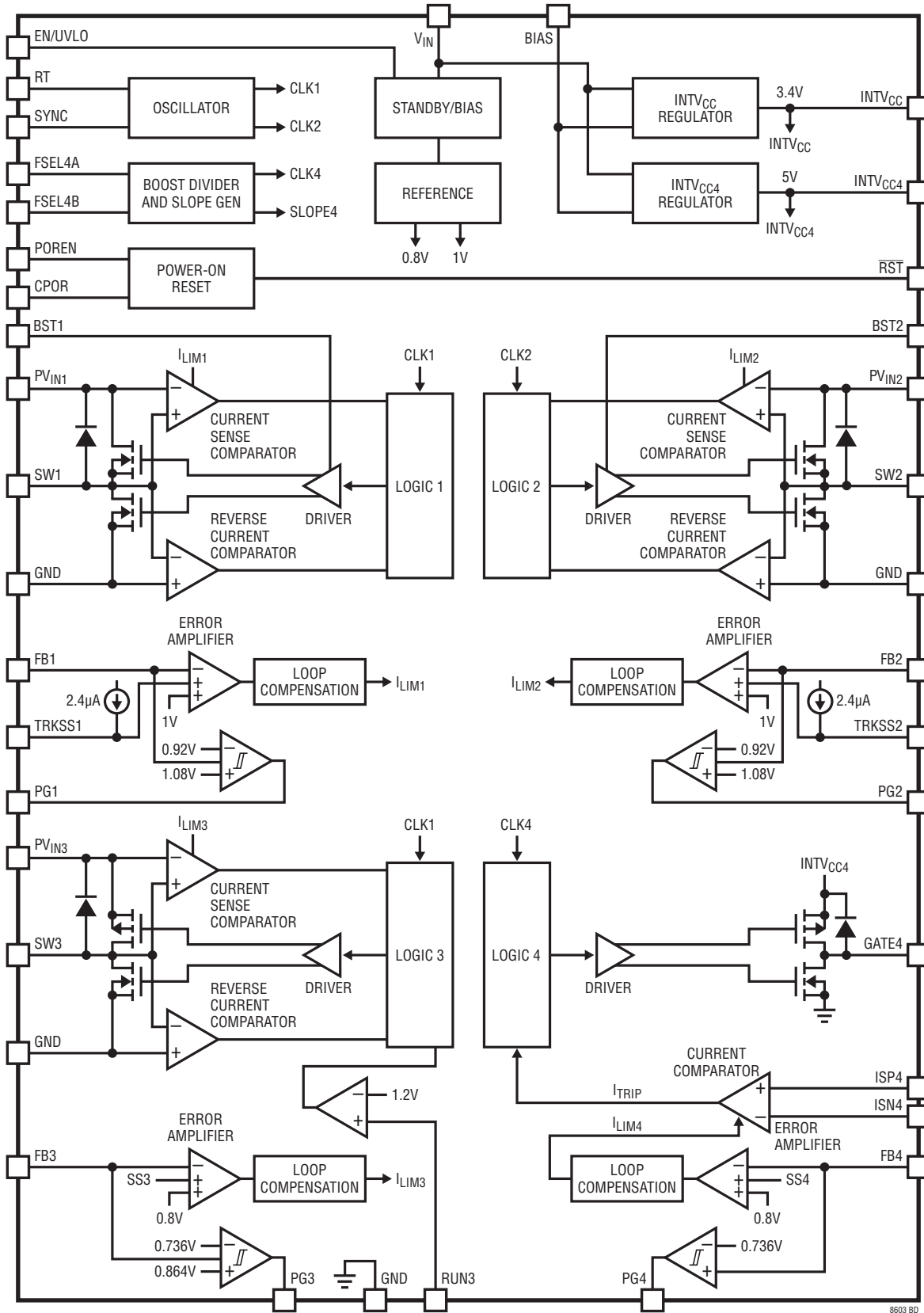
**PV<sub>IN3</sub> (Pin 34):** Input Supply Voltage to Low Voltage Channel 3. This pin will normally be connected to the output of one of the high voltage converters but can be supplied from any voltage in the specified range. It should be bypassed locally with a low ESR ceramic capacitor to ground with a low inductance connection to the exposed pad.

**SW3 (Pin 36):** Low Voltage Converter Switch Node. This is the output of the internal power switches for Channel 3.

**PV<sub>IN1</sub>, PV<sub>IN2</sub> (Pins 37, 14):** Input Supply to High Voltage Channels 1 and 2, respectively. These pins can be powered from the boost converter output or any voltage in the specified range. Each pin should be bypassed locally with a low ESR ceramic capacitor to ground with a low inductance connection to the exposed pad.

**POREN (Pin 39):** Power-On Reset Enable. This is a logic input that starts the ramp on the POR timing capacitor. This input has a weak pull-up to allow direct connection to open-drain outputs.

**BLOCK DIAGRAM**



8603 BD

## OPERATION

The LT8603 combines two 42V input step-down converters (Channels 1 and 2), one 5.5V input step-down converter (Channel 3) and a boost controller (Channel 4) to provide a flexible system that can be configured to generate up to four regulated outputs. For example, the boost controller may be used to guarantee a supply to the high voltage converters above their minimum dropout voltage even during the cold crank cycle in an automobile.

### Start-Up

When enabled by setting the EN/UVLO voltage above its threshold, the LT8603 INTV<sub>CC</sub> regulator charges its output capacitor to supply the internal chip circuitry. If BIAS is higher than 3.1V, BIAS supplies current to the INTV<sub>CC</sub> regulator to reduce V<sub>IN</sub> quiescent current.

The boost controller is enabled with a logic high on either one or both of the FSEL4A and FSEL4B pins. Once enabled, the INTV<sub>CC4</sub> regulator charges its output capacitor bringing the INTV<sub>CC4</sub> supply into regulation. When the voltage at INTV<sub>CC4</sub> exceeds 4.0V, the boost controller gate driver will begin supplying gate drive pulses to the external MOSFET. Like the INTV<sub>CC</sub> regulator, the INTV<sub>CC4</sub> regulator can also draw power from the BIAS pin when BIAS exceeds 4.6V.

### High Voltage Buck Regulators (Channels 1 and 2)

Each high voltage channel is a synchronous buck regulator that operates from an independent PV<sub>IN</sub> pin. The internal top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB pin to control the peak current in the top switch. The reference of the error amplifier is determined by the lower of the internal 1V reference and the voltage at its TRKSS pin. While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2A for Channel 1 or 3.3A for Channel 2 flowing through the bottom switch,

the next clock cycle will be delayed until switch current returns to a safe level. The TRKSS pins can be used for controlled start-up or tracking of another supply.

### Low Voltage Buck Regulator (Channel 3)

The low voltage channel is a synchronous buck regulator that operates from an independent PV<sub>IN</sub> pin. The PV<sub>IN</sub> pin has an undervoltage lockout set at 2.35V. The top power MOSFET is turned on at the beginning of each oscillator cycle, and turned off when the current flowing through the top MOSFET reaches a level determined by the error amplifier. The error amplifier measures the output voltage through an external resistor divider tied to the FB3 pin to control the peak current in the top switch. The reference of the error amplifier is an internal 800mV reference. While the top MOSFET is off, the bottom MOSFET is turned on for the remainder of the oscillator cycle or until the inductor current starts to reverse. If overload conditions result in more than 2.4A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The low voltage channel has a RUN3 pin to allow power sequencing, plus an internal soft-start circuit that ramps the output voltage up in 1ms.

### Boost Controller (Channel 4)

The boost controller includes an error amplifier, loop compensation, current comparator, switch control logic, and a gate driver. The controller is enabled and its clock frequency selected by control of the FSEL4A and FSEL4B pins as described in the Applications Information section.

The required external N-channel MOSFET is turned on by the internal clock and turned off when the inductor current sensed by the current comparator exceeds its threshold. The error amplifier adjusts the current comparator threshold by comparing the FB4 voltage to an internal 0.8V reference voltage. The output voltage is set by a resistor divider from the output to the FB4 pin. The internal INTV<sub>CC4</sub> regulator provides the gate drive for the external MOSFET.



## OPERATION

### Multiphase Switching

The oscillator generates two clock signals 180° out of phase with each other. Channels 1 and 3 operate from CLK1, while Channels 2 and 4 operate from CLK2. The clock for Channel 4 may be selected as either a  $\div 1$ ,  $\div 2$  or  $\div 5$  version of CLK2 using the FSEL4A and FSEL4B pins. Regardless of the divide ratio chosen, the Channel 4 clock edges remain aligned to the CLK2 edges.

Since a buck regulator only draws input current during the top switch on cycle, multiphase operation reduces peak input current and doubles the input current frequency. These effects reduce input current ripple and reduce the input capacitance required.

### Undervoltage Lockout

The EN/UVLO pin is used to put the LT8603 in shutdown, reducing the input current to less than 1 $\mu$ A. The accurate 1.2V threshold of the EN/UVLO pin provides a programmable  $V_{IN}$  undervoltage lockout through an external resistor divider tied to the EN/UVLO pin. A 50mV hysteresis voltage on the EN/UVLO pin prevents switching noise from inadvertently shutting down the LT8603.

### Power Good Comparators

Channels 1, 2 and 3 have power good comparators that trip when the feedback pin is more than 8% above or below its reference voltage. Channel 4 has a power good comparator that indicates when the output voltage is more than 8% below its reference. The PG output pins are open-drain and pulled low when the corresponding output is out of regulation. The PG outputs are not valid until  $INTV_{CC}$  rises to 2.7V.

### Power-On Reset Timer

The LT8603 includes a power-on reset timer. The power-on reset timeout period is adjustable using an external capacitor on the CPOR pin as described in the Applications Information section. The timer is initiated when the POREN pin is higher than 1.2V. The output of the POR timer, the  $\overline{RST}$  pin, is an open-drain output with a weak internal pull-up of 100k to approximately 2V.  $\overline{RST}$  is held low until the expiration of the POR timer. The  $\overline{RST}$  pin is only valid when the LT8603 is enabled and  $INTV_{CC}$  is above 2.7V.

## APPLICATIONS INFORMATION

### SYSTEM ARCHITECTURE

The LT8603 combines three buck converters with a boost controller to provide a flexible system supply that can be configured to generate up to four regulated outputs. The 4 channels are independently powered and can be connected in a variety of ways. For example, the output of the boost may be used to supply the input voltage to the buck converters resulting in three tightly regulated outputs even when the boost input voltage falls below the regulated buck outputs such as occurs during an automotive cold crank scenario. Alternatively, if the boost controller is driven from a buck output or is configured as a SEPIC converter, the LT8603 provides up to four tightly regulated outputs.

### V<sub>IN</sub> Voltage Range

The minimum voltage at V<sub>IN</sub> for the LT8603 internal circuitry and the buck converters to start is 3.1V, however, at least 4V is required for the boost controller and the INTV<sub>CC4</sub> regulator to start. The boost controller can be configured to supply V<sub>IN</sub> and the PV<sub>IN</sub> pins once it has started; after start-up the input voltage to the boost controller can go lower than 3V.

### Enable and Undervoltage Lockout

The EN/UVLO pin can be used to program a minimum system start voltage or an undervoltage lockout (UVLO) voltage. It has an internal threshold of 1.2V with 50mV hysteresis. The UVLO divider circuit is shown in Figure 1.

The UVLO threshold is given by:

$$V_{(UVLO)} = \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \cdot 1.2V$$

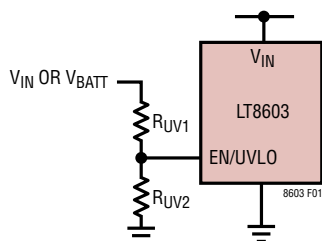


Figure 1. UVLO Divider

### Switching Frequency

All 4 channels share a single oscillator. The buck channels switch at the oscillator frequency. The boost channel can switch at f<sub>OSC</sub>, f<sub>OSC</sub>/2 or f<sub>OSC</sub>/5. The switching frequency range of all 4 channels should be determined before selecting the oscillator frequency. A low frequency usually provides better efficiency and a wider operating range due to lower switching losses and less sensitivity to timing constraints such as minimum on- and off-times. A high switching frequency uses smaller components and moves the switching noise away from sensitive frequency bands, such as the AM radio band, but does so at the cost of lower efficiency. A high switching frequency also decreases the duty cycle range because of finite minimum on- and off-times which are independent of the switching frequency.

The oscillator frequency can be programmed from 250kHz to 2.2MHz by tying a resistor from the RT pin to ground. Table 1 shows the necessary value of R<sub>T</sub> for some common switching frequencies.

Table 1. Oscillator Frequency (f<sub>OSC</sub>) vs R<sub>T</sub> Value

OSCILLATOR FREQUENCY (MHz)	R <sub>T</sub> (kΩ)
0.25	244
0.35	173
0.5	120
0.75	79.2
1.0	58.9
1.25	46.8
1.5	38.7
1.75	33.0
2.0	28.7
2.2	26.0

The following equation approximates the values shown in Table 1:

$$R_T = \frac{59.8}{(f_{OSC} - 0.007)} - 1.3$$

The RT pin is sensitive to noise so the resistor should be placed close to the LT8603 and away from noise sources.

## APPLICATIONS INFORMATION

The internal oscillator of the LT8603 can be synchronized to an external clock of 250kHz up to 2.2MHz applied to the SYNC pin. The  $R_T$  value should be chosen such that the frequency set by  $R_T$  is close to the anticipated external clock frequency.

### Mode Selection and Synchronization

To select low ripple Burst Mode operation, the SYNC pin should be connected to a voltage below 0.3V such as ground. To select pulse-skipping operation, connect the SYNC pin to an available voltage above 1.2V such as  $INTV_{CC}$ .

To synchronize the LT8603 to an external frequency, drive the SYNC pin with a pulse train with a high voltage above 1.2V and a low voltage below 0.3V. The minimum pulse width is 120ns for a high pulse and 90ns for a low pulse. The LT8603 will operate in pulse-skipping mode while synchronized to an external clock. The LT8603 may be synchronized over a 250kHz to 2.2MHz range. The  $R_T$  resistor should be chosen to set the LT8603 switching frequency close to the synchronization input.

For some applications it is desirable for the LT8603 to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First, in pulse-skipping mode the clock stays awake at all times and all switching cycles are aligned to the clock. Second, full frequency switching is reached at a lower output load in pulse-skipping than Burst Mode operation. These two differences come at the expense of increased quiescent current for pulse-skipping. To enable pulse-skipping mode, the SYNC pin is tied high either to a logic output or to the  $INTV_{CC}$  pin. Do not leave the SYNC pin floating.

### $INTV_{CC}$ Regulator

The  $INTV_{CC}$  supplies the common circuitry such as the oscillator and reference but its main current demand comes from the gate drivers for the high voltage buck converters. The current draw will depend on the operating frequency, the higher the switching frequency, the greater the current drawn from  $INTV_{CC}$ . The regulator is supplied by  $V_{IN}$  at start-up, but it will draw its supply current from BIAS if BIAS is at least 3.1V. If the BIAS

pin is connected to a switching regulator channel it will improve efficiency, reduce on-chip dissipation and lower the sleep current. The  $INTV_{CC}$  may be used to configure other inputs and supply pull-ups related to the LT8603. It is not recommended to draw more than 1mA or connect  $INTV_{CC}$  to any components not related to the LT8603 to avoid unexpected interactions.

## BOOST CONTROLLER

### Functional Description

Channel 4 is a set of functional elements that are connected to external components to form a boost converter. The Block Diagram in Figure 2 shows these elements and how they are connected internally.

The error amplifier compares a fractional part of the output voltage to an 800mV reference. The output,  $I_{LIM4}$ , goes to the current comparator to set the peak current.

The current comparator senses the inductor current using a small sense resistor across the ISP4 and ISN4 pins. The trip level is set by the error amplifier output,  $I_{LIM4}$ , and the slope compensation signal, SLOPE4. The maximum

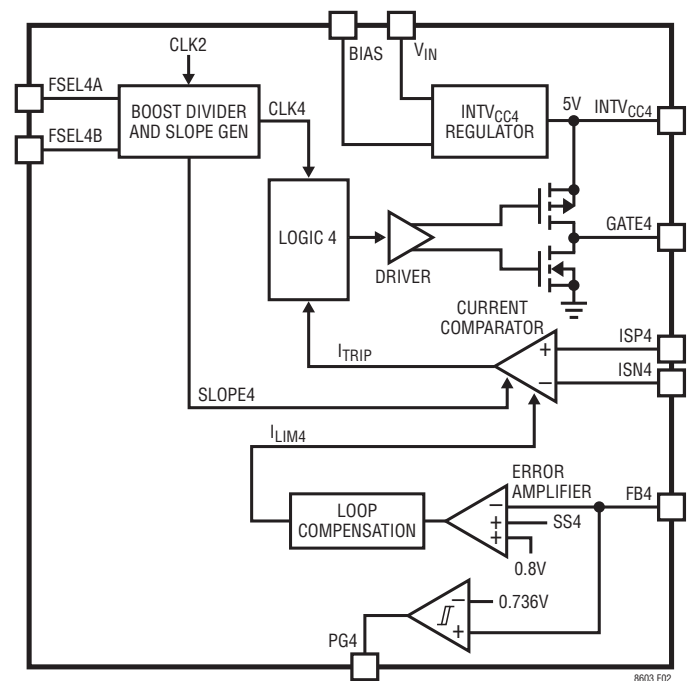


Figure 2. Boost Controller Block Diagram

## APPLICATIONS INFORMATION

trip level is 50mV. ISP4 and ISN4 have an operational common range of 2V to 42V and an absolute maximum rating of  $\pm 42V$ . This allows reverse battery protection with a single diode in series with external MOSFET drain.

The logic block turns on the external MOSFET on a CLK4 signal, and then turns it off on an I<sub>TRIP</sub> from the current comparator, or when maximum duty cycle is reached.

The LT8603 has a frequency divider that allows the controller switching frequency to be less than the oscillator frequency. The boost controller is specified for a f<sub>SW</sub> between 250kHz and 2.2MHz; do not set the divider to operate the boost controller below 250kHz. The FSEL4A and FSEL4B pins control the oscillator frequency as shown in Table 2.

**Table 2. Boost Frequency Selection**

BOOST FREQ f <sub>SW4</sub>	FSEL4A	FSEL4B
0 (Boost Shutdown)	Low	Low
f <sub>osc</sub> /5	High	Low
f <sub>osc</sub> /2	Low	High
f <sub>osc</sub>	High	High

The boost controller is enabled by the FSEL4A and FSEL4B pins. When both pins are low, the boost controller is shut down. When either or both pins are set high, a boost controller start-up sequence is initiated. During start-up, the INTV<sub>CC4</sub> regulator is turned on charging the external INTV<sub>CC4</sub> capacitor. Once INTV<sub>CC4</sub> reaches 4V, the controller logic is turned on and switching begins. A 1ms soft-start ramp is applied to the error amplifier to minimize inrush current.

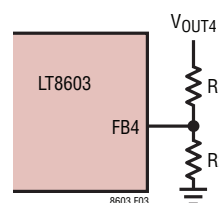
The INTV<sub>CC4</sub> regulator is a low dropout, linear regulator that provides power to the GATE4 drive circuit. It is dedicated to the boost controller and is shut down when the boost controller is shut down. It can draw power from either V<sub>IN</sub> or BIAS, depending on the BIAS voltage. When BIAS is less than 4.6V, the regulator will draw power from V<sub>IN</sub> and regulate to 4.6V. When BIAS is greater than 4.6V but less than 5V, the regulator sets INTV<sub>CC4</sub> equal to BIAS and draws power from BIAS. When BIAS is greater than

5V, the regulator generates 5V and draws power from BIAS. Do not use the INTV<sub>CC4</sub> output for external circuitry.

A comparator senses when the output voltage is above 92% of the programmed value and generates a power good signal at the PG4 pin.

### Setting the Output Voltage

The boost controller's output voltage is set by connecting the FB4 pin to a resistor divider from the output as shown in Figure 3.



**Figure 3. Feedback Resistor Divider**

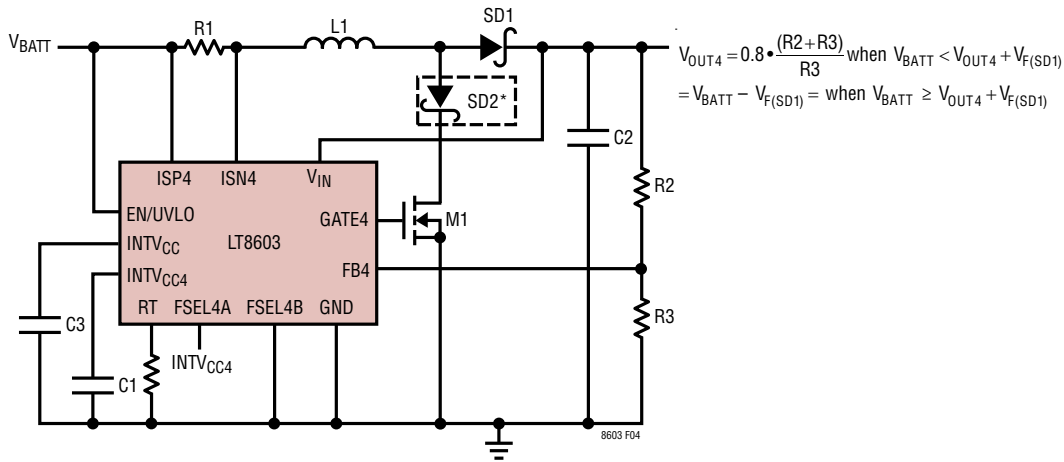
The value of R2 is best selected first as this establishes how much current is in the string based on  $I = V_{FB4}/R2$  where  $V_{FB4} = 0.8V$ . The current should be chosen such that it is not influenced by anticipated leakage or noise. R1 can then be calculated from:

$$R1 = R2 \cdot ((V_{OUT4}/V_{FB4}) - 1)$$

### Boost Configuration

The LT8603 boost controller configured as a standard boost regulator is shown in Figure 4. The boost controller output voltage is set by connecting FB4 to an external divider. For the following example, R2 and R3 are chosen such that  $OUT4 = 8V$ . If the battery voltage (V<sub>BATT</sub>) is above 8V plus a diode forward voltage, the boost controller will be inactive consuming minimal quiescent current. If the battery voltage drops below 8V plus a diode forward voltage, such as during an automotive cold crank cycle, the boost controller will become active to maintain 8V at OUT4. With OUT4 connected to V<sub>IN</sub>, the input supply must reach 4V plus the diode forward voltage to start.

APPLICATIONS INFORMATION



\*SD2 IS FOR REVERSE INPUT PROTECTION. SHORT IF NOT NEEDED.

Figure 4. Channel 4 in Boost Configuration

Once started however, the LT8603 will maintain the output voltage at OUT4 with  $V_{BATT}$  as low as 2V. The ISP4 and ISN4 pins sense the inductor current for the current mode control loop across current sense resistor R1. The ISP4 and ISN4 pins will accurately sense the inductor current down to 2V and will tolerate negative voltages as large as -42V without damage.

By adding diode SD2 in series with the main switch transistor M1, the entire regulator will be tolerant of negative input supply voltages.

One of the limitations of the boost configuration is that it cannot provide short-circuit protection for the boost output as the diode always provides a DC current path from input to output. If short-circuit overload protection is required the SEPIC configuration should be considered. See the SEPIC Configuration section for more information on the SEPIC converter.

**Boost: Duty Cycle and Max Switching Frequency**

In continuous conduction mode (CCM), the operating duty cycle as a function of input and output voltage is given by:

$$D = \left( \frac{V_{OUT} + V_D - V_{BATT}}{V_{OUT} + V_D} \right)$$

where  $V_D$  is the forward voltage drop of the diode.

Thus the maximum duty cycle ( $D_{MAX}$ ) in terms of the minimum  $V_{BATT}$  is:

$$D_{MAX} = \frac{V_{OUT} + V_D - V_{BATT(MIN)}}{V_{OUT} + V_D}$$

For a given input and output voltage, the switching frequency is limited by the expected maximum duty cycle,  $D_{MAX}$ , and minimum switch off time,  $t_{OFF(MIN)}$ . The  $f_{SW(MAX)}$  at  $D_{MAX}$  is given by:

$$f_{SW(MAX)} = \frac{D_{MAX}}{t_{OFF(MIN)}}$$

**Boost: Inductor and Sense Resistor Selection**

The boost regulator inductor and sense resistor ( $R_{SENSE}$ ) should be sized according to the maximum input current. The maximum input current will occur at the minimum input voltage (maximum duty cycle) and maximum output load.

The maximum average inductor current, which is equal to the average input current, can be calculated from:

$$I_{L(MAX)} = \frac{I_{OUT(MAX)}}{1 - D_{MAX}}$$

## APPLICATIONS INFORMATION

From this the ripple current can be specified using:

$$\Delta I_L = \chi \cdot I_{L(\text{MAX})} = \chi \cdot I_{\text{OUT}(\text{MAX})} \cdot \frac{1}{1 - D_{\text{MAX}}}$$

where  $\chi$  in the above equation represents the percentage peak-to-peak ripple current in the inductor relative to  $I_{L(\text{MAX})}$ . Choosing the inductor ripple current,  $\Delta I_L$ , has a direct impact on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of  $\Delta I_L$  increases the converter's output current capability but requires larger inductors. Choosing larger values of  $\Delta I_L$  provides faster transient response and allows the use of smaller inductors but results in higher input current ripple, greater core losses, and lower output current capability. In addition, larger values of  $\Delta I_L$  at high duty cycle may result in sub-harmonic oscillation. The typical range for  $\chi$  is 20% to 40% though careful evaluation of system stability should be made to ensure adequate design margin. The peak inductor current will be the average inductor current plus half the ripple current. The LT8603 current sense comparator has a built-in current limit threshold of 50mV across ISP4 and ISN4 so the peak voltage across the sense resistor should be kept to no more than 80% of this or 40mV. Therefore, the value of  $R_{\text{SENSE}}$  should be:

$$R_{\text{SENSE}} = \frac{0.04}{I_{L(\text{PEAK})}}$$

$I_{L(\text{PEAK})}$  can be calculated from:

$$I_{L(\text{PEAK})} = \left(1 + \frac{\chi}{2}\right) \cdot \frac{I_{\text{OUT}(\text{MAX})}}{1 - D_{\text{MAX}}}$$

The inductor value to achieve the required ripple is given by following equation:

$$L = \frac{V_{\text{BATT}(\text{MIN})}}{\Delta I_L \cdot f_{\text{SW}}} \cdot D_{\text{MAX}}$$

The inductor should have a saturation current exceeding the current limit value of:

$$I_{\text{LIM}} = \frac{0.05}{R_{\text{SENSE}}}$$

Finally, the ESR and magnetic loss of the inductor contribute to overall system power loss. For best efficiency, an inductor with low ESR and a core rated for the desired operating frequency should be chosen. The sense resistor should be chosen to have adequate power handling capability. The maximum power dissipation is given by:

$$P_{\text{RSENSE}} = \frac{0.05^2}{R_{\text{SENSE}}}$$

For example, a 4m $\Omega$  could dissipate up to 0.625W.

### Boost: MOSFET Selection

For the boost configuration, the selected external MOSFET should have a  $BV_{\text{DSS}}$  rating exceeding, with margin, the larger of either the maximum input voltage or the boost output voltage plus a diode forward voltage. The maximum input voltage should include careful consideration of possible transient conditions. In addition, the chosen MOSFET should be compatible with the LT8603's nominal gate drive of 4.6V and have a low value of  $R_{\text{DS}(\text{ON})}$  for best efficiency. The current rating for the MOSFET must be greater than the peak inductor current. Finally, the maximum gate drive current required by the external MOSFET should not exceed the 40mA capability of the LT8603. The current drawn by the gate driver is given by:

$$I_{\text{DRIVE}} = Q_g \cdot f_{\text{SW}}$$

where  $Q_g$  is the MOSFET gate charge and  $f_{\text{SW}}$  is programmed switching frequency.

For example, if  $Q_g$  is 20nC and  $f_{\text{SW}}$  is 1MHz, the drive requirement is 20mA.

### Boost: Diode Selection

In the boost converter, the rectifier diode, SD1, only conducts when the switch is off. The average diode current is equal to the output current. The peak current is equal to the peak inductor current and is given by:

$$I_{\text{D}(\text{PEAK})} = \left(1 + \frac{\chi}{2}\right) \cdot \frac{I_{\text{OUT}(\text{MAX})}}{1 - D_{\text{MAX}}}$$

## APPLICATIONS INFORMATION

The power dissipated by the diode is given by:

$$P_D = I_{OUT(MAX)} \cdot V_D$$

Therefore, a rectifier diode should be chosen with a low forward voltage drop at peak current for best efficiency and a reverse breakdown voltage greater than  $V_{OUT4(MAX)}$ .

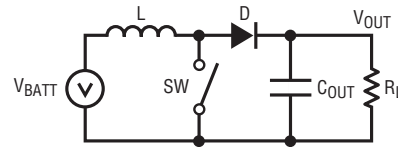
If the reverse protection diode (SD2) is needed, the reverse breakdown voltage must be greater than the desired reverse polarity protection.

### Boost: Output Capacitor

The output capacitor has two essential functions. First, the output capacitor filters the LT8603's discontinuous output current to produce the DC output current. In this role, the capacitor determines the output ripple, thus low impedance at the switching frequency is important. Second, the output capacitor stores energy in order to satisfy transient load conditions and stabilize the LT8603's control loop. Typically, the low equivalent series resistance of X5R and X7R ceramic capacitors provide low output ripple and good transient response.

For some applications, transient performance can be improved with higher output capacitance and/or the addition of a feedforward capacitor placed between the boost output voltage and the boost feedback pin. Note that larger output capacitance may be required when lower switching frequencies are used or when there is significant inductance to the load due to long wire or cables. Increasing the output capacitance will also decrease the output ripple.

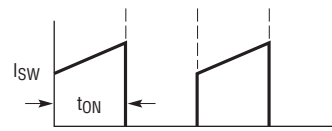
When choosing a capacitor, special attention should be given to the capacitor's data sheet to understand the effective capacitance under the relevant operating conditions of voltage bias and temperature. For good starting values, refer to the Typical Applications section. For all applications, careful evaluation of system stability should be made to ensure adequate design margin.



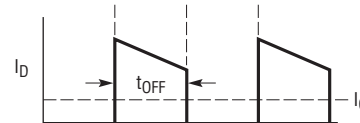
5a. Circuit Diagram



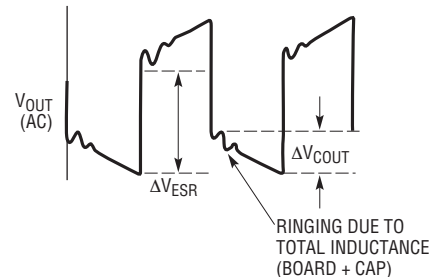
5b. Inductor and Input Currents



5c. Switch Current



5d. Diode and Output Currents



5e. Output Voltage Ripple Waveform

8603 F05

Figure 5. Switching Waveforms for a Boost Converter

### Boost: Input Capacitor

The input capacitor is in series with the inductor so the input current waveform is continuous and the  $d_i/d_t$  is limited.

An input capacitor should be chosen to handle the RMS input capacitor ripple current as given by:

$$I_{RMS(CIN)} = 0.6 \cdot \chi \cdot I_{OUTMAX}$$

## APPLICATIONS INFORMATION

Ensure that capacitors present at the input are rated to withstand any voltage transients that may be applied.

The value of input capacitance is a function of the source impedance. In general, the higher the source impedance, the higher the required input capacitance. The Typical Applications section provides reasonable starting values for input capacitance but careful evaluation of each application must be made to ensure adequate design margin.

### SEPIC Configuration

Figure 6 shows the boost controller configured as a single-ended primary inductance converter or SEPIC. The SEPIC configuration offers two primary advantages over the standard boost configuration. First, it operates like a buck/boost which means it will regulate to an accurate output voltage for any input voltage. Second, it offers short-circuit protection and 0V output in shutdown since there is no DC path from the input to the output. The disadvantage is a more complex circuit requiring additional components as compared to a standard boost configuration. Since there is no DC path to the output, the LT8603  $V_{IN}$  cannot be connected directly to the SEPIC output. As a result, diode SD3 is used to ensure start-up, and SD4 is used to ensure operation to low  $V_{BATT}$  once started. If

$V_{BATT}$  drops below 4V after the SEPIC is in regulation, SD4 maintains  $V_{IN}$  at the SEPIC output voltage. Just as with the standard boost configuration, optional diode SD2 provides reverse battery protection.

Figure 7 shows a simplified topology and the current flow for each of the switch positions once steady state is reached. Both inductors increase current during the switch on cycle (Figure 7b). The DC currents of L1 and L2 are not necessarily equal:  $I_{L1(DC)}$  must be equal to  $I_{VBATT(DC)}$  since there is no other DC path for the current flow from  $V_{BATT}$ . By the same argument,  $I_{L2(DC)}$  must be equal to  $I_{OUT(DC)}$ . Figure 8 shows the current waveforms of the SEPIC converter.

Although uncoupled inductors can be used in the SEPIC converter, coupled inductors provide several advantages and are preferred for most applications. Uncoupled inductors require double the inductance of the coupled inductors and two inductors at twice the inductance usually cost more than one coupled inductor. Also, uncoupled inductors form a tank with the coupling capacitor which can ring at very low frequencies. Uncoupled inductors can be an advantage, however, in high power or high duty cycle converters since the current is split between two cores.

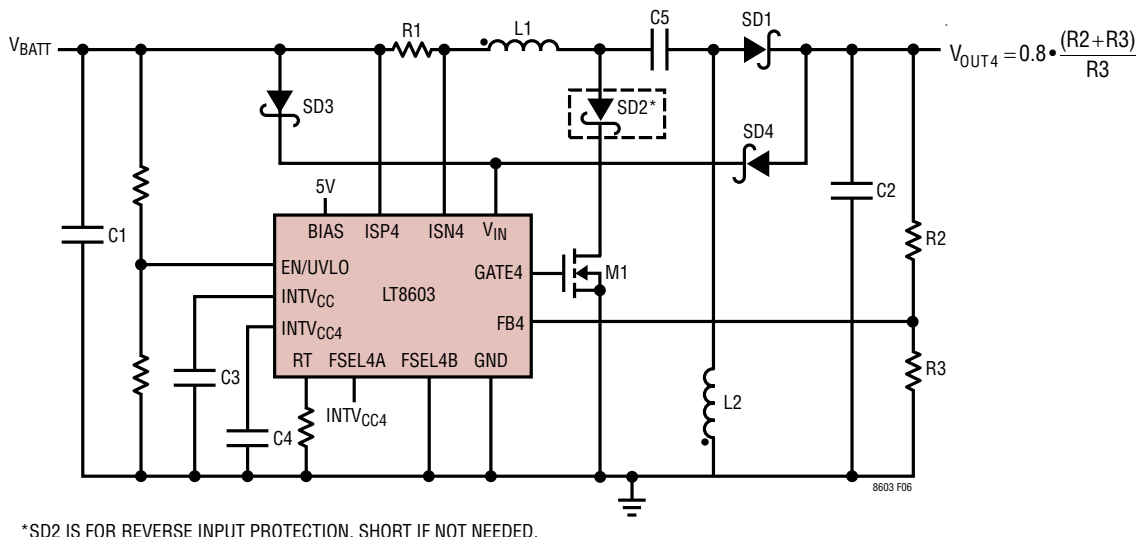
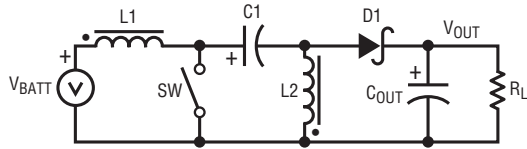


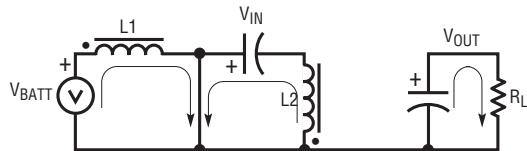
Figure 6. Channel 4 in SEPIC Configuration



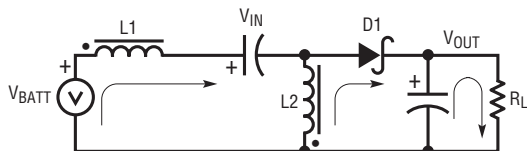
## APPLICATIONS INFORMATION



7a. SEPIC Topology



7b. Current Flow During Switch On-Time



7c. Current Flow During Switch Off-Time

8603 F07

Figures 7. SEPIC Topology and Current Flow

### SEPIC: Duty Cycle and Frequency

With the SEPIC configuration operating in continuous conduction mode (CCM), the duty cycle is given by:

$$D = \left( \frac{V_{OUT} + V_D}{V_{BATT} + V_{OUT} + V_D} \right)$$

The maximum switching frequency of the SEPIC converter is limited by both maximum and minimum duty cycles. The maximum duty cycle is set by  $V_{BATT(MIN)}$ . The maximum switching frequency,  $f_{SW(MAX)}$  at  $V_{BATT(MIN)}$  is given by:

$$f_{SW(MAX)@V_{BATT(MIN)}} = 1 - \frac{\left[ \frac{V_{OUT} + V_D}{V_{BATT(MIN)} + V_{OUT} + V_D} \right]}{t_{OFF(MIN)}}$$

The minimum duty cycle is set by  $V_{BATT(MAX)}$ . The maximum switching frequency at  $V_{BATT(MAX)}$  is given by:

$$f_{SW(MAX)@V_{BATT(MAX)}} = \frac{\left[ \frac{V_{OUT} + V_D}{V_{BATT(MAX)} + V_{OUT} + V_D} \right]}{t_{ON(MIN)}}$$

The lower of these frequencies is the maximum switching frequency for the SEPIC converter.

### SEPIC: Inductor and $R_{SENSE}$ Selection

Choosing the inductor ripple current,  $\Delta I_L$ , has a direct impact on the choice of the inductor value and the converter's maximum output current capability. Choosing smaller values of  $\Delta I_L$  increases the converter's output current capability but requires larger inductors. Choosing larger values of  $\Delta I_L$  provides faster transient response and allows the use of smaller inductors but results in higher input current ripple, greater core losses, and lower output current capability. In addition, larger values of  $\Delta I_L$  at high duty cycle may result in sub-harmonic oscillation.

Given an operating input voltage range and operating frequency, the inductor value is given by:

$$L = \frac{V_{BATT(MIN)} \cdot D_{MAX}}{\Delta I_L \cdot f_{SW}}$$

where,

$$\Delta I_L = \frac{\chi \cdot I_{OUT(MAX)} \cdot D_{MAX}}{1 - D_{MAX}}$$

$\chi$  in the above equation represents the percentage peak-to-peak ripple current in the inductor relative to the maximum average inductor current. The typical range of  $\chi$  is 20% to 40% though careful evaluation of system stability should be made to ensure adequate design margin.

For coupled inductors,  $L1 = L2$  and the effective inductance is doubled due to the mutual inductance. The value of each equal winding is given by:

$$L1 = L2 = \frac{V_{BATT(MIN)} \cdot D_{MAX}}{2 \cdot \Delta I_L \cdot f_{SW}}$$

The maximum input current of the SEPIC converter is calculated at the minimum input voltage and full load current.

The peak inductor current can be significantly higher than the output current. The following equations assume CCM operation and calculate the maximum peak inductor current at minimum  $V_{BATT}$ :

## APPLICATIONS INFORMATION

For a coupled inductor:

$$I_{L(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{OUT(MAX)} \cdot \left(1 + \frac{V_{OUT} + V_D}{V_{BATT(MIN)}}\right)$$

For uncoupled inductors:

$$I_{L1(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{OUTMAX} \cdot \frac{V_{OUT} + V_D}{V_{BATT(MIN)}}$$

$$I_{L2(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{OUT(MAX)} \cdot \frac{V_{BATT(MIN)} + V_D}{V_{BATT(MIN)}}$$

R<sub>SENSE</sub> can then be calculated by:

$$R_{SENSE} = \frac{0.04}{I_{L1(PEAK)}}$$

The chosen inductor(s) should be rated for the maximum expected current.

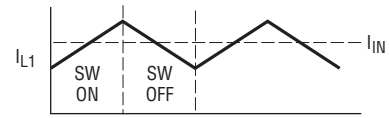
### SEPIC: MOSFET Selection

For the SEPIC configuration, the selected MOSFET should have a BVD<sub>SS</sub> rating exceeding, with margin, the maximum input voltage plus the maximum output voltage plus the maximum diode forward voltage. The maximum input voltage should include careful consideration of possible transient conditions. In addition, the chosen MOSFET should be compatible with the LT8603's nominal gate drive of 4.6V and have a low value of R<sub>DS(ON)</sub> for best efficiency. The current rating for the MOSFET must be greater than the peak switch current of:

$$I_{SW(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{OUT(MAX)} \cdot \frac{1}{1 - D_{MAX}}$$

Finally, the maximum gate drive current required by the external MOSFET should not exceed the 40mA capability of the LT8603. The current drawn by the gate driver is given by:

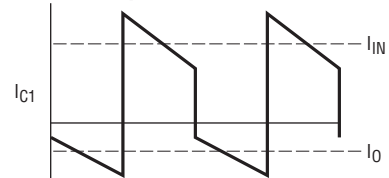
$$I_{DRIVE} = Q_g \cdot f_{SW}$$



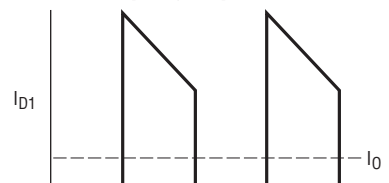
8a. Input Inductor Current



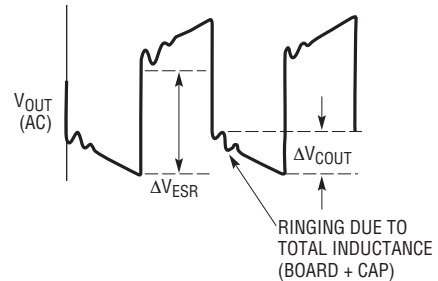
8b. Output Inductor Current



8c. DC Coupling Capacitor Current



8d. Diode Current



8e. Output Ripple Voltage

8603 F08

Figure 8. SEPIC Converter Switching Waveforms

### SEPIC: Diode Selection

For the rectifier diode, SD1, the peak reverse voltage that the diode must withstand is:

$$V_{BATT(MAX)} + V_{OUT}$$

The average forward current is equal to the output current and the peak current is given by:

$$I_{D(PEAK)} = \left(1 + \frac{\chi}{2}\right) \cdot I_{OUT(MAX)} \cdot \left(\frac{V_{OUT} + V_D}{V_{BATT(MIN)}} + 1\right)$$