Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

65V, 8A Synchronous Step-Down Silent Switcher 2 with 2.5µA Quiescent Current

FEATURES

- **Silent Switcher®2 Architecture**
  - **Ultralow EMI/EMC Emissions on Any PCB**
  - **Eliminates PCB Layout Sensitivity**
  - **Internal Bypass Capacitors Reduce Radiated EMI**
  - **Optional Spread Spectrum Modulation**
- **High Efficiency at High Frequency**
  - **Up to 95% Efficiency at 1MHz, $12V_{IN}$ to $5V_{OUT}$**
  - **Up to 94% Efficiency at 2MHz, $12V_{IN}$ to $5V_{OUT}$**
- **Wide Input Voltage Range: 3.4V to 65V**
- **Ultralow Quiescent Current Burst Mode Operation**
  - **2.5µA I_Q Regulating $12V_{IN}$ to $3.3V_{OUT}$ (LT8645S)**
  - **Output Ripple < $10mV_{P-P}$**
- **External Compensation: Fast Transient Response and Current Sharing (LT8646S)**
- Fast Minimum Switch On-Time: 40ns
- Low Dropout Under All Conditions: 60mV at 1A
- Adjustable and Synchronizable: 200kHz to 2.2MHz
- Peak Current Mode Operation
- Output Soft-Start and Tracking
- Small 32-Lead 6mm × 4mm LQFN Package

APPLICATIONS

- Automotive and Industrial Supplies
- General Purpose Step-Down
- GSM Power Supplies

DESCRIPTION

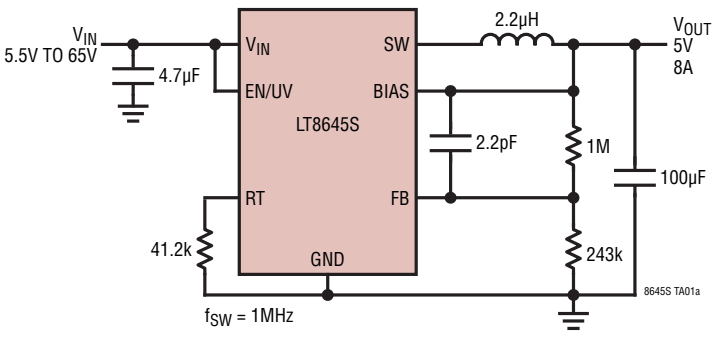
The LT®8645S/LT8646S synchronous step-down regulator features second generation Silent Switcher architecture designed to minimize EMI/EMC emissions while delivering high efficiency at high switching frequencies. This includes the integration of bypass capacitors to optimize all the fast current loops inside and make it easy to achieve advertised EMI performance by eliminating layout sensitivity. This performance makes the LT8645S/LT8646S ideal for noise sensitive applications and environments.

The fast, clean, low-overshoot switching edges enable high efficiency operation even at high switching frequencies, leading to a small overall solution size. Peak current mode control with a 40ns minimum on-time allows high step-down ratios even at high switching frequencies. The LT8646S has external compensation via the V_C pin to enable current sharing and fast transient response at high switching frequencies. A CLKOUT pin enables synchronizing other regulators to the LT8645S/LT8646S.

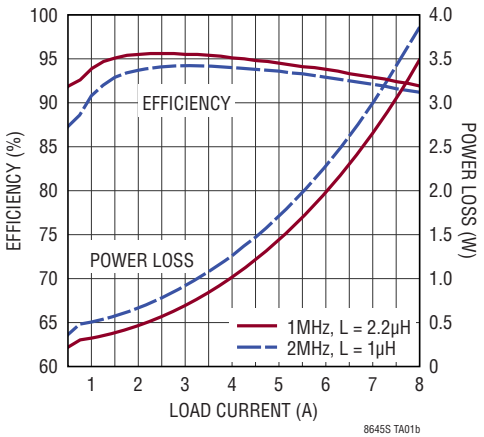
Burst Mode® operation enables ultralow standby current consumption, pulse-skipping mode allows full switching frequency at lower output loads, or spread spectrum operation can further reduce EMI/EMC emissions.

TYPICAL APPLICATION

5V 8A Step-Down Converter



$12V_{IN}$ to $5V_{OUT}$ Efficiency



ABSOLUTE MAXIMUM RATINGS

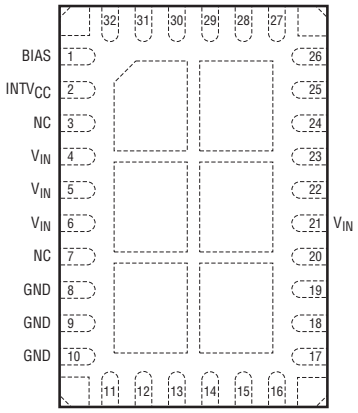
(Note 1)

V_{IN}, EN/UV 65V
PG.....42V
BIAS.....25V
FB, TR/SS 4V
SYNC/MODE Voltage 6V

PIN CONFIGURATION

LT8645S

TOP VIEW



LQFN PACKAGE
32-LEAD (6mm × 4mm × 0.94mm)

LT8646S

ORDER INFORMATION

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C.

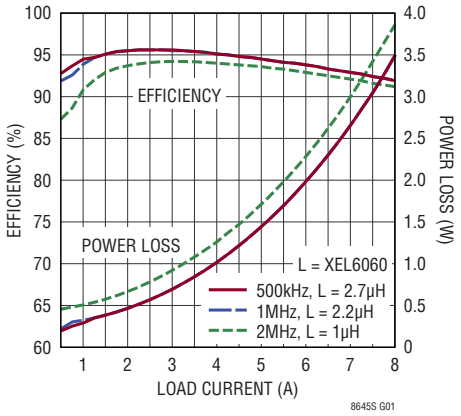
PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum Input Voltage		●		3.0	3.4	V
V_{IN} Quiescent Current in Shutdown	$V_{EN/UV}$ = 0V	 ●		0.9 0.9	3 10	µA µA
LT8645S V_{IN} Quiescent Current in Sleep (Internal Compensation)	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V	 ●		1.7 1.7	4 10	µA µA
LT8646S V_{IN} Quiescent Current in Sleep (External Compensation)	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V, V_{BIAS} = 0V	 ●		230 230	290 340	µA µA
	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V, V_{BIAS} = 5V			16	25	µA
LT8646S BIAS Quiescent Current in Sleep	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 0V, V_{BIAS} = 5V			200	260	µA
LT8645S V_{IN} Quiescent Current when Active	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 2V, R_T = 60.4k, V_{BIAS} = 0V			0.4	0.6	mA
LT8646S V_{IN} Quiescent Current when Active	$V_{EN/UV}$ = 2V, V_{FB} > 0.97V, V_{SYNC} = 2V, R_T = 60.4k, V_{BIAS} = 0V			0.6	0.8	mA
LT8645S V_{IN} Current in Regulation	V_{OUT} = 0.97V, V_{IN} = 6V, I_{LOAD} = 100µA, V_{SYNC} = 0V V_{OUT} = 0.97V, V_{IN} = 6V, I_{LOAD} = 1mA, V_{SYNC} = 0V	● ●		17 200	60 400	µA µA
Feedback Reference Voltage	V_{IN} = 6V V_{IN} = 6V	 ●	0.964 0.958	0.970 0.970	0.976 0.982	V V
Feedback Voltage Line Regulation	V_{IN} = 4.0V to 42V	●		0.004	0.025	%/V
Feedback Pin Input Current	V_{FB} = 1V		–20		20	nA
LT8646S Error Amp Transconductance	V_C = 1.25V			1.7		mS
LT8646S Error Amp Gain				350		V/V
LT8646S V_C Source Current	V_{FB} = 0.77V, V_C = 1.25V			350		µA
LT8646S V_C Sink Current	V_{FB} = 1.17V, V_C = 1.25V			350		µA
LT8646S V_C Pin to Switch Current Gain				8		A/V
LT8646S V_C Clamp Voltage				2.6		V
BIAS Pin Current Consumption	V_{BIAS} = 3.3V, f_{SW} = 2MHz			22		mA
Minimum On-Time	I_{LOAD} = 2A, SYNC = 0V I_{LOAD} = 2A, SYNC = 2V	● ●		40 35	65 60	ns ns
Minimum Off-Time				80	110	ns
Oscillator Frequency	R_T = 221k R_T = 60.4k R_T = 18.2k	● ● ●	180 665 1.8	210 700 1.95	240 735 2.1	kHz kHz MHz
Top Power NMOS On-Resistance	I_{SW} = 1A			36		mΩ
Top Power NMOS Current Limit		●	10.5	14	17.5	A
Bottom Power NMOS On-Resistance	V_{INTVCC} = 3.4V, I_{SW} = 1A			25		mΩ
Bottom Power NMOS Current Limit	V_{INTVCC} = 3.4V		8.5	11	13.5	A
SW Leakage Current	V_{IN} = 42V, V_{SW} = 0V, 42V		–1.5		1.5	µA
EN/UV Pin Threshold	EN/UV Rising	●	0.95	1.01	1.07	V
EN/UV Pin Hysteresis				45		mV
EN/UV Pin Current	$V_{EN/UV}$ = 2V		–20		20	nA
PG Upper Threshold Offset from V_{FB}	V_{FB} Falling	●	5	7.5	10	%
PG Lower Threshold Offset from V_{FB}	V_{FB} Rising	●	–10.5	–8	–5.5	%

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PG Hysteresis				0.4		%
PG Leakage	V_{PG} = 3.3V		–40		40	nA
PG Pull-Down Resistance	V_{PG} = 0.1V	●		750	2000	Ω
SYNC/MODE Threshold	SYNC/MODE DC and Clock Low Level Voltage SYNC/MODE Clock High Level Voltage SYNC/MODE DC High Level Voltage	● ● ●	0.7 2.2	0.9 1.2 2.55	 1.4 2.9	V V V
Spread Spectrum Modulation Frequency Range	R_T = 60.4k, V_{SYNC} = 3.3V			24		%
Spread Spectrum Modulation Frequency	V_{SYNC} = 3.3V			2.5		kHz
TR/SS Source Current		●	1.2	1.9	2.6	µA
TR/SS Pull-Down Resistance	Fault Condition, TR/SS = 0.1V			220		Ω

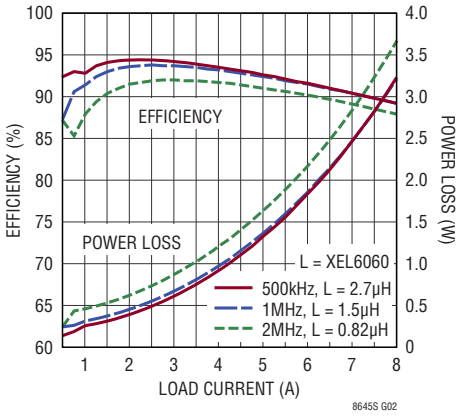
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.**o560.23869ah35t6usk4u1 1 Tf 7.6 0 0 8 419.3942 531.5168 T4 60.22 -2.718 Td 8 41t -19T 8.55 0 NC/MODE DC W22 -2.718 Td 8 41t 8 4y2C may caus 6-2.718 Td 8 41t -15168 T4 60.22 -2.718 s2/ 865617.1025 168 s718 Td 8 41t -d 8 iM42:8-2mk/0a 5617.12aus 6-2.718 Td 8 41t -15168 T4 60.T65**

TYPICAL PERFORMANCE CHARACTERISTICS

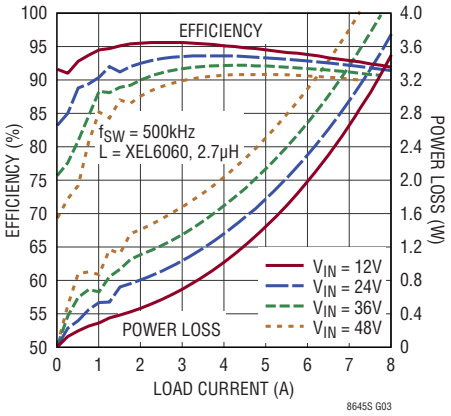
$12V_{IN}$ to $5V_{OUT}$ Efficiency vs Frequency



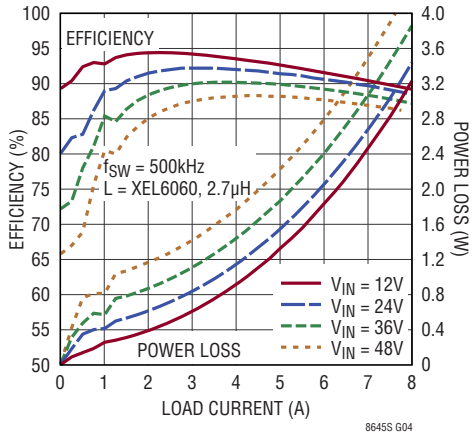
$12V_{IN}$ to $3.3V_{OUT}$ Efficiency vs Frequency



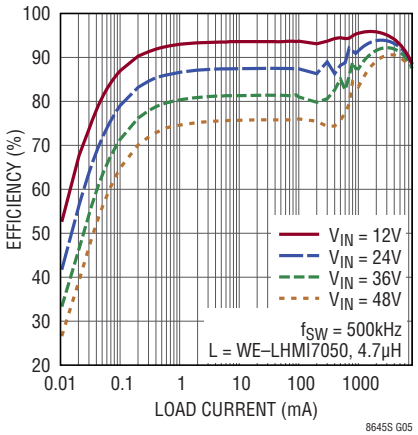
Efficiency at $5V_{OUT}$



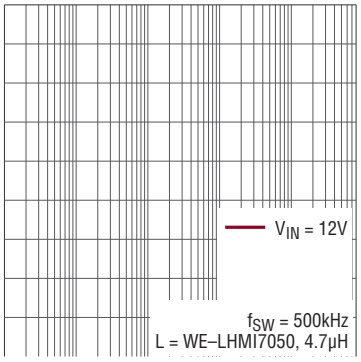
Efficiency at $3.3V_{OUT}$



LT8645S Low Load Efficiency at $5V_{OUT}$



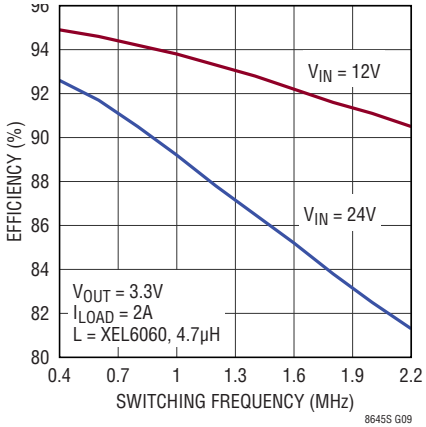
LT8646S Low Load Efficiency at $5V_{OUT}$



LT8645S Low Load Efficiency at $3.3V_{OUT}$

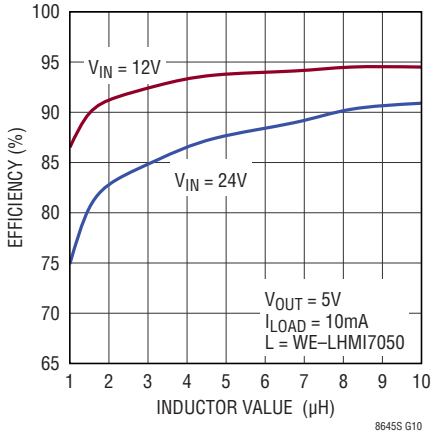
LT8646S Low Load Efficiency at $3.3V_{OUT}$

Efficiency vs Frequency

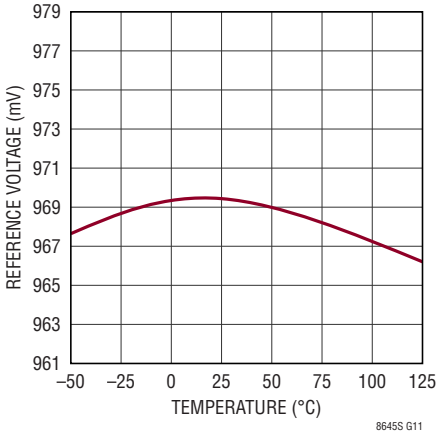


TYPICAL PERFORMANCE CHARACTERISTICS

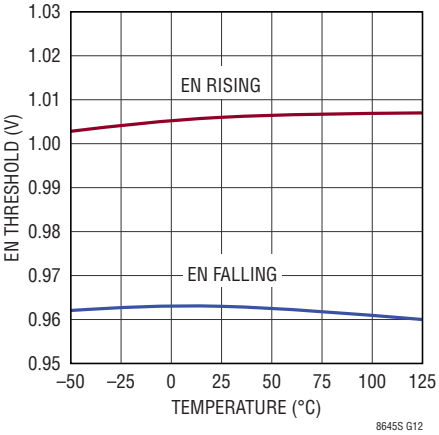
Burst Mode Operation Efficiency vs Inductor Value (LT8645S)



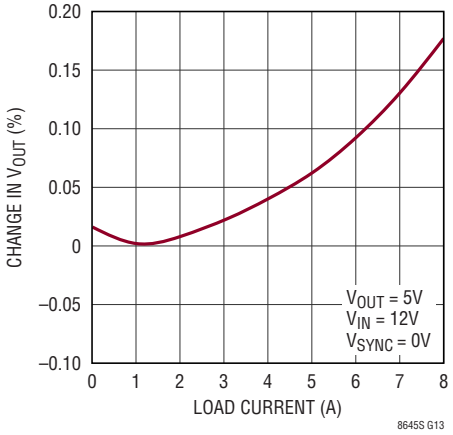
Reference Voltage



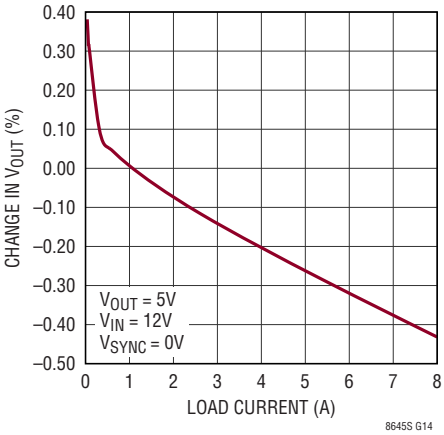
EN Pin Thresholds



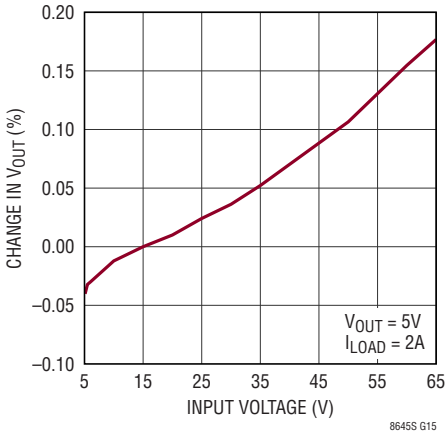
LT8645S Load Regulation



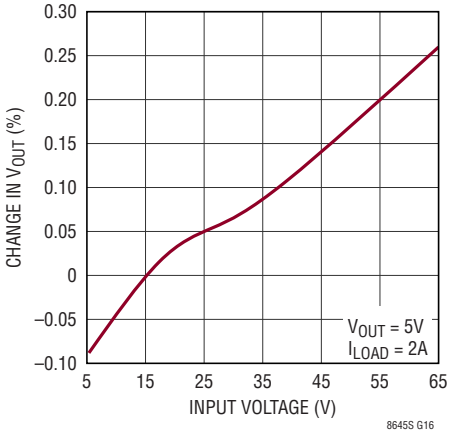
LT8646S Load Regulation



LT8645S Line Regulation

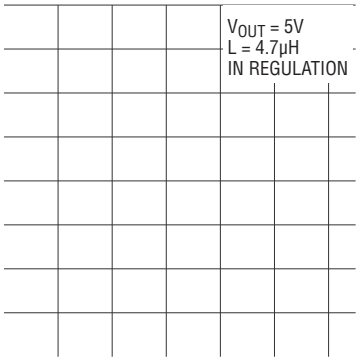


LT8646S Line Regulation



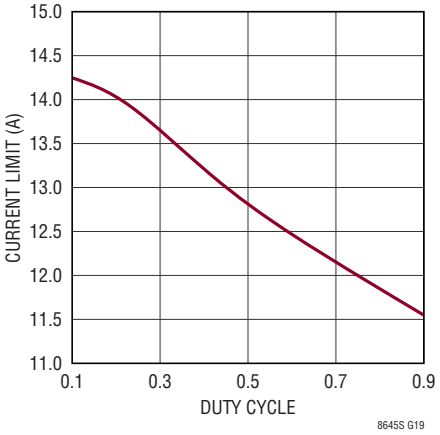
LT8645S No-Load Supply Current

LT8646S No-Load Supply Current

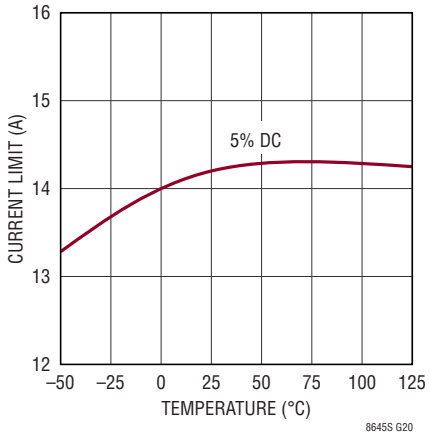


TYPICAL PERFORMANCE CHARACTERISTICS

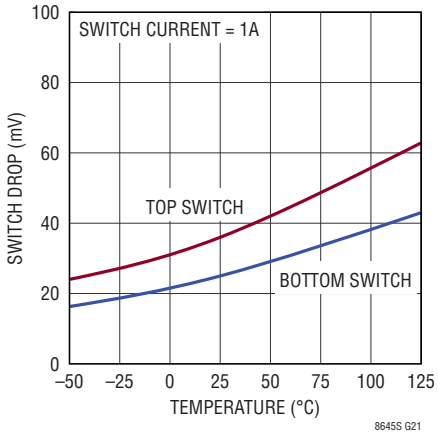
Top FET Current Limit vs Duty Cycle



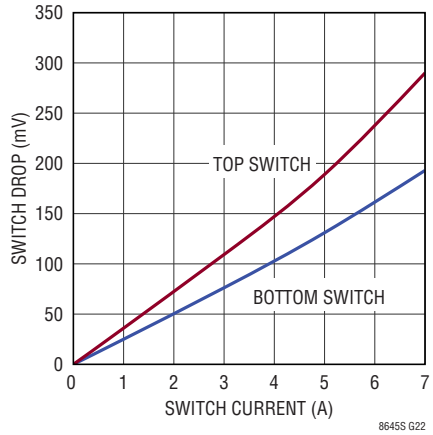
Top FET Current Limit



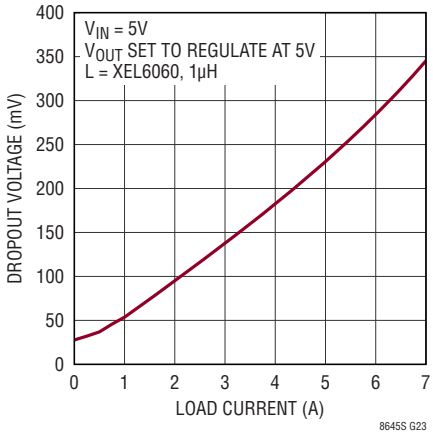
Switch Drop vs Temperature



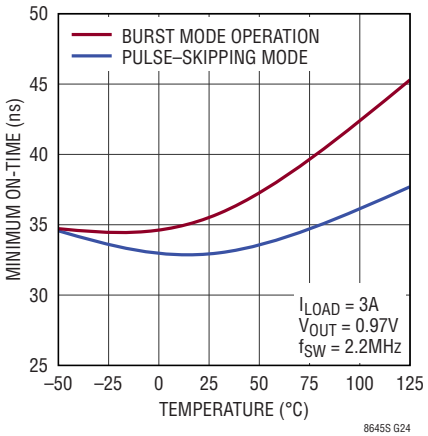
Switch Drop vs Switch Current



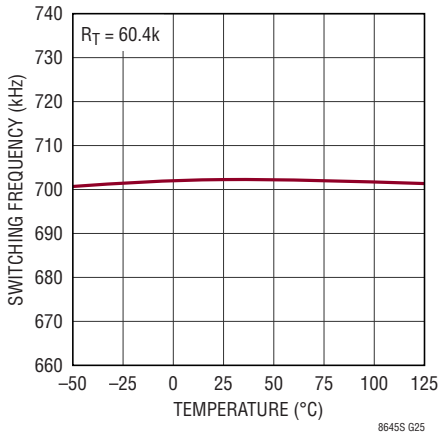
Dropout Voltage



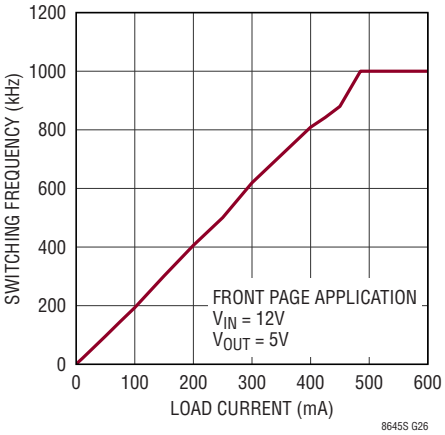
Minimum On-Time



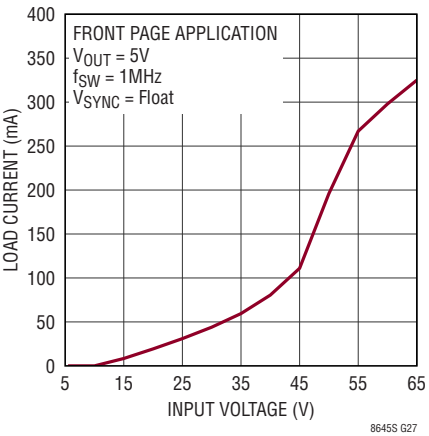
Switching Frequency



Burst Frequency

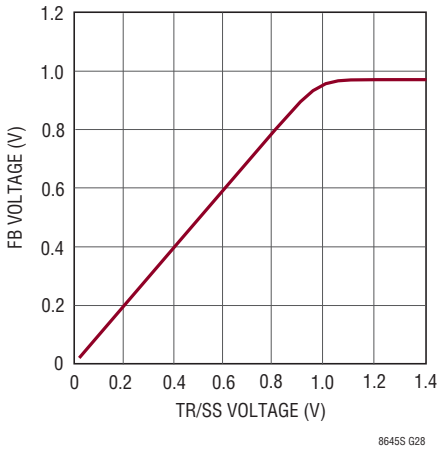


Minimum Load to Full Frequency (Pulse-Skipping Mode)

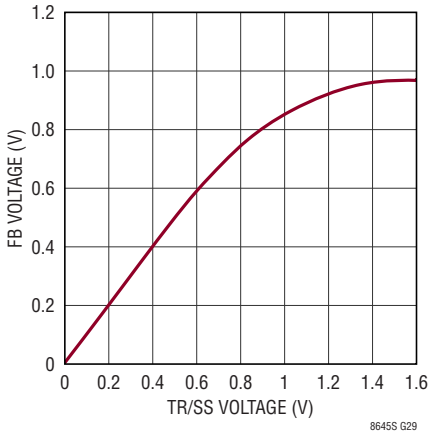


TYPICAL PERFORMANCE CHARACTERISTICS

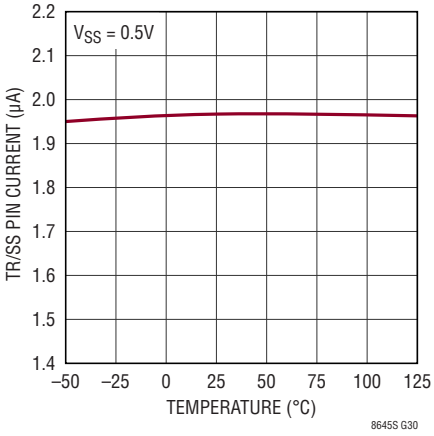
LT8645S Soft-Start Tracking



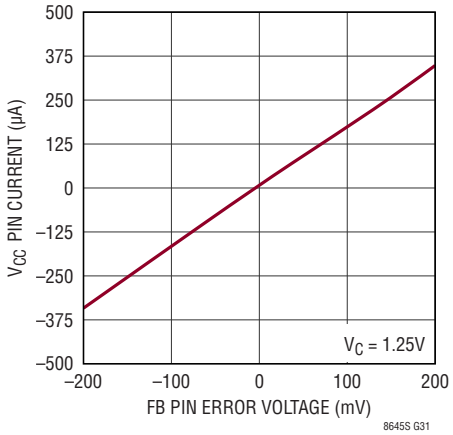
LT8646S Soft-Start Tracking



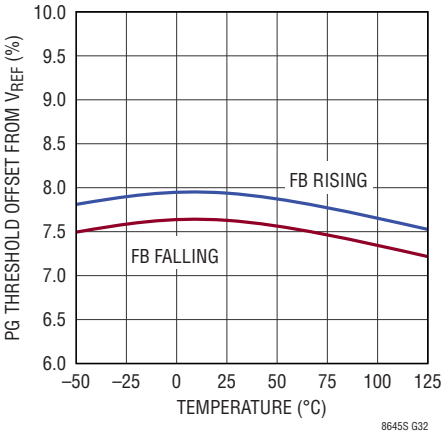
Soft-Start Current



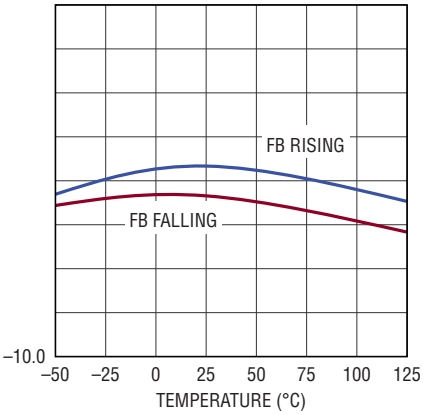
LT8646S Error Amp Output Current



PG High Thresholds



PG Low Thresholds



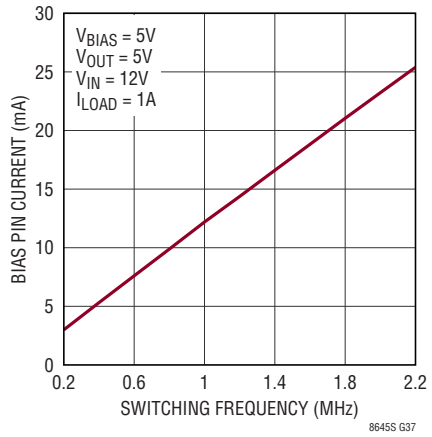
RT Programmed Switching Frequency

Minimum Input Voltage

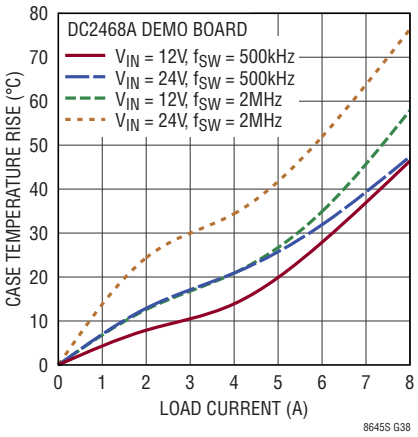
Bias Pin Current

TYPICAL PERFORMANCE CHARACTERISTICS

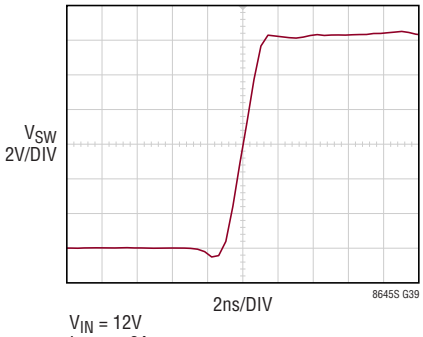
Bias Pin Current



Case Temperature Rise

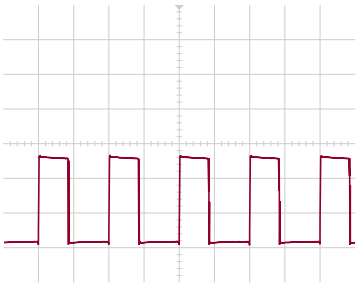


Switch Rising Edge



V_{IN} = 12V
I_{LOAD} = 3A

Switching Waveforms, Full Frequency Continuous Operation

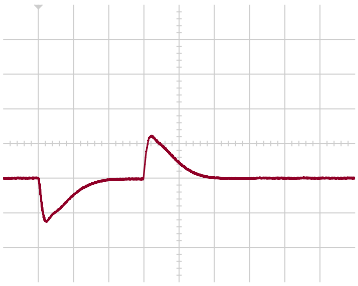


Switching Waveforms, Burst Mode Operation

Switching Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

LT8645S Transient Response; Internal Compensation



LT8646S Transient Response; External Compensation

LT8645S Transient Response; 300mA (Burst Mode Operation) to 1.3A Transient

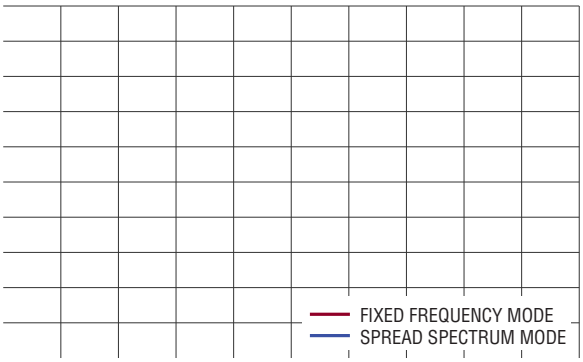
LT8646S Transient Response; 300mA (Burst Mode Operation) to 1.3A Transient

Start-Up Dropout Performance

Start-Up Dropout Performance

TYPICAL PERFORMANCE CHARACTERISTICS

Conducted EMI Performance



DC2468A DEMO BOARD
(WITH EMI FILTER INSTALLED)
14V INPUT TO 5V OUTPUT AT 4A, f_{SW} = 2MHz

Radiated EMI Performance
(CISPR25 Radiated Emission Test with Class 5 Peak Limits)

PIN FUNCTIONS

BIAS (Pin 1): The internal regulator will draw current from BIAS instead of V_{IN} when BIAS is tied to a voltage higher than 3.1V. For output voltages of 3.3V to 25V this pin should be tied to V_{OUT}. If this pin is tied to a supply other than V_{OUT} use a 1µF local bypass capacitor on this pin. If no supply is available, tie to GND. However, especially for high input or high frequency applications, BIAS should be tied to output or an external supply of 3.3V or above.

$INTV_{CC}$ (Pin 2): Internal 3.4V Regulator Bypass Pin. The internal power drivers and control circuits are powered from this voltage. $INTV_{CC}$ maximum output current is 25mA. Do not load the $INTV_{CC}$ pin with external circuitry. $INTV_{CC}$ current will be supplied from BIAS if BIAS > 3.1V, otherwise current will be drawn from V_{IN}. Voltage on $INTV_{CC}$ will vary between 2.8V and 3.4V when BIAS is between 3.0V and 3.6V. This pin should be floated.

NC (Pins 3, 7, 20, 24): No Connect. This pin is not connected to internal circuitry and can be tied anywhere on the PCB, typically ground.

V_{IN} (Pins 4, 5, 6, 21, 22, 23): The V_{IN} pins supply current to the LT8645S/LT8646S internal circuitry and to the internal topside power switch. These pins must be tied together and be locally bypassed with a capacitor of 4.7µF or more. Be sure to place the positive terminal of the input capacitor as close as possible to the V_{IN} pins, and the negative capacitor terminal as close as possible to the GND pins. See the Applications Information section for a sample layout.

GND (Pins 8, 9, 10, 17, 18, 19, Exposed Pad Pins 33–38): Ground. Place the negative terminal of the input capacitor as close to the GND pins as possible. See the Applications Information section for a sample layout. The exposed pads should be soldered to the PCB for good thermal performance. If necessary due to manufacturing limitations Pins 33 to 38 may be left disconnected, however thermal performance will be degraded.

BST (Pin 11): This pin is used to provide a drive voltage, higher than the input voltage, to the topside power switch. This pin should be floated.

SW (Pins 12, 13, 14, 15, 16): The SW pins are the outputs of the internal power switches. Tie these pins together and connect them to the inductor and boost capacitor. This node should be kept small on the PCB for good performance and low EMI.

EN/UV (Pin 25): The LT8645S/LT8646S is shut down when this pin is low and active when this pin is high. The hysteretic threshold voltage is 1.00V going up and 0.96V going down. Tie to V_{IN} if the shutdown feature is not used. An external resistor divider from V_{IN} can be used to program a V_{IN} threshold below which the LT8645S/LT8646S will shut down.

RT (Pin 26): A resistor is tied between RT and ground to set the switching frequency.

CLKOUT (Pin 27): In pulse-skipping mode, spread spectrum, and synchronization modes, the CLKOUT pin will provide a ~200ns wide pulse at the switch frequency. The low and high levels of the CLKOUT pin are ground and $INTV_{CC}$ respectively, and the drive strength of the CLKOUT pin is several hundred ohms. In Burst Mode operation, the CLKOUT pin will be low. Float this pin if the CLKOUT function is not used.

SYNC/MODE (Pin 28): This pin programs four different operating modes: 1) Burst Mode. Tie this pin to ground for Burst Mode operation at low output loads—this will result in ultralow quiescent current. 2) Pulse-skipping mode. This mode offers full frequency operation down to low output loads before pulse skipping occurs. Float this pin for pulse-skipping mode. When floating, pin leakage currents should be <1µA. 3) Spread spectrum mode. Tie this pin high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V for pulse-skipping mode with spread spectrum modulation. 4) Synchronization mode. Drive this pin with a clock source to synchronize to an external frequency. During synchronization the part will operate in pulse-skipping mode.

PIN FUNCTIONS

TR/SS (Pin 29): Output Tracking and Soft-Start Pin. This pin allows user control of output voltage ramp rate during start-up. For the LT8645S, a TR/SS voltage below 0.97V forces it to regulate the FB pin to equal the TR/SS pin voltage. When TR/SS is above 0.97V, the tracking function is disabled and the internal reference resumes control of the error amplifier. For the LT8646S, a TR/SS voltage below 1.6V forces it to regulate the FB pin to a function of the TR/SS pin voltage. See plot in the Typical Performance Characteristics section. When TR/SS is above 1.6V, the tracking function is disabled and the internal reference resumes control of the error amplifier. An internal 1.9µA pull-up current from $INTV_{CC}$ on this pin allows a capacitor to program output voltage slew rate. This pin is pulled to ground with an internal 200Ω MOSFET during shutdown and fault conditions; use a series resistor if driving from a low impedance output. This pin may be left floating if the tracking function is not needed.

GND (Pin 30 LT8645S Only): Ground. Connect this pin to system ground and to the ground plane. This pin is also connected to ground internally, and can be left floating on PCB to be pin compatible with the LT8646S.

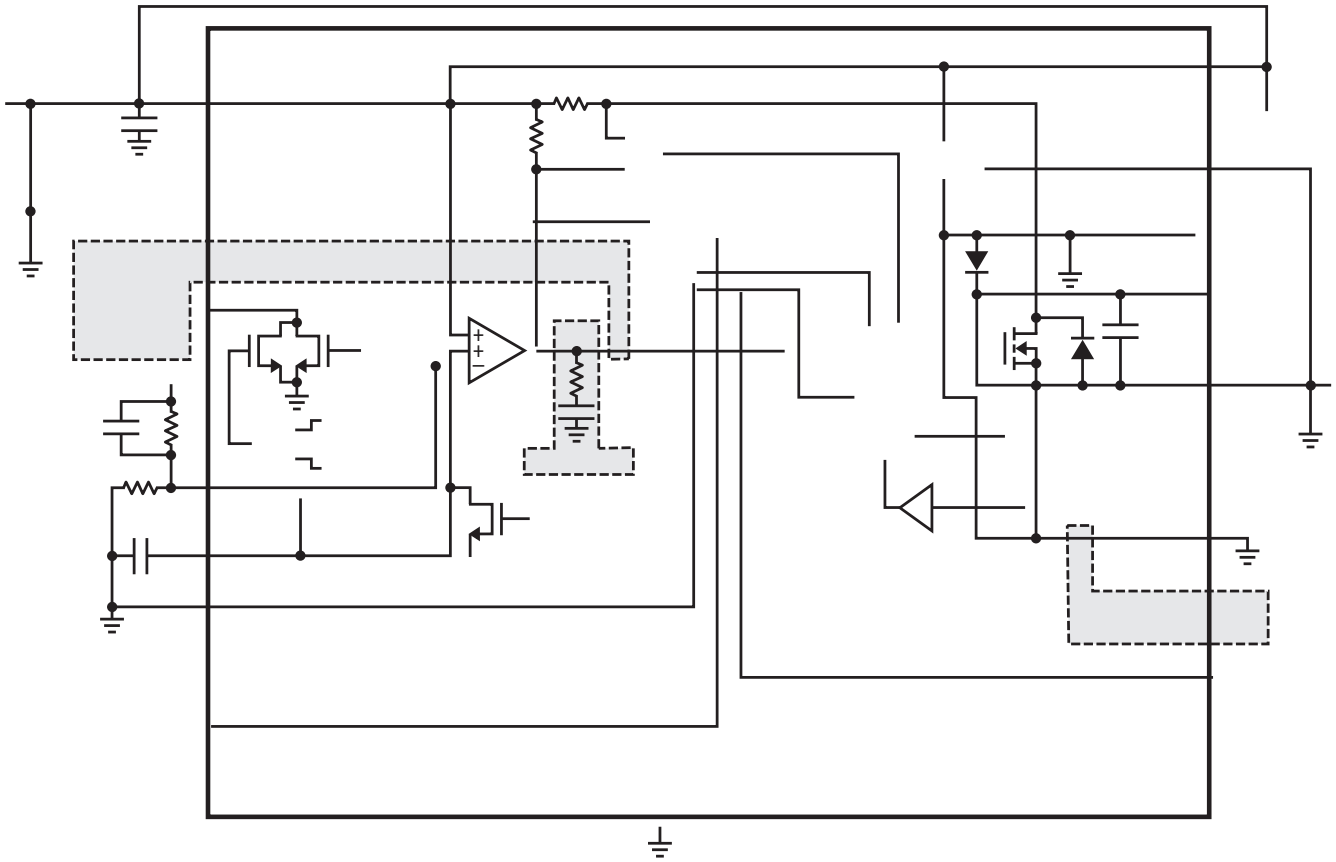
V_C (Pin 30, LT8646S Only): The VC pin is the output of the internal error amplifier. The voltage on this pin controls the peak switch current. Tie an R_C network from this pin to ground to compensate the control loop.

PG (Pin 31): The PG pin is the open-drain output of an internal comparator. PG remains low until the FB pin is within ±8% of the final regulation voltage, and there are no fault conditions. PG is pulled low when EN/UV is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown. PG is valid when V_{IN} is above 3.4V.

FB (Pin 32): The LT8645S/LT8646S regulates the FB pin to 0.97V. Connect the feedback resistor divider tap to this pin. Also, connect a phase lead capacitor between FB and V_{OUT}. Typically, this capacitor is 1pF to 10pF.

Corner Pins: These pins are for mechanical support only and can be tied anywhere on the PCB, typically ground.

BLOCK DIAGRAM



OPERATION

The LT8645S/LT8646S is a monolithic, constant frequency, current mode step-down DC/DC converter. An oscillator, with frequency set using a resistor on the RT pin, turns on the internal top power switch at the beginning of each clock cycle. Current in the inductor then increases until the top switch current comparator trips and turns off the top power switch. The peak inductor current at which the top switch turns off is controlled by the voltage on the internal VC node. The error amplifier servos the VC node by comparing the voltage on the V_{FB} pin with an internal 0.97V reference. When the load current increases it causes a reduction in the feedback voltage relative to the reference leading the error amplifier to raise the VC voltage until the average inductor current matches the new load current. When the top power switch turns off, the synchronous power switch turns on until the next clock cycle begins or inductor current falls to zero. If overload conditions result in more than 11A flowing through the bottom switch, the next clock cycle will be delayed until switch current returns to a safe level.

The "S" in LT8645S/LT8646S refers to the second generation Silent Switcher technology. This technology allows fast switching edges for high efficiency at high switching frequencies, while simultaneously achieving good EMI/EMC performance. This includes the integration of ceramic capacitors into the package for V_{IN}, BST, and $INTV_{CC}$ (see Block Diagram). These caps keep all the fast AC current loops small, which improves EMI/EMC performance.

If the EN/UV pin is low, the LT8645S/LT8646S is shut down and draws approximately 1µA from the input. When the EN/UV pin is above 1V, the switching regulator will become active.

To optimize efficiency at light loads, the LT8645S/LT8646S operates in Burst Mode operation in light load situations. Between bursts, all circuitry associated with controlling the output switch is shut down, reducing the input supply current to 1.7µA (LT8645S) or 230µA (LT8646S with BIAS = 0). In a typical application, 2.5µA (LT8645S) or 120µA (LT8646S with BIAS = $5V_{OUT}$) will be consumed from the input supply when regulating with no load. The SYNC/MODE pin is tied low to use Burst Mode operation and can be floated to use pulse-skipping mode. If a clock is applied to the SYNC/MODE pin, the part will synchronize to an external clock frequency and operate in pulse-skipping mode. While in pulse-skipping mode the oscillator operates continuously and positive SW transitions are aligned to the clock. During light loads, switch pulses are skipped to regulate the output and the quiescent current will be several hundred µA.

To improve EMI/EMC, the LT8645S/LT8646S can operate in spread spectrum mode. This feature varies the clock with a triangular frequency modulation of +20%. For example, if the LT8645S/LT8646S's frequency is programmed to switch at 2MHz, spread spectrum mode will modulate the oscillator between 2MHz and 2.4MHz. The SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V to enable spread spectrum modulation with pulse-skipping mode.

To improve efficiency across all loads, supply current to internal circuitry can be sourced from the BIAS pin when biased at 3.3V or above. Else, the internal circuitry will draw current from V_{IN}. The BIAS pin should be connected to V_{OUT} if the LT8645S/LT8646S output is programmed at 3.3V to 25V.

The V_C pin optimizes the loop compensation of the switching regulator based on the programmed switching frequency, allowing for a fast transient response. The V_C pin also enables current sharing and a CLKOUT pin enables synchronizing other regulators to the LT8646S.

Comparators monitoring the FB pin voltage will pull the PG pin low if the output voltage varies more than ±8% (typical) from the set point, or if a fault condition is present.

The oscillator reduces the LT8645S/LT8646S's operating frequency when the voltage at the FB pin is low. This frequency foldback helps to control the inductor current when the output voltage is lower than the programmed value which occurs during start-up or overcurrent conditions. When a clock is applied to the SYNC/MODE pin, the SYNC/MODE pin is floated, or held DC high, the frequency foldback is disabled and the switching frequency will slow down only during overcurrent conditions.

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Low EMI PCB Layout

The LT8645S/LT8646S is specifically designed to minimize EMI/EMC emissions and also to maximize efficiency when switching at high frequencies. For optimal performance the LT8645S/LT8646S should use multiple V_{IN} bypass capacitors.

Two small 0.47µF capacitors can be placed as close as possible to the LT8645S/LT8646S: One capacitor on each side of the device (C_{OPT1}, C_{OPT2}). A third capacitor with a larger value, 4.7µF or higher, should be placed near C_{OPT1} or C_{OPT2}.

See Figure 1 for a recommended PCB layouts.

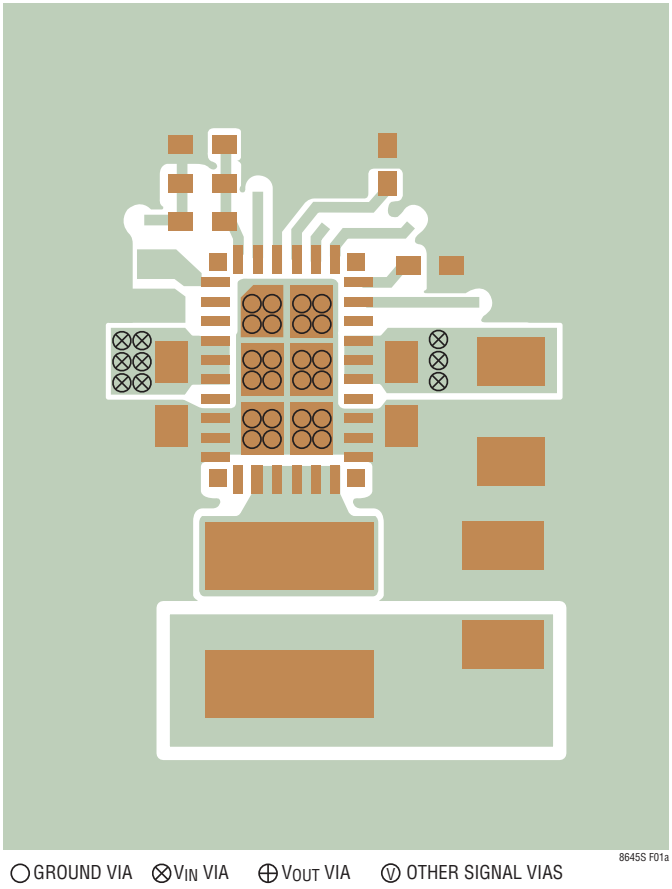

Figure 1. Recommended PCB Layouts for the LT8645S and LT8646S

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For more detail and PCB design files refer to the Demo Board guide for the LT8645S/LT8646S.

Note that large, switched currents flow in the LT8645S/LT8646S V_{IN} and GND pins and the input capacitors. The loops formed by the input capacitors should be as small as possible by placing the capacitors adjacent to the V_{IN} and GND pins. Capacitors with small case size such as 0603 or 0805 are optimal due to lowest parasitic inductance.

The input capacitors, along with the inductor and output capacitors, should be placed on the same side of the circuit board, and their connections should be made on that layer. Place a local, unbroken ground plane under the application circuit on the layer closest to the surface layer. The SW and BOOST nodes should be as small as possible.

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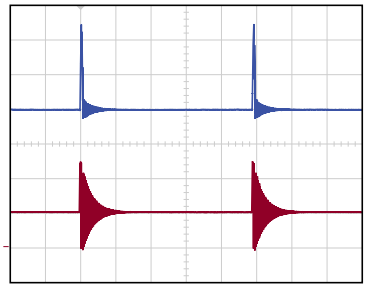
loads, the current in the feedback resistor divider must be minimized as it appears to the output as load current.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8645S/LT8646S can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

While in Burst Mode operation the current limit of the top switch is approximately 1.25A (as shown in Figure 3), resulting in low output voltage ripple. Increasing the output capacitance will decrease output ripple proportionally. As load ramps upward from zero the switching frequency will increase but only up to the switching frequency programmed by the resistor at the RT pin as shown in Figure 2a.

Switching Waveforms, Burst Mode Operation



FRONT PAGE APPLICATION
$12V_{IN}$ TO $5V_{OUT}$ AT 10mA
V_{SYNC} = 0V

Figure 3. Burst Mode Operation

The output load at which the LT8645S/LT8646S reaches the programmed frequency varies based on input voltage, output voltage, and inductor choice. To select low ripple Burst Mode operation, tie the SYNC/MODE pin below 0.4V (this can be ground or a logic low output).

Pulse-Skipping Mode

For some applications it is desirable for the LT8645S/LT8646S to operate in pulse-skipping mode, offering two major differences from Burst Mode operation. First is the clock stays awake at all times and all switching cycles are aligned to the clock. In this mode much of the internal circuitry is awake at all times, increasing quiescent current to several hundred µA. Second is that full switching frequency is reached at lower output load than in Burst Mode operation (see Figure 2b). To enable pulse-skipping mode, float the SYNC/MODE pin. Leakage current in this pin should be <1µA. See Block Diagram for internal pull-up and pull-down resistance.

Spread Spectrum Mode

The LT8645S/LT8646S features spread spectrum operation to further reduce EMI/EMC emissions. To enable spread spectrum operation, the SYNC/MODE pin should be tied high to $INTV_{CC}$ (~3.4V) or an external supply of 3V to 4V. In this mode, triangular frequency modulation is used to vary the switching frequency between the value programmed by RT to approximately 20% higher than that value. The modulation frequency is approximately 3kHz. For example, when the LT8645S/LT8646S is programmed to 2MHz, the frequency will vary from 2MHz to 2.4MHz at

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a 3kHz rate. When spread spectrum operation is selected, Burst Mode operation is disabled, and the part will run in pulse-skipping mode.

Synchronization

To synchronize the LT8645S/LT8646S oscillator to an external frequency, connect a square wave to the SYNC/MODE pin. The square wave amplitude should have valleys that are below 0.4V and peaks above 1.5V (up to 6V), with a minimum on-time and off-time of 50ns.

The LT8645S/LT8646S will not enter Burst Mode operation at low output loads while synchronized to an external clock, but instead will pulse-skip to maintain regulation. The LT8645S/LT8646S may be synchronized over a 200kHz to 2.2MHz range. The RT resistor should be chosen to set the LT8645S/LT8646S switching frequency equal to or below the lowest synchronization input. For example, if the synchronization signal will be 500kHz and higher, the RT should be selected for 500kHz. The slope compensation is set by the RT value, while the minimum slope compensation required to avoid subharmonic oscillations is established by the inductor size, input voltage, and output voltage. Since the synchronization frequency will not change the slopes of the inductor current waveform, if the inductor is large enough to avoid subharmonic oscillations at the frequency set by RT, then the slope compensation will be sufficient for all synchronization frequencies.

The LT8645S/LT8646S does not operate in forced continuous mode regardless of SYNC/MODE signal.

FB Resistor Network

The output voltage is programmed with a resistor divider between the output and the FB pin. Choose the resistor values according to:

$$R1 = R2\left(\frac{V_{OUT}}{0.97V} - 1\right) \quad (1)$$

Reference designators refer to the Block Diagram. 1% resistors are recommended to maintain output voltage accuracy.

For the LT8645S, if low input quiescent current and good light-load efficiency are desired, use large resistor values for the FB resistor divider. The current flowing in the divider acts as a load current, and will increase the no-load input current to the converter, which is approximately:

$$I_Q = 1.7\mu A + \left(\frac{V_{OUT}}{R1+R2}\right)\left(\frac{V_{OUT}}{V_{IN}}\right)\left(\frac{1}{n}\right) \quad (2)$$

where 1.7µA is the quiescent current of the LT8645S and the second term is the current in the feedback divider reflected to the input of the buck operating at its light load efficiency n. For a 3.3V application with R1 = 1M and R2 = 412k, the feedback divider draws 2.3µA. With V_{IN} = 12V and n = 80%, this adds 0.8µA to the 1.7µA quiescent current resulting in 2.5µA no-load current from the 12V supply. Note that this equation implies that the no-load current is a function of V_{IN}; this is plotted in the Typical Performance Characteristics section.

When using large FB resistors, a 1pF to 10pF phase-lead capacitor should be connected from V_{OUT} to FB.

Setting the Switching Frequency

The LT8645S/LT8646S uses a constant frequency PWM architecture that can be programmed to switch from 200kHz to 2.2MHz by using a resistor tied from the RT pin to ground. A table showing the necessary R_T value for a desired switching frequency is in Table 1.

The R_T resistor required for a desired switching frequency can be calculated using:

$$R_T = \frac{46.5}{f_{SW}} - 5.2 \quad (3)$$

where R_T is in kΩ and f_{SW} is the desired switching frequency in MHz.

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Table 1. SW Frequency vs R_T Value

f_{SW} (MHz)	R_T (kΩ)
0.2	232
0.3	150
0.4	110
0.5	88.7
0.6	71.5
0.7	60.4
0.8	52.3
1.0	41.2
1.2	33.2
1.4	28.0
1.6	23.7
1.8	20.5
2.0	17.8
2.2	15.8

Operating Frequency Selection and Trade-Offs

Selection of the operating frequency is a trade-off between efficiency, component size, and input voltage range. The advantage of high frequency operation is that smaller inductor and capacitor values may be used. The disadvantages are lower efficiency and a smaller input voltage range.

The highest switching frequency ($f_{SW(MAX)}$) for a given application can be calculated as follows:

$$f_{SW(MAX)} = \frac{V_{OUT} + V_{SW(BOT)}}{t_{ON(MIN)}\left(V_{IN} - V_{SW(TOP)} + V_{SW(BOT)}\right)} \quad (4)$$

where V_{IN} is the typical input voltage, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.2V, respectively at maximum load) and $t_{ON(MIN)}$ is the minimum top switch on-time (see the Electrical Characteristics). This equation shows that a slower switching frequency is necessary to accommodate a high V_{IN}/V_{OUT} ratio.

For transient operation, V_{IN} may go as high as the absolute maximum rating of 65V regardless of the R_T value, however the LT8645S/LT8646S will reduce switching frequency as necessary to maintain control of inductor current to assure safe operation.

The LT8645S/LT8646S is capable of a maximum duty cycle of approximately 99%, and the V_{IN}-to-V_{OUT} dropout is limited by the $R_{DS(ON)}$ of the top switch. In this mode the LT8645S/LT8646S skips switch cycles, resulting in a lower switching frequency than programmed by RT.

For applications that cannot allow deviation from the programmed switching frequency at low V_{IN}/V_{OUT} ratios use the following formula to set switching frequency:

$$V_{IN(MIN)} = \frac{V_{OUT} + V_{SW(BOT)}}{1 - f_{SW} \bullet t_{OFF(MIN)}} - V_{SW(BOT)} + V_{SW(TOP)} \quad (5)$$

where $V_{IN(MIN)}$ is the minimum input voltage without skipped cycles, V_{OUT} is the output voltage, $V_{SW(TOP)}$ and $V_{SW(BOT)}$ are the internal switch drops (~0.3V, ~0.2V, respectively at maximum load), f_{SW} is the switching frequency (set by RT), and $t_{OFF(MIN)}$ is the minimum switch off-time. Note that higher switching frequency will increase the minimum input voltage below which cycles will be dropped to achieve higher duty cycle.

Inductor Selection and Maximum Output Current

The LT8645S/LT8646S is designed to minimize solution size by allowing the inductor to be chosen based on the output load requirements of the application. During overload or short-circuit conditions the LT8645S/LT8646S safely tolerates operation with a saturated inductor through the use of a high speed peak-current mode architecture.

A good first choice for the inductor value is:

$$L = \left(\frac{V_{OUT} + V_{SW(BOT)}}{f_{SW}}\right) \bullet 0.4 \quad (6)$$

where f_{SW} is the switching frequency in MHz, V_{OUT} is the output voltage, $V_{SW(BOT)}$ is the bottom switch drop (~0.2V) and L is the inductor value in µH.

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To avoid overheating and poor efficiency, an inductor must be chosen with an RMS current rating that is greater than the maximum expected output load of the application. In addition, the saturation current (typically labeled I_{SAT}) rating of the inductor must be higher than the load current plus 1/2 of in inductor ripple current:

$$I_{L(PEAK)} = I_{LOAD(MAX)} + \frac{1}{2}\Delta I_L \quad (7)$$

where ΔI_L is the inductor ripple current as calculated in Equation 9 and $I_{LOAD(MAX)}$ is the maximum output load for a given application.

As a quick example, an application requiring 2A output should use an inductor with an RMS rating of greater than 2A and an I_{SAT} of greater than 3A. During long duration overload or short-circuit conditions, the inductor RMS rating requirement is greater to avoid overheating of the inductor. To keep the efficiency high, the series resistance (DCR) should be less than 0.02Ω, and the core material should be intended for high frequency applications.

The LT8645S/LT8646S limits the peak switch current in order to protect the switches and the system from overload faults. The top switch current limit (I_{LIM}) is 14A at low duty cycles and decreases linearly to 11.5A at DC = 0.9. The inductor value must then be sufficient to supply the desired maximum output current ($I_{OUT(MAX)}$), which is a function of the switch current limit (I_{LIM}) and the ripple current.

$$I_{OUT(MAX)} = I_{LIM} - \frac{\Delta I_L}{2} \quad (8)$$

The peak-to-peak ripple current in the inductor can be calculated as follows:

$$\Delta I_L = \frac{V_{OUT}}{L \bullet f_{SW}} \bullet \left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right) \quad (9)$$

where f_{SW} is the switching frequency of the LT8645S/LT8646S, and L is the value of the inductor. Therefore, the maximum output current that the LT8645S/LT8646S will deliver depends on the switch current limit, the inductor value, and the input and output voltages. The inductor value may have to be increased if the inductor ripple current does not allow sufficient maximum output current ($I_{OUT(MAX)}$) given the switching frequency, and maximum input voltage used in the desired application.

When operating at high V_{IN} (greater than 40V) and at a frequency and duty cycle that would require a switch on-time of less than 100ns, choose an inductor such that the ΔI_L is greater than 1.5A in order to prevent duty cycle jitter.

In order to achieve higher light load efficiency, more energy must be delivered to the output during the single small pulses in Burst Mode operation such that the LT8645S/LT8646S can stay in sleep mode longer between each pulse. This can be achieved by using a larger value inductor (i.e., 4.7µH), and should be considered independent of switching frequency when choosing an inductor. For example, while a lower inductor value would typically be used for a high switching frequency application, if high light load efficiency is desired, a higher inductor value should be chosen. See curve in Typical Performance Characteristics.

The optimum inductor for a given application may differ from the one indicated by this design guide. A larger value inductor provides a higher maximum load current and reduces the output voltage ripple. For applications requiring smaller load currents, the value of the inductor may be lower and the LT8645S/LT8646S may operate with higher ripple current. This allows use of a physically smaller inductor, or one with a lower DCR resulting in higher efficiency. Be aware that low inductance may result in discontinuous mode operation, which further reduces maximum load current.

For more information about maximum output current and discontinuous operation, see Analog Devices' Application Note 44.

Finally, for duty cycles greater than 50% ($V_{OUT}/V_{IN} > 0.5$), a minimum inductance is required to avoid sub-harmonic oscillation. See Application Note 19.

Input Capacitors

The V_{IN} of the LT8645S/LT8646S should be bypassed with at least three ceramic capacitors for best performance. Two small ceramic capacitors of 0.47µF can be placed close to the part; one on each side of the device (C_{OPT1}, C_{OPT2}). These capacitors should be 0603 or 0805 in size. For automotive applications requiring 2 series

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from the source, so source current increases as source voltage drops. This looks like a negative resistance load to the source and can cause the source to current limit or latch low under low source voltage conditions. The $V_{IN(EN)}$ threshold prevents the regulator from operating at source voltages where the problems might occur. This threshold can be adjusted by setting the values R3 and R4 such that they satisfy the following equation:

$$V_{IN(EN)} = \left(\frac{R3}{R4} + 1\right) \bullet 1.01V \quad (10)$$

where the LT8645S/LT8646S will remain off until V_{IN} is above $V_{IN(EN)}$. Due to the comparator's hysteresis, switching will not stop until the input falls slightly below $V_{IN(EN)}$.

When operating in Burst Mode operation for light load currents, the current through the $V_{IN(EN)}$ resistor network can easily be greater than the supply current consumed by the LT8645S/LT8646S. Therefore, the $V_{IN(EN)}$ resistors should be large to minimize their effect on efficiency at low loads.

$INTV_{CC}$ Regulator

An internal low dropout (LDO) regulator produces the 3.4V supply from V_{IN} that powers the drivers and the internal bias circuitry. The $INTV_{CC}$ can supply enough current for the LT8645S/LT8646S's circuitry. To improve efficiency the internal LDO can also draw current from the BIAS pin when the BIAS pin is at 3.1V or higher. Typically the BIAS pin can be tied to the output of the LT8645S/LT8646S, or can be tied to an external supply of 3.3V or above. If BIAS is connected to a supply other than V_{OUT}, be sure to bypass with a local ceramic capacitor. If the BIAS pin is below 3.0V, the internal LDO will consume current from V_{IN}. Applications with high input voltage and high switching frequency where the internal LDO pulls current from V_{IN} will increase die temperature because of the higher power dissipation across the LDO. Do not connect an external load to the $INTV_{CC}$ pin.

Frequency Compensation (LT8646S Only)

Loop compensation determines the stability and transient performance, and is provided by the components tied to the V_C pin. Generally, a capacitor (C_C) and a resistor (R_C) in series to ground are used. Designing the compensation network is a bit complicated and the best values depend on the application. A practical approach is to start with one of the circuits in this data sheet that is similar to your application and tune the compensation network to optimize the performance. LTspice® simulations can help in this process. Stability should then be checked across all operating conditions, including load current, input voltage and temperature. The LT1375 data sheet contains a more thorough discussion of loop compensation and describes how to test the stability using a transient load.

Figure 4 shows an equivalent circuit for the LT8646S control loop. The error amplifier is a transconductance amplifier with finite output impedance. The power section, consisting of the modulator, power switches, and inductor, is modeled as a transconductance amplifier generating an output current proportional to the voltage at the V_C pin. Note that the output capacitor integrates this current, and that the capacitor on the V_C pin (C_C) integrates the error amplifier output current, resulting in two poles in the loop. A zero is required and comes from a resistor R_C in series with C_C. This simple model works well as long as the value

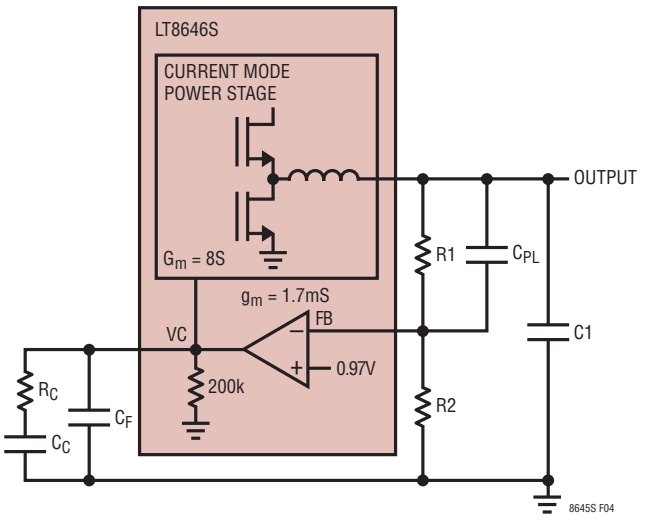

Figure 4. Model for Loop Response

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of the inductor is not too high and the loop crossover frequency is much lower than the switching frequency. A phase lead capacitor (CpI) across the feedback divider can be used to improve the transient response and is required to cancel the parasitic pole caused by the feedback node to ground capacitance.

Output Voltage Tracking and Soft-Start

The LT8645S/LT8646S allows the user to program its output voltage ramp rate by means of the TR/SS pin. An internal 1.9µA pulls up the TR/SS pin to $INTV_{CC}$. Putting an external capacitor on TR/SS enables soft starting the output to prevent current surge on the input supply. During the soft-start ramp the output voltage will proportionally track the TR/SS pin voltage.

For output tracking applications, TR/SS can be externally driven by another voltage source. For the LT8645S, from 0V to 0.97V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to that of TR/SS pin. When TR/SS is above 0.97V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. For the LT8646S, from 0V to 1.6V, the TR/SS voltage will override the internal 0.97V reference input to the error amplifier, thus regulating the FB pin voltage to a function of the TR/SS pin. See plot in the Typical Performance Characteristics section. When TR/SS is above 1.6V, tracking is disabled and the feedback voltage will regulate to the internal reference voltage. The TR/SS pin may be left floating if the function is not needed.

An active pull-down circuit is connected to the TR/SS pin which will discharge the external soft-start capacitor in the case of fault conditions and restart the ramp when the faults are cleared. Fault conditions that clear the soft-start capacitor are the EN/UV pin transitioning low, V_{IN} voltage falling too low, or thermal shutdown.

Output Power Good

When the LT8645S/LT8646S's output voltage is within the ±8% window of the regulation point, the output voltage is considered good and the open-drain PG pin goes high impedance and is typically pulled high with an external resistor. Otherwise, the internal pull-down device will pull the PG pin low. To prevent glitching both the upper and lower thresholds include 0.4% of hysteresis. PG is valid when V_{IN} is above 3.4V

The PG pin is also actively pulled low during several fault conditions: EN/UV pin is below 1V, $INTV_{CC}$ has fallen too low, V_{IN} is too low, or thermal shutdown.

Paralleling (LT8646S Only)

To increase the possible output current, two LT8646Ss can be connected in parallel to the same output. To do this, the V_C and FB pins are connected together, and each LT8646S's SW node is connected to the common output through its own inductor. The CLKOUT pin of one LT8646S should be connected to the SYNC/MODE pin of the second LT8646S to have both devices operate in the same mode. During pulse-skipping, Spread Spectrum, and Synchronization modes, both devices will operate at the same frequency. Figure 5 shows an application where two LT8646S are paralleled to get one output capable of up to 16A.

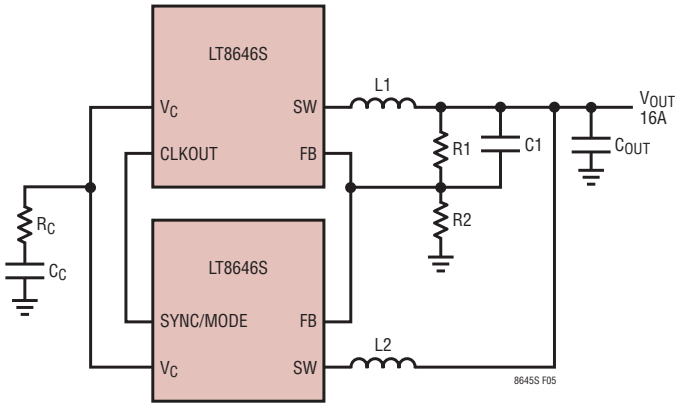

Figure 5. Paralleling Two LT8646S

Shorted and Reversed Input Protection

The LT8645S/LT8646S will tolerate a shorted output. Several features are used for protection during output short-circuit and brownout conditions. The first is the switching frequency will be folded back while the output is lower than the set point to maintain inductor current control. Second, the bottom switch current is monitored such that if inductor current is beyond safe levels switching of the top switch will be delayed until such time as the inductor current falls to safe levels.

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Frequency foldback behavior depends on the state of the SYNC pin: If the SYNC pin is low the switching frequency will slow while the output voltage is lower than the programmed level. If the SYNC pin is connected to a clock source, floated, or tied high, the LT8645S/LT8646S will stay at the programmed frequency without foldback and only slow switching if the inductor current exceeds safe levels.

There is another situation to consider in systems where the output will be held high when the input to the LT8645S/LT8646S is absent. This may occur in battery charging applications or in battery-backup systems where a battery or some other supply is diode ORed with the LT8645S/LT8646S's output. If the V_{IN} pin is allowed to float and the EN pin is held high (either by a logic signal or because it is tied to V_{IN}), then the LT8645S/LT8646S's internal circuitry will pull its quiescent current through its SW pin. This is acceptable if the system can tolerate several µA in this state. If the EN pin is grounded the SW pin current will drop to near 1µA. However, if the V_{IN} pin is grounded while the output is held high, regardless of EN, parasitic body diodes inside the LT8645S/LT8646S can pull current from the output through the SW pin and the V_{IN} pin. Figure 6 shows a connection of the V_{IN} and EN/UV pins that will allow the LT8645S/LT8646S to run only when the input voltage is present and that protects against a shorted or reversed input.

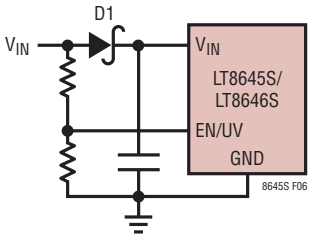

Figure 6. Reverse V_{IN} Protection

Thermal Considerations

For higher ambient temperatures, care should be taken in the layout of the PCB to ensure good heat sinking of the LT8645S/LT8646S. The ground pins on the bottom of the package should be soldered to a ground plane. This ground should be tied to large copper layers below with thermal vias; these layers will spread heat dissipated by the LT8645S/LT8646S. Placing additional vias can reduce thermal resistance further. The maximum load current should be derated as the ambient temperature approaches the maximum junction rating. Power dissipation within the LT8645S/LT8646S can be estimated by calculating the total power loss from an efficiency measurement and subtracting the inductor loss. The die temperature is calculated by multiplying the LT8645S/LT8646S power dissipation by the thermal resistance from junction to ambient.

The internal overtemperature protection monitors the junction temperature of the LT8645S/LT8646S. If the junction temperature reaches approximately 180°C, the LT8645S/LT8646S will stop switching and indicate a fault condition until the temperature drops about 10°C cooler.

Temperature rise of the LT8645S/LT8646S is worst when operating at high load, high V_{IN}, and high switching frequency. If the case temperature is too high for a given application, then either V_{IN}, switching frequency, or load current can be decreased to reduce the temperature to an acceptable level. Figure 7 shows examples of how case temperature rise can be managed by reducing V_{IN}, switching frequency, or load.

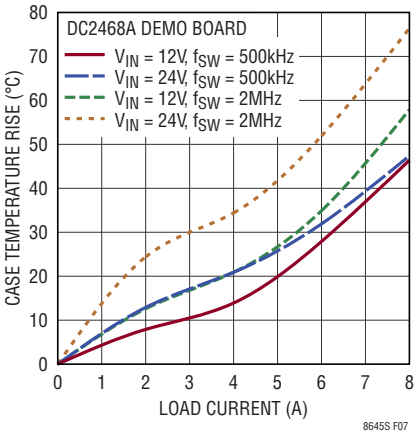

Figure 7. Case Temperature Rise

The LT8645S/LT8646S's top switch current limit decreases with higher duty cycle operation for slope compensation. This also limits the output current the LT8645S/LT8646S can deliver for a given application. See curve in the Typical Performance Characteristics section.