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80V V_{IN} and V_{OUT} Synchronous 4-Switch Buck-Boost DC/DC Controller

FEATURES

- **Single Inductor Allows V_{IN} Above, Below, or Equal to Regulated V_{OUT}**
- **V_{IN} Range 2.8V (Need $EXTV_{CC}$ > 6.4V) to 80V**
- **V_{OUT} Range: 1.3V to 80V**
- **Quad N-Channel MOSFET Gate Drivers**
- **Synchronous Rectification: Up to 98% Efficiency**
- **Input and Output Current Monitor Pins**
- **Synchronizable Fixed Frequency: 100kHz to 400kHz**
- **Integrated Input Current, Input Voltage, Output Current and Output Voltage Feedback Loops**
- Improved Light Load Transition from DCM to FCM
- Improved IMON_OUT, IMON_IN Offset When Cold
- Clock Output Usable To Monitor Die Temperature

APPLICATIONS

- High Voltage Buck-Boost Converters
- Input or Output Current Limited Converters

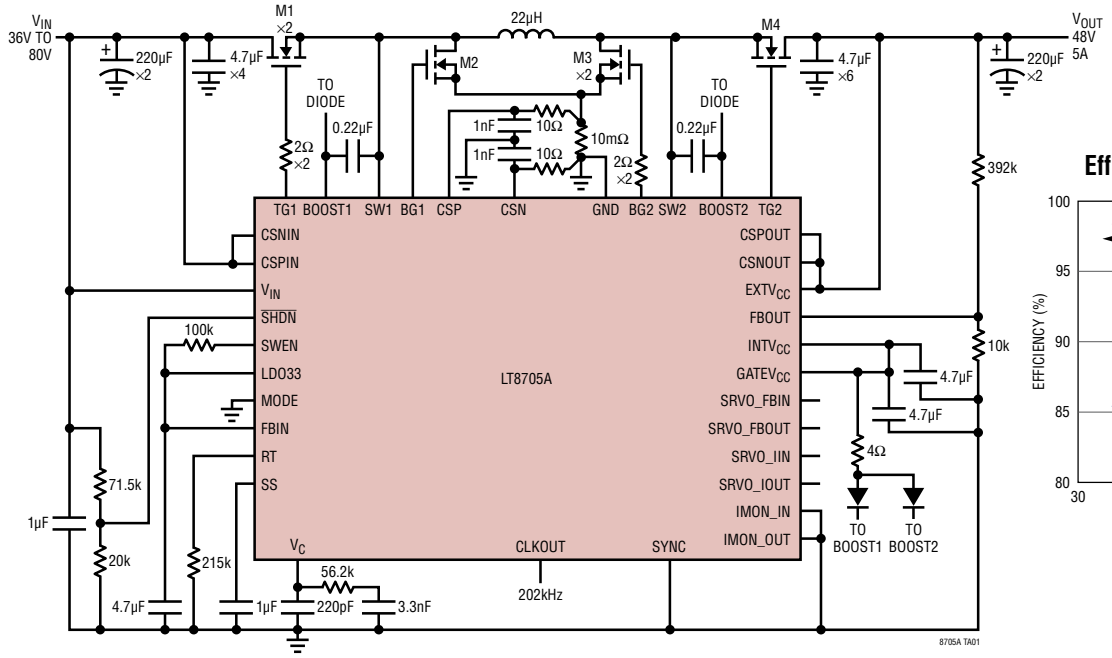
DESCRIPTION

The LT®8705A is a high performance buck-boost switching regulator controller that operates from input voltages above, below or equal to the output voltage. The part has integrated input current, input voltage, output current and output voltage feedback loops. With a wide 2.8V to 80V input and 1.3V to 80V output range, the LT8705A is compatible with most solar, automotive, telecom and battery-powered systems. The LT8705A is an improved pin compatible version of the LT8705 and is recommended for new designs. See LT8705A vs LT8705 in the Applications Information section for more information.

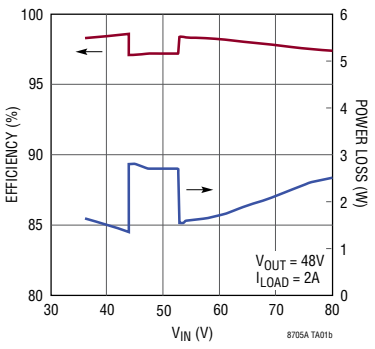
The LT8705A includes a MODE pin to select among Burst Mode® operation, discontinuous or continuous conduction mode at light loads. Additional features include a 3.3V/12mA LDO, a synchronizable fixed operating frequency, and onboard gate drivers.

TYPICAL APPLICATION

Telecom Voltage Stabilizer



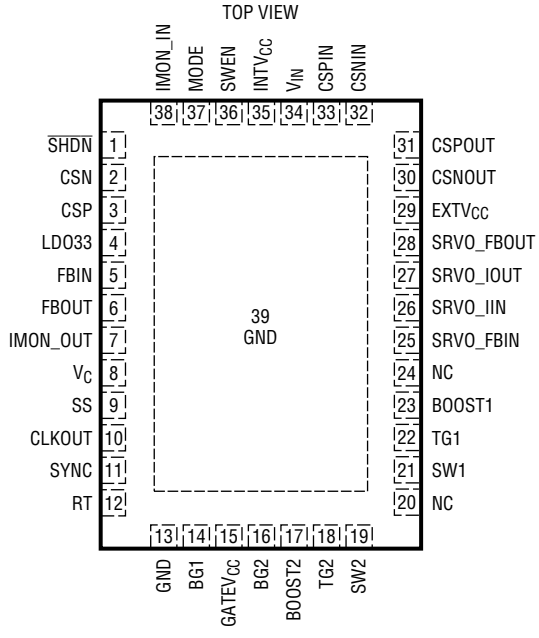
Efficiency and Power Loss



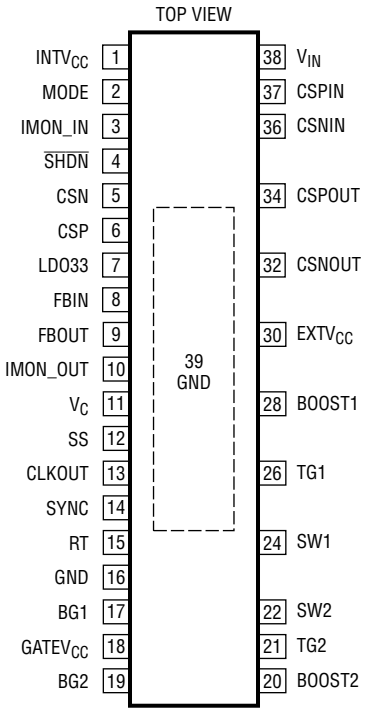
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CSP}-V_{CSN}, V_{CSPIN}-V_{CSNIN}, V_{CSPOUT}-V_{CSNOUT} ..... –0.3V to 0.3V
SS, CLKOUT, CSP, CSN Voltage ..... –0.3V to 3V
V_C Voltage (Note 2) ..... –0.3V to 2.2V
RT, LDO33, FBOUT Voltage ..... –0.3V to 5V
IMON_IN, IMON_OUT Voltage ..... –0.3V to 5V
SYNC Voltage ..... –0.3V to 5.5V
$INTV_{CC}$, $GATEV_{CC}$ Voltage ..... –0.3V to 7V
V_{BOOST1}-V_{SW1}, V_{BOOST2}-V_{SW2} ..... –0.3V to 7V
SWEN, MODE Voltage ..... –0.3V to 7V
SRVO_FBIN, SRVO_FBOUT Voltage ..... –0.3V to 30V
SRVO_IIN, SRVO_IOUT Voltage ..... –0.3V to 30V
FBIN, $\overline{SHDN}$ Voltage ..... –0.3V to 30V
CSNIN, CSPIN, CSPOUT, CSNOUT Voltage .. –0.3V to 80V
V_{IN}, $EXTV_{CC}$ Voltage ..... –0.3V to 80V
SW1, SW2 Voltage ..... 81V (Note 7)
BOOST1, BOOST2 Voltage ..... –0.3V to 87V
BG1, BG2, TG1, TG2 ..... (Note 6)
Operating Junction Temperature Range
LT8705AE (Notes 3, 8) ..... –40°C to 125°C
LT8705AI (Notes 3, 8) ..... –40°C to 125°C
LT8705AH (Notes 3, 8) ..... –40°C to 150°C
LT8705AMP (Notes 3, 8) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package ..... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



FE PACKAGE
VARIATION: FE38(31)
38-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LT8705A#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT8705AEUHF#PBF	LT8705AEUHF#TRPBF	8705A	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT8705AIUHF#PBF	LT8705AIUHF#TRPBF	8705A	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LT8705AEFE#PBF	LT8705AEFE#TRPBF	LT8705AFE	38-Lead Plastic TSSOP	–40°C to 125°C
LT8705AIFE#PBF	LT8705AIFE#TRPBF	LT8705AFE	38-Lead Plastic TSSOP	–40°C to 125°C
LT8705AHFE#PBF	LT8705AHFE#TRPBF	LT8705AFE	38-Lead Plastic TSSOP	–40°C to 150°C
LT8705AMPFE#PBF	LT8705AMPFE#TRPBF	LT8705AFE	38-Lead Plastic TSSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/

For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Voltage Supplies and Regulators						
V_{IN} Operating Voltage Range	$EXTV_{CC}$ = 0V $EXTV_{CC}$ = 7.5V	● ●	5.5 2.8		80 80	V V
V_{IN} Quiescent Current	Not Switching, V_{EXTVCC} = 0			2.65	4.2	mA
V_{IN} Quiescent Current in Shutdown	$V_{\overline{SHDN}}$ = 0V			0	1	µA
$EXTV_{CC}$ Switchover Voltage	I_{INTVCC} = 20mA, V_{EXTVCC} Rising	●	6.15	6.4	6.6	V
$EXTV_{CC}$ Switchover Hysteresis				0.18		V
$INTV_{CC}$ Current Limit	Maximum Current Draw from $INTV_{CC}$ and LDO33 Pins Combined. Regulated from V_{IN} or $EXTV_{CC}$ (12V) $INTV_{CC}$ = 5.25V $INTV_{CC}$ = 4.5V	 ● ●	 90 28	 127 42	 165 55	 mA mA
$INTV_{CC}$ Voltage	Regulated from V_{IN}, I_{INTVCC} = 20mA Regulated from $EXTV_{CC}$ (12V), I_{INTVCC} = 20mA	● ●	6.15 6.15	6.35 6.35	6.55 6.55	V V
$INTV_{CC}$ Load Regulation	I_{INTVCC} = 0mA to 50mA			–0.5	–1.5	%
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling, $GATEV_{CC}$ Connected to $INTV_{CC}$	●	4.45	4.65	4.85	V
$INTV_{CC}$, $GATEV_{CC}$ Undervoltage Lockout Hysteresis	$GATEV_{CC}$ Connected to $INTV_{CC}$			160		mV
$INTV_{CC}$ Regulator Dropout Voltage	V_{IN}-V_{INTVCC}, I_{INTVCC} = 20mA			245		mV
LDO33 Pin Voltage	5mA from LDO33 Pin	●	3.23	3.295	3.35	V
LDO33 Pin Load Regulation	I_{LDO33} = 0.1mA to 5mA			–0.25	–1	%
LDO33 Pin Current Limit		●	12	17.25	22	mA
LDO33 Pin Undervoltage Lockout	LDO33 Falling		2.96	3.04	3.12	V
LDO33 Pin Undervoltage Lockout Hysteresis				35		mV
Switching Regulator Control						
Maximum Current Sense Threshold (V_{CSP} – V_{CSN})	Boost Mode, Minimum M3 Switch Duty Cycle (LT8705AE, LT8705AI) (LT8705AH, LT8705AMP)	 ● ●	 102 100	 117 117	 132 134	 mV mV
Maximum Current Sense Threshold (V_{CSN} – V_{CSP})	Buck Mode, Minimum M2 Switch Duty Cycle (LT8705AE, LT8705AI) (LT8705AH, LT8705AMP)	 ● ●	 69 67	 86 86	 102 104	 mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gain from V_C to Maximum Current Sense Voltage (V_{CSP}-V_{CSN}) (A5 in the Block Diagram)	Boost Mode Buck Mode			150 –150		mV/V mV/V
$\overline{SHDN}$ Input Voltage High	$\overline{SHDN}$ Rising to Enable the Device	●	1.184	1.234	1.284	V
$\overline{SHDN}$ Input Voltage High Hysteresis				50		mV
$\overline{SHDN}$ Input Voltage Low	Device Disabled, Low Quiescent Current (LT8705AE, LT8705AI) (LT8705AH, LT8705AMP)	 ● ●			 0.35 0.3	 V V
$\overline{SHDN}$ Pin Bias Current	$V_{\overline{SHDN}}$ = 3V $V_{\overline{SHDN}}$ = 12V			0 11	1 22	µA µA
SWEN Rising Threshold Voltage (Note 5)		●	1.156	1.206	1.256	V
SWEN Threshold Voltage Hysteresis (Note 5)				22		mV
MODE Pin Forced Continuous Mode Threshold		●	0.4			V
MODE Pin Burst Mode Range		●	1.0		1.7	V
MODE Pin Discontinuous Mode Threshold		●			2.3	V
Soft-Start Charging Current	V_{SS} = 0.5V		13	19	25	µA
Soft-Start Discharge Current	V_{SS} = 0.5V			9.5		µA
Voltage Regulator Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltage for FBOUT	V_C = 1.2V (LT8705AE, LT8705AI) V_C = 1.2V (LT8705AH, LT8705AMP)	● ●	1.193 1.191	1.207 1.207	1.222 1.222	V V
Regulation Voltage for FBIN	V_C = 1.2V (LT8705AE, LT8705AI) V_C = 1.2V (LT8705AH, LT8705AMP)	● ●	1.184 1.182	1.205 1.205	1.226 1.226	V V
Line Regulation for FBOUT and FBIN Error Amp Reference Voltage	V_{IN} = 12V to 80V; Not Switching			0.002	0.005	%/V
FBOUT Pin Bias Current	Current Out of Pin			15		nA
FBOUT Error Amp EA4 g_m				315		µmho
FBOUT Error Amp EA4 Voltage Gain				220		V/V
FBIN Pin Bias Current	Current Out of Pin			10		nA
FBIN Error Amp EA3 g_m				130		µmho
FBIN Error Amp EA3 Voltage Gain				90		V/V
SRVO_FBIN Activation Threshold (Note 5)	(V_{FBIN} Falling) – (Regulation Voltage for FBIN), V_{FBOUT} = V_{IMON_IN} = V_{IMON_OUT} = 0V		56	72	89	mV
SRVO_FBIN Activation Threshold Hysteresis (Note 5)	V_{FBOUT} = V_{IMON_IN} = V_{IMON_OUT} = 0V			33		mV
SRVO_FBOUT Activation Threshold (Note 5)	(V_{FBOUT} Rising) – (Regulation Voltage for FBOUT), V_{FBIN} = 3V, V_{IMON_IN} = V_{IMON_OUT} = 0V		–37	–29	–21	mV
SRVO_FBOUT Activation Threshold Hysteresis (Note 5)	V_{FBIN} = 3V, V_{IMON_IN} = 0V, V_{IMON_OUT} = 0V			15		mV
SRVO_FBIN, SRVO_FBOUT Low Voltage (Note 5)	I = 100µA	●		110	330	mV
SRVO_FBIN, SRVO_FBOUT Leakage Current (Note 5)	V_{SRVO_FBIN} = V_{SRVO_FBOUT} = 2.5V	●		0	1	µA
Current Regulation Loops (Refer to Block Diagram to Locate Amplifiers)						
Regulation Voltages for IMON_IN and IMON_OUT	V_C = 1.2V	●	1.187	1.208	1.229	V
Line Regulation for IMON_IN and IMON_OUT Error Amp Reference Voltage	V_{IN} = 12V to 80V; Not Switching			0.002	0.005	%/V
CSPIN, CSNIN Bias Current	BOOST Capacitor Charge Control Block Not Active I_{CSPIN} + I_{CSNIN}, V_{CSPIN} = V_{CSNIN} = 12V			31		µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 2)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CSPIN, CSNIN Common Mode Operating Voltage Range		●	1.5		80	V
CSPIN, CSNIN Differential Operating Voltage Range		●	–100		100	mV
$V_{CSPIN-CSNIN}$ to IMON_IN Amplifier A7 g_m	$V_{CSPIN} – V_{CSNIN}$ = 50mV, V_{CSPIN} = 5.025V					
	(All Grades)		0.95	1	1.05	mmho
	(LT8705AE, LT8705AI)	●	0.94	1	1.06	mmho
	(LT8705AH, LT8705AMP)	●	0.93	1	1.07	mmho
IMON_IN Maximum Output Current		●	100			µA
IMON_IN Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_IN Error Amp EA2 g_m				185		µmho
IMON_IN Error Amp EA2 Voltage Gain				130		V/V
CSPOUT, CSNOUT Bias Current	BOOST Capacitor Charge Control Block Not Active					
	$I_{CSPOUT} + I_{CSNOUT}$, $V_{CSPOUT} = V_{CSNOUT}$ = 12V			45		µA
	$I_{CSPOUT} + I_{CSNOUT}$, $V_{CSPOUT} = V_{CSNOUT}$ = 1.5V			4		µA
CSPOUT, CSNOUT Common Mode Operating Voltage Range		●	0		80	V
CSPOUT, CSNOUT Differential Mode Operating Voltage Range		●	–100		100	mV
$V_{CSPOUT-CSNOUT}$ to IMON_OUT Amplifier A6 g_m	$V_{CSPOUT} – V_{CSNOUT}$ = 50mV, V_{CSPOUT} = 5.025V					
	(All Grades)		0.95	1	1.05	mmho
	(LT8705AE, LT8705AI)	●	0.94	1	1.085	mmho
	(LT8705AH, LT8705AMP)	●	0.93	1	1.095	mmho
	$V_{CSPOUT} – V_{CSNOUT}$ = 5mV, V_{CSPOUT} = 5.0025V					
	(All Grades)		0.65	1	1.35	mmho
	(LT8705AE, LT8705AI)	●	0.55	1	1.6	mmho
	(LT8705AH, LT8705AMP)	●	0.5	1	1.65	mmho
IMON_OUT Maximum Output Current		●	100			µA
IMON_OUT Overvoltage Threshold		●	1.55	1.61	1.67	V
IMON_OUT Error Amp EA1 g_m				185		µmho
IMON_OUT Error Amp EA1 Voltage Gain				130		V/V
SRVO_IIN Activation Threshold (Note 5)	(V_{IMON_IN} Rising) – (Regulation Voltage for IMON_IN), V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_OUT} = 0V		–60	–49	–37	mV
SRVO_IIN Activation Threshold Hysteresis (Note 5)	V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_OUT} = 0V			22		mV
SRVO_IOUT Activation Threshold (Note 5)	(V_{IMON_OUT} Rising) – (Regulation Voltage for IMON_OUT), V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_IN} = 0V		–62	–51	–39	mV
SRVO_IOUT Activation Threshold Hysteresis (Note 5)	V_{FBIN} = 3V, V_{FBOUT} = 0V, V_{IMON_IN} = 0V			22		mV
SRVO_IIN, SRVO_IOUT Low Voltage (Note 5)	I = 100µA	●		110	330	mV
SRVO_IIN, SRVO_IOUT Leakage Current (Note 5)	$V_{SRVO\_IIN} = V_{SRVO\_IOUT}$ = 2.5V	●		0	1	µA
NMOS Gate Drivers						
TG1, TG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1, TG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Rise Time	C_{LOAD} = 3300pF (Note 4)			20		ns
BG1, BG2 Fall Time	C_{LOAD} = 3300pF (Note 4)			20		ns
TG1 Off to BG1 On Delay	C_{LOAD} = 3300pF Each Driver			100		ns
BG1 Off to TG1 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
TG2 Off to BG2 On Delay	C_{LOAD} = 3300pF Each Driver			100		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, $\overline{SHDN}$ = 3V unless otherwise noted. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
BG2 Off to TG2 On Delay	C_{LOAD} = 3300pF Each Driver			80		ns
Minimum On-Time for Main Switch in Boost Operation ($t_{ON(M3,MIN)}$)	Switch M3, C_{LOAD} = 3300pF			265		ns
Minimum On-Time for Synchronous Switch in Buck Operation ($t_{ON(M2,MIN)}$)	Switch M2, C_{LOAD} = 3300pF			260		ns
Minimum Off-Time for Main Switch in Steady-State Boost Operation	Switch M3, C_{LOAD} = 3300pF			245		ns
Minimum Off-Time for Synchronous Switch in Steady-State Buck Operation	Switch M2, C_{LOAD} = 3300pF			245		ns
Oscillator						
Switch Frequency Range	SYNCing or Free Running		100		400	kHz
Switching Frequency, f_{OSC}	R_T = 365k R_T = 215k R_T = 124K	● ● ●	102 170 310	120 202 350	142 235 400	kHz kHz kHz
SYNC High Level for Synchronization		●	1.3			V
SYNC Low Level for Synchronization		●			0.5	V
SYNC Clock Pulse Duty Cycle	V_{SYNC} = 0V to 2V		20		80	%
Recommended Minimum SYNC Ratio f_{SYNC}/f_{OSC}				3/4		
CLKOUT Output Voltage High	1mA Out of CLKOUT Pin		2.3	2.45	2.55	V
CLKOUT Output Voltage Low	1mA Into CLKOUT Pin			25	100	mV
CLKOUT Duty Cycle	T_J = –40°C T_J = 25°C T_J = 125°C			22.7 44.1 77		% % %
CLKOUT Rise Time	C_{LOAD} = 200pF			30		ns
CLKOUT Fall Time	C_{LOAD} = 200pF			25		ns
CLKOUT Phase Delay	SYNC Rising to CLKOUT Rising, f_{OSC} = 100kHz	●	160	180	200	Deg

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Do not force voltage on the V_C pin.

Note 3: The LT8705AE is guaranteed to meet performance specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LT8705AI is guaranteed over the full –40°C to 125°C junction temperature range. The LT8705AH is guaranteed over the full –40°C to 150°C operating junction temperature range. The LT8705AMP is guaranteed over the full –55°C to 150°C operating junction temperature range. Operating lifetime is derated at junction temperatures greater than 125°C.

Note 4: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 5: This specification not applicable in the FE38 package.

Note 6: Do not apply a voltage or current source to these pins. They must be connected to capacitive loads only, otherwise permanent damage may occur.

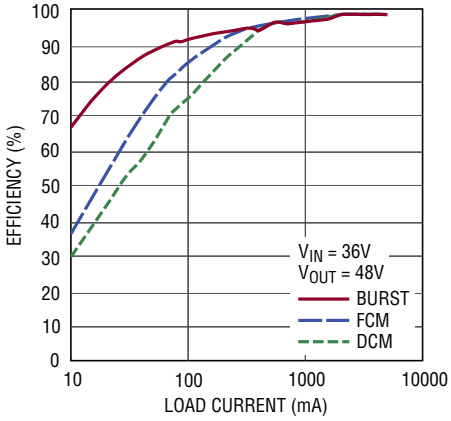
Note 7: Negative voltages on the SW1 and SW2 pins are limited, in an application, by the body diodes of the external NMOS devices, M2 and M3, or parallel Schottky diodes when present. The SW1 and SW2 pins are tolerant of these negative voltages in excess of one diode drop below ground, guaranteed by design.

Note 8: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed the maximum operating junction temperature when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

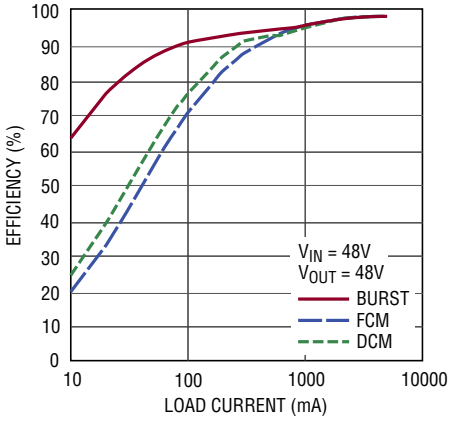
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

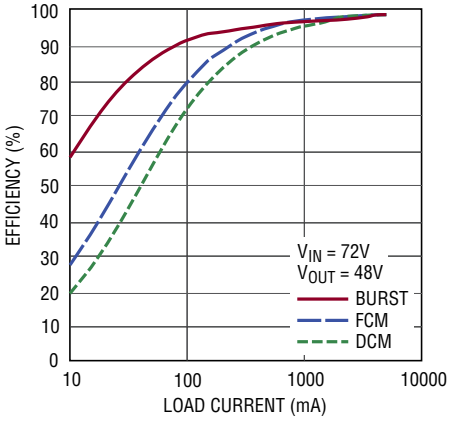
Efficiency vs Output Current (Boost Region-Figure 15)



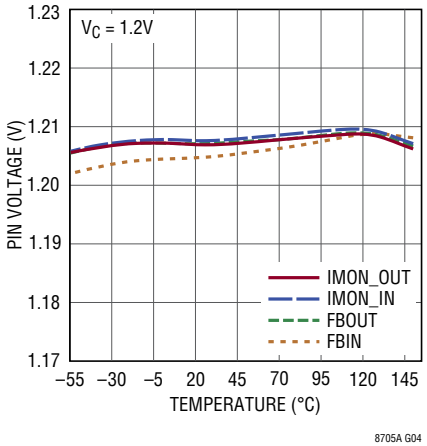
Efficiency vs Output Current (Buck-Boost Region-Figure 15)



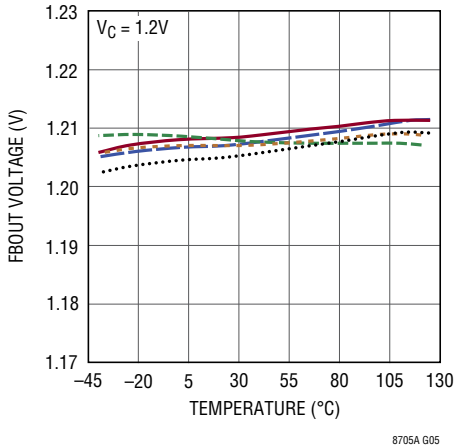
Efficiency vs Output Current (Buck Region-Figure 15)



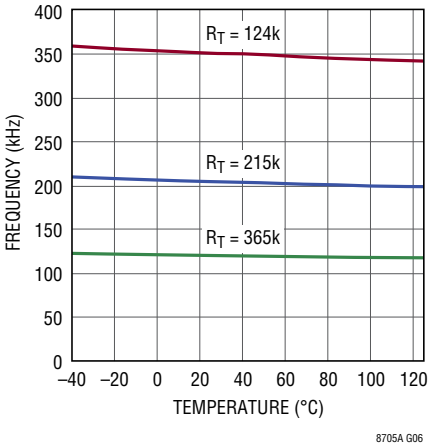
Feedback Voltages



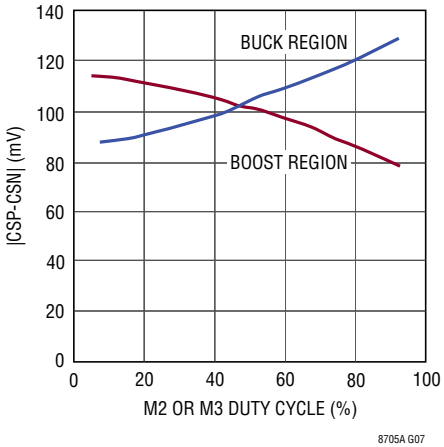
FBOUT Voltages (Five Parts)



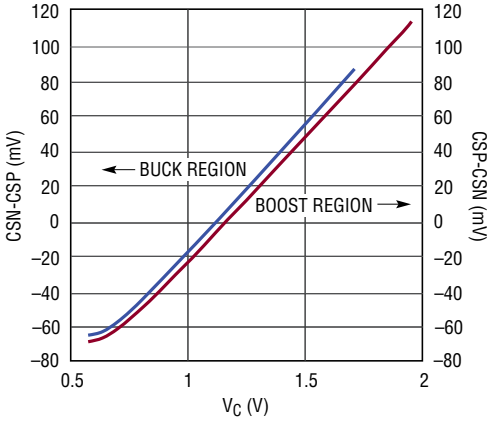
Oscillator Frequency



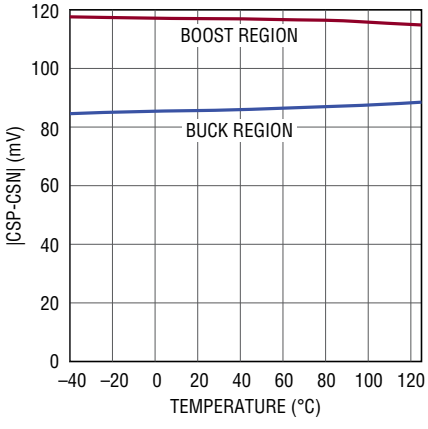
Maximum Inductor Current Sense Voltage vs Duty Cycle



Inductor Current Sense Voltage at Minimum Duty Cycle

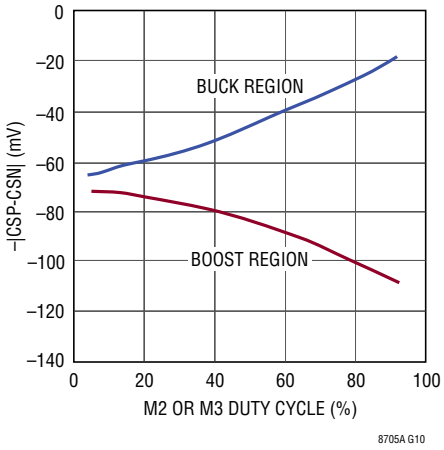


Maximum Inductor Current Sense Voltage at Minimum Duty Cycle

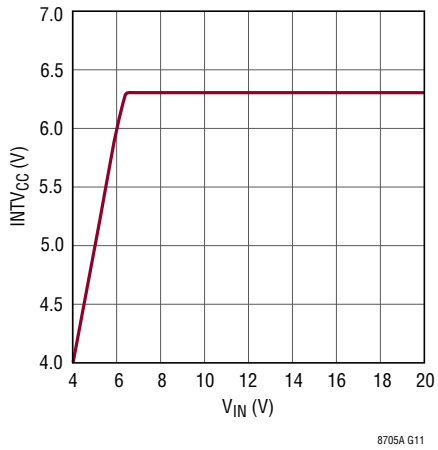


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

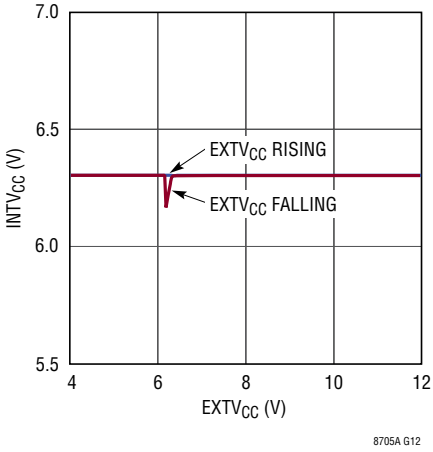
Minimum Inductor Current Sense Voltage in Forced Continuous Mode



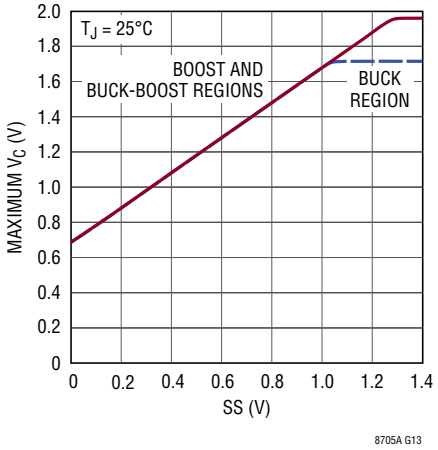
$INTV_{CC}$ Line Regulation ($EXTV_{CC}$ = 0V)



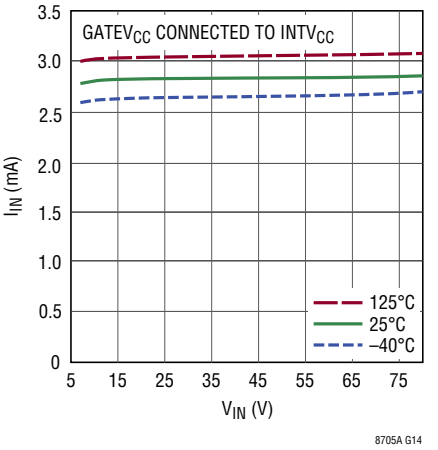
$INTV_{CC}$ Line Regulation (V_{IN} = 12V)



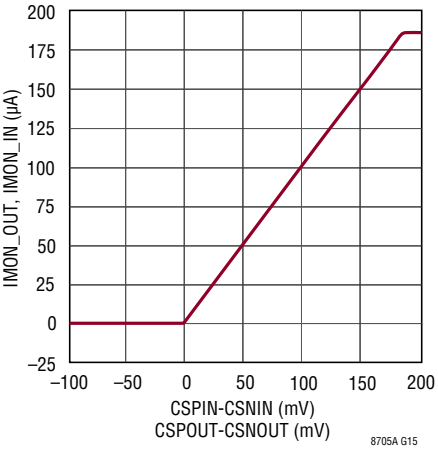
Maximum V_C vs SS



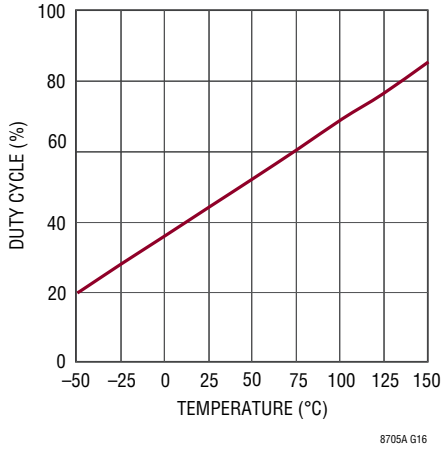
V_{IN} Supply Current vs Voltage (Not Switching)



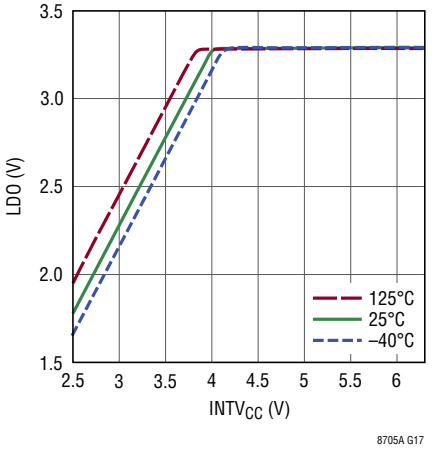
IMON Output Currents



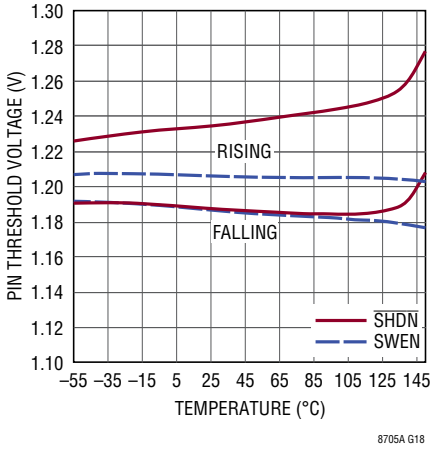
CLKOUT Duty Cycle



LDO33 Pin Regulation (I_{LDO33} = 1mA)



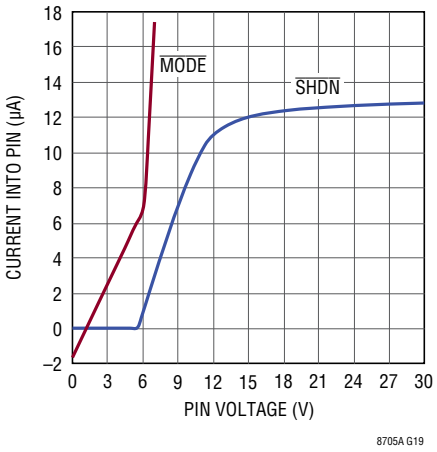
$\overline{SHDN}$ and SWEN Pin Thresholds vs Temperature



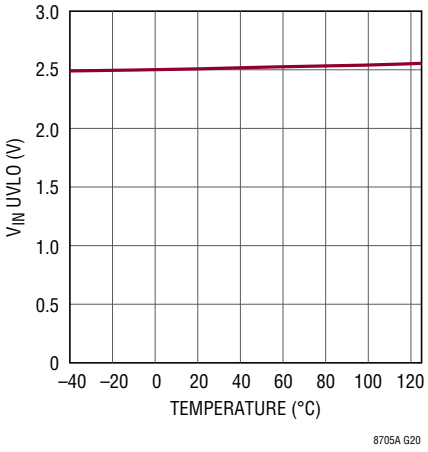
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise specified.

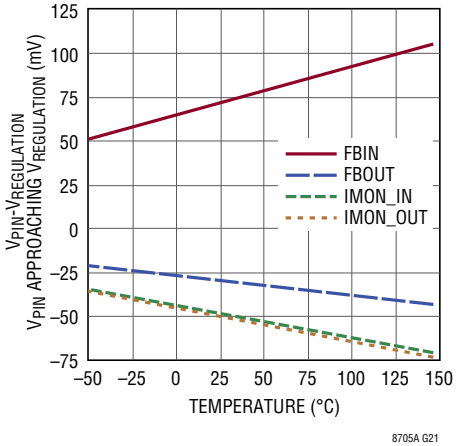
$\overline{SHDN}$ and MODE Pin Currents



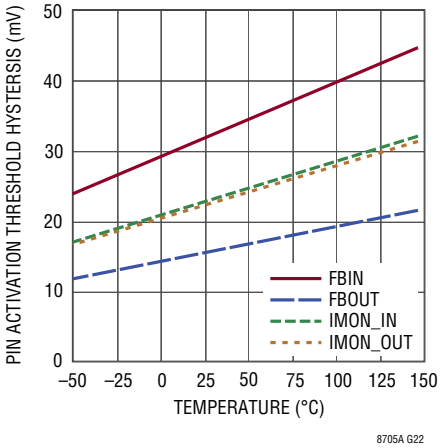
Internal V_{IN} UVLO



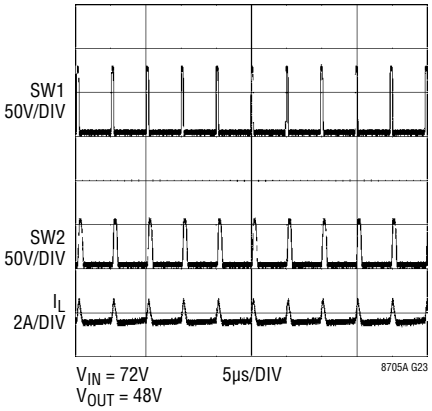
SRVO_xx Pin Activation Thresholds



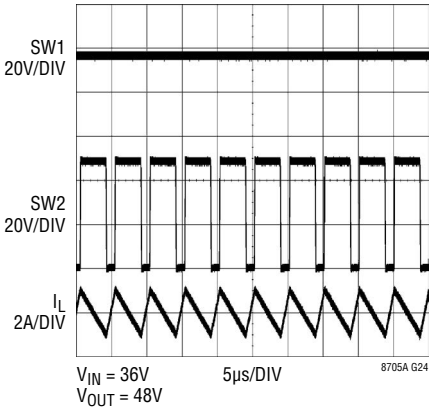
SRVO_xx Pin Activation Threshold Hysteresis



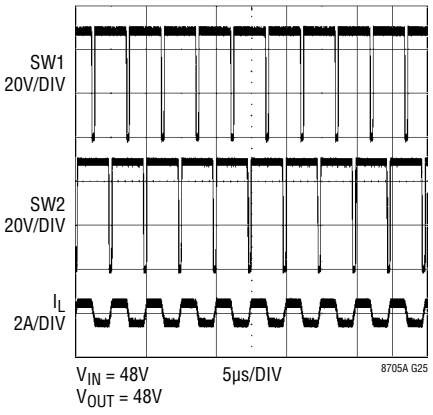
Discontinuous Mode (Figure 15)



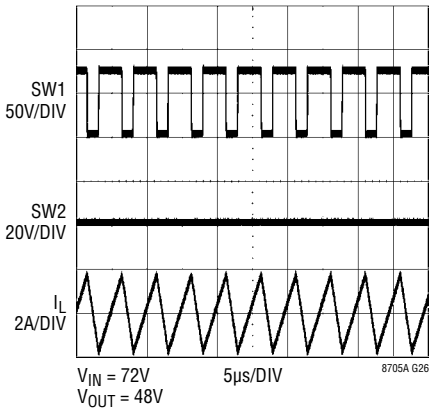
Forced Continuous Mode (Figure 15)



Forced Continuous Mode (Figure 14)

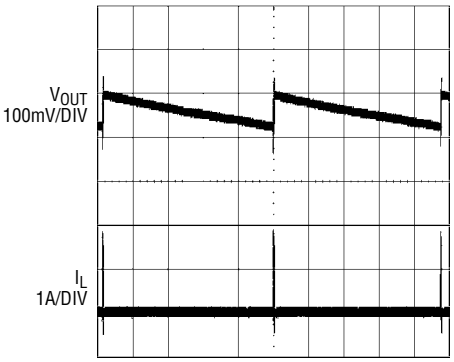


Forced Continuous Mode (Figure 14)

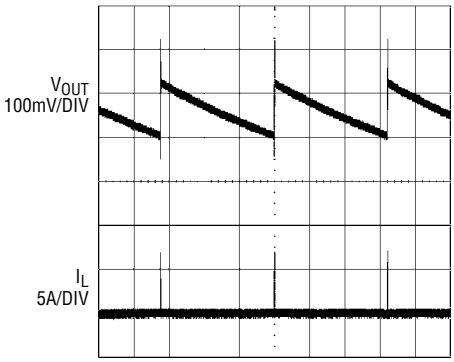


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise specified.

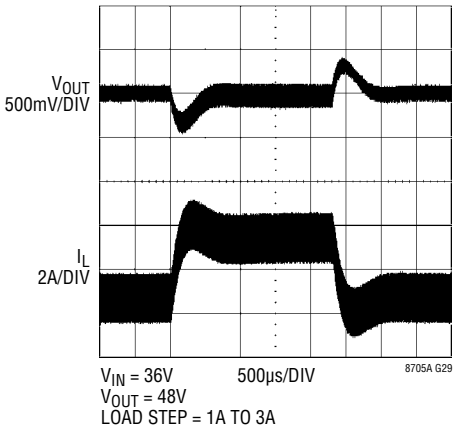
Burst Mode Operation (Figure 14)



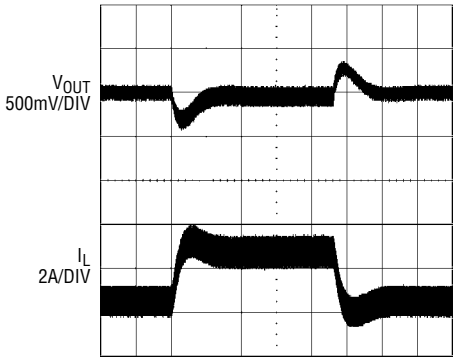
Burst Mode Operation (Figure 14)



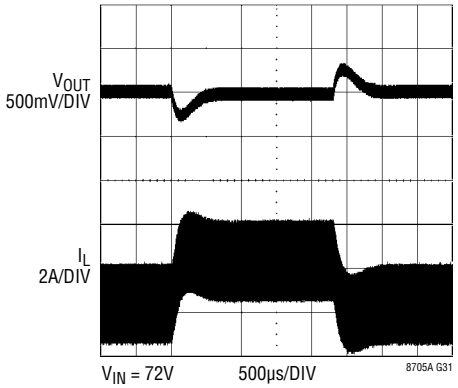
Load Step (Figure 14)



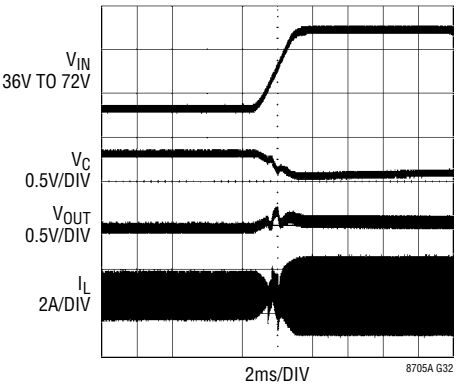
Load Step (Figure 14)



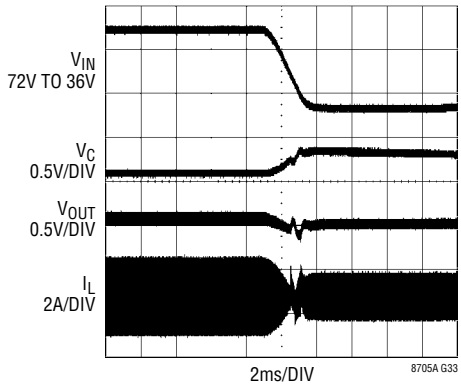
Load Step (Figure 14)



Line Transient (Figure 14)



Line Transient (Figure 14)



PIN FUNCTIONS (QFN/TSSOP)

$\overline{SHDN}$ (Pin 1/Pin 4): Shutdown Pin. Tie high to enable device. Ground to shut down and reduce quiescent current to a minimum. Do not float this pin.

CSN (Pin 2/Pin 5): The (–) Input to the Inductor Current Sense and Reverse-Current Detect Amplifier.

CSP (Pin 3/Pin 6): The (+) Input to the Inductor Current Sense and Reverse-Current Detect Amplifier. The V_C pin voltage and built-in offsets between CSP and CSN pins, in conjunction with the R_{SENSE} resistor value, set the current trip threshold.

LDO33 (Pin 4/Pin 7): 3.3V Regulator Output. Bypass this pin to ground with a minimum 0.1µF ceramic capacitor.

FBIN (Pin 5/Pin 8): Input Feedback Pin. This pin is connected to the input error amplifier input.

FBOUT (Pin 6/Pin 9): Output Feedback Pin. This pin connects the error amplifier input to an external resistor divider from the output.

IMON_OUT (Pin 7/Pin 10): Output Current Monitor Pin. The current out of this pin is proportional to the output current. See the Operation and Applications Information sections.

V_C (Pin 8/Pin 11): Error Amplifier Output Pin. Tie external compensation network to this pin.

SS (Pin 9/Pin 12): Soft-Start Pin. Place at least 100nF of capacitance here. Upon start-up, this pin will be charged by an internal resistor to 2.5V.

CLKOUT (Pin 10/Pin 13): Clock Output Pin. Use this pin to synchronize one or more compatible switching regulator ICs to the LT8705A. CLKOUT toggles at the same frequency as the internal oscillator or as the SYNC pin, but is approximately 180° out of phase. CLKOUT may also be used as a temperature monitor since the CLKOUT duty cycle varies linearly with the part's junction temperature. The CLKOUT pin can drive capacitive loads up to 200pF.

SYNC (Pin 11/Pin 14): To synchronize the switching frequency to an outside clock, simply drive this pin with a clock. The high voltage level of the clock needs to exceed 1.3V, and the low level should be less than 0.5V. Drive this pin to less than 0.5V to revert to the internal free-running clock. See the Applications Information section for more information.

RT (Pin 12/Pin 15): Timing Resistor Pin. Adjusts the switching frequency. Place a resistor from this pin to ground to set the free-running frequency. Do not float this pin.

BG1, BG2 (Pins 14, 16/Pins 17, 19): Bottom Gate Drive. Drives the gates of the bottom N-channel MOSFETs between ground and $GATEV_{CC}$.

$GATEV_{CC}$ (Pin 15/Pin 18): Power Supply for Gate Drivers. Must be connected to the $INTV_{CC}$ pin. Do not power from any other supply. Locally bypass to GND.

BOOST1, BOOST2 (Pins 23, 17/Pins 28, 20): Boosted Floating Driver Supply. The (+) terminal of the bootstrap capacitor connects here. The BOOST1 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{IN} + $GATEV_{CC}$. The BOOST2 pin swings from a diode voltage below $GATEV_{CC}$ up to V_{OUT} + $GATEV_{CC}$

TG1, TG2 (Pins 22, 18/Pins 26, 21): Top Gate Drive. Drives the top N-channel MOSFETs with voltage swings equal to $GATEV_{CC}$ superimposed on the switch node voltages.

SW1, SW2 (Pins 21, 19/Pins 24, 22): Switch Nodes. The (–) terminals of the bootstrap capacitors connect here.

SRVO_FBIN (Pin 25 QFN Only): Open-Drain Logic Output. This pin is pulled to ground when the input voltage feedback loop is active.

SRVO_IIN (Pin 26 QFN Only): Open-Drain Logic Output. The pin is pulled to ground when the input current loop is active.

SRVO_IOUT (Pin 27 QFN Only): Open-Drain Logic Output. The pin is pulled to ground when the output current feedback loop is active.

SRVO_FBOUT (Pin 28 QFN Only): Open-Drain Logic Output. This pin is pulled to ground when the output voltage feedback loop is active.

$EXTV_{CC}$ (Pin 29/Pin 30): External V_{CC} Input. When $EXTV_{CC}$ exceeds 6.4V (typical), $INTV_{CC}$ will be powered from this pin. When $EXTV_{CC}$ is lower than 6.22V (typical), $INTV_{CC}$ will be powered from V_{IN}.

CSNOUT (Pin 30/Pin 32): The (–) Input to the Output Current Monitor Amplifier. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

PIN FUNCTIONS (QFN/TSSOP)

CSPOUT (Pin 31/Pin 34): The (+) Input to the Output Current Monitor Amplifier. This pin and the CSNOUT pin measure the voltage across the sense resistor, R_{SENSE2}, to provide the output current signals. Connect this pin to V_{OUT} when not in use. See Applications Information section for proper use of this pin.

CSNIN (Pin 32/Pin 36): The (–) Input to the Input Current Monitor Amplifier. This pin and the CSPIN pin measure the voltage across the sense resistor, R_{SENSE1}, to provide the input current signals. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

CSPIN (Pin 33/Pin 37): The (+) Input to the Input Current Monitor Amplifier. Connect this pin to V_{IN} when not in use. See Applications Information section for proper use of this pin.

V_{IN} (Pin 34/Pin 38): Main Input Supply Pin. It must be locally bypassed to ground.

$INTV_{CC}$ (Pin 35/Pin 1): Internal 6.35V Regulator Output. Must be connected to the $GATEV_{CC}$ pin. $INTV_{CC}$ is powered from $EXTV_{CC}$ when the $EXTV_{CC}$ voltage is higher than 6.4V, otherwise $INTV_{CC}$ is powered from V_{IN} . Bypass this pin to ground with a minimum 4.7µF ceramic capacitor.

SWEN (Pin 36 QFN Only): Switch Enable Pin. Tie high to enable switching. Ground to disable switching. Don't float this pin. This pin is internally tied to $INTV_{CC}$ in the TSSOP package.

IMON_IN (Pin 38/Pin 3): Input Current Monitor Pin. The current out of this pin is proportional to the input current. See the Operation and Applications Information sections.

MODE (Pin 37/Pin 2): Mode Pin. The voltage applied to this pin sets the operating mode of the controller. When the applied voltage is less than 0.4V, the forced continuous current mode is active. When this pin is allowed to float, Burst Mode operation is active. When the MODE pin voltage is higher than 2.3V, discontinuous mode is active.

GND (Pin 13, Exposed Pad Pin 39/Pin 16, Exposed Pad Pin 39): Ground. Tie directly to local ground plane.

BLOCK DIAGRAM

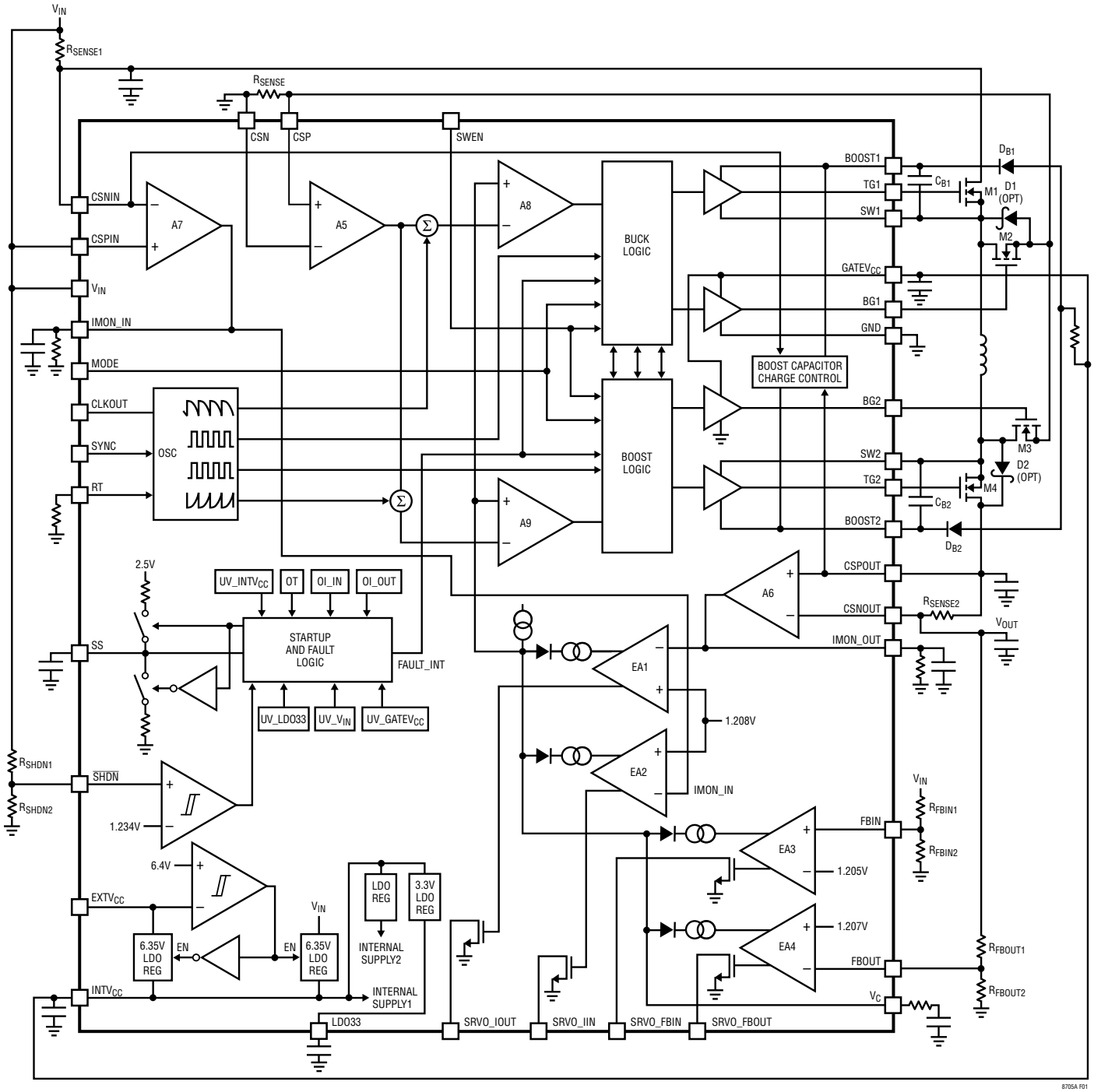


Figure 1. Block Diagram

OPERATION

Refer to the Block Diagram (Figure 1) when reading the following sections about the operation of the LT8705A.

Main Control Loop

The LT8705A is a current mode controller that provides an output voltage above, equal to or below the input voltage. The LTC® proprietary topology and control architecture employs a current-sensing resistor (R_{SENSE}) in buck or boost modes. The inductor current is controlled by the voltage on the V_C pin, which is the diode-AND of error amplifiers EA1-EA4. In the simplest form, where the output is regulated to a constant voltage, the FBOUT pin receives the output voltage feedback signal, which is compared to the internal reference voltage by EA4. Low output voltages would create a higher V_C voltage, and thus more current would flow into the output. Conversely, higher output voltages would cause V_C to drop, thus reducing the current fed into the output.

The LT8705A contains four error amplifiers (EA1-EA4) allowing it to regulate or limit the output current (EA1), input current (EA2), input voltage (EA3) and/or output voltage (EA4). In a typical application, the output voltage might be regulated using EA4, while the remaining error amplifiers are monitoring for excessive input or output current or an input undervoltage condition. In other applications, such as a battery charger, the output current regulator (EA1) can facilitate constant current charging until a predetermined voltage is reached where the output voltage (EA4) control would take over.

$INTV_{CC}$/$EXTV_{CC}$/$GATEV_{CC}$/LDO33 Power

Power for the top and bottom MOSFET drivers, the LDO33 pin and most internal circuitry is derived from the $INTV_{CC}$ pin. $INTV_{CC}$ is regulated to 6.35V (typical) from either the V_{IN} or $EXTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 6.22V (typical), an internal low dropout regulator regulates $INTV_{CC}$ from V_{IN}. If $EXTV_{CC}$ is taken above 6.4V (typical), another low dropout regulator will instead regulate $INTV_{CC}$ from $EXTV_{CC}$. Regulating $INTV_{CC}$ from $EXTV_{CC}$ allows the power to be derived from the lowest supply voltage (highest efficiency) such as the LT8705A switching regulator output (see $INTV_{CC}$ Regulators and $EXTV_{CC}$ Connection in the Applications Information section for more details).

The $GATEV_{CC}$ pin directly powers the bottom MOSFET drivers for switches M2 and M3. $GATEV_{CC}$ should always be connected to $INTV_{CC}$ and should not be powered or connected to any other source. Undervoltage lock outs (UVLOs) monitoring $INTV_{CC}$ and $GATEV_{CC}$ disable the switching regulator when the pins are below 4.65V (typical).

The LDO33 pin is available to provide power to external components such as a microcontroller and/or to provide an accurate bias voltage. Load current is limited to 17.25mA (typical). As long as $\overline{SHDN}$ is high the LDO33 output is linearly regulated from the $INTV_{CC}$ pin and is not affected by the $INTV_{CC}$ or $GATEV_{CC}$ UVLOs or the SWEN pin voltage. LDO33 will remain regulated as long as $\overline{SHDN}$ is high and sufficient voltage is available on $INTV_{CC}$ (typically > 4.0V). An undervoltage lockout, monitoring LDO33, will disable the switching regulator when LDO33 is below 3.04V (typical).

Start-Up

Figure 2 illustrates the start-up sequence for the LT8705A. The master shutdown pin for the chip is $\overline{SHDN}$. When driven below 0.35V (LT8705AE, LT8705AI) or 0.3V (LT8705AH, LT8705AMP) the chip is disabled (chip off state) and quiescent current is minimal. Increasing the $\overline{SHDN}$ voltage can increase quiescent current but will not enable the chip until $\overline{SHDN}$ is driven above 1.234V (typical) after which the $INTV_{CC}$ and LDO33 regulators are enabled (switcher off state). External devices powered by the LDO33 pin can become active at this time if enough voltage is available on V_{IN} or $EXTV_{CC}$ to raise $INTV_{CC}$, and thus LDO33, to an adequate voltage.

Starting up the switching regulator happens after SWEN (switcher enable) is also driven above 1.206V (typical), $INTV_{CC}$ and $GATEV_{CC}$ have risen above 4.81V (typical) and the LDO33 pin has risen above 3.08V (typical) (initialize state). The SWEN pin is not available in the TSSOP package. In this package the SWEN pin is internally connected to $INTV_{CC}$.

Start-Up: Soft-Start of Switch Current

In the initialize state, the SS (soft-start) pin is pulled low to prepare for soft starting the regulator. If forced continuous mode is selected (MODE pin low), the part is put into discontinuous mode during soft-start to prevent current

OPERATION

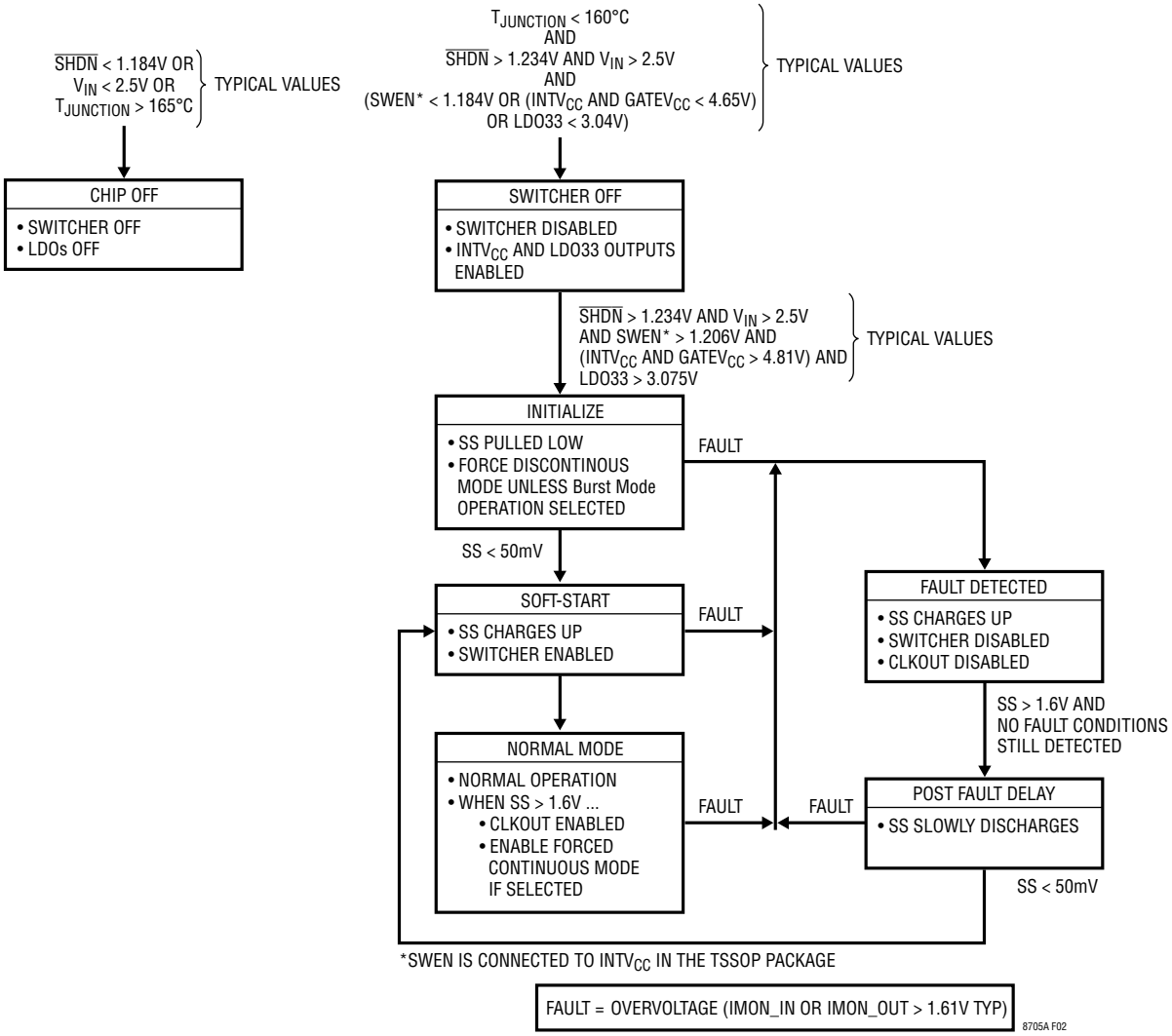


Figure 2. Start-Up and Fault Sequence

from being drawn out of the output and forced into the input. After SS has been discharged to less than 50mV, a soft-start of the switching regulator begins (soft-start state). The soft-start circuitry provides for a gradual ramp-up of the inductor current by gradually allowing the V_C voltage to rise (refer to V_C vs SS Voltage in the Typical Performance Characteristics). This prevents abrupt surges of current from being drawn out of the input power supply. An integrated 100k resistor pulls the SS pin to ≅2.5V. The ramp rate of the SS pin voltage is set by this 100k resistor and the external capacitor connected to this pin. Once SS gets to 1.6V, the CLKOUT pin is enabled, the part is allowed to enter forced continuous mode (if MODE is low) and an internal regulator pulls SS up quickly to ≅2.5V. Typical values for the external soft-start capacitor range from 100nF to 1µF. A minimum of 100nF is recommended.

Fault Conditions

The LT8705A activates a fault sequence under certain operating conditions. If any of these conditions occur (see Figure 2) the CLKOUT pin and internal switching activity are disabled. At the same time, a timeout sequence commences where the SS pin is charged up to a minimum of 1.6V (fault detected state). The SS pin will continue

OPERATION

charging up to 2.5V and be held there in the case of a fault event that persists. After the fault condition had ended and SS is greater than 1.6V, SS will then slowly discharge to 50mV (post fault delay state). This timeout period relieves the part and other downstream power components from electrical and thermal stress for a minimum amount of time as set by the voltage ramp rate on the SS pin. After SS has discharged to < 50mV, the LT8705A will enter the soft-start state and restart switching activity.

Power Switch Control

Figure 3 shows a simplified diagram of how the four power switches are connected to the inductor, V_{IN}, V_{OUT} and ground. Figure 4 shows the regions of operation for the LT8705A as a function of V_{OUT}-V_{IN} or switch duty cycle DC. The power switches are properly controlled so the transfer between modes is continuous.

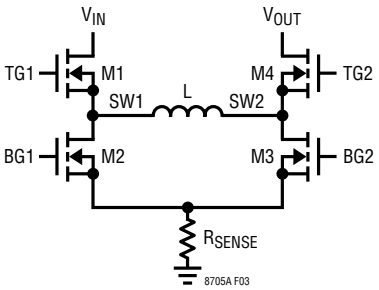


Figure 3. Simplified Diagram of the Output Switches

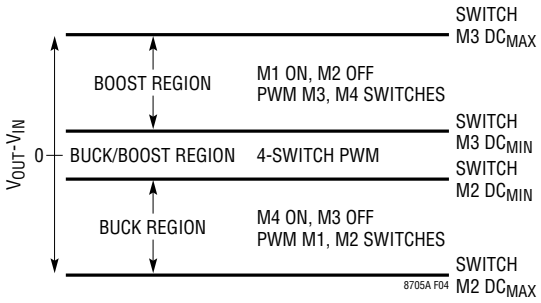


Figure 4. Operating Regions vs V_{OUT}-V_{IN}

Power Switch Control: Buck Region (V_{IN} >> V_{OUT})

When V_{IN} is significantly higher than V_{OUT}, the part will run in the buck region. In this region switch M3 is always off. Also, switch M4 is always on unless reverse current is detected while in Burst Mode operation or discontinuous mode. At the start of every cycle, synchronous switch M2 is turned on first. Inductor current is sensed by amplifier A5 while switch M2 is on. A slope compensation ramp is added to the sensed voltage which is then compared by A8 to a reference that is proportional to V_C. After the sensed inductor current falls below the reference, switch M2 is turned off and switch M1 is turned on for the remainder of the cycle. Switches M1 and M2 will alternate, behaving like a typical synchronous buck regulator.

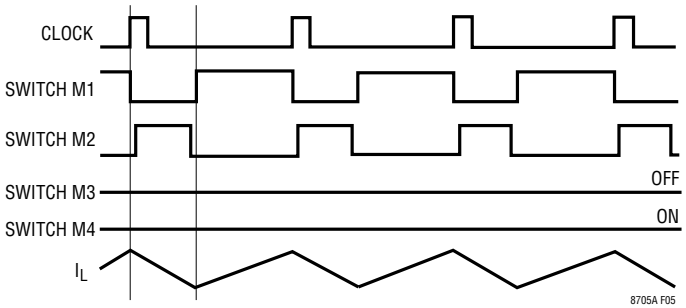


Figure 5. Buck Region (V_{IN} >> V_{OUT})

The part will continue operating in the buck region over a range of switch M2 duty cycles. The duty cycle of switch M2 in the buck region is given by:

$$DC_{(M2,BUCK)} = \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter in buck mode reaches $DC_{(ABSMIN,M2,BUCK)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M2,BUCK)}$ the part will move to the buck-boost region.

$$DC_{(ABSMIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M2,MIN)}$ is the minimum on-time for the synchronous switch in buck operation (260ns typical, see Electrical Characteristics).

f is the switching frequency

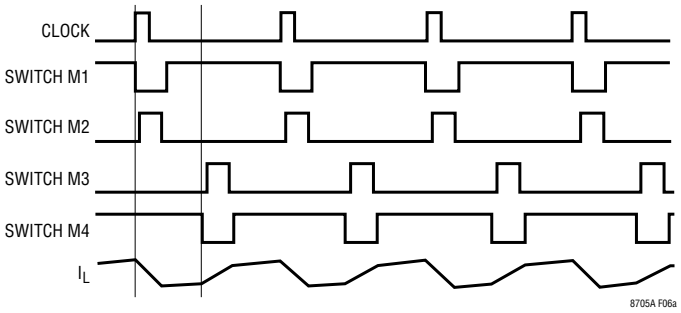
When V_{IN} is much higher than V_{OUT} the duty cycle of switch M2 will increase, causing the M2 switch off-time to decrease. The M2 switch off-time should be kept above 245ns (typical, see Electrical Characteristics) to maintain steady-state operation, avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

OPERATION

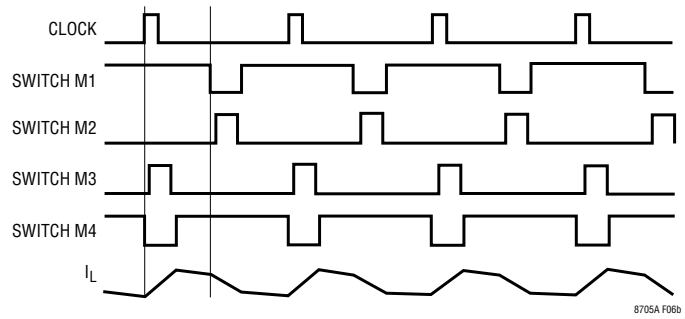
Power Switch Control: Buck-Boost ($V_{IN} \cong V_{OUT}$)

When V_{IN} is close to V_{OUT}, the controller enters the buck-boost region. Figure 6 shows typical waveforms in this region. Every cycle, if the controller starts with switches M2 and M4 turned on, the controller first operates as if in the buck region. When A8 trips, switch M2 is turned off and M1 is turned on until the middle of the clock cycle. Next, switch M4 turns off and M3 turns on. The LT8705A then operates as if in boost mode until A9 trips. Finally switch M3 turns off and M4 turns on until the end of the cycle.

If the controller starts with switches M1 and M3 turned on, the controller first operates as if in the boost region. When A9 trips, switch M3 is turned off and M4 is turned on until the middle of the clock cycle. Next, switch M1 turns off and M2 turns on. The LT8705A then operates as if in buck mode until A8 trips. Finally switch M2 turns off and M1 turns on until the end of the cycle.



(6a) Buck-Boost Region ($V_{IN} \geq V_{OUT}$)



(6b) Buck-Boost Region ($V_{IN} \leq V_{OUT}$)

Figure 6. Buck-Boost Region

Power Switch Control: Boost Region ($V_{IN} << V_{OUT}$)

When V_{OUT} is significantly higher than V_{IN}, the part will run in the boost region. In this region switch M1 is always on and switch M2 is always off. At the start of every cycle, switch M3 is turned on first. Inductor current is sensed by amplifier A5 while switch M3 is on. A slope compensation ramp is added to the sensed voltage which is then compared (A9) to a reference that is proportional to V_C. After the sensed inductor current rises above the reference voltage, switch M3 is turned off and switch M4 is turned on for the remainder of the cycle. Switches M3 and M4 will alternate, behaving like a typical synchronous boost regulator.

The part will continue operating in the boost region over a range of switch M3 duty cycles. The duty cycle of switch M3 in the boost region is given by:

$$DC_{(M3,BOOST)} = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \bullet 100\%$$

As V_{IN} and V_{OUT} get closer to each other, the duty cycle decreases until the minimum duty cycle of the converter in boost mode reaches $DC_{(ABSMIN,M3,BOOST)}$. If the duty cycle becomes lower than $DC_{(ABSMIN,M3,BOOST)}$ the part will move to the buck-boost region:

$$DC_{(ABSMIN,M3,BOOST)} \cong t_{ON(M3,MIN)} \bullet f \bullet 100\%$$

where:

$t_{ON(M3,MIN)}$ is the minimum on-time for the main switch in boost operation (265ns typical, see Electrical Characteristics)

f is the switching frequency

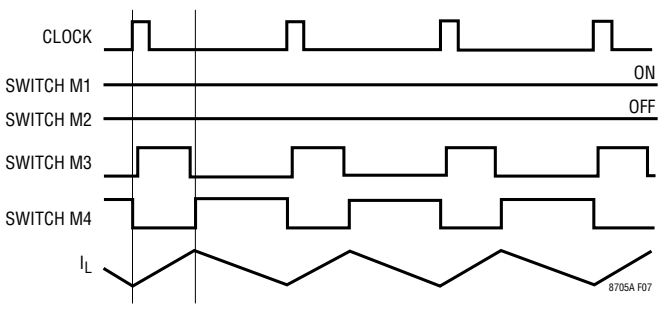


Figure 7. Boost Region ($V_{IN} << V_{OUT}$)

OPERATION

When V_{OUT} is much higher than V_{IN} the duty cycle of switch M3 will increase, causing the M3 switch off-time to decrease. The M3 switch off-time should be kept above 245ns (typical, see Electrical Characteristics) to maintain steady-state operation, avoid duty cycle jitter, increased output ripple and reduction in maximum output current.

Light Load Current Operation (MODE Pin)

Under light current load conditions, the LT8705A can be set to operate in discontinuous mode, forced continuous mode, or Burst Mode operation. To select forced continuous mode, tie the MODE pin to a voltage below 0.4V (i.e., ground). To select discontinuous mode, tie MODE to a voltage above 2.3V (i.e., LDO33). To select Burst Mode operation, float the MODE pin or tie it between 1.0V and 1.7V.

Discontinuous Mode: When the LT8705A is in discontinuous mode, synchronous switch M4 is held off whenever reverse current in the inductor is detected. This is to prevent current draw from the output and/or feeding current to the input supply. Under very light loads, the current comparator may also remain tripped for several cycles and force switches M1 and M3 to stay off for the same number of cycles (i.e., skipping pulses). Synchronous switch M2 will remain on during the skipped cycles, but since switch M4 is off, the inductor current will not reverse.

Burst Mode Operation: Burst Mode operation sets a V_C level, with about 25mV of hysteresis, below which switching activity is inhibited and above which switching activity is re-enabled. A typical example is when, at light output currents, V_{OUT} rises and forces the V_C pin below the threshold that temporarily inhibits switching. After V_{OUT} drops slightly and V_C rises ~25mV the switching is resumed, initially in the buck-boost region. Burst Mode operation can increase efficiency at light load currents by eliminating unnecessary switching activity and related power losses. Burst Mode operation handles reverse-current detection similar to discontinuous mode. The M4 switch is turned off when reverse current is detected.

Forced Continuous Mode: The forced continuous mode allows the inductor current to reverse directions without any switches being forced "off" to prevent this from happening. At very light load currents the inductor current will swing positive and negative as the appropriate average current is delivered to the output. During soft-start, when the SS pin is below 1.6V, the part will be forced into discontinuous mode to prevent pulling current from the output to the input. After SS rises above 1.6V, forced continuous mode will be enabled.

Voltage Regulation Loops

The LT8705A provides two constant-voltage regulation loops, one for output voltage and one for input voltage. A resistor divider between V_{OUT}, FBOUT and GND senses the output voltage. As with traditional voltage regulators, when FBOUT rises near or above the reference voltage of EA4 (1.207V typical, see Block Diagram), the V_C voltage is reduced to command the amount of current that keeps V_{OUT} regulated to the desired voltage.

The input voltage can also be sensed by connecting a resistor divider between V_{IN}, FBIN and GND. When the FBIN voltage falls near or below the reference voltage of EA3 (1.205V typical, see Block Diagram), the V_C voltage is reduced to also reduce the input current. For applications with a high input source impedance (i.e., a solar panel), the input voltage regulation loop can prevent the input voltage from becoming too low under high output load conditions. For applications with a lower input source impedance (i.e., batteries and voltage supplies), the FBIN pin can be used to stop switching activity when the input power supply voltage gets too low for proper system operation. See the Applications Information section for more information about setting up the voltage regulation loops.

Current Monitoring and Regulation

The LT8705A provides two constant-current regulation loops, one for input current and one for output current. A sensing resistor close to the input capacitor, sensed by CSPIN and CSNIN, monitors the input current. A current, linearly proportional to the sense voltage (V_{CSPIN}-V_{CSNIN}), is forced out of the IMON_IN pin and into an external resistor. The resulting voltage V_{IMON_IN} is therefore linearly proportional to the input current. Similarly, a sensing resistor close to the output capacitor, and sensed by

OPERATION

CSPOUT and CSNOUT will monitor the output current and generate a voltage V_{IMON_OUT} that is linearly proportional to the output current.

When the input or output current causes the respective IMON_IN or IMON_OUT voltage to rise near or above 1.208V (typical), the V_C pin voltage will be pulled down to maintain the desired maximum input and/or output current (see EA1 and EA2 on the Block Diagram). The input current limit function prevents overloading the DC input source, while the output current limit provides a building block for battery charger or LED driver applications. It can also serve as short-circuit protection for a constant-voltage regulator. See the Applications Information section for more information about setting up the current regulation loops.

SRVO Pins

The QFN package has four open-drain SRVO pins: SRVO_FBIN, SRVO_FBOUT, SRVO_IIN, SRVO_IOUT. Place pull-up resistors from the desired SRVO pin(s) to a power supply less than 30V (i.e., the LDO33 pin) to enable reading of their logic states. The SRVO_FBOUT, SRVO_IIN and SRVO_IOUT pins are pulled low when their associated error amp (EA4, EA2, EA1) input voltages are near or greater than their regulation voltages (≅1.2V typical). SRVO_FBIN is pulled low when FBIN is near or lower than its regulation voltage (≅1.2V typical). The SRVO pins can therefore be used as indicators of when their respective feedback loops are active. For example, the SRVO_FBOUT pin pulls low when FBOUT rises to within 29mV (typical, see Electrical Characteristics) of its regulation voltage (1.207V typical). The pull-down turns off after FBOUT falls to more than 44mV (typical) lower than its regulation voltage. As another example, the SRVO_IOUT pin can be read to determine when the output current has nearly reached its predetermined limit. A logic "1" on SRVO_IOUT indicates that the output current has not reached the current limit and a logic "0" indicates that it has.

CLKOUT and Temperature Sensing

The CLKOUT pin toggles at the LT8705A's internal clock frequency whether the internal clock is synchronized to an external source or is free-running based on the external R_T resistor. The CLKOUT pin can be used to synchronize other devices to the LT8705A's switching frequency. Also, the duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues.

APPLICATIONS INFORMATION

The first page shows a typical LT8705A application circuit. After the switching frequency is selected, external component selection continues with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs are selected. Finally, C_{IN} and C_{OUT} are selected. The following examples and equations assume continuous conduction mode unless otherwise specified. The circuit can be configured for operation up to an input and/or output voltage of 80V.

LT8705A vs LT8705

The LT8705A is a pin for pin compatible, minor silicon revision of the LT8705. The LT8705A contains a few main improvements over the LT8705.

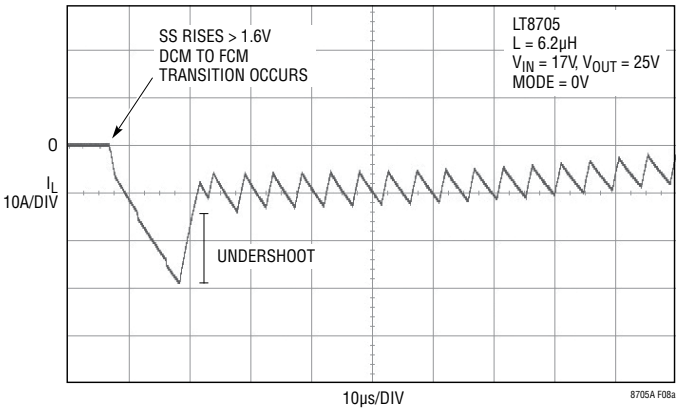
The first main improvement effects the transition from DCM (discontinuous conduction mode) to FCM (forced continuous mode) operation. The most common transition from DCM to FCM occurs during soft-start while the MODE pin is driven low, thus selecting FCM operation. As illustrated in the startup sequence of Figure 2, the LT8705 and LT8705A begin operating in DCM, even if MODE is set to FCM. When the SS pin rises above 1.6V the LT8705 and LT8705A transition from DCM to FCM.

The improved LT8705A reduces or eliminates the inductor current (I_L) undershoot that could occur during the following operating conditions…

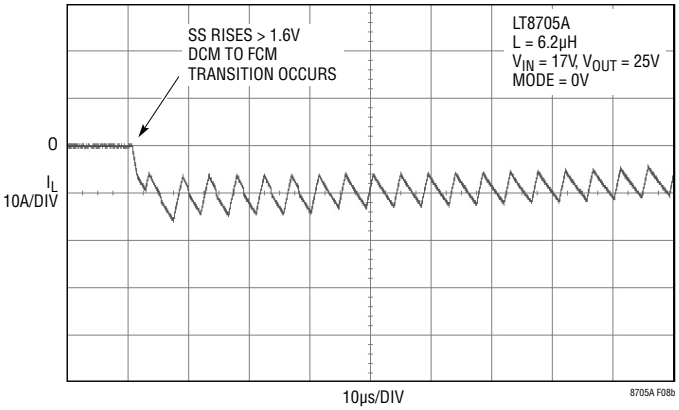
- The operating MODE transitions from DCM to FCM and
- V_C is low enough to command a negative inductor current (I_L) and
- V_{OUT} is near or greater than V_{IN} at the time of the transition

Figure 8 shows examples of the inductor current undershoot that has been reduced with the LT8705A (Figure 8b) as compared to the LT8705 (Figure 8a). Note that most LT8705 applications will not exhibit nearly as much undershoot as shown in Figure 8a. Conditions that reduce the amount of undershoot are…

- Higher inductance
- Higher frequency
- Higher V_C during the DCM to FCM transition
- Lower V_{IN} during the DCM to FCM transition
- Lower $V_{OUT} – V_{IN}$ during the DCM to FCM transition



(8a)



(8b)

Figure 8. LT8705 and LT8705A Inductor Current During DCM to FCM Transition

The operating conditions for Figures 8a and 8b were intentionally set to maximize undershoot, including having V_C at the lowest possible voltage at the time of the transition.

The second main improvement effects the IMON_IN and IMON_OUT currents, typically when operating below –25°C, when the respective $V_{CSPIN} – V_{CSNIN}$ or $V_{CSPOUT} – V_{CSNOUT}$ voltages are very close to 0mV. Using the LT8705 under these conditions, the IMON_OUT or IMON_IN output current can increase, above the expected amount, by a few µA. The increased current, above the expected amount, diminishes as $V_{CSPIN} – V_{CSNIN}$ or $V_{CSPOUT} – V_{CSNOUT}$ increases and is typically gone when $V_{CSPIN} – V_{CSNIN}$ or $V_{CSPOUT} – V_{CSNOUT}$ becomes 5mV or greater. The LT8705A has been improved to eliminate the additional output current under those conditions.

APPLICATIONS INFORMATION

Operating Frequency Selection

The LT8705A uses a constant frequency architecture between 100kHz and 400kHz. The frequency can be set using the internal oscillator or can be synchronized to an external clock source. Selection of the switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires more inductance and/or capacitance to maintain low output ripple voltage. For high power applications, consider operating at lower frequencies to minimize MOSFET heating from switching losses. The switching frequency can be set by placing an appropriate resistor from the RT pin to ground and tying the SYNC pin low. The frequency can also be synchronized to an external clock source driven into the SYNC pin. The following sections provide more details.

Internal Oscillator

The operating frequency of the LT8705A can be set using the internal free-running oscillator. When the SYNC pin is driven low (<0.5V), the frequency of operation is set by the value of a resistor from the RT pin to ground. An internally trimmed timing capacitor resides inside the IC. The oscillator frequency is calculated using the following formula:

$$f_{OSC} = \left(\frac{43,750}{R_T + 1}\right) kHz$$

where f_{OSC} is in kHz and R_T is in kΩ. Conversely, R_T (in kΩ) can be calculated from the desired frequency (in kHz) using:

$$R_T = \left(\frac{43,750}{f_{OSC}} - 1\right) k\Omega$$

SYNC Pin and Clock Synchronization

The operating frequency of the LT8705A can be synchronized to an external clock source. To synchronize to the external source, simply provide a digital clock signal into the SYNC pin. The LT8705A will operate at the SYNC clock frequency.

The duty cycle of the SYNC signal must be between 20% and 80% for proper operation. Also, the frequency of the SYNC signal must meet the following two criteria:

1. SYNC may not toggle outside the frequency range of 100kHz to 400kHz unless it is stopped low to enable the free-running oscillator.
2. The SYNC pin frequency can always be higher than the free-running oscillator set frequency, f_{OSC}, but should not be less than 25% below f_{OSC}.

After SYNC begins toggling, it is recommended that switching activity is stopped before the SYNC pin stops toggling. Excess inductor current can result when SYNC stops toggling as the LT8705A transitions from the external SYNC clock source to the internal free-running oscillator clock. Switching activity can be stopped by driving either the SWEN or $\overline{SHDN}$ pin low.

CLKOUT Pin and Clock Synchronization

The CLKOUT pin can drive up to 200pF and toggles at the LT8705A's internal clock frequency whether the internal clock is synchronized to the SYNC pin or is free-running based on the external R_T resistor. The rising edge of CLKOUT is approximately 180° out of phase from the internal clock's rising edge or the SYNC pin's rising edge if it is toggling. CLKOUT toggles only in normal mode (see Figure 2).

The CLKOUT pin can be used to synchronize other devices to the LT8705A's switching frequency. For example, the CLKOUT pin can be tied to the SYNC pin of another LT8705A regulator which will operate approximately 180° out of phase of the master LT8705A due to the CLKOUT phase shift. The frequency of the master LT8705A can be set by the external R_T resistor or by toggling the SYNC pin. CLKOUT will begin oscillating after the master LT8705A enters normal mode (see Figure 2). Note that the RT pin of the slave LT8705A must have a resistor tied to ground. In general, use the same value R_T resistor for all of the synchronized LT8705As.

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The duty cycle of CLKOUT is proportional to the die temperature and can be used to monitor the die for thermal issues. See the Junction Temperature Measurement section for more information.

Inductor Current Sensing and Slope Compensation

The LT8705A operates using inductor current mode control. As described previously in the Power Switch Control section, the LT8705A measures the peak of the inductor current waveform in the boost region and the valley of the inductor current waveform in the buck region. The inductor current is sensed across the R_{SENSE} resistor with pins CSP and CSN. During any given cycle, the peak (boost region) or valley (buck region) of the inductor current is controlled by the V_C pin voltage.

Slope compensation provides stability in constant-frequency current mode control architectures by preventing subharmonic oscillations at high duty cycles. This is accomplished internally by adding a compensating ramp to the inductor current signal in the boost region, or subtracting a ramp from the inductor current signal in the buck region. At higher duty cycles, this results in a reduction of maximum inductor current in the boost region, and an increase of the maximum inductor current in the buck region. For example, refer to the Maximum Inductor Current Sense Voltage vs Duty Cycle graph in the Typical Performance Characteristics section. The graph shows that, with V_C at its maximum voltage, the maximum inductor sense voltage V_{RSENSE} is between 78mV and 117mV depending on the duty cycle. It also shows that the maximum inductor valley current in the buck region is 86mV increasing to ~130mV at higher duty cycles.

R_{SENSE} Selection and Maximum Current

The R_{SENSE} resistance must be chosen properly to achieve the desired amount of output current. Too much resistance can limit the output current below the application requirements. Start by determining the maximum allowed R_{SENSE} resistance in the boost region, $R_{SENSE(MAX,BOOST)}$. Follow this by finding the maximum allowed R_{SENSE} resistance in the buck region, $R_{SENSE(MAX,BUCK)}$. The selected R_{SENSE} resistance must be smaller than both.

Boost Region: In the boost region, the maximum output current capability is the least when V_{IN} is at its minimum and V_{OUT} is at its maximum. Therefore R_{SENSE} must be chosen to meet the output current requirements under these conditions.

Start by finding the boost region duty cycle when V_{IN} is minimum and V_{OUT} is maximum using:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{V_{IN(MIN)}}{V_{OUT(MAX)}}\right) \bullet 100\%$$

For example, an application with a V_{IN} range of 12V to 48V and V_{OUT} set to 36V will have:

$$DC_{(MAX,M3,BOOST)} \cong \left(1 - \frac{12V}{36V}\right) \bullet 100\% = 67\%$$

Referring to the Maximum Inductor Current Sense Voltage graph in the Typical Performance Characteristics section, the maximum R_{SENSE} voltage at 67% duty cycle is ≅93mV, or:

$$V_{RSENSE(MAX,BOOST,\ MAX)} \cong 93mV$$

for V_{IN} = 12V, V_{OUT} = 36V.

Next, the inductor ripple current in the boost region must be determined. If the main inductor L is not known, the maximum ripple current $\Delta I_{L(MAX,BOOST)}$ can be estimated by choosing $\Delta I_{L(MAX,BOOST)}$ to be 30% to 50% of the maximum inductor current in the boost region as follows:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{V_{OUT(MAX)} \bullet I_{OUT(MAX,BOOST)}}{V_{IN(MIN)} \bullet \left(\frac{100\%}{\%Ripple} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BOOST)}$ is the maximum output load current required in the boost region

%Ripple is 30% to 50%

For example, using $V_{OUT(MAX)}$ = 36V, $V_{IN(MIN)}$ = 12V, $I_{OUT(MAX,BOOST)}$ = 2A and %Ripple = 40% we can estimate:

$$\Delta I_{L(MAX,BOOST)} \cong \frac{36V \bullet 2A}{12V \bullet \left(\frac{100\%}{40\%} - 0.5\right)} = 3A$$

APPLICATIONS INFORMATION

Otherwise, if the inductor value is already known then $\Delta I_{L(MAX,BOOST)}$ can be more accurately calculated as follows:

$$\Delta I_{L(MAX,BOOST)} = \frac{\left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right) \bullet V_{IN(MIN)}}{f \bullet L} A$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage in the boost region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the maximum ripple current is known, the maximum allowed R_{SENSE} in the boost region can be calculated as follows:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet V_{RSENSE(MAX,BOOST,MAX)} \bullet V_{IN(MIN)}}{\left(2 \bullet I_{OUT(MAX,BOOST)} \bullet V_{OUT(MIN)}\right) + \left(\Delta I_{L(MAX,BOOST)} \bullet V_{IN(MIN)}\right)} \Omega$$

where $V_{RSENSE(MAX,BOOST,MAX)}$ is the maximum inductor current sense voltage as discussed in the previous section.

Using values from the previous examples:

$$R_{SENSE(MAX,BOOST)} = \frac{2 \bullet 93mV \bullet 12}{(2 \bullet 2A \bullet 36V) + (3A \bullet 12V)} = 12.4m\Omega$$

Buck Region: In the buck region, the maximum output current capability is the least when operating at the minimum duty cycle. This is because the slope compensation ramp increases the maximum R_{SENSE} voltage with increasing duty cycle. The minimum duty cycle for buck operation can be calculated using:

$$DC_{(MIN,M2,BUCK)} \cong t_{ON(M2,MIN)} \bullet f \bullet 100\%$$

where $t_{ON(M2,MIN)}$ is 260ns (typical value, see Electrical Characteristics)

Before calculating the maximum R_{SENSE} resistance, however, the inductor ripple current must be determined. If the main inductor L is not known, the ripple current $\Delta I_{L(MIN,BUCK)}$ can be estimated by choosing $\Delta I_{L(MIN,BUCK)}$ to be 10% of the maximum inductor current in the buck region as follows:

$$\Delta I_{L(MIN,BUCK)} \cong \frac{I_{OUT(MAX,BUCK)}}{\left(\frac{100\%}{10\%} - 0.5\right)} A$$

where:

$I_{OUT(MAX,BUCK)}$ is the maximum output load current required in the buck region.

If the inductor value is already known then $\Delta I_{L(MIN,BUCK)}$ can be calculated as follows:

$$\Delta I_{L(MIN,BUCK)} = \frac{\left(\frac{DC_{(MIN,M2,BUCK)}}{100\%}\right) \bullet V_{OUT(MIN)}}{f \bullet L} A$$

where:

$DC_{(MIN,M2,BUCK)}$ is the minimum duty cycle percentage in the buck region as calculated previously.

f is the switching frequency

L is the inductance of the main inductor

After the inductor ripple current is known, the maximum allowed R_{SENSE} in the buck region can be calculated as follows:

$$R_{SENSE(MAX,BUCK)} = \frac{2 \bullet 86mV}{\left(2 \bullet I_{OUT(MAX,BUCK)}\right) - \Delta I_{L(MIN,BUCK)}}$$

Final R_{SENSE} Value: The final R_{SENSE} value should be lower than both $R_{SENSE(MAX,BOOST)}$ and $R_{SENSE(MAX,BUCK)}$. A margin of 30% or more is recommended.

Figure 9 shows approximately how the maximum output current and maximum inductor current would vary with V_{IN}/V_{OUT} while all other operating parameters remain constant (frequency = 350kHz, inductance = 10µH, R_{SENSE} = 10mΩ). This graph is normalized and accounts for changes in maximum current due to the slope compensation ramps and the effects of changing ripple current. The curve is theoretical, but can be used as a guide to predict relative changes in maximum output and inductor current over a range of V_{IN}/V_{OUT} voltages.

APPLICATIONS INFORMATION

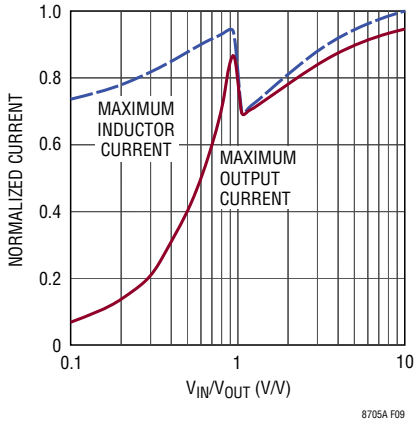

Figure 9. Currents vs V_{IN}/V_{OUT} Ratio

Reverse Current Limit

When the forced continuous mode is selected (MODE pin low), inductor current is allowed to reverse directions and flow from the V_{OUT} side to the V_{IN} side. This can lead to current sinking from the output and being forced into the input. The reverse current is at a maximum magnitude when V_C is lowest. The graph of Minimum Inductor Current Sense Voltage in FCM in the Typical Performance Characteristics section can help to determine the maximum reverse current capability.

Inductor Selection

For high efficiency, choose an inductor with low core loss, such as ferrite. Also, the inductor should have low DC resistance to reduce the I^2R losses, and must be able to handle the peak inductor current without saturating. To minimize radiated noise, use a toroid, pot core or shielded bobbin inductor.

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. The following sections discuss several criteria to consider when choosing an inductor value. For optimal performance, choose an inductor that meets all of the following criteria.

Inductor Selection: Adequate Load Current in the Boost Region

Small value inductors result in increased ripple currents and thus, due to the limited peak inductor current, decrease the maximum average current that can be provided to the load (I_{OUT}) while operating in the boost region.

In order to provide adequate load current at low V_{IN} voltages in the boost region, L should be at least:

$$L_{(MIN1,BOOST)} \cong \frac{V_{IN(MIN)} \bullet \left(\frac{DC_{(MAX,M3,BOOST)}}{100\%}\right)}{2 \bullet f \bullet \left(\frac{V_{RSENSE(MAX,BOOST,MAX)}}{R_{SENSE}} - \frac{I_{OUT(MAX)} \bullet V_{OUT(MAX)}}{V_{IN(MIN)}}\right)}$$

where:

$DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection and Maximum Current section).

f is the switching frequency

$V_{RSENSE(MAX,BOOST,MAX)}$ is the maximum current sense voltage in the boost region at maximum duty cycle (see R_{SENSE} Selection and Maximum Current section)

Negative values of $L_{(MIN1,BOOST)}$ indicate that the output load current I_{OUT} can't be delivered in the boost region because the inductor current limit is too low. If $L_{(MIN1,BOOST)}$ is too large or is negative, consider reducing the R_{SENSE} resistor value to increase the inductor current limit.

Inductor Selection: Subharmonic Oscillations

The LT8705A's internal slope compensation circuits will prevent subharmonic oscillations that can otherwise occur when V_{IN}/V_{OUT} is less than 0.5 or greater than 2. The slope compensation circuits will prevent these oscillations provided that the inductance exceeds a minimum value (see the earlier section Inductor Current Sensing and Slope Compensation for more information). Choose an inductance greater than all of the relevant $L_{(MIN)}$ limits discussed below. Negative results can be interpreted as zero.

In the boost region, if V_{OUT} can be greater than twice V_{IN}, calculate $L_{(MIN2,BOOST)}$ as follows:

$$L_{(MIN2,BOOST)} = \frac{\left[V_{OUT(MAX)} - \left(\frac{V_{IN(MIN)} \bullet V_{OUT(MAX)}}{V_{OUT(MAX)} - V_{IN(MIN)}}\right)\right] \bullet R_{SENSE}}{0.08 \bullet f} H$$

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In the buck region, if V_{IN} can be greater than twice V_{OUT}, calculate $L_{(MIN1,BUCK)}$ as follows:

$$L_{(MIN1,BUCK)} = \frac{V_{IN(MAX)} \bullet \left(1 - \frac{V_{OUT(MAX)}}{V_{IN(MAX)} - V_{OUT(MIN)}}\right) \bullet R_{SENSE}}{0.08 \bullet f} H$$

Inductor Selection: Maximum Current Rating

The inductor must have a rating greater than its peak operating current to prevent inductor saturation resulting in efficiency loss. The peak inductor current in the boost region is:

$$I_{L(MAX,BOOST)} \cong I_{OUT(MAX)} \bullet \frac{V_{OUT(MAX)}}{V_{IN(MIN)}} + \left(\frac{V_{IN(MIN)} \bullet \left(\frac{DC_{(MAX,M3,BOOST}}{100\%}\right)}{2 \bullet L \bullet f}\right) A$$

where $DC_{(MAX,M3,BOOST)}$ is the maximum duty cycle percentage of the M3 switch (see R_{SENSE} Selection and Maximum Current section).

The peak inductor current when operating in the buck region is:

$$I_{L(MAX,BUCK)} \cong I_{OUT(MAX)} + \left(\frac{V_{OUT(MIN)} \bullet \left(\frac{DC_{(MAX,M2,BUCK}}{100\%}\right)}{2 \bullet L \bullet f}\right) A$$

where $DC_{(MAX,M2,BUCK)}$ is the maximum duty cycle percentage of the M2 switch in the buck region given by:

$$DC_{(MAX,M2,BUCK)} \cong \left(1 - \frac{V_{OUT(MIN)}}{V_{IN(MAX)}}\right) \bullet 100\%$$

Note that the inductor current can be higher during load transients and if the load current exceeds the expected maximum $I_{OUT(MAX)}$. It can also be higher during start-up if inadequate soft-start capacitance is used or during output shorts. Consider using the output current limiting to prevent the inductor current from becoming excessive. Output current limiting is discussed later in the Input/Output Current Monitoring and Limiting section. Careful board evaluation of the maximum inductor current is recommended.

Power MOSFET Selection and Efficiency Considerations

The LT8705A requires four external N-channel power MOSFETs, two for the top switches (switches M1 and M4, shown in Figure 3) and two for the bottom switches (switches M2 and M3, shown in Figure 3). Important parameters for the power MOSFETs are the breakdown voltage, $V_{BR,DSS}$, threshold voltage, $V_{GS,TH}$, on-resistance, $R_{DS(ON)}$, reverse-transfer capacitance, C_{RSS} (gate-to-drain capacitance), and maximum current, $I_{DS(MAX)}$. The gate drive voltage is set by the 6.35V GATEV_{CC} supply. Consequently, logic-level threshold MOSFETs must be used in LT8705A applications.

It is very important to consider power dissipation when selecting power MOSFETs. The most efficient circuit will use MOSFETs that dissipate the least amount of power. Power dissipation must be limited to avoid overheating that might damage the devices. For most buck-boost applications the M1 and M3 switches will have the highest power dissipation where M2 will have the lowest unless the output becomes shorted. In some cases it can be helpful to use two or more MOSFETs in parallel to reduce power dissipation in each device. This is most helpful when power is dominated by I^2R losses while the MOSFET is "on". The additional capacitance of connecting MOSFETs in parallel can sometimes slow down switching edge rates and consequently increase total switching power losses.

The following sections provide guidelines for calculating power consumption of the individual MOSFETs. From a known power dissipation, the MOSFET junction temperature can be obtained using the following formula:

$$T_J = T_A + P \bullet R_{TH(JA)}$$