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## FEATURES

- Software Programmable Features
  - Unipolar/Bipolar Conversion
  - Four Differential/Eight Single-Ended Inputs
  - MSB- or LSB-First Data Sequence
  - Variable Data Word Length
  - Power Shutdown
- Built-In Sample-and-Hold
- Single Supply 5V or  $\pm 5V$  Operation
- Direct Four-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- 50kHz Maximum Throughput Rate
- Available in 20-Lead PDIP and SO Wide Packages

## KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 13 $\mu$ s Max Over Temp
- Low Supply Current: 6.0mA

## DESCRIPTION

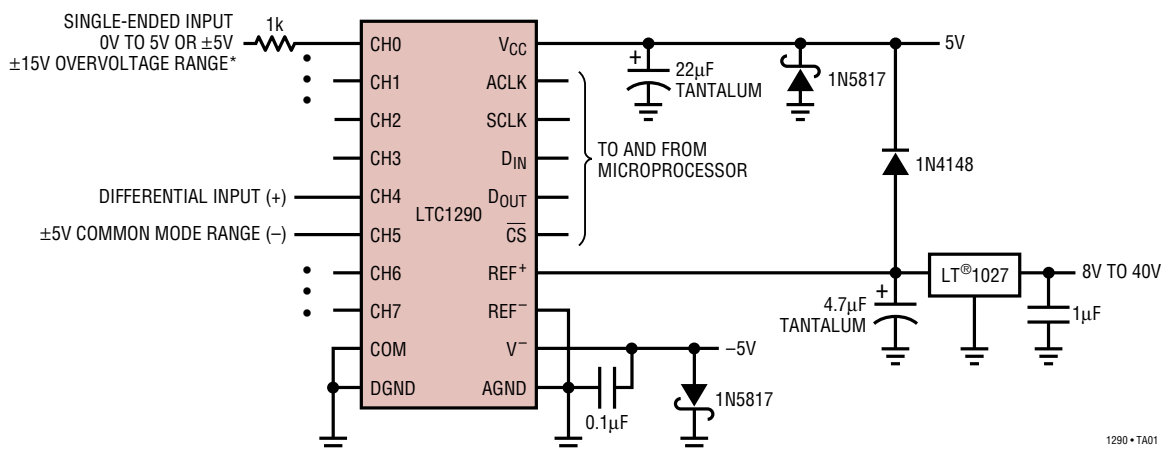
The LTC<sup>®</sup>1290 is a data acquisition component which contains a serial I/O successive approximation A/D converter. It uses LTCMOS<sup>™</sup> switched capacitor technology to perform either 12-bit unipolar or 11-bit plus sign bipolar A/D conversions. The 8-channel input multiplexer can be configured for either single-ended or differential inputs (or combinations thereof). An on-chip sample-and-hold is included for all single-ended input channels. When the LTC1290 is idle it can be powered down with a serial word in applications where low power consumption is desired.

The serial I/O is designed to be compatible with industry standard full duplex serial interfaces. It allows either MSB- or LSB-first data and automatically provides 2's complement output coding in the bipolar mode. The output data word can be programmed for a length of 8, 12 or 16 bits. This allows easy interface to shift registers and a variety of processors.

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## TYPICAL APPLICATION

**12-Bit 8-Channel Sampling Data Acquisition System**



\* FOR OVERVOLTAGE PROTECTION ON ONLY ONE CHANNEL LIMIT THE INPUT CURRENT TO 15mA. FOR OVERVOLTAGE PROTECTION ON MORE THAN ONE CHANNEL LIMIT THE INPUT CURRENT TO 7mA PER CHANNEL AND 28mA FOR ALL CHANNELS. (SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION SECTION.) CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED OR ANY OTHER CHANNEL IS OVERVOLTAGED ( $V_{IN} < V^-$  OR  $V_{IN} > V_{CC}$ ).

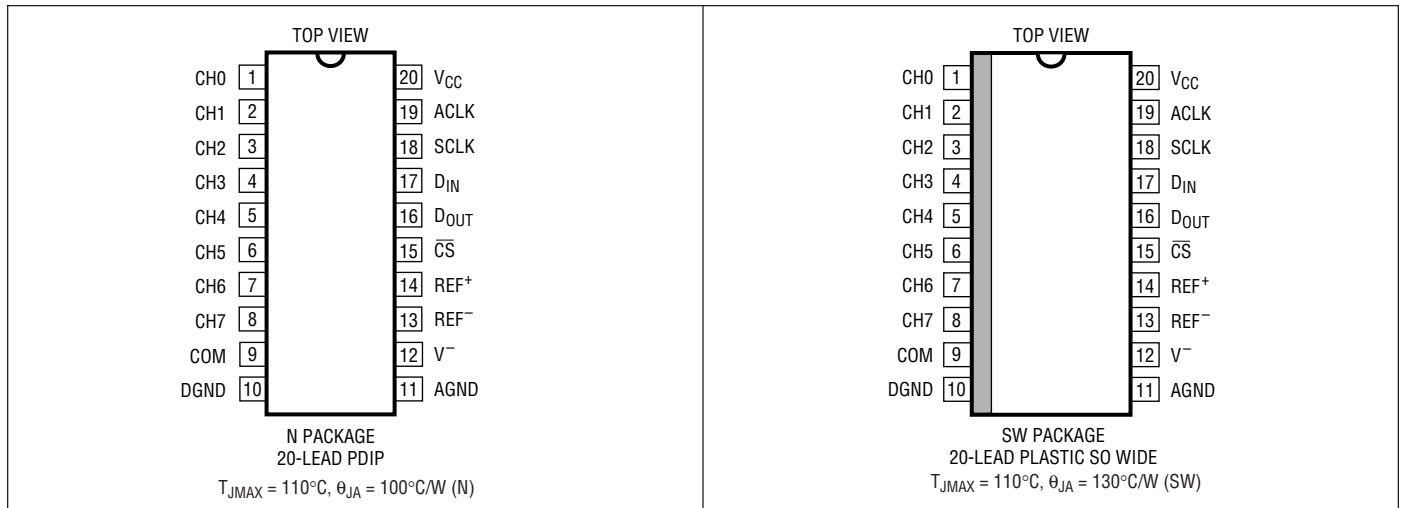
# LTC1290

## ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltage ( $V_{CC}$ ) to GND or  $V^-$  ..... 12V  
 Negative Supply Voltage ( $V^-$ ) ..... -6V to GND Voltage  
 Analog/Reference Inputs ..... ( $V^-$ ) -0.3V to  $V_{CC} + 0.3V$   
 Digital Inputs ..... -0.3V to 12V  
 Digital Outputs ..... -0.3V to  $V_{CC} + 0.3V$   
 Power Dissipation ..... 500mW

Operating Temperature Range  
 LTC1290BC, LTC1290CC, LTC1290DC .... 0°C to 70°C  
 LTC1290BI, LTC1290CI, LTC1290DI .... -40°C to 85°C  
 LTC1290BM, LTC1290CM,  
 LTC1290DM (**OBSOLETE**) ..... -55°C to 125°C  
 Storage Temperature Range ..... -65°C to 150°C  
 Lead Temperature (Soldering, 10 sec.) ..... 300°C

## PACKAGE/ORDER INFORMATION



| ORDER PART NUMBER  | N PART MARKING | ORDER PART NUMBER  | SW PART MARKING |
|--|----------------|--|-----------------|
| LTC1290BIN<br>LTC1290CIN<br>LTC1290DIN<br>LTC1290BCN<br>LTC1290CCN<br>LTC1290DCN   |                | LTC1290BCSW<br>LTC1290CCSW<br>LTC1290DCSW<br>LTC1290BISW<br>LTC1290CISW<br>LTC1290DISW |                 |
| J PACKAGE<br>20-LEAD CERAMIC DIP<br>$T_{JMAX} = 150^\circ\text{C}$ , $q_{JA} = 80^\circ\text{C/W}$ (J)<br>LTC1290BMJ<br>LTC1290CMJ<br>LTC1290DMJ<br>LTC1290BIJ<br>LTC1290CIJ<br>LTC1290DIJ<br><b>OBSOLETE PACKAGE</b><br>Consider N Package for Alternate Source |                |  |                 |

**Order Options** Tape and Reel: Add #TR  
 Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF  
 Lead Free Part Marking: <http://www.linear.com/leadfree/>

\*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.



## CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

| PARAMETER  | CONDITIONS                          |   | LTC1290B  |     |      | LTC1290C  |     |      | LTC1290D  |     |       | UNITS |
|--|-------------------------------------|---|---|-----|------|---|-----|------|---|-----|-------|-------|
|  |                                     |   | MIN   | TYP | MAX  | MIN   | TYP | MAX  | MIN   | TYP | MAX   |       |
| Offset Error   | (Note 4)                            | ● |   |     | ±1.5 |   |     | ±1.5 |   |     | ±1.5  | LSB   |
| Linearity Error (INL)  | (Notes 4, 5)                        | ● |   |     | ±0.5 |   |     | ±0.5 |   |     | ±0.75 | LSB   |
| Gain Error   | (Note 4)                            | ● |   |     | ±0.5 |   |     | ±1.0 |   |     | ±4.0  | LSB   |
| Minimum Resolution for Which No Missing Codes are Guaranteed |                                     | ● |   |     | 12   |   |     | 12   |   |     | 12    | Bits  |
| Analog and REF Input Range                                   | (Note 7)                            |   | $(V^-) - 0.05\text{V to } V_{\text{CC}} + 0.05\text{V}$ |     |      | $(V^-) - 0.05\text{V to } V_{\text{CC}} + 0.05\text{V}$ |     |      | $(V^-) - 0.05\text{V to } V_{\text{CC}} + 0.05\text{V}$ |     |       | V     |
| On Channel Leakage Current (Note 8)                          | On Channel = 5V<br>Off Channel = 0V | ● |   |     | ±1   |   |     | ±1   |   |     | ±1    | μA    |
|  | On Channel = 0V<br>Off Channel = 5V | ● |   |     | ±1   |   |     | ±1   |   |     | ±1    | μA    |
| Off Channel Leakage Current (Note 8)                         | On Channel = 5V<br>Off Channel = 0V | ● |   |     | ±1   |   |     | ±1   |   |     | ±1    | μA    |
|  | On Channel = 0V<br>Off Channel = 5V | ● |   |     | ±1   |   |     | ±1   |   |     | ±1    | μA    |

## AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

| SYMBOL            | PARAMETER  | CONDITIONS                           | LTC1290B/LTC1290C/LTC1290D   |                       |     | UNITS       |    |
|-------------------|--|--------------------------------------|--|-----------------------|-----|-------------|----|
|                   |  |                                      | MIN  | TYP                   | MAX |             |    |
| $f_{\text{SCLK}}$ | Shift Clock Frequency  | $V_{\text{CC}} = 5\text{V}$ (Note 6) | 0  |                       | 2.0 | MHz         |    |
| $f_{\text{ACLK}}$ | A/D Clock Frequency  | $V_{\text{CC}} = 5\text{V}$ (Note 6) | (Note 10)  |                       | 4.0 | MHz         |    |
| $t_{\text{ACC}}$  | Delay Time from $\overline{\text{CS}}\downarrow$ to $\text{D}_{\text{OUT}}$ Data Valid | (Note 9)                             |  | 2                     |     | ACLK Cycles |    |
| $t_{\text{SMPL}}$ | Analog Input Sample Time   | See Operating Sequence               |  | 7                     |     | SCLK Cycles |    |
| $t_{\text{CONV}}$ | Conversion Time  | See Operating Sequence               |  | 52                    |     | ACLK Cycles |    |
| $t_{\text{CYC}}$  | Total Cycle Time   | See Operating Sequence (Note 6)      | 12 SCLK + 56 ACLK  |                       |     | Cycles      |    |
| $t_{\text{dDO}}$  | Delay Time, SCLK $\downarrow$ to $\text{D}_{\text{OUT}}$ Data Valid                    | See Test Circuits                    | LTC1290BC, LTC1290CC<br>LTC1290DC, LTC1290BI<br>LTC1290CI, LTC1290DI | ●                     | 130 | 220         | ns |
|                   |  |                                      | LTC1290BM, LTC1290CM<br>LTC1290DM<br>(OBSOLETE)                      | ●                     | 180 | 270         | ns |
| $t_{\text{dis}}$  | Delay Time, $\overline{\text{CS}}\uparrow$ to $\text{D}_{\text{OUT}}$ Hi-Z             | See Test Circuits                    | ●  | 70                    | 100 | ns          |    |
| $t_{\text{en}}$   | Delay Time, 2nd ACLK $\downarrow$ to $\text{D}_{\text{OUT}}$ Enabled                   | See Test Circuits                    | ●  | 130                   | 200 | ns          |    |
| $t_{\text{hCS}}$  | Hold Time, $\overline{\text{CS}}$ After Last SCLK $\downarrow$                         | $V_{\text{CC}} = 5\text{V}$ (Note 6) |  | 0                     |     | ns          |    |
| $t_{\text{hDI}}$  | Hold Time, $\text{D}_{\text{IN}}$ After SCLK $\uparrow$                                | $V_{\text{CC}} = 5\text{V}$ (Note 6) |  | 50                    |     | ns          |    |
| $t_{\text{hDO}}$  | Time Output Data Remains Valid After SCLK $\downarrow$                                 |                                      |  | 50                    |     | ns          |    |
| $t_{\text{f}}$    | $\text{D}_{\text{OUT}}$ Fall Time  | See Test Circuits                    | ●  | 65                    | 130 | ns          |    |
| $t_{\text{r}}$    | $\text{D}_{\text{OUT}}$ Rise Time  | See Test Circuits                    | ●  | 25                    | 50  | ns          |    |
| $t_{\text{suDI}}$ | Setup Time, $\text{D}_{\text{IN}}$ Stable Before SCLK $\uparrow$                       | $V_{\text{CC}} = 5\text{V}$ (Note 6) |  | 50                    |     | ns          |    |
| $t_{\text{suCS}}$ | Setup Time, $\overline{\text{CS}}\downarrow$ Before Clocking in First Address Bit      | (Notes 6, 9)                         |  | 2 ACLK Cycles + 100ns |     |             |    |
| $t_{\text{WHCS}}$ | $\overline{\text{CS}}$ High Time During Conversion                                     | $V_{\text{CC}} = 5\text{V}$ (Note 6) |  | 52                    |     | ACLK Cycles |    |
| $C_{\text{IN}}$   | Input Capacitance  | Analog Inputs On Channel             |  | 100                   |     | pF          |    |
|                   |  | Analog Inputs Off Channel            |  | 5                     |     | pF          |    |
|                   |  | Digital Inputs                       |  | 5                     |     | pF          |    |

## DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

| SYMBOL       | PARAMETER                 | CONDITIONS  | LTC1290B/LTC1290C/LTC1290D |   |  | UNITS         |               |    |               |
|--------------|---------------------------|---|----------------------------|---|--|---------------|---------------|----|---------------|
|              |                           |   | MIN                        | TYP   | MAX  |               |               |    |               |
| $V_{IH}$     | High Level Input Voltage  | $V_{CC} = 5.25\text{V}$   | ●                          | 2.0   |  | V             |               |    |               |
| $V_{IL}$     | Low Level Input Voltage   | $V_{CC} = 4.75\text{V}$   | ●                          |   | 0.8  | V             |               |    |               |
| $I_{IH}$     | High Level Input Current  | $V_{IN} = V_{CC}$   | ●                          |   | 2.5  | $\mu\text{A}$ |               |    |               |
| $I_{IL}$     | Low Level Input Current   | $V_{IN} = 0\text{V}$  | ●                          |   | -2.5   | $\mu\text{A}$ |               |    |               |
| $V_{OH}$     | High Level Output Voltage | $V_{CC} = 4.75\text{V}$<br>$I_O = 10\mu\text{A}$<br>$I_O = 360\mu\text{A}$                              | ●                          |   | 4.7  | V             |               |    |               |
|              |                           |   |                            | 2.4   | 4.0  |               |               |    |               |
| $V_{OL}$     | Low Level Output Voltage  | $V_{CC} = 4.75\text{V}$<br>$I_O = 1.6\text{mA}$   | ●                          |   | 0.4  | V             |               |    |               |
| $I_{OZ}$     | High-Z Output Leakage     | $V_{OUT} = V_{CC}$ , $\overline{\text{CS}}$ High<br>$V_{OUT} = 0\text{V}$ , $\overline{\text{CS}}$ High | ●                          |   | 3  | $\mu\text{A}$ |               |    |               |
|              |                           |   |                            | ●   | -3   |               |               |    |               |
| $I_{SOURCE}$ | Output Source Current     | $V_{OUT} = 0\text{V}$   |                            |   | -20  | $\text{mA}$   |               |    |               |
| $I_{SINK}$   | Output Sink Current       | $V_{OUT} = V_{CC}$  |                            |   | 20   | $\text{mA}$   |               |    |               |
| $I_{CC}$     | Positive Supply Current   | $\overline{\text{CS}}$ High   | ●                          |   | 6  | 12            | $\text{mA}$   |    |               |
|              |                           |   |                            | $\overline{\text{CS}}$ High<br>Power Shutdown<br>ACLK Off | LTC1290BC, LTC1290CC<br>LTC1290DC, LTC1290BI<br>LTC1290CI, LTC1290DI |               | 5             | 10 | $\mu\text{A}$ |
|              |                           |   |                            |   | LTC1290BM, LTC1290CM<br>LTC1290DM<br>(OBSOLETE)                      | ●             |               | 5  | 15            |
| $I_{REF}$    | Reference Current         | $V_{REF} = 5\text{V}$   | ●                          |   | 10   | 50            | $\mu\text{A}$ |    |               |
| $I^-$        | Negative Supply Current   | $\overline{\text{CS}}$ High   | ●                          |   | 1  | 50            | $\mu\text{A}$ |    |               |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

**Note 2:** All voltage values are with respect to ground with DGND, AGND and  $\text{REF}^-$  wired together (unless otherwise noted).

**Note 3:**  $V_{CC} = 5\text{V}$ ,  $V_{REF+} = 5\text{V}$ ,  $V_{REF-} = 0\text{V}$ ,  $V^- = 0\text{V}$  for unipolar mode and  $-5\text{V}$  for bipolar mode,  $\text{ACLK} = 4.0\text{MHz}$  unless otherwise specified.

**Note 4:** These specs apply for both unipolar and bipolar modes. In bipolar mode, one LSB is equal to the bipolar input span ( $2V_{REF}$ ) divided by 4096. For example, when  $V_{REF} = 5\text{V}$ ,  $1\text{LSB (bipolar)} = 2(5\text{V})/4096 = 2.44\text{mV}$ .

**Note 5:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 6:** Recommended operating conditions.

**Note 7:** Two on-chip diodes are tied to each reference and analog input which will conduct for reference or analog input voltages one diode drop below  $V^-$  or one diode drop above  $V_{CC}$ . Be careful during testing at low

$V_{CC}$  levels (4.5V), as high level reference or analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the reference or analog input does not exceed the supply voltage by more than 50mV, the output code will be correct. To achieve an absolute 0V to 5V input voltage range will therefore require a minimum supply voltage of 4.950V over initial tolerance, temperature variations and loading.

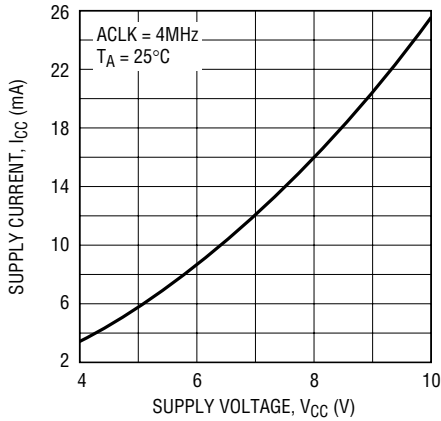
**Note 8:** Channel leakage current is measured after the channel selection.

**Note 9:** To minimize errors caused by noise at the chip select input, the internal circuitry waits for two ACLK falling edge after a chip select falling edge is detected before responding to control input signals. Therefore, no attempt should be made to clock an address in or data out until the minimum chip select setup time has elapsed.

**Note 10:** Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it's recommended that  $f_{\text{ACLK}} \geq 125\text{kHz}$  at  $85^\circ\text{C}$  and  $f_{\text{ACLK}} \geq 15\text{kHz}$  at  $25^\circ\text{C}$ .

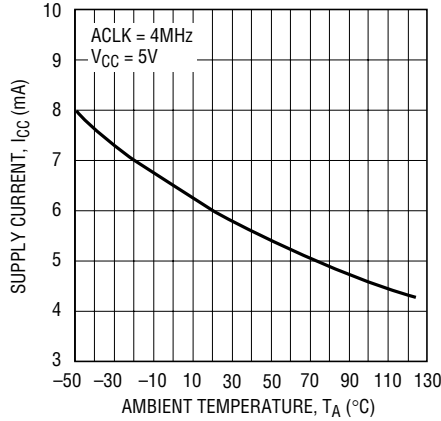
# TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



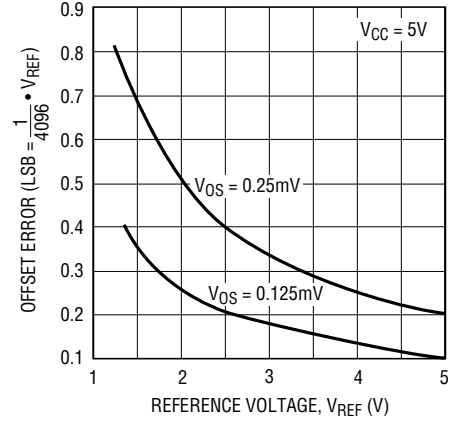
1290 • TPC01

Supply Current vs Temperature



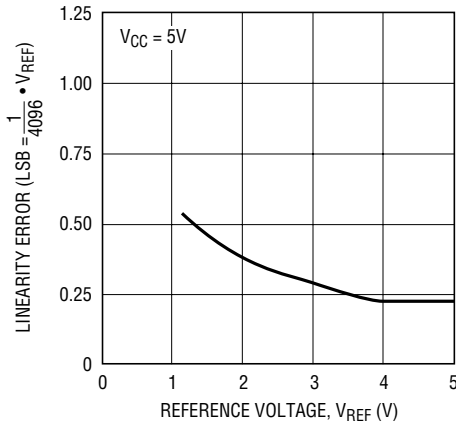
LT1290 • TPC02

Unadjusted Offset Voltage vs Reference Voltage



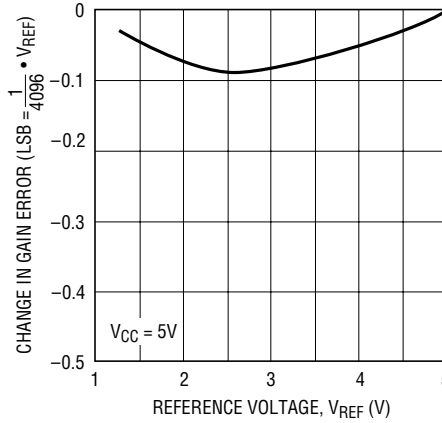
1290 • TPC03

Change in Linearity vs Reference Voltage



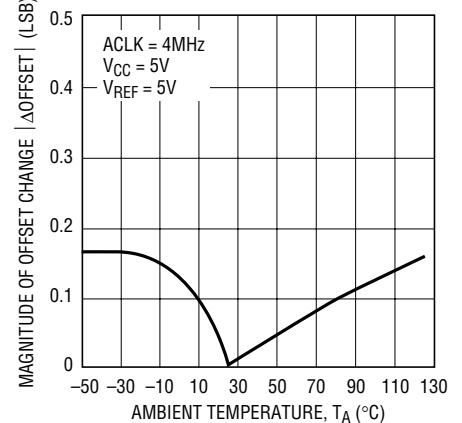
1290 • TPC04

Change in Gain vs Reference Voltage



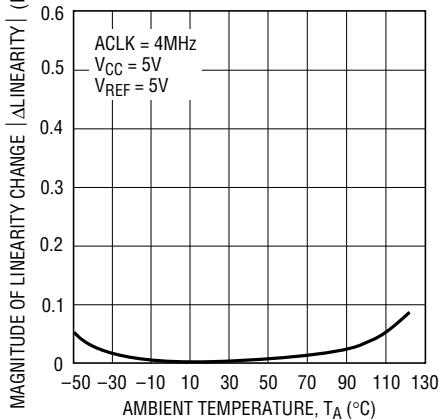
1290 • TPC05

Change in Offset vs Temperature



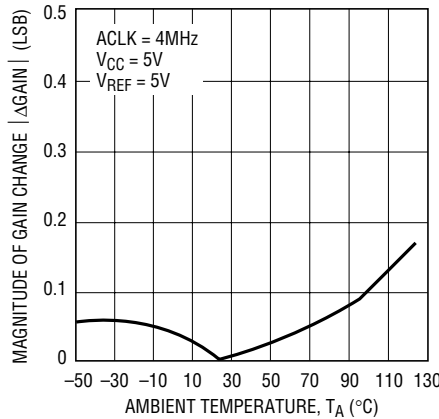
1290 • TPC06

Change in Linearity Error vs Temperature



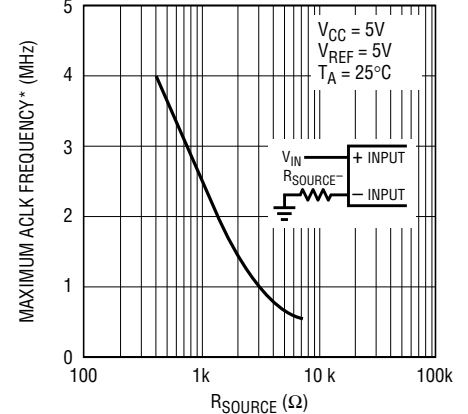
1290 • TPC07

Change in Gain Error vs Temperature



1290 • TPC08

Maximum ACLK Frequency vs Source Resistance

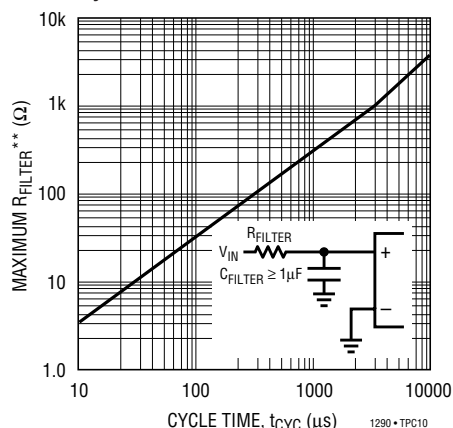


1290 • TPC09

\* MAXIMUM ACLK FREQUENCY REPRESENTS THE ACLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 4MHz VALUE IS FIRST DETECTED.

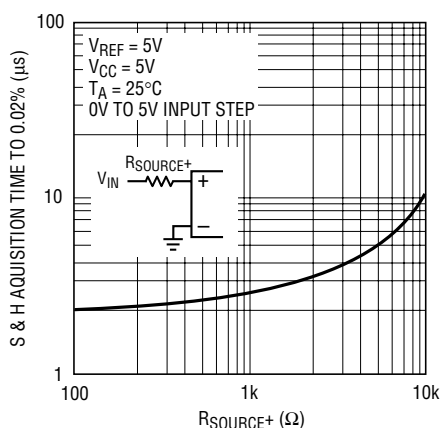
## TYPICAL PERFORMANCE CHARACTERISTICS

**Maximum Filter Resistor vs Cycle Time**



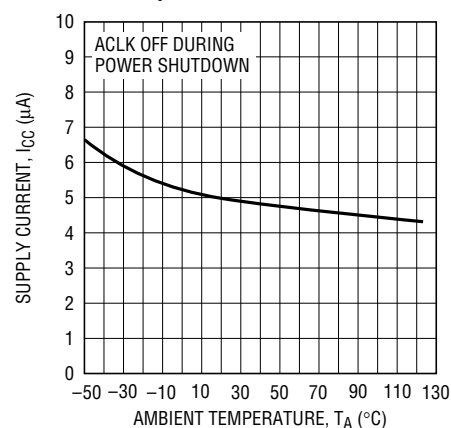
\*\* MAXIMUM  $R_{FILTER}$  REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL-SCALE ERROR FROM ITS VALUE AT  $R_{FILTER} = 0$  IS FIRST DETECTED.

**Sample-and-Hold Acquisition Time vs Source Resistance**



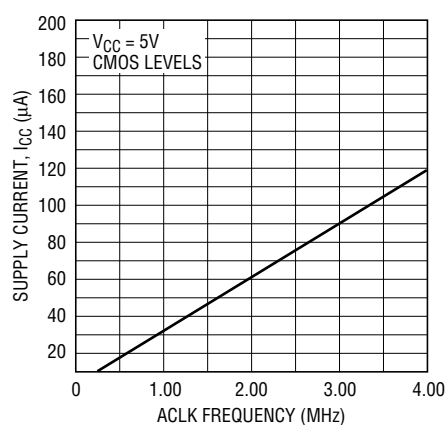
LTC1290 • TPC11

**Supply Current (Power Shutdown) vs Temperature**



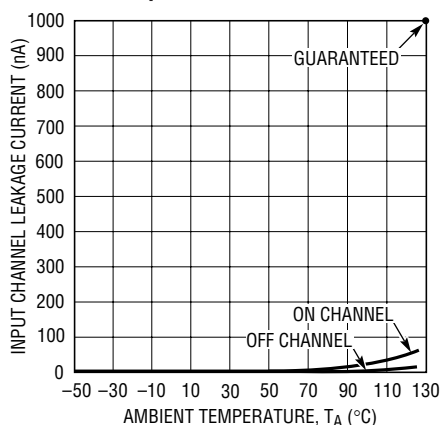
1290 • TPC12

**Supply Current (Power Shutdown) vs ACLK**



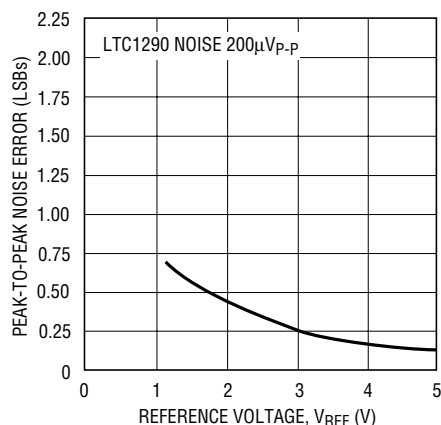
1290 • TPC13

**Input Channel Leakage Current vs Temperature**



1290 • TPC14

**Noise Error vs Reference Voltage**



1290 • TPC15

## PIN FUNCTIONS

**CH0 to CH7 (Pin 1 to Pin 8):** Analog Inputs. The analog inputs must be free of noise with respect to AGND.

**COM (Pin 9):** Common. The common pin defines the zero reference point for all single-ended inputs. It must be free of noise and is usually tied to the analog ground plane.

**DGND (Pin 10):** Digital Ground. This is the ground for the internal logic. Tie to the ground plane.

**AGND (Pin 11):** Analog Ground. AGND should be tied directly to the analog ground plane.

**V<sup>-</sup> (Pin 12):** Negative Supply. Tie V<sup>-</sup> to most negative potential in the circuit. (Ground in single supply applications.)

**REF<sup>-</sup>, REF<sup>+</sup> (Pins 13, 14):** Reference Inputs. The reference inputs must be kept free of noise with respect to AGND.

**CS (Pin 15):** Chip Select Input. A logic low on this input enables data transfer.

**DO<sub>OUT</sub> (Pin 16):** Digital Data Output. The A/D conversion result is shifted out of this output.



## PIN FUNCTIONS

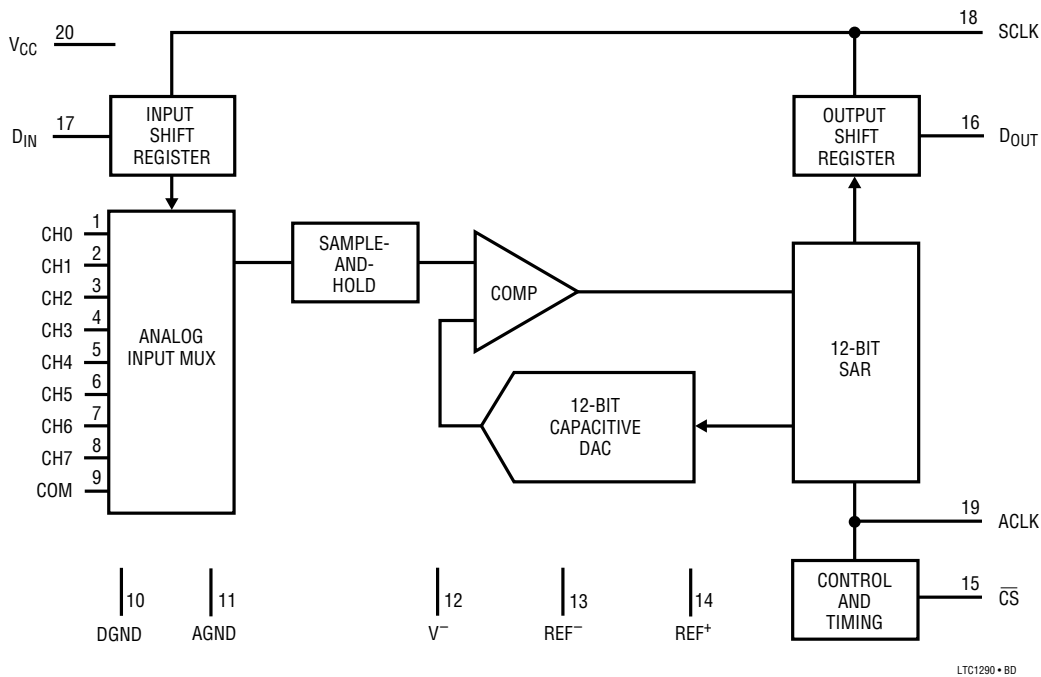
**D<sub>IN</sub> (Pin 17):** Digital Data Input. The A/D configuration word is shifted into this input after  $\overline{CS}$  is recognized.

**SCLK (Pin 18):** Shift Clock. This clock synchronizes the serial data transfer.

**ACLK (Pin 19):** A/D Conversion Clock. This clock controls the A/D conversion process.

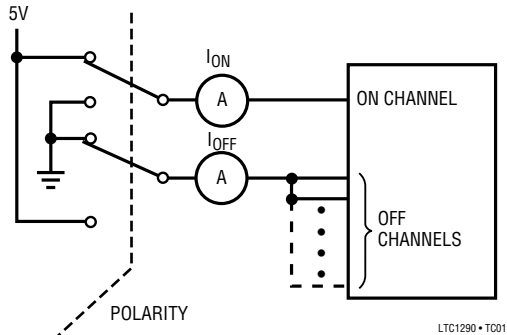
**V<sub>CC</sub> (Pin 20):** Positive Supply. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

## BLOCK DIAGRAM

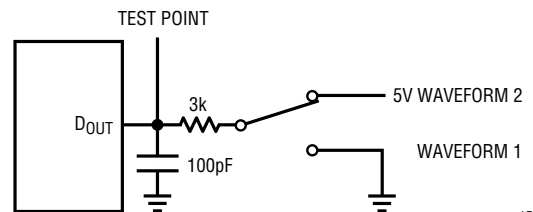


## TEST CIRCUITS

On and Off Channel Leakage Current

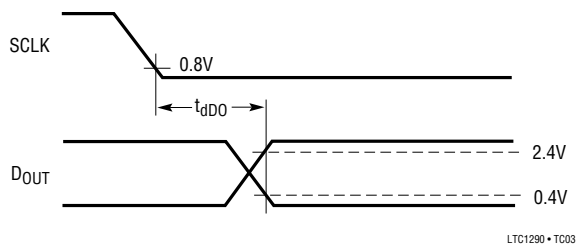


Load Circuit for  $t_{dis}$  and  $t_{en}$

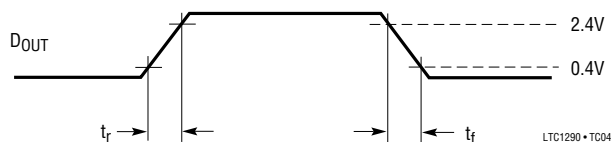


# TEST CIRCUITS

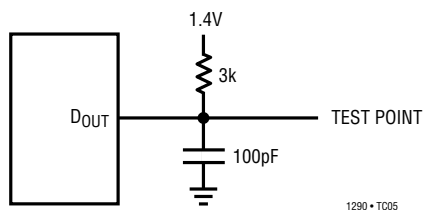
Voltage Waveforms for  $D_{OUT}$  Delay Time,  $t_{dDO}$



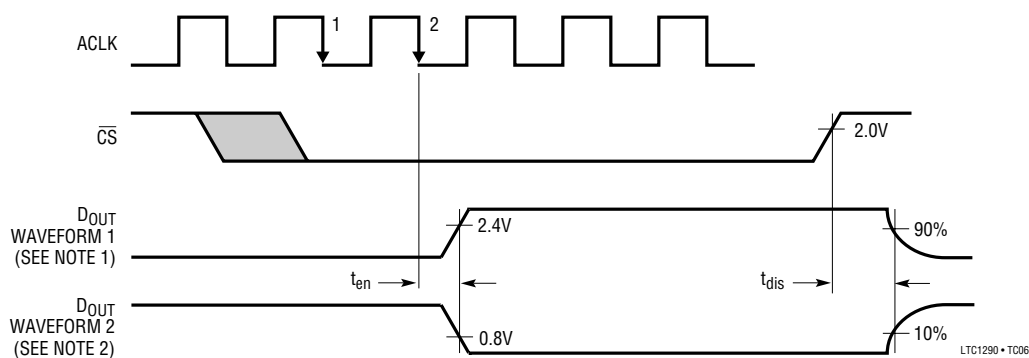
Voltage Waveform for  $D_{OUT}$  Rise and Fall Times,  $t_r$ ,  $t_f$



Load Circuit for  $t_{dDO}$ ,  $t_r$  and  $t_f$



Voltage Waveforms for  $t_{en}$  and  $t_{dis}$



NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.  
 NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

## APPLICATIONS INFORMATION

The LTC1290 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, full duplex serial interface
5. Control and timing logic

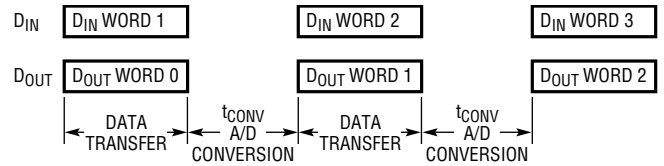
### DIGITAL CONSIDERATIONS

#### Serial Interface

The LTC1290 communicates with microprocessors and other external circuitry via a synchronous, full duplex, four-wire serial interface (see Operating Sequence). The shift clock (SCLK) synchronizes the data transfer with each bit being transmitted on the falling SCLK edge and captured on the rising SCLK edge in both transmitting and receiving systems. The data is transmitted and received simultaneously (full duplex).

Data transfer is initiated by a falling chip select ( $\overline{CS}$ ) signal. After the falling  $\overline{CS}$  is recognized, an 8-bit input word is shifted into the  $D_{IN}$  input which configures the LTC1290 for the next conversion. Simultaneously, the result of the

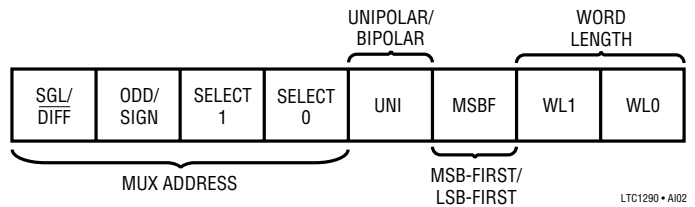
previous conversion is output on the  $D_{OUT}$  line. At the end of the data exchange the requested conversion begins and  $\overline{CS}$  should be brought high. After  $t_{CONV}$ , the conversion is complete and the results will be available on the next data transfer cycle. As shown below, the result of a conversion is delayed by one  $\overline{CS}$  cycle from the input word requesting it.



LTC1290 • A101

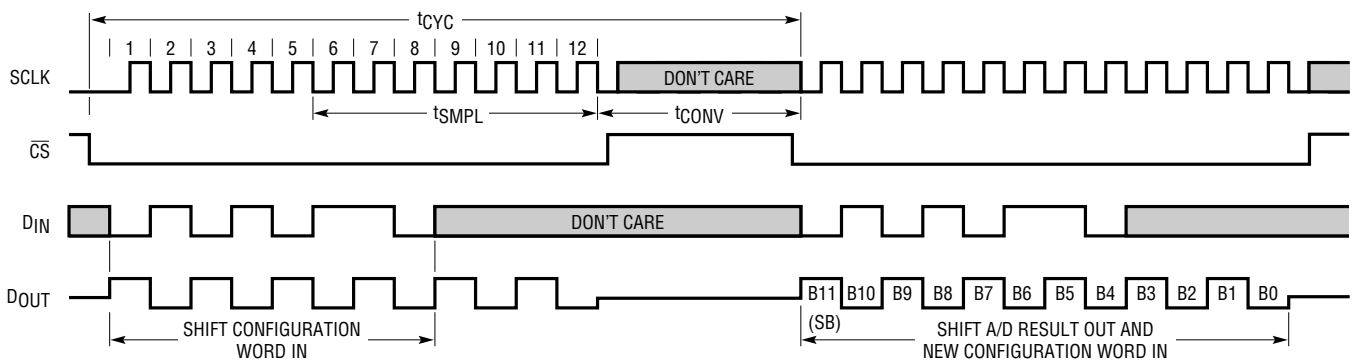
#### Input Data Word

The LTC1290 8-bit data word is clocked into the  $D_{IN}$  input on the first eight rising SCLK edges after chip select is recognized. Further inputs on the  $D_{IN}$  pin are then ignored until the next  $\overline{CS}$  cycle. The eight bits of the input word are defined as follows:



LTC1290 • A102

#### Operating Sequence (Example: Differential Inputs (CH3-CH2), Bipolar, MSB-First and 12-Bit Word Length)



LTC1290 • A103

# APPLICATIONS INFORMATION

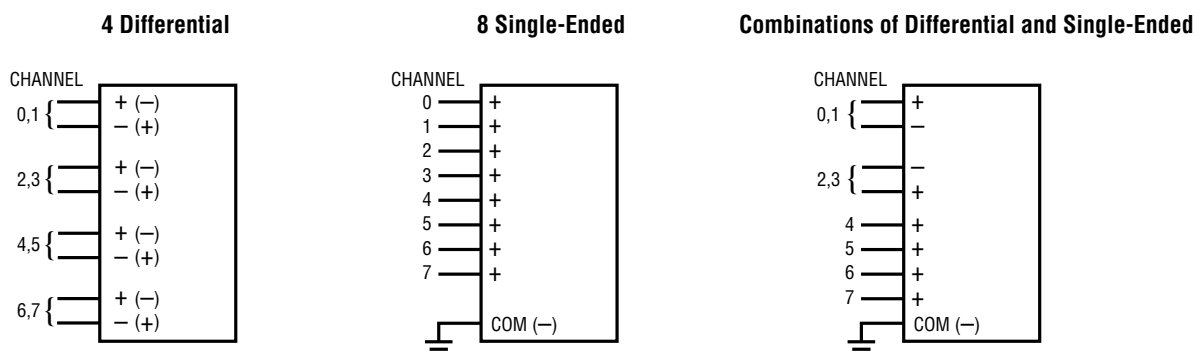
## MUX Address

The first four bits of the input word assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of Table 1. Note that in differential

mode ( $SGL/DIFF = 0$ ) measurements are limited to four adjacent input pairs with either polarity. In single-ended mode, all input channels are measured with respect to COM.

Table 1. Multiplexer Channel Selection

| MUX ADDRESS |          |          |   | DIFFERENTIAL CHANNEL SELECTION |   |   |   |   |   |   | MUX ADDRESS |          |          |          | SINGLE-ENDED CHANNEL SELECTION |   |   |   |   |   |   |   |   |     |
|-------------|----------|----------|---|--------------------------------|---|---|---|---|---|---|-------------|----------|----------|----------|--------------------------------|---|---|---|---|---|---|---|---|-----|
| SGL/DIFF    | ODD SIGN | SELECT 1 | 0 | 0                              | 1 | 2 | 3 | 4 | 5 | 6 | 7           | SGL/DIFF | ODD SIGN | SELECT 1 | 0                              | 0 | 1 | 2 | 3 | 4 | 5 | 6 | 7 | COM |
| 0           | 0        | 0        | 0 | +                              | - |   |   |   |   |   |             | 1        | 0        | 0        | 0                              | + |   |   |   |   |   |   |   | -   |
| 0           | 0        | 0        | 1 |                                |   | + | - |   |   |   |             | 1        | 0        | 0        | 1                              |   |   | + |   |   |   |   |   | -   |
| 0           | 0        | 1        | 0 |                                |   |   |   | + | - |   |             | 1        | 0        | 1        | 0                              |   |   |   |   | + |   |   |   | -   |
| 0           | 0        | 1        | 1 |                                |   |   |   |   |   | + | -           | 1        | 0        | 1        | 1                              |   |   |   |   |   |   | + |   | -   |
| 0           | 1        | 0        | 0 | -                              | + |   |   |   |   |   |             | 1        | 1        | 0        | 0                              |   | + |   |   |   |   |   |   | -   |
| 0           | 1        | 0        | 1 |                                |   | - | + |   |   |   |             | 1        | 1        | 0        | 1                              |   |   | + |   |   |   |   |   | -   |
| 0           | 1        | 1        | 0 |                                |   |   |   | - | + |   |             | 1        | 1        | 1        | 0                              |   |   |   |   |   | + |   |   | -   |
| 0           | 1        | 1        | 1 |                                |   |   |   |   |   | - | +           | 1        | 1        | 1        | 1                              |   |   |   |   |   |   | + |   | -   |



### Changing the MUX Assignment “On the Fly”

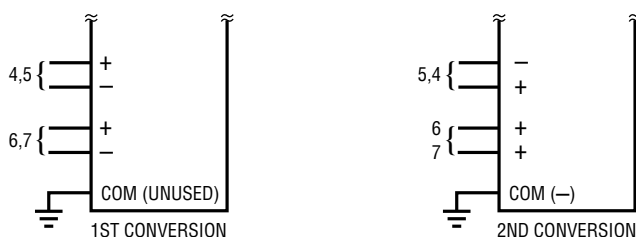


Figure 1. Examples of Multiplexer Options on the LTC1290

LTC1290 • F01

# APPLICATIONS INFORMATION

## Unipolar/Bipolar (UNI)

The fifth input bit (UNI) determines whether the conversion will be unipolar or bipolar. When UNI is a logical one, a unipolar conversion will be performed on the selected

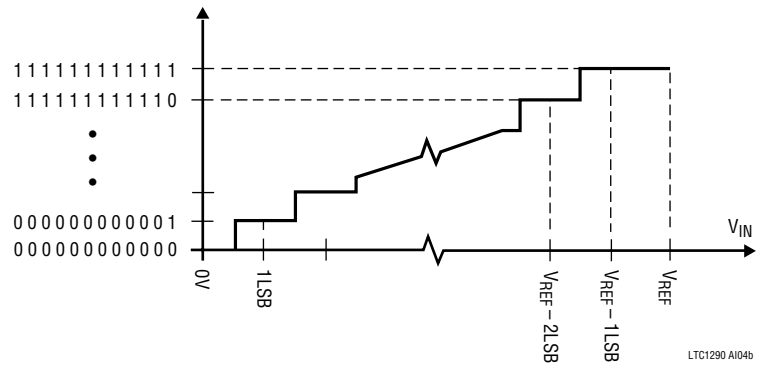
input voltage. When UNI is a logical zero, a bipolar conversion will result. The input span and code assignment for each conversion type are shown in the figures below.

Unipolar Output Code (UNI = 1)

| OUTPUT CODE  | INPUT VOLTAGE           | INPUT VOLTAGE (V <sub>REF</sub> = 5V) |
|--------------|-------------------------|---------------------------------------|
| 111111111111 | V <sub>REF</sub> - 1LSB | 4.9988V                               |
| 111111111110 | V <sub>REF</sub> - 2LSB | 4.9976V                               |
| ⋮            | ⋮                       | ⋮                                     |
| 000000000001 | 1LSB                    | 0.0012V                               |
| 000000000000 | 0V                      | 0V                                    |

LTC1290-AI04a

Unipolar Transfer Curve (UNI = 1)



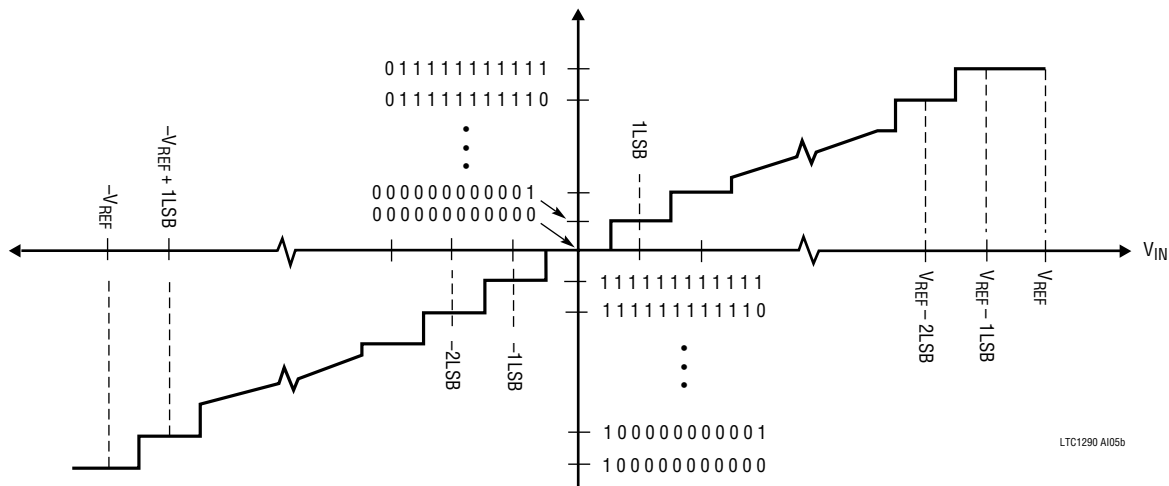
LTC1290 AI04b

Bipolar Output Code (UNI = 0)

| OUTPUT CODE  | INPUT VOLTAGE           | INPUT VOLTAGE (V <sub>REF</sub> = 5V) | OUTPUT CODE  | INPUT VOLTAGE               | INPUT VOLTAGE (V <sub>REF</sub> = 5V) |
|--------------|-------------------------|---------------------------------------|--------------|-----------------------------|---------------------------------------|
| 011111111111 | V <sub>REF</sub> - 1LSB | 4.9976V                               | 111111111111 | -1LSB                       | -0.0024V                              |
| 011111111110 | V <sub>REF</sub> - 2LSB | 4.9851V                               | 111111111110 | -2LSB                       | -0.0048V                              |
| ⋮            | ⋮                       | ⋮                                     | ⋮            | ⋮                           | ⋮                                     |
| 000000000001 | 1LSB                    | 0.0024V                               | 100000000001 | -(V <sub>REF</sub> ) + 1LSB | -4.9976V                              |
| 000000000000 | 0V                      | 0V                                    | 100000000000 | -(V <sub>REF</sub> )        | -5.0000V                              |

LTC1290 AI05a

Bipolar Transfer Curve (UNI = 0)



LTC1290 AI05b



## APPLICATIONS INFORMATION

### MSB-First/LSB-First Format (MSBF)

The output data of the LTC1290 is programmed for MSB-first or LSB-first sequence using the MSBF bit. For MSB first output data the input word clocked to the LTC1290 should always contain a logical one in the sixth bit location (MSBF bit). Likewise for LSB-first output data the input word clocked to the LTC1290 should always contain a zero in the MSBF bit location. The MSBF bit affects only the order of the output data word. The order of the input word is unaffected by this bit.

| MSBF | OUTPUT FORMAT |
|------|---------------|
| 0    | LSB First     |
| 1    | MSB First     |

### Word Length (WL1, WLO) and Power Shutdown

The last two bits of the input word (WL1 and WLO) program the output data word length and the power shutdown feature of the LTC1290. Word lengths of 8, 12 or 16 bits can be selected according to the following table. The WL1 and WLO bits in a given  $D_{IN}$  word control the length of the present, not the next,  $D_{OUT}$  word. WL1 and WLO are never “don’t cares” and must be set for the correct  $D_{OUT}$  word length even when a “dummy”  $D_{IN}$  word is sent. On any transfer cycle, the word length should be made equal to the number of SCLK cycles sent by the MPU. Power down will occur when  $WL1 = 0$  and  $WLO = 1$  is selected. The previous conversion result will be clocked out as a 10 bit word so a “dummy” conversion is required before powering down the LTC1290. Conversions are

resumed once  $\overline{CS}$  goes low or an SCLK is applied, if  $\overline{CS}$  is already low.

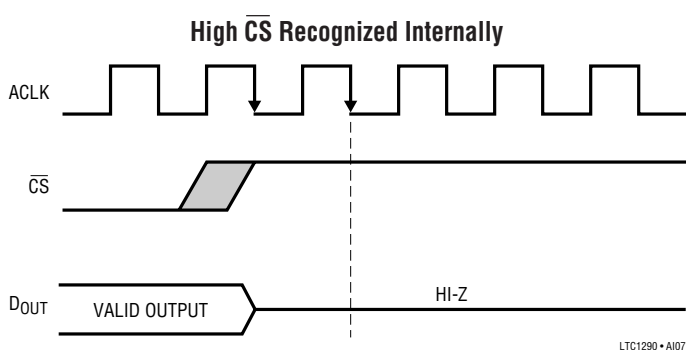
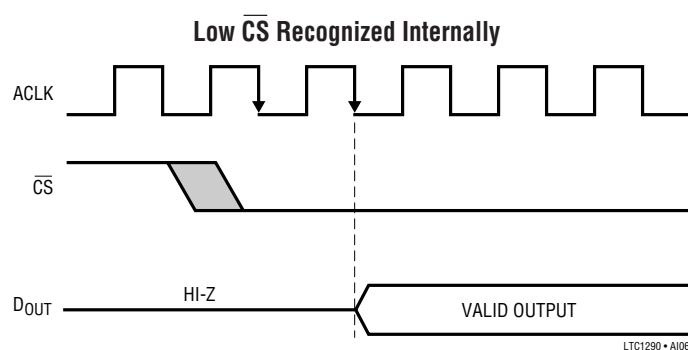
| WL1 | WLO | OUTPUT WORD LENGTH |
|-----|-----|--------------------|
| 0   | 0   | 8-Bits             |
| 0   | 1   | Power Shutdown     |
| 1   | 0   | 12-Bits            |
| 1   | 1   | 16-Bits            |

### Deglitcher

A deglitching circuit has been added to the Chip Select input of the LTC1290 to minimize the effects of errors caused by noise on that input. This circuit ignores changes in state on the  $\overline{CS}$  input that are shorter in duration than one ACLK cycle. After a change of state on the  $\overline{CS}$  input, the LTC1290 waits for two falling edge of the ACLK before recognizing a valid chip select. One indication of  $\overline{CS}$  recognition is the  $D_{OUT}$  line becoming active (leaving the Hi-Z state). Note that the deglitching applies to both the rising and falling  $\overline{CS}$  edges.

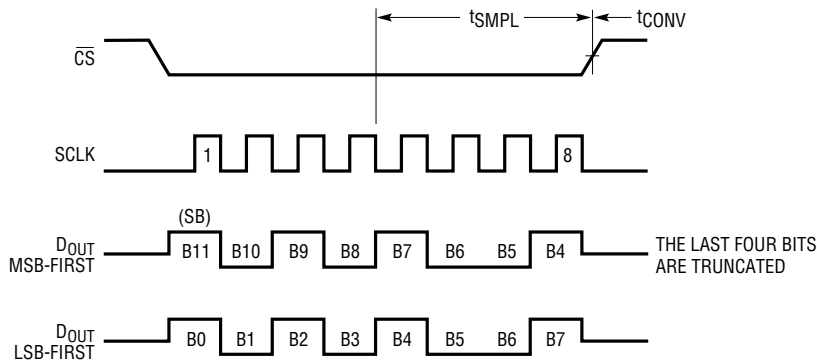
### $\overline{CS}$ Low During Conversion

In the normal mode of operation,  $\overline{CS}$  is brought high during the conversion time. The serial port ignores any SCLK activity while  $\overline{CS}$  is high. The LTC1290 will also operate with  $\overline{CS}$  low during the conversion. In this mode, SCLK must remain low during the conversion as shown in the following figure. After the conversion is complete, the  $D_{OUT}$  line will become active with the first output bit. Then the data transfer can begin as normal.

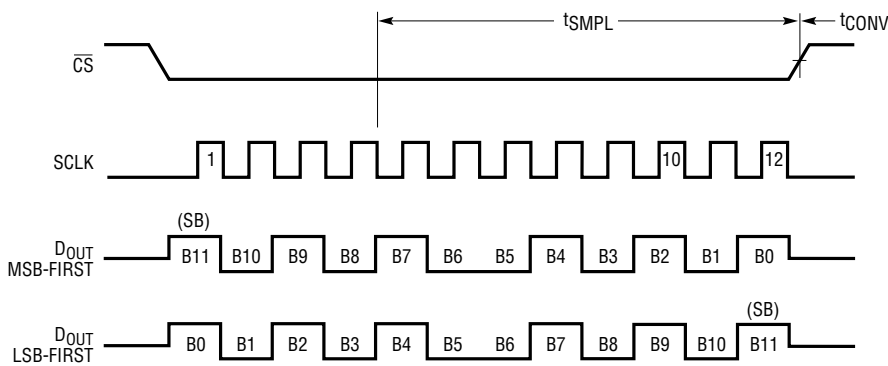


# APPLICATIONS INFORMATION

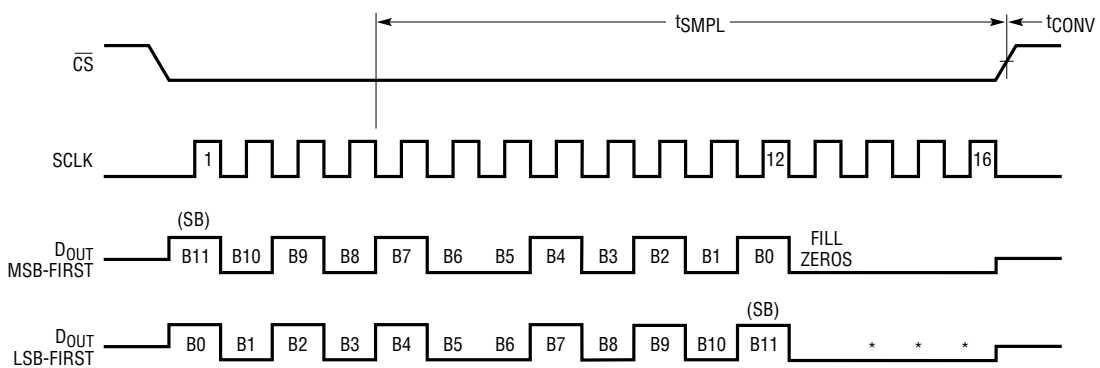
## 8-Bit Word Length



## 12-Bit Word Length



## 16-Bit Word Length



\* IN UNIPOLAR MODE, THESE BITS ARE FILLED WITH ZEROS.  
 IN BIPOLAR MODE, THE SIGN BIT IS EXTENDED INTO THESE LOCATIONS.

LTC1290 F02

Figure 2. Data Output ( $D_{OUT}$ ) Timing with Different Word Lengths

## APPLICATIONS INFORMATION

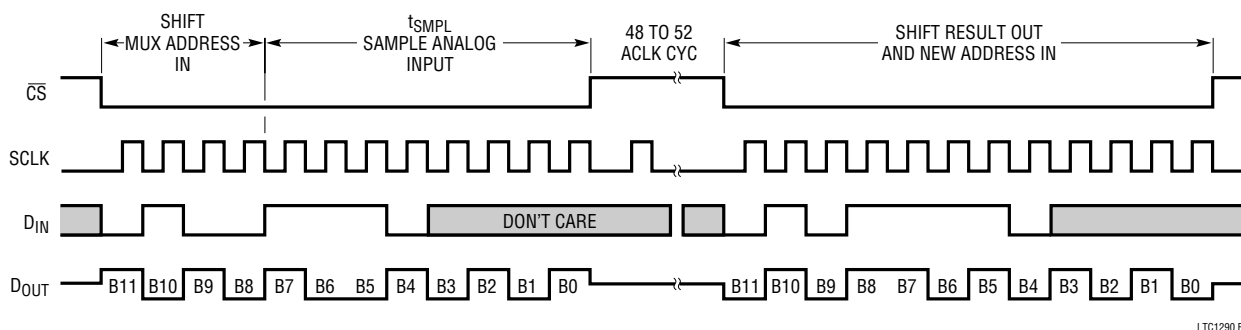


Figure 3.  $\overline{CS}$  High During Conversion

LTC1290 F03

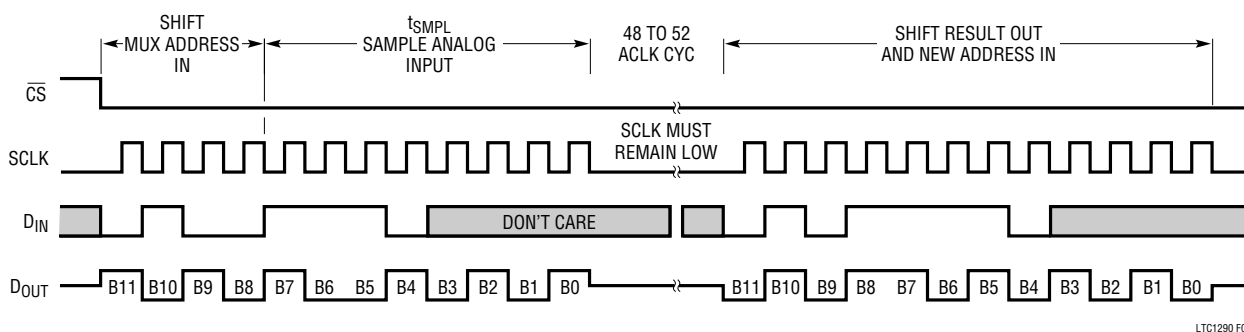


Figure 4.  $\overline{CS}$  Low During Conversion ( $\overline{CS}$  Must go High to Low Once to Insure Proper Operation in this Mode)

LTC1290 F04

### Microprocessor Interfaces

The LTC1290 can interface directly (without external hardware) to most popular microprocessor (MPU) synchronous serial formats (see Table 2). If an MPU without a serial interface is used, then four of the MPU's parallel port lines can be programmed to form the serial link to the LTC1290. Included here are two serial interface examples and one example showing a parallel port programmed to form the serial interface

### Serial Port Microprocessors

Most synchronous serial formats contain a shift clock (SCLK) and two data lines, one for transmitting and one for receiving. In most cases data bits are transmitted on the falling edge of the clock (SCLK) and captured on the rising edge. However, serial port formats vary among MPU manufactures as to the smallest number of bits that can be sent in one group (e.g., 4-bit, 8-bit or 16-bit transfers). They also vary as to the order in which the bits are transmitted (LSB or MSB first). The following examples show how the LTC1290 accommodates these differences.

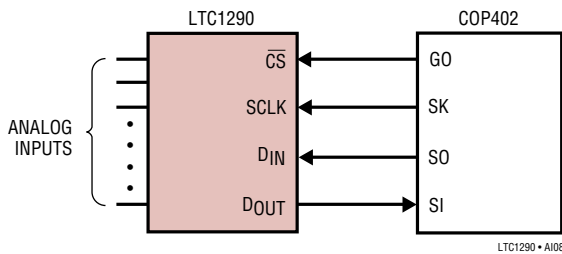
## APPLICATIONS INFORMATION

**Table 2. Microprocessors with Hardware Serial Interfaces Compatible with the LTC1290\*\***

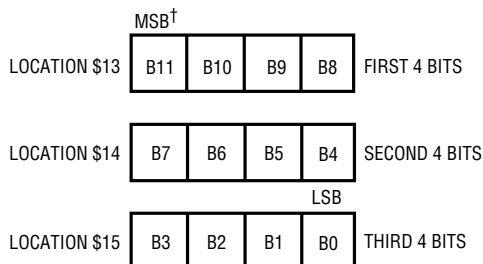
| PART NUMBER                   | TYPE OF INTERFACE |
|-------------------------------|-------------------|
| <b>Motorola</b>               |                   |
| MC6805S2, S3                  | SPI               |
| MC68HC11                      | SPI               |
| MC68HC05                      | SPI               |
| <b>RCA</b>                    |                   |
| CDP68HC05                     | SPI               |
| <b>Hitachi</b>                |                   |
| HD6305                        | SCI Synchronous   |
| HD6301                        | SCI Synchronous   |
| HD63701                       | SCI Synchronous   |
| HD6303                        | SCI Synchronous   |
| HD64180                       | SCI Synchronous   |
| <b>National Semiconductor</b> |                   |
| COP400 Family                 | MICROWIRE™        |
| COP800 Family                 | MICROWIRE/PLUS™   |
| NS8050U                       | MICROWIRE/PLUS    |
| HPC16000 Family               | MICROWIRE/PLUS    |
| <b>Texas Instruments</b>      |                   |
| TMS7002                       | Serial Port       |
| TMS7042                       | Serial Port       |
| TMS70C02                      | Serial Port       |
| TMS70C42                      | Serial Port       |
| TMS32011*                     | Serial Port       |
| TMS32020                      | Serial Port       |
| TMS370C050                    | SPI               |

\*Requires external hardware  
 \*\* Contact factory for interface information for processors not on this list

### Hardware and Software Interface to COP402 Processor



### D<sub>OUT</sub> from LTC1290 Stored in COP402 RAM



†B11 IS MSB IN UNIPOLAR OR SIGN BIT IN BIPOLAR

### National MICROWIRE (COP402)

The COP402 transfers data MSB first and in 4-bit increments (nibbles). This is easily accommodated by setting the LTC1290 to MSB-first format and 12-bit word length. The data output word is then received by the COP402 in three 4-bit blocks.

#### COP402 Code

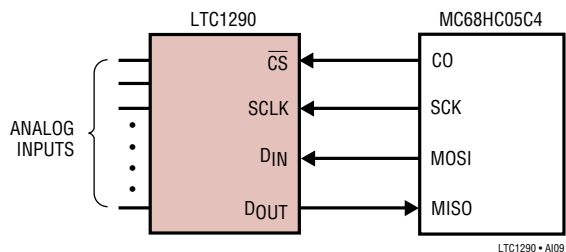
| MNEMONIC | COMMENTS                                 |
|----------|--|
| CLRA     | Must be First Instruction                |
| LBI 1,0  | BR = 1BD = 0 Initialize B Reg.           |
| STII 8   | First D <sub>IN</sub> Nibble in \$10     |
| STII E   | Second D <sub>IN</sub> Nibble in \$11    |
| STII 0   | Null Data in \$12, B = \$13              |
| LEI C    | Set EN to (1100) BIN                     |
| SC       | Carry Set                                |
| LDD 1,0  | Load First D <sub>IN</sub> Nibble In ACC |
| OGI 0    | Go (CS) Cleared                          |
| XAS      | ACC to Shift Reg. Begin Shift            |
| LDD 1,1  | Load Next D <sub>IN</sub> Nibble in ACC  |
| NOP      | Timing                                   |
| XAS      | Next Nibble, Shift Continues             |
| XIS 0    | First Nibble D <sub>OUT</sub> to \$13    |
| LDD 1,2  | Put Null Data in ACC                     |
| XAS      | Shift Continues, D <sub>OUT</sub> to ACC |
| XIS 0    | Next Nibble D <sub>OUT</sub> to \$14     |
| RC       | Clear Carry                              |
| CLRA     | Clear ACC                                |
| XAS      | Third Nibble D <sub>OUT</sub> to ACC     |
| OGI 1    | Go (CS) Set                              |
| XIS 0    | Third Nibble D <sub>OUT</sub> to \$15    |
| LBI 1,3  | Set B Reg. For Next Loop                 |

### Motorola SPI (MC68HC05C4)

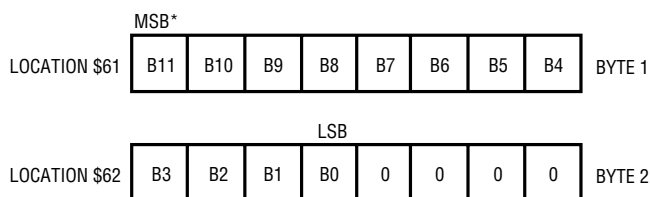
The MC68HC05C4 transfers data MSB first and in 8-bit increments. Programming the LTC1290 for MSB-first format and 16-bit word length allows the 12-bit data output to be received by the MPU as two 8-bit bytes with the final four unused bits filled with zeros by the LTC1290.

## APPLICATIONS INFORMATION

### Hardware and Software Interface to Motorola MC68HC05C4 Processor



### DOUT from LTC1290 Stored in MC68HC05C4 RAM



\*B11 IS MSB IN UNIPOLAR OR SIGN BIT IN BIPOLAR

### MC68HC05C4 Code

|       | MNEMONIC    | COMMENTS                                    |
|-------|-------------|---|
|       | LDA #\$50   | Configuration Data for SPCR                 |
|       | STA \$0A    | Load Data Into SPCR (\$0A)                  |
|       | LDA #\$FF   | Config. Data for Port C DDR                 |
|       | STA \$06    | Load Data Into Port C DDR                   |
|       | LDA #\$0F   | Load LTC1290 D <sub>IN</sub> Data Into ACC  |
|       | STA \$50    | Load LTC1290 D <sub>IN</sub> Data Into \$50 |
| START | BCLR 0,\$20 | CO Goes Low ( $\overline{CS}$ Goes Low)     |
|       | LDA \$50    | Load D <sub>IN</sub> Into ACC from \$50     |
|       | STA \$0C    | Load D <sub>IN</sub> Into SPI, Start SCK    |
|       | NOP         | 8 NOPs for Timing                           |
|       | LDA \$0B    | Check SPI Status Reg                        |
|       | LDA \$0C    | Load LTC1290 MSBs Into ACC                  |
|       | STA \$61    | Store MSBs in \$61                          |
|       | STA \$0C    | Start Next SPI Cycle                        |
|       | NOP         | 6 NOPs for Timing                           |
|       | BSET 0,\$02 | CO Goes High ( $\overline{CS}$ Goes High)   |
|       | LDA \$0B    | Check SPI Status Register                   |
|       | LDA \$0C    | Load LTC1290 LSBs Into ACC                  |
|       | STA \$62    | Store LSBs in \$62                          |

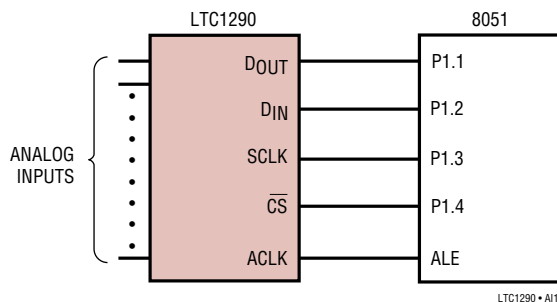
### Parallel Port Microprocessors

When interfacing the LTC1290 to an MPU which has a parallel port, the serial signals are created on the port with software. Three MPU port lines are programmed to create the  $\overline{CS}$ , SCLK and D<sub>IN</sub> signals for the LTC1290. A fourth port line reads the D<sub>OUT</sub> line. An example is made of the Intel 8051/8052/80C252 family.

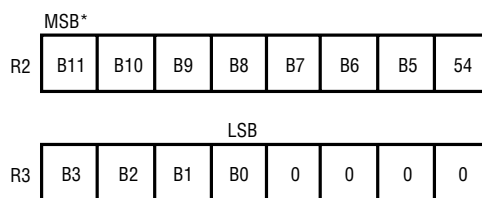
### Intel 8051

To interface to the 8051, the LTC1290 is programmed for MSB-first format and 12-bit word length. The 8051 generates  $\overline{CS}$ , SCLK and D<sub>IN</sub> on three port lines and reads D<sub>OUT</sub> on the fourth.

### Hardware and Software Interface to Intel 8051 Processor



### DOUT from LTC1290 Stored in 8051 RAM



\*B11 IS MSB IN UNIPOLAR OR SIGN BIT IN BIPOLAR



## APPLICATIONS INFORMATION

### 8051 Code

|            | MNEMONIC                  | COMMENTS                       |
|------------|---------------------------|--------------------------------|
| CONT       | MOV P1,#02H               | Bit 1 Port 1 Set as Input      |
|            | CLR P1.3                  | SCLK Goes Low                  |
|            | SETB P1.4                 | $\overline{CS}$ Goes High      |
|            | MOV A,#0EH                | $D_{IN}$ Word for LTC1290      |
| LOOP       | CLR P1.4                  | $\overline{CS}$ Goes Low       |
|            | MOV R4,#08H               | Load Counter                   |
|            | NOP                       | Delay for Deglitcher           |
|            | MOV C,P1.1                | Read Data Bit Into Carry       |
|            | RLC A                     | Rotate Data Bit Into ACC       |
|            | MOV P1.2,C                | Output $D_{IN}$ Bit to LTC1290 |
|            | SETB P1.3                 | SCLK Goes High                 |
|            | CLR P1.3                  | SCLK Goes Low                  |
|            | DJNZ R4,LOOP              | Next Bit                       |
|            | MOV R2,A                  | Store MSBs in R2               |
|            | MOV C,P1.1                | Read Data Bit Into Carry       |
|            | CLR A                     | Clear ACC                      |
|            | RLC A                     | Rotate Data Bit Into ACC       |
|            | SETB P1.3                 | SCLK Goes High                 |
|            | CLR P1.3                  | SCLK Goes Low                  |
|            | MOV C,P1.1                | Read Data Bit Into Carry       |
|            | RLC A                     | Rotate Data Bit Into ACC       |
|            | SETB P1.3                 | SCLK Goes High                 |
|            | CLR P1.3                  | SCLK Goes Low                  |
|            | MOV C,P1.1                | Read Data Bit Into Carry       |
| RLC A      | Rotate Data Bit Into ACC  |                                |
| SETB P1.3  | SCLK Goes High            |                                |
| CLR P1.3   | SCLK Goes Low             |                                |
| MOV C,P1.1 | Read Data Bit Into Carry  |                                |
| RLC A      | Rotate Data Bit Into ACC  |                                |
| SETB P1.3  | SCLK Goes High            |                                |
| CLR P1.3   | SCLK Goes Low             |                                |
| MOV C,P1.1 | Read Data Bit Into Carry  |                                |
| RRC A      | Rotate Right Into ACC     |                                |
| RRC A      | Rotate Right Into ACC     |                                |
| RRC A      | Rotate Right Into ACC     |                                |
| RRC A      | Rotate Right Into ACC     |                                |
| MOV R3,A   | Store LSBs in R3          |                                |
| SETB P1.3  | SCLK Goes High            |                                |
| CLR P1.3   | SCLK Goes Low             |                                |
| SETB P1.4  | $\overline{CS}$ Goes High |                                |
| DELAY      | MOV R5,#0BH               | Load Counter                   |
|            | DJNZ R5,DELAY             | Go to Delay if Not Done        |

### Sharing the Serial Interface

The LTC1290 can share the same 3-wire serial interface with other peripheral components or other LTC1290s (see Figure 5). In this case, the  $\overline{CS}$  signals decide which LTC1290 is being addressed by the MPU.

### ANALOG CONSIDERATIONS

#### 1. Grounding

The LTC1290 should be used with an analog ground plane and single point grounding techniques.

AGND (Pin 11) should be tied directly to this ground plane.

DGND (Pin 10) can also be tied directly to this ground plane because minimal digital noise is generated within the chip itself.

$V_{CC}$  (Pin 20) should be bypassed to the ground plane with a 22 $\mu$ F tantalum with leads as short as possible.  $V^-$  (Pin 12) should be bypassed with a 0.1 $\mu$ F ceramic disk. For single supply applications,  $V^-$  can be tied to the ground plane.

It is also recommended that  $REF^-$  (Pin 13) and COM (Pin 9) be tied directly to the ground plane. All analog inputs should be referenced directly to the single point ground. Digital inputs and outputs should be shielded from and/or routed away from the reference and analog circuitry.

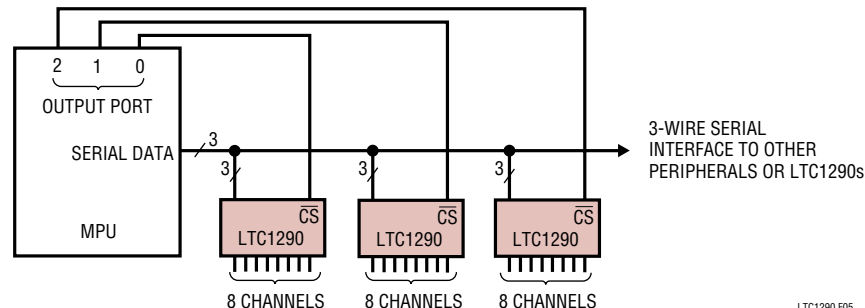
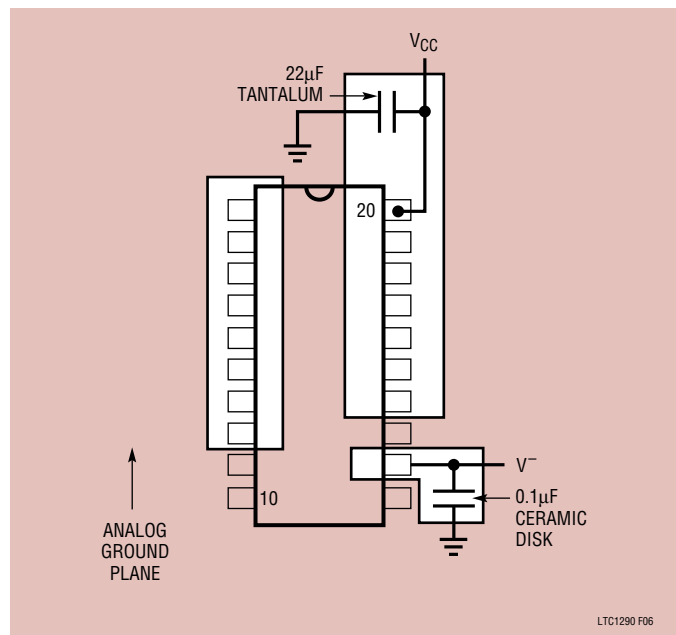


Figure 5. Several LTC1290s Sharing One 3-Wire Serial Interface

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**Figure 6. Example Ground Plane for the LTC1290**

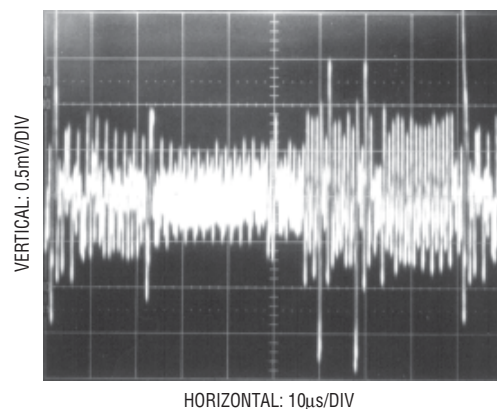
Figure 6 shows an example of an ideal ground plane design for a two-sided board. Of course, this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

### 2. Bypassing

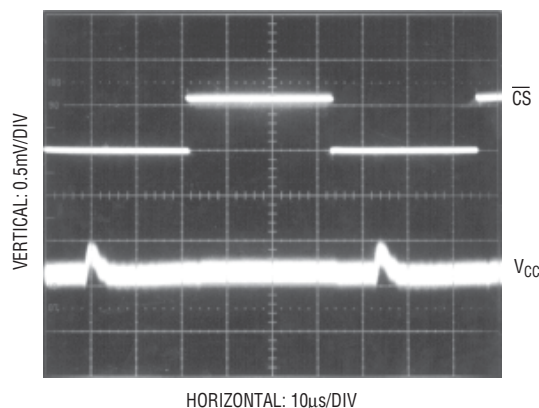
For good performance,  $V_{CC}$  must be free of noise and ripple. Any changes in the  $V_{CC}$  voltage with respect to analog ground during a conversion cycle can induce errors or noise in the output code.  $V_{CC}$  noise and ripple can be kept below 0.5mV by bypassing the  $V_{CC}$  pin directly to the analog ground plane with a 22µF tantalum capacitor and leads as short as possible. The lead from the device to the  $V_{CC}$  supply should also be kept to a minimum and the  $V_{CC}$  supply should have a low output impedance such as that obtained from a voltage regulator (e.g., LT1761). Figures 7 and 8 show the effects of good and poor  $V_{CC}$  bypassing.

### 3. Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1290 have capacitive switching input current spikes. These current



**Figure 7. Poor  $V_{CC}$  Bypassing. Noise and Ripple Can Cause A/D Errors**



**Figure 8. Good  $V_{CC}$  Bypassing Keeps Noise and Ripple on  $V_{CC}$  Below 1mV**

spikes settle quickly and do not cause a problem. However, if large source resistances are used or if slow settling op amps drive the inputs, care must be taken to insure that the transients caused by the current spikes settle completely before the conversion begins.

#### Source Resistance

The analog inputs of the LTC1290 look like a 100pF capacitor ( $C_{IN}$ ) in series with a 500Ω resistor ( $R_{ON}$ ) as shown in Figure 9.  $C_{IN}$  gets switched between the selected “+” and “-” inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constants be short enough to allow the analog inputs to completely settle within the allowed time.

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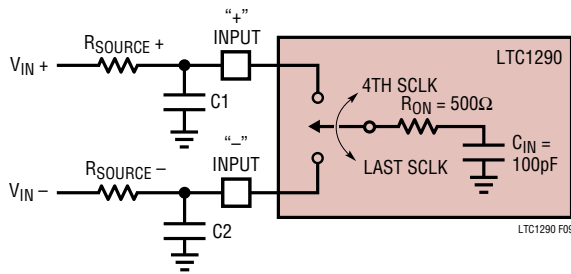


Figure 9. Analog Input Equivalent Circuit

### “+” Input Settling

This input capacitor is switched onto the “+” input during the sample phase ( $t_{SMPL}$ , see Figure 10). The sample phase starts at the 4th SCLK cycle and lasts until the falling edge of the last SCLK (the 8th, 12th or 16th SCLK cycle depending on the selected word length). The voltage on the “+” input must settle completely within this sample time. Minimizing  $R_{SOURCE+}$  and C1 will improve the input settling time. If large “+” input source resistance must be used, the sample time can be increased by using a slower SCLK frequency or selecting a longer word length. With the minimum possible sample time of  $2\mu s$ ,  $R_{SOURCE+} < 1k$  and  $C1 < 20pF$  will provide adequate settling.

### “-” Input Settling

At the end of the sample phase the input capacitor switches to the “-” input and the conversion starts (see Figure 10). During the conversion, the “+” input voltage is effectively “held” by the sample-and-hold and will not affect the conversion result. However, it is critical that the “-” input voltage be free of noise and settle completely during the first four ACLK cycles of the conversion time. Minimizing  $R_{SOURCE-}$  and C2 will improve settling time. If large “-” input source resistance must be used, the time allowed for settling can be extended by using a slower ACLK frequency. At the maximum ACLK rate of 4MHz,  $R_{SOURCE-} < 250\Omega$  and  $C2 < 20pF$  will provide adequate settling.

### Input Op Amps

When driving the analog inputs with an op amp it is important that the op amp settle within the allowed time (see Figure 10). Again, the “+” and “-” input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1797, LT1800 and LT1812 single supply op amps can be made to settle well even with the minimum settling windows of  $2\mu s$  (“+” input) and  $1\mu s$  (“-” input) which occur at the

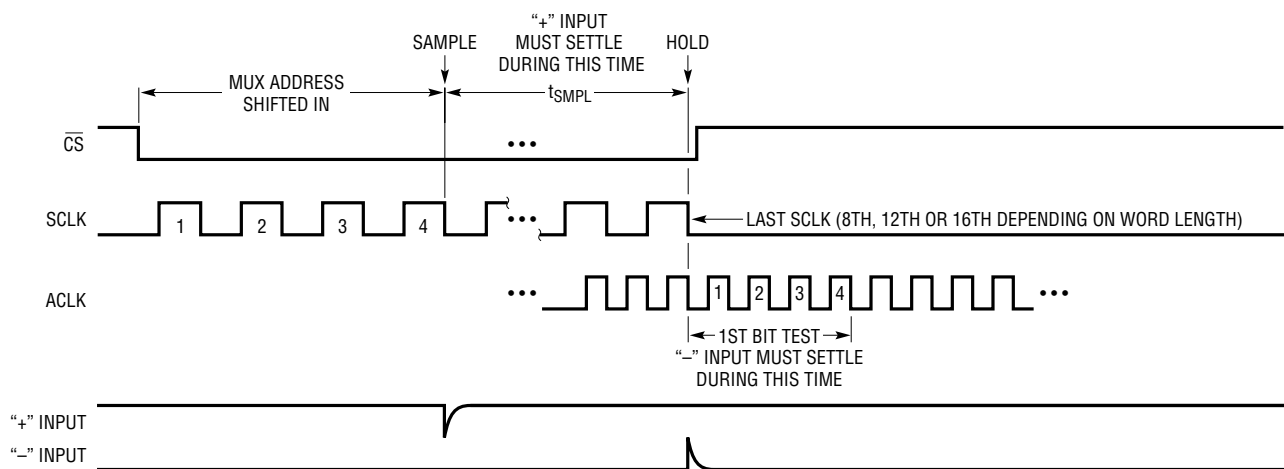


Figure 10. “+” and “-” Input Settling Windows

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maximum clock rates (ACLK = 4MHz and SCLK = 2MHz). Figures 11 and 12 show examples of adequate and poor op amp settling.

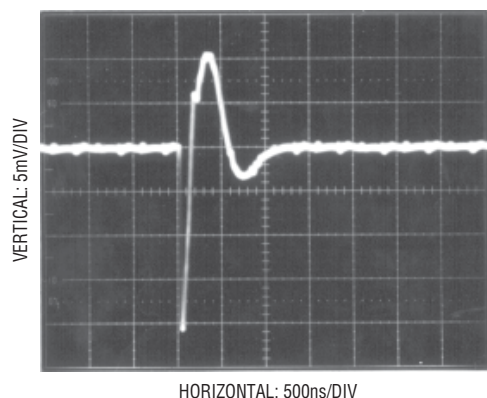


Figure 11. Adequate Settling of Op Amps Driving Analog Input

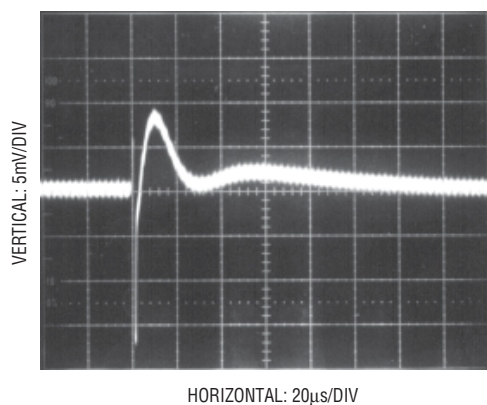


Figure 12. Poor Op Amp Settling Can Cause A/D Errors

### RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 13. For large values of  $C_F$  (e.g., 1 $\mu$ F), the capacitive input switching currents are averaged into a net DC current. Therefore, a filter should be chosen with a small resistor and large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately  $I_{DC} = (100\text{pF})(V_{IN}/t_{CYC})$  and is roughly proportional to  $V_{IN}$ . When running at the minimum cycle time of 20 $\mu$ s, the input current equals 25 $\mu$ A at  $V_{IN} = 5$ V. In this case, a filter resistor of 5 $\Omega$  will cause 0.1LSB of full-scale error. If a larger filter resistor must be used, errors can be eliminated by increasing the cycle time as shown in the typical curve of Maximum Filter Resistor vs Cycle Time.

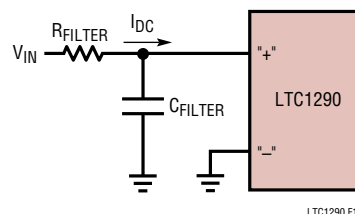


Figure 13. RC Input Filtering

### Input Leakage Current

Input leakage currents can also create errors if the source resistance gets too large. For instance, the maximum input leakage specification of 1 $\mu$ A (at 125 $^{\circ}$ C) flowing through a source resistance of 1k $\Omega$  will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see the typical curve of Input Channel Leakage Current vs Temperature).

### Noise Coupling Into Inputs

High source resistance input signals (>500 $\Omega$ ) are more sensitive to coupling from external sources. It is preferable to use channels near the center of the package (i.e., CH2 to CH7) for signals which have the highest output resistance because they are essentially shielded by the pins on the package ends (DGND and CH0). Grounding any unused inputs (especially the end pin, CH0) will also reduce outside coupling into high source resistances.

## 4. Sample-and-Hold

### Single-Ended Inputs

The LTC1290 provides a built-in sample-and-hold (S&H) function for all signals acquired in the single-ended mode (COM pin grounded). This sample-and-hold allows the LTC1290 to convert rapidly varying signals (see the typical curve of S&H Acquisition Time vs Source Resistance). The input voltage is sampled during the  $t_{SMPL}$  time as shown in Figure 10. The sampling interval begins after the fourth MUX address bit is shifted in and continues during the remainder of the data transfer. On the falling edge of the final SCLK, the S&H goes into hold mode and the conversion begins. The voltage will be held on either the 8th, 12th or 16th falling edge of the SCLK depending on the word length selected.

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### Differential Inputs

With differential inputs or when the COM pin is not tied to ground, the A/D no longer converts just a single voltage but rather the difference between two voltages. In these cases, the voltage on the selected “+” input is still sampled and held and therefore may be rapidly time varying just as in single-ended mode. However, the voltage on the selected “-” input must remain constant and be free of noise and ripple throughout the conversion time. Otherwise, the differencing operation may not be performed accurately. The conversion time is 52 ACLK cycles. Therefore, a change in the “-” input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the “-” input this error would be:

$$V_{\text{ERROR (MAX)}} = (V_{\text{PEAK}})(2\pi) [f(\text{“-”})](52/f_{\text{ACLK}})$$

Where  $f(\text{“-”})$  is the frequency of the “-” input voltage,  $V_{\text{PEAK}}$  is its peak amplitude and  $f_{\text{ACLK}}$  is the frequency of the ACLK. In most cases  $V_{\text{ERROR}}$  will not be significant. For a 60Hz signal on the “-” input to generate a 0.25LSB error (300 $\mu$ V) with the converter running at ACLK = 4MHz, its peak value would have to be 61mV.

### 5. Reference Inputs

The voltage between the reference inputs of the LTC1290 defines the voltage span of the A/D converter. The reference inputs will have transient capacitive switching currents due to the switched capacitor conversion technique (see Figure 14). During each bit test of the conversion (every 4 ACLK cycles), a capacitive current spike will be generated on the reference pins by the A/D. These current spikes settle quickly and do not cause a problem. However, if slow settling circuitry is used to drive the reference inputs, care must be taken to insure that transients caused by these current spikes settle completely during each bit test of the conversion.

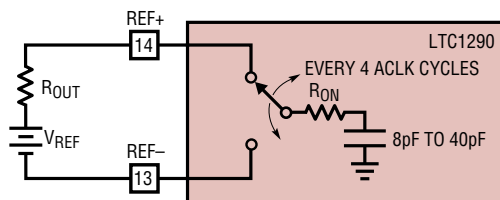


Figure 14. Reference Input Equivalent Circuit

When driving the reference inputs, two things should be kept in mind:

1. Transients on the reference inputs caused by the capacitive switching currents must settle completely during each bit test (each 4 ACLK cycles). Figures 15 and 16 show examples of both adequate and poor settling. Using a slower ACLK will allow more time for the reference to settle. However, even at the maximum ACLK rate of 4MHz most references and op amps can be made to settle within the 1 $\mu$ s bit time. For example the LT1236 will settle adequately.
2. It is recommended that REF<sup>-</sup> input be tied directly to the analog ground plane. If REF<sup>-</sup> is biased at a voltage other than ground, the voltage must not change during a conversion cycle. This voltage must also be free of noise and ripple with respect to analog ground.

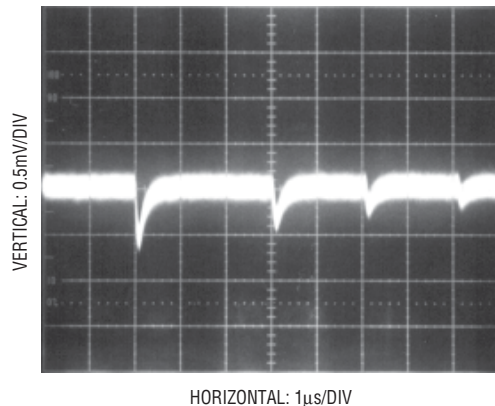


Figure 15. Adequate Reference Settling

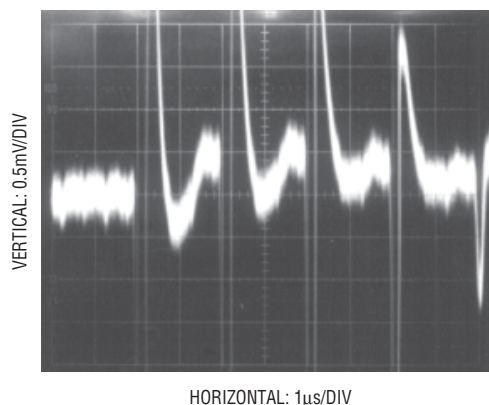


Figure 16. Poor Reference Settling Can Cause A/D Errors



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### 6. Reduced Reference Operation

The effective resolution of the LTC1290 can be increased by reducing the input span of the converter. The LTC1290 exhibits good linearity and gain over a wide range of reference voltages (see the typical curves of Linearity and Gain Error vs Reference Voltage). However, care must be taken when operating at low values of  $V_{REF}$  because of the reduced LSB step size and the resulting higher accuracy requirement placed on the converter. The following factors must be considered when operating at low  $V_{REF}$  values:

1. Offset
2. Noise

#### Offset with Reduced $V_{REF}$

The offset of the LTC1290 has a larger effect on the output code when the A/D is operated with reduced reference voltage. The offset (which is typically a fixed voltage) becomes a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Unadjusted Offset Error vs Reference Voltage shows how offset in LSBs is related to reference voltage for a typical value of  $V_{OS}$ . For example, a  $V_{OS}$  of 0.1mV which is 0.1LSB with a 5V reference becomes 0.4LSB with a 1.25V reference. If this offset is unacceptable, it can be corrected digitally by the receiving system or by offsetting the “–” input to the LTC1290.

#### Noise with Reduced $V_{REF}$

The total input referred noise of the LTC1290 can be reduced to approximately 200 $\mu$ V peak-to-peak using a ground plane, good bypassing, good layout techniques and minimizing noise on the reference inputs. This noise is insignificant with a 5V reference but will become a larger fraction of an LSB as the size of the LSB is reduced. The typical curve of Noise Error vs Reference Voltage shows the LSB contribution of this 200 $\mu$ V of noise.

For operation with a 5V reference, the 200 $\mu$ V noise is only 0.16LSB peak-to-peak. In this case, the LTC1290 noise will contribute virtually no uncertainty to the output code. However, for reduced references, the noise may become a significant fraction of an LSB and cause undesirable jitter in the output code. For example, with a 1.25V reference, this same 200 $\mu$ V noise is 0.64LSB peak-to-peak. This will

reduce the range of input voltages over which a stable output code can be achieved by 0.64LSB. In this case averaging readings may be necessary.

This noise data was taken in a very clean setup. Any setup induced noise (noise or ripple on  $V_{CC}$ ,  $V_{REF}$ ,  $V_{IN}$  or  $V^-$ ) will add to the internal noise. The lower the reference voltage to be used, the more critical it becomes to have a clean, noise-free setup.

### 7. LTC1290 AC Characteristics

Two commonly used figures of merit for specifying the dynamic performance of the A/D's in digital signal processing applications are the Signal-to-Noise Ratio (SNR) and the “effective number of bits (ENOB).” SNR is defined as the ratio of the RMS magnitude of the fundamental to the RMS magnitude of all the nonfundamental signals up to the Nyquist frequency (half the sampling frequency). The theoretical maximum SNR for a sine wave input is given by:

$$\text{SNR} = (6.02N + 1.76\text{dB})$$

where N is the number of bits. Thus the SNR is a function of the resolution of the A/D. For an ideal 12-bit A/D the SNR is equal to 74dB. A Fast Fourier Transform (FFT) plot of the output spectrum of the LTC1290 is shown in Figures 17a and 17b. The input ( $f_{IN}$ ) frequencies are 1kHz and 25kHz with the sampling frequency ( $f_S$ ) at 50.6kHz. The SNR obtained from the plot are 73.25dB and 72.54dB.

Rewriting the SNR expression it is possible to obtain the equivalent resolution based on the SNR measurement.

$$N = (\text{SNR} - 1.76\text{dB})/6.02$$

This is the so-called effective number of bits (ENOB). For the example shown in Figures 17a and 17b,  $N = 11.9$  bits and 11.8 bits, respectively. Figure 18 shows a plot of ENOB as a function of input frequency. The curve shows the A/D's ENOB remain in the range of 11.9 to 11.8 for input frequencies up to  $f_S/2$ .

Figure 19 shows an FFT plot of the output spectrum for two tones applied to the input of the A/D. Nonlinearities in the A/D will cause distortion products at the sum and difference frequencies of the fundamentals and products of the fundamentals. This is classically referred to as intermodulation distortion (IMD).

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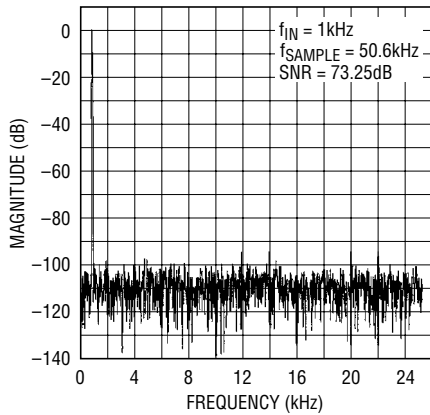


Figure 17a. LTC1290 FFT Plot

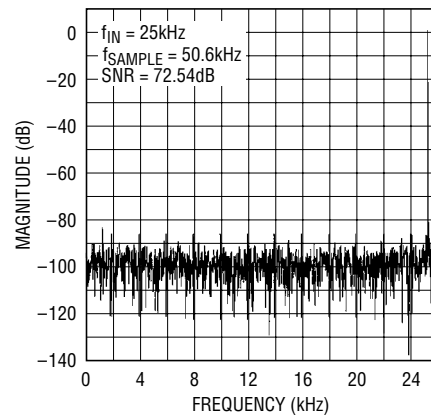


Figure 17b. LTC1290 FFT Plot

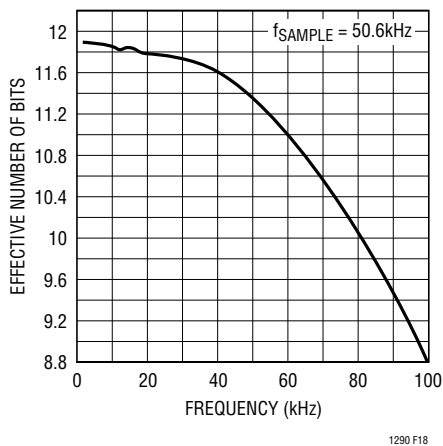


Figure 18. LTC1290 ENOB vs Input Frequency

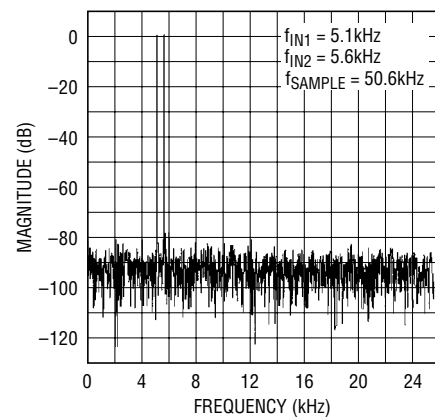


Figure 19. LTC1290 FFT Plot

## 8. Overvoltage Protection

Applying signals to the analog MUX that exceed the positive or negative supply of the device will degrade the accuracy of the A/D and possibly damage the device. For example this condition would occur if a signal is applied to the analog MUX before power is applied to the LTC1290. Another example is the input source is operating from different supplies of larger value than the LTC1290. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp or current limit the input source. As shown in Figure 20, a 1k resistor is enough to stand off  $\pm 15V$  (15mA for one only channel). If more than one channel exceeds the supplies

then the following guidelines can be used. Limit the current to 7mA per channel and 28mA for all channels. This means four channels can handle 7mA of input current each. Reducing the ACLK and SCLK frequencies from the maximum of 4MHz and 2MHz, respectively, (see Typical Performance Characteristics curves Maximum ACLK Frequency vs Source Resistance and Sample-and-Hold Acquisition Time vs Source Resistance) allows the use of larger current limiting resistors. Use 1N4148 diode clamps from the MUX inputs to  $V_{CC}$  and  $V^-$  if the value of the series resistor will not allow the maximum clock speeds to be used or if an unknown source is used to drive the LTC1290 MUX inputs.

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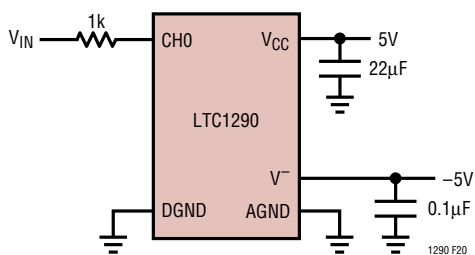


Figure 20. Overtoltage Protection for MUX

How the various power supplies to the LTC1290 are applied can also lead to overvoltage conditions. For single supply operation (i.e., unipolar mode), if  $V_{CC}$  and  $REF^+$  are not tied together, then  $V_{CC}$  should be turned on first, then  $REF^+$ . If this sequence cannot be met, connecting a diode from  $REF^+$  to  $V_{CC}$  is recommended (see Figure 21).

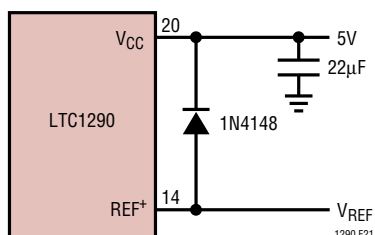


Figure 21

For dual supplies (bipolar mode) placing two Schottky diodes from  $V_{CC}$  and  $V^-$  to ground (Figure 23) will prevent power supply reversal from occurring when an input source is applied to the analog MUX before power is applied to the device. Power supply reversal occurs, for example, if the input is pulled below  $V^-$  then  $V_{CC}$  will pull a diode drop below ground which could cause the device not to power up properly. Likewise, if the input is pulled above  $V_{CC}$  then  $V^-$  will be pulled a diode drop above ground. If no inputs are present on the MUX, the Schottky diodes are not required if  $V^-$  is applied first, then  $V_{CC}$ .

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device  $V_{CC}$  without damaging the device.

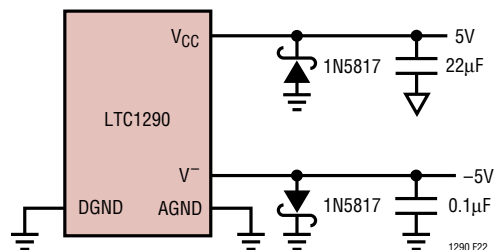


Figure 22. Power Supply Reversal