Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Dual Smart Battery System Manager

FEATURES

- **SMBus Charger/Selector for Two Smart Batteries***
- **Voltage and Current Accuracy within 0.2% of Value Reported by Battery**
- **Simplifies Construction of "Smart Battery System Manager"**
- **Includes All SMBus Charger V1.1 Safety Features**
- **Supports Autonomous Operation without a Host**
- **Allows Both Batteries to Discharge Simultaneously into Single Load with Low Loss (Ideal Diode)**
- SMBus Switching for Dual Batteries with Alarm Monitoring for Charging Battery at All Times
- Pin Programmable Limits for Maximum Charge Current and Voltage Improve Safety
- Fast Autonomous PowerPath™ Switching (<10µs)
- Low Loss Simultaneous Charging of Two Batteries
- >95% Efficient Synchronous Buck Charger
- AC Adapter Current Limiting* Maximizes Charge Rate
- SMBus Accelerator Improves SMBus Timing**
- Available in 48-Lead TSSOP Package

APPLICATIONS

- Portable Computers and Instruments
- Standalone Dual Smart Battery Chargers
- Battery Backup Systems

DESCRIPTION

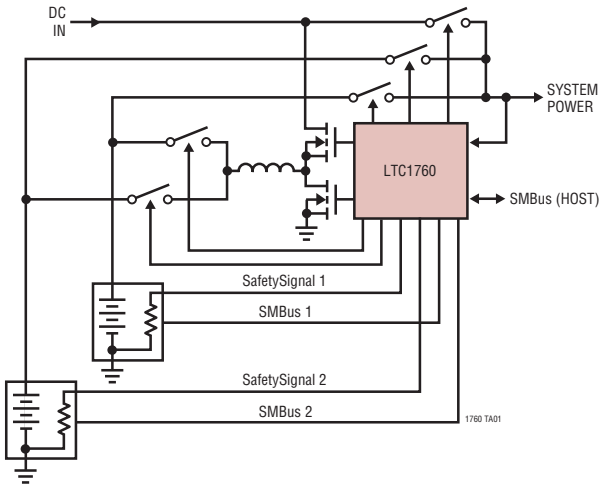
The LTC®1760 Smart Battery System Manager is a highly-integrated SMBus Level 3 battery charger and selector intended for products using dual smart batteries. Three SMBus interfaces allow the LTC1760 to servo to the internal voltage and currents measured by the batteries while allowing an SMBus Host device to monitor either battery's status. Charging accuracy is determined by the battery's internal voltage and current measurements, typically better than ±0.2%.

A proprietary PowerPath architecture supports simultaneous charging or discharging of both batteries. Typical battery run times are extended by up to 10%, while charging times are reduced by up to 50%. The LTC1760 automatically switches between power sources in less than 10µs to prevent power interruption upon battery or wall adapter removal.

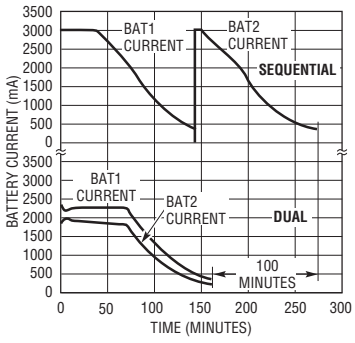
The LTC1760 implements all elements of a version 1.1 "Smart Battery System Manager" except for the generation of composite battery information. An internal multiplexer cleanly switches the SMBus Host to either of the two attached Smart Batteries without generating partial messages to batteries or SMBus Host. Thermistors on both batteries are automatically monitored for temperature and disconnection information (SafetySignal).

TYPICAL APPLICATION

Dual Battery Charger/Selector System Architecture



Dual vs Sequential Charging



BATTERY TYPE: 10.8V Li-Ion (MOLTECH NI2020)
REQUESTED CURRENT = 3A
REQUESTED VOLTAGE = 12.3V
MAX CHARGER CURRENT = 4.1A

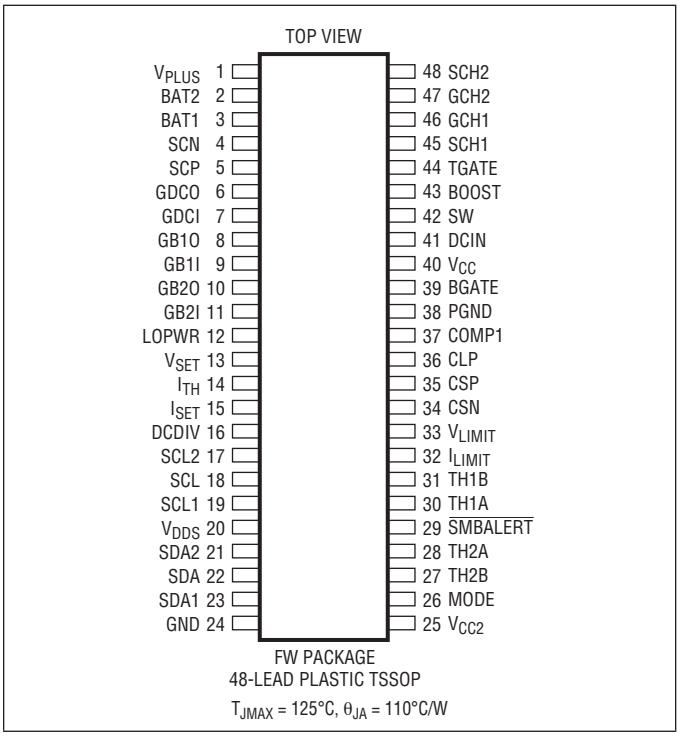
1760 TA03

ABSOLUTE MAXIMUM RATINGS

(Note 1)

DCIN, SCP, SCN, CLP,
V_{PLUS}, SW to GND ..... –0.3V to 32V
SCH1, SCH2 to GND ..... –0.3V to 28V
BOOST to GND ..... –0.3V to 37V
CSP, CSN, BAT1, BAT2 to GND ..... –0.3V to 28V
LOPWR, DCDIV to GND ..... –0.3V to 10V
V_{CC2}, V_{DDS} to GND ..... –0.3V to 7V
SDA1, SDA2, SDA, SCL1,
SCL2, SCL, $\overline{SMBALERT}$ to GND ..... –0.3V to 7V
MODE to GND ..... –0.3V to V_{CC2} +0.3V
COMP1 to GND ..... –0.3V to 5V
Maximum DC Current Into Pin
SDA1, SDA2, SDA, SCL1, SCL2, SCL ..... ±3mA
TH1A, TH2A ..... –5mA
TH1B, TH2B ..... –102µA
Operating Junction Temperature Range
(Note 6) ..... –40°C to 125°C
Storage Temperature ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



ORDER INFORMATION

(http://www.linear.com/product/LTC1760#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1760CFW#PBF	LTC1760CFW#TRPBF	LTC1760CFW	48-Lead Plastic TSSOP	0°C to 85°C
LTC1760IFW#PBF	LTC1760IFW#TRPBF	LTC1760IFW	48-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 6). V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, V_{VDDS} = 3.3V, V_{VCC2} = 5.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply and Reference							
	DCIN Operating Range	DCIN Selected		6		28	V
I_{CH0} I_{CH1}	DCIN Operating Current	Not Charging (DCIN Selected) (Note 10) Charging (DCIN Selected) (Note 10)			1 1.3	1.5 2	mA mA
I_{VCC2_AC1} I_{VCC2_AC0}	V_{CC2} Operating Current	AC Present (Note 11) AC Not Present (Note 11)			0.75 75	1 100	mA µA
	Battery Operating Voltage Range	Battery Selected, PowerPath Function Battery Selected, Charging Function (Note 2)		6 0		28 28	V V
I_{BAT}	Battery Drain Current	Battery Selected, Not Charging, V_{DCIN} = 0V (Note 10)			175		µA
 V_{FDC} V_{FB1} V_{FB2} V_{FSCN}	V_{PLUS} Diodes Forward Voltage: DCIN to V_{PLUS} BAT1 to V_{PLUS} BAT2 to V_{PLUS} SCN to V_{PLUS}	 I_{VCC} = 10mA I_{VCC} = 0mA I_{VCC} = 0mA I_{VCC} = 0mA			 0.8 0.7 0.7 0.7		 V V V V
UVLO	Undervoltage Lockout Threshold	V_{PLUS} Ramping Down, Measured at V_{PLUS} to GND	●	3		5	V
V_{VCC}	V_{CC} Regulator Output Voltage		●	4.9	5.2	5.5	V
V_{LDR}	V_{CC} Load Regulation	No External Connection Beyond Applications Shown Herein			0.2	1	%
Switching Regulator							
V_{TOL}	Voltage Accuracy	With Respect to Voltage Reported by Battery V_{CHMIN} < Requested Voltage < V_{LIMIT}	●	–32		32	mV
I_{TOL}	Current Accuracy	With Respect to Current Reported by Battery 4mV/R_{SENSE} < Requested Current < I_{LIMIT} (Min) (Note 12) R_{ILIMIT} = 0 (Short to GND) R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short I_{LIMIT} to V_{CC2})	 ● ● ● ●	 –2 –4 –8 –8		 2 4 8 8	 mA mA mA mA
f_{OSC}	Regulator Switching Frequency			255	300	345	kHz
f_{DO}	Regulator Switching Frequency in Low Dropout Mode	Duty Cycle ≥99%		20	25		kHz
DC_{MAX}	Regulator Maximum Duty Cycle			99	99.5		%
I_{MAX}	Maximum Current Sense Threshold	V_{ITH} = 2.2V		140	155	190	mV
I_{SNS}	CA1 Input Bias Current	V_{CSP} = V_{CSN} > 5V			150		µA
CMSL	CA1 Input Common Mode Low			0			V
CMSH	CA1 Input Common Mode High					V_{DCIN} – 0.2	V
V_{CL1}	CL1 Turn-On Threshold	 C-Grade (Note 6) I-Grade (Note 6)	 ● ●	95 94 90	100 100 100	105 108 108	mV mV mV
 TG t_r TG t_r	TGATE Transition Time: TGATE Rise Time TGATE Fall Time	 C_{LOAD} = 3300pF, 10% to 90% C_{LOAD} = 3300pF, 10% to 90%			 50 50	 90 90	 ns ns
 BG t_r BG t_f	BGATE Transition Time BGATE Rise Time BGATE Fall Time	 C_{LOAD} = 3300pF, 10% to 90% C_{LOAD} = 3300pF, 10% to 90%			 50 40	 90 80	 ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 6). V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, V_{VDDS} = 3.3V, V_{VCC2} = 5.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Trip Points							
V_{TR}	DCDIV/LOPWR Threshold	V_{DCDIV} or V_{LOPWR} Falling C-Grade (Note 6) I-Grade (Note 6)	 ● ●	 1.166 1.162	 1.19 1.19	 1.215 1.215	 V V
V_{THYS}	DCDIV/LOPWR Hysteresis Voltage	V_{DCDIV} or V_{LOPWR} Rising			30		mV
I_{BVT}	DCDIV/LOPWR Input Bias Current	V_{DCDIV} or V_{LOPWR} = 1.19V			20	200	nA
V_{TSC}	Short-Circuit Comparator Threshold	$V_{SCP} - V_{SCN}$, $V_{CC} \geq 5V$ C-Grade (Note 6) I-Grade (Note 6)	 ● ●	 90 88	 100 100	 115 115	 mV mV
V_{FTO}	Fast PowerPath Turn-Off Threshold	V_{DCDIV} Rising from V_{CC}		6	7	7.9	V
V_{OVSD}	Overvoltage Shutdown Threshold as a Percent of Programmed Charger Voltage	V_{SET} Rising from 0.8V until TGATE and BGATE Stop Switching			107		%
DACs							
I_{RES}	I_{DAC} Resolution	Guaranteed Monotonic		10			Bits
t_{IP} t_{ILOW}	I_{DAC} Pulse Period: Normal Mode Wake-Up Mode			6	10 50	15	µs ms
	Charging Current Granularity	R_{ILIMIT} = 0 (Short I_{LIMIT} to GND) R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short I_{LIMIT} to V_{CC2})			1 2 4 4		mA mA mA mA
I_{WAKE_UP}	Wake-Up Charging Current (Note 5)			60	80	100	mA
I_{LIMIT}	Charging Current Limit	C-Grade (Note 6) R_{ILIMIT} = 0 (Short I_{LIMIT} to GND) R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short I_{LIMIT} to V_{CC2}) I-Grade (Note 6) R_{ILIMIT} = 0 (Short I_{LIMIT} to GND) R_{ILIMIT} = 10k ±1% R_{ILIMIT} = 33k ±1% R_{ILIMIT} = Open (or Short I_{LIMIT} to V_{CC2})	 ● ● ● ● ● ● ● ●	 980 1960 2490 3920 930 1870 2380 3750	 1000 2000 3000 4000 1000 2000 3000 4000	 1070 2140 3210 4280 1110 2220 3320 4430	 mA mA mA mA mA mA mA mA
V_{RES}	V_{DAC} Resolution	Guaranteed Monotonic (5V < V_{BAT} < 25V)		11			Bits
V_{STEP}	V_{DAC} Granularity				16		mV
V_{LIMIT}	Charging Voltage Limit (Note 7)	R_{VLIMIT} = 0 (Short V_{LIMIT} to GND) R_{VLIMIT} = 10k ±1% R_{VLIMIT} = 33k ±1% R_{VLIMIT} = 100k ±1% R_{VLIMIT} = Open (or Short V_{LIMIT} to V_{CC2})(Note 13)	● ● ● ● ●	8400 12608 16832 21024	8432 12640 16864 21056 32768	8464 12672 16896 21088	mV mV mV mV mV
Charge MUX Switches							
t_{ONC}	GCH1/GCH2 Turn-On Time	$V_{GCHX} - V_{SCHX}$ > 3V, C_{LOAD} = 3000pF			5	10	ms
t_{OFFC}	GCH1/GCH2 Turn-Off Time	$V_{GCHX} - V_{SCHX}$ < 1V, from Time of $V_{CSN} < V_{BATX}$ – 30mV, C_{LOAD} = 3000pF			15		µs
V_{CON}	CH Gate Clamp Voltage GCH1 GCH2	I_{LOAD} = 1µA $V_{GCH1} - V_{SCH1}$ $V_{GCH2} - V_{SCH2}$	 	 5 5	 5.8 5.8	 7 7	 V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 6). V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, V_{VDDS} = 3.3V, V_{VCC2} = 5.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{COFF}	CH Gate Off Voltage GCH1 GCH2	I_{LOAD} =10µA $V_{GCH1} – V_{SCH1}$ $V_{GCH2} – V_{SCH2}$		 –0.8 –0.8	 –0.4 –0.4	 0 0	 V V
V_{TOC}	CH Switch Reverse Turn-Off Voltage	$V_{BATX} – V_{CSN}$, 5V ≤ V_{BATX} ≤ 28V C-Grade (Note 6) I-Grade (Note 6)	 ● ●	 5 2	 20 20	 40 40	 mV mV
V_{FC}	CH Switch Forward Regulation Voltage	$V_{CSN} – V_{BATX}$, 5V ≤ V_{BATX} ≤ 28V	●	15	35	60	mV
$I_{OC(SRC)}$ $I_{OC(SNK)}$	GCH1/GCH2 Active Regulation: Max Source Current Max Sink Current	$V_{GCHX} – V_{SCHX}$ = 1.5V			 –2 2		 µA µA
V_{CHMIN}	BATX Voltage Below Which Charging is Inhibited	(Note 14)		3.5		4.7	V
PowerPath Switches							
t_{DLY}	Blanking Period after UVLO Trip	Switches Held Off			250		ms
t_{PPB}	Blanking Period after LOPWR Trip	Switches in 3-Diode Mode			1		sec
t_{ONPO}	GB1O/GB2O/GDCO Turn-On Time	V_{GS} < –3V, from Time of Battery/DC Removal, or LOPWR Indication, C_{LOAD} = 3000pF	●		5	10	µs
t_{OFFPO}	GB1O/GB2O/GDCO Turn-Off Time	V_{GS} > –1V, from Time of Battery/DC Removal, or LOPWR Indication, C_{LOAD} = 3000pF	●		3	7	µs
V_{PONO}	Output Gate Clamp Voltage GB1O GB2O GDCO	I_{LOAD} = 1µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1O} Highest (V_{BAT2} or V_{SCP}) – V_{GB2O} Highest (V_{DCIN} or V_{SCP}) – V_{GDCO}		 4.75 4.75 4.75	 6.25 6.25 6.25	 7 7 7	 V V V
V_{POFFO}	Output Gate Off Voltage GB1O GB2O GDCO	I_{LOAD} = –25µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1O} Highest (V_{BAT2} or V_{SCP}) – V_{GB2O} Highest (V_{DCIN} or V_{SCP}) – V_{GDCO}			 0.18 0.18 0.18	 0.25 0.25 0.25	 V V V
V_{TOP}	PowerPath Switch Reverse Turn-Off Voltage	$V_{SCP} – V_{BATX}$ or $V_{SCP} – V_{DCIN}$ 6V ≤ V_{SCP} ≤ 28V C-Grade (Note 6) I-Grade (Note 6)	 ● ●	 5 2	 20 20	 60 60	 mV mV
V_{FP}	PowerPath Switch Forward Regulation Voltage	$V_{BATX} – V_{SCP}$ or $V_{DCIN} – V_{SCP}$ 6V ≤ V_{SCP} ≤ 28V	●	0	25	50	mV
$I_{OP(SRC)}$ $I_{OP(SNK)}$	GDCI/GB1I/GB2I Active Regulation: Source Current Sink Current	(Note 3)			 –4 75		 µA µA
t_{ONPI}	Gate B1I/B2I/DCI Turn-On Time	V_{GS} < –3V, C_{LOAD} = 3000pF (Note 4)			300		µs
t_{OFFPI}	Gate B1I/B2I/DCI Turn-Off Time	V_{GS} > –1V, C_{LOAD} = 3000pF (Note 4)			10		µs
V_{PONI}	Input Gate Clamp Voltage GB1I GB2I GDCI	I_{LOAD} = 1µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1I} Highest (V_{BAT2} or V_{SCP}) – V_{GB2I} Highest (V_{DCIN} or V_{SCP}) – V_{GDCI}		 4.75 4.75 4.75	 6.7 6.7 6.7	 7.5 7.5 7.5	 V V V
V_{POFFI}	Input Gate Off Voltage GB1I GB2I GDCI	I_{LOAD} = –25µA Highest (V_{BAT1} or V_{SCP}) – V_{GB1I} Highest (V_{BAT2} or V_{SCP}) – V_{GB2I} Highest (V_{DCIN} or V_{SCP}) – V_{GDCI}			 0.18 0.18 0.18	 0.25 0.25 0.25	 V V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 6). V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, V_{VDDS} = 3.3V, V_{VCC2} = 5.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Thermistor							
	Thermistor Trip COLD-RANGE to OVER-RANGE	$C_{LOAD(MAX)}$ = 300pF (Note 9) R1A = R2A = 1130Ω ±1% R1B = R2B = 54900Ω ±1%	●	95	100	105	kΩ
	Thermistor Trip IDEAL-RANGE to COLD-RANGE	$C_{LOAD(MAX)}$ = 300pF (Note 9) R1A = R2A = 1130Ω ±1% R1B = R2B = 54900Ω ±1%	●	28.5	30	32.5	kΩ
	Thermistor Trip HOT-RANGE to IDEAL-RANGE	$C_{LOAD(MAX)}$ = 300pF (Note 9) R1A = R2A = 1130Ω ±1% R1B = R2B = 54900Ω ±1% C-Grade (Note 6) I-Grade (Note 6)	 ● ●	 2.85 2.83	 3 3	 3.15 3.15	 kΩ kΩ
	Thermistor Trip UNDER-RANGE to HOT-RANGE	$C_{LOAD(MAX)}$ = 300pF (Note 9) R1A = R2A = 1130Ω ±1% R1B = R2B = 54900Ω ±1%	●	425	500	575	Ω
Logic Levels							
	SCL/SCL1/SCL2/SDA/SDA1/ SDA2 Input Low Voltage (V_{IL})		●			0.8	V
	SCL/SCL1/SCL2/SDA/SDA1/ SDA2 Input High Voltage (V_{IH})		●	2.1			V
	SCL/SCL1/SCL2/SDA/SDA1/ SDA2 Input Leakage Current	V_{SDA}, V_{SCL}, V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2} = 0.8V	●	–5		5	µA
	SCL/SCL1/SCL2/SDA/SDA1/ SDA2 Input Leakage Current	V_{SDA}, V_{SCL}, V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2} = 2.1V	●	–5		5	µA
I_{PULLUP}	SCL1/SDA1/SCL2/SDA2 Pull-Up Current When Not Connected to SMBus Host	V_{SCL1}, V_{SDA1}, V_{SCL2}, V_{SDA2} = 0.4V V_{VCC2} = 4.85V and 5.55V (Current is Through Internal Series Resistor and Schottky to V_{CC2})		165	220	350	µA
	SCL1/SDA1/SCL2/SDA2 Series Impedance to Host SMBus	V_{SDA1}, V_{SCL1}, V_{SDA2}, V_{SCL2} = 0.8V	●			300	Ω
	SCL/SDA Output Low Voltage (V_{OL}). LTC1760 Driving the Pin	I_{PULLUP} = 350µA	●			0.4	V
	SCL1/SDA1/SCL2/SDA2 Pullup Output Low Voltage (V_{OL}). LTC1760 Driving the Pin with Battery SMBus not Connected to Host SMBus	I_{PULLUP} Internal to LTC1760	●			0.4	V
	SCL1/SDA1/SCL2/SDA2 Output Low Voltage (V_{OL}). LTC1760 Driving the Pin with Battery SMBus Connected to Host SMBus	I_{PULLUP} = 350µA on Host Side	●			0.4	V
	SCL/SCL1/SCL2/SDA/SDA1/ SDA2/ $\overline{SMBALERT}$ Power Down Leakage	V_{VCC2} = 0V, V_{VDDS} = 0V, V_{SCL}, V_{SCL1}, V_{SCL2}, V_{SDA}, V_{SDA1}, V_{SDA2}, $V_{\overline{SMBALERT}}$ = 5.5V	●			2	µA
	$\overline{SMBALERT}$ Output Low Voltage (V_{OL})	I_{PULLUP} = 500µA	●			0.4	V
	$\overline{SMBALERT}$ Output Pull-Up Current	$V_{\overline{SMBALERT}}$ = 0.4V		3.5	10	17.5	µA
V_{IL_VDDS} V_{IH_VDDS}	V_{DDS} Input Low Voltage (V_{IL}) V_{DDS} Input High Voltage (V_{IH}) V_{DDS} Operating Voltage V_{DDS} Operating Current	 V_{SCL}, V_{SDA} = V_{VDDS} , V_{VDDS} = 5V	● ● ● 	 2.6 3 	 	1.5 5.5 18	V V V µA
V_{IL_MODE}	MODE Input Low Voltage (V_{IL})	V_{VCC2} = 4.85V	●			V_{VCC2} • 0.3	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 6). V_{DCIN} = 20V, V_{BAT1} = 12V, V_{BAT2} = 12V, V_{VDDS} = 3.3V, V_{VCC2} = 5.2V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH_MODE}	MODE Input High Voltage (V_{IH})	V_{VCC2} = 4.85V	●	V_{VCC2} • 0.7			V
	MODE Input Current (I_{IH})	MODE = V_{VCC2} • 0.7V, V_{VCC2} = 4.85V	●	–1		1	µA
	MODE Input Current (I_{IL})	MODE = V_{VCC2} • 0.3V, V_{VCC2} = 4.85V	●	–1		1	µA
Charger Timing							
$t_{TIMEOUT}$	Timeout for Wake-Up Charging and Controlled Charging		●	140	175	210	sec
t_{QUERY}	Sampling Rate Used by the LTC1760 to Update Charging Parameters				1		sec
SMBus Timing							
	SCL Serial-Clock High Period(t_{HIGH})	At I_{PULLUP} = 350µA, C_{LOAD} = 150pF (Note 8)	●	4			µs
	SCL Serial-Clock Low Period (t_{LOW})	At I_{PULLUP} = 350µA, C_{LOAD} = 150pF (Note 8)	●	4.7			µs
	SDA/SCL Rise Time (t_r)	C_{LOAD} = 150pF, RPU = 9.31k (Note 8)	●			1000	ns
	SDA/SCL Fall Time (t_f)	C_{LOAD} = 150pF, RPU = 9.31k (Note 8)	●			300	ns
	SMBus Accelerator Trip Voltage Range		●	0.8		1.42	V
	Start-Condition Setup Time ($t_{SU:STA}$)		●	4.7			µs
	Start-Condition Hold Time ($t_{HD:STA}$)		●	4			µs
	SDA to SCL Rising-Edge Setup Time ($t_{SU:DAT}$)		●	250			ns
	SDA to SCL Falling-Edge Hold Time, Slave Clocking in Data ($t_{HD:DAT}$)		●	300			ns
$t_{TIMEOUT\_SMB}$	The LTC1760 will Release the SMBus and Terminate the Current Master or Slave Command if the Command is not Completed Before this Time		●	25		35	ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Battery voltage must be adequate to drive gates of PowerPath P-channel FET switches. This does not affect charging voltage of the battery, which can be zero volts during wake-up charging.

Note 3: DCIN, BAT1, BAT2 are held at 12V and GDCI, GB1I, GB2I are forced to 10.5V. SCP is set at 12V to measure source current at GDCI, GB1I and GB2I. SCP is set at 11.9V to measure sink current at GDCI, GB1I and GB2I.

Note 4: Extrapolated from testing with C_L = 50pF.

Note 5: Accuracy dependent upon external sense resistor and compensation components.

Note 6: The LTC1760 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC1760C is guaranteed to meet specifications from 0°C to 70°C junction temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC1760I is guaranteed over the –40°C to 125°C operating junction temperature range.

Note 7: Charger servos to the value reported by a Voltage() query. This is the internal cell voltage measured by the battery electronics and may be lower than the terminal voltage. Refer to "Operation Section 3.7" for more information.

Note 8: C_{LOAD} is the combined capacitance on the host's SMBus connection and the selected battery's SMBus connection.

Note 9: C_{LOAD_MAX} is the maximum allowed combined capacitance on THxA, THxB and the battery's SafetySignalx connections.

Note 10: Does not include current supplied by V_{CC} to V_{CC2} (I_{VCC2_AC1} or I_{VCC2_AC0})

Note 11: Measured with thermistors not present, R_{VLIMIT} and R_{ILIMIT} removed and $\overline{SMBALERT}$ = 1. See Applications Information section: "Calculating IC Operating Current" for example on how to calculate total IC operating current.

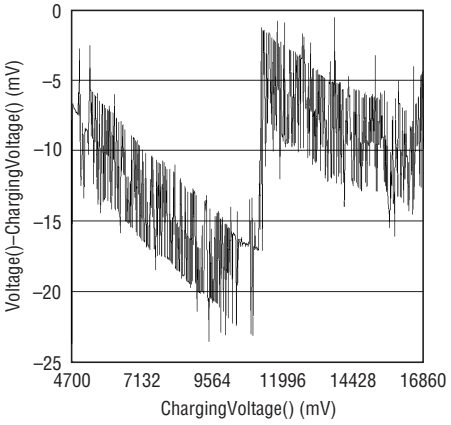
Note 12: Requested currents below 44mV/R_{SENSE} may not servo correctly due to charger offsets. The charging current for requested currents below 4mV/R_{SENSE} will be between 4mV/R_{SENSE} and (Requested Current – 8mA). Refer to Applications Information: "Setting Charger Output Current Limit" for values of R_{SENSE}.

Note 13: This limit is greater than the absolute maximum for the charger. Therefore, there is no effective limitation for the voltage when this option is selected.

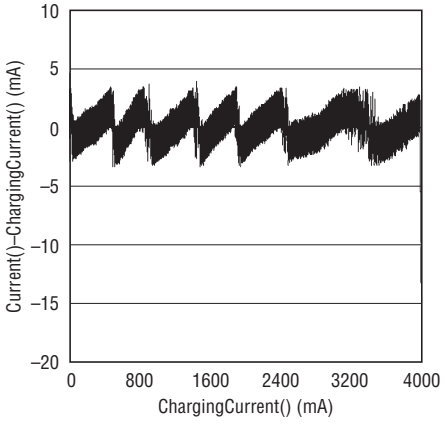
Note 14: Does not apply to Wake-Up Mode.

TYPICAL PERFORMANCE CHARACTERISTICS

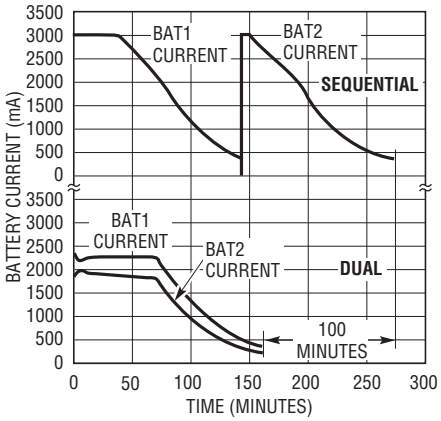
Charging Voltage Accuracy



Charging Current Accuracy

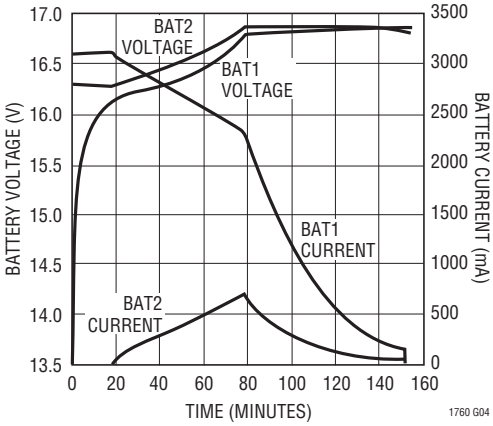


Dual Battery Charge Time vs Sequential Battery Charging



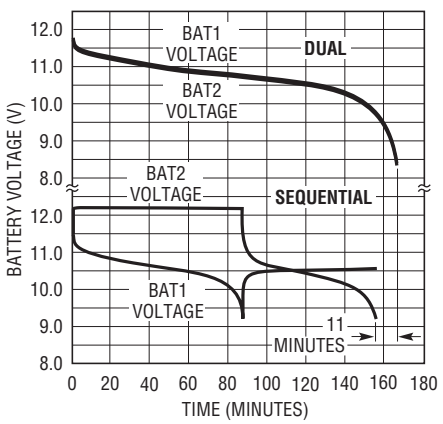
BATTERY TYPE: 10.8V Li-Ion (MOLTECH NI2020)
REQUESTED CURRENT = 3A
REQUESTED VOLTAGE = 12.3V
MAX CHARGER CURRENT = 4.1A

Dual Charging Batteries with Different Charge State



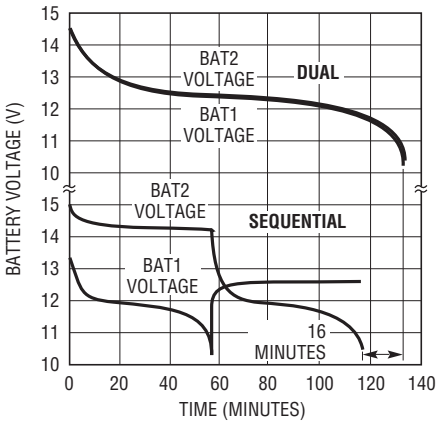
BAT1 INITIAL CAPACITY = 0%
BAT2 INITIAL CAPACITY = 90%
PROGRAMMED CHARGER CURRENT = 3A
PROGRAMMED CHARGER VOLTAGE = 16.8V

Dual Battery Discharge Time vs Sequential Battery Discharge (Li-Ion)



BATTERY TYPE: 10.8V Li-Ion (MOLTECH NI2020)
LOAD CURRENT = 3A

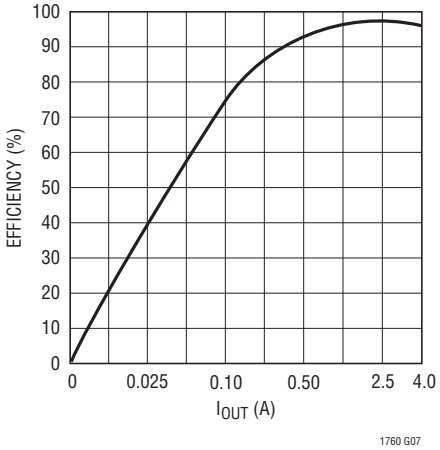
Dual Battery Dischage Time vs Sequential Battery Discharge (NiMH)



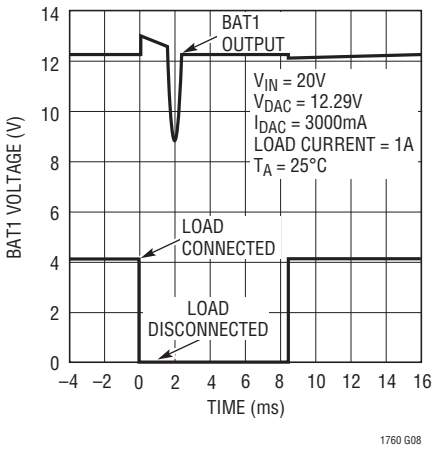
BATTERY TYPE: 12V NiMH (MOLTECH NJ1020)
LOAD: 33W

TYPICAL PERFORMANCE CHARACTERISTICS

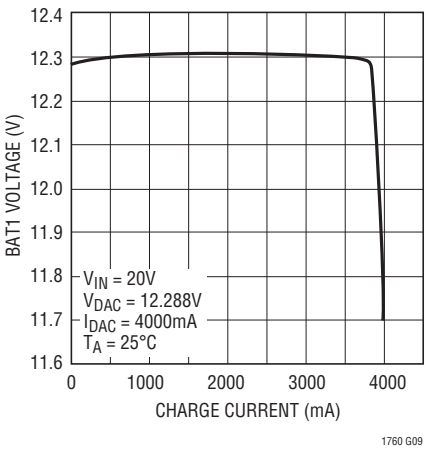
Efficiency vs Charging Current



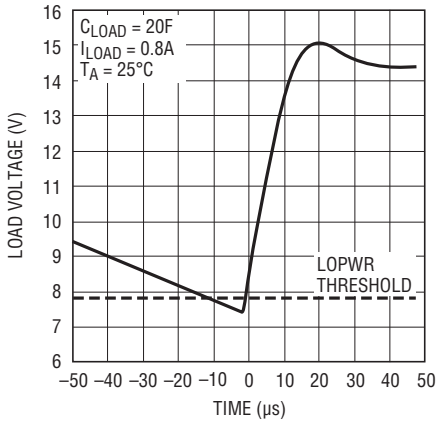
Load Dump



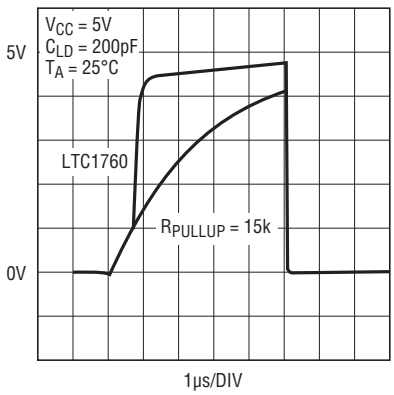
Load Regulation



PowerPath Switching 1 and 2



SMBus Accelerator Operation



PIN FUNCTIONS

Input Power Related

SCN (Pin 4): PowerPath Current Sensing Negative Input. This pin should be connected directly to the "bottom" (output side) of the sense resistor, R_{SC}, in series with the three PowerPath switch pairs, for detecting short-circuit current events. Also powers the LTC1760 internal circuitry when all other sources are absent.

SCP (Pin 5): PowerPath Current Sensing Positive Input. This pin should be connected directly to the "top" (switch side) of the sense resistor, R_{SC}, in series with the three PowerPath switch pairs, for detecting short-circuit current events.

GDCO (Pin 6): DCIN Output Switch Gate Drive. Together with GDCI, this pin drives the gate of the P-channel switch in series with the DCIN input switch.

GDCI (Pin 7): DCIN Input Switch Gate Drive. Together with GDCO, this pin drives the gate of the P-channel switch connected to the DCIN input.

PIN FUNCTIONS

GB1O (Pin 8): BAT1 Output Switch Gate Drive. Together with GB1I, this pin drives the gate of the P-channel switch in series with the BAT1 input switch.

GB1I (Pin 9): BAT1 Input Switch Gate Drive. Together with GB1O, this pin drives the gate of the P-channel switch connected to the BAT1 input.

GB2O (Pin 10): BAT2 Output Switch Gate Drive. Together with GB2I, this pin drives the gate of the P-channel switch in series with the BAT2 input switch.

GB2I (Pin 11): BAT2 Input Switch Gate Drive. Together with GB2O, this pin drives the gate of the P-channel switch connected to the BAT2 input.

CLP (Pin 36): The Positive Input to the Supply Current Limiting Amplifier CL1. The threshold is set at 100mV above the voltage at the DCIN pin. When used to limit supply current, a filter is needed to filter out the switching noise.

Battery Charging Related

V_{SET} (Pin 13): The Tap Point of a Programmable Resistor Divider which Provides Battery Voltage Feedback to the Charger. A capacitor from CSN to V_{SET} and from V_{SET} to GND provide necessary compensation and filtering for the voltage loop.

I_{TH} (Pin 14): The Control Signal of the Inner Loop of the Current Mode PWM. Higher I_{TH} voltage corresponds to higher charging current in normal operation. A capacitor of at least 0.1µF to GND filters out PWM ripple. Typical full-scale output current is 30µA. Nominal voltage range for this pin is 0V to 2.4V.

I_{SET} (Pin 15): A capacitor from I_{SET} to GND is required to filter higher frequency components from the delta-sigma I_{DAC}.

I_{LIMIT} (Pin 32): An external resistor (R_{ILIMIT}) is connected between this pin and GND. The value of the external resistor programs the range and resolution of the programmed charger current.

V_{LIMIT} (Pin 33): An external resistor (R_{VLIMIT}) is connected between this pin and GND. The value of the external resistor programs the range and resolution of the voltage DAC.

CSN (Pin 34): Current Amplifier CA1 Input. Connect this to the common output of the charger MUX switches.

CSP (Pin 35): Current Amplifier CA1 Input. This pin and the CSN pin measure the voltage across the charge current sense resistor, R_{SENSE}, to provide the instantaneous current signals required for both peak and average current mode operation.

COMP1 (Pin 37): The Compensation Node for the Amplifier CL1. A capacitor is required from this pin to GND if input current amplifier CL1 is used. At input adapter current limit, this node rises to 1V. By forcing COMP1 to GND, amplifier CL1 will be defeated (no adapter current limit). COMP1 can source 10µA.

BGATE (Pin 39): Drives the gate of the bottom external MOSFET of the battery charger buck converter.

SW (Pin 42): PWM Switch Node. Connected to the source of the top external MOSFET. Used as reference for top gate driver.

BOOST (Pin 43): Supply to Topside Floating Driver. The bootstrap capacitor is returned to this pin. Voltage swing at this pin is from a diode drop below V_{CC} to (DCIN + V_{CC}).

TGATE (Pin 44): Drives the gate of the top external MOSFET of the battery charger buck converter.

SCH1 (Pin 45), SCH2 (Pin 48): Charger MUX N-Channel Switch Source Returns. These two pins are connected to the sources of the back-to-back switch pairs Q3/Q4 and Q9/Q10 (see Typical Applications). A small pull-down current source returns these nodes to 0V when the switches are turned off.

GCH1 (Pin 46), GCH2 (Pin 47): Charger MUX N-Channel Switch Gate Drives. These two pins drive the gates of the back-to-back switch pairs, Q3/Q4 and Q9/Q10, between the charger output and the two batteries (see Typical Applications).

External Power Supply Pins

V_{PLUS} (Pin 1): Supply. The V_{PLUS} pin is connected via four internal diodes to the DCIN, SCN, BAT1, and BAT2 pins. Bypass this pin with a 0.1µF capacitor and a 1µF capacitor (see Typical Applications for complete circuit).

BAT1 (Pin 3), BAT2 (Pin 2): These two pins are the inputs from the two batteries for power to the LTC1760.

PIN FUNCTIONS

LOPWR (Pin 12): LOPWR Comparator Input from SCN External Resistor Divider to GND. If the voltage at LOPWR pin is lower than the LOPWR comparator threshold, then system power has failed and power is autonomously switched to a higher voltage source, if available.

DCDIV (Pin 16): External DC Source Comparator Input from DCIN External Resistor Divider to GND. If the voltage at DCDIV pin is above the DCDIV comparator threshold, then the AC_PRESENT bit is set and the wall adapter power is considered to be adequate to charge the batteries. If DCDIV rises more than 1.8V above V_{CC}, then all of the power path switches are latched off until all power is removed. A capacitor from DCDIV to GND is recommended to prevent noise-induced false emergency turn-off conditions from being detected. Refer to "Section 8.3" and "Typical Application".

DCIN (Pin 41): Supply. External DC power source. A 0.1µF bypass capacitor must be connected to this pin as close as possible. No series resistance is allowed, since the adapter current limit comparator input is also this pin.

Internal Power Supply Pins

V_{DDS} (Pin 20): Power Supply for SMBus Accelerators. Also used in conjunction with MODE pin to modify the LTC1760 operating mode.

GND (Pin 24): Ground for Low Power Circuitry.

V_{CC2} (Pin 25): Power Supply is used Primarily to Power Internal Logic Circuitry. Must be connected to V_{CC}.

PGND (Pin 38): High Current Ground Return for BGATE Driver.

V_{CC} (Pin 40): Internal Regulator Output. Bypass this output with at least a 2µF to 4.7µF capacitor. Do not use this regulator output to supply external circuitry except as shown in the application circuit.

SBS Interface Pins

SCL2 (Pin 17): SMBus Clock Signal to Smart Battery 2. Do not connect to an external pull-up. The LTC1760 connects this pin to an internal pull-up (I_{PULLUP}) when required.

SCL (Pin 18): SMBus Clock Signal to SMBus Host. Also used to determine flashing rate for stand-alone charge indicators. Requires an external pullup to V_{DDS} (normal SMBus operating mode). Connected to internal SMBus accelerator.

SCL1 (Pin 19): SMBus Clock Signal to Smart Battery 1. Do not connect to an external pull-up. The LTC1760 connects this pin to an internal pull-up (I_{PULLUP}) when required.

SDA2 (Pin 21): SMBus Data Signal to Smart Battery 2. Do not connect to an external pull-up. The LTC1760 connects this pin to an internal pull-up (I_{PULLUP}) when required.

SDA (Pin 22): SMBus Data Signal to SMBus Host. Also used to indicate charging status of Battery 2. Requires an external pullup to V_{DDS}. Connected to internal SMBus accelerator.

SDA1 (Pin 23): SMBus Data Signal to Smart Battery 1. Do not connect to an external pull-up. The LTC1760 connects this pin to an internal pull-up (I_{PULLUP}) when required.

MODE (Pin 26): Used in conjunction with V_{DDS} to allow SCL, SDA and $\overline{\text{SMBALERT}}$ to indicate charging status. May also be used as a hardware charge inhibit.

TH2B (Pin 27): Thermistor Force/Sense Connection to Smart Battery 2 SafetySignal. Connect to Battery 2 thermistor through resistor network shown in "Typical Application."

TH2A (Pin 28): Thermistor Force/Sense Connection to Smart Battery 2 SafetySignal. Connect to Battery 2 thermistor through resistor network shown in "Typical Application."

$\overline{\text{SMBALERT}}$ (Pin 29): Active Low Interrupt Pin. Signals SMBus Host that there has been a change of status in battery or AC presence. Open drain with weak current source pull-up to V_{CC2} (with Schottky to allow it to be pulled to 5V externally). Also used to indicate charging status of Battery 1.

TH1A (Pin 30): Thermistor Force/Sense Connection to Smart Battery 1 SafetySignal. Connect to Battery 1 thermistor through resistor network shown in "Typical Application."

TH1B (Pin 31): Thermistor Force/Sense Connection to Smart Battery 1 SafetySignal. Connect to Battery 1 thermistor through resistor network shown in "Typical Application."

BLOCK DIAGRAM

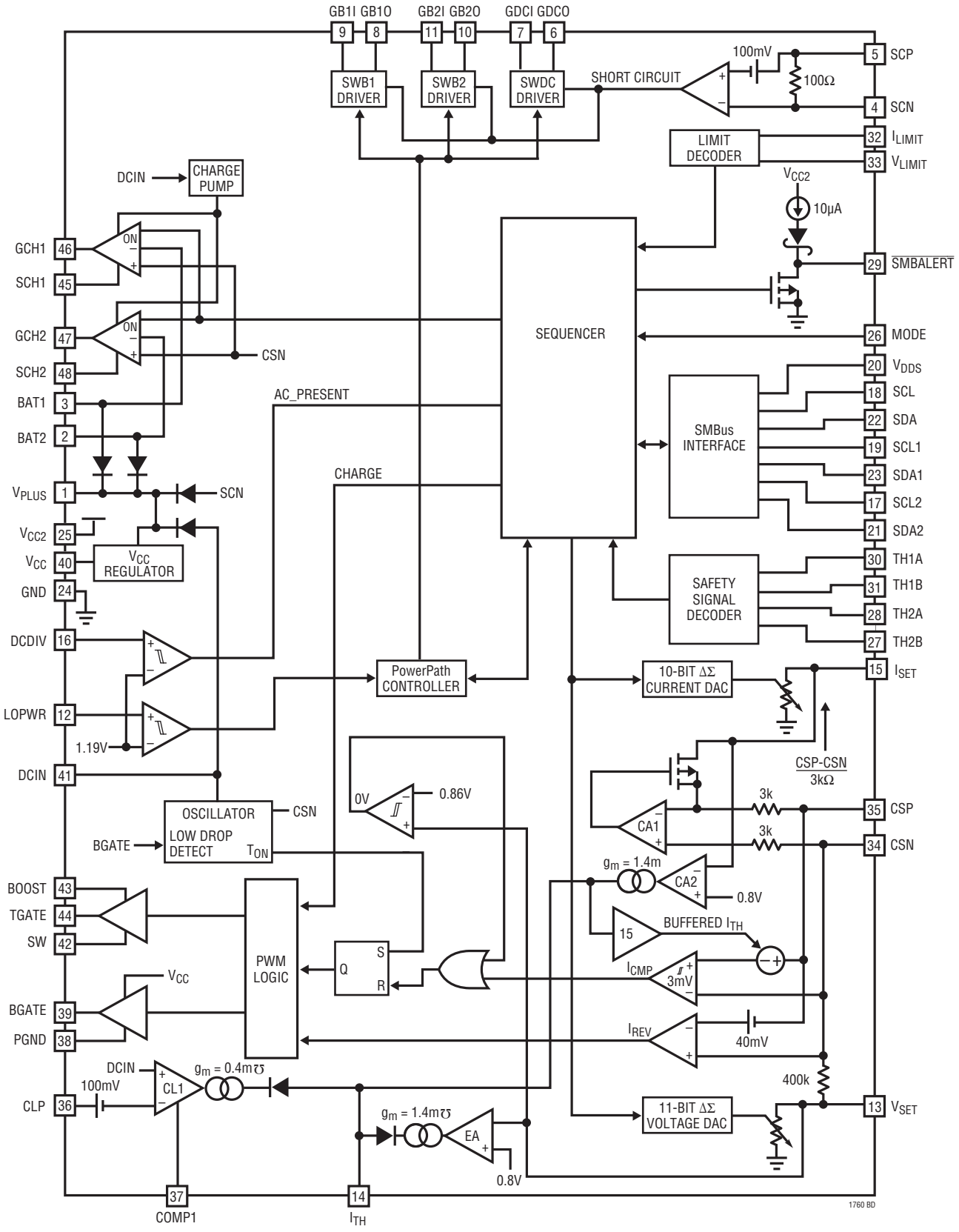


TABLE OF CONTENTS (For Operation Section)

OPERATION (Refer to Block Diagram and Typical Application Figure)

1 Overview

The LTC1760 is composed of an SMBus interface with dual port capability, a sequencer for managing system power and the charging and discharging of two batteries, a battery charger controller, charge MUX controller, PowerPath controller, a 10-bit current DAC (I_{DAC}) and 11-bit voltage DAC (V_{DAC}). When coupled with optional system software for generating composite battery information, it forms a complete Smart Battery System Manager for charging and selecting two smart batteries. The battery charger is controlled by the sequencer which uses a Level 3 SMBus interface to read ChargingVoltage(), Voltage(), ChargingCurrent(), Current(), Alarm() and BatteryMode(). This information, together with thermistor measurements allows the sequencer to select the charging battery and safely servo on voltage and current. Charging can be accomplished only if the voltage at DCDIV indicates that sufficient voltage is available from the input power source, usually an AC adapter. The charge MUX, which selects the battery to be charged, is capable of charging both batteries simultaneously. The charge MUX switch drivers are configured to allow charger current to share between the two batteries and to prevent current from flowing in a reverse direction in the switch. The amount of current that each battery receives will depend upon the relative capacity of each battery and the battery voltage. This can result in significantly shorter charging times (up to 50% for Li-Ion batteries) than sequential charging of each battery.

The sequencer also selects which of the pairs of PFET switches will provide power to the system load. If the system voltage drops below the threshold set by the LOPWR resistor divider, then all of the output-side PFETs are turned on quickly. The input-side PFETs act as diodes in this mode and power is taken from the highest voltage source available at the DCIN, BAT1, or BAT2 inputs. The input-side PowerPath switch driver that is delivering power then closes its input switch to reduce the power dissipation in the PFET bulk diode. In effect, this system provides diode-like behavior from the FET switches, without the attendant high power dissipation from diodes. The Host is informed of this 3-Diode mode status when it polls the PowerPath status register via the SMBus interface. High speed PowerPath switching at the LOPWR trip point is handled autonomously.

Simultaneous discharge of both batteries is supported. The switch drivers prevent reverse current flow in the switches and automatically discharge both batteries into the load, sharing current according to the relative capacity of the batteries. Simultaneous dual discharge can increase battery operating time by up to 10% by reducing losses in the switches and reducing internal battery losses associated with high discharge rates.

2 The SMBus Interface

2.1 SMBus Interface Overview

The SMBus interface allows the LTC1760 to communicate with two batteries and the SMBus Host. The SMBus Interface supports true dual port operation by allowing the SMBus Host to be connected to the SMBus of either battery. The LTC1760 is able to operate as an SMBus Master or Slave device. The LTC1760 SMBUS address is 0×14 (8-bit format).

References:

Smart Battery System Manager Specification: Revision 1.1, SBS Implementers Forum.

Smart Battery Data Specification: Revision 1.1, SBS Implementers Forum.

Smart Battery Charger Specification: Revision 1.1, SBS Implementers Forum

System Management Bus Specification: Revision 1.1, SBS Implementers Forum

I^2C-Bus and How to Use it: V1.0, Philips Semiconductor.

OPERATION

2.2 Data Bit Definition of Supported SMBus Functions.

Function	LTC1760 SMBus Mode	Access	SMBus Address	Command Code	Data Type	Data Bit or Nibble Definition/Allowed Values (See section 2.3 for Details) D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
BatterySystemState()	Slave	Read/ Write	7-bit: 0001_010b 8-bit: 0×14	0×01	Status/ Control	SMB_BAT4	SMB_BAT3	SMB_BAT2	SMB_BAT1	POWER_BY_BAT4	POWER_BY_BAT3	POWER_BY_BAT2	POWER_BY_BAT1	CHARGE_BAT4	CHARGE_BAT3	CHARGE_BAT2	CHARGE_BAT1	PRESENT_ BAT4	PRESENT_ BAT3	PRESENT_ BAT2	PRESENT_ BAT1
						0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1	0	0	0/1	0/1
BatterySystemStateCont()	Slave	Read/ Write	7-bit: 0001_010b 8-bit: 0×14	0×02	Status/ Control	RESERVED	RESERVED	RESERVED	RESERVED	CALIBRATE_BAT4	CALIBRATE_BAT3	CALIBRATE_BAT2	CALIBRATE_BAT1	RESERVED	CALIBRATE	CHARGER_POR	CHARGING_INHIBIT	CALIBRATE_REQUEST	CALIBRATE_REQUEST_SUPPORT	POWER_NOT_GOOD	AC_PRESENT
						0	0	0	0	0	0	0/1	0/1	0	0/1	0/1	0/1	0/1	1	0/1	0/1
BatterySystemInfo()	Slave	Read	7-bit: 0001_010b 8-bit: 0×14	0×04	Status	RESERVED				RESERVED				BATTERY SYSTEM REVISION				BATTERY SUPPORTED			
						0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1
LTC()	Slave	Read/ Write	7-bit: 0001_010b 8-bit: 0×14	0×3C	Status/ Control	POWER_OFF	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	TURBO	RESERVED	RESERVED	RESERVED	LTC_VERSION3	LTC_VERSION2	LTC_VERSION1	LTC_VERSION0
						0/1	0	0	0	0	0	0	1	0/1	0	0	0	0	0	0	1
BatteryMode()	Master	Read	7-bit: 0001_011b 8-bit: 0×16	0×03	Status	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	CONDITION_FLAG	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1

OPERATION

Function	LTC1760 Mode	Access	SMBus Address	Command Code	Data Type	Data Bit or Nibble Definition/Allowed Values (See section 2.3 for Details) D15	D14	D13	D12	D11	D10	D09	D08	D07	D06	D05	D04	D03	D02	D01	D00
Current()	Master	Read	7-bit: 0001_011b 8-bit: 0×16	0×0A	Value	IA15	IA14	IA13	IA12	IA11	IA10	IA09	IA08	IA07	IA06	IA05	IA04	IA03	IA02	IA01	IA00
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
Voltage()	Master	Read	7-bit: 0001_011b 8-bit: 0×16	0×09	Status/ Control	VA15	VA14	VA13	VA12	VA11	VA10	VA09	VA08	VA07	VA06	VA05	VA04	VA03	VA02	VA01	VA00
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
ChargingCurrent()	Master	Read	7-bit: 0001_011b 8-bit: 0×16	0×14	Status	IR15	IR14	IR13	IR12	IR11	IR10	IR09	IR08	IR07	IR06	IR05	IR04	IR03	IR02	IR01	IR00
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
ChargingVoltage()	Master	Read	7-bit: 0001_011b 8-bit: 0×16	0×15	Status/ Control	VR15	VR14	VR13	VR12	VR11	VR10	VR09	VR08	VR07	VR06	VR05	VR04	VR03	VR02	VR01	VR00
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
AlarmWarning()	Master	Read	7-bit: 0001_010b 8-bit: 0×16	0×16	Status	OVER_CHARGED	TERMINATE_CHARGE_ALARM	TERMINATE_CHARGE_RESERVED	OVER_TEMP_ALARM	TERMINATE_DISCHARGE_ALARM	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	FULLY_DISCHARGED	RESERVED	RESERVED	RESERVED	RESERVED
						0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
AlertResponse() see (1)	Slave	Read Byte	7-bit: 0001_100b 8-bit: 0×18	N/A	Register									ARA_ADD07	ARA_ADD06	ARA_ADD05	ARA_ADD04	ARA_ADD03	ARA_ADD02	ARA_ADD01	ARA_ADD00
														0	0	0	1	0	1	0	0

(1) Read-byte format. 0×14 is returned as the interrupt address of the LTC1760.

OPERATION

2.3 Description of Supported SMBus Functions

The functions are described as follows:

Function Name() (command code)

Description:

A brief description of the function.

Purpose:

The purpose of the function, and an example where appropriate.

SMBus Protocol: Refer to Section 2.5 and to the SMBus specification for more details.

Input, Output or Input/Output: A description of the data supplied to, or returned by, the function.

Whenever the LTC1760 encounters a valid command with invalid data, it ACKs the command, and ignores the invalid data. For example, if an attempt is made to select Battery 1 and 2 to simultaneously communicate with the system host, the LTC1760 will just ignore the request.

2.3.1 BatterySystemState() (0×01)

Description:

This function returns the present state of the LTC1760 and allows access to individual batteries. The information is broken into four nibbles that report:

Which battery is communicating with the SMBus Host

Which batteries, if any, or AC is powering the system

Which batteries are connected to the Smart Charger

Which batteries are present.

The LTC1760 provides a mechanism to notify the system whenever there is a change in its state. Specifically, the LTC1760 provides the system with a notification whenever:

- A battery is added or removed (Polling or $\overline{\text{SMBALERT}}$).
- AC power is connected or disconnected (Polling or $\overline{\text{SMBALERT}}$).
- The LTC1760 autonomously changes the configura-tion of the batteries supplying power (Polling only).
- The LTC1760 autonomously changes the configuration of the batteries being charged (Polling only).

Purpose:

Used by the SMBus Host to determine the present state of the LTC1760 and the attached batteries. It also may be used to determine the state of the battery system after the LTC1760 notifies the SMBus Host of a change via $\overline{\text{SMBALERT}}$.

SMBus Protocol: Read or Write Word.

Input/Output: word – Refer to "Section 2.2" for bit mapping.

SMB_BAT[4:1] Nibble

The read/write SMB_BAT[4:1] nibble is used by the SMBus Host to select with which individual battery to communicate or to determine with which individual battery it is communicating.

For example, an application that displays the remaining capacity of all batteries would write to this nibble to individually select each battery in turn and get its capacity.

Allowed values are:

0010b: SMBus Host is communicating with Battery 2.

0001b: SMBus Host is communicating with Battery 1. (Power On Reset Value)

To change this nibble, set only one of the lower two bits of this nibble high. All other values will simply be ignored.

POWER_BY_BAT[4:1] Nibble

The read only POWER_BY_BAT[4:1] nibble is used by the SMBus Host to determine which batteries are powering the system. All writes to this nibble will be ignored.

Allowed values are:

0011b: System powered by both Battery 2 and Battery 1 simultaneously.

0010b: System powered by Battery 2 only.

0001b: System powered by Battery 1 only.

0000b: System powered by AC adapter only.

OPERATION

CHARGE_BAT[4:1] Nibble

The read only CHARGE_BAT[4:1]nibble is used by the SMBus Host to determine which, if any, battery is being charged. All writes to this nibble will be ignored.

Allowed values are:

0011b: Both Battery 2 and Battery 1 being charged.

0010b: Only Battery 2 is being charged.

0001b: Only Battery 1 is being charged.

0000b: No battery being charged.

An indication that multiple batteries are being charged simultaneously does not indicate that the batteries are being charged at the same rate or that they will complete their charge at the same time. To actually determine when an individual battery will be fully charged, use the SMB_BAT[4:1] nibble to individually select the battery of interest and read the TimeToFull() value.

PRESENT_BAT[4:1] Nibble

The read only PRESENT_BAT[4:1]nibble is used by the SMBus Host to determine how many and which batteries are present. All writes to this nibble will be ignored.

Allowed values are:

0011b: Both Battery 2 and Battery 1 are present.

0010b: Only Battery 2 is present.

0001b: Only Battery 1 is present.

0000b: No batteries are present.

2.3.2 BatterySystemStateCont() (0×02)

Description:

This function returns additional state information of the LTC1760 and provides a mechanism to prohibit charging. This command also removes any requirement for the SMBus Host to communicate directly with the charger to obtain AC presence information. When the LTC1760 is used, access to the charger 8-bit address, 0×012, is blocked.

Purpose:

Used by the SMBus Host to retrieve additional state information from the LTC1760 and the overall system power configuration. It may also be used by the system to prohibit any battery charging.

SMBus Protocol: Read or Write Word.

Input/Output: word - Refer to “Section 2.2” for bit mapping

AC_PRESENT Bit

The read only AC_PRESENT bit is used to show the user the status of AC availability to power the system. It may be used internally by the SMBus Host in conjunction with other information to determine when it is appropriate to allow a battery conditioning cycle. Whenever there is a change in the AC status, the LTC1760 asserts $\overline{\text{SMBALERT}}$ low. In response, the system has to read this register to determine the actual presence of AC. The LTC1760 uses the DCDIV pin to measure the presence of AC.

Allowed values are:

1b: The LTC1760 has determined that AC is present.

0b: The LTC1760 has determined that AC is not present.

POWER_NOT_GOOD Bit

The read only POWER_NOT_GOOD bit is used to show that the voltage delivered to the system load is inadequate. This is determined by the LOPWR comparator.

The POWER_NOT_GOOD bit will also be set if the LTC1760 has detected a short circuit condition (see “Section 8.2”) or an emergency turn-off condition (see “Section 8.3”). Under either of these conditions the power paths will be shut off even if battery or DC power is available.

Allowed values are:

1b: The LTC1760 has determined that the voltage delivered to the system load is inadequate.

0b: The LTC1760 has determined that the voltage delivered to the system load is adequate.

CALIBRATE_REQUEST_SUPPORT Bit

The read only CALIBRATE_REQUEST_SUPPORT bit is always set high to indicate that the LTC1760 has a mechanism to determine when any of the attached batteries are in need of a calibration cycle.

OPERATION

CALIBRATE_REQUEST Bit

The read only CALIBRATE_REQUEST bit is set whenever the LTC1760 has determined that one or both of the connected batteries need a calibration cycle.

Allowed values are:

1b: The LTC1760 has determined that one or both batteries requires calibration.

0b: The LTC1760 has determined that neither battery require calibration.

CHARGING_INHIBIT Bit

The read/write CHARGING_INHIBIT bit is used by the SMBus Host to inhibit charging or to determine if charging is inhibited. This bit is also set if the MODE pin is used to inhibit charging.

Allowed values are:

1b: The LTC1760 will not allow any battery charging to occur.

0b: The LTC1760 may charge batteries as needed, (Power On Reset Value).

CHARGER_POR Bit

The read/write CHARGER_POR bit is used to force a charger power on reset.

Writing a 1 to this bit will cause a charger power on reset with the following effects.

- Charging will be turned off and wake-up charging will be resumed. This is the same as if the batteries were removed and then reinserted.
- The three minute wake-up watchdog timer will be restarted.

Writing a 0 to this bit has no effect. A read of this bit always returns a 0.

CALIBRATE Bit

The read/write CALIBRATE bit is used either to show the status of battery calibration cycles in the LTC1760 or to begin or end a calibration cycle.

CALIBRATE_BAT[4:1] Nibble

The read/write CALIBRATE_BAT[4:1]nibble is used by the SMBus Host to select the battery to be calibrated or to determine which individual battery is being calibrated.

Allowed read values are:

0010b: Battery 2 is being calibrated. CALIBRATE must be 1.

0001b: Battery 1 is being calibrated. CALIBRATE must be 1.

0000b: No batteries are being calibrated.

Allowed write values are:

0010b: Select Battery 2 for calibration.

0001b: Select Battery 1 for calibration.

0000b: Allow LTC1760 to choose battery to be calibrated.

All other values will simply be ignored. This provides a mechanism to update the other BatterySystemStateCont() bits without altering this nibble.

2.3.3 BatterySystemInfo() (0×04)

Description:

The SMBus Host uses this function to determine the capabilities of the LTC1760.

Purpose:

Allows the SMBus Host to determine the number of batteries the LTC1760 supports as well as the specification revision implemented by the LTC1760.

SMBus Protocol: Read Word

Input/Output: word — Refer to “Section 2.2” for bit mapping.

BATTERIES_SUPPORTED Nibble

The read only BATTERIES_SUPPORTED nibble is used by the SMBus Host to determine how many batteries the LTC1760 can support. The two-battery LTC1760 always returns 0011b for this nibble.

OPERATION

BATTERY_SYSTEM_REVISION Nibble

The read only BATTERY_SYSTEM_REVISION nibble reports the version of the Smart Battery System Manager specification supported.

LTC1760 always returns 1000b for this nibble, indicating Version 1.0 without optional PEC support.

2.3.4 LTC() (0×3C)

Description:

This function returns the LTC version nibble and allows the user to perform expanded Smart Battery System Manager functions.

Purpose:

Used by the SMBus Host to determine the version of the LTC1760 and to program and monitor TURBO and POWER_OFF special functions.

SMBus Protocol: Read or Write Word.

Input/Output: word — Refer to "Section 2.2" for bit mapping.

POWER_OFF Bit

This read/write bit allows the LTC1760 to turn off all power paths.

Allowed values:

1b: All power paths are off.

0b: All power paths are enabled. (power on reset value).

TURBO Bit

This read/write bit allows the LTC1760 to enter TURBO charging mode. Refer to "section 3.6".

Allowed values:

1b: Turbo charging mode enabled.

0b: Turbo charging mode disabled. (Power On Reset Value).

LTC_Version[3:0] Nibble

This read only nibble always returns 0001b as the LTC1760 version.

2.3.5 BatteryMode() (0×03)

Description:

This function is used by the LTC1760 to read the battery's Mode register.

Purpose:

Allows the LTC1760 to determine if a battery requires a conditioning/calibration cycle.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Input/Output: word — Refer to "Section 2.2" for bit mapping.

CONDITION_FLAG Bit

The CONDITION_FLAG bit is set whenever the battery requires calibration.

Allowed values:

1b: Battery requires calibration. (Also known as a Condition Cycle Request).

0b: Battery does not require calibration.

2.3.6 Voltage() (0×09)

Description:

This function is used by the LTC1760 to read the actual cell-pack voltage .

Purpose:

Allows the LTC1760 to determine the cell pack voltage and close the charging voltage servo loop.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Output: unsigned integer — battery terminal voltage in milli-volts. Refer to "Section 2.2" for bit mapping.

Units: mV.

Range: 0 to 65,535 mV.

OPERATION

2.3.7 Current() (0×0A)

Description:

This function is used by the LTC1760 to read the actual current being supplied through the battery terminals.

Purpose:

Allows the LTC1760 to determine how much current a battery is receiving through its terminals and close the charging current servo loop.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Output: signed integer (2's complement) — charge/discharge rate in mA increments - positive for charge, negative for discharge. Refer to "Section 2.2" for bit mapping.

Units: mA.

Range: 0 to 32,767 mA for charge or 0 to -32,768 mA for discharge.

2.3.8 ChargingCurrent() (0×14)

Description:

This function is used by the LTC1760 to read the Smart Battery's desired charging current.

Purpose:

Allows the LTC1760 to determine the maximum charging current.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Output: unsigned integer — maximum charger output current in mA. Refer to "Section 2.2" for bit mapping.

Units: mA.

Range: 0 to 65,534 mA.

2.3.9 ChargingVoltage() (0×15)

Description:

This function is used by the LTC1760 to read the Smart Battery's desired charging voltage.

Purpose:

Allows the LTC1760 to determine the maximum charging voltage.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Output: unsigned integer — charger output voltage in mV. Refer to "Section 2.2" for bit mapping.

Units: mV.

Range: 0 to 65,534 mV.

2.3.10 AlarmWarning() (0×16)

Description:

This function is used by the LTC1760 to read the Smart Battery's Alarm register.

Purpose:

Allows the LTC1760 to determine the state of all applicable alarm flags.

SMBus Protocol: Read Word. LTC1760 reads Battery 1 or Battery 2 as an SMBus Master.

Output: unsigned integer – Refer to "Section 2.2" for bit mapping.

OVER_CHARGED_ALARM Bit

The read only OVER_CHARGED_ALARM bit is used by the LTC1760 to determine if charging may continue.

Allowed values are:

1b: The LTC1760 will not charge this battery.

0b: The LTC1760 may charge this battery if other conditions permit charging.

TERMINATE_CHARGE_ALARM Bit

The read only TERMINATE_CHARGE_ALARM bit is used by the LTC1760 to determine if charging may continue.

Allowed values are:

1b: The LTC1760 will not charge this battery.

0b: The LTC1760 may charge this battery if other conditions permit charging.

OPERATION

TERMINATE_CHARGE_RESERVED Bit

The read only TERMINATE_CHARGE_RESERVED bit is used by the LTC1760 to determine if charging may continue.

Allowed values are:

1b: The LTC1760 will not charge this battery.

0b: The LTC1760 may charge this battery if other conditions permit charging.

OVER_TEMP_ALARM Bit

The read only OVER_TEMP_ALARM bit is used by the LTC1760 to determine if charging may continue.

Allowed values are:

1b: The LTC1760 will not charge this battery.

0b: The LTC1760 may charge this battery if other conditions permit charging.

TERMINATE_DISCHARGE_ALARM Bit

The read only TERMINATE_DISCHARGE_ALARM bit is used by the LTC1760 to determine if discharge from the battery is still allowed. This is used for PowerPath management and battery calibration.

Allowed values are:

1b: The LTC1760 will terminate calibration and should try to not use this battery in the power path. When all other power paths fail the LTC1760 will ignore this alarm and still try to supply system power from this battery.

0b: The LTC1760 may continue discharging this battery.

FULLY_DISCHARGED Bit

The read only FULLY_DISCHARGED bit is used by the LTC1760 to determine if discharge from the battery is still allowed. This is used for PowerPath management and battery calibration.

Allowed values are:

1b: The LTC1760 will terminate calibration and should try to not use this battery in the power path. When all other power paths fail the LTC1760 will ignore this alarm and still try to supply system power from this battery.

0b: The LTC1760 may continue discharging this battery.

2.3.11 AlertResponse()

Description:

The SMBus Host uses the Alert Response Address (ARA) to simultaneously address all devices on the SMBus and determine which devices are currently asserting $\overline{\text{SMBALERT}}$.

Purpose:

This command allows the SMBus Host to identify the subset of devices that have new status data. This reduces the number of reads required to refresh all status information from the system. The SMBus Host begins an ARA by transmitting the 8-bit address, 0×18, to all devices. ARA-compliant devices that are asserting $\overline{\text{SMBALERT}}$ will then simultaneously return their address on the next read byte. While transmitting their address each device monitors SDA. If a lower address is present, the device transmitting the higher address will see that SDA does not match and it will stop transmitting its address. When a device sees its full address has been received it will stop asserting $\overline{\text{SMBALERT}}$ and the Host will know to read status from this device. Subsequent ARA requests will allow the Host to complete the list of devices requiring servicing.

Output:

The LTC1760 will transmit its 8-bit address, 0x14, in response to an ARA request. The LTC1760 will stop transmitting its address if another device with a lower address is also responding to the ARA. The LTC1760 will de-assert $\overline{\text{SMBALERT}}$ when it successfully returns its address.

The following events will cause the LTC1760 to pull-down the SMBALERT# bus through the $\overline{\text{SMBALERT}}$ pin:

- Change of AC_PRESENT in the BatterySystemStateCont() function.
- Change of BATTERY_PRESENT in the BatterySystemState() function.
- Internal power on reset condition.

Refer to “Section 2.2” for bit mapping.

2.4 SMBus Dual Port Operation

The SMBus Interface includes the LTC1760’s SMBus controller, as well as circuitry to arbitrate and connect the battery and SMBus Host interfaces. The SMBus controller generates and interprets all LTC1760 SMBus functions.

OPERATION

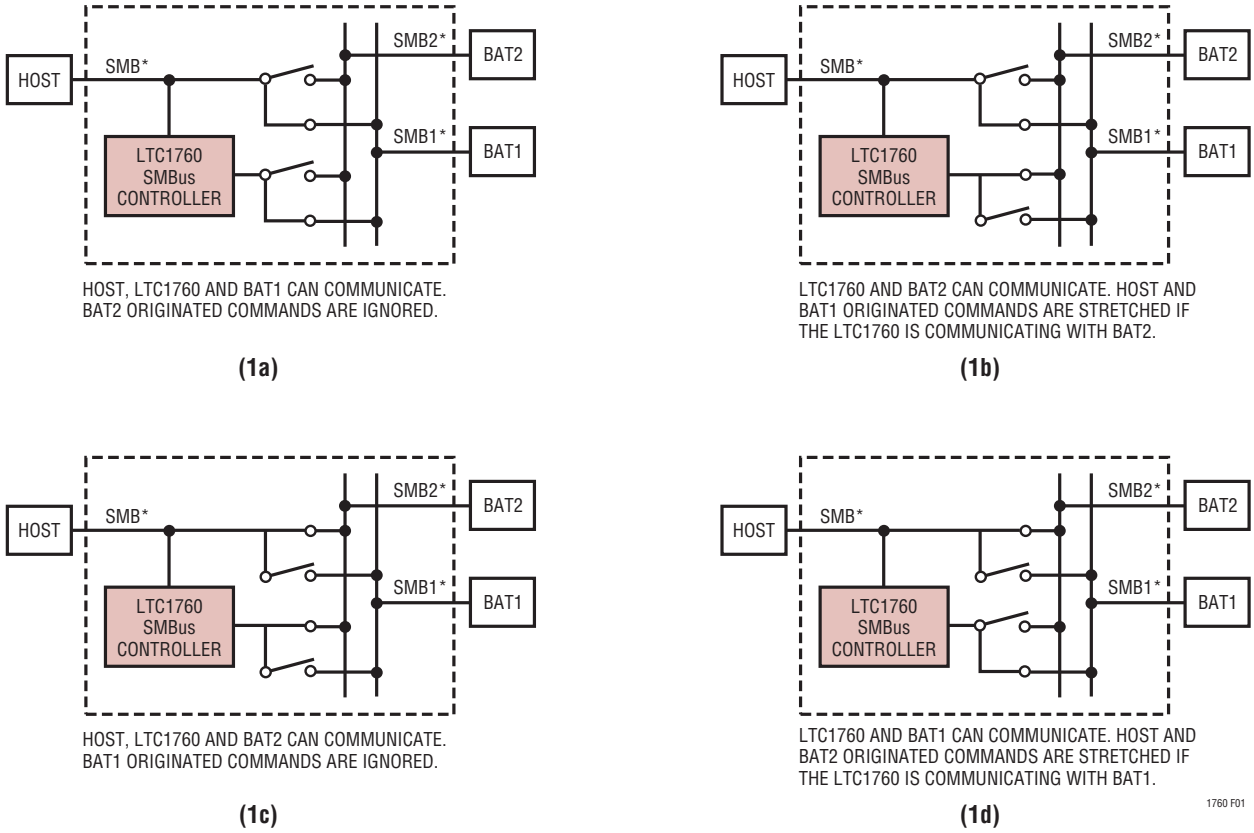


Figure 1. Switch Configurations Used by the LTC1760 for Managing Dual Port Battery Communication

The dual port operation allows the SMBus Host to be connected to the SMBus of either battery by setting the SMB_BAT[4:1] nibble. Arbitration is handled by stretching an SMBus start sequence when a bus collision might occur. Whenever configurations are switched, the LTC1760 will generate a harmless SMBus reset on SMB1 and SMB2 as required. The four possible configurations are illustrated in Figure 1. Sample SMBus communications are shown in Figures 2 and 3.

2.5 LTC1760 SMBus Controller Operation

SMBus communication with the LTC1760 is handled by the SMBus Controller, a sub-block of the SMBus Interface. Data is clocked into the SMBus Controller block shift register after the rising SCL edge. Data is clocked out of the SMBus Control block shift register after the falling edge of SCL.

The LTC1760 acting as a Slave will acknowledge (ACK) each byte of serial data. The Command byte will be NACKed if an invalid command code is transmitted to the LTC1760. The SMBus Controller must respond if addressed as a combined Smart Battery System Manager at 8-bit address 0×14. A valid address includes a legal Read/Write bit. The SMBus Controller will ignore invalid data although the data transmission with the invalid data will still be ACKed.

When the LTC1760, acting as a bus Master receives a NACK, it will terminate the transmission and provide a STOP condition on the bus.

Detection of a STOP condition, power on reset, or SMBus time out will reset the Controller to an initial state at any time.

The LTC1760 supports ARA, Write Word and Read Word protocols as an SMBus Slave. The LTC1760 supports Read Word protocol as an SMBus Master.

Refer to “System Management Bus Specification” for a complete description of required operation and symbols.

OPERATION

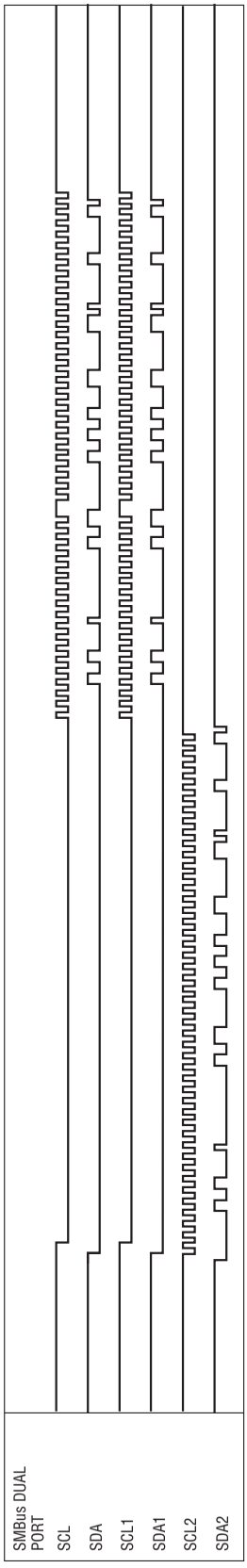


Figure 2. LTC1760 Stretches Host's Communication With Battery 1 While It Completes a Read Of Battery 2. (Configuration b)

OPERATION

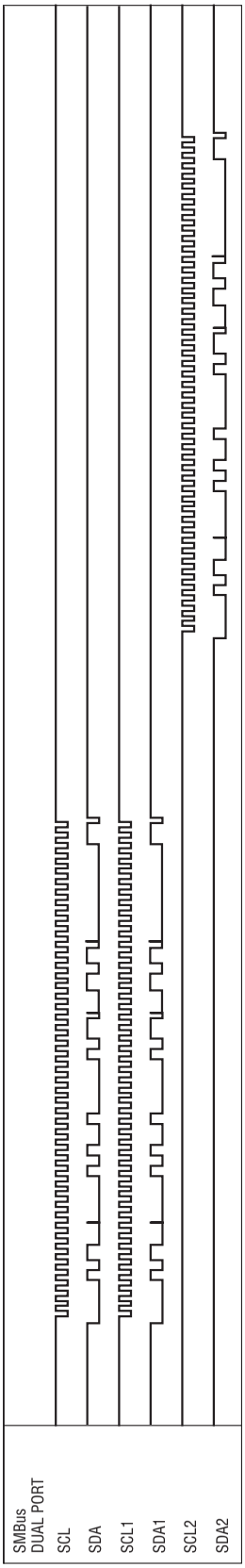


Figure 3. LTC1760 Queries Battery 1 Followed By Battery 2 For Requested Current. (Configuration b)