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16-/14-/11-Bit 2.7Gsps DACs

FEATURES

- 80dBc SFDR at 50MHz f_{OUT}
- >68dBc SFDR from DC to 1080MHz f_{OUT}
- 40mA Nominal Full-Scale, ±1V Output Compliant
- 10mA to 60mA Adjustable Full-Scale Current Range
- Single or Dual Port DDR LVDS and DHSTL Interface
- Low Latency (7.5 Cycles for Single Port, 11 Cycles for Dual Port)
- >78dBc 2-Tone IMD from DC to 1000MHz f_{OUT}
- –156dBc/Hz Additive Phase Noise at 1MHz Offset for 65MHz f_{OUT}
- 170-Lead (9mm × 15mm) BGA Package

APPLICATIONS

- Broadband Communication Systems
- DOCSIS CMTS
- Direct RF Synthesis
- Radar
- Instrumentation
- Automatic Test Equipment

DESCRIPTION

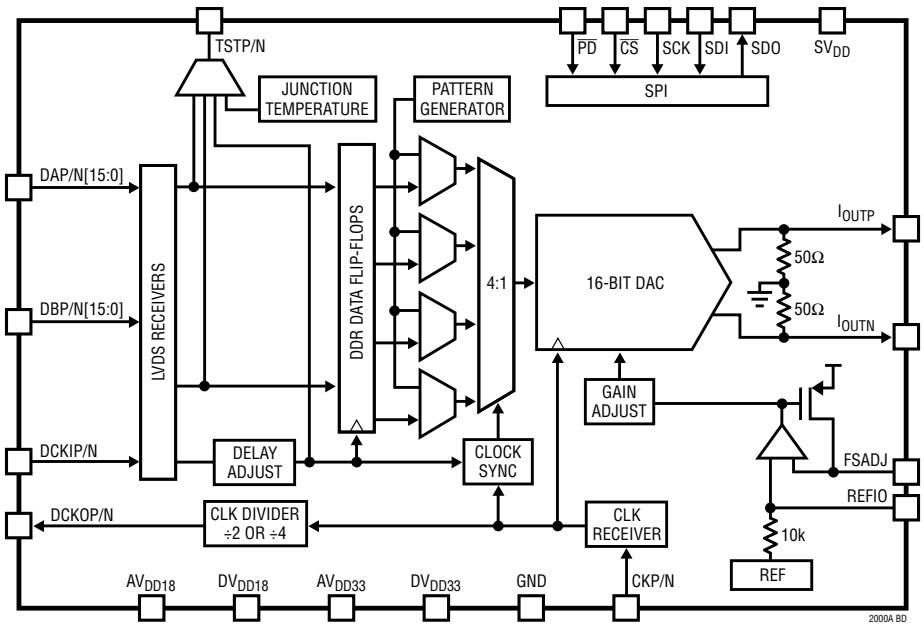
The LTC®2000A is a family of 16-/14-/11-bit 2.7Gsps current steering DACs with exceptional spectral purity.

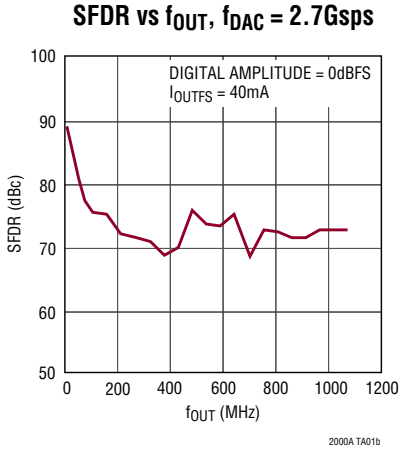
The single (1.35Gsps mode) or dual (2.7Gsps mode) port source synchronous LVDS interface supports data rates of up to 1.35Gbps using a 675MHz DDR data clock, which can be either in quadrature or in phase with the data. An internal synchronizer automatically aligns the data with the DAC sample clock.

Additional features such as pattern generation, LVDS loopout and junction temperature sensing simplify system development and testing.

A serial peripheral interface (SPI) port allows configuration and read back of internal registers. Operating from 1.86V and 3.3V supplies, the LTC2000A consumes 2.41W at 2.7Gsps and 1.43W at 1.35Gsps.

BLOCK DIAGRAM





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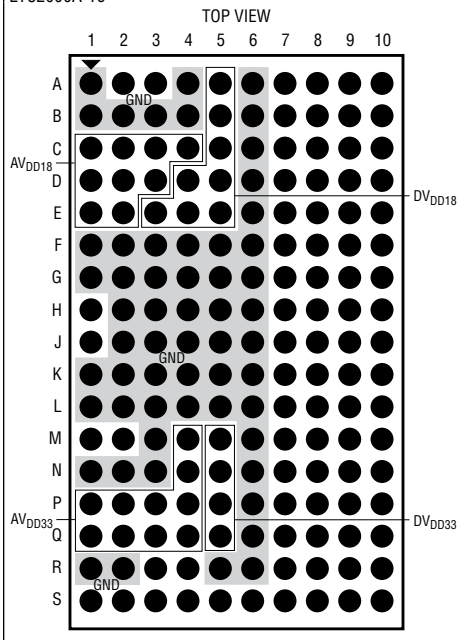
ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

AV_{DD33}, DV_{DD33}, SV_{DD} ..... –0.3V to 4V
AV_{DD18}, DV_{DD18} ..... –0.3V to 2V
I_{OUTP}, I_{OUTN} ..... –1.2V to Min (AV_{DD33} + 0.3V, 4V)
FSADJ, REFIO ..... –0.3V to Min (AV_{DD33} + 0.3V, 4V)
DCKIP, DCKIN ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
DCKOP, DCKON ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
DAP/N, DBP/N ..... –0.3V to Min (DV_{DD33} + 0.3V, 4V)
TSTP, TSTN ..... –0.3V to Min (AV_{DD33} + 0.3V, 4V)
CKP, CKN ..... –0.3V to Min (AV_{DD18} + 0.3V, 2V)
$\overline{CS}$, $\overline{PD}$, SCK, SDI, SDO ... –0.3V to Min (SV_{DD} + 0.3V, 4V)
Operating Temperature Range
LTC2000AC ..... 0°C to 70°C
LTC2000AI ..... –40°C to 85°C
Maximum Junction Temperature ..... 125°C
Storage Temperature Range ..... –55°C to 125°C
Lead Temperature (Soldering, 10 sec) ..... 260°C

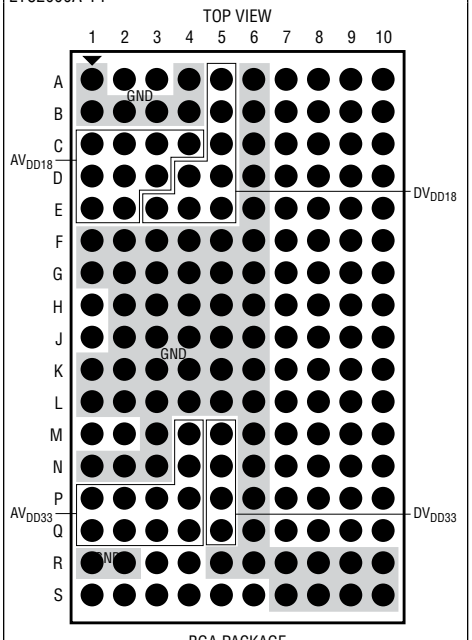
PIN CONFIGURATION

LTC2000A-16



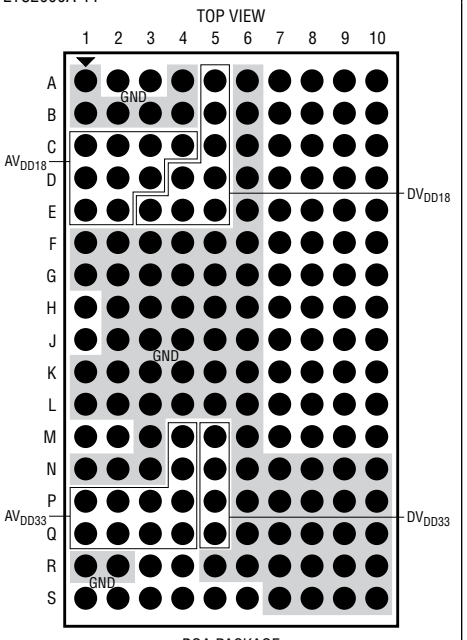
BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

LTC2000A-14



BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

LTC2000A-11



BGA PACKAGE
170-LEAD (9mm × 15mm × 1.54mm)
T_{JMAX} = 125°C, θ_{JA} = 20°C/W, θ_{JB} = 8°C/W,
θ_{JCtop} = 9°C/W, $\theta_{JCbottom}$ = 3°C/W

ORDER INFORMATION

LTC2000A C Y –16 #PBF

LEAD FREE DESIGNATOR
PBF = Lead Free

RESOLUTION
16 = 16-Bit Resolution
14 = 14-Bit Resolution
11 = 11-Bit Resolution

PACKAGE TYPE
170-Lead (15mm × 9mm × 1.54mm) BGA

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)

PRODUCT PART NUMBER

PART NUMBER	BALL FINISH	PART MARKING*	PACKAGE TYPE	MSL RATING	TEMPERATURE RANGE
LTC2000ACY-16#PBF	SAC305 (RoHS)	LTC2000Y-16	BGA	3	0°C to 70°C
LTC2000ACY-14#PBF	SAC305 (RoHS)	LTC2000Y-14	BGA	3	0°C to 70°C
LTC2000ACY-11#PBF	SAC305 (RoHS)	LTC2000Y-11	BGA	3	0°C to 70°C
LTC2000AIY-16#PBF	SAC305 (RoHS)	LTC2000Y-16	BGA	3	–40°C to 85°C
LTC2000AIY-14#PBF	SAC305 (RoHS)	LTC2000Y-14	BGA	3	–40°C to 85°C
LTC2000AIY-11#PBF	SAC305 (RoHS)	LTC2000Y-11	BGA	3	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.8V to 1.92V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, 12.5Ω load from $I_{OUTP/N}$ to GND including internal 50Ω termination, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC Performance							
	Resolution	LTC2000A-16	●	16			Bits
		LTC2000A-14	●	14			Bits
		LTC2000A-11	●	11			Bits
DNL	Differential Nonlinearity	LTC2000A-16	●		±0.5	±2.7	LSB
		LTC2000A-14	●		±0.2	±1	LSB
		LTC2000A-11	●		±0.1	±0.5	LSB
INL	Integral Nonlinearity	LTC2000A-16	●		±1	±4	LSB
		LTC2000A-14	●		±0.5	±2	LSB
		LTC2000A-11	●		±0.2	±1	LSB
	Offset Error	LTC2000A-16	●			±0.05	% FSR
		LTC2000A-14	●			±0.06	% FSR
		LTC2000A-11	●			±0.09	% FSR
	Offset Error Drift				1		ppm/°C
	Gain Error				±0.5		% FSR
	Gain Error Drift				5		ppm/°C
	Power Supply Rejection Ratio	Full-Scale; AV_{DD33} = 3.135V to 3.465V			69		dB
Analog Output							
	Full-Scale Output Current	R_{FSADJ} = 500Ω			40		mA
	Output Compliance Range		●	–1		1	V
	Output Resistance	$I_{OUTP/N}$ to GND	●	42	50	58	Ω
	Output Capacitance				6		pF
	Output Bandwidth	$R_{IOUTP/N}$ = 12.5Ω, –3dB Excluding sin(x)/x			2.1		GHz
AC Performance							
	Maximum Update Rate	Dual-Port Mode Single-Port Mode	● ●	2.7 1.35			Gsps Gsps
SFDR	Spurious Free Dynamic Range f_{DAC} = 1.25Gsps, 0dBFS	f_{OUT} = 50MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 250MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75%			82 82 74 74		dBc dBc dBc dBc
	Spurious Free Dynamic Range f_{DAC} = 2.7Gsps, 0dBFS	f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 200MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 1000MHz, LIN_DIS = 0, LIN_GN = 75%	 ● 	 67 	75 72 75 72		dBc dBc dBc dBc
		f_{OUT} = 500MHz, LIN_DIS = 1 f_{OUT} = 1000MHz, LIN_DIS = 1			67 61		dBc dBc
IMD	2-Tone Intermodulation Distortion $f_{OUT2} = f_{OUT1} + 1.25MHz$ f_{DAC} = 1.25Gsps, –6dBFS	f_{OUT} = 50MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 100MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 250MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75%			103 93 97 84		dBc dBc dBc dBc
	2-Tone Intermodulation Distortion $f_{OUT2} = f_{OUT1} + 1.25MHz$ f_{DAC} = 2.7Gsps, –6dBFS	f_{OUT} = 100MHz, LIN_DIS = 1 f_{OUT} = 200MHz, LIN_DIS = 1 f_{OUT} = 500MHz, LIN_DIS = 1 f_{OUT} = 1000MHz, LIN_DIS = 1			87 86 82 80		dBc dBc dBc dBc
		f_{OUT} = 500MHz, LIN_DIS = 0, LIN_GN = 75% f_{OUT} = 1000MHz, LIN_DIS = 0, LIN_GN = 75%			79 68		dBc dBc

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.8V to 1.92V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, 12.5Ω load from $I_{OUTP/N}$ to GND including internal 50Ω termination, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
NSD	Noise Spectral Density 0dBFS Single Tone, f_{DAC} = 2.7Gsps, I_{OUTFS} = 40mA	LTC2000A-16, f_{OUT} = 100MHz LTC2000A-16, f_{OUT} = 350MHz LTC2000A-16, f_{OUT} = 550MHz LTC2000A-16, f_{OUT} = 950MHz			–164 –158 –155 –153		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
		LTC2000A-14, f_{OUT} = 100MHz LTC2000A-14, f_{OUT} = 350MHz LTC2000A-14, f_{OUT} = 550MHz LTC2000A-14, f_{OUT} = 950MHz			–163 –158 –155 –153		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
		LTC2000A-11, f_{OUT} = 100MHz LTC2000A-11, f_{OUT} = 350MHz LTC2000A-11, f_{OUT} = 550MHz LTC2000A-11, f_{OUT} = 950MHz			–156 –154 –153 –150		dBm/Hz dBm/Hz dBm/Hz dBm/Hz
	Phase Noise f_{DAC} = 2.7Gsps, f_{OUT} = 65MHz 0dBFS Single Tone, I_{OUTFS} = 40mA	10kHz Offset 1MHz Offset			–141 –156		dBc/Hz dBc/Hz
WCDMA ACLR	WCDMA ACLR (Single Carrier) Adjacent/Alternate Adjacent Channel	f_{DAC} = 2.7Gsps, f_{OUT} = 350MHz f_{DAC} = 2.7Gsps, f_{OUT} = 950MHz			78/79 72/75		dBc dBc
Latency							
	Latency (Note 5)	Single-Port Mode Dual-Port Mode, DAP/N Data Dual-Port Mode, DBP/N Data			7.5 10 11		Cycles Cycles Cycles
	Aperture Delay	CKP/N Rising to $I_{OUTP/N}$ Transition			3		ns
	Settling Time	±0.1% FSR, Full-Scale Step			2.2		ns
Reference							
	Output Voltage		●	1.225	1.25	1.275	V
	Input Voltage		●	1.1		1.4	V
	Reference Temperature Coefficient				±25		ppm/°C
	Output Impedance				10		kΩ
DAC Clock Inputs (CKP, CKN)							
	Differential Input Voltage Range		●	±0.3		±1.8	V
	Common-Mode Input Voltage	Set Internally			1		V
	Sampling Clock Frequency		●	50		2700	MHz
	Input Impedance				5		kΩ
LVDS Inputs (DCKIP, DCKIN, DAP/N, DBP/N)							
	Differential Input Voltage Range		●	±0.2		±0.6	V
	Common-Mode Voltage Range		●	0.4		1.8	V
	Differential Input Impedance		●	95	120	145	Ω
	Maximum Data Rate		●			1350	Mbps
	LVDS Clock Frequency		●	25		675	MHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.8V to 1.92V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, 12.5Ω load from $I_{OUTP/N}$ to GND including internal 50Ω termination, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LVDS Output (DCKOP, DCKON)							
	Differential Output Voltage	100Ω Differential Load, DCKO_ISEL = 0 50Ω Differential Load, DCKO_ISEL = 1	● ●	0.24 0.24	0.36 0.36	0.48 0.48	V V
	Common-Mode Output Voltage		●	1.075	1.2	1.325	V
	Internal Termination Resistance	DCKO_TRM = 1			100		Ω
CMOS Digital Inputs ($\overline{CS}$, $\overline{PD}$, SCK, SDI)							
V_{IH}	Digital Input High Voltage		●	70			$\%V_{SVDD}$
V_{IL}	Digital Input Low Voltage		●			30	$\%V_{SVDD}$
I_{LK}	Digital Input Leakage	V_{IN} = GND or SV_{DD}	●			±10	µA
C_{IN}	Digital Input Capacitance				8		pF
CMOS Digital Output (SDO)							
V_{OH}	Digital Output High Voltage	I_{SOURCE} = 0.2mA	●	85			$\%V_{SVDD}$
V_{OL}	Digital Output Low Voltage	I_{SINK} = 1.6mA	●			15	$\%V_{SVDD}$
	Hi-Z Output Leakage		●			±10	µA
	Hi-Z Output Capacitance				8		pF
Power Supply							
V_{VDD33}	AV_{DD33}, DV_{DD33} Supply Voltage		●	3.135	3.3	3.465	V
V_{VDD18}	AV_{DD18}, D_{VDD18} Supply Voltage		●	1.8	1.86	1.92	V
V_{SVDD}	SV_{DD} SPI Supply Voltage		●	1.71		3.465	V
I_{AVDD33}	AV_{DD33} Supply Current, AV_{DD33} = 3.3V	$\overline{PD}$ = SV_{DD} $\overline{PD}$ = GND	● ●		68 0.1	78 10	mA µA
I_{DVDD33}	DV_{DD33} Supply Current, DV_{DD33} = 3.3V	$\overline{PD}$ = SV_{DD} $\overline{PD}$ = GND	● ●		8 0.1	14 5	mA µA
I_{AVDD18}	AV_{DD18} Supply Current, AV_{DD18} = 1.86V	f_{DAC} = 2700MHz f_{DAC} = 1350MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND	● ● ● ●		780 425 23 3	870 480 27 180	mA mA mA µA
I_{DVDD18}	DV_{DD18} Supply Current, DV_{DD18} = 1.86V	f_{DAC} = 2700MHz f_{DAC} = 1350MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND	● ● ● ●		380 210 10 0.1	440 240 14 240	mA mA mA µA
I_{SVDD}	SV_{DD} Supply Current (Note 4), SV_{DD} = 3.3V	f_{SCK} = 0Hz	●		0.1	5	µA
	Total Power Dissipation	f_{DAC} = 2700MHz f_{DAC} = 1350MHz f_{DAC} = 0Hz, $\overline{PD}$ = SV_{DD} f_{DAC} = 0Hz, $\overline{PD}$ = GND			2408 1432 312 6		mW mW mW µW

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. AV_{DD18}, DV_{DD18} = 1.8V to 1.92V, AV_{DD33}, DV_{DD33} = 3.135V to 3.465V, SV_{DD} = 1.71V to 3.465V, R_{FSADJ} = 500Ω, output load 50Ω double terminated, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_1	SDI Valid to SCK Setup	(Note 3)	●	4			ns
t_2	SDI Valid to SCK Hold	(Note 3)	●	4			ns
t_3	SCK High Time	(Note 3)	●	9			ns
t_4	SCK Low Time	(Note 3)	●	9			ns
t_5	$\overline{CS}$ Pulse Width	(Note 3)	●	10			ns
t_6	SCK High to $\overline{CS}$ High	(Note 3)	●	7			ns
t_7	$\overline{CS}$ Low to SCK High	(Note 3)	●	7			ns
t_{10}	$\overline{CS}$ High to SCK High	(Note 3)	●	7			ns
t_{13}	SCK Low to SDO Valid	Unloaded (Note 3)	●	10			ns
	SCK Frequency	50% Duty Cycle (Note 3)	●			50	MHz
t_{11}	LVDS DAP/N, DBP/N to DCKI Setup Time (Note 3)	DCKI_Q = 1 DCKI_Q = 0, DCKI_TADJ = 000	● ●	200 570			ps ps
t_{12}	LVDS DAP/N, DBP/N to DCKI Hold Time (Note 3)	DCKI_Q = 1 DCKI_Q = 0, DCKI_TADJ = 000	● ●	200 –170			ps ps

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltages are with respect to GND.

Note 3: Guaranteed by design and not production tested.

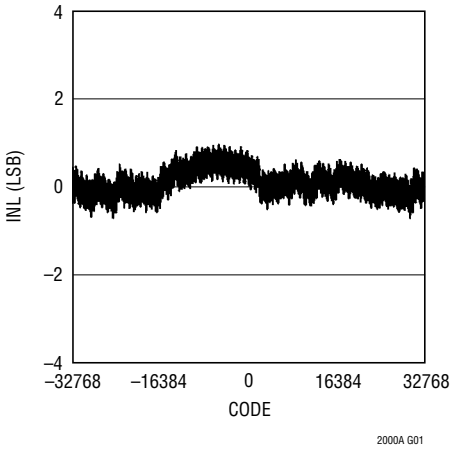
Note 4: Digital inputs at 0V or SV_{DD}.

Note 5: Latency is the delay from a transition on DCKIP/N until the CKP/N transition which causes the sample on DAP/N or DBP/N to appear at the DAC output $I_{OUTP/N}$, as measured in DAC sample clock (CKP/N) cycles.

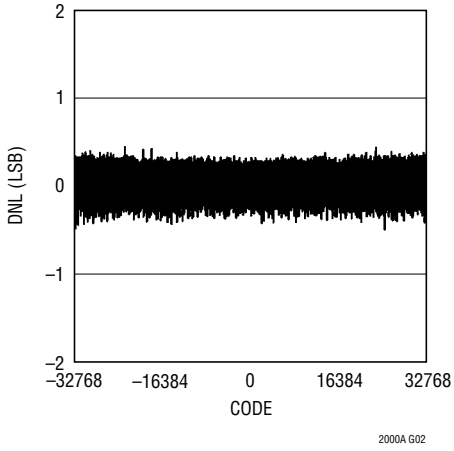
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, unless otherwise noted.

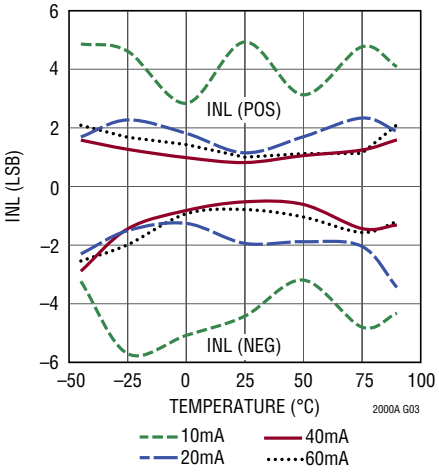
LTC2000A-16 Integral Nonlinearity (INL)



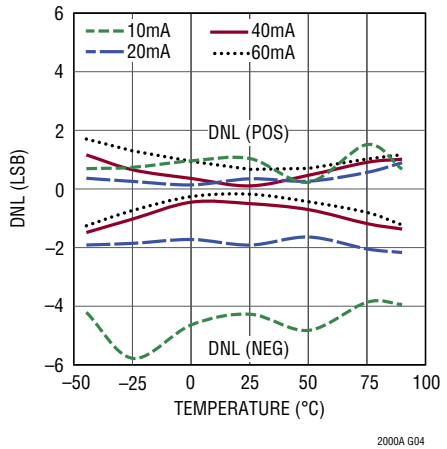
LTC2000A-16 Differential Nonlinearity (DNL)



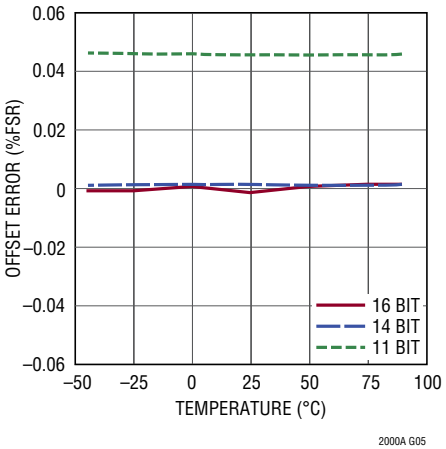
INL vs I_{OUTFS} and Temperature



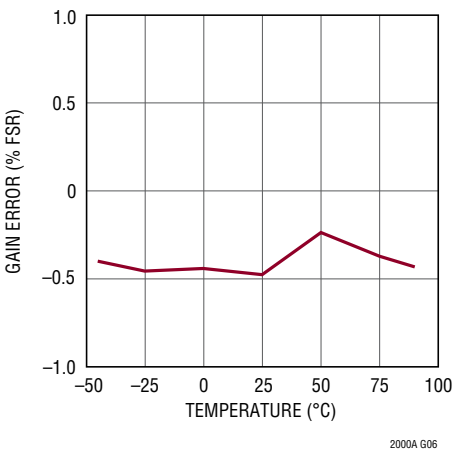
DNL vs I_{OUTFS} and Temperature



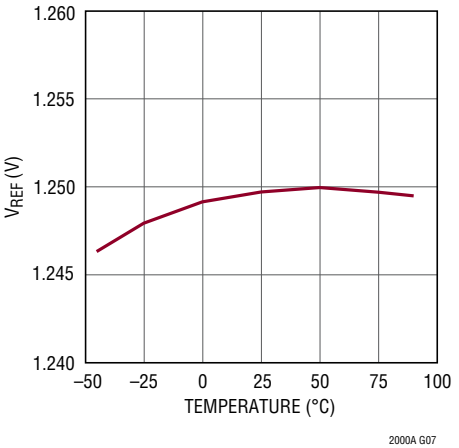
Offset Error vs Temperature



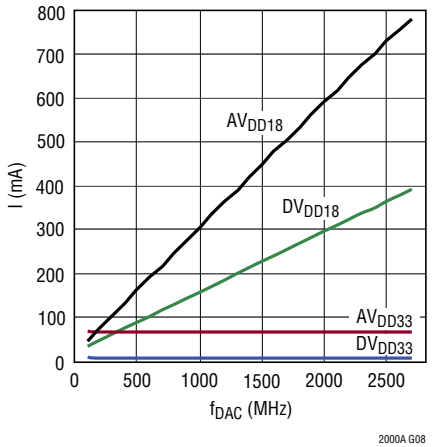
Gain Error vs Temperature



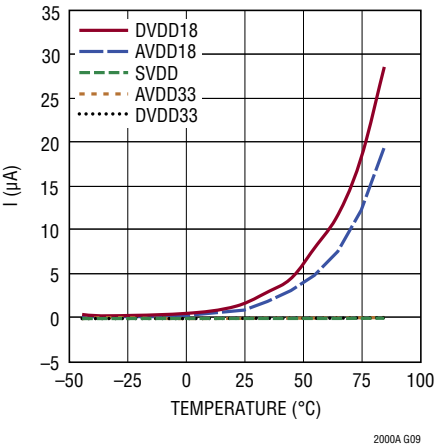
Reference Output Voltage vs Temperature



Supply Current vs f_{DAC}



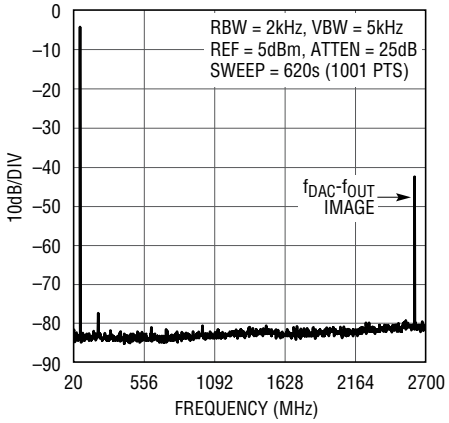
Shutdown Current vs Temperature



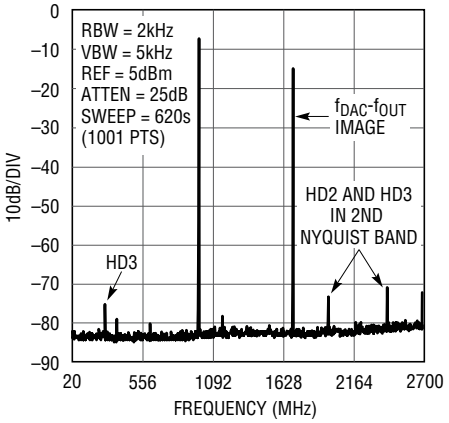
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

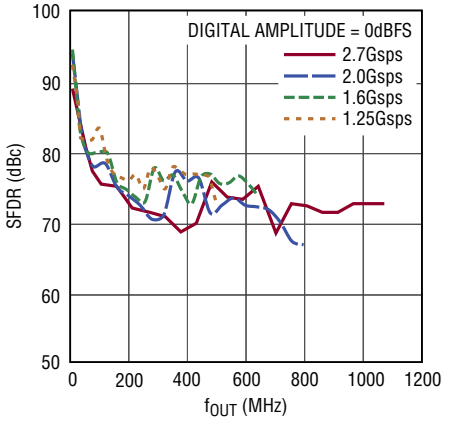
Single-Tone Spectrum at f_{OUT} = 70MHz, f_{DAC} = 2.7Gsps



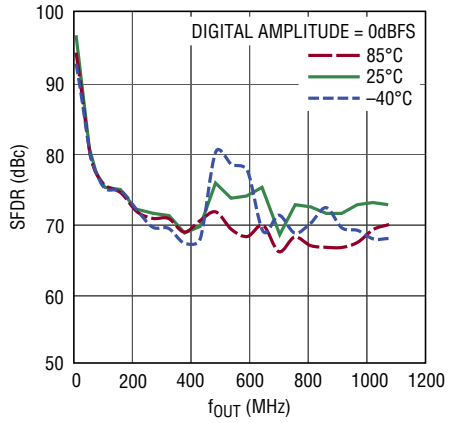
Single-Tone Spectrum at f_{OUT} = 990MHz, f_{DAC} = 2.7Gsps



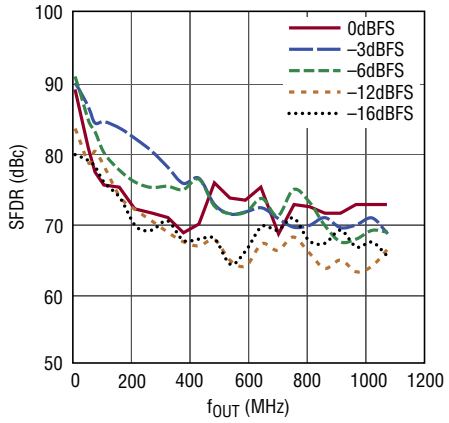
SFDR vs f_{OUT} and f_{DAC}



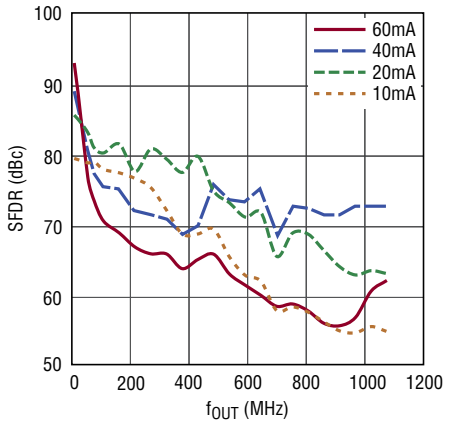
SFDR vs f_{OUT} and Temperature, f_{DAC} = 2.7Gsps



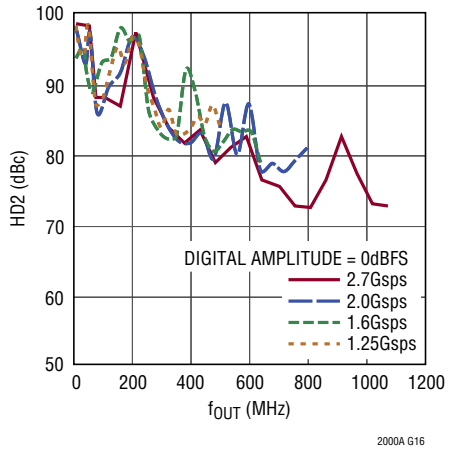
SFDR vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.7Gsps



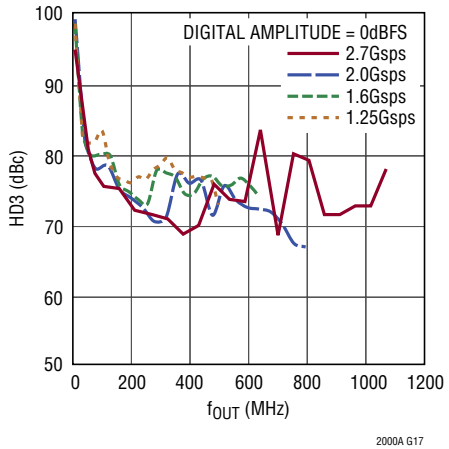
SFDR vs f_{OUT} and I_{OUTFS}, f_{DAC} = 2.7Gsps



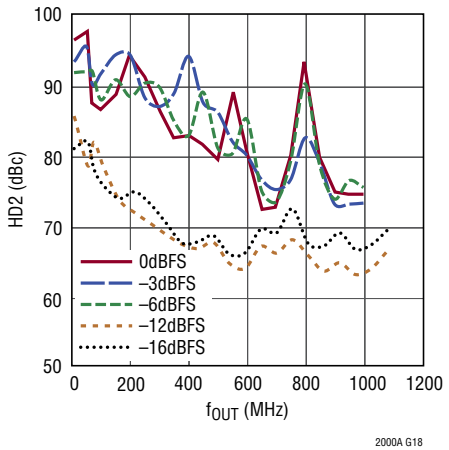
HD2 vs f_{OUT} and f_{DAC}



HD3 vs f_{OUT} and f_{DAC}



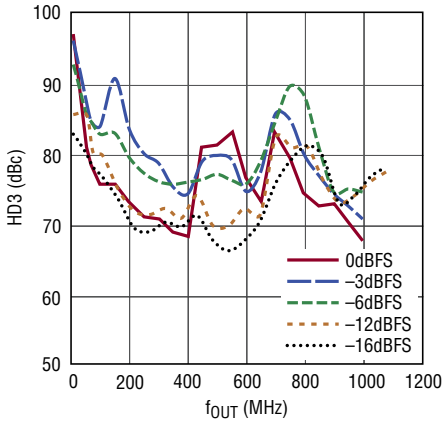
HD2 vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.7Gsps



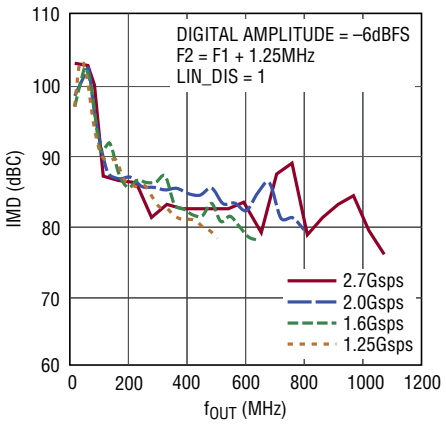
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

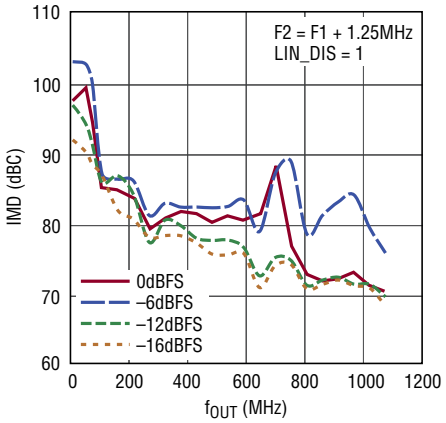
HD3 vs f_{OUT} and Digital Amplitude (dBFS), f_{DAC} = 2.7Gsps



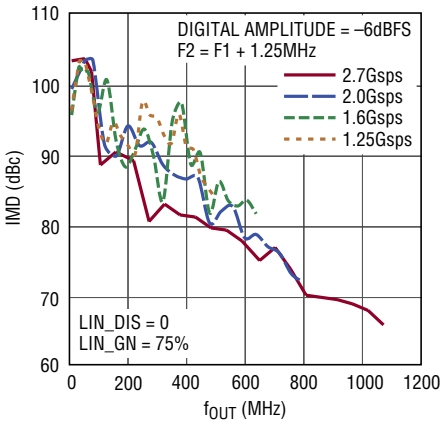
2-Tone IMD vs f_{OUT} and f_{DAC}



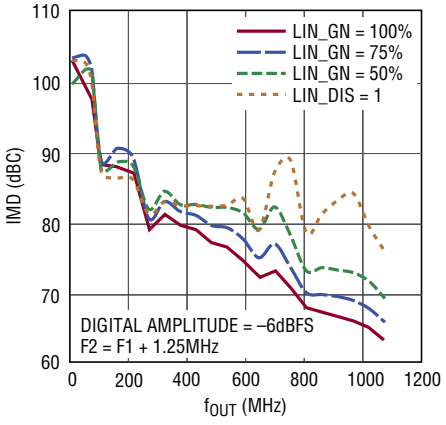
2-Tone IMD vs f_{OUT} and Digital Amplitude, f_{DAC} = 2.7Gsps



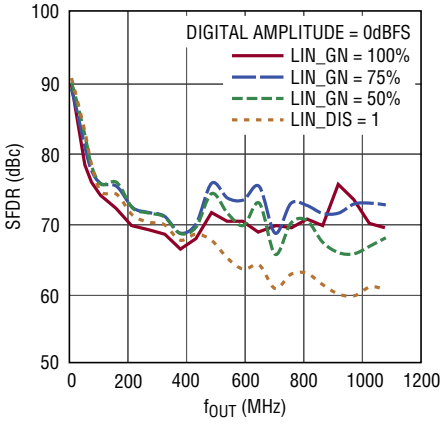
2-Tone IMD vs f_{OUT} and f_{DAC} with Default Linearization



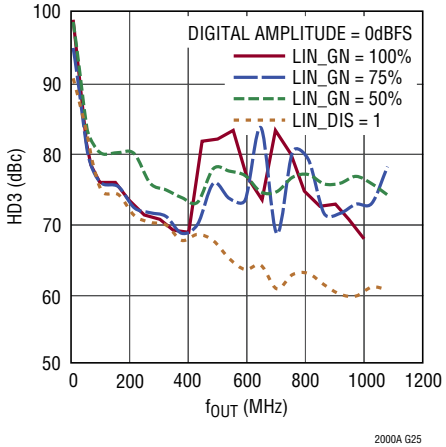
2-Tone IMD vs f_{OUT} and Linearization Setting, f_{DAC} = 2.7Gsps



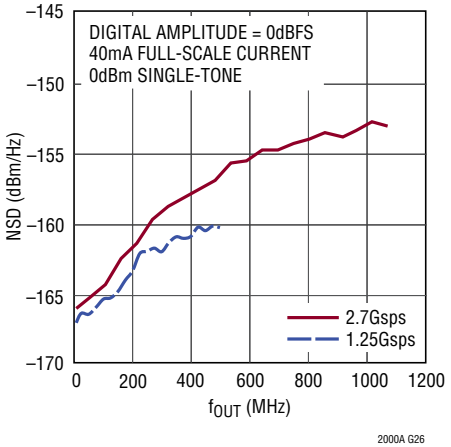
SFDR vs f_{OUT} and Linearization Setting, f_{DAC} = 2.7Gsps



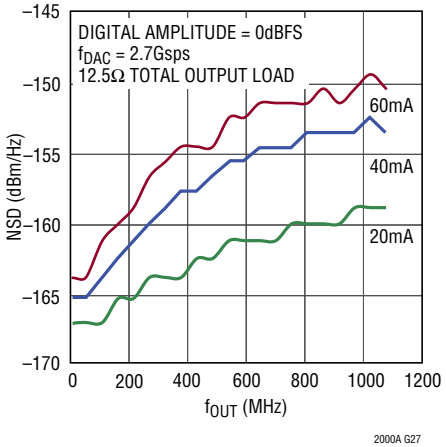
HD3 vs f_{OUT} and Linearization Setting, f_{DAC} = 2.7Gsps



LTC2000A-16 Single-Tone NSD vs f_{OUT} and f_{DAC}



LTC2000A-16 Single-Tone NSD vs f_{OUT} and I_{OUTFS}



TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

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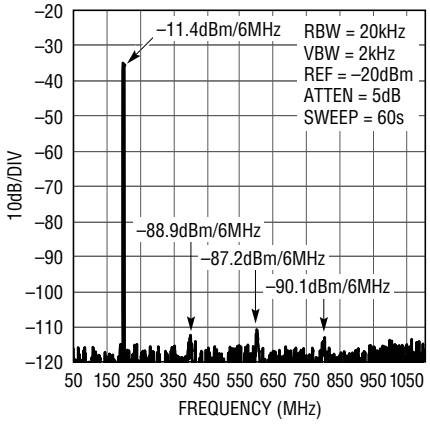
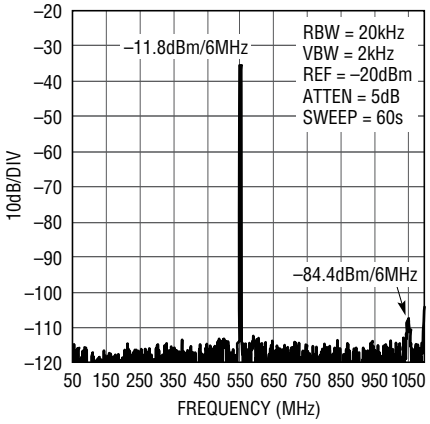
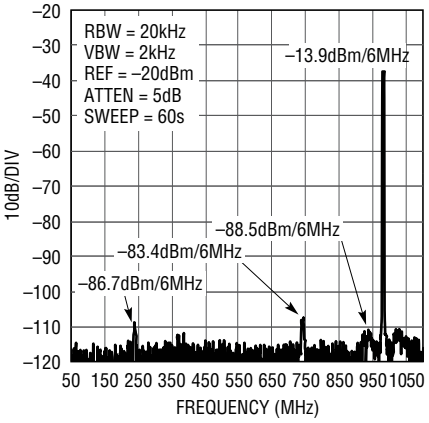
Single Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.7Gsps



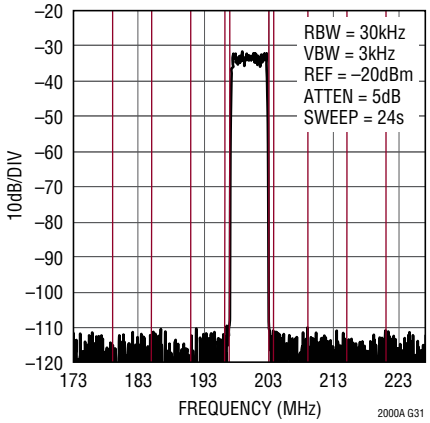
Single Carrier DOCSIS Mid Band Wideband ACLR, f_{DAC} = 2.7Gsps



Single Carrier DOCSIS High Band Wideband ACLR, f_{DAC} = 2.7Gsps



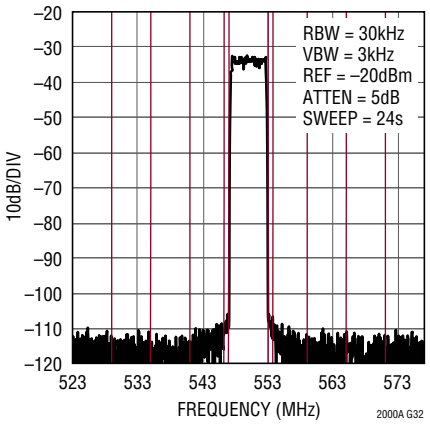
Single Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –11.40dBm, CENTER FREQ = 200MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–99.97dBm	–95.33dBm
6.375MHz	5.25MHz	–95.69dBm	–95.18dBm
12.00MHz	6MHz	–96.89dBm	–95.80dBm
18.00MHz	6MHz	–96.68dBm	–96.60dBm
24.00MHz	6MHz	–96.19dBm	–95.94dBm

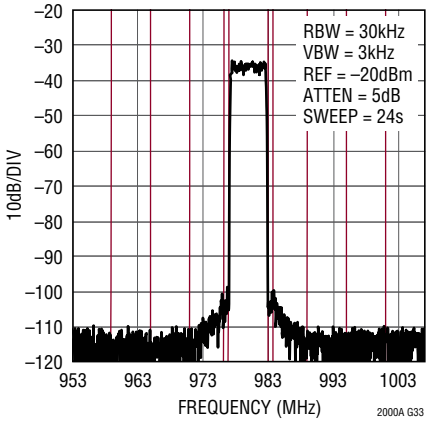
Single Carrier DOCSIS Mid Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –11.85dBm, CENTER FREQ = 550MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–95.92dBm	–92.58dBm
6.375MHz	5.25MHz	–91.68dBm	–91.81dBm
12.00MHz	6MHz	–94.58dBm	–94.33dBm
18.00MHz	6MHz	–94.54dBm	–94.36dBm
24.00MHz	6MHz	–94.17dBm	–94.16dBm

Single Carrier DOCSIS High Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –13.95dBm, CENTER FREQ = 980MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–89.76dBm	–90.00dBm
6.375MHz	5.25MHz	–87.24dBm	–86.24dBm
12.00MHz	6MHz	–92.87dBm	–92.16dBm
18.00MHz	6MHz	–93.36dBm	–92.29dBm
24.00MHz	6MHz	–92.65dBm	–91.52dBm

TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

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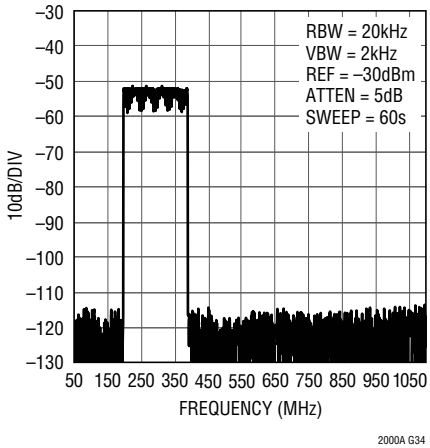
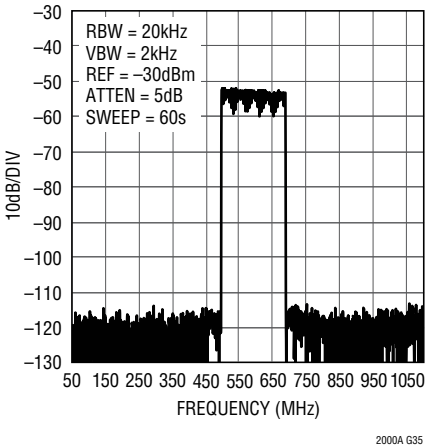
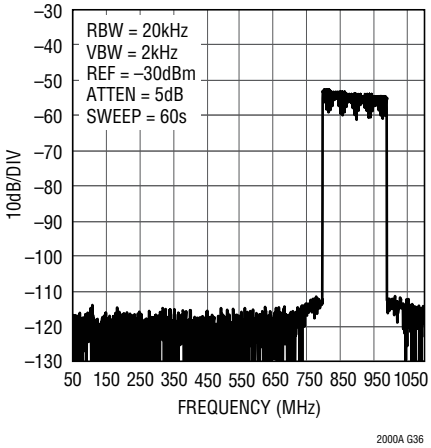
32-Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.7Gsps



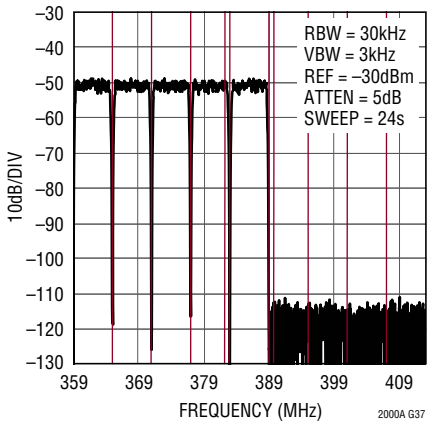
32-Carrier DOCSIS Mid Band Wideband ACLR, f_{DAC} = 2.7Gsps



32 Carrier DOCSIS High Band Wideband ACLR, f_{DAC} = 2.7Gsps



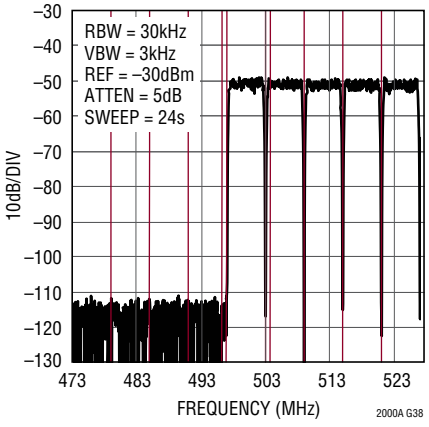
32-Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –28.77dBm, CENTER FREQ = 386MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–39.64dBm	–103.72dBm
6.375MHz	5.25MHz	–29.39dBm	–94.79dBm
12.00MHz	6MHz	–28.89dBm	–94.96dBm
18.00MHz	6MHz	–28.83dBm	–95.34dBm
24.00MHz	6MHz	–28.74dBm	–95.75dBm

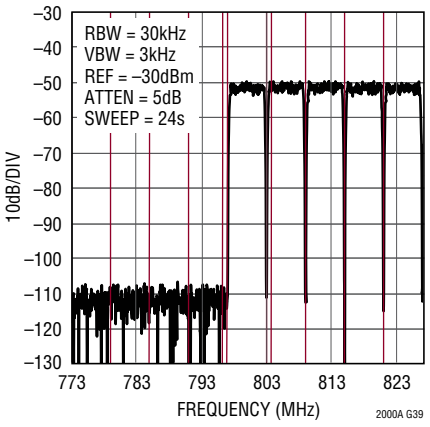
32 Carrier DOCSIS Mid Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –28.59dBm, CENTER FREQ = 500MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–102.11dBm	–39.71dBm
6.375MHz	5.25MHz	–94.82dBm	–28.18dBm
12.00MHz	6MHz	–94.42dBm	–28.96dBm
18.00MHz	6MHz	–94.16dBm	–29.11dBm
24.00MHz	6MHz	–94.17dBm	–29.04dBm

32 Carrier DOCSIS High Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –29.43dBm, CENTER FREQ = 800MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–97.92dBm	–40.25dBm
6.375MHz	5.25MHz	–89.60dBm	–29.56dBm
12.00MHz	6MHz	–89.45dBm	–29.23dBm
18.00MHz	6MHz	–89.52dBm	–29.40dBm
24.00MHz	6MHz	–89.38dBm	–29.56dBm

TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

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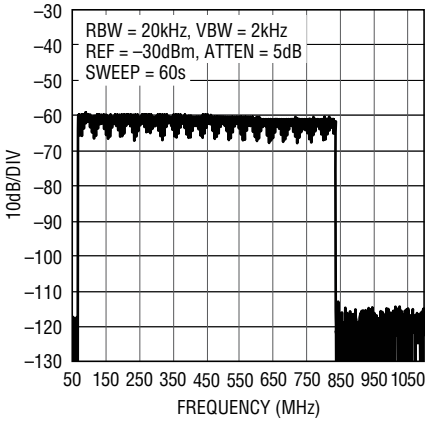
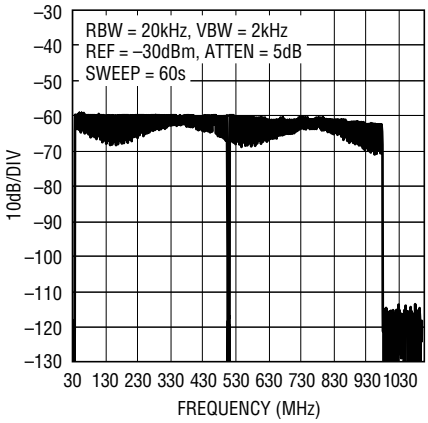
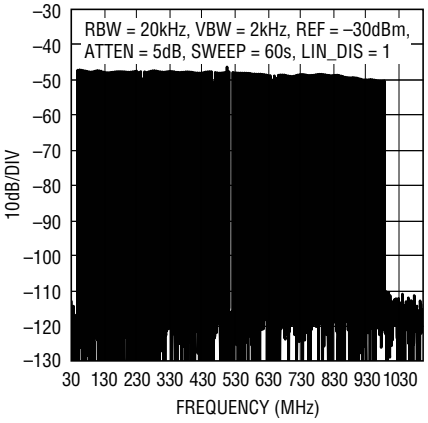
128 Carrier DOCSIS Low Band Wideband ACLR, f_{DAC} = 2.7Gsps



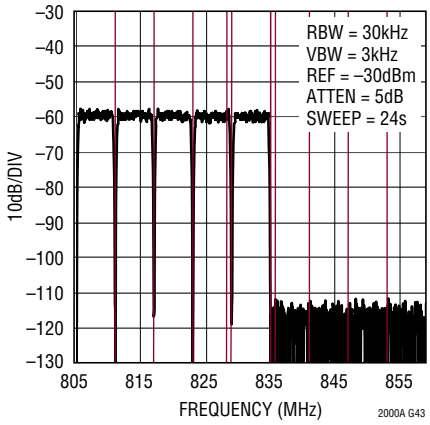
157 Carrier DOCSIS Gap Channel Wideband ACLR, f_{DAC} = 2.7Gsps



157 Carrier Tones with Gap Channel Wideband ACLR, f_{DAC} = 2.7Gsps



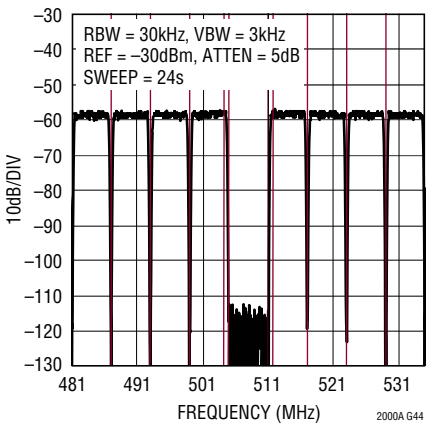
128 Carrier DOCSIS Low Band Narrowband ACLR, f_{DAC} = 2.7Gsps



CARRIER POWER = –37.77dBm, CENTER FREQ = 832MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–47.75dBm	–104.61dBm
6.375MHz	5.25MHz	–38.07dBm	–95.82dBm
12.00MHz	6MHz	–37.57dBm	–95.53dBm
18.00MHz	6MHz	–37.39dBm	–95.43dBm
24.00MHz	6MHz	–37.27dBm	–95.18dBm

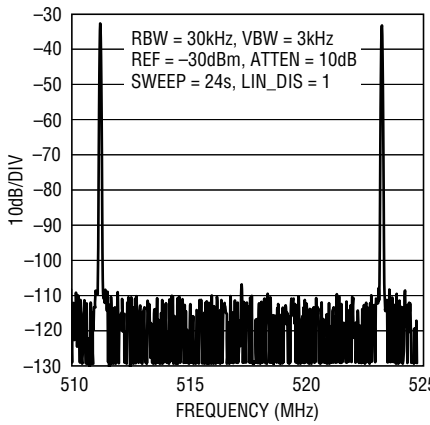
157 Carrier DOCSIS Gap Channel Narrowband ACLR, f_{DAC} = 2.7Gsps



GAP CHANNEL POWER = –96.61dBm, CENTER FREQ = 508MHz

OFFSET FREQ	BW	LOWER	UPPER
3.375MHz	750kHz	–47.17dBm	–48.00dBm
6.375MHz	5.25MHz	–36.79dBm	–36.67dBm
12.00MHz	6MHz	–36.58dBm	–36.56dBm
18.00MHz	6MHz	–36.76dBm	–36.60dBm
24.00MHz	6MHz	–36.76dBm	–36.69dBm

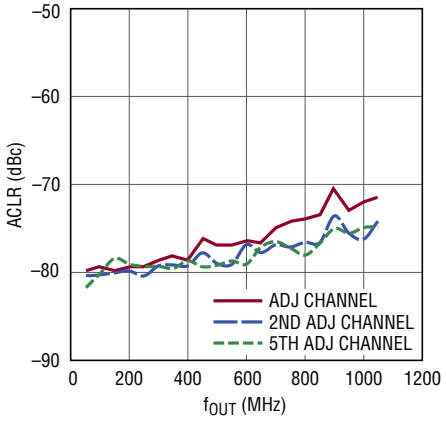
157 Carrier Tones with Gap Channel Narrowband ACLR, f_{DAC} = 2.7Gsps



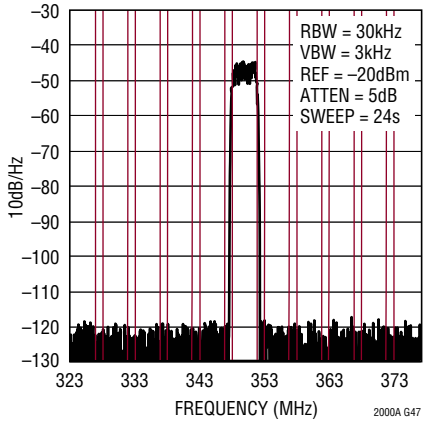
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

LTC2000A-16 Single Carrier WCDMA ACLR vs f_{OUT}, f_{DAC} = 2.7Gsps



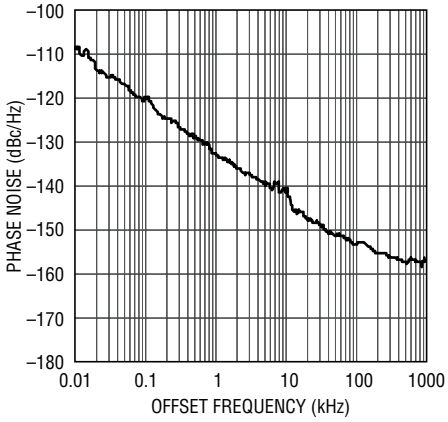
LTC2000A-16 Single Carrier WCDMA ACLR at 350MHz, f_{DAC} = 2.7Gsps



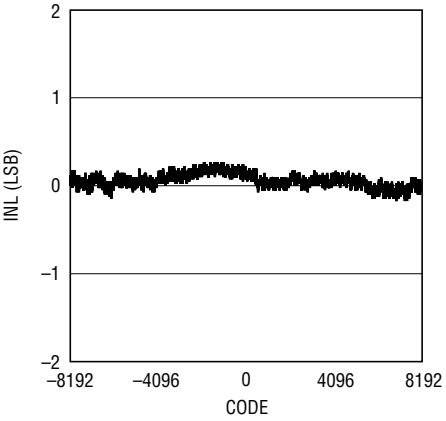
CARRIER POWER = –16.44dBm, CENTER FREQ = 350MHz

OFFSET FREQ	BW	LOWER	UPPER
5.00MHz	3.84MHz	–95.14dBm	–94.76dBm
10.00MHz	3.84MHz	–95.76dBm	–96.22dBm
15.00MHz	3.84MHz	–95.41dBm	–95.10dBm
20.00MHz	3.84MHz	–95.69dBm	–96.41dBm
25.00MHz	3.84MHz	–95.00dBm	–96.69dBm

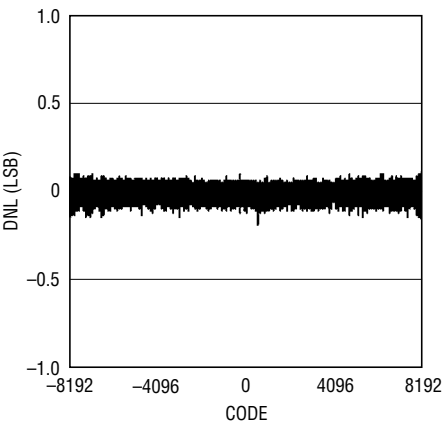
Additive Phase Noise, f_{OUT} = 65MHz, f_{DAC} = 2.7Gsps



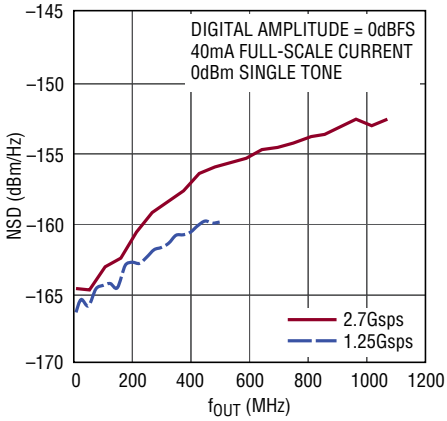
LTC2000A-14 Integral Nonlinearity (INL)



LTC2000A-14 Differential Nonlinearity (DNL)



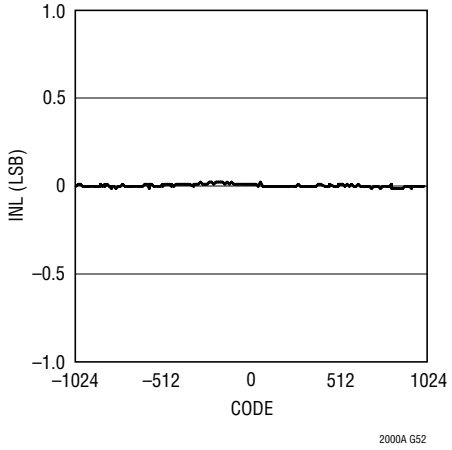
LTC2000A-14 Single-Tone NSD vs f_{OUT} and f_{DAC}



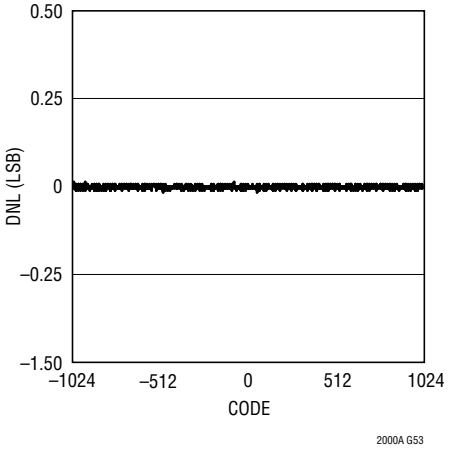
TYPICAL PERFORMANCE CHARACTERISTICS

I_{OUTFS} = 40mA, T_A = 25°C, AV_{DD18} = DV_{DD18} = 1.86V, AV_{DD33} = DV_{DD33} = 3.3V, R_{LOAD} = 12.5Ω, LIN_DIS = 0, LIN_ GN = 75% unless otherwise noted.

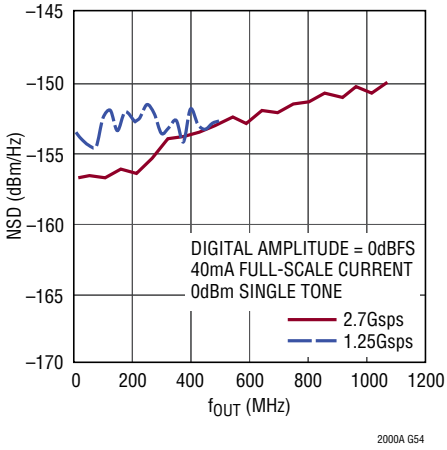
LTC2000A-11 Integral Nonlinearity (INL)



LTC2000A-11 Differential Nonlinearity (DNL)



LTC2000A-11 Single-Tone NSD vs f_{OUT} and f_{DAC}



PIN FUNCTIONS

AV_{DD18}: 1.8V Analog Supply Voltage Input. 1.8V to 1.92V.

AV_{DD33}: 3.3V Analog Supply Voltage Input. 3.135V to 3.465V.

CKP, CKN: DAC Sample Clock Inputs. Maximum clock frequency (f_{DAC}) is 2700MHz. Clock signal should be AC coupled.

$\overline{CS}$: Serial Interface Chip Select Input. When $\overline{CS}$ is low, SCK is enabled for shifting data on SDI into the register. When $\overline{CS}$ is taken high, SCK is disabled and SDO is high impedance.

DAP[15:0], DAN[15:0]: Port A LVDS Data Inputs. Maximum data rate is 1.35Gbps. Port A is used only in dual-port mode. Connect to GND if not used. The data input format is two's complement.

DBP[15:0], DBN[15:0]: Port B LVDS Data Inputs. Maximum data rate is 1.35Gbps. In single-port mode, only Port B is used. In dual-port mode, the sample from Port B appears at $I_{OUTP/N}$ one cycle after the sample from Port A. The data input format is two's complement.

DCKIP, DCKIN: LVDS Data Clock Inputs. Maximum frequency (f_{DCKI}) is 675MHz. In dual-port mode, f_{DCKI} = f_{DAC}/4. In single-port mode, f_{DCKI} = f_{DAC}/2

DCKOP, DCKON: LVDS Data Clock Outputs. Maximum frequency is 675MHz. Select frequency (f_{DAC}/4 or f_{DAC}/2), output current (3.5mA or 7mA), and termination (none or 100Ω) using register 0x02.

DV_{DD18}: 1.8V Digital Supply Voltage Input. 1.8V to 1.92V.

DV_{DD33}: 3.3V Digital Supply Voltage Input. 3.135V to 3.465V.

FSADJ: Full-Scale Adjust Pin. The DAC full-scale current is 16 • (V_{REFIO}/R_{FSADJ}). Connect a 500Ω resistor from FSADJ to GND to set the full-scale current to 40mA.

GND: Ground.

I_{OUTP}, I_{OUTN}: DAC Analog Current Outputs. Differential output is nominally ±40mA. Maximum update rate is 2.7Gsps. The output current is evenly divided between I_{OUTP} and I_{OUTN} when the two's compliment DAC code is set to mid-scale (all zeros).

$\overline{PD}$ (Pin S1): Active Low Power-Down Input. When $\overline{PD}$ is low, the LTC2000A supply current is less than 440µA. To exit power-down mode switch $\overline{PD}$ high to SV_{DD}.

PIN FUNCTIONS

REFIO: Reference Voltage Input or Output. The 1.25V internal reference is available at the pin through a 10k internal resistor. May be overdriven with an external reference voltage between 1.1V and 1.4V.

SCK: Serial Interface Clock Input. Maximum frequency is 50MHz.

SDI: Serial Interface Data Input. Data on SDI is clocked in on the rising edge of SCK.

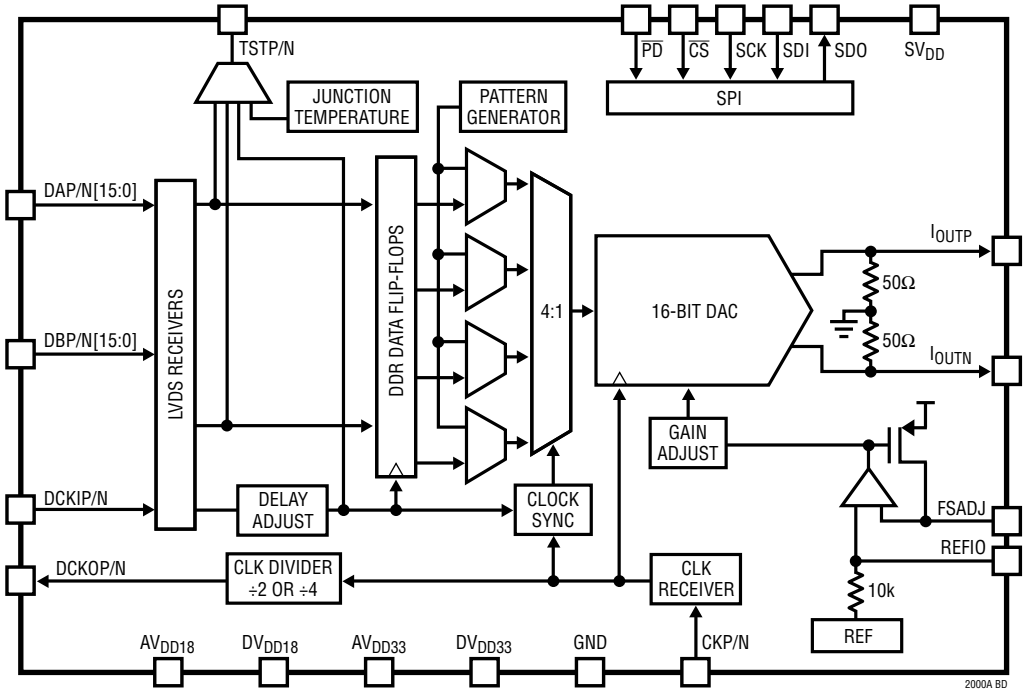
SDO: Serial Interface Data Output. Data is clocked out onto SDO by the falling edge of SCK. SDO is high impedance when $\overline{CS}$ is high.

SV_{DD}: SPI Supply Voltage Input. 1.71V to 3.465V.

TSTP, TSTN: Test Output Pins. May be optionally used to measure internal temperature or timing of LVDS inputs. See Measuring Internal Junction Temperature and Measuring LVDS Input Timing Skew sections in Applications Information. Use SPI internal registers 0x18 and 0x19 to control TSTP/N. Connect to GND if not used.

Note: For pin locations, refer to the Pin Locations section of this data sheet.

BLOCK DIAGRAM



TIMING DIAGRAMS

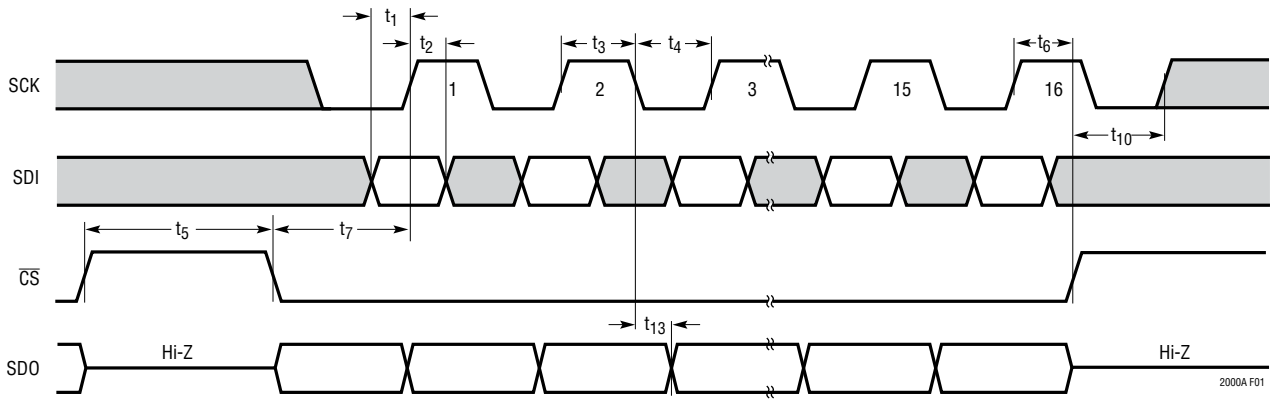


Figure 1. Serial Interface Timing

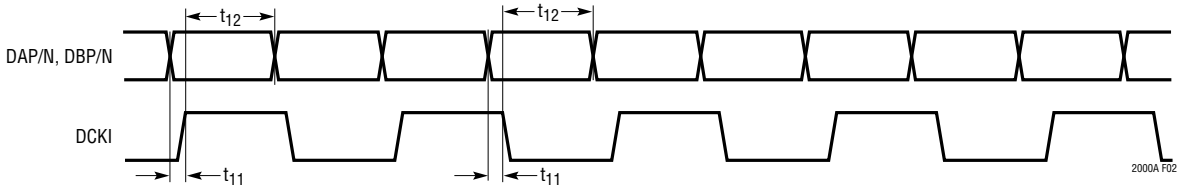


Figure 2. LVDS Interface Timing (DCKI_Q = 0, DCK_TADJ = 000)

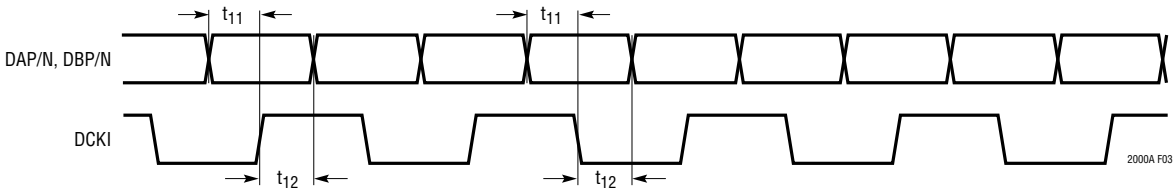


Figure 3. LVDS Interface Timing (DCKI_Q = 1)

OPERATION

Introduction

The LTC2000A is a family of 2.7Gsps current steering DACs. Three resolutions (16-, 14-, 11-bit) are available in a 170-lead BGA package. The LTC2000A features high output bandwidth and output current, while maintaining a clean output spectrum with low spurs, making it ideal for generating high frequency or broadband signals. The LTC2000A output current is nominally 40mA and is a scaled (16x) replica of the current flowing out of the FSADJ pin (nominally 2.5mA). The high output current allows flexibility in the output impedance, and the high FSADJ current and low scaling factor give excellent close-in phase noise performance.

The LTC2000A has two 16-, 14-, 11-bit wide LVDS or DHSTL-compatible parallel data input ports (DAP/N, DBP/N). Each data input port is capable of receiving two's complement data at up to 1.35Gbps using a double data rate (DDR) data input clock (DCKIP/N) at up to 675MHz. The DDR data input clock may be either in quadrature or in phase with the data arriving on the data input ports.

OPERATION

After incoming data is sampled by DCKIP/N, an internal multiplexer interleaves the data for resampling by the DAC sample clock (CKP/N). See Figures 4a and 4b. After a pipeline delay (latency) of up to 11 DAC sample clock cycles, the rising edges of CKP/N update the DAC code and a proportional differential output current is steered between the two outputs ($I_{OUTP/N}$). Note it takes about 3ns (aperture delay) from the CKP/N rising edge that updates a DAC code to the actual $I_{OUTP/N}$ transition for that DAC code.

An internal clock synchronizer monitors the incoming phase of DCKIP/N and chooses the appropriate phase for the multiplexer control signals to ensure that the data is sampled correctly by CKP/N. The LTC2000A also generates an LVDS clock output (DCKOP/N) by dividing the sample clock frequency to simplify clocking of the host FPGA or ASIC. Additional features such as pattern generation, LVDS loopout, and junction temperature sensing simplify system development and testing.

The serial peripheral interface (SPI) port allows configuration and read back of the internal registers which control the above functions.

Dual-Port Mode

In dual-port mode, data is written to both ports A and B simultaneously and then subsequently interleaved inside the LTC2000A, allowing DAC output sampling rates of up to 2.7Gsps. Figures 4a and 4b show a simplified block diagram and sample waveforms for dual-port operation.

The LVDS data input ports A and B are sampled on both the falling and rising edges of the DDR data input clock (DCKIP/N) by four groups of flip-flops. The contents of these flip-flops are then interleaved by the 4:1 MUX and sampled by the DAC sample clock (CKP/N) at frequencies up to 2.7GHz, with data from port A (DAP/N) preceding data from port B (DBP/N) at the DAC output.

Note that the sample clock (CKP/N) frequency is always four times the DDR data input clock (DCKIP/N) frequency in dual-port mode. For example, to use the DAC at 2.7Gsps, apply a 2.7GHz clock to CKP/N and a 675MHz clock to DCKIP/N and send data into both ports A and B (DAP/N, DBP/N) at 1.35Gsps per port.

Latency is defined as the delay from the DCKIP/N transition that samples a DAC code to the CKP/N rising transition which causes that sample to appear at the DAC output $I_{OUTP/N}$. In dual-port mode the latency from DAP/N to $I_{OUTP/N}$ is 10 sample clock cycles and the latency from DBP/N to $I_{OUTP/N}$ is 11 cycles, starting from the CKP/N rising edge that immediately follows the DCKIP/N transition that sampled the DAC code (Figure 4b).

Single-Port Mode

In single-port mode, data is written to port B (DBP/N) only, allowing DAC output sampling rates of up to 1.35Gsps. Figures 4c and 4d show a block diagram and sample waveforms representing single-port operation. Samples are written to port B (DBP/N) and sampled on both the falling and rising edges of the DDR data input clock (DCKIP/N) by two groups of flip-flops. The contents of these flip-flops are then interleaved into a single data stream by the 2:1 MUX and sampled by the DAC sample clock (CKP/N) at frequencies up to 1.35GHz.

Note that in single-port mode the sample clock (CKP/N) frequency is always twice the DDR data input clock (DCKIP/N) frequency. For example, to use the DAC at 1.35Gsps, apply a 1.35GHz clock to CKP/N and a 675MHz clock to DCKIP/N and send data into port B (DBP/N) at 1.35Gsps. In single-port mode, port A (DAP/N) should be grounded. Due to the design of the internal clock synchronizer in single port mode, there is a half cycle shift in the single port latency. The latency from DBP/N to $I_{OUTP/N}$ in single-port mode is 7.5 sample clock cycles, starting from the CKP/N falling edge that immediately follows the DCKIP/N transition that sampled the DAC code (Figure 4d).

OPERATION

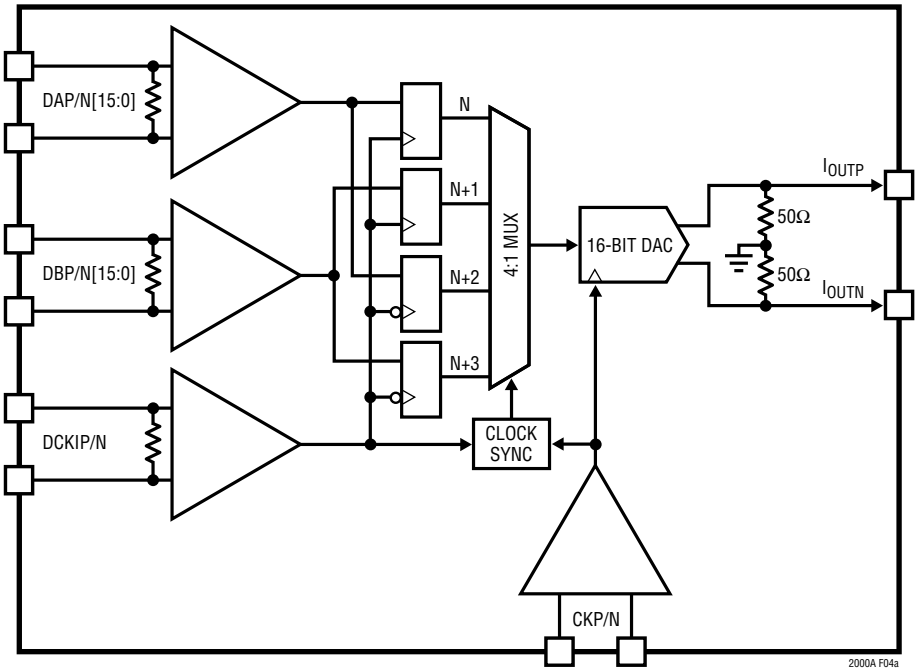


Figure 4a. Simplified Block Diagram – Dual-Port Operation

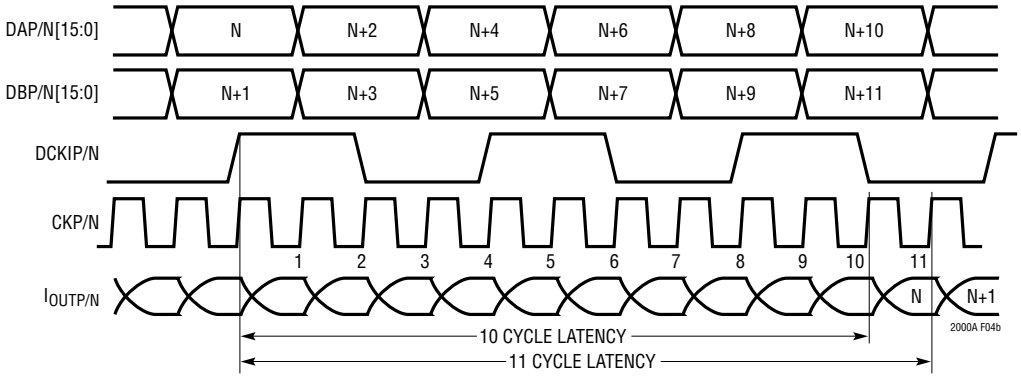


Figure 4b. Sample Waveforms – Dual-Port Operation

OPERATION

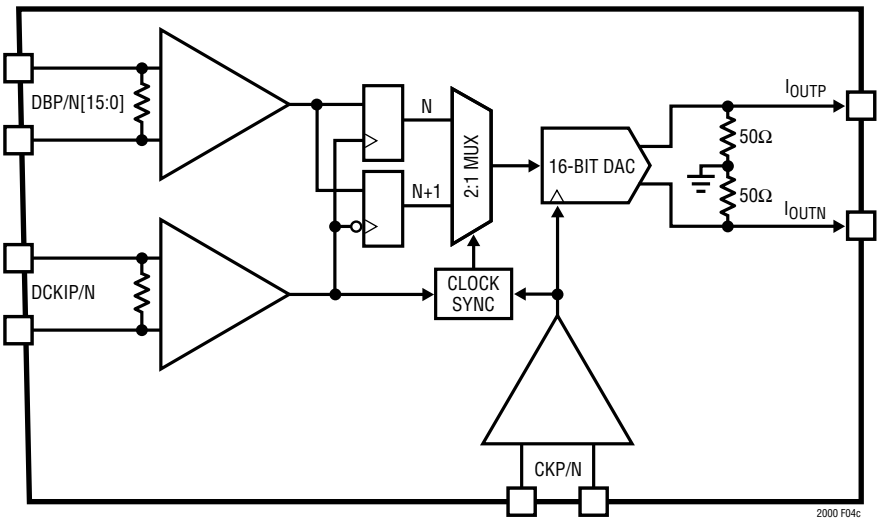


Figure 4c. Simplified Block Diagram – Single-Port Operation

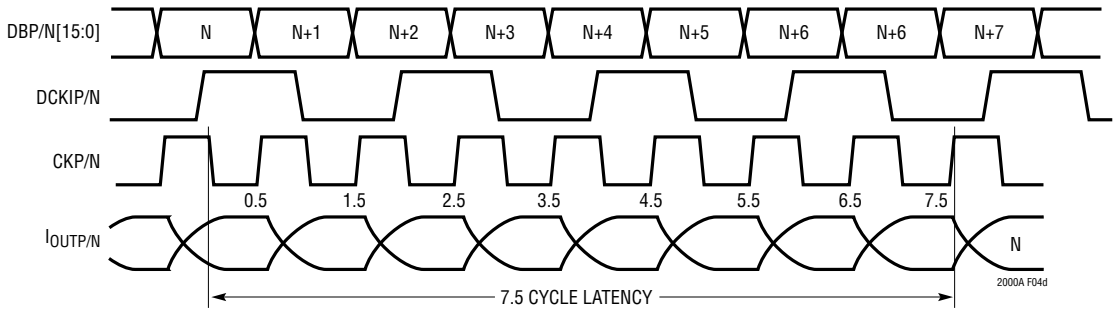


Figure 4d. Sample Waveforms – Single-Port Operation

OPERATION

Serial Peripheral Interface (SPI)

The LTC2000A uses an SPI/MICROWIRE-compatible 3-wire serial interface to configure and read back internal registers. The SV_{DD} pin is the power supply for the SPI interface (nominally 1.8V or 3.3V). The $\overline{CS}$ input is level triggered. When this input is taken low, it acts as a chip-select signal, enabling the SDI and SCK buffers and the SPI input register. After the falling edge of $\overline{CS}$, the first data byte clocked into SDI by the rising edges of SCK is the command byte. The first bit of the command byte signifies a read (R/W = 1) or write (R/W = 0) operation. The next seven bits contain the register address, which completes the command byte.

The next byte transferred after the command byte is the data byte. For write operations, the data byte is written to the SPI register specified by the register address set in the command byte. During read operations, the data byte is ignored, and the contents of the selected SPI register are clocked out onto the SDO pin by the falling edges of SCK. During write operations, SDO will be low. When $\overline{CS}$ goes high, SDO is high impedance. Figure 5 shows the SPI command and data input.

Users wishing to transfer multiple bytes of data at once may do so, with the address for each subsequent byte automatically incremented internally. The address will continue to increment until $\overline{CS}$ goes high or until address bits A[4:0] reach 0x1F, after which subsequent bytes will continue to be written to the same address.

Reserved address and bit locations should not be written with any value other than zero. Table 11 contains a full description of all internal SPI registers and can be found in the SPI Register Summary section.

Power-On Reset

The internal power-on reset circuit will reset the LTC2000A upon power up and clear the output to mid-scale when power is first applied, making system initialization consistent and repeatable. All internal registers are reset to 0x00, with the exception of register address 0x08, which resets to 0x08. A software reset can also be applied by using the SPI interface to load 0x01 into register address 0x01, setting SW_RST to 1 (see Table 1). Note that the SW_RST bit is automatically cleared when $\overline{CS}$ returns high. It is recommended that users perform a software reset once all power supplies are stable.

Power Down

Users wishing to save power when the DAC is not being used may reduce the supply current to less than 440µA by pulling the $\overline{PD}$ pin to GND or by writing to register 0x01 to set FULL_PD = 1. Alternatively, users may power down unused portions of the chip individually using DAC_PD, CK_PD, DCKO_DIS, DCKI_EN, DA_EN, and DB_EN in registers 0x01, 0x02, 0x03, and 0x04 (see Table 1).

Reference Operation

The LTC2000A has a 1.25V internal bandgap voltage reference that drives the REFIO pin through a 10k internal resistor, and should be buffered if driving any additional external load. For noise performance, a 0.1µF capacitor to GND is recommended on the REFIO pin, but is not required for stability.

In the case where an external reference would be preferred, the external reference is simply applied to the REFIO pin and overdrives the internal reference. The acceptable external reference range is 1.1V to 1.4V.

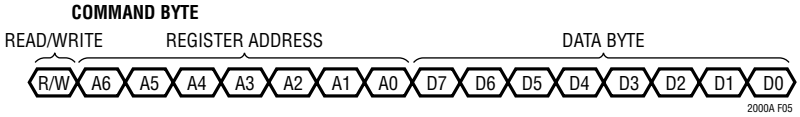


Figure 5. SPI Command and Data Input

OPERATION

Table 1. Power-On Reset and Power-Down SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x01	0	SW_RST	Software Reset. Set SW_RST = 1 to restore all registers to their power-on reset state. SW_RST is automatically cleared when $\overline{CS}$ returns high. All registers reset to 0x00, except address 0x08 which resets to 0x08.
	1	DAC_PD	DAC Power Down. Set DAC_PD = 1 to power down the DAC and FSADJ bias circuits.
	2	FULL_PD	Full Power Down. Set FULL_PD = 1 to power down all active circuits on the chip and reduce the supply current to less than 100µA.
0x02	0	CK_PD	CKP/N Clock Receiver Power Down. CKP/N clock receiver is powered down when CK_PD = 1.
	4	DCKO_DIS	DCKOP/N Output Disable. Set DCKO_DIS = 1 to power down the DCKO LVDS transmitter. For DCKO_DIS = 1, DCKOP/N are high impedance.
0x03	0	DCKI_EN	DCKIP/N Clock Receiver Enable. Set DCKI_EN = 1 to enable the DCKI clock receiver.
0x04	0	DA_EN	DAC Data Port A LVDS Receiver Enable. Set DA_EN = 1 to enable port A (DAP/N) LVDS receivers. For DA_EN = 0, port A LVDS receivers are powered down and port A data will be zeroes.
	1	DB_EN	DAC Data Port B LVDS Receiver Enable. Set DB_EN = 1 to enable port B (DBP/N) LVDS receivers. For DB_EN = 0, port B LVDS receivers are powered down and port B data will be zeroes.

Note: Registers 0x01 to 0x04 reset to 0x00 (default).

Setting the Full-Scale Current

The full-scale DAC output current (I_{OUTFS}) is nominally 40mA, but can be adjusted as low as 10mA or as high as 60mA. The full-scale current is set by placing an external resistor (R_{FSADJ}) between the FSADJ pin and GND. An internal reference control loop amplifier sets the current flowing through R_{FSADJ} such that the voltage at FSADJ is equal to the voltage at REFIO, which is typically 1.25V. I_{OUTFS} is set as a scaled replica of the current flowing out of the FSADJ pin (I_{FSADJ}):

$$I_{FSADJ} = \frac{V_{REFIO}}{R_{FSADJ}}$$

$$I_{OUTFS} = 16 \bullet I_{FSADJ} \bullet \frac{256}{256 + GAIN\_ADJ}$$

where GAIN_ADJ is a 6-bit two's complement number from –32 to 31 (nominally 0) which can be programmed using SPI register 0x09 as shown in Table 2. For example, for R_{FSADJ} = 500Ω, V_{REFIO} = 1.25V, and GAIN_ADJ = 0x00, the control loop will force 1.25V at the FSADJ pin, causing 2.5mA to flow through R_{FSADJ}. I_{OUTFS} will then be set to 16 • 2.5mA = 40mA.

Changing GAIN_ADJ to 0x1F (+31) will decrease the current by 10.8% to 35.7mA. Changing GAIN_ADJ to 0x20 (–32) will increase the current by 14.3% to 45.7mA.

Note that GAIN_ADJ appears in the denominator of the equation for I_{OUTFS}, so the adjustment resolution varies from 0.5% to 0.3% per step. The circuit shown in Figure 6 may be used to vary the full-scale output current beyond the range of the GAIN_ADJ register.

DAC linearity and harmonic distortion may be degraded when using full-scale currents other than 40mA. The full-scale current must not exceed 60mA, and is recommended to be at least 10mA.

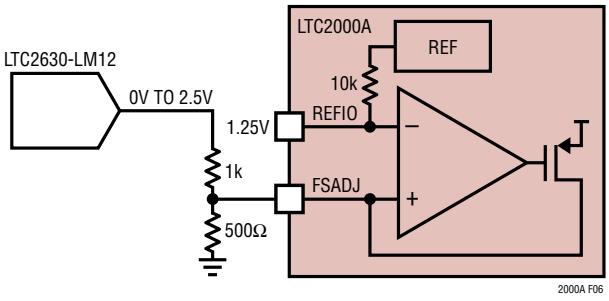


Figure 6. LTC2000A Full-Scale Adjust from 20mA to 60mA

OPERATION

Table 2. Full-Scale Gain Adjustment

ADDRESS	BIT	NAME	DESCRIPTION			
			GAIN_ADJ (HEX)	GAIN_ADJ (DECIMAL)	GAIN ADJUSTMENT	FULL-SCALE CURRENT (R_{FSADJ} = 500Ω, V_{REFIO} = 1.25V)
0x09	[5:0]	GAIN_ADJ	0x1F	+31	89.2%	35.68mA
			0x1E	+30	89.5%	35.80mA
			—	—	—	—
			0x01	+1	99.6%	39.84mA
			0x00	0	100.0%	40.00mA
			0x3F	–1	100.4%	40.16mA
			—	—	—	—
			0x21	–31	113.8%	45.51mA
			0x20	–32	114.3%	45.71mA

Note: Register 0x09 resets to 0x00 (default).

DAC Transfer Function

The LTC2000A contains an array of current sources that are steered through differential switches to either I_{OUTP} or I_{OUTN}, depending on the DAC code programmed through the LVDS parallel interface. The LTC2000A uses a 16-/14-/11-bit two's complement DAC code. The complementary current outputs, I_{OUTP} and I_{OUTN}, source current from 0mA to I_{OUTFS}. For I_{OUTFS} = 40mA (nominal), I_{OUTP} swings from 0mA (for zero-scale DAC code) to 40mA (for full-scale DAC code). I_{OUTN} is complementary to I_{OUTP}. When the DAC code is set to mid-scale (all zeros), I_{OUTFS} is evenly divided between I_{OUTP} and I_{OUTN}. I_{OUTP} and I_{OUTN} are given by the following formulas:

LTC2000A-16:

$$I_{OUTP} = I_{OUTFS} \bullet (CODE + 32768)/65536 + I_{OUTCM}$$
$$I_{OUTN} = I_{OUTFS} \bullet (32768 - CODE - 1)/65536 + I_{OUTCM}$$

LTC2000A-14:

$$I_{OUTP} = I_{OUTFS} \bullet (CODE + 8192)/16384 + I_{OUTCM}$$
$$I_{OUTN} = I_{OUTFS} \bullet (8192 - CODE - 1/4)/16384 + I_{OUTCM}$$

LTC2000A-11:

$$I_{OUTP} = I_{OUTFS} \bullet (CODE + 1024)/2048 + I_{OUTCM}$$
$$I_{OUTN} = I_{OUTFS} \bullet (1024 - CODE - 1/32)/2048 + I_{OUTCM}$$

The DAC code ranges from -2^{N-1} to $2^{N-1} - 1$, with N being the DAC resolution (16/14/11). I_{OUTCM} is a small, constant common-mode output current that is equal to approximately 0.2% full-scale, or 80µA for I_{OUTFS} = 40mA.

The LTC2000A differential output currents typically drive a resistive load either directly or drive an equivalent resistive load through a transformer (see the Output Configurations section). The voltage outputs generated by the I_{OUTP} and I_{OUTN} outputs currents are then:

$$V_{OUTP} = I_{OUTP} \bullet R_{LOAD}$$
$$V_{OUTN} = I_{OUTN} \bullet R_{LOAD}$$
$$V_{DIFF} = V_{OUTP} - V_{OUTN} = (I_{OUTP} - I_{OUTN}) \bullet R_{LOAD}$$

Substituting the values above gives:

LTC2000A-16:

$$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1)/4096$$

LTC2000A-14:

$$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1/4)/1024$$

LTC2000A-11:

$$V_{DIFF} = V_{REFIO} \bullet (R_{LOAD}/R_{FSADJ}) \bullet (2 \bullet CODE + 1/32)/128$$

Note that the gain of the DAC depends on the ratio of R_{LOAD} to R_{FSADJ}, and the gain error tempco is affected by the temperature tracking of R_{LOAD} with R_{FSADJ}.

Analog Outputs ($I_{OUTP/N}$)

The two complementary analog outputs ($I_{OUTP/N}$) have low output capacitance that, with appropriate R_{LOAD} values, can achieve high output bandwidths of 2.1GHz. The analog outputs also have an internal impedance of 50Ω to GND that will affect the calculation of R_{LOAD} and the output

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voltage swing of the DAC. For example, loading both I_{OUTP} and I_{OUTN} with external 50Ω resistors to GND will cause R_{LOAD} to equal 25Ω. Assuming an I_{OUTFS} of 40mA, V_{DIFF} will swing between 1V and –1V.

The specified output compliance voltage range is ±1V. Above 1V, the differential current steering switches will start to approach the transition from saturation to linear region and degrade DAC linearity. Below –1V protection diodes will limit the swing of the DAC. Small voltage swings and low common-mode voltages typically result in the best distortion performance.

DAC Sample Clock (CKP/N)

The DAC sample clock (CKP/N) is used to update the LTC2000A outputs at rates of up to 2.7Gsps. Provide a clean, low jitter differential clock at up to 2.7GHz on pins CKP/N (see Generating the DAC Sample Clock section). The DC bias point of CKP/N is set internally through a 5kΩ impedance. A 0dBm DAC sample clock should be sufficient to obtain the performance shown in the Typical Performance Characteristics section. For best jitter and phase noise, AC couple a differential clock onto CKP/N with balanced duty cycle and the highest possible amplitude and slew rate.

Use SPI register 0x02 to control the DAC sample clock receiver (Table 3). The LTC2000A contains a clock detector which sets CK_OK = 1 if the DAC sample clock is present and f_{DAC} > 50MHz. When the sample clock is not present (CK_OK = 0), the DAC output is forced to mid-scale and the internal data path is held at reset. Set CK_PD = 1 to power down the clock receiver and save power when the DAC is not being used. Note that at power-on reset, the DAC sample clock receiver is on by default.

Divided Clock Output (DCKOP/N)

The LTC2000A contains a programmable clock divider and LVDS transmitter which provide a divided version (either $f_{DAC}/4$ or $f_{DAC}/2$) of the DAC sample clock for use by the host FPGA or ASIC. Use SPI register 0x02 to control DCKOP/N (Table 3). At power-on reset, the LVDS transmitter will provide a clock signal at $f_{DAC}/4$ with a 3.5mA differential output current.

If desired, set DCKO_DIV = 1 to change the divided clock output frequency to $f_{DAC}/2$. The output current can be increased to 7mA by setting DCKO_ISEL = 1, and an internal 100Ω differential termination can be enabled by setting DCKO_TRM = 1. Set DCKO_DIS = 1 to disable the LVDS transmitter and save power when not in use.

LVDS Data Clock Input (DCKIP/N)

The DAC code data written to the LTC2000A is captured on both the rising and falling edges of DCKIP/N. For single-port operation, provide a DDR clock at half the DAC sample clock frequency ($f_{DCKI} = f_{DAC}/2$). To use a 1.35GHz sample clock in single-port mode, provide a 675MHz clock on DCKIP/N. For dual-port operation, provide a DDR clock at one quarter the DAC sample clock frequency ($f_{DCKI} = f_{DAC}/4$). To use a 2.7GHz sample clock in dual-port mode, provide a 675MHz clock on DCKIP/N.

Table 3. DAC Sample Clock, and Divided Clock Output SPI Registers

ADDRESS	BIT	NAME	DESCRIPTION
0x02	0	CK_PD	CKP/N Clock Receiver Power Down When CK_PD = 1
	1	CK_OK	CKP/N Clock Present Indicator. When CK_OK = 1, clock is present at CKP/N pins and f_{DAC} > 50MHz. When CK_OK = 0, DAC output is forced to mid-scale. CK_OK is read only.
	4	DCKO_DIS	DCKOP/N Output Disable. Set DCKO_DIS = 1 to power down the DCKO LVDS transmitter. For DCKO_DIS = 1, DCKOP/N are high impedance.
	5	DCKO_DIV	DCKOP/N Divide Select. When DCKO_DIV = 0, $f_{DCKOP/N} = f_{DAC}/4$. When DCKO_DIV = 1, $f_{DCKOP/N} = f_{DAC}/2$.
	6	DCKO_ISEL	DCKOP/N Output Current Select. When DCKO_ISEL = 0, output current is 3.5mA. When DCKO_ISEL = 1, output current is 7mA.
	7	DCKO_TRM	DCKOP/N Internal Termination On. When DCKO_TRM = 0, there is no internal termination at DCKOP/N. When DCKO_TRM = 1, there is 100Ω between DCKOP and DCKON.

Note: Register 0x02 resets to 0x00 (default).