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## FEATURES

- 74dB SNR
- 88dB SFDR
- Low Power: 81mW/49mW/35mW
- Single 1.8V Supply
- CMOS, DDR CMOS or DDR LVDS Outputs
- Selectable Input Ranges: 1V<sub>P-P</sub> to 2V<sub>P-P</sub>
- 800MHz Full-Power Bandwidth S/H
- Optional Data Output Randomizer
- Optional Clock Duty Cycle Stabilizer
- Shutdown and Nap Modes
- Serial SPI Port for Configuration
- Pin Compatible 14-Bit and 12-Bit Versions
- 40-Pin (6mm × 6mm) QFN Package

## APPLICATIONS

- Communications
- Cellular Base Stations
- Software Defined Radios
- Portable Medical Imaging
- Multi-Channel Data Acquisition
- Nondestructive Testing

## DESCRIPTION

The [LTC®2258-14/LTC2257-14/LTC2256-14](#) are sampling 14-bit A/D converters designed for digitizing high frequency, wide dynamic range signals. They are perfect for demanding communications applications with AC performance that includes 74dB SNR and 88dB spurious free dynamic range (SFDR). Ultralow jitter of 0.17ps<sub>RMS</sub> allows undersampling of IF frequencies with excellent noise performance.

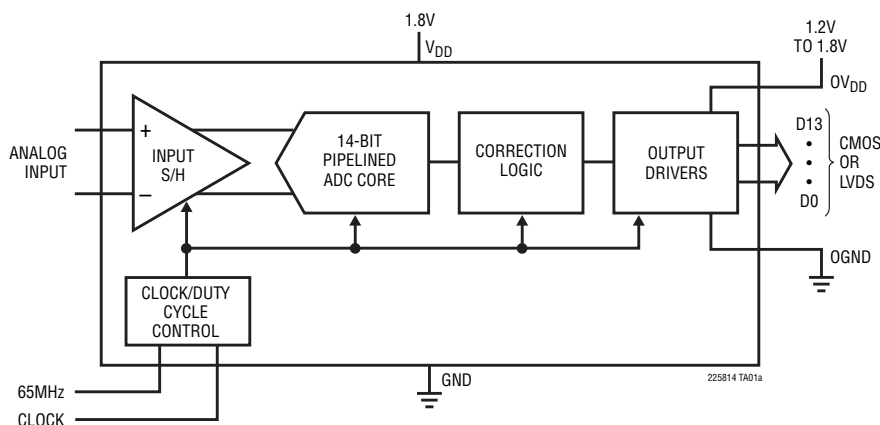
DC specs include ±1LSB INL (typical), ±0.3LSB DNL (typical) and no missing codes over temperature. The transition noise is a low 1.13LSB<sub>RMS</sub>.

The digital outputs can be either full rate CMOS, double data rate CMOS, or double data rate LVDS. A separate output power supply allows the CMOS output swing to range from 1.2V to 1.8V.

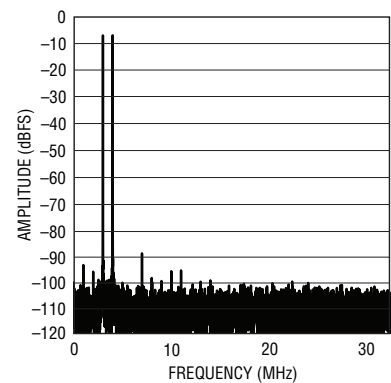
The ENC<sup>+</sup> and ENC<sup>-</sup> inputs may be driven differentially or single ended with a sine wave, PECL, LVDS, TTL or CMOS inputs. An optional clock duty cycle stabilizer allows high performance at full speed for a wide range of clock duty cycles.

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## TYPICAL APPLICATION



LTC2258-14 2-Tone FFT,  
 $f_{IN} = 68\text{MHz}$  and  $69\text{MHz}$



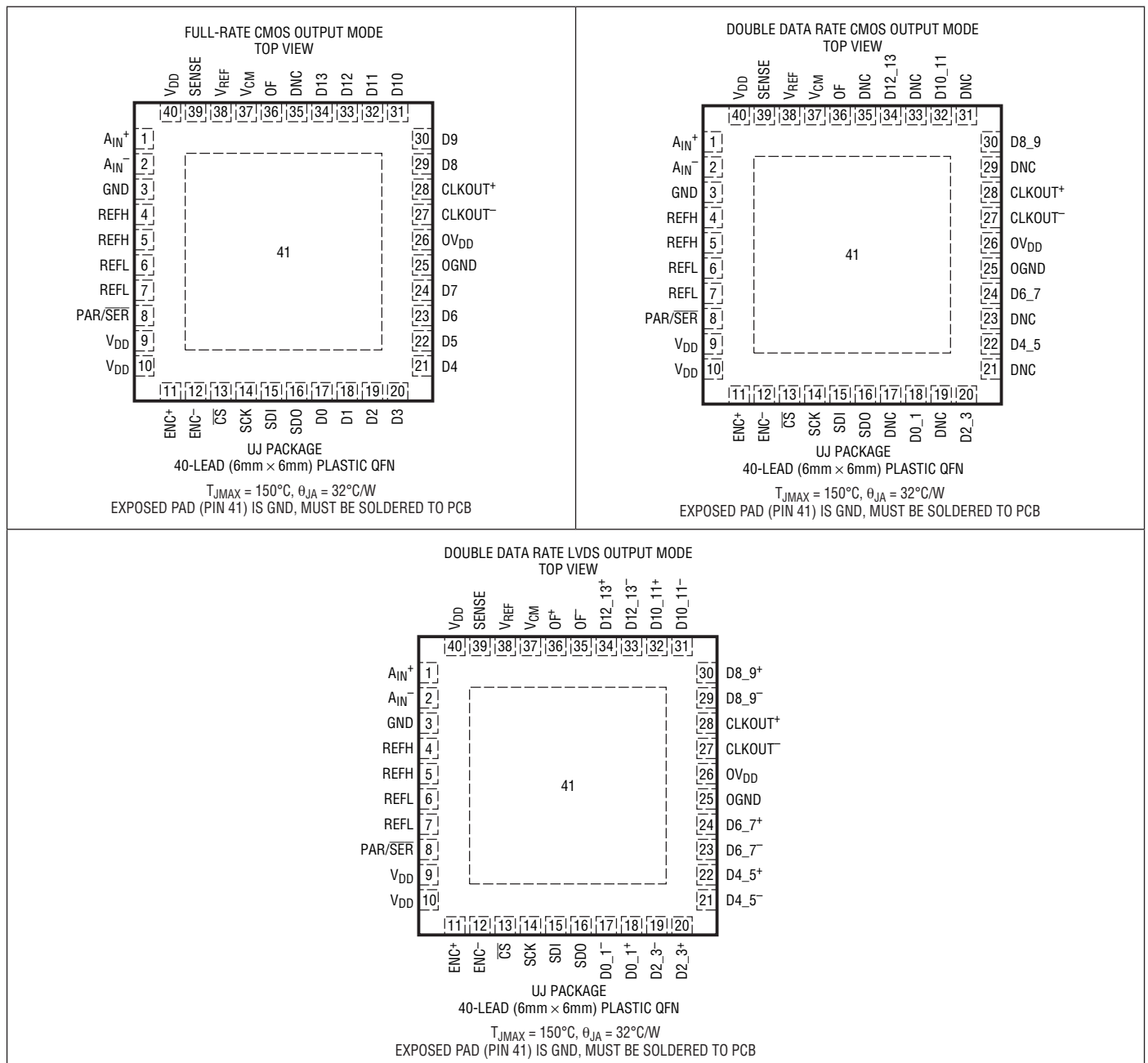
# LTC2258-14

## LTC2257-14/LTC2256-14

### ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Supply Voltages ( $V_{DD}$ , $OV_{DD}$ ).....	-0.3V to 2V	Digital Output Voltage.....	-0.3V to ( $OV_{DD} + 0.3V$ )
Analog Input Voltage ( $A_{IN}^+$ , $A_{IN}^-$ , PAR/SER, SENSE) (Note 3).....	-0.3V to ( $V_{DD} + 0.2V$ )	Operating Temperature Range:	
Digital Input Voltage ( $ENC^+$ , $ENC^-$ , CS, SDI, SCK) (Note 4).....	-0.3V to 3.9V	LTC2258C, LTC2257C, LTC2256C.....	0°C to 70°C
SDO (Note 4).....	-0.3V to 3.9V	LTC2258I, LTC2257I, LTC2256I.....	-40°C to 85°C
		Storage Temperature Range.....	-65°C to 150°C

### PIN CONFIGURATIONS



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## ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2258CUJ-14#PBF	LTC2258CUJ-14#TRPBF	LTC2258UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2258IUJ-14#PBF	LTC2258IUJ-14#TRPBF	LTC2258UJ-14	40-Lead (6mm × 6mm) Plastic QFN	−40°C to 85°C
LTC2257CUJ-14#PBF	LTC2257CUJ-14#TRPBF	LTC2257UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2257IUJ-14#PBF	LTC2257IUJ-14#TRPBF	LTC2257UJ-14	40-Lead (6mm × 6mm) Plastic QFN	−40°C to 85°C
LTC2256CUJ-14#PBF	LTC2256CUJ-14#TRPBF	LTC2256UJ-14	40-Lead (6mm × 6mm) Plastic QFN	0°C to 70°C
LTC2256IUJ-14#PBF	LTC2256IUJ-14#TRPBF	LTC2256UJ-14	40-Lead (6mm × 6mm) Plastic QFN	−40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 5)

PARAMETER	CONDITIONS	LTC2258-14			LTC2257-14			LTC2256-14			UNITS	
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
Resolution (No Missing Codes)		●	14		14		14		14		Bits	
Integral Linearity Error	Differential Analog Input (Note 6)	●	−3	±1	3	−2.5	±1	2.5	−2.5	±1	2.5	LSB
Differential Linearity Error	Differential Analog Input	●	−0.8	±0.3	0.8	−0.8	±0.3	0.8	−0.8	±0.3	0.8	LSB
Offset Error	(Note 7)	●	−9	±1.5	9	−9	±1.5	9	−9	±1.5	9	mV
Gain Error	Internal Reference			±1.5			±1.5			±1.5		%FS
	External Reference	●	−1.5	±0.4	1.5	−1.5	±0.4	1.5	−1.5	±0.4	1.5	%FS
Offset Drift				±20			±20			±20		μV/°C
Full-Scale Drift	Internal Reference			±30			±30			±30		ppm/°C
	External Reference			±10			±10			±10		ppm/°C
Transition Noise	External Reference			1.13			1.13			1.13		LSB <sub>RMS</sub>

# LTC2258-14

## LTC2257-14/LTC2256-14

### ANALOG INPUT

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}$	Analog Input Range ( $A_{IN}^+ - A_{IN}^-$ )	$1.7V < V_{DD} < 1.9V$	●		1 to 2		$V_{P-P}$
$V_{IN(CM)}$	Analog Input Common Mode ( $(A_{IN}^+ + A_{IN}^-)/2$ )	Differential Analog Input (Note 8)	●	$V_{CM} - 100\text{mV}$	$V_{CM}$	$V_{CM} + 100\text{mV}$	V
$V_{SENSE}$	External Voltage Reference Applied to SENSE	External Reference Mode	●	0.625	1.250	1.300	V
$I_{INCM}$	Analog Input Common Mode Current	Per Pin, 65MSPS Per Pin, 40MSPS Per Pin, 25MSPS			81 50 31		$\mu\text{A}$ $\mu\text{A}$ $\mu\text{A}$
$I_{IN1}$	Analog Input Leakage Current	$0 < A_{IN}^+, A_{IN}^- < V_{DD}$ , No Encode	●	-1		1	$\mu\text{A}$
$I_{IN2}$	PAR/SER Input Leakage Current	$0 < \text{PAR/SER} < V_{DD}$	●	-3		3	$\mu\text{A}$
$I_{IN3}$	SENSE Input Leakage Current	$0.625 < \text{SENSE} < 1.3V$	●	-6		6	$\mu\text{A}$
$t_{AP}$	Sample-and-Hold Acquisition Delay Time				0		ns
$t_{JITTER}$	Sample-and-Hold Acquisition Delay Jitter				0.17		psRMS
CMRR	Analog Input Common Mode Rejection Ratio				80		dB
BW-3B	Full-Power Bandwidth	Figure 6 Test Circuit			800		MHz

### DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$ . (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC2258-14			LTC2257-14			LTC2256-14			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-Noise Ratio	5MHz Input	●		74		73.4		72.9		dB	
		30MHz Input	●	72.4	73.8	71.9	73.2	71.2	72.8		dB	
		70MHz Input			73.7		73.1		72.1		dB	
		140MHz Input			73		72.6		71.8		dB	
SFDR	Spurious Free Dynamic Range 2nd or 3rd Harmonic	5MHz Input	●		90		90		90		dB	
		30MHz Input	●	78	90	80	90	80	90		dB	
		70MHz Input			90		90		90		dB	
		140MHz Input			84		84		84		dB	
	Spurious Free Dynamic Range 4th Harmonic or Higher	5MHz Input	●		90		90		90		dB	
		30MHz Input	●	85	90	85	90	85	90		dB	
S/(N+D)	Signal-to-Noise Plus Distortion Ratio	5MHz Input	●		73.8		73.2		72.8		dB	
		30MHz Input	●	71.5	73.7	71.5	73.1	70.7	72.7		dB	
		70MHz Input			73.6		73		72		dB	
		140MHz Input			72.5		72.3		71.2		dB	

### INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 5)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{CM}$ Output Voltage	$I_{OUT} = 0$	$0.5 \cdot V_{DD} - 25\text{mV}$	$0.5 \cdot V_{DD}$	$0.5 \cdot V_{DD} + 25\text{mV}$	V
$V_{CM}$ Output Temperature Drift			$\pm 25$		ppm/ $^\circ\text{C}$
$V_{CM}$ Output Resistance	$-600\mu\text{A} < I_{OUT} < 1\text{mA}$		4		$\Omega$
$V_{REF}$ Output Voltage	$I_{OUT} = 0$	1.225	1.250	1.275	V
$V_{REF}$ Output Temperature Drift			$\pm 25$		ppm/ $^\circ\text{C}$
$V_{REF}$ Output Resistance	$-400\mu\text{A} < I_{OUT} < 1\text{mA}$		7		$\Omega$
$V_{REF}$ Line Regulation	$1.7V < V_{DD} < 1.9V$		0.6		mV/V

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**DIGITAL INPUTS AND OUTPUTS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>ENCODE INPUTS (ENC<sup>+</sup>, ENC<sup>-</sup>)</b>							
<b>Differential Encode Mode (ENC<sup>-</sup> Not Tied to GND)</b>							
V <sub>ID</sub>	Differential Input Voltage	(Note 8)	●	0.2			V
V <sub>ICM</sub>	Common Mode Input Voltage	Internally Set Externally Set (Note 8)	●	1.1	1.2	1.6	V V
V <sub>IN</sub>	Input Voltage Range	ENC <sup>+</sup> , ENC <sup>-</sup> to GND	●	0.2		3.6	V
R <sub>IN</sub>	Input Resistance	(See Figure 10)			10		kΩ
C <sub>IN</sub>	Input Capacitance	(Note 8)			3.5		pF
<b>Single-Ended Encode Mode (ENC<sup>-</sup> Tied to GND)</b>							
V <sub>IH</sub>	High Level Input Voltage	V <sub>DD</sub> = 1.8V	●	1.2			V
V <sub>IL</sub>	Low Level Input Voltage	V <sub>DD</sub> = 1.8V	●			0.6	V
V <sub>IN</sub>	Input Voltage Range	ENC <sup>+</sup> to GND	●	0		3.6	V
R <sub>IN</sub>	Input Resistance	(See Figure 11)			30		kΩ
C <sub>IN</sub>	Input Capacitance	(Note 8)			3.5		pF
<b>DIGITAL INPUTS (CS, SDI, SCK)</b>							
V <sub>IH</sub>	High Level Input Voltage	V <sub>DD</sub> = 1.8V	●	1.3			V
V <sub>IL</sub>	Low Level Input Voltage	V <sub>DD</sub> = 1.8V	●			0.6	V
I <sub>IN</sub>	Input Current	V <sub>IN</sub> = 0V to 3.6V	●	-10		10	μA
C <sub>IN</sub>	Input Capacitance	(Note 8)			3		pF
<b>SDO OUTPUT (Open-Drain Output. Requires 2k Pull-Up Resistor if SDO is Used)</b>							
R <sub>OL</sub>	Logic Low Output Resistance to GND	V <sub>DD</sub> = 1.8V, SDO = 0V			200		Ω
I <sub>OH</sub>	Logic High Output Leakage Current	SDO = 0V to 3.6V	●	-10		10	μA
C <sub>OUT</sub>	Output Capacitance	(Note 8)			4		pF
<b>DIGITAL DATA OUTPUTS (CMOS MODES: FULL DATA RATE AND DOUBLE DATA RATE)</b>							
<b>OV<sub>DD</sub> = 1.8V</b>							
V <sub>OH</sub>	High Level Output Voltage	I <sub>O</sub> = -500μA	●	1.750	1.790		V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>O</sub> = 500μA	●		0.010	0.050	V
<b>OV<sub>DD</sub> = 1.5V</b>							
V <sub>OH</sub>	High Level Output Voltage	I <sub>O</sub> = -500μA			1.488		V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>O</sub> = 500μA			0.010		V
<b>OV<sub>DD</sub> = 1.2V</b>							
V <sub>OH</sub>	High Level Output Voltage	I <sub>O</sub> = -500μA			1.185		V
V <sub>OL</sub>	Low Level Output Voltage	I <sub>O</sub> = 500μA			0.010		V
<b>DIGITAL DATA OUTPUTS (LVDS MODE)</b>							
V <sub>OD</sub>	Differential Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	247	350 175	454	mV mV
V <sub>OS</sub>	Common Mode Output Voltage	100Ω Differential Load, 3.5mA Mode 100Ω Differential Load, 1.75mA Mode	●	1.125	1.250 1.250	1.375	V V
R <sub>TERM</sub>	On-Chip Termination Resistance	Termination Enabled, OV <sub>DD</sub> = 1.8V			100		Ω

# LTC2258-14

## LTC2257-14/LTC2256-14

### POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. (Note 9)

SYMBOL	PARAMETER	CONDITIONS	LTC2258-14			LTC2257-14			LTC2256-14			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
<b>CMOS Output Modes: Full Data Rate and Double Data Rate</b>													
V <sub>DD</sub>	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV <sub>DD</sub>	Output Supply Voltage	(Note 10)	●	1.1		1.9	1.1		1.9	1.1		1.9	V
I <sub>VDD</sub>	Analog Supply Current	DC Input Sine Wave Input	●		44.7	49.5		27	30		19.5	22	mA mA
I <sub>OVDD</sub>	Digital Supply Current	Sine Wave Input, OV <sub>DD</sub> =1.2V			2.6			1.6			1.1		mA
P <sub>DISS</sub>	Power Dissipation	DC Input Sine Wave Input, OV <sub>DD</sub> =1.2V	●		80.5	90		48.6	54		35.1	40	mW mW
					84.7			52.1			37.1		
<b>LVDS Output Mode</b>													
V <sub>DD</sub>	Analog Supply Voltage	(Note 10)	●	1.7	1.8	1.9	1.7	1.8	1.9	1.7	1.8	1.9	V
OV <sub>DD</sub>	Output Supply Voltage	(Note 10)	●	1.7		1.9	1.7		1.9	1.7		1.9	V
I <sub>VDD</sub>	Analog Supply Current	Sine Wave Input	●		48.9	54		31.4	35		23.5	26	mA
I <sub>OVDD</sub>	Digital Supply Current	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	● ●		20.7	23		20.7	23		20.7	23	mA mA
					40.5	44		40.5	44		40.5	44	
P <sub>DISS</sub>	Power Dissipation	Sine Input, 1.75mA Mode Sine Input, 3.5mA Mode	● ●		125.3	139		93.8	105		79.6	89	mW mW
					160.9	177		129.4	143		115.2	126	
<b>All Output Modes</b>													
P <sub>SLEEP</sub>	Sleep Mode Power				0.5			0.5			0.5		mW
P <sub>NAP</sub>	Nap Mode Power				9			9			9		mW
P <sub>DIFFCLK</sub>	Power Increase with Differential Encode Mode Enabled (No increase for Nap or Sleep Modes)				10			10			10		mW

### TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T<sub>A</sub> = 25°C. (Note 5)

SYMBOL	PARAMETER	CONDITIONS	LTC2258-14			LTC2257-14			LTC2256-14			UNITS	
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
f <sub>S</sub>	Sampling Frequency	(Note 10)	●	1		65	1		40	1		25	MHz
t <sub>L</sub>	ENC Low Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	7.3	7.69	500	11.88	12.5	500	19	20	500	ns ns
t <sub>H</sub>	ENC High Time (Note 8)	Duty Cycle Stabilizer Off Duty Cycle Stabilizer On	● ●	7.3	7.69	500	11.88	12.5	500	19	20	500	ns ns
					2.0	7.69	500		2.00	12.5	500		
t <sub>AP</sub>	Sample-and-Hold Acquisition Delay Time				0			0			0		ns

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>Digital Data Outputs (CMOS Modes: Full Data Rate and Double Data Rate)</b>						
t <sub>D</sub>	ENC to Data Delay	C <sub>L</sub> = 5pF (Note 8)	●	1.1	1.7	3.1 ns
t <sub>C</sub>	ENC to CLKOUT Delay	C <sub>L</sub> = 5pF (Note 8)	●	1	1.4	2.6 ns
t <sub>SKEW</sub>	DATA to CLKOUT Skew	t <sub>D</sub> - t <sub>C</sub> (Note 8)	●	0	0.3	0.6 ns
	Pipeline Latency	Full Data Rate Mode Double Data Rate Mode			5.0 5.5	Cycles Cycles

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**TIMING CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 5)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
<b>Digital Data Outputs (LVDS Mode)</b>							
$t_D$	ENC to Data Delay	$C_L = 5\text{pF}$ (Note 8)	●	1.1	1.8	3.2	ns
$t_C$	ENC to CLKOUT Delay	$C_L = 5\text{pF}$ (Note 8)	●	1	1.5	2.7	ns
$t_{\text{SKEW}}$	DATA to CLKOUT Skew	$t_D - t_C$ (Note 8)	●	0	0.3	0.6	ns
	Pipeline Latency				5.5		Cycles
<b>SPI Port Timing (Note 8)</b>							
$t_{\text{SCK}}$	SCK Period	Write Mode Readback Mode, $C_{\text{SDO}} = 20\text{pF}$ , $R_{\text{PULLUP}} = 2\text{k}$	● ●	40 250			ns ns
$t_S$	$\overline{\text{CS}}$ to SCK Setup Time		●	5			ns
$t_H$	SCK to $\overline{\text{CS}}$ Setup Time		●	5			ns
$t_{\text{DS}}$	SDI Setup Time		●	5			ns
$t_{\text{DH}}$	SDI Hold Time		●	5			ns
$t_{\text{DO}}$	SCK Falling to SDO Valid	Readback Mode, $C_{\text{SDO}} = 20\text{pF}$ , $R_{\text{PULLUP}} = 2\text{k}$	●			125	ns

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND with GND and OGND shorted (unless otherwise noted).

**Note 3:** When these pin voltages are taken below GND or above  $V_{\text{DD}}$ , they will be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND or above  $V_{\text{DD}}$  without latchup.

**Note 4:** When these pin voltages are taken below GND they will be clamped by internal diodes. When these pin voltages are taken above  $V_{\text{DD}}$  they will not be clamped by internal diodes. This product can handle input currents of greater than 100mA below GND without latchup.

**Note 5:**  $V_{\text{DD}} = 0V_{\text{DD}} = 1.8\text{V}$ ,  $f_{\text{SAMPLE}} = 65\text{MHz}$  (LTC2258), 40MHz (LTC2257), or 25MHz (LTC2256), LVDS outputs with internal

termination disabled, differential  $\text{ENC}^+/\text{ENC}^- = 2V_{\text{P-P}}$  sine wave, input range =  $2V_{\text{P-P}}$  with differential drive, unless otherwise noted.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a best fit straight line to the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** Offset error is the offset voltage measured from  $-0.5$  LSB when the output code flickers between 00 0000 0000 0000 and 11 1111 1111 1111 in 2's complement output mode.

**Note 8:** Guaranteed by design, not subject to test.

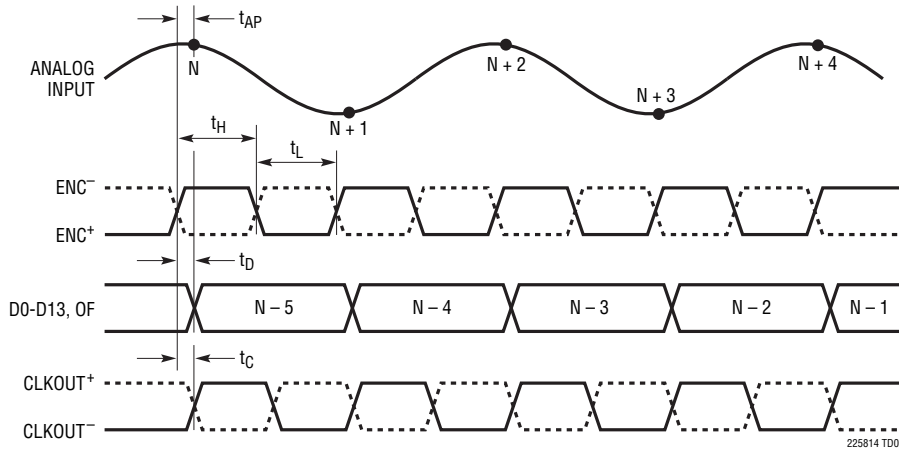
**Note 9:**  $V_{\text{DD}} = 1.8\text{V}$ ,  $f_{\text{SAMPLE}} = 65\text{MHz}$  (LTC2258), 40MHz (LTC2257), or 25MHz (LTC2256),  $\text{ENC}^+ = \text{single-ended } 1.8\text{V}$  square wave,  $\text{ENC}^- = 0\text{V}$ , input range =  $2V_{\text{P-P}}$  with differential drive, 5pF load on each digital output unless otherwise noted.

**Note 10:** Recommended operating conditions.

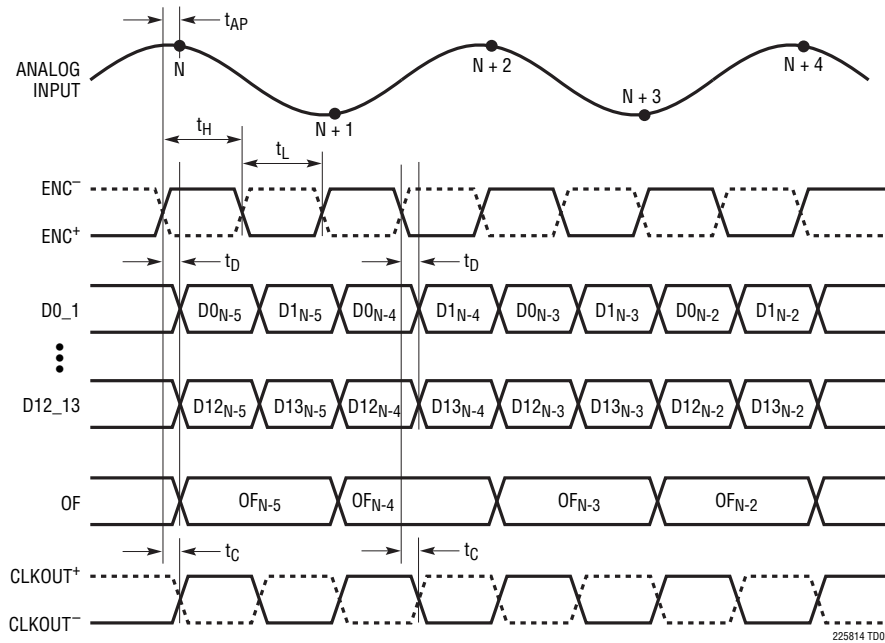


## TIMING DIAGRAMS

**Full-Rate CMOS Output Mode Timing**  
All Outputs Are Single-Ended and Have CMOS Levels

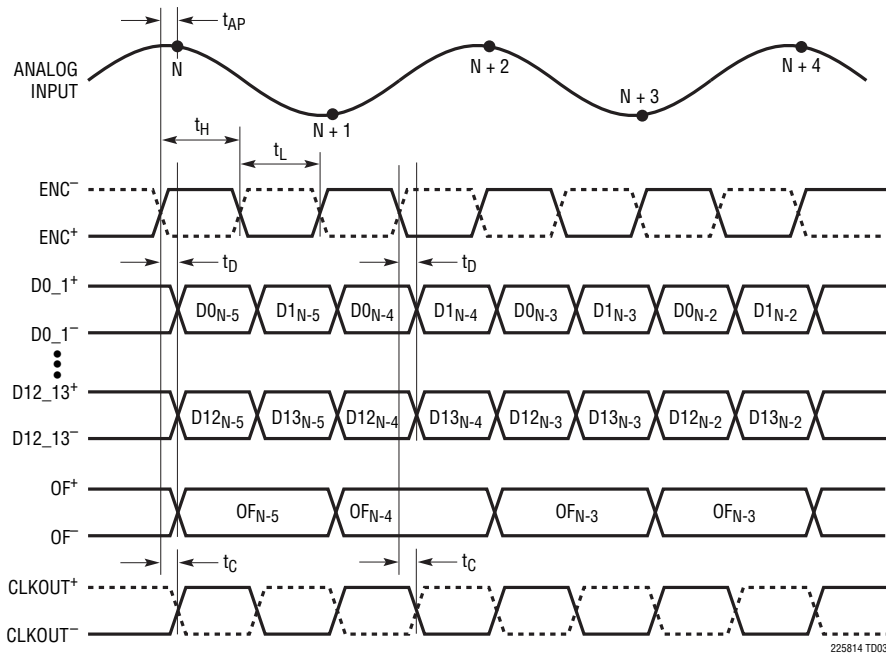


**Double Data Rate CMOS Output Mode Timing**  
All Outputs Are Single-Ended and Have CMOS Levels

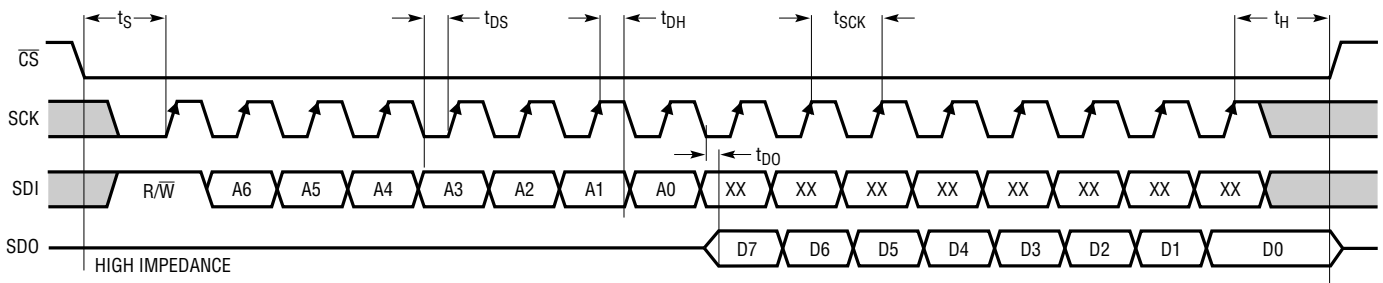


## TIMING DIAGRAMS

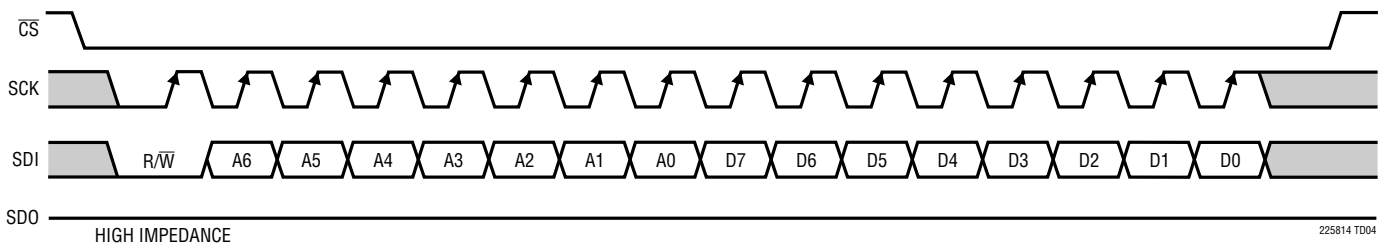
**Double Data Rate LVDS Output Mode Timing**  
All Outputs Are Differential and Have LVDS Levels



**SPI Port Timing (Readback Mode)**

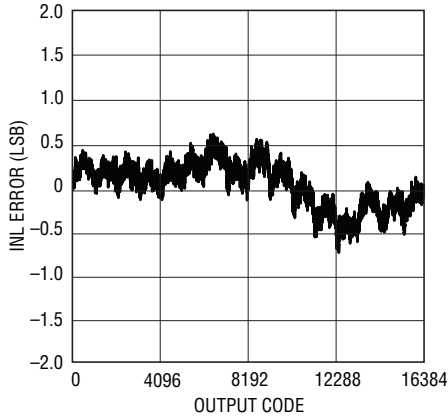


**SPI Port Timing (Write Mode)**



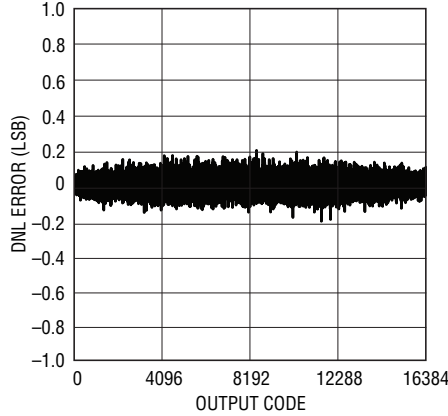
## TYPICAL PERFORMANCE CHARACTERISTICS

LTC2258-14: Integral Nonlinearity (INL)



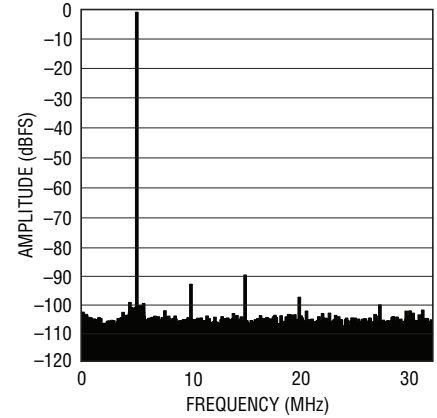
225814 G01

LTC2258-14: Differential Nonlinearity (DNL)



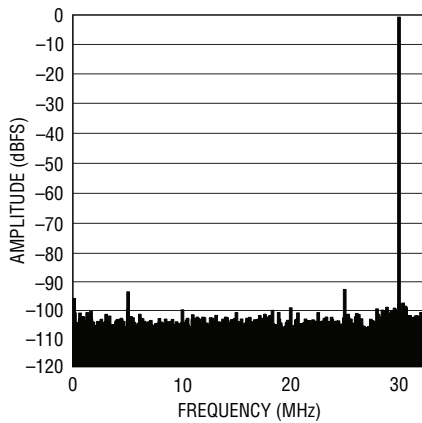
225814 G02

LTC2258-14: 8k Point FFT,  $f_{IN} = 5\text{MHz}$ ,  $-1\text{dBFS}$ , 65Mps



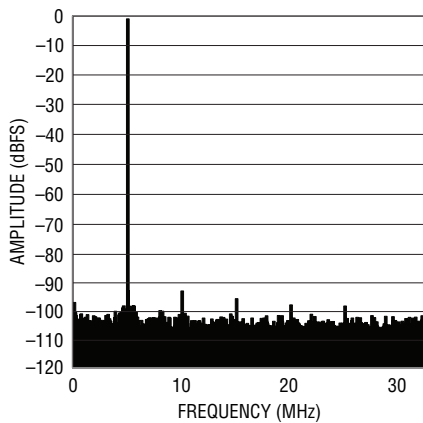
225814 G03

LTC2258-14: 8k Point FFT,  $f_{IN} = 30\text{MHz}$ ,  $-1\text{dBFS}$ , 65Mps



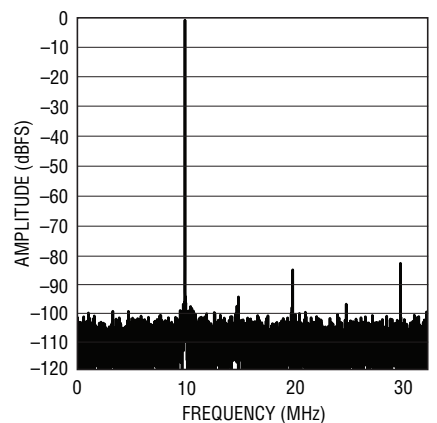
225814 G04

LTC2258-14: 8k Point FFT,  $f_{IN} = 70\text{MHz}$ ,  $-1\text{dBFS}$ , 65Mps



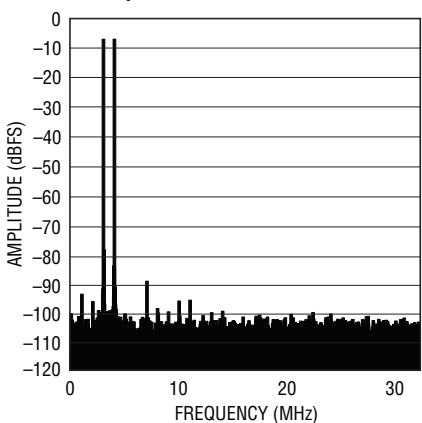
225814 G05

LTC2258-14: 8k Point FFT,  $f_{IN} = 140\text{MHz}$ ,  $-1\text{dBFS}$ , 65Mps



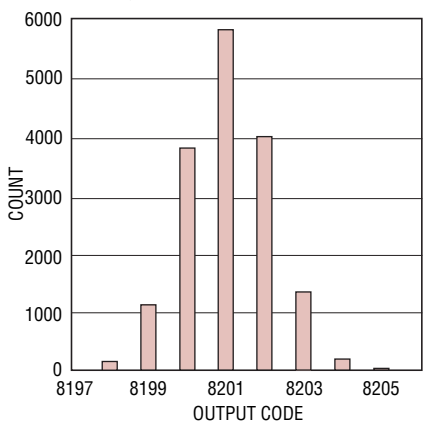
225814 G06

LTC2258-14: 8k Point 2-Tone FFT,  $f_{IN} = 68\text{MHz}$ ,  $69\text{MHz}$ ,  $-1\text{dBFS}$ , 65Mps



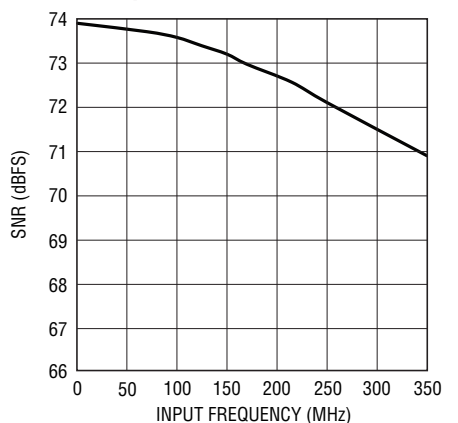
225814 G07

LTC2258-14: Shorted Input Histogram



225814 G08

LTC2258-14: SNR vs Input Frequency,  $-1\text{dB}$ , 2V Range, 65Mps

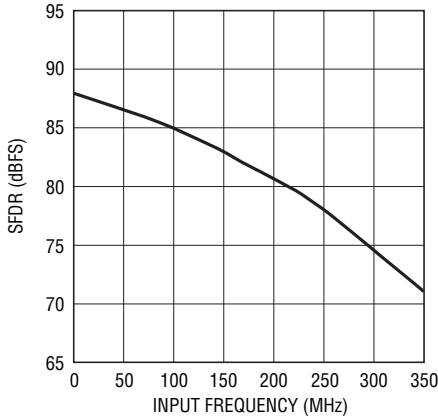


225814 G09

225814fc

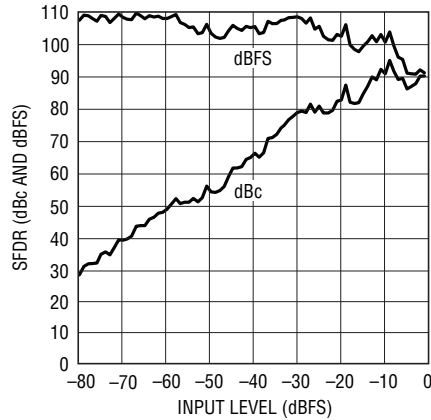
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC2258-14: SFDR vs Input Frequency, -1dB, 2V Range, 65Mps**



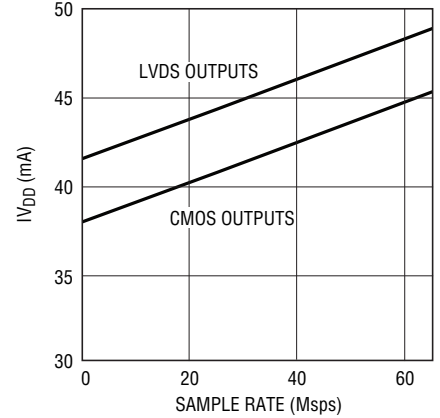
225814 G10

**LTC2258-14: SFDR vs Input Level,  $f_{IN} = 70\text{MHz}$ , 2V Range, 65Mps**



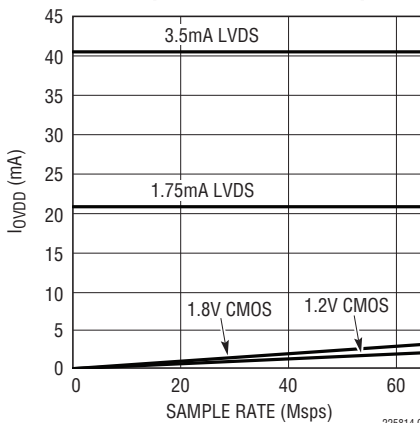
225814 G12

**LTC2258-14:  $I_{VDD}$  vs Sample Rate, 5MHz Sine Wave Input, -1dB**



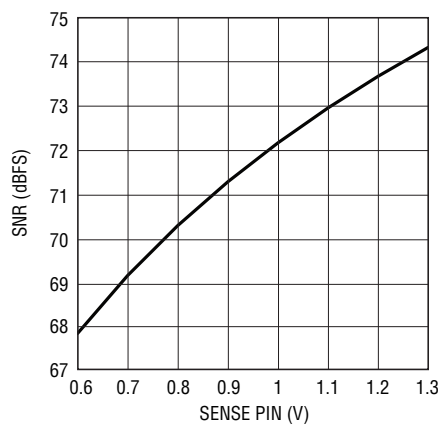
225814 G13

**LTC2258-14:  $I_{OVD}$  vs Sample Rate, 5MHz Sine Wave Input, -1dB, 5pF on Each Data Output**



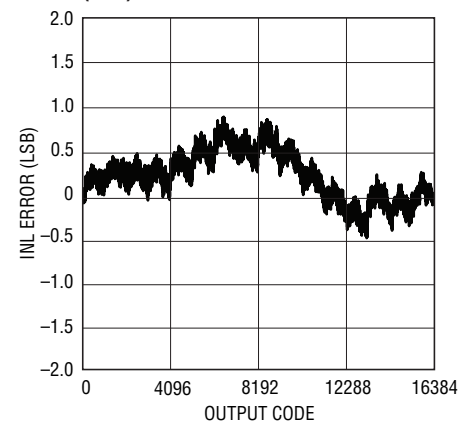
225814 G14

**LTC2258-14: SNR vs SENSE,  $f_{IN} = 5\text{MHz}$ , -1dB**



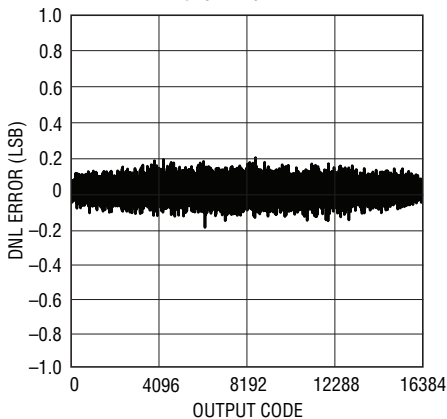
225814 G15

**LTC2257-14: Integral Nonlinearity (INL)**



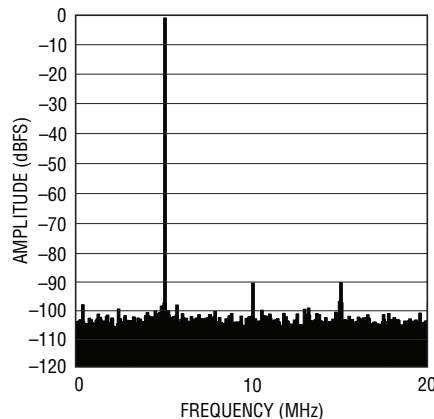
225814 G21

**LTC2257-14: Differential Nonlinearity (DNL)**



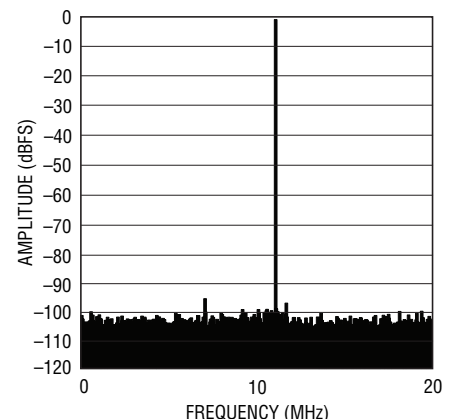
225814 G22

**LTC2257-14: 8k Point FFT,  $f_{IN} = 5\text{MHz}$ , -1dBFS, 40Mps**



225814 G23

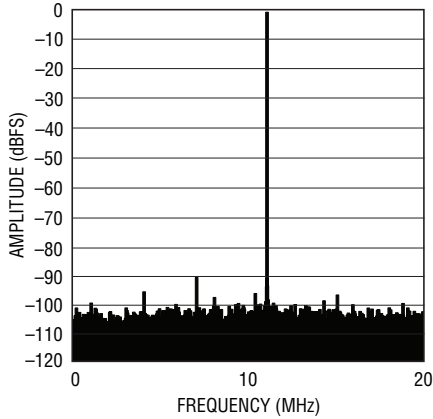
**LTC2257-14: 8k Point FFT,  $f_{IN} = 29\text{MHz}$ , -1dBFS, 40Mps**



225814 G24

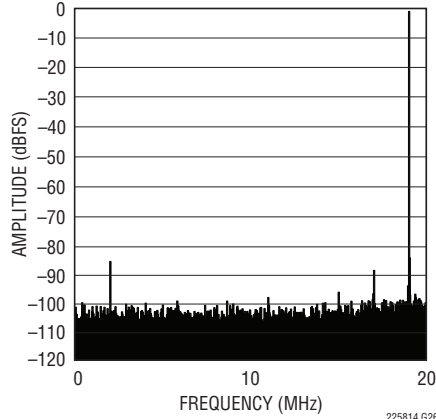
## TYPICAL PERFORMANCE CHARACTERISTICS

LTC2257-14: 8k Point FFT,  
 $f_{IN} = 69\text{MHz}$ ,  $-1\text{dBFS}$ ,  $40\text{Mps}$



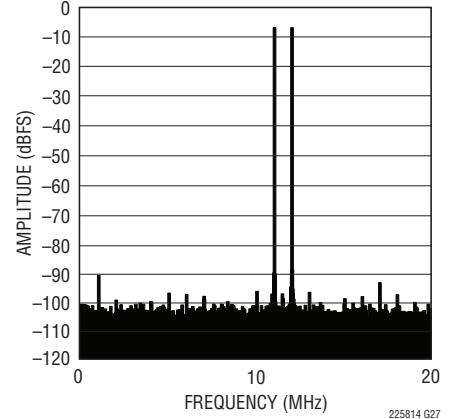
225814 G25

LTC2257-14: 8k Point FFT,  
 $f_{IN} = 139\text{MHz}$ ,  $-1\text{dBFS}$ ,  $40\text{Mps}$



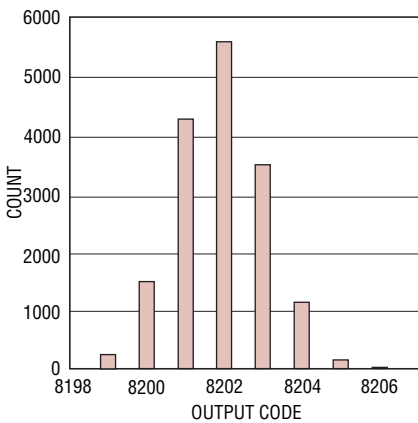
225814 G26

LTC2257-14: 8k Point 2-Tone FFT,  
 $f_{IN} = 68\text{MHz}$ ,  $69\text{MHz}$ ,  $-1\text{dBFS}$ ,  
 $40\text{Mps}$



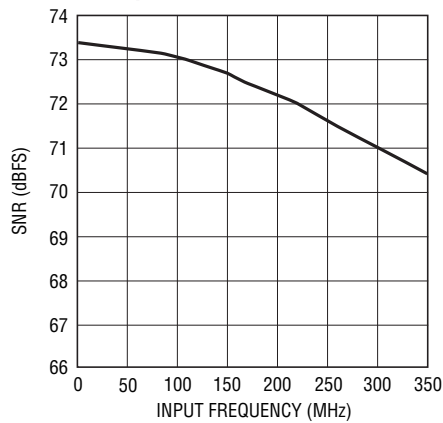
225814 G27

LTC2257-14: Shorted Input  
Histogram



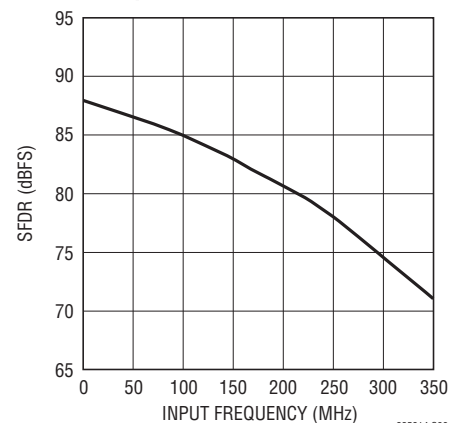
225814 G28

LTC2257-14: SNR vs Input  
Frequency,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $40\text{Mps}$



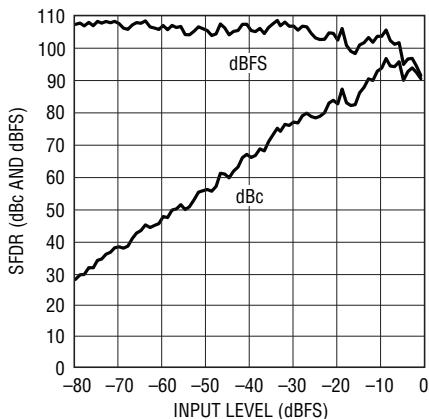
225814 G29

LTC2257-14: SFDR vs Input  
Frequency,  $-1\text{dB}$ ,  $2\text{V}$  Range,  
 $40\text{Mps}$



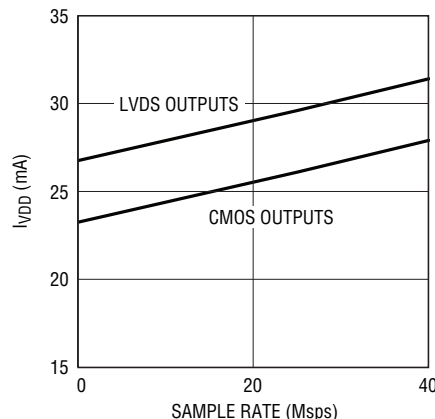
225814 G30

LTC2257-14: SFDR vs Input Level,  
 $f_{IN} = 70\text{MHz}$ ,  $2\text{V}$  Range,  $40\text{Mps}$



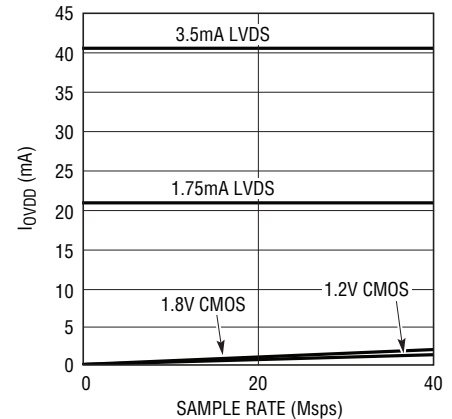
225814 G32

LTC2257-14:  $I_{VDD}$  vs Sample Rate,  
 $5\text{MHz}$  Sine Wave Input,  $-1\text{dB}$



225814 G33

LTC2257-14:  $I_{VDD}$  vs Sample  
Rate,  $5\text{MHz}$  Sine Wave Input,  
 $-1\text{dB}$ ,  $5\text{pF}$  on Each Data Output



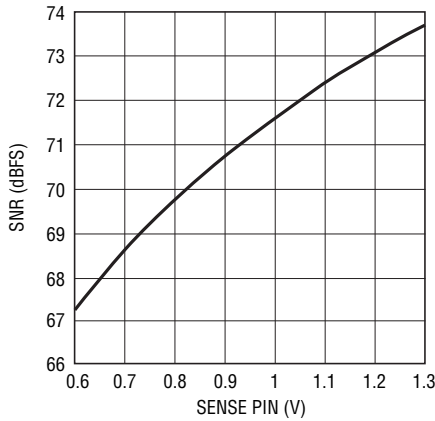
225814 G34

225814fc



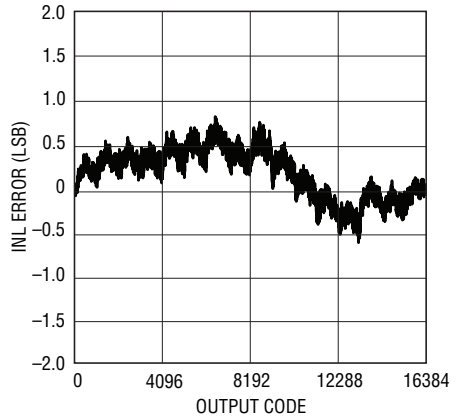
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC2257-14: SNR vs SENSE,**  
 $f_{IN} = 5\text{MHz}, -1\text{dB}$



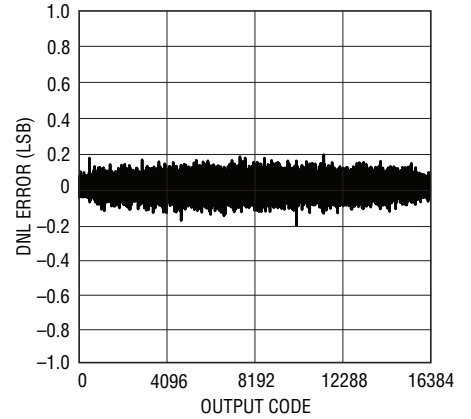
225814 G35

**LTC2256-14: Integral Nonlinearity (INL)**



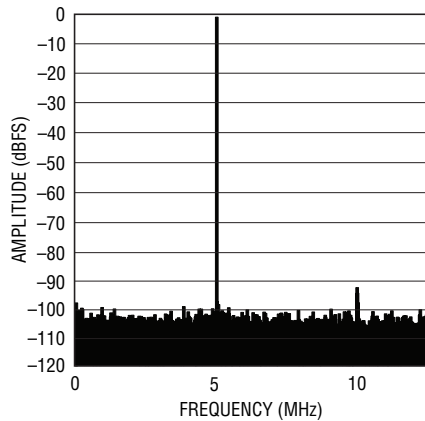
225814 G41

**LTC2256-14: Differential Nonlinearity (DNL)**



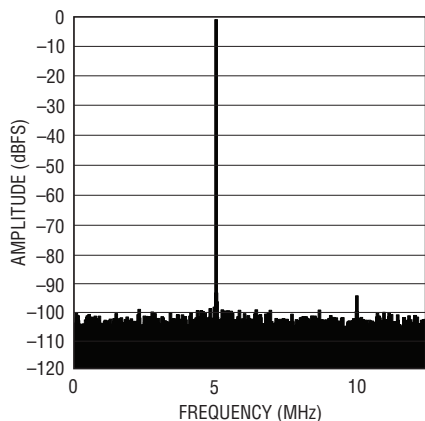
225814 G42

**LTC2256-14: 8k Point FFT,**  
 $f_{IN} = 5\text{MHz}, -1\text{dBFS}, 25\text{Mpsps}$



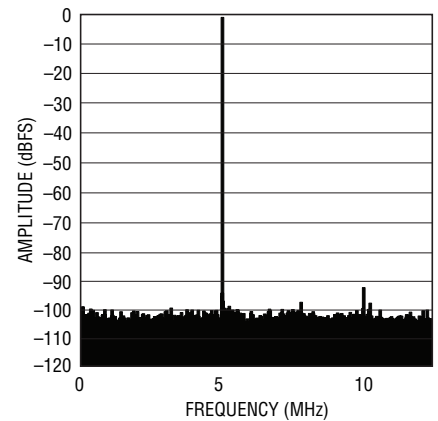
225814 G43

**LTC2256-14: 8k Point FFT,**  
 $f_{IN} = 30\text{MHz}, -1\text{dBFS}, 25\text{Mpsps}$



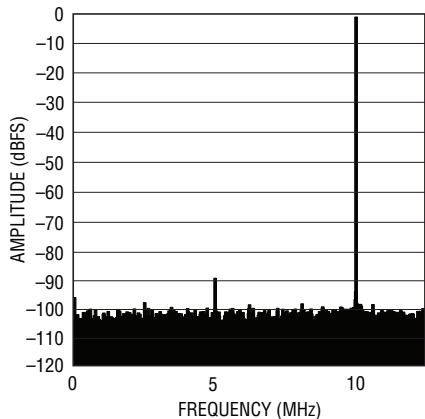
225814 G44

**LTC2256-14: 8k Point FFT,**  
 $f_{IN} = 70\text{MHz}, -1\text{dBFS}, 25\text{Mpsps}$



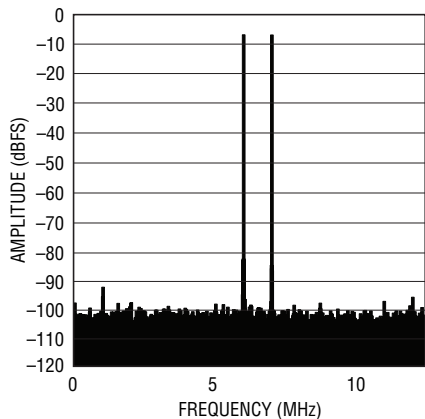
225814 G45

**LTC2256-14: 8k Point FFT,**  
 $f_{IN} = 140\text{MHz}, -1\text{dBFS}, 25\text{Mpsps}$



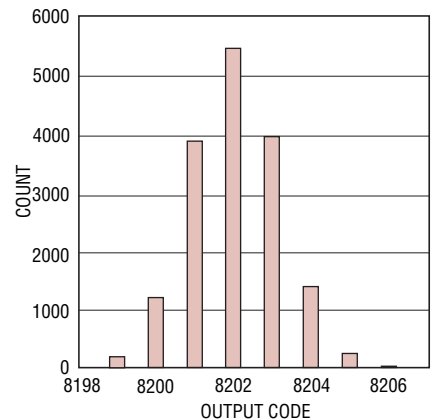
225814 G46

**LTC2256-14: 8k Point 2-Tone FFT,**  
 $f_{IN} = 68\text{MHz}, 69\text{MHz}, -1\text{dBFS}, 25\text{Mpsps}$



225814 G47

**LTC2256-14: Shorted Input Histogram**

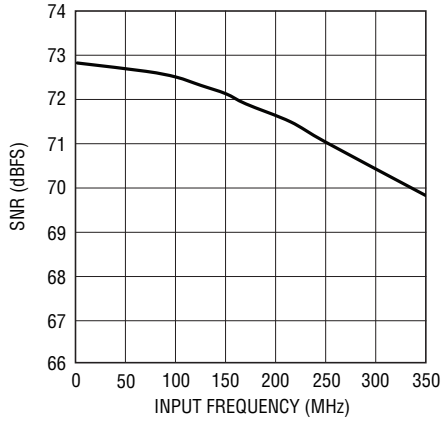


225814 G48

225814fc

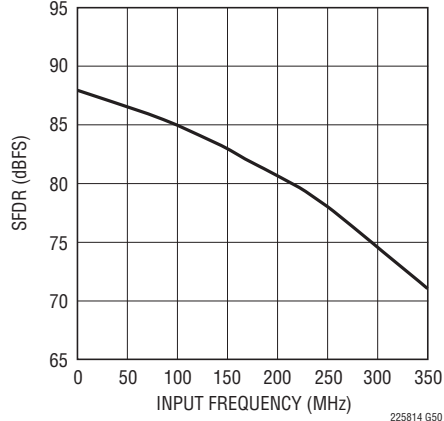
## TYPICAL PERFORMANCE CHARACTERISTICS

**LTC2256-14: SNR vs Input Frequency, -1dB, 2V Range, 25Mpsps**



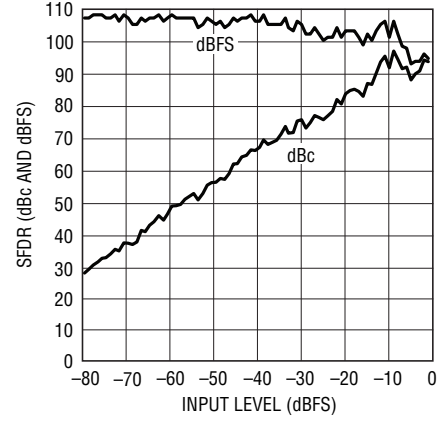
225814 G49

**LTC2256-14: SFDR vs Input Frequency, -1dB, 2V Range, 25Mpsps**



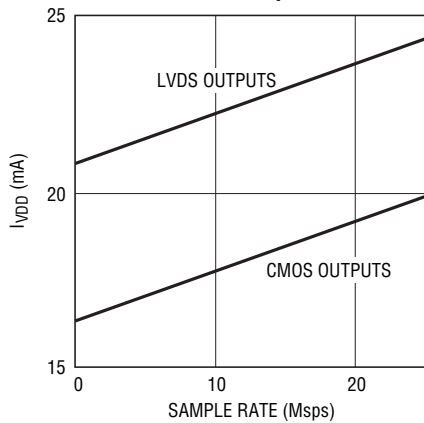
225814 G50

**LTC2256-14: SFDR vs Input Level,  $f_{IN} = 70\text{MHz}$ , 2V Range, 25Mpsps**



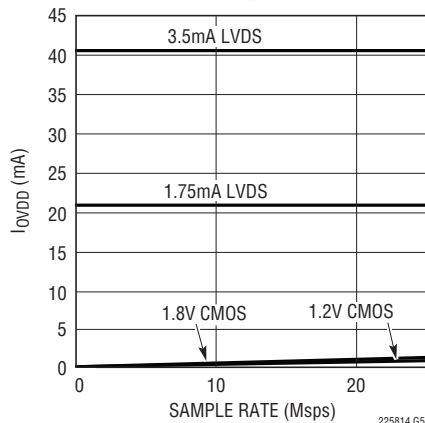
225814 G52

**LTC2256-14:  $I_{VDD}$  vs Sample Rate, 5MHz Sine Wave Input, -1dB**



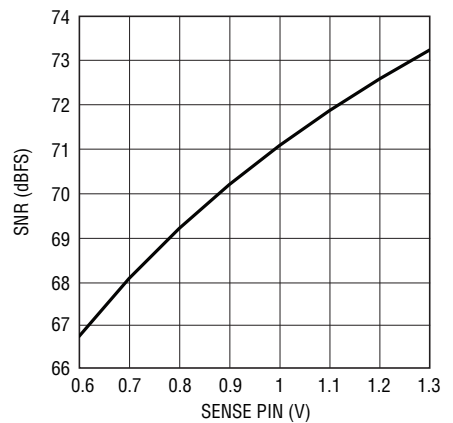
225814 G53

**LTC2256-14:  $I_{OVD}$  vs Sample Rate, 5MHz Sine Wave Input, -1dB, 5pF on Each Data Output**



225814 G54

**LTC2256-14: SNR vs SENSE,  $f_{IN} = 5\text{MHz}$ , -1dB**



225814 G55

## PIN FUNCTIONS

### PINS THAT ARE THE SAME FOR ALL DIGITAL OUTPUT MODES

**A<sub>IN</sub><sup>+</sup> (Pin 1):** Positive Differential Analog Input.

**A<sub>IN</sub><sup>-</sup> (Pin 2):** Negative Differential Analog Input.

**GND (Pin 3):** ADC Power Ground.

**REFH (Pins 4, 5):** ADC High Reference. Bypass to Pins 6, 7 with a 2.2μF ceramic capacitor and to ground with a 0.1μF ceramic capacitor.

**REFL (Pins 6, 7):** ADC Low Reference. Bypass to Pins 4, 5 with a 2.2μF ceramic capacitor and to ground with a 0.1μF ceramic capacitor.

**PAR/ $\overline{\text{SER}}$  (Pin 8):** Programming Mode Selection Pin. Connect to ground to enable the serial programming mode.  $\overline{\text{CS}}$ , SCK, SDI, SDO become a serial interface that control the A/D operating modes. Connect to V<sub>DD</sub> to enable the parallel programming mode where  $\overline{\text{CS}}$ , SCK, SDI become parallel logic inputs that control a reduced set of the A/D operating modes. PAR/ $\overline{\text{SER}}$  should be connected directly to ground or the V<sub>DD</sub> of the part and not be driven by a logic signal.

**V<sub>DD</sub> (Pins 9, 10, 40):** 1.8V Analog Power Supply. Bypass to ground with 0.1μF ceramic capacitors. Pins 9 and 10 can share a bypass capacitor.

**ENC<sup>+</sup> (Pin 11):** Encode Input. Conversion starts on the rising edge.

**ENC<sup>-</sup> (Pin 12):** Encode Complement Input. Conversion starts on the falling edge.

**$\overline{\text{CS}}$  (Pin 13):** In serial programming mode, (PAR/ $\overline{\text{SER}}$  = 0V),  $\overline{\text{CS}}$  is the serial interface chip select input. When  $\overline{\text{CS}}$  is low, SCK is enabled for shifting data on SDI into the mode control registers. In the parallel programming mode (PAR/ $\overline{\text{SER}}$  = V<sub>DD</sub>),  $\overline{\text{CS}}$  controls the clock duty cycle stabilizer. When  $\overline{\text{CS}}$  is low, the clock duty cycle stabilizer is turned off. When  $\overline{\text{CS}}$  is high, the clock duty cycle stabilizer is turned on.  $\overline{\text{CS}}$  can be driven with 1.8V to 3.3V logic.

**SCK (Pin 14):** In serial programming mode, (PAR/ $\overline{\text{SER}}$  = 0V), SCK is the serial interface clock input. In the

parallel programming mode (PAR/ $\overline{\text{SER}}$  = V<sub>DD</sub>), SCK controls the digital output mode. When SCK is low, the full-rate CMOS output mode is enabled. When SCK is high, the double data rate LVDS output mode (with 3.5mA output current) is enabled. SCK can be driven with 1.8V to 3.3V logic.

**SDI (Pin 15):** In serial programming mode, (PAR/ $\overline{\text{SER}}$  = 0V), SDI is the serial interface data input. Data on SDI is clocked into the mode control registers on the rising edge of SCK. In the parallel programming mode (PAR/ $\overline{\text{SER}}$  = V<sub>DD</sub>), SDI can be used to power down the part. When SDI is low, the part operates normally. When SDI is high, the part enters sleep mode. SDI can be driven with 1.8V to 3.3V logic.

**SDO (Pin 16):** In serial programming mode, (PAR/ $\overline{\text{SER}}$  = 0V), SDO is the optional serial interface data output. Data on SDO is read back from the mode control registers and can be latched on the falling edge of SCK. SDO is an open-drain NMOS output that requires an external 2k pull-up resistor to 1.8V-3.3V. If read back from the mode control registers is not needed, the pull-up resistor is not necessary and SDO can be left unconnected. In the parallel programming mode (PAR/ $\overline{\text{SER}}$  = V<sub>DD</sub>), SDO is not used and should not be connected.

**OGND (Pin 25):** Output Driver Ground.

**OV<sub>DD</sub> (Pin 26):** Output Driver Supply. Bypass to ground with a 0.1μF ceramic capacitor.

**V<sub>CM</sub> (Pin 37):** Common Mode Bias Output, Nominally Equal to V<sub>DD</sub>/2. V<sub>CM</sub> should be used to bias the common mode of the analog inputs. Bypass to ground with a 0.1μF ceramic capacitor.

**V<sub>REF</sub> (Pin 38):** Reference Voltage Output, Nominally 1.25V. Bypass to ground with a 1μF ceramic capacitor.

**SENSE (Pin 39):** Reference Programming Pin. Connecting SENSE to V<sub>DD</sub> selects the internal reference and a ±1V input range. Connecting SENSE to ground selects the internal reference and a ±0.5V input range. An external reference between 0.625V and 1.3V applied to SENSE selects an input range of ±0.8 • V<sub>SENSE</sub>.

## PIN FUNCTIONS

### FULL-RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to  $OV_{DD}$ )

**D0 to D13 (Pins 17-24, 29-34):** Digital Outputs. D13 is the MSB.

**CLKOUT<sup>-</sup> (Pin 27):** Inverted version of CLKOUT<sup>+</sup>.

**CLKOUT<sup>+</sup> (Pin 28):** Data Output Clock. The digital outputs normally transition at the same time as the falling edge of CLKOUT<sup>+</sup>. The phase of CLKOUT<sup>+</sup> can also be delayed relative to the digital outputs by programming the mode control registers.

**DNC (Pin 35):** Do not connect this pin.

**OF (Pin 36):** Over/Under Flow Digital Output. OF is high when an overflow or underflow has occurred.

### DOUBLE DATA RATE CMOS OUTPUT MODE

All Pins Below Have CMOS Output Levels (OGND to  $OV_{DD}$ )

**D0\_1 to D12\_13 (Pins 18, 20, 22, 24, 30, 32, 34):** Double Data Rate Digital Outputs. Two data bits are multiplexed onto each output pin. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT<sup>+</sup> is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT<sup>+</sup> is high.

**CLKOUT<sup>-</sup> (Pin 27):** Inverted version of CLKOUT<sup>+</sup>.

**CLKOUT<sup>+</sup> (Pin 28):** Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT<sup>+</sup>. The phase of CLKOUT<sup>+</sup> can also be delayed relative to the digital outputs by programming the mode control registers.

**DNC (Pins 17, 19, 21, 23, 29, 31, 33, 35):** Do not connect these pins.

**OF (Pin 36):** Over/Under Flow Digital Output. OF is high when an overflow or underflow has occurred.

### DOUBLE DATA RATE LVDS OUTPUT MODE

All Pins Below Have LVDS Output Levels. The Output Current Level is Programmable. There is an Optional Internal 100 $\Omega$  Termination Resistor Between the Pins of Each LVDS Output Pair.

**D0\_1<sup>-</sup>/D0\_1<sup>+</sup> to D12\_13<sup>-</sup>/D12\_13<sup>+</sup> (Pins 17/18, 19/20, 21/22, 23/24, 29/30, 31/32, 33/34):** Double Data Rate Digital Outputs. Two data bits are multiplexed onto each differential output pair. The even data bits (D0, D2, D4, D6, D8, D10, D12) appear when CLKOUT<sup>+</sup> is low. The odd data bits (D1, D3, D5, D7, D9, D11, D13) appear when CLKOUT<sup>+</sup> is high.

**CLKOUT<sup>-</sup>/CLKOUT<sup>+</sup> (Pins 27/28):** Data Output Clock. The digital outputs normally transition at the same time as the falling and rising edges of CLKOUT<sup>+</sup>. The phase of CLKOUT<sup>+</sup> can also be delayed relative to the digital outputs by programming the mode control registers.

**OF<sup>-</sup>/OF<sup>+</sup> (Pins 35/36):** Over/Under Flow Digital Output. OF<sup>+</sup> is high when an overflow or underflow has occurred.

## FUNCTIONAL BLOCK DIAGRAM

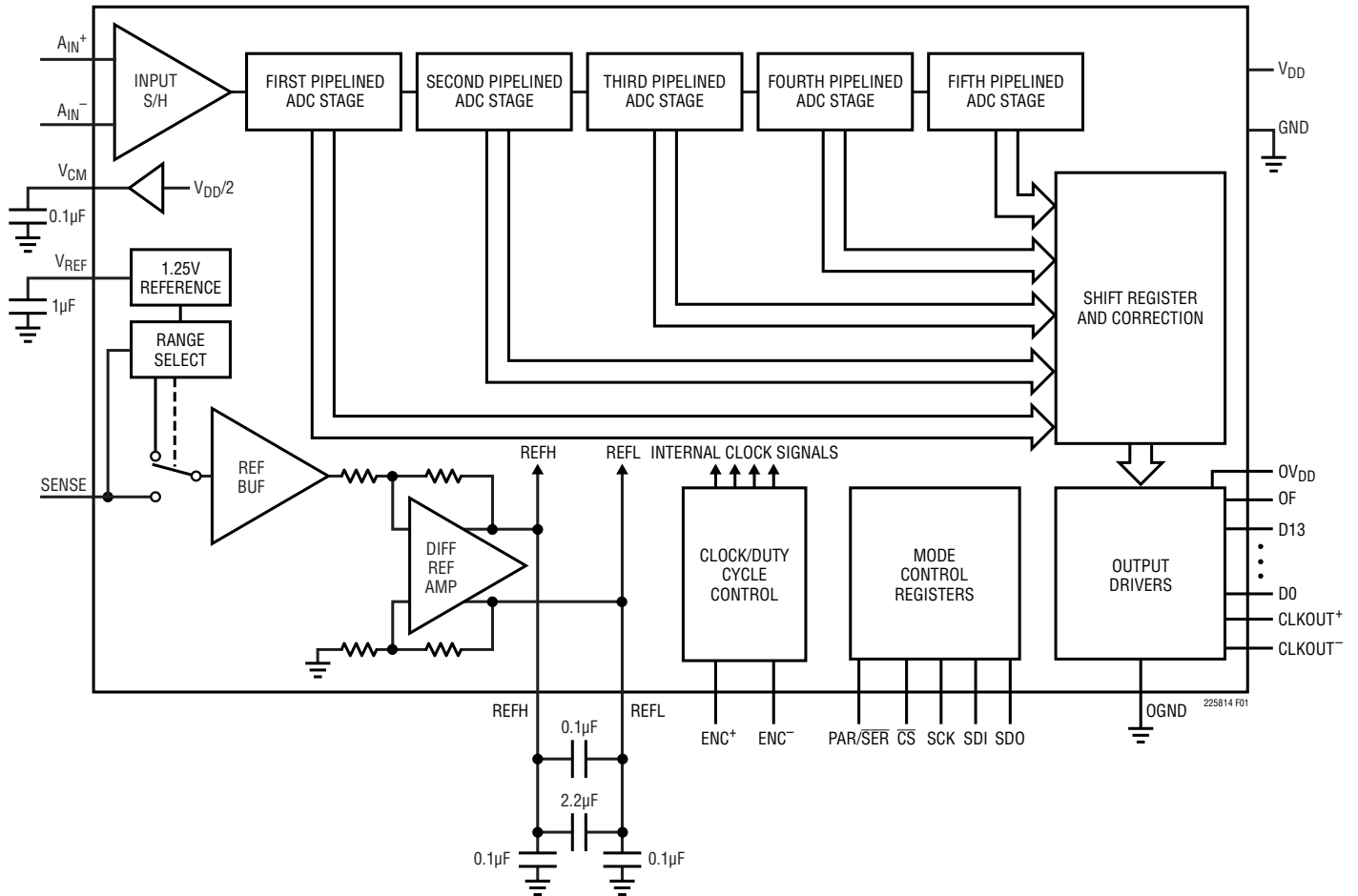


Figure 1. Functional Block Diagram



## APPLICATIONS INFORMATION

### CONVERTER OPERATION

The LTC2258-14/LTC2257-14/LTC2256-14 are low power 14-bit 65Msps/40Msps/25Msps A/D converters that are powered by a single 1.8V supply. The analog inputs should be driven differentially. The encode input can be driven differentially, or single ended for lower power consumption. The digital outputs can be CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system.) Many additional features can be chosen by programming the mode control registers through a serial SPI port. See the Serial Programming Mode section.

### ANALOG INPUT

The analog input is a differential CMOS sample-and-hold circuit (Figure 2). The inputs should be driven differentially around a common mode voltage set by the  $V_{CM}$  output pin, which is nominally  $V_{DD}/2$ . For the 2V input range, the inputs should swing from  $V_{CM} - 0.5V$  to  $V_{CM} + 0.5V$ . There should be  $180^\circ$  phase difference between the inputs.

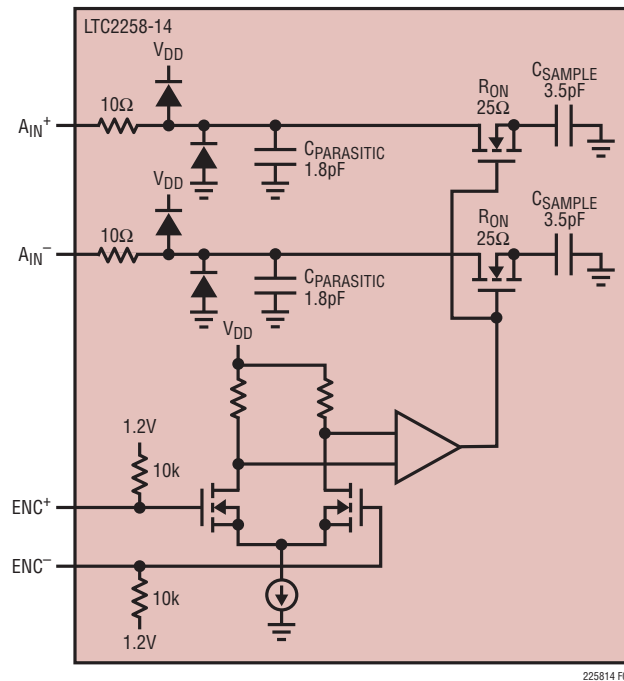


Figure 2. Equivalent Input Circuit

## APPLICATIONS INFORMATION

### INPUT DRIVE CIRCUITS

#### Input filtering

If possible, there should be an RC lowpass filter right at the analog inputs. This lowpass filter isolates the drive circuitry from the A/D sample-and-hold switching, and also limits wideband noise from the drive circuitry. Figure 3 shows an example of an input RC filter. The RC component values should be chosen based on the application's input frequency.

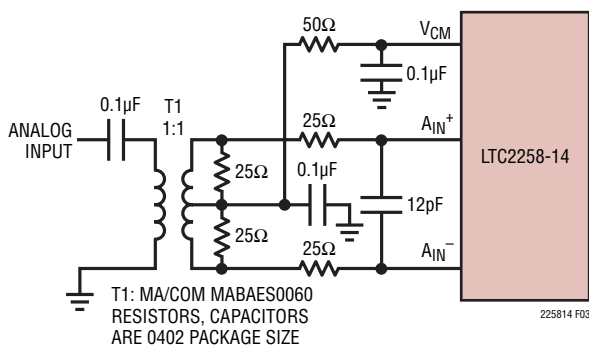


Figure 3. Analog Input Circuit Using a Transformer. Recommended for Input Frequencies from 5MHz to 70MHz

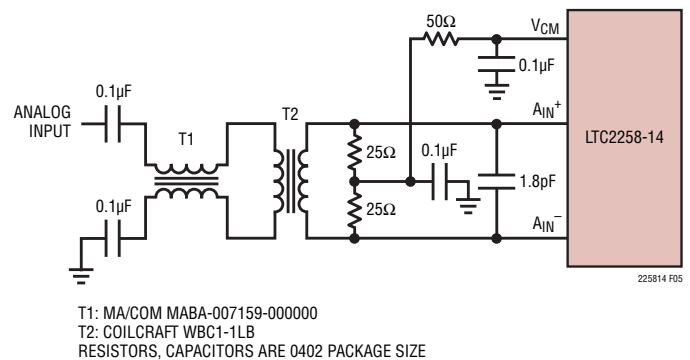


Figure 5. Recommended Front-End Circuit for Input Frequencies from 170MHz to 270MHz

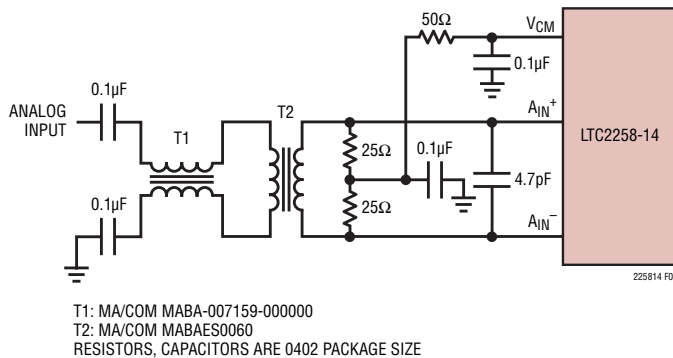


Figure 4. Recommended Front-End Circuit for Input Frequencies from 70MHz to 170MHz

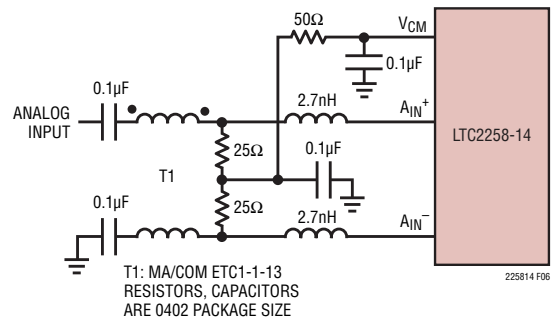


Figure 6. Recommended Front-End Circuit for Input Frequencies Above 270MHz

## APPLICATIONS INFORMATION

### Amplifier Circuits

Figure 7 shows the analog input being driven by a high speed differential amplifier. The output of the amplifier is AC coupled to the A/D so the amplifier's output common mode voltage can be optimally set to minimize distortion.

At very high frequencies an RF gain block will often have lower distortion than a differential amplifier. If the gain block is single-ended, then a transformer circuit (Figures 4 to 6) should convert the signal to differential before driving the A/D.

### Reference

The LTC2258-14/2257-14/2256-14 has an internal 1.25V voltage reference. For a 2V input range using the internal reference, connect SENSE to  $V_{DD}$ . For a 1V input range using the internal reference, connect SENSE to ground. For a 2V input range with an external reference, apply a 1.25V reference voltage to SENSE (Figure 9).

The input range can be adjusted by applying a voltage to SENSE that is between 0.625V and 1.30V. The input range will then be  $1.6 \cdot V_{SENSE}$ .

The  $V_{REF}$ , REFH and REFL pins should be bypassed as shown in Figure 8. The  $0.1\mu\text{F}$  capacitor between REFH and REFL should be as close to the pins as possible (not on the back side of the circuit board).

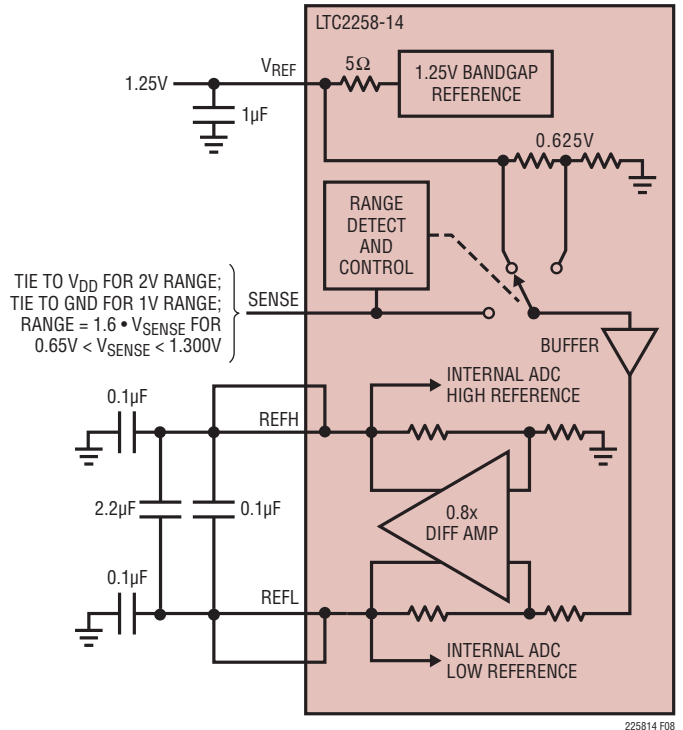


Figure 8. Reference Circuit

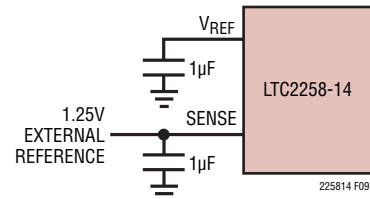


Figure 9. Using an External 1.25V Reference

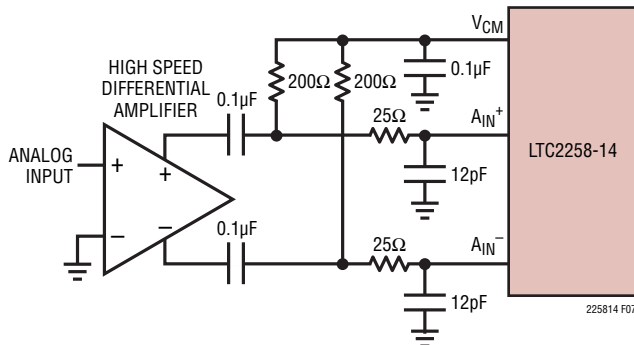


Figure 7. Front-End Circuit Using a High Speed Differential Amplifier

## APPLICATIONS INFORMATION

### Encode Input

The signal quality of the encode inputs strongly affects the A/D noise performance. The encode inputs should be treated as analog signals—do not route them next to digital traces on the circuit board. There are two modes of operation for the encode inputs: the differential encode mode (Figure 10) and the single-ended encode mode (Figure 11).

The differential encode mode is recommended for sinusoidal, PECL or LVDS encode inputs (Figures 12, 13). The encode inputs are internally biased to 1.2V through 10k equivalent resistance. The encode inputs can be taken above  $V_{DD}$  (up to 3.6V), and the common mode range is from 1.1V to 1.6V. In the differential encode mode,  $ENC^-$  should stay at least 200mV above ground to avoid falsely triggering the single-ended encode mode. For good jitter performance  $ENC^+$  and  $ENC^-$  should have fast rise and fall times.

The single-ended encode mode should be used with CMOS encode inputs. To select this mode,  $ENC^-$  is connected to ground and  $ENC^+$  is driven with a square wave encode input.  $ENC^+$  can be taken above  $V_{DD}$  (up to 3.6V) so 1.8V to 3.3V CMOS logic levels can be used. The  $ENC^+$  threshold is 0.9V. For good jitter performance  $ENC^+$  should have fast rise and fall times.

### Clock Duty Cycle Stabilizer

For good performance the encode signal should have a 50% ( $\pm 5\%$ ) duty cycle. If the optional clock duty cycle stabilizer circuit is enabled, the encode duty cycle can vary from 30% to 70% and the duty cycle stabilizer will maintain a constant 50% internal duty cycle. If the encode signal changes frequency or is turned off, the duty cycle stabilizer circuit requires one hundred clock cycles to lock onto the input clock. The duty cycle stabilizer is enabled

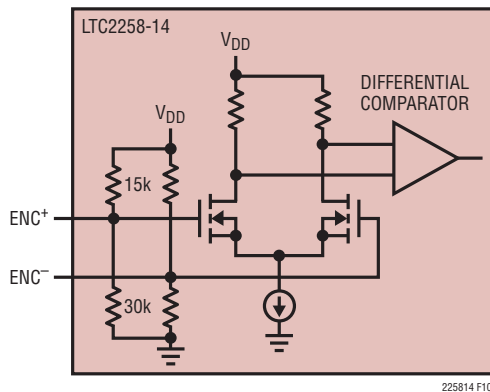


Figure 10. Equivalent Encode Input Circuit for Differential Encode Mode

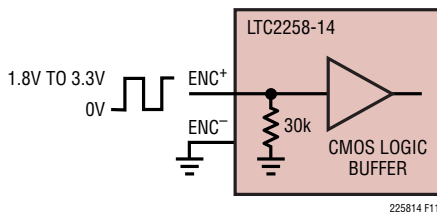


Figure 11. Equivalent Encode Input Circuit for Single-Ended Encode Mode

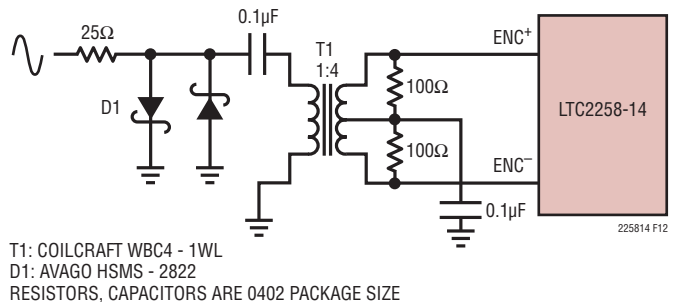


Figure 12. Sinusoidal Encode Drive

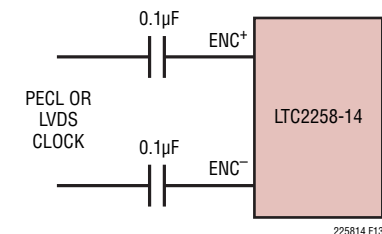


Figure 13. PECL or LVDS Encode Drive

## APPLICATIONS INFORMATION

by mode control register A2 (serial programming mode), or by  $\overline{CS}$  (parallel programming mode).

For applications where the sample rate needs to be changed quickly, the clock duty cycle stabilizer can be disabled. If the duty cycle stabilizer is disabled, care should be taken to make the sampling clock have a 50% ( $\pm 5\%$ ) duty cycle. The duty cycle stabilizer should not be used below 5MSPS.

### DIGITAL OUTPUTS

#### Digital Output Modes

The LTC2258-14/LTC2257-14/LTC2256-14 can operate in three digital output modes: full rate CMOS, double data rate CMOS (to halve the number of output lines), or double data rate LVDS (to reduce digital noise in the system). The output mode is set by mode control register A3 (serial programming mode), or by SCK (parallel programming mode). Note that double data rate CMOS cannot be selected in the parallel programming mode.

#### Full-Rate CMOS Mode

In full-rate CMOS mode the 14 digital outputs (D0-D13), overflow (OF), and the data output clocks (CLKOUT<sup>+</sup>, CLKOUT<sup>-</sup>) have CMOS output levels. The outputs are powered by  $OV_{DD}$  and OGND which are isolated from the A/D core power and ground.  $OV_{DD}$  can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance, the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

#### Double Data Rate CMOS Mode

In double data rate CMOS mode, two data bits are multiplexed and output on each data pin. This reduces the number of data lines by seven, simplifying board routing and reducing the number of input pins needed to receive the data. The 7 digital outputs (D0\_1, D2\_3, D4\_5, D6\_7, D8\_9, D10\_11, D12\_13), overflow (OF), and the data output clocks (CLKOUT<sup>+</sup>, CLKOUT<sup>-</sup>) have CMOS output levels. The outputs are powered by  $OV_{DD}$  and OGND which are isolated from the A/D core power and ground.  $OV_{DD}$  can range from 1.1V to 1.9V, allowing 1.2V through 1.8V CMOS logic outputs.

For good performance the digital outputs should drive minimal capacitive loads. If the load capacitance is larger than 10pF a digital buffer should be used.

#### Double Data Rate LVDS Mode

In double data rate LVDS mode, two data bits are multiplexed and output on each differential output pair. There are 7 LVDS output pairs (D0\_1<sup>+</sup>/D0\_1<sup>-</sup> through D12\_13<sup>+</sup>/D12\_13<sup>-</sup>) for the digital output data. Overflow (OF<sup>+</sup>/OF<sup>-</sup>) and the data output clock (CLKOUT<sup>+</sup>/CLKOUT<sup>-</sup>) each have an LVDS output pair.

By default the outputs are standard LVDS levels: 3.5mA output current and a 1.25V output common mode voltage. An external 100 $\Omega$  differential termination resistor is required for each LVDS output pair. The termination resistors should be located as close as possible to the LVDS receiver.

The outputs are powered by  $OV_{DD}$  and OGND which are isolated from the A/D core power and ground. In LVDS mode,  $OV_{DD}$  must be 1.8V.

#### Programmable LVDS Output Current

In LVDS mode, the default output driver current is 3.5mA. This current can be adjusted by serially programming mode control register A3. Available current levels are 1.75mA, 2.1mA, 2.5mA, 3mA, 3.5mA, 4mA and 4.5mA.

#### Optional LVDS Driver Internal Termination

In most cases using just an external 100 $\Omega$  termination resistor will give excellent LVDS signal integrity. In addition, an optional internal 100 $\Omega$  termination resistor can be enabled by serially programming mode control register A3. The internal termination helps absorb any reflections caused by imperfect termination at the receiver. When the internal termination is enabled, the output driver current is increased by 1.6x to maintain about the same output voltage swing.

#### Overflow Bit

The overflow output bit (OF) outputs a logic high when the analog input is either overranged or underranged. The overflow bit has the same pipeline latency as the data bits.



## APPLICATIONS INFORMATION

### Phase Shifting the Output Clock

In full-rate CMOS mode the data output bits normally change at the same time as the falling edge of CLKOUT<sup>+</sup>, so the rising edge of CLKOUT<sup>+</sup> can be used to latch the output data. In double data rate CMOS and LVDS modes the data output bits normally change at the same time as the falling and rising edges of CLKOUT<sup>+</sup>. To allow adequate setup-and-hold time when latching the data, the CLKOUT<sup>+</sup> signal may need to be phase shifted relative to the data output bits. Most FPGAs have this feature; this is generally the best place to adjust the timing.

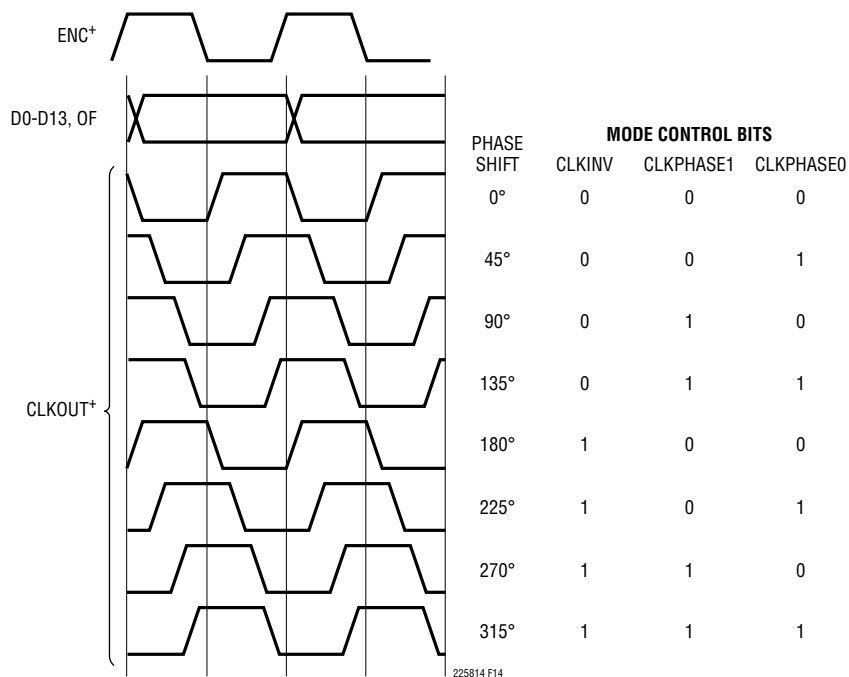
The LTC2258-14/LTC2257-14/LTC2256-14 can also phase shift the CLKOUT<sup>+</sup>/CLKOUT<sup>-</sup> signals by serially programming mode control register A2. The output clock can be shifted by 0°, 45°, 90° or 135°. To use the phase shifting feature the clock duty cycle stabilizer must be turned on. Another control register bit can invert the polarity of CLKOUT<sup>+</sup> and CLKOUT<sup>-</sup>, independently of the phase shift. The combination of these two features enables phase shifts of 45° up to 315° (Figure 14).

### DATA FORMAT

Table 1 shows the relationship between the analog input voltage, the digital data output bits and the overflow bit. By default the output data format is offset binary. The 2's complement format can be selected by serially programming mode control register A4.

**Table 1. Output Codes vs Input Voltage**

A <sub>IN</sub> <sup>+</sup> - A <sub>IN</sub> <sup>-</sup> (2V Range)	OF	D13-D0 (OFFSET BINARY)	D13-D0 (2's COMPLEMENT)
>1.000000V	1	11 1111 1111 1111	01 1111 1111 1111
+0.999878V	0	11 1111 1111 1111	01 1111 1111 1111
+0.999756V	0	11 1111 1111 1110	01 1111 1111 1110
+0.000122V	0	10 0000 0000 0001	00 0000 0000 0001
+0.000000V	0	10 0000 0000 0000	00 0000 0000 0000
-0.000122V	0	01 1111 1111 1111	11 1111 1111 1111
-0.000244V	0	01 1111 1111 1110	11 1111 1111 1110
-0.999878V	0	00 0000 0000 0001	10 0000 0000 0001
-1.000000V	0	00 0000 0000 0000	10 0000 0000 0000
≤-1.000000V	1	00 0000 0000 0000	10 0000 0000 0000



**Figure 14. Phase Shifting CLKOUT**

## APPLICATIONS INFORMATION

### Digital Output Randomizer

Interference from the A/D digital outputs is sometimes unavoidable. Digital interference may be from capacitive or inductive coupling or coupling through the ground plane. Even a tiny coupling factor can cause unwanted tones in the ADC output spectrum. By randomizing the digital output before it is transmitted off chip, these unwanted tones can be randomized which reduces the unwanted tone amplitude.

The digital output is “randomized” by applying an exclusive-OR logic operation between the LSB and all other data output bits. To decode, the reverse operation is applied—an exclusive-OR operation is applied between the LSB and all other bits. The LSB, OF and CLKOUT outputs are not affected. The output randomizer is enabled by serially programming mode control register A4.

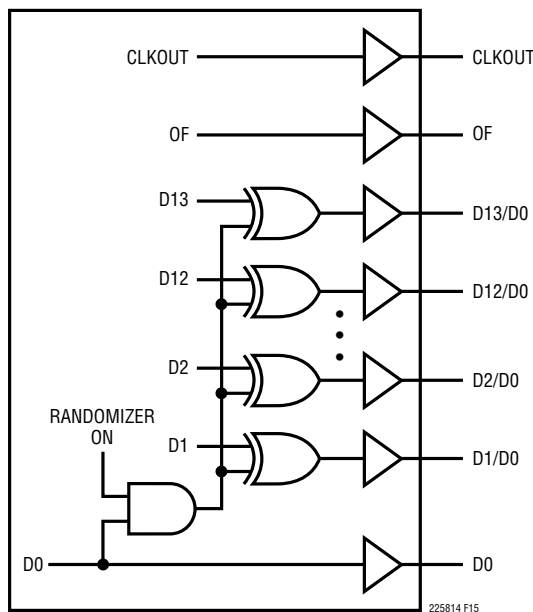


Figure 15. Functional Equivalent of Digital Output Randomizer

### Alternate Bit Polarity

Another feature that reduces digital feedback on the circuit board is the alternate bit polarity mode. When this mode is enabled, all of the odd bits (D1, D3, D5, D7, D9, D11, D13) are inverted before the output buffers. The even bits (D0, D2, D4, D6, D8, D10, D12), OF and CLKOUT are not affected. This can reduce digital currents in the circuit board ground plane and reduce digital noise, particularly for very small analog input signals.

When there is a very small signal at the input of the A/D that is centered around mid-scale, the digital outputs toggle between mostly 1s and mostly 0s. This simultaneous switching of most of the bits will cause large currents in the ground plane. By inverting every other bit, the alternate bit polarity mode makes half of the bits transition high while half of the bits transition low. To first order, this cancels current flow in the ground plane, reducing the digital noise.

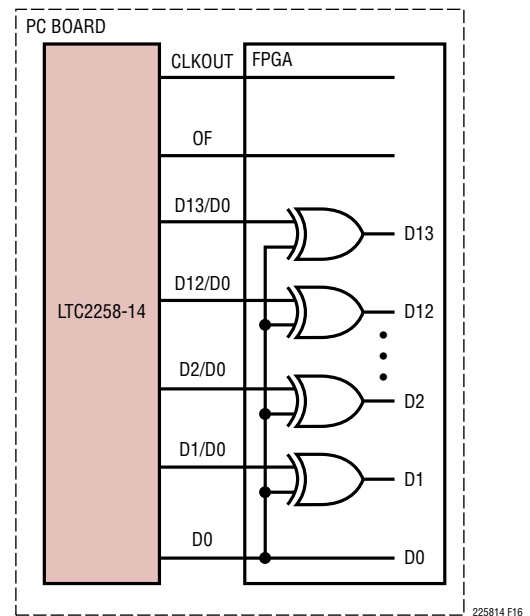


Figure 16. Unrandomizing a Randomized Digital Output Signal

## APPLICATIONS INFORMATION

The digital output is decoded at the receiver by inverting the odd bits (D1, D3, D5, D7, D9, D11, D13.) The alternate bit polarity mode is independent of the digital output randomizer—either, both or neither function can be on at the same time. When alternate bit polarity mode is on, the data format is offset binary and the 2's complement control bit has no effect. The alternate bit polarity mode is enabled by serially programming mode control register A4.

### Digital Output Test Patterns

To allow in-circuit testing of the digital interface to the A/D, there are several test modes that force the A/D data outputs (OF, D13-D0) to known values:

All 1s: All outputs are 1

All 0s: All outputs are 0

Alternating: Outputs change from all 1s to all 0s on alternating samples

Checkerboard: Outputs change from 10101010101010 to 01010101010101 on alternating samples

The digital output test patterns are enabled by serially programming mode control register A4. When enabled, the test patterns override all other formatting modes: 2's complement, randomizer, alternate-bit-polarity.

### Output Disable

The digital outputs may be disabled by serially programming mode control register A3. All digital outputs including OF and CLKOUT are disabled. The high impedance disabled state is intended for long periods of inactivity—it is too slow to multiplex a data bus between multiple converters at full speed.

### Sleep and Nap Modes

The A/D may be placed in sleep or nap modes to conserve power. In sleep mode the entire A/D converter is powered down, resulting in 0.5mW power consumption. Sleep mode is enabled by mode control register A1 (serial programming mode), or by SDI (parallel programming mode). The amount of time required to recover from sleep mode

depends on the size of the bypass capacitors on  $V_{REF}$ , REFH, and REFL. For the suggested values in Figure 8, the A/D will stabilize after 2ms.

In nap mode the A/D core is powered down while the internal reference circuits stay active, allowing faster wake-up than from sleep mode. Recovering from nap mode requires at least 100 clock cycles. If the application demands very accurate DC settling then an additional 50 $\mu$ s should be allowed so the on-chip references can settle from the slight temperature shift caused by the change in supply current as the A/D leaves nap mode. Nap mode is enabled by mode control register A1 in the serial programming mode.

## DEVICE PROGRAMMING MODES

The operating modes of the LTC2258-14/LTC2257-14/LTC2256-14 can be programmed by either a parallel interface or a simple serial interface. The serial interface has more flexibility and can program all available modes. The parallel interface is more limited and can only program some of the more commonly used modes.

### Parallel Programming Mode

To use the parallel programming mode,  $\overline{PAR/SER}$  should be tied to  $V_{DD}$ . The  $\overline{CS}$ , SCK and SDI pins are binary logic inputs that set certain operating modes. These pins can be tied to  $V_{DD}$  or ground, or driven by 1.8V, 2.5V or 3.3V CMOS logic. Table 2 shows the modes set by  $\overline{CS}$ , SCK and SDI.

**Table 2. Parallel Programming Mode Control Bits ( $\overline{PAR/SER} = V_{DD}$ )**

PIN	DESCRIPTION
$\overline{CS}$	Clock Duty Cycle Stabilizer Control Bit 0 = Clock Duty Cycle Stabilizer Off 1 = Clock Duty Cycle Stabilizer On
SCK	Digital Output Mode Control Bit 0 = Full-Rate CMOS Output Mode 1 = Double Data Rate LVDS Output Mode (3.5mA LVDS Current, Internal Termination Off)
SDI	Power Down Control Bit 0 = Normal Operation 1 = Sleep Mode