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# 16-Bit, 1MSPS 8-Channel Differential $\pm 10.24V$ Input SoftSpan ADC with Wide Input Common Mode Range

## FEATURES

- 1MSPS Throughput
- $\pm 1$ LSB INL (Maximum)
- Guaranteed 16-Bit, No Missing Codes
- Differential, Wide Common Mode Range Inputs
- 8-Channel Multiplexer with SoftSpan Input Ranges:
  - $\pm 10.24V$ , 0V to 10.24V,  $\pm 5.12V$ , 0V to 5.12V
  - $\pm 12.5V$ , 0V to 12.5V,  $\pm 6.25V$ , 0V to 6.25V
- 94.4dB Single-Conversion SNR (Typical)
- $-109$ dB THD (Typical) at  $f_{IN} = 2$ kHz
- 118dB CMRR, 125dB Active Crosstalk (Typical)
- Rail-to-Rail Input Overdrive Tolerance
- Programmable Sequencer with No-Latency Control
- Guaranteed Operation to 125°C
- Integrated Reference and Buffer (4.096V)
- SPI CMOS (1.8V to 5V) and LVDS Serial I/O
- No Pipeline Delay, No Cycle Latency
- 180mW Power Dissipation (Typical)
- 48-Lead (7mm  $\times$  7mm) LQFP Package

## APPLICATIONS

- Programmable Logic Controllers
- Industrial Process Control
- Power Line Monitoring
- Test and Measurement

## DESCRIPTION

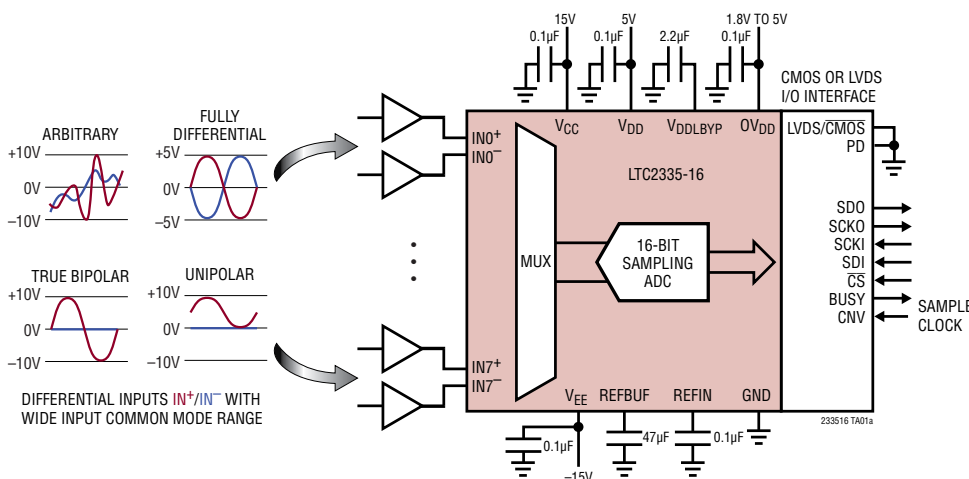
The LTC<sup>®</sup>2335-16 is a 16-bit, low noise 8-channel multiplexed successive approximation register (SAR) ADC with differential, wide common mode range inputs. Operating from a 5V low voltage supply, flexible high voltage supplies, and using the internal reference and buffer, this SoftSpan<sup>™</sup> ADC can be configured on a conversion-by-conversion basis to accept  $\pm 10.24V$ , 0V to 10.24V,  $\pm 5.12V$ , or 0V to 5.12V signals on any channel. Alternately, the ADC may be programmed to cycle through a sequence of channels and ranges without further user intervention.

The wide input common mode range and 118dB CMRR of the LTC2335-16 analog inputs allow the ADC to directly digitize a variety of signals, simplifying signal chain design. This input signal flexibility, combined with  $\pm 1$ LSB INL, no missing codes at 16 bits, and 94.4dB SNR, makes the LTC2335-16 an ideal choice for many high voltage applications requiring wide dynamic range.

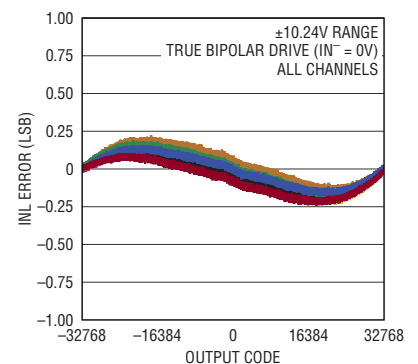
The LTC2335-16 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces.

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## TYPICAL APPLICATION



**Integral Nonlinearity vs Output Code and Channel**



233516f

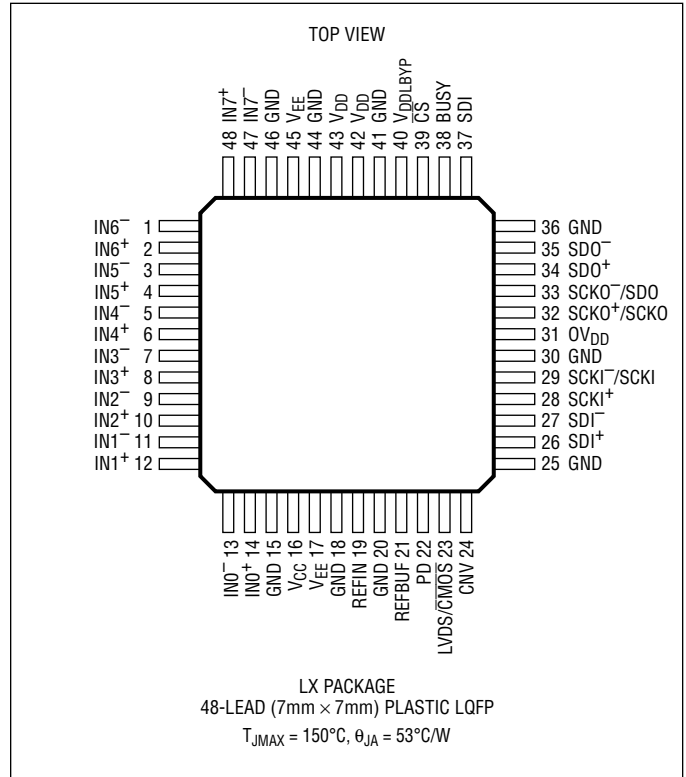
# LTC2335-16

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{CC}$ ) .....	-0.3V to ( $V_{EE} + 40V$ )
Supply Voltage ( $V_{EE}$ ).....	-17.4V to 0.3V
Supply Voltage Difference ( $V_{CC} - V_{EE}$ ).....	40V
Supply Voltage ( $V_{DD}$ ) .....	6V
Supply Voltage ( $OV_{DD}$ ).....	6V
Internal Regulated Supply Bypass ( $V_{DDLBY}$ ) ... (Note 3)	
Analog Input Voltage	
$IN0^+$ to $IN7^+$ ,	
$IN0^-$ to $IN7^-$ (Note 4) .....	( $V_{EE} - 0.3V$ ) to ( $V_{CC} + 0.3V$ )
REFIN.....	-0.3V to 2.8V
REFBUF, CNV (Note 5) .....	-0.3V to ( $V_{DD} + 0.3V$ )
Digital Input Voltage (Note 5).....	-0.3V to ( $OV_{DD} + 0.3V$ )
Digital Output Voltage (Note 5) ..	-0.3V to ( $OV_{DD} + 0.3V$ )
Power Dissipation .....	500mW
Operating Temperature Range	
LTC2335C .....	0°C to 70°C
LTC2335I .....	-40°C to 85°C
LTC2335H.....	-40°C to 125°C
Storage Temperature Range .....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

LEAD FREE FINISH	TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2335CLX-16#PBF	LTC2335CLX-16#PBF	LTC2335LX-16	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2335ILX-16#PBF	LTC2335ILX-16#PBF	LTC2335LX-16	48-Lead (7mm × 7mm) Plastic LQFP	-40°C to 85°C
LTC2335HLX-16#PBF	LTC2335HLX-16#PBF	LTC2335LX-16	48-Lead (7mm × 7mm) Plastic LQFP	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 6)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN+}$	Absolute Input Range (IN0+ to IN7+)	(Note 7)	●	$V_{EE}$		$V_{CC} - 4$	V
$V_{IN-}$	Absolute Input Range (IN0- to IN7-)	(Note 7)	●	$V_{EE}$		$V_{CC} - 4$	V
$V_{IN+} - V_{IN-}$	Input Differential Voltage Range	SoftSpan 7: $\pm 2.5 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 6: $\pm 2.5 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 5: 0V to $2.5 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 4: 0V to $2.5 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 3: $\pm 1.25 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 2: $\pm 1.25 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 1: 0V to $1.25 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 0: 0V to $1.25 \cdot V_{REFBUF}/1.024$ Range (Note 7)	● ● ● ● ● ● ● ●	$-2.5 \cdot V_{REFBUF}$ $-2.5 \cdot V_{REFBUF}/1.024$ 0 0 $-1.25 \cdot V_{REFBUF}$ $-1.25 \cdot V_{REFBUF}/1.024$ 0 0		$2.5 \cdot V_{REFBUF}$ $2.5 \cdot V_{REFBUF}/1.024$ $2.5 \cdot V_{REFBUF}$ $2.5 \cdot V_{REFBUF}/1.024$ $1.25 \cdot V_{REFBUF}$ $1.25 \cdot V_{REFBUF}/1.024$ $1.25 \cdot V_{REFBUF}$ $1.25 \cdot V_{REFBUF}/1.024$	V V V V V V V V
$V_{CM}$	Input Common Mode Voltage Range	(Note 7)	●	$V_{EE}$		$V_{CC} - 4$	V
$V_{IN+} - V_{IN-}$	Input Differential Overdrive Tolerance	(Note 8)	●	$-(V_{CC} - V_{EE})$		$(V_{CC} - V_{EE})$	V
$I_{IN}$	Analog Input Leakage Current		●	-1		1	$\mu\text{A}$
$C_{IN}$	Analog Input Capacitance	Sample Mode Hold Mode			50 10		pF pF
CMRR	Input Common Mode Rejection Ratio	$V_{IN+} = V_{IN-} = 18\text{V}_{p-p}$ 200Hz Sine	●	100	118		dB
$V_{IHCNV}$	CNV High Level Input Voltage		●	1.3			V
$V_{ILCNV}$	CNV Low Level Input Voltage		●			0.5	V
$I_{INCNV}$	CNV Input Current	$V_{IN} = 0\text{V}$ to $V_{DD}$	●	-10		10	$\mu\text{A}$

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	16			Bits
	No Missing Codes		●	16			Bits
	Transition Noise	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges SoftSpans 5 and 4: 0V to $10.24\text{V}$ and 0V to $10\text{V}$ Ranges SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges SoftSpans 1 and 0: 0V to $5.12\text{V}$ and 0V to $5\text{V}$ Ranges			0.33 0.65 0.5 1.0		$\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$
INL	Integral Linearity Error	(Note 10)	●	-1	$\pm 0.3$	1	LSB
DNL	Differential Linearity Error	(Note 11)	●	-0.9	$\pm 0.2$	0.9	LSB
ZSE	Zero-Scale Error	(Note 12)	●	-550	$\pm 160$	550	$\mu\text{V}$
	Zero-Scale Error Drift				$\pm 2$		$\mu\text{V}/^\circ\text{C}$
FSE	Full-Scale Error	(Note 12)	●	-0.1	$\pm 0.025$	0.1	%FS
	Full-Scale Error Drift				$\pm 2.5$		ppm/ $^\circ\text{C}$

## DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{IN} = -1\text{dBFS}$ . (Notes 9, 13)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
SINAD	Signal-to-(Noise + Distortion) Ratio	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	91.8	94.3		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	87.2	90.1		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	89.3	92.0		dB
		SoftSpans 1 and 0: $0\text{V}$ to $5.12\text{V}$ and $0\text{V}$ to $5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	83.8	87.0		dB
SNR	Signal-to-Noise Ratio	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	92.3	94.4		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	87.3	90.1		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	89.5	92.0		dB
		SoftSpans 1 and 0: $0\text{V}$ to $5.12\text{V}$ and $0\text{V}$ to $5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	83.8	87.0		dB
THD	Total Harmonic Distortion	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●		-109	-101	dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●		-111	-99	dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●		-113	-104	dB
		SoftSpans 1 and 0: $0\text{V}$ to $5.12\text{V}$ and $0\text{V}$ to $5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●		-114	-103	dB
SFDR	Spurious Free Dynamic Range	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	101	110		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	99	112		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	105	114		dB
		SoftSpans 1 and 0: $0\text{V}$ to $5.12\text{V}$ and $0\text{V}$ to $5\text{V}$ Ranges, $f_{IN} = 2\text{kHz}$	●	105	115		dB
	Channel-to-Channel Active Crosstalk	Alternating Conversions with $18\text{V}_{\text{P-P}}$ $200\text{Hz}$ Sine in $\pm 10.24\text{V}$ Range, Crosstalk to Any Other Channel			-125	dB	
	-3dB Input Bandwidth			7		MHz	
	Aperture Delay			1		ns	
	Aperture Delay Matching			150		ps	
	Aperture Jitter			3		ps <sub>RMS</sub>	
	Transient Response	Full-Scale Step, 0.005% Settling		360		ns	

## INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{\text{REFIN}}$	Internal Reference Output Voltage		2.043	2.048	2.053	V	
	Internal Reference Temperature Coefficient	(Note 14)		●	5	20	ppm/ $^\circ\text{C}$
	Internal Reference Line Regulation	$V_{\text{DD}} = 4.75\text{V}$ to $5.25\text{V}$			0.1	mV/V	
	Internal Reference Output Impedance				20	k $\Omega$	
$V_{\text{REFIN}}$	REFIN Voltage Range	REFIN Overdriven (Note 7)	1.25		2.2	V	

## REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{REFBUF}}$	Reference Buffer Output Voltage	REFIN Overdriven, $V_{\text{REFIN}} = 2.048\text{V}$	● 4.091	4.096	4.101	V
	REFBUF Voltage Range	REFBUF Overdriven (Notes 7, 15)	● 2.5		5	V
	REFBUF Input Impedance	$V_{\text{REFIN}} = 0\text{V}$ , Buffer Disabled		13		k $\Omega$
$I_{\text{REFBUF}}$	REFBUF Load Current	$V_{\text{REFBUF}} = 5\text{V}$ , (Notes 15, 16) $V_{\text{REFBUF}} = 5\text{V}$ , Acquisition or Nap Mode (Note 15)	●	1.1 0.39	1.4	mA mA

## DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
<b>CMOS Digital Inputs and Outputs</b>						
$V_{\text{IH}}$	High Level Input Voltage		● $0.8 \cdot OV_{\text{DD}}$			V
$V_{\text{IL}}$	Low Level Input Voltage		●		$0.2 \cdot OV_{\text{DD}}$	V
$I_{\text{IN}}$	Digital Input Current	$V_{\text{IN}} = 0\text{V}$ to $OV_{\text{DD}}$	● -10		10	$\mu\text{A}$
$C_{\text{IN}}$	Digital Input Capacitance			5		pF
$V_{\text{OH}}$	High Level Output Voltage	$I_{\text{OUT}} = -500\mu\text{A}$	● $OV_{\text{DD}} - 0.2$			V
$V_{\text{OL}}$	Low Level Output Voltage	$I_{\text{OUT}} = 500\mu\text{A}$	●		0.2	V
$I_{\text{OZ}}$	Hi-Z Output Leakage Current	$V_{\text{OUT}} = 0\text{V}$ to $OV_{\text{DD}}$	● -10		10	$\mu\text{A}$
$I_{\text{SOURCE}}$	Output Source Current	$V_{\text{OUT}} = 0\text{V}$		-50		mA
$I_{\text{SINK}}$	Output Sink Current	$V_{\text{OUT}} = OV_{\text{DD}}$		50		mA
<b>LVDS Digital Inputs and Outputs</b>						
$V_{\text{ID}}$	Differential Input Voltage		● 200	350	600	mV
$R_{\text{ID}}$	On-Chip Input Termination Resistance	$\overline{\text{CS}} = 0\text{V}$ , $V_{\text{ICM}} = 1.2\text{V}$ $\overline{\text{CS}} = OV_{\text{DD}}$	● 90	106 10	125	$\Omega$ M $\Omega$
$V_{\text{ICM}}$	Common-Mode Input Voltage		● 0.3	1.2	2.2	V
$I_{\text{ICM}}$	Common-Mode Input Current	$V_{\text{IN}+} = V_{\text{IN}-} = 0\text{V}$ to $OV_{\text{DD}}$	● -10		10	$\mu\text{A}$
$V_{\text{OD}}$	Differential Output Voltage	$R_{\text{L}} = 100\Omega$ Differential Termination	● 275	350	425	mV
$V_{\text{OCM}}$	Common-Mode Output Voltage	$R_{\text{L}} = 100\Omega$ Differential Termination	● 1.1	1.2	1.3	V
$I_{\text{OZ}}$	Hi-Z Output Leakage Current	$V_{\text{OUT}} = 0\text{V}$ to $OV_{\text{DD}}$	● -10		10	$\mu\text{A}$

## POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage		●	0		38	V
$V_{EE}$	Supply Voltage		●	-16.5		0	V
$V_{CC} - V_{EE}$	Supply Voltage Difference		●	10		38	V
$V_{DD}$	Supply Voltage		●	4.75	5.00	5.25	V
$I_{VCC}$	Supply Current	1Msps Sample Rate	●		3.5	4.3	mA
		Acquisition Mode	●		3.8	4.5	mA
		Nap Mode	●		0.7	0.9	mA
		Power Down Mode	●		1	15	$\mu\text{A}$
$I_{VEE}$	Supply Current	1Msps Sample Rate	●	-5.1	-4.0		mA
		Acquisition Mode	●	-4.9	-4.0		mA
		Nap Mode	●	-1.1	-0.8		mA
		Power Down Mode	●	-15	-1		$\mu\text{A}$

### CMOS I/O Mode

$OV_{DD}$	Supply Voltage		●	1.71		5.25	V
$I_{VDD}$	Supply Current	1Msps Sample Rate	●		12.6	14.5	mA
		1Msps Sample Rate, $V_{REFBUF} = 5V$ (Note 15)	●		11.3	13.0	mA
		Acquisition Mode	●		1.6	2.1	mA
		Nap Mode	●		1.4	1.9	mA
		Power Down Mode (C-Grade and I-Grade)	●		65	175	$\mu\text{A}$
$I_{OVDD}$	Supply Current	1Msps Sample Rate ( $C_L = 25\text{pF}$ )	●		2.6	4.2	mA
		Acquisition or Nap Mode	●		1	20	$\mu\text{A}$
		Power Down Mode	●		1	20	$\mu\text{A}$
$P_D$	Power Dissipation	1Msps Sample Rate	●		182	224	mW
		Acquisition Mode	●		125	152	mW
		Nap Mode	●		30	40	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.36	1.4	mW
		Power Down Mode (H-Grade)	●		0.36	2.8	mW

### LVDS I/O Mode

$OV_{DD}$	Supply Voltage		●	2.375		5.25	V
$I_{VDD}$	Supply Current	1Msps Sample Rate	●		14.8	17.1	mA
		1Msps Sample Rate, $V_{REFBUF} = 5V$ (Note 15)	●		13.8	15.9	mA
		Acquisition Mode	●		3.2	3.8	mA
		Nap Mode	●		3.0	3.7	mA
		Power Down Mode (C-Grade and I-Grade)	●		65	175	$\mu\text{A}$
$I_{OVDD}$	Supply Current	1Msps Sample Rate, ( $R_L = 100\Omega$ )	●		7	8.5	mA
		Acquisition or Nap Mode ( $R_L = 100\Omega$ )	●		7	8.0	mA
		Power Down Mode	●		1	20	$\mu\text{A}$
$P_D$	Power Dissipation	1Msps Sample Rate	●		204	248	mW
		Acquisition Mode	●		151	180	mW
		Nap Mode	●		55	69	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.36	1.4	mW
		Power Down Mode (H-Grade)	●		0.36	2.8	mW

## ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$f_{\text{SMPL}}$	Maximum Sampling Frequency		●		1	MSPS	
$t_{\text{CYC}}$	Time Between Conversions		●	1		$\mu\text{s}$	
$t_{\text{CONV}}$	Conversion Time		●	450	500	550	ns
$t_{\text{ACQ}}$	Acquisition Time	$(t_{\text{ACQ}} = t_{\text{CYC}} - t_{\text{CONV}} - t_{\text{BUSY}})$	●	420	480		ns
$t_{\text{CNVH}}$	CNV High Time		●	40			ns
$t_{\text{CNVL}}$	CNV Low Time		●	420			ns
$t_{\text{BUSY}}^{\text{LH}}$	CNV $\uparrow$ to BUSY Delay	$C_L = 25\text{pF}$	●		30		ns
$t_{\text{QUIET}}$	Digital I/O Quiet Time from CNV $\uparrow$		●	20			ns
$t_{\text{PDH}}$	PD High Time		●	40			ns
$t_{\text{PDL}}$	PD Low Time		●	40			ns
$t_{\text{WAKE}}$	REFBUF Wake-Up Time	$C_{\text{REFBUF}} = 47\mu\text{F}$ , $C_{\text{REFIN}} = 0.1\mu\text{F}$			200		ms

### CMOS I/O Mode

$t_{\text{SCKI}}$	SCKI Period	(Notes 17, 18)	●	10			ns
$t_{\text{SCKIH}}$	SCKI High Time		●	4			ns
$t_{\text{SCKIL}}$	SCKI Low Time		●	4			ns
$t_{\text{SSDISCKI}}$	SDI Setup Time from SCKI $\uparrow$	(Note 17)	●	2			ns
$t_{\text{HSDISCKI}}$	SDI Hold Time from SCKI $\uparrow$	(Note 17)	●	1			ns
$t_{\text{DSDOSCKI}}$	SDO Data Valid Delay from SCKI $\uparrow$	$C_L = 25\text{pF}$ (Note 17)	●			7.5	ns
$t_{\text{HSDOSCKI}}$	SDO Remains Valid Delay from SCKI $\uparrow$	$C_L = 25\text{pF}$ (Note 17)	●	1.5			ns
$t_{\text{SKEW}}$	SDO to SCKO Skew	(Note 17)	●	-1	0	1	ns
$t_{\text{DSDOBUSYL}}$	SDO Data Valid Delay from BUSY $\downarrow$	$C_L = 25\text{pF}$ (Note 17)	●	0			ns
$t_{\text{EN}}$	Bus Enable Time After $\overline{\text{CS}}\downarrow$	(Note 17)	●			15	ns
$t_{\text{DIS}}$	Bus Relinquish Time After $\overline{\text{CS}}\uparrow$	(Note 17)	●			15	ns

### LVDS I/O Mode

$t_{\text{SCKI}}$	SCKI Period	(Note 19)	●	4			ns
$t_{\text{SCKIH}}$	SCKI High Time	(Note 19)	●	1.5			ns
$t_{\text{SCKIL}}$	SCKI Low Time	(Note 19)	●	1.5			ns
$t_{\text{SSDISCKI}}$	SDI Setup Time from SCKI	(Notes 11, 19)	●	1.2			ns
$t_{\text{HSDISCKI}}$	SDI Hold Time from SCKI	(Notes 11, 19)	●	-0.2			ns
$t_{\text{DSDOSCKI}}$	SDO Data Valid Delay from SCKI	(Notes 11, 19)	●			6	ns
$t_{\text{HSDOSCKI}}$	SDO Remains Valid Delay from SCKI	(Notes 11, 19)	●	1			ns
$t_{\text{SKEW}}$	SDO to SCKO Skew	(Note 11)	●	-0.4	0	0.4	ns
$t_{\text{DSDOBUSYL}}$	SDO Data Valid Delay from BUSY $\downarrow$	(Note 11)	●	0			ns
$t_{\text{EN}}$	Bus Enable Time After $\overline{\text{CS}}\downarrow$		●			50	ns
$t_{\text{DIS}}$	Bus Relinquish Time After $\overline{\text{CS}}\uparrow$		●			15	ns



## ADC TIMING CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to ground.

**Note 3:**  $V_{DDLBY}$  is the output of an internal voltage regulator, and should only be connected to a 2.2 $\mu$ F ceramic capacitor to bypass the pin to GND, as described in the Pin Functions section. Do not connect this pin to any external circuitry.

**Note 4:** When these pin voltages are taken below  $V_{EE}$  or above  $V_{CC}$ , they will be clamped by internal diodes. This product can handle input currents of up to 100mA below  $V_{EE}$  or above  $V_{CC}$  without latch-up.

**Note 5:** When these pin voltages are taken below ground or above  $V_{DD}$  or  $OV_{DD}$ , they will be clamped by internal diodes. This product can handle currents of up to 100mA below ground or above  $V_{DD}$  or  $OV_{DD}$  without latch-up.

**Note 6:**  $-16.5V \leq V_{EE} \leq 0V$ ,  $0V \leq V_{CC} \leq 38V$ ,  $10V \leq (V_{CC} - V_{EE}) \leq 38V$ ,  $V_{DD} = 5V$ , unless otherwise specified.

**Note 7:** Recommended operating conditions.

**Note 8:** Refer to Absolute Maximum Ratings section for pin voltage limits related to device reliability.

**Note 9:**  $V_{CC} = 15V$ ,  $V_{EE} = -15V$ ,  $V_{DD} = 5V$ ,  $OV_{DD} = 2.5V$ ,  $f_{SAMPL} = 1M$ sp/s, internal reference and buffer, true bipolar input signal drive in bipolar SoftSpan ranges, unipolar signal drive in unipolar SoftSpan ranges, unless otherwise specified.

**Note 10:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 11:** Guaranteed by design, not subject to test.

**Note 12:** For bipolar SoftSpan ranges 7, 6, 3, and 2, zero-scale error is the offset voltage measured from  $-0.5LSB$  when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Full-scale error for these SoftSpan ranges is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. For unipolar SoftSpan ranges 5, 4, 1, and 0, zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001. Full-scale error for these SoftSpan ranges is the worst-case deviation of the last code transition from ideal and includes the effect of offset error.

**Note 13:** All specifications in dB are referred to a full-scale input in the relevant SoftSpan input range, except for crosstalk, which is referred to the crosstalk injection signal amplitude.

**Note 14:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

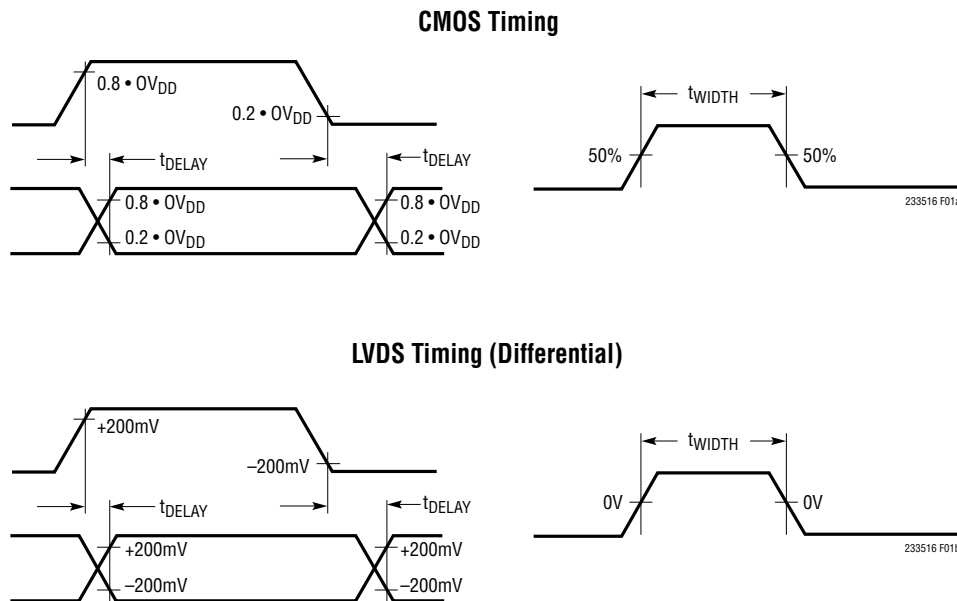
**Note 15:** When REFBUF is overdriven, the internal reference buffer must be disabled by setting REFIN = 0V.

**Note 16:**  $I_{REFBUF}$  varies proportionally with sample rate.

**Note 17:** Parameter tested and guaranteed at  $OV_{DD} = 1.71V$ ,  $OV_{DD} = 2.5V$ , and  $OV_{DD} = 5.25V$ .

**Note 18:** A  $t_{SCKI}$  period of 10ns minimum allows a shift clock frequency of up to 100MHz for rising edge capture.

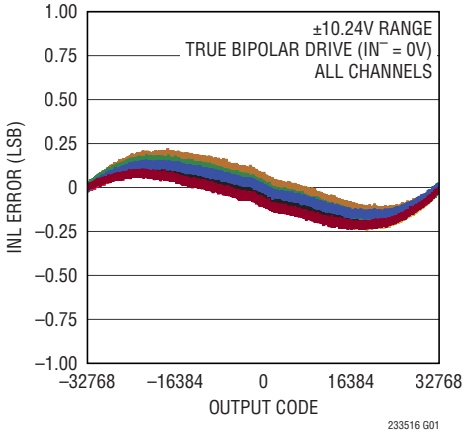
**Note 19:**  $V_{ICM} = 1.2V$ ,  $V_{ID} = 350mV$  for LVDS differential input pairs.



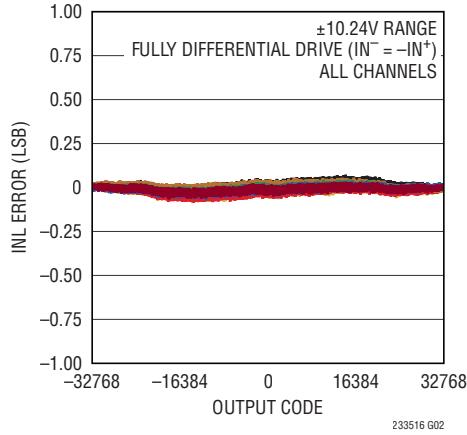
**Figure 1. Voltage Levels for Timing Specifications**

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ),  $f_{SAMPL} = 1\text{Mpsps}$ , unless otherwise noted.

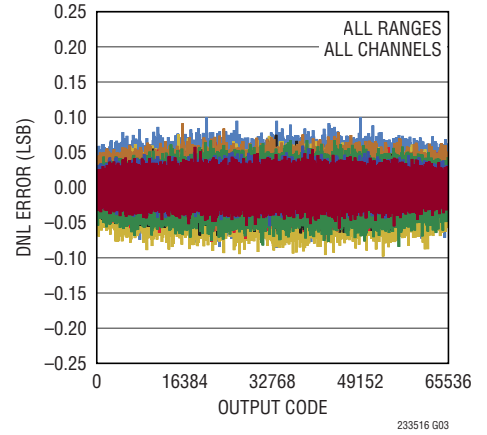
**Integral Nonlinearity vs Output Code and Channel**



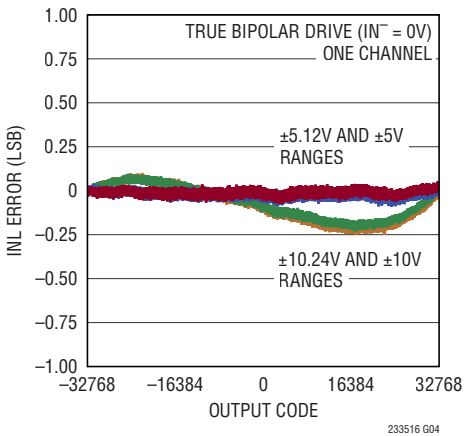
**Integral Nonlinearity vs Output Code and Channel**



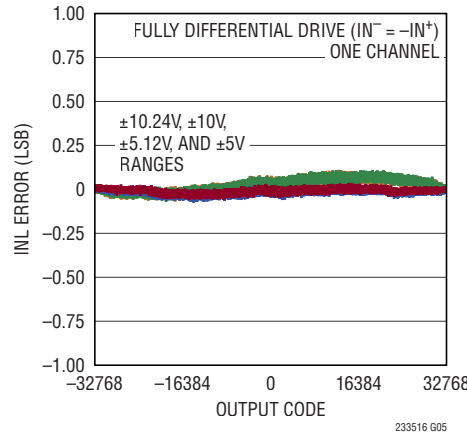
**Differential Nonlinearity vs Output Code and Range**



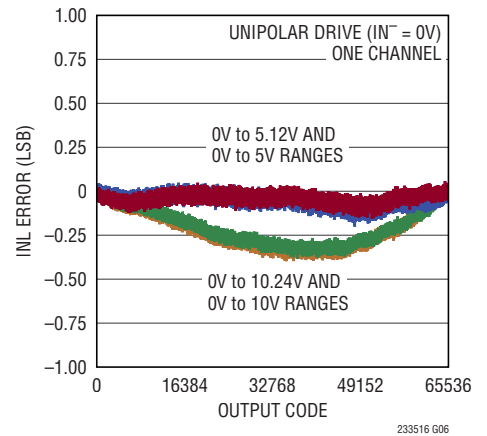
**Integral Nonlinearity vs Output Code and Range**



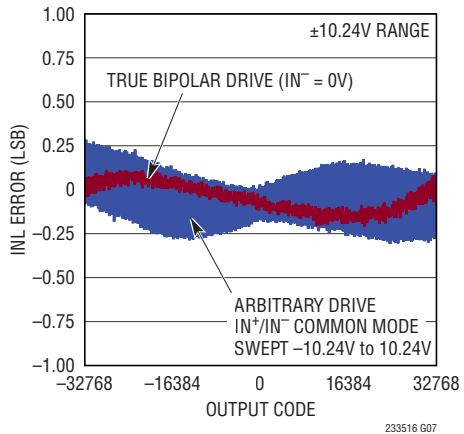
**Integral Nonlinearity vs Output Code and Range**



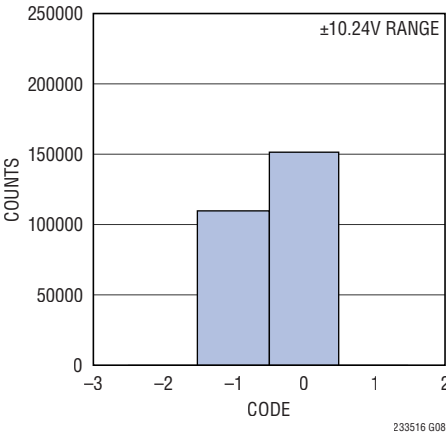
**Integral Nonlinearity vs Output Code and Range**



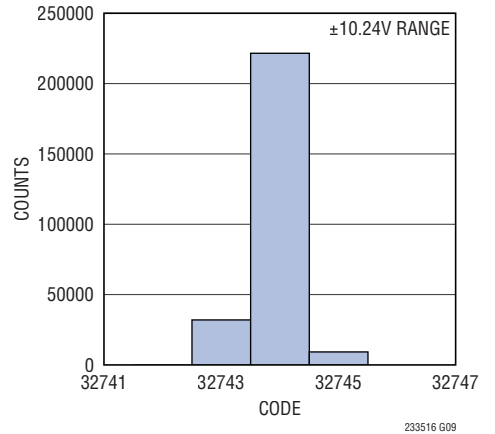
**Integral Nonlinearity vs Output Code**



**DC Histogram (Zero-Scale)**

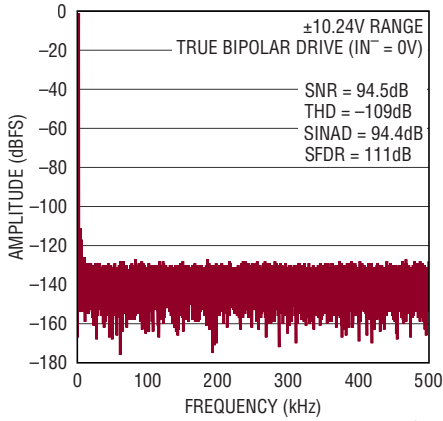


**DC Histogram (Near Full-Scale)**



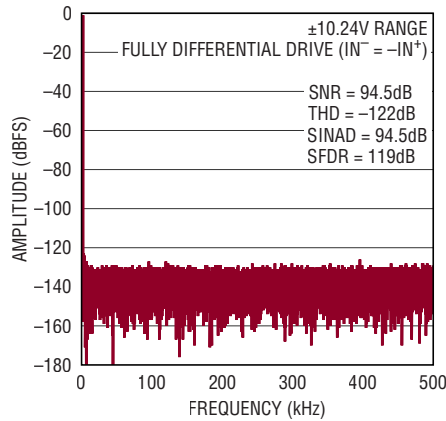
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{CC} = +15\text{V}$ , $V_{EE} = -15\text{V}$ , $V_{DD} = 5\text{V}$ , $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ), $f_{SMPL} = 1\text{Mpsps}$ , unless otherwise noted.

**32k Point FFT  $f_{SMPL} = 1\text{Mpsps}$ ,  $f_{IN} = 2\text{kHz}$**



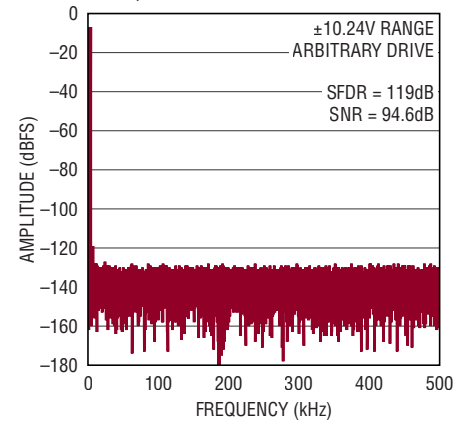
233516 G10

**32k Point FFT  $f_{SMPL} = 1\text{Mpsps}$ ,  $f_{IN} = 2\text{kHz}$**



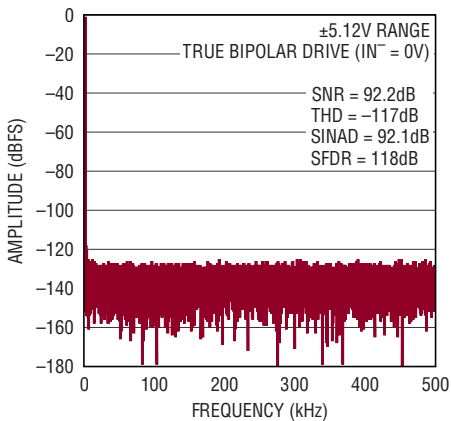
233516 G11

**32k Point Arbitrary Two-Tone FFT  $f_{SMPL} = 1\text{Mpsps}$ ,  $IN^+ = -7\text{dBFS}$  2kHz Sine,  $IN^- = -7\text{dBFS}$  3.1kHz Sine**



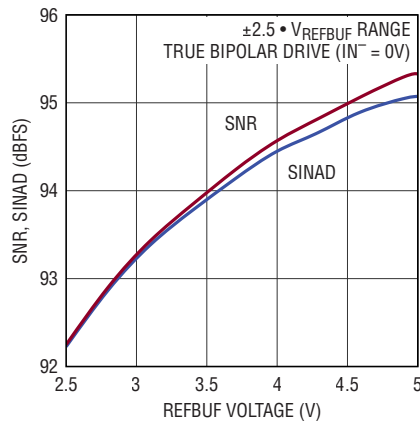
233516 G12

**32k Point FFT  $f_{SMPL} = 1\text{Mpsps}$ ,  $f_{IN} = 2\text{kHz}$**



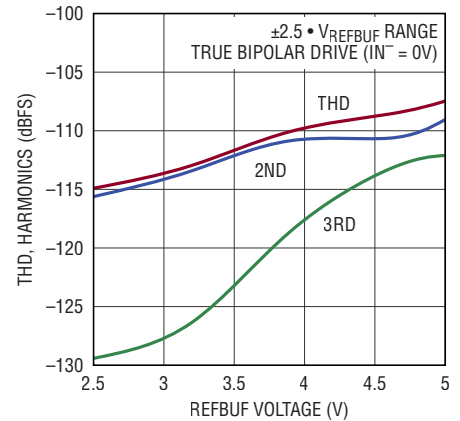
233516 G13

**SNR, SINAD vs  $V_{REFBUF}$ ,  $f_{IN} = 2\text{kHz}$**



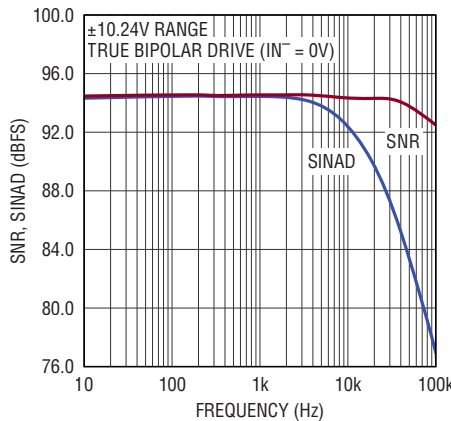
233516 G14

**THD, Harmonics vs  $V_{REFBUF}$ ,  $f_{IN} = 2\text{kHz}$**



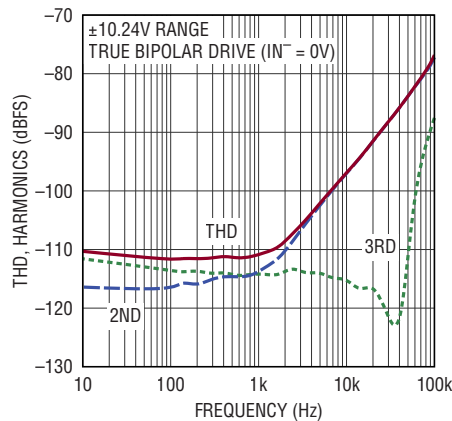
233516 G15

**SNR, SINAD vs Input Frequency**



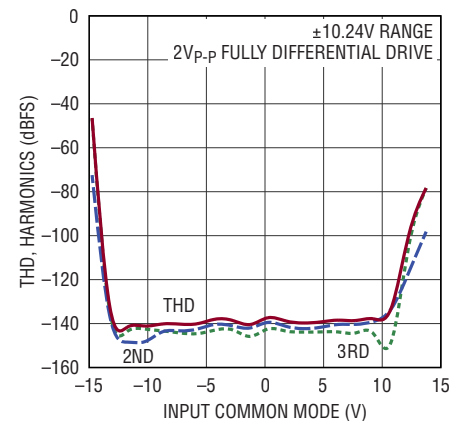
233516 G16

**THD, Harmonics vs Input Frequency**



233516 G17

**THD, Harmonics vs Input Common Mode,  $f_{IN} = 2\text{kHz}$**

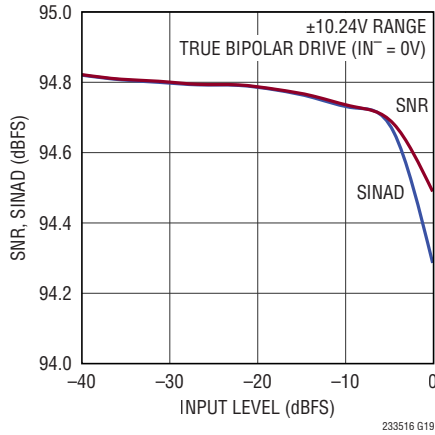


233516 G18

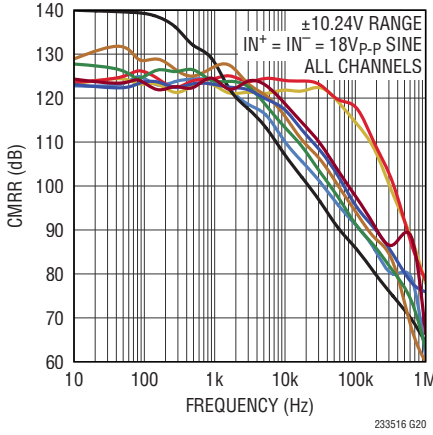
233516f

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ),  $f_{SAMPL} = 1\text{Mpsps}$ , unless otherwise noted.

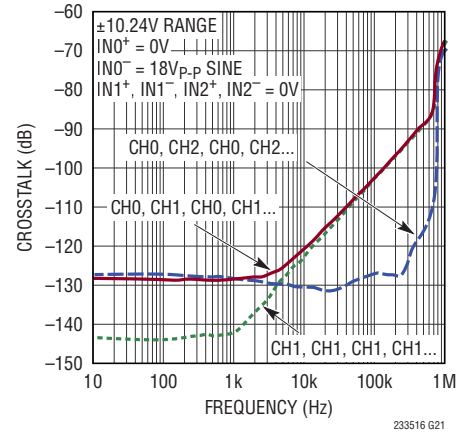
**SNR, SINAD vs Input Level,**  
 $f_{IN} = 2\text{kHz}$



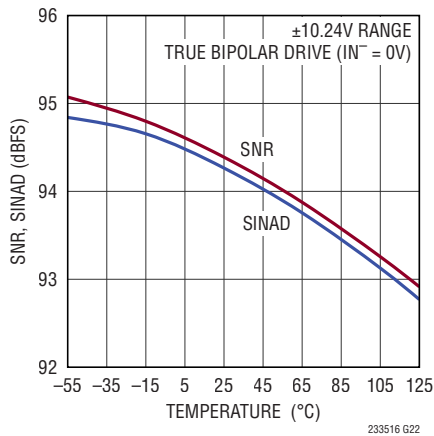
**CMRR vs Input Frequency and Channel**



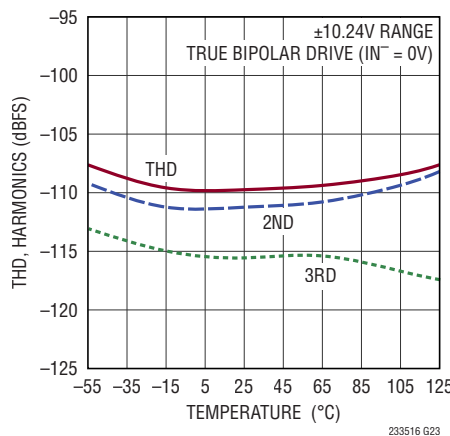
**Crosstalk vs Input Frequency and Conversion Sequence**



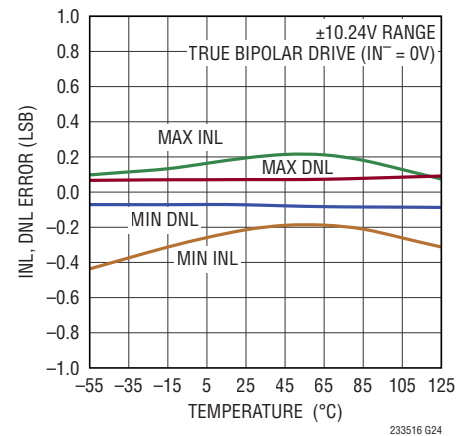
**SNR, SINAD vs Temperature,**  
 $f_{IN} = 2\text{kHz}$



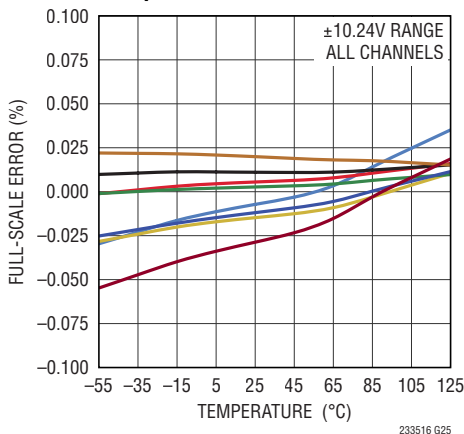
**THD, Harmonics vs Temperature,**  
 $f_{IN} = 2\text{kHz}$



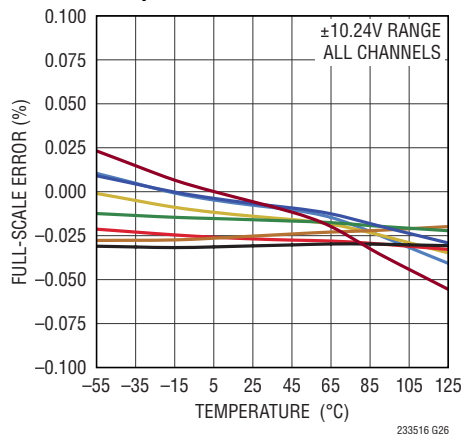
**INL, DNL vs Temperature**



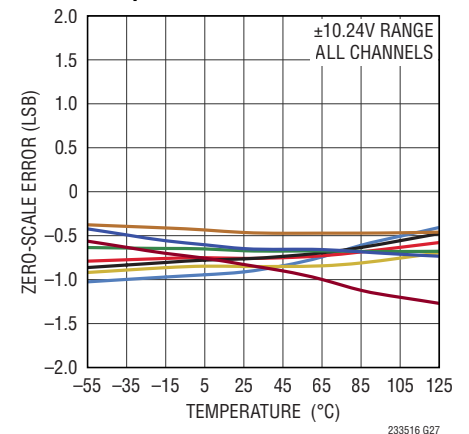
**Positive Full-Scale Error vs Temperature and Channel**



**Negative Full-Scale Error vs Temperature and Channel**

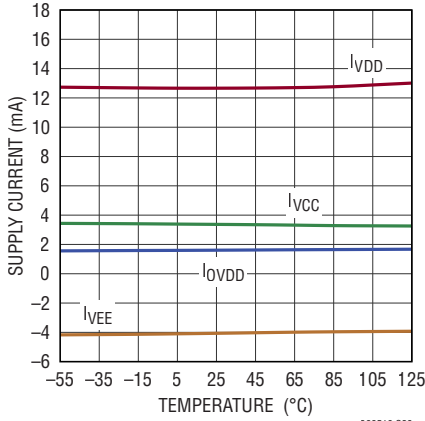


**Zero-Scale Error vs Temperature and Channel**



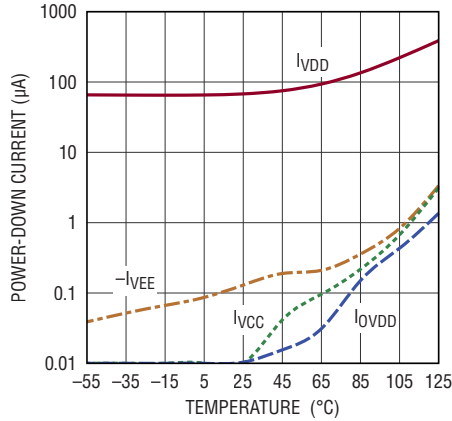
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{CC} = +15\text{V}$ , $V_{EE} = -15\text{V}$ , $V_{DD} = 5\text{V}$ , $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ), $f_{SAMPL} = 1\text{Mps}$ , unless otherwise noted.

**Supply Current vs Temperature**



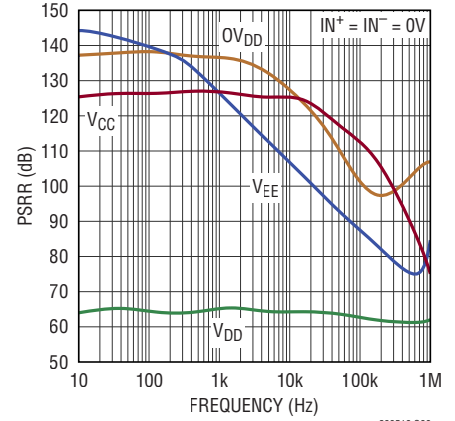
233516 G28

**Power-Down Current vs Temperature**



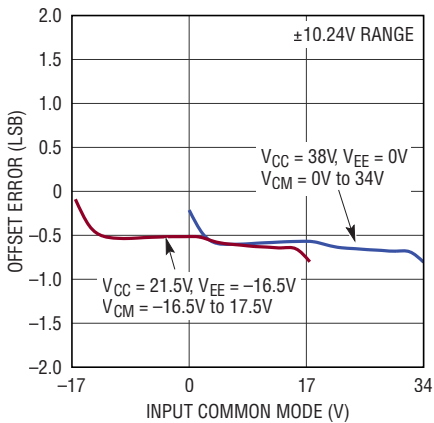
233516 G29

**PSRR vs Frequency**



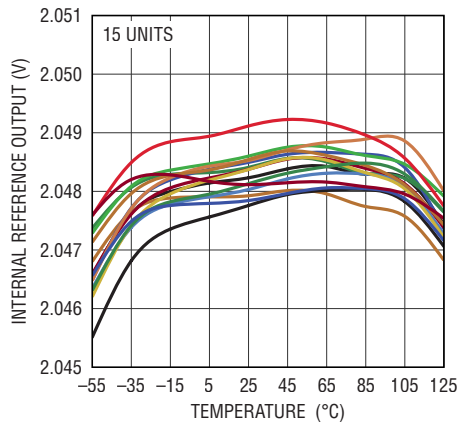
233516 G30

**Offset Error vs Input Common Mode**



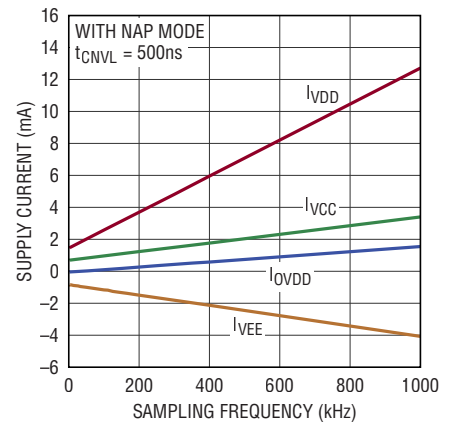
233516 G31

**Internal Reference Output vs Temperature**



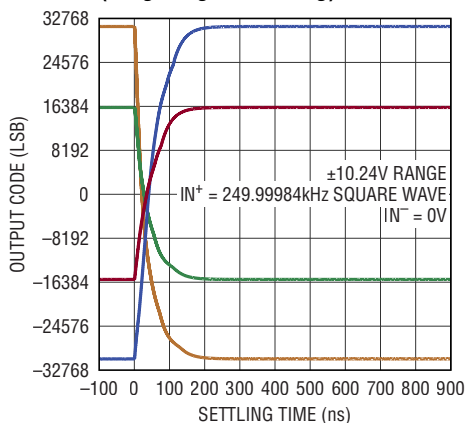
233516 G32

**Supply Current vs Sampling Rate**



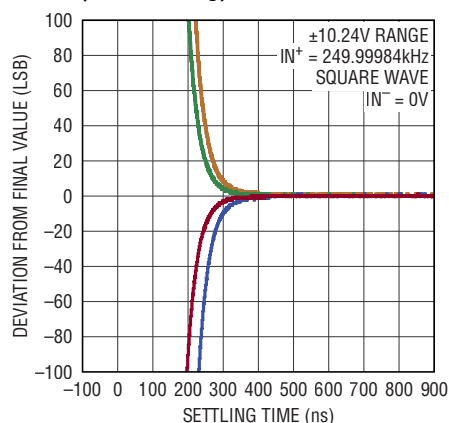
233516 G33

**Step Response (Large-Signal Settling)**



233516 G34

**Step Response (Fine Settling)**



233516 G35

## PIN FUNCTIONS

### Pins that are the Same for All Digital I/O Modes

**IN0<sup>+</sup> to IN7<sup>+</sup>, IN0<sup>-</sup> to IN7<sup>-</sup> (Pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 47, and 48):** Positive and Negative Analog Inputs, Channels 0 to 7. The converter samples ( $V_{IN+} - V_{IN-}$ ) and digitizes the selected channel. Wide input common mode range ( $V_{EE} \leq V_{CM} \leq V_{CC} - 4V$ ) and high common mode rejection allow the inputs to accept a wide variety of signal swings. Full-scale input range is determined by the selected SoftSpan configuration.

**GND (Pins 15, 18, 20, 25, 30, 36, 41, 44, 46):** Ground. Solder all GND pins to a solid ground plane.

**V<sub>CC</sub> (Pin 16):** Positive High Voltage Power Supply. The range of  $V_{CC}$  is 0V to 38V with respect to GND and 10V to 38V with respect to  $V_{EE}$ . Bypass  $V_{CC}$  to GND close to the pin with a 0.1 $\mu$ F ceramic capacitor. In applications where  $V_{CC}$  is shorted to GND this capacitor may be omitted.

**V<sub>EE</sub> (Pins 17, 45):** Negative High Voltage Power Supply. The range of  $V_{EE}$  is 0V to -16.5V with respect to GND and -10V to -38V with respect to  $V_{CC}$ . Connect Pins 17 and 45 together and bypass the  $V_{EE}$  network to GND close to Pin 17 with a 0.1 $\mu$ F ceramic capacitor. In applications where  $V_{EE}$  is shorted to GND this capacitor may be omitted.

**REFIN (Pin 19):** Bandgap Reference Output/Reference Buffer Input. An internal bandgap reference nominally outputs 2.048V on this pin. An internal reference buffer amplifies  $V_{REFIN}$  to create the converter master reference voltage  $V_{REFBUF} = 2 \cdot V_{REFIN}$  on the REFBUF pin. When using the internal reference, bypass REFIN to GND (Pin 20) close to the pin with a 0.1 $\mu$ F ceramic capacitor to filter the bandgap output noise. If more accuracy is desired, overdrive REFIN with an external reference in the range of 1.25V to 2.2V.

**REFBUF (Pin 21):** Internal Reference Buffer Output. An internal reference buffer amplifies  $V_{REFIN}$  to create the converter master reference voltage  $V_{REFBUF} = 2 \cdot V_{REFIN}$  on this pin, nominally 4.096V when using the internal bandgap reference. Bypass REFBUF to GND (Pin 20) close to the pin with a 47 $\mu$ F ceramic capacitor. The internal reference

buffer may be disabled by grounding its input at REFIN. With the buffer disabled, overdrive REFBUF with an external reference voltage in the range of 2.5V to 5V. When using the internal reference buffer, limit the loading of any external circuitry connected to REFBUF to less than 10 $\mu$ A. Using a high input impedance amplifier to buffer  $V_{REFBUF}$  to any external circuits is recommended.

**PD (Pin 22):** Power Down Input. When this pin is brought high, the LTC2335-16 is powered down and subsequent conversion requests are ignored. If this occurs during a conversion, the device powers down once the conversion completes. If this pin is brought high twice without an intervening conversion, an internal global reset is initiated, equivalent to a power-on-reset event. Logic levels are determined by  $OV_{DD}$ .

**LVDS/CMOS (Pin 23):** I/O Mode Select. Tie this pin to  $OV_{DD}$  to select LVDS I/O mode, or to ground to select CMOS I/O mode. Logic levels are determined by  $OV_{DD}$ .

**CNV (Pin 24):** Conversion Start Input. A rising edge on this pin puts the internal sample-and-holds into the hold mode and initiates a new conversion. CNV is not gated by  $\overline{CS}$ , allowing conversions to be initiated independent of the state of the serial I/O bus.

**BUSY (Pin 38):** Busy Output. The BUSY signal indicates that a conversion is in progress. This pin transitions low-to-high at the start of each conversion and stays high until the conversion is complete. Logic levels are determined by  $OV_{DD}$ .

**V<sub>DDL</sub>BYP (Pin 40):** Internal 2.5V Regulator Bypass Pin. The voltage on this pin is generated via an internal regulator operating off of  $V_{DD}$ . This pin must be bypassed to GND close to the pin with a 2.2 $\mu$ F ceramic capacitor. Do not connect this pin to any external circuitry.

**V<sub>DD</sub> (Pins 42, 43):** 5V Power Supply. The range of  $V_{DD}$  is 4.75V to 5.25V. Connect Pins 42 and 43 together and bypass the  $V_{DD}$  network to GND with a shared 0.1 $\mu$ F ceramic capacitor close to the pins.

## PIN FUNCTIONS

### CMOS I/O Mode

**SDI<sup>+</sup>, SDI<sup>-</sup>, SCKI<sup>+</sup>, SDO<sup>+</sup>, SDO<sup>-</sup> (Pins 26, 27, 28, 34, and 35):** LVDS Inputs and Outputs. In CMOS I/O mode these pins are Hi-Z.

**SCKI (Pin 29):** CMOS Serial Clock Input. Drive SCKI with the serial I/O clock. SCKI rising edges latch serial data in on SDI and clock serial data out on SDO. For standard SPI bus operation, capture output data at the receiver on rising edges of SCKI. SCKI is allowed to idle either high or low. Logic levels are determined by  $OV_{DD}$ .

**$OV_{DD}$  (Pin 31):** I/O Interface Power Supply. In CMOS I/O mode, the range of  $OV_{DD}$  is 1.71V to 5.25V. Bypass  $OV_{DD}$  to GND (Pin 30) close to the pin with a 0.1 $\mu$ F ceramic capacitor.

**SCKO (Pin 32):** CMOS Serial Clock Output. SCKI rising edges trigger transitions on SCKO that are skew-matched to the serial output data stream on SDO. The resulting SCKO frequency is half that of SCKI. Rising and falling edges of SCKO may be used to capture SDO data at the receiver (FPGA) in double data rate (DDR) fashion. For standard SPI bus operation, SCKO is not used and should be left unconnected. SCKO is forced low at the falling edge of BUSY. Logic levels are determined by  $OV_{DD}$ .

**SDO (Pin 33):** CMOS Serial Data Output. The most recent conversion result along with channel configuration information is clocked out onto the SDO pin on each rising edge of SCKI. Output data formatting is described in the Digital Interface section. Logic levels are determined by  $OV_{DD}$ .

**SDI (Pin 37):** CMOS Serial Data Input. Drive this pin with the desired MUX control words (see Table 1a), latched on the rising edges of SCKI. Hold SDI low while clocking SCKI to configure the next conversion according to the previously programmed sequence. Logic levels are determined by  $OV_{DD}$ .

**$\overline{CS}$  (Pin 39):** Chip Select Input. The serial data I/O bus is enabled when  $\overline{CS}$  is low and is disabled and Hi-Z when  $\overline{CS}$  is high.  $\overline{CS}$  also gates the external shift clock, SCKI. Logic levels are determined by  $OV_{DD}$ .

### LVDS I/O Mode

**SDI<sup>+</sup>, SDI<sup>-</sup> (Pins 26 and 27):** LVDS Positive and Negative Serial Data Input. Differentially drive SDI<sup>+</sup>/SDI<sup>-</sup> with the desired MUX control words (see Table 1a), latched on both the rising and falling edges of SCKI<sup>+</sup>/SCKI<sup>-</sup>. The SDI<sup>+</sup>/SDI<sup>-</sup> input pair is internally terminated with a 100 $\Omega$  differential resistor when  $\overline{CS}$  is low.

**SCKI<sup>+</sup>, SCKI<sup>-</sup> (Pins 28 and 29):** LVDS Positive and Negative Serial Clock Input. Differentially drive SCKI<sup>+</sup>/SCKI<sup>-</sup> with the serial I/O clock. SCKI<sup>+</sup>/SCKI<sup>-</sup> rising and falling edges latch serial data in on SDI<sup>+</sup>/SDI<sup>-</sup> and clock serial data out on SDO<sup>+</sup>/SDO<sup>-</sup>. Idle SCKI<sup>+</sup>/SCKI<sup>-</sup> low, including when transitioning  $\overline{CS}$ . The SCKI<sup>+</sup>/SCKI<sup>-</sup> input pair is internally terminated with a 100 $\Omega$  differential resistor when  $\overline{CS}$  is low.

**$OV_{DD}$  (Pin 31):** I/O Interface Power Supply. In LVDS I/O mode, the range of  $OV_{DD}$  is 2.375V to 5.25V. Bypass  $OV_{DD}$  to GND (Pin 30) close to the pin with a 0.1 $\mu$ F ceramic capacitor.

**SCKO<sup>+</sup>, SCKO<sup>-</sup> (Pins 32 and 33):** LVDS Positive and Negative Serial Clock Output. SCKO<sup>+</sup>/SCKO<sup>-</sup> outputs a copy of the input serial I/O clock received on SCKI<sup>+</sup>/SCKI<sup>-</sup>, skew-matched with the serial output data stream on SDO<sup>+</sup>/SDO<sup>-</sup>. Use the rising and falling edges of SCKO<sup>+</sup>/SCKO<sup>-</sup> to capture SDO<sup>+</sup>/SDO<sup>-</sup> data at the receiver (FPGA). The SCKO<sup>+</sup>/SCKO<sup>-</sup> output pair must be differentially terminated with a 100 $\Omega$  resistor at the receiver (FPGA).

**SDO<sup>+</sup>, SDO<sup>-</sup> (Pins 34 and 35):** LVDS Positive and Negative Serial Data Output. The most recent conversion result along with channel configuration information is clocked out onto SDO<sup>+</sup>/SDO<sup>-</sup> on both rising and falling edges of SCKI<sup>+</sup>/SCKI<sup>-</sup>. The SDO<sup>+</sup>/SDO<sup>-</sup> output pair must be differentially terminated with a 100 $\Omega$  resistor at the receiver (FPGA).

**SDI (Pin 37):** CMOS Serial Data Input. In LVDS I/O mode this pin is Hi-Z.

**$\overline{CS}$  (Pin 39):** Chip Select Input. The serial data I/O bus is enabled when  $\overline{CS}$  is low, and is disabled and Hi-Z when  $\overline{CS}$  is high.  $\overline{CS}$  also gates the external shift clock, SCKI<sup>+</sup>/SCKI<sup>-</sup>. The internal 100 $\Omega$  differential termination resistors on the SCKI<sup>+</sup>/SCKI<sup>-</sup> and SDI<sup>+</sup>/SDI<sup>-</sup> input pairs are disabled when  $\overline{CS}$  is high. Logic levels are determined by  $OV_{DD}$ .

## CONFIGURATION TABLES

**Table 1a. SoftSpan Configuration Table. Use This Table with Table 1b to Choose Binary SoftSpan Codes SS[2:0] Based on Desired Analog Input Range. Combine MUX Word Header (10) with Binary Channel Number and SoftSpan Code to Form MUX Control Word C[7:0]. Use Serial Interface to Program LTC2335-16 Sequencer as Shown in Figures 17 to 20**

BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE	FULL SCALE RANGE	BINARY FORMAT OF CONVERSION RESULT
111	$\pm 2.5 \cdot V_{REFBUF}$	$5 \cdot V_{REFBUF}$	Two's Complement
110	$\pm 2.5 \cdot V_{REFBUF}/1.024$	$5 \cdot V_{REFBUF}/1.024$	Two's Complement
101	0V to $2.5 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Straight Binary
100	0V to $2.5 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Straight Binary
011	$\pm 1.25 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Two's Complement
010	$\pm 1.25 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Two's Complement
001	0V to $1.25 \cdot V_{REFBUF}$	$1.25 \cdot V_{REFBUF}$	Straight Binary
000	0V to $1.25 \cdot V_{REFBUF}/1.024$	$1.25 \cdot V_{REFBUF}/1.024$	Straight Binary

**Table 1b. Reference Configuration Table. The LTC2335-16 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage,  $V_{REFBUF}$**

REFERENCE CONFIGURATION	$V_{REFIN}$	$V_{REFBUF}$	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
Internal Reference with Internal Buffer	2.048V	4.096V	111	$\pm 10.24V$
			110	$\pm 10V$
			101	0V to 10.24V
			100	0V to 10V
			011	$\pm 5.12V$
			010	$\pm 5V$
			001	0V to 5.12V
			000	0V to 5V
External Reference with Internal Buffer (REFIN Pin Externally Overdriven)	1.25V (Min Value)	2.5V	111	$\pm 6.25V$
			110	$\pm 6.104V$
			101	0V to 6.25V
			100	0V to 6.104V
			011	$\pm 3.125V$
			010	$\pm 3.052V$
			001	0V to 3.125V
			000	0V to 3.052V
	2.2V (Max Value)	4.4V	111	$\pm 11V$
			110	$\pm 10.742V$
			101	0V to 11V
			100	0V to 10.742V
			011	$\pm 5.5V$
			010	$\pm 5.371V$
			001	0V to 5.5V
			000	0V to 5.371V



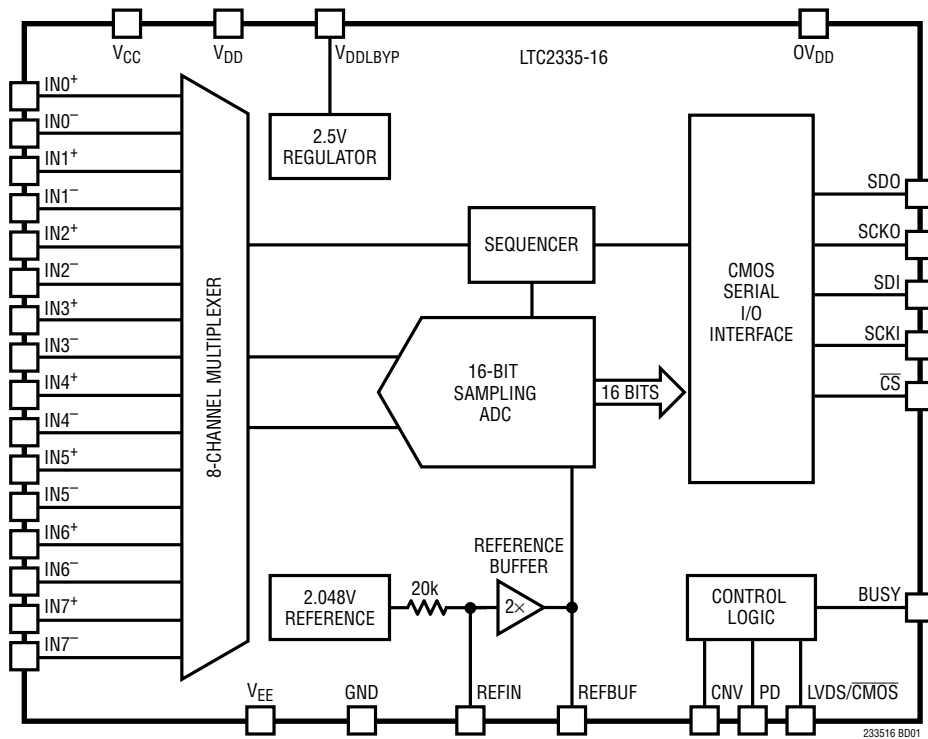
## CONFIGURATION TABLES

Table 1b. Reference Configuration Table (Continued). The LTC2335-16 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage,  $V_{REFBUF}$

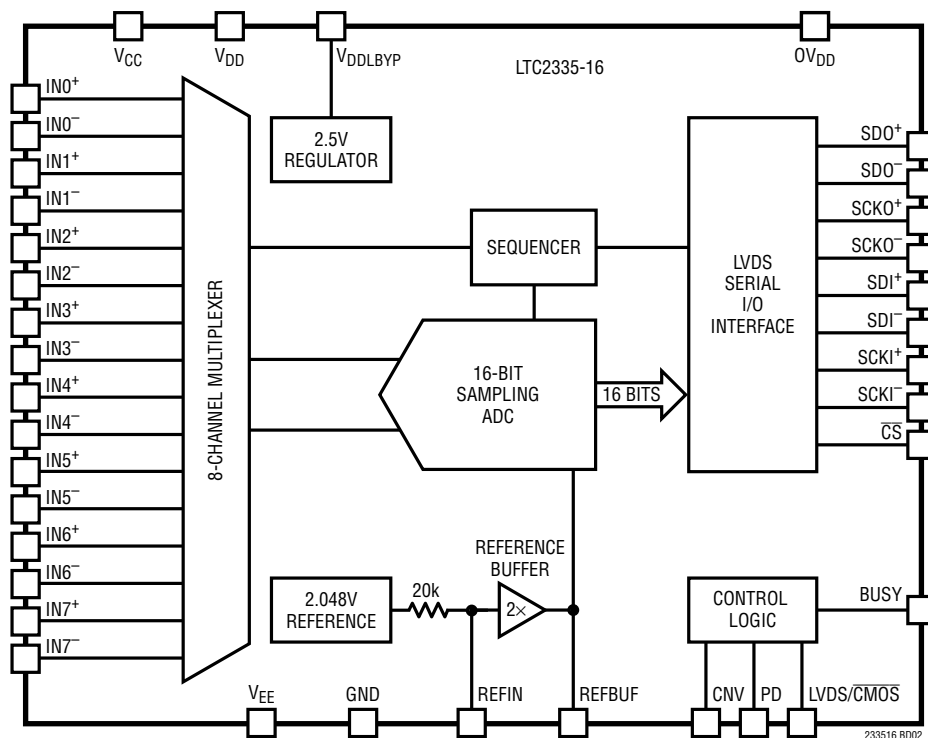
REFERENCE CONFIGURATION	$V_{REFIN}$	$V_{REFBUF}$	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
External Reference Unbuffered (REFBUF Pin Externally Overdriven, REFIN Pin Grounded)	0V	2.5V (Min Value)	111	$\pm 6.25V$
			110	$\pm 6.104V$
			101	0V to 6.25V
			100	0V to 6.104V
			011	$\pm 3.125V$
			010	$\pm 3.052V$
			001	0V to 3.125V
			000	0V to 3.052V
	0V	5V (Max Value)	111	$\pm 12.5V$
			110	$\pm 12.207V$
			101	0V to 12.5V
			100	0V to 12.207V
			011	$\pm 6.25V$
			010	$\pm 6.104V$
			001	0V to 6.25V
			000	0V to 6.104V

# FUNCTIONAL BLOCK DIAGRAM

CMOS I/O Mode



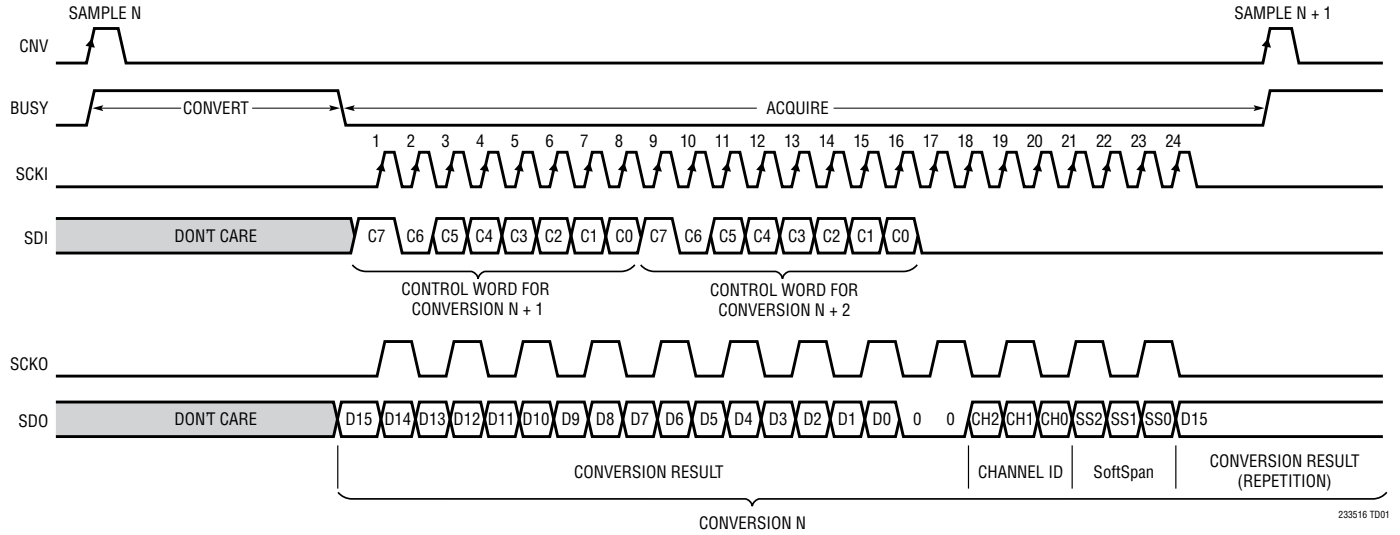
LVDS I/O Mode



## TIMING DIAGRAM

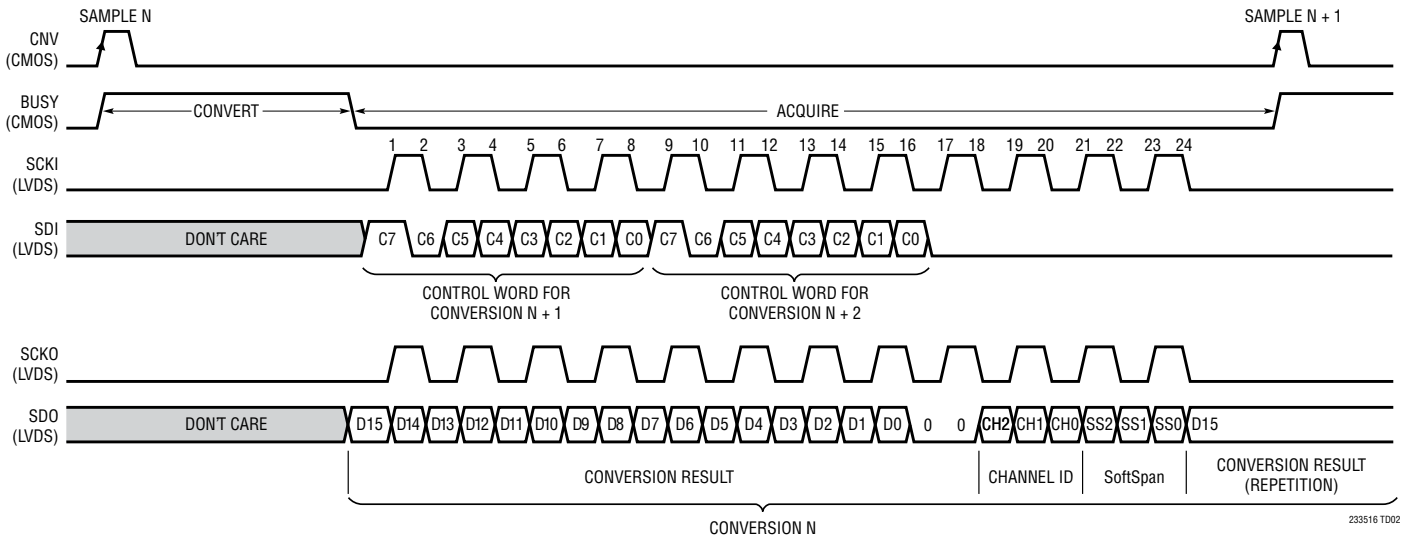
### CMOS I/O Mode

$\overline{CS} = PD = 0$



### LVDS I/O Mode

$\overline{CS} = PD = 0$



## APPLICATIONS INFORMATION

### OVERVIEW

The LTC2335-16 is a 16-bit, low noise 8-channel multiplexed successive approximation register (SAR) ADC with differential, wide common mode range inputs. The ADC operates from a 5V low voltage supply and flexible high voltage supplies, nominally  $\pm 15\text{V}$ . Using the integrated low-drift reference and buffer ( $V_{\text{REFBUF}} = 4.096\text{V}$  nominal), this SoftSpan ADC can be configured on a conversion-by-conversion basis to accept  $\pm 10.24\text{V}$ ,  $0\text{V}$  to  $10.24\text{V}$ ,  $\pm 5.12\text{V}$ , or  $0\text{V}$  to  $5.12\text{V}$  signals on any channel. Alternately, the ADC may be programmed to cycle through a sequence of channels and ranges without further user intervention. The input signal range may be expanded up to  $\pm 12.5\text{V}$  using an external 5V reference.

The wide input common mode range and high CMRR (118dB typical,  $V_{\text{IN}+} = V_{\text{IN}-} = 18\text{V}_{\text{P-P}}$  200Hz Sine) of the LTC2335-16 analog inputs allow the ADC to directly digitize a variety of signals, simplifying signal chain design. The absolute common mode input range is determined by the choice of high voltage supplies, which may be biased asymmetrically around ground and include the ability for either the positive or negative supply to be tied directly to ground. This input signal flexibility, combined with  $\pm 1\text{LSB}$  INL, no missing codes at 16-bits, and 94.4dB SNR, makes the LTC2335-16 an ideal choice for many high voltage applications requiring wide dynamic range.

The LTC2335-16 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces, enabling it to communicate equally well with legacy microcontrollers and modern FPGAs. The LTC2335-16 typically dissipates 180mW when converting at 1MSPs throughput. Optional nap and power down modes may be employed to further reduce power consumption during inactive periods.

### CONVERTER OPERATION

The LTC2335-16 operates in two phases. During the acquisition phase, the sampling capacitors in each channel connect to their respective analog input pins and track the differential analog input voltage ( $V_{\text{IN}+} - V_{\text{IN}-}$ ). A rising edge on the CNV pin transitions the S/H circuits from track mode to hold mode, sampling the input signals and initiating a conversion. During the conversion phase, the selected channel's sampling capacitors are connected to a 16-bit

charge redistribution capacitor D/A converter (CDAC). The CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input voltage with binary-weighted fractions of the channel's SoftSpan full-scale range (e.g.,  $V_{\text{FSR}}/2$ ,  $V_{\text{FSR}}/4 \dots V_{\text{FSR}}/65536$ ) using a differential comparator. At the end of this process, the CDAC output approximates the channel's sampled analog input. The ADC control logic then prepares the 16-bit digital output code for serial transfer.

### TRANSFER FUNCTION

The LTC2335-16 digitizes the full-scale voltage range into  $2^{16}$  levels. In conjunction with the ADC master reference voltage,  $V_{\text{REFBUF}}$ , the selected SoftSpan configuration determines its input voltage range, full-scale range, LSB size, and the binary format of its conversion result, as shown in Tables 1a and 1b. For example, employing the internal reference and buffer ( $V_{\text{REFBUF}} = 4.096\text{V}$  nominal), SoftSpan 7 configures a channel to accept a  $\pm 10.24\text{V}$  bipolar analog input voltage range, which corresponds to a  $20.48\text{V}$  full-scale range with a  $312.5\mu\text{V}$  LSB. Other SoftSpan configurations and reference voltages may be employed to convert both larger and smaller bipolar and unipolar input ranges. Conversion results are output in two's complement binary format for all bipolar SoftSpan ranges, and in straight binary format for all unipolar SoftSpan ranges. The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3.

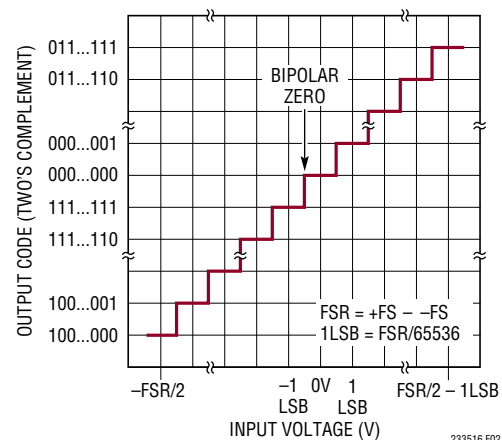


Figure 2. LTC2335-16 Two's Complement Transfer Function

## APPLICATIONS INFORMATION

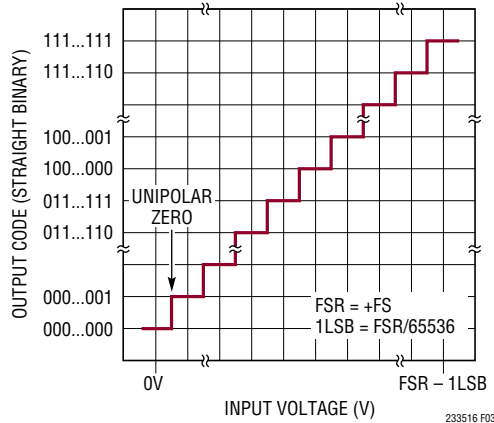


Figure 3. LTC2335-16 Straight Binary Transfer Function

## ANALOG INPUTS

The LTC2335-16 samples the voltage difference ( $V_{IN+} - V_{IN-}$ ) between its analog input pins over a wide common mode input range while attenuating unwanted signals common to both input pins by the common-mode rejection ratio (CMRR) of the ADC. Wide common mode input range coupled with high CMRR allows the  $IN^+/IN^-$  analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between ( $V_{CC} - 4V$ ) and  $V_{EE}$ . This unique feature of the LTC2335-16 enables it to accept a wide variety of signal swings, including traditional classes of analog input signals such as pseudo-differential unipolar, pseudo-differential true bipolar, and fully differential, simplifying signal chain design.

The wide operating range of the high voltage supplies offers further input common mode flexibility. As long as the voltage difference limits of  $10V \leq V_{CC} - V_{EE} \leq 38V$  are observed,  $V_{CC}$  and  $V_{EE}$  may be independently biased anywhere within their own individual allowed operating ranges, including the ability for either of the supplies to be tied directly to ground. This feature enables the common mode input range of the LTC2335-16 to be tailored to the specific application's requirements.

In all SoftSpan ranges, each channel's analog inputs can be modeled by the equivalent circuit shown in Figure 4. At the start of acquisition, the 40pF sampling capacitors ( $C_{IN}$ ) connect to the analog input pins  $IN^+/IN^-$  through

the sampling switches, each of which has approximately  $600\Omega$  ( $R_{IN}$ ) of on-resistance. This behavior occurs on all channels, so that the LTC2335-16 may respond instantly to user-requested changes in multiplexer configuration with no additional settling time required.

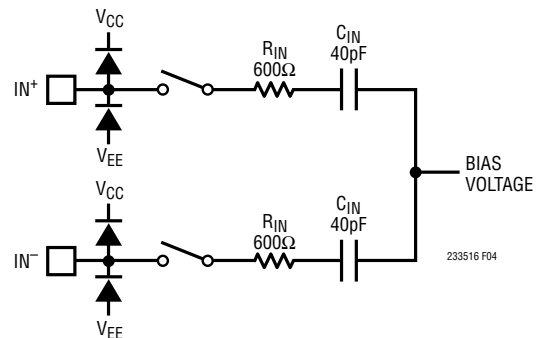


Figure 4. Equivalent Circuit for Differential Analog Inputs, Single Channel Shown

The initial voltage on both capacitors of the just-converted channel will be approximately the sampled common mode voltage  $(V_{IN+} + V_{IN-})/2$  from the previous conversion. Other channels' capacitors will retain approximately the voltage of their respective  $IN^+/IN^-$  pin at the beginning of the previous conversion. The external circuitry connected to  $IN^+$  and  $IN^-$  must source or sink the charge that flows through  $R_{IN}$  as the sampling capacitors settle from their initial voltages to the new input pin voltages over the course of the acquisition interval. During conversion, nap, and power down modes, the analog inputs draw only a small leakage current. The diodes at the inputs provide ESD protection.

## Bipolar SoftSpan Input Ranges

For conversions configured in SoftSpan ranges 7, 6, 3, or 2, the LTC2335-16 digitizes the differential analog input voltage ( $V_{IN+} - V_{IN-}$ ) over a bipolar span of  $\pm 2.5 \cdot V_{REFBUF}$ ,  $\pm 2.5 \cdot V_{REFBUF}/1.024$ ,  $\pm 1.25 \cdot V_{REFBUF}$ , or  $\pm 1.25 \cdot V_{REFBUF}/1.024$ , respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where  $IN^+$  and  $IN^-$  swing above and below each

## APPLICATIONS INFORMATION

other. Traditional examples include fully differential input signals, where  $IN^+$  and  $IN^-$  are driven 180 degrees out-of-phase with respect to each other centered around a common mode voltage  $(V_{IN^+} + V_{IN^-})/2$ , and pseudo-differential true bipolar input signals, where  $IN^+$  swings above and below a ground reference level, driven on  $IN^-$ . Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the  $IN^+/IN^-$  analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $V_{EE}$ . The output data format for all bipolar SoftSpan ranges is two's complement.

### Unipolar SoftSpan Input Ranges

For conversions configured in SoftSpan ranges 5, 4, 1, or 0, the LTC2335-16 digitizes the differential analog input voltage  $(V_{IN^+} - V_{IN^-})$  over a unipolar span of 0V to  $2.5 \cdot V_{REFBUF}$ , 0V to  $2.5 \cdot V_{REFBUF}/1.024$ , 0V to  $1.25 \cdot V_{REFBUF}$ , or 0V to  $1.25 \cdot V_{REFBUF}/1.024$ , respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where  $IN^+$  remains above  $IN^-$ . A traditional example includes pseudo-differential unipolar input signals, where  $IN^+$  swings above a ground reference level, driven on  $IN^-$ . Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the  $IN^+/IN^-$  analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $V_{EE}$ . The output data format for all unipolar SoftSpan ranges is straight binary.

### INPUT DRIVE CIRCUITS

The initial voltage on each channel's sampling capacitors at the start of acquisition must settle to the new input pin voltages during the acquisition interval. The external circuitry connected to  $IN^+$  and  $IN^-$  must source or sink the charge that flows through  $R_{IN}$  as this settling occurs. The LTC2335-16 sampling network RC time constant of

24ns implies a 16-bit settling time to a full-scale step of approximately  $11 \cdot (R_{IN} \cdot C_{IN}) = 264ns$ . The impedance and self-settling of external circuitry connected to the analog input pins will increase the overall settling time required. Low impedance sources can directly drive the inputs of the LTC2335-16 without gain error, but high impedance sources should be buffered to ensure sufficient settling during acquisition and to optimize the linearity and distortion performance of the ADC. Settling time is an important consideration even for DC input signals, as the voltages on the sampling capacitors will differ from the analog input pin voltages at the start of acquisition.

Most applications should use a buffer amplifier to drive the analog inputs of the LTC2335-16. The amplifier provides low output impedance, enabling fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the charge flow at the analog inputs when entering acquisition.

### Input Filtering

The noise and distortion of an input buffer amplifier and other supporting circuitry must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the buffer amplifier with a low-bandwidth filter to minimize noise. The simple one-pole RC lowpass filter shown in Figure 5 is sufficient for many applications.

At the output of the buffer, a lowpass RC filter network formed by the  $600\Omega$  sampling switch on-resistance ( $R_{IN}$ ) and the 40pF sampling capacitance ( $C_{IN}$ ) limits the input bandwidth on each channel to 7MHz, which is fast enough to allow for sufficient transient settling during acquisition while simultaneously filtering driver wideband noise. A buffer amplifier with low noise density should be selected to minimize SNR degradation over this bandwidth. An additional filter network may be placed between the buffer output and ADC input to further minimize the noise

## APPLICATIONS INFORMATION

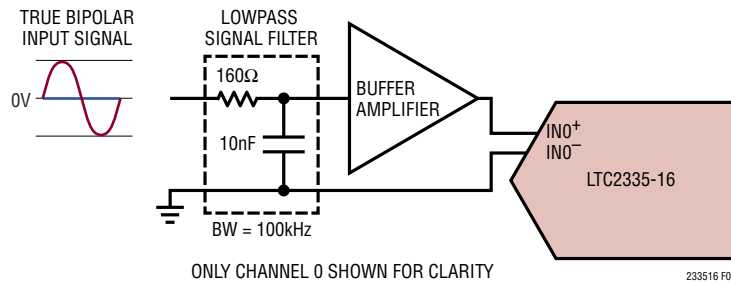


Figure 5. True Bipolar Signal Chain with Input Filtering

contribution of the buffer. A simple one-pole lowpass RC filter is sufficient for many applications.

This filter interacts with the buffer amplifier and slows input settling. It is important that the inputs settle to 16-bit resolution within the ADC acquisition time ( $t_{ACQ}$ ), as insufficient settling can limit INL and THD performance.

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO/COG and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

### Buffering Arbitrary and Fully Differential Analog Input Signals

The wide common mode input range and high CMRR of the LTC2335-16 allow each channel's  $IN^+$  and  $IN^-$  pins to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $V_{EE}$ . This unique feature of the LTC2335-16 enables it to accept

a wide variety of signal swings, simplifying signal chain design. In many applications, connecting a channel's  $IN^+$  and  $IN^-$  pins directly to the existing signal chain circuitry will not allow the channel's sampling network to settle to 16-bit resolution within the ADC acquisition time ( $t_{ACQ}$ ). In these cases, it is recommended that two unity-gain buffers be inserted between the signal source and the ADC input pins, as shown in Figure 6a. Table 2 lists several amplifier and lowpass filter combinations recommended for use in this circuit.

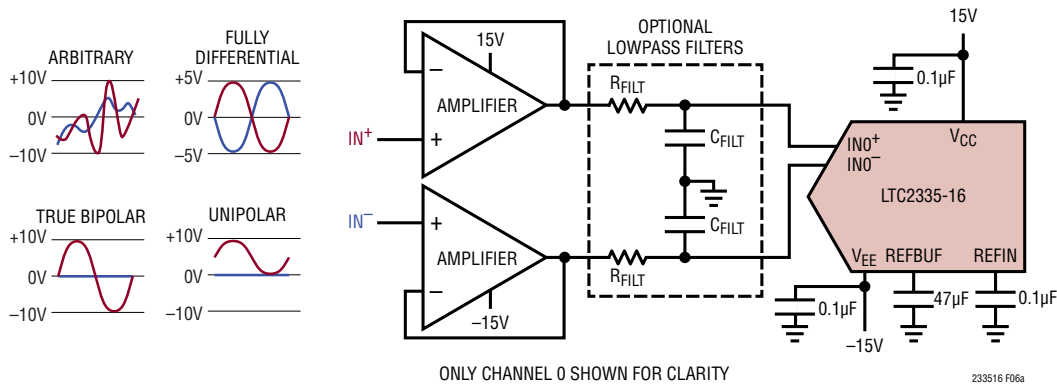
The LT1358 combines fast settling, high linearity, and low input-referred noise density, allowing it to approach the full ADC data sheet SNR and THD specifications, when used with a lowpass filter, as shown in the FFT plots in Figures 6b to 6e. It may be used without a filter at a loss of 0.2dB SNR due to wideband noise. The LT1469 achieves the full ADC specifications for DC precision, THD, and linearity, at a cost of 0.5dB in SNR. Finally, the LT1355 provides a good general-purpose combination of THD and SNR at a lower power. Neither the LT1469 nor LT1355 can afford the slowing effect of a lowpass filter if they are to be used at the minimum  $t_{ACQ}$  of 420ns.

**Table 2. Recommended Amplifier and Filter Combinations for the Buffer Circuits in Figures 6a and 9. AC Performance Measured Using Circuit in Figure 6a,  $\pm 10.24V$  Range**

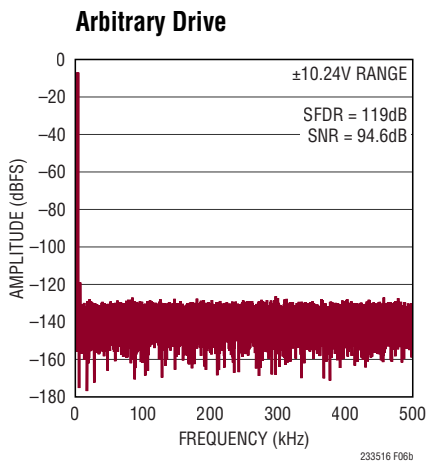
AMPLIFIER	$R_{FILT}$ ( $\Omega$ )	$C_{FILT}$ (pF)	INPUT SIGNAL DRIVE	SNR (dB)	THD (dB)	SINAD (dB)	SFDR (dB)
$\frac{1}{2}$ LT1358	100	270	FULLY DIFFERENTIAL	94.5	-120	94.5	120
$\frac{1}{2}$ LT1469	0	0	FULLY DIFFERENTIAL	94.0	-124	94.0	120
$\frac{1}{2}$ LT1358	100	270	TRUE BIPOLAR	94.5	-107	94.3	108
$\frac{1}{2}$ LT1358	0	0	TRUE BIPOLAR	94.3	-108	94.2	110
$\frac{1}{2}$ LT1469	0	0	TRUE BIPOLAR	94.0	-109	94.0	110
$\frac{1}{2}$ LT1355	0	0	TRUE BIPOLAR	94.1	-103	93.6	104

233516f

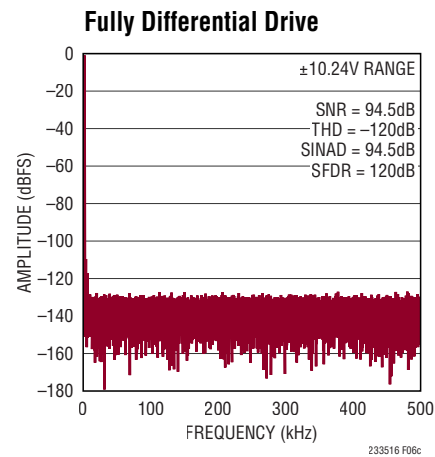
# APPLICATIONS INFORMATION



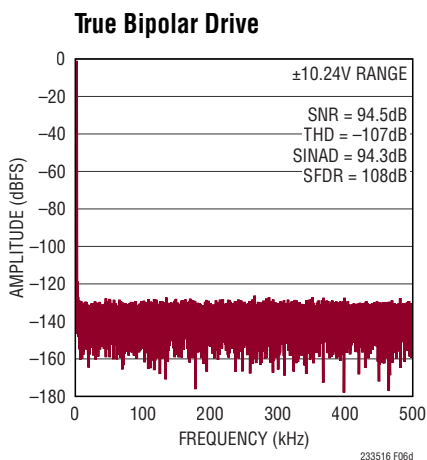
**Figure 6a. Buffering Arbitrary, Fully Differential, True Bipolar, and Unipolar Signals. See Table 2 for Recommended Amplifier and Filter Combinations**



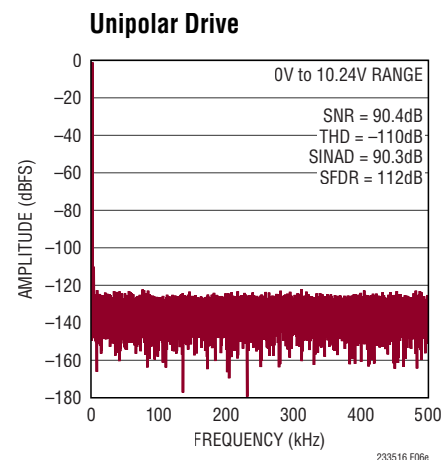
**Figure 6b. Two-Tone Test.  $IN^+ = -7$ dBFS 2kHz Sine,  $IN^- = -7$ dBFS 3.1kHz Sine, 32k Point FFT,  $f_{SAMPL} = 1$ Msp. Circuit Shown in Figure 6a with LT1358 Amplifiers,  $R_{FILT} = 100\Omega$ ,  $C_{FILT} = 270$ pF**



**Figure 6c.  $IN^+/IN^- = -1$ dBFS 2kHz Fully Differential Sine,  $V_{CM} = 0$ V, 32k Point FFT,  $f_{SAMPL} = 1$ Msp. Circuit Shown in Figure 6a with LT1358 Amplifiers,  $R_{FILT} = 100\Omega$ ,  $C_{FILT} = 270$ pF**



**Figure 6d.  $IN^+ = -1$ dBFS 2kHz True Bipolar Sine,  $IN^- = 0$ V, 32k Point FFT,  $f_{SAMPL} = 1$ Msp. Circuit Shown in Figure 6a with LT1358 Amplifiers,  $R_{FILT} = 100\Omega$ ,  $C_{FILT} = 270$ pF**



**Figure 6e.  $IN^+ = -1$ dBFS 2kHz Unipolar Sine,  $IN^- = 0$ V, 32k Point FFT,  $f_{SAMPL} = 1$ Msp. Circuit Shown in Figure 6a with LT1358 Amplifiers,  $R_{FILT} = 100\Omega$ ,  $C_{FILT} = 270$ pF**



## APPLICATIONS INFORMATION

The two-tone test shown in Figure 6b demonstrates the arbitrary input drive capability of the LTC2335-16. This test simultaneously drives  $IN^+$  with a  $-7\text{dBFS}$   $2\text{kHz}$  single-ended sine wave and  $IN^-$  with a  $-7\text{dBFS}$   $3.1\text{kHz}$  single-ended sine wave. Together, these signals sweep the analog inputs across a wide range of common mode and differential mode voltage combinations, similar to the more general arbitrary input signal case. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity will digitize this signal as two  $-7\text{dBFS}$  spectral tones, one at each sine wave frequency. The FFT plot in Figure 6b demonstrates the LTC2335-16 response, which approaches this ideal with  $118\text{dB}$  of SFDR limited by the converter's second harmonic distortion response to the  $3.1\text{kHz}$  sine wave on  $IN^-$ .

The ability of the LTC2335-16 to accept arbitrary signal swings over a wide input common mode range with high CMRR can simplify application solutions. In practice,

many sensors produce a differential sensor voltage riding on top of a large common mode signal. Figure 7a depicts one way of using the LTC2335-16 to digitize signals of this type. The amplifier stage provides a differential gain of approximately  $10\text{V/V}$  to the desired sensor signal while the unwanted common mode signal is attenuated by the ADC CMRR. The circuit employs the  $\pm 5\text{V}$  SoftSpan range of the ADC. Figure 7b shows measured CMRR performance of this solution, which is competitive with the best commercially available instrumentation amplifiers. Figure 7c shows measured AC performance of this solution.

In Figure 8, another application circuit is shown which uses two channels of the LTC2335-16 to sense the voltage on and bidirectional current through a sense resistor over a wide common mode range. In many applications of this type, the impedance of the external circuitry is low enough that the ADC sampling network can fully settle without buffering.

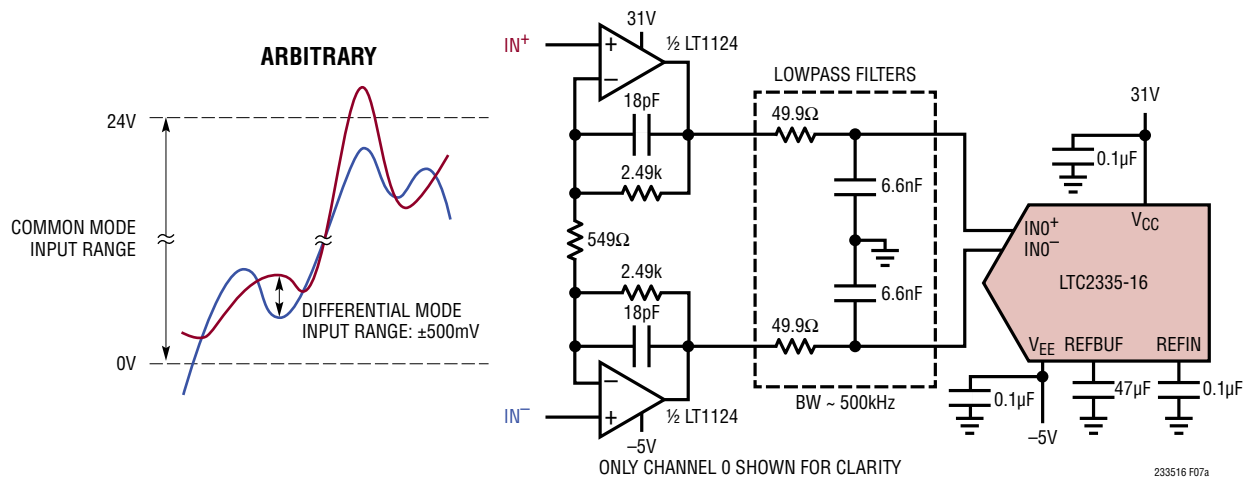


Figure 7a. Digitize Differential Signals Over a Wide Common Mode Range

# APPLICATIONS INFORMATION

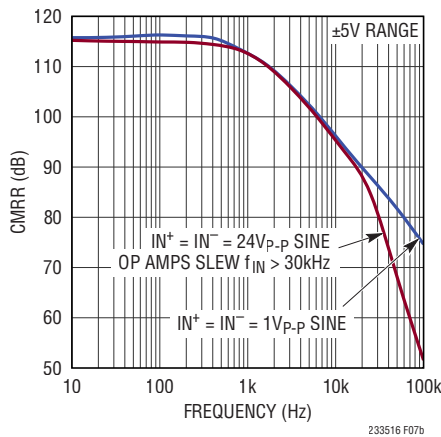


Figure 7b. CMRR vs Input Frequency. Circuit Shown in Figure 7a

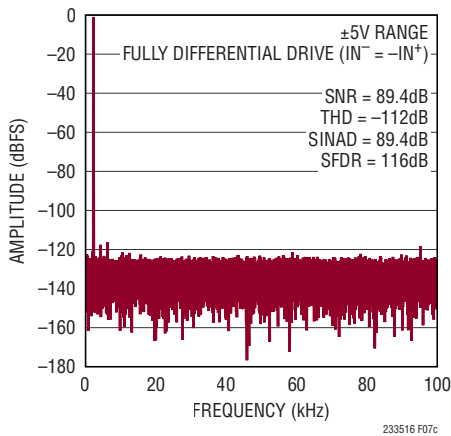
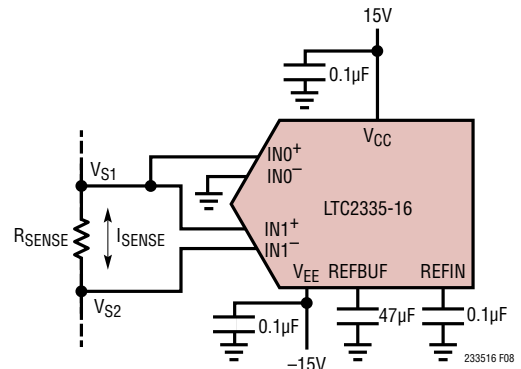


Figure 7c.  $IN^+/IN^- = 450\text{mV } 2\text{kHz}$  Fully Differential Sine,  $0\text{V} \leq V_{CM} \leq 24\text{V}$ , 32k Point FFT,  $f_{SAMPL} = 200\text{kpsps}$ . Circuit Shown in Figure 7a



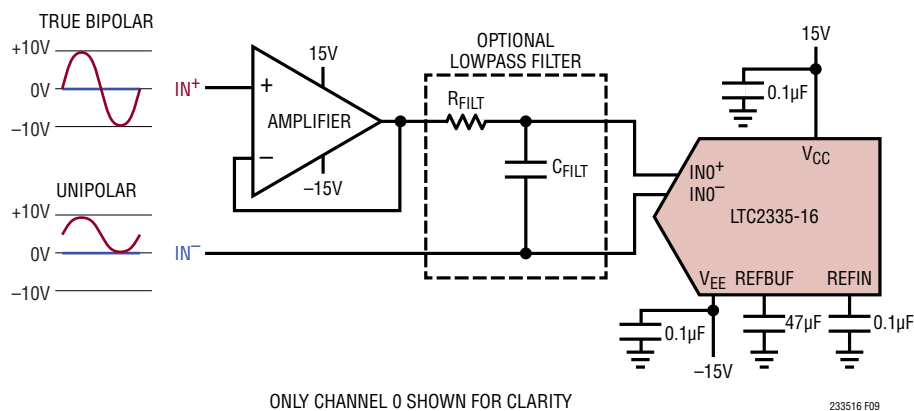
ONLY CHANNELS 0 AND 1 SHOWN FOR CLARITY

$$I_{SENSE} = \frac{V_{S1} - V_{S2}}{R_{SENSE}} \quad \begin{matrix} -10.24\text{V} \leq V_{S1} \leq 10.24\text{V} \\ -10.24\text{V} \leq V_{S2} \leq 10.24\text{V} \end{matrix}$$

Figure 8. Sense Voltage (CH0) and Current (CH1) Over a Wide Common Mode Range

## Buffering Single-Ended Analog Input Signals

While the circuit shown in Figure 6a is capable of buffering single-ended input signals, the circuit shown in Figure 9 is preferable when the single-ended signal reference level is inherently low impedance and doesn't require buffering. This circuit eliminates one driver and lowpass filter, reducing part count, power dissipation, and SNR degradation due to driver noise. Using the recommended driver and filter combinations in Table 2, the performance of this circuit with single-ended input signals is on par with the performance of the circuit in Figure 6a.



ONLY CHANNEL 0 SHOWN FOR CLARITY

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Figure 9. Buffering Single-Ended Input Signals. See Table 2 For Recommended Amplifier and Filter Combinations