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Buffered Quad, 16-Bit, 350ksps/Ch  
Differential  $\pm 10.24V$  ADC with  
 $30V_{P-P}$  Common Mode Range

**FEATURES**

- Simultaneous Sampling of 4 Buffered Channels
- 350ksps per Channel Throughput
- 500pA/12nA Max Input Leakage at 85°C/125°C
- $\pm 1$ LSB INL (Maximum,  $\pm 10.24V$  Range)
- Guaranteed 16-Bit, No Missing Codes
- Differential, Wide Common Mode Range Inputs
- Per-Channel SoftSpan Input Ranges:
  - $\pm 10.24V$ , 0V to 10.24V,  $\pm 5.12V$ , 0V to 5.12V
  - $\pm 12.5V$ , 0V to 12.5V,  $\pm 6.25V$ , 0V to 6.25V
- 94.2dB Single-Conversion SNR (Typical)
- $-110$ dB THD (Typical) at  $f_{IN} = 2$ kHz
- 128dB CMRR (Typical) at  $f_{IN} = 200$ Hz
- Rail-to-Rail Input Overdrive Tolerance
- Integrated Reference and Buffer (4.096V)
- SPI CMOS (1.8V to 5V) and LVDS Serial I/O
- Internal Conversion Clock, No Cycle Latency
- 175mW Power Dissipation (44mW/Ch Typical)
- 48-Lead (7mm x 7mm) LQFP Package

**APPLICATIONS**

- Programmable Logic Controllers
- Industrial Process Control
- Power Line Monitoring
- Test and Measurement

**DESCRIPTION**

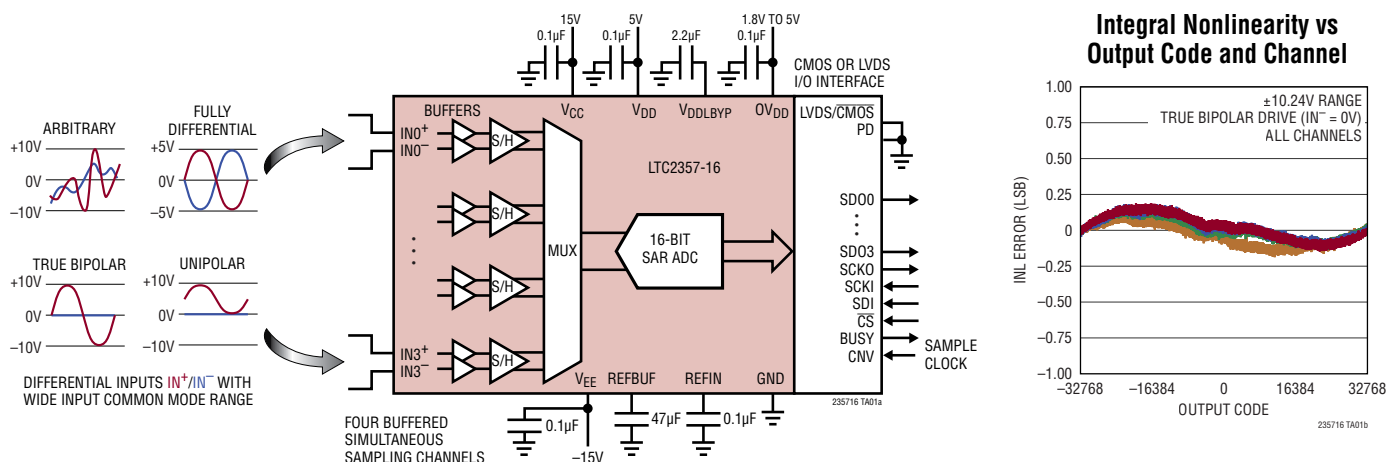
The LTC<sup>®</sup>2357-16 is a 16-bit, low noise 4-channel simultaneous sampling successive approximation register (SAR) ADC with buffered differential, wide common mode range picoamp inputs. Operating from a 5V low voltage supply, flexible high voltage supplies, and using the internal reference and buffer, each channel of this SoftSpan<sup>™</sup> ADC can be independently configured on a conversion-by-conversion basis to accept  $\pm 10.24V$ , 0V to 10.24V,  $\pm 5.12V$ , or 0V to 5.12V signals. Individual channels may also be disabled to increase throughput on the remaining channels.

The integrated picoamp-input analog buffers, wide input common mode range and 128dB CMRR of the LTC2357-16 allow the ADC to directly digitize a variety of signals using minimal board space and power. This input signal flexibility, combined with  $\pm 1$ LSB INL, no missing codes at 16 bits, and 94.2dB SNR, makes the LTC2357-16 an ideal choice for many high voltage applications requiring wide dynamic range.

The LTC2357-16 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces. Between one and four lanes of data output may be employed in CMOS mode, allowing the user to optimize bus width and throughput.

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**TYPICAL APPLICATION**



235716f

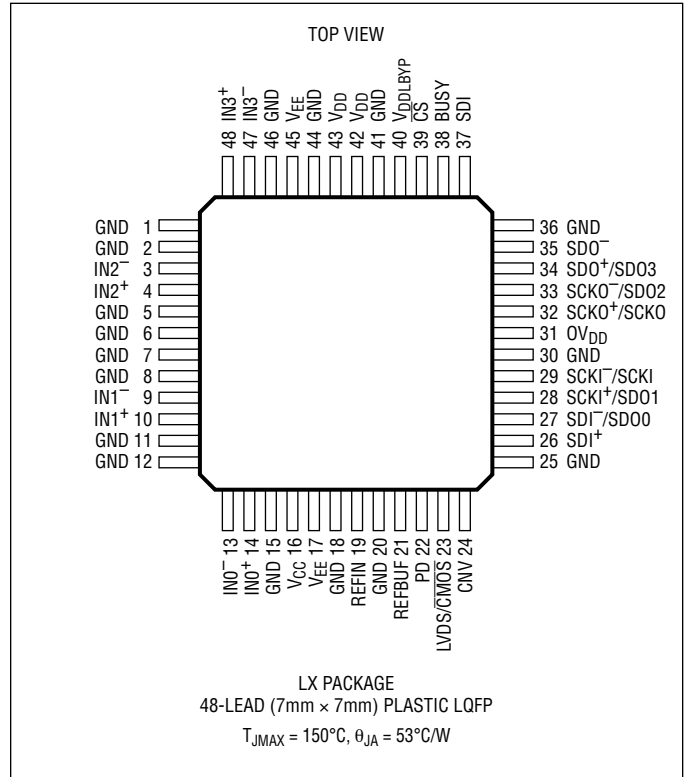
# LTC2357-16

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{CC}$ )	.....	-0.3V to ( $V_{EE} + 40V$ )
Supply Voltage ( $V_{EE}$ )	.....	-17.4V to 0.3V
Supply Voltage Difference ( $V_{CC} - V_{EE}$ )	.....	40V
Supply Voltage ( $V_{DD}$ )	.....	6V
Supply Voltage ( $OV_{DD}$ )	.....	6V
Internal Regulated Supply Bypass ( $V_{DDLBY}$ ) ...	(Note 3)	
Analog Input Voltage		
$IN0^+$ to $IN3^+$ ,		
$IN0^-$ to $IN3^-$ (Note 4) .....		
REFIN	.....	( $V_{EE} - 0.3V$ ) to ( $V_{CC} + 0.3V$ )
REFBUF, CNV (Note 5)	.....	-0.3V to ( $V_{DD} + 0.3V$ )
Digital Input Voltage (Note 5).....		
-0.3V to ( $OV_{DD} + 0.3V$ )		
Digital Output Voltage (Note 5) ..		
-0.3V to ( $OV_{DD} + 0.3V$ )		
Power Dissipation	.....	500mW
Operating Temperature Range		
LTC2357C	.....	0°C to 70°C
LTC2357I	.....	-40°C to 85°C
LTC2357H	.....	-40°C to 125°C
Storage Temperature Range	.....	-65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION

<http://www.linear.com/product/LTC2357-16#orderinfo>

TRAY	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2357CLX-16#PBF	LTC2357LX-16	48-Lead (7mm × 7mm) Plastic LQFP	0°C to 70°C
LTC2357ILX-16#PBF	LTC2357LX-16	48-Lead (7mm × 7mm) Plastic LQFP	-40°C to 85°C
LTC2357HLX-16#PBF	LTC2357LX-16	48-Lead (7mm × 7mm) Plastic LQFP	-40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 6)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN+}$	Absolute Input Range (IN0+ to IN3+)	(Note 7)	●	$V_{EE} + 4$	$V_{CC} - 4$	V
$V_{IN-}$	Absolute Input Range (IN0- to IN3-)	(Note 7)	●	$V_{EE} + 4$	$V_{CC} - 4$	V
$V_{IN+} - V_{IN-}$	Input Differential Voltage Range	SoftSpan 7: $\pm 2.5 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 6: $\pm 2.5 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 5: 0V to $2.5 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 4: 0V to $2.5 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 3: $\pm 1.25 \cdot V_{REFBUF}$ Range (Note 7) SoftSpan 2: $\pm 1.25 \cdot V_{REFBUF}/1.024$ Range (Note 7) SoftSpan 1: 0V to $1.25 \cdot V_{REFBUF}$ Range (Note 7)	● ● ● ● ● ● ●	$-2.5 \cdot V_{REFBUF}$ $-2.5 \cdot V_{REFBUF}/1.024$ 0 0 $-1.25 \cdot V_{REFBUF}$ $-1.25 \cdot V_{REFBUF}/1.024$ 0	$2.5 \cdot V_{REFBUF}$ $2.5 \cdot V_{REFBUF}/1.024$ $2.5 \cdot V_{REFBUF}$ $2.5 \cdot V_{REFBUF}/1.024$ $1.25 \cdot V_{REFBUF}$ $1.25 \cdot V_{REFBUF}/1.024$ $1.25 \cdot V_{REFBUF}$	V V V V V V V
$V_{CM}$	Input Common Mode Voltage Range	(Note 7)	●	$V_{EE} + 4$	$V_{CC} - 4$	V
$V_{IN+} - V_{IN-}$	Input Differential Overdrive Tolerance	(Note 8)	●	$-(V_{CC} - V_{EE})$	$(V_{CC} - V_{EE})$	V
$I_{OVERDRIVE}$	Input Overdrive Current Tolerance	$V_{IN+} > V_{CC}$ , $V_{IN-} > V_{CC}$ (Note 8) $V_{IN+} < V_{EE}$ , $V_{IN-} < V_{EE}$ (Note 8)	● ●	0	10	mA mA
$I_{IN}$	Analog Input Leakage Current	C-Grade and I-Grade H-Grade	● ●	5	500 12	pA pA nA
$I_{IN+} - I_{IN-}$	Analog Input Leakage Offset Current	$V_{IN+} = V_{IN-}$ $V_{IN+} = V_{IN-}$ , C-Grade and I-Grade $V_{IN+} = V_{IN-}$ , H-Grade	● ●	$\pm 1$	100 1.2	pA pA nA
$R_{IN}$	Analog Input Resistance	For Each Pin		>1000		G $\Omega$
$C_{IN}$	Analog Input Capacitance			3		pF
CMRR	Input Common Mode Rejection Ratio	$V_{IN+} = V_{IN-} = 18V_{p-p}$ 200Hz Sine	●	105	128	dB
$V_{IHCNV}$	CNV High Level Input Voltage		●	1.3		V
$V_{ILCNV}$	CNV Low Level Input Voltage		●		0.5	V
$I_{INCNV}$	CNV Input Current	$V_{IN} = 0V$ to $V_{DD}$	●	-10	10	$\mu\text{A}$

## CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	16			Bits
	No Missing Codes		●	16			Bits
	Transition Noise	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range			0.35 0.7 0.5 1.1		$\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$ $\text{LSB}_{\text{RMS}}$
INL	Integral Linearity Error	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges (Note 10)	●	-1	$\pm 0.3$	1	LSB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges (Note 10)	●	-1.25	$\pm 0.4$	1.25	LSB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges (Note 10)	●	-1	$\pm 0.4$	1	LSB
		SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range (Note 10)	●	-1.5	$\pm 0.5$	1.5	LSB
DNL	Differential Linearity Error	(Note 11)	●	-0.9	$\pm 0.1$	0.9	LSB
ZSE	Zero-Scale Error	(Note 12)	●	-900	$\pm 160$	900	$\mu\text{V}$
	Zero-Scale Error Drift				$\pm 4$		$\mu\text{V}/^\circ\text{C}$
FSE	Full-Scale Error	$V_{\text{REFBUF}} = 4.096\text{V}$ (REFBUF Overdriven) (Note 12)	●	-0.1	$\pm 0.025$	0.1	%FS
	Full-Scale Error Drift	$V_{\text{REFBUF}} = 4.096\text{V}$ (REFBUF Overdriven) (Note 12)			$\pm 2.5$		$\text{ppm}/^\circ\text{C}$

## DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $A_{\text{IN}} = -1\text{dBFS}$ . (Notes 9, 13)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	91.2	94.1		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	86.4	89.6		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	88.8	91.6		dB
		SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range, $f_{\text{IN}} = 2\text{kHz}$	●	83.3	86.5		dB
SNR	Signal-to-Noise Ratio	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	91.3	94.2		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	86.5	89.7		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	88.9	91.6		dB
		SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range, $f_{\text{IN}} = 2\text{kHz}$	●	83.4	86.5		dB
THD	Total Harmonic Distortion	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●		-110	-101	dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●		-111	-99	dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●		-112	-102	dB
		SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range, $f_{\text{IN}} = 2\text{kHz}$	●		-113	-99	dB
SFDR	Spurious Free Dynamic Range	SoftSpans 7 and 6: $\pm 10.24\text{V}$ and $\pm 10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	101	112		dB
		SoftSpans 5 and 4: $0\text{V}$ to $10.24\text{V}$ and $0\text{V}$ to $10\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	99	113		dB
		SoftSpans 3 and 2: $\pm 5.12\text{V}$ and $\pm 5\text{V}$ Ranges, $f_{\text{IN}} = 2\text{kHz}$	●	103	114		dB
		SoftSpan 1: $0\text{V}$ to $5.12\text{V}$ Range, $f_{\text{IN}} = 2\text{kHz}$	●	99	114		dB
	Channel-to-Channel Crosstalk	One Channel Converting $18\text{V}_{\text{P-P}}$ $200\text{Hz}$ Sine in $\pm 10.24\text{V}$ Range, Crosstalk to All Other Channels			-109		dB
	-3dB Input Bandwidth				6		MHz
	Aperture Delay				1		ns
	Aperture Delay Matching				150		ps
	Aperture Jitter				3		$\text{ps}_{\text{RMS}}$
	Transient Response	Full-Scale Step, 0.005% Settling			420		ns

## INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$V_{\text{REFIN}}$	Internal Reference Output Voltage		2.043	2.048	2.053	V
	Internal Reference Temperature Coefficient	(Note 14)	●	5	20	ppm/ $^\circ\text{C}$
	Internal Reference Line Regulation	$V_{\text{DD}} = 4.75\text{V}$ to $5.25\text{V}$		0.1		mV/V
	Internal Reference Output Impedance			20		k $\Omega$
$V_{\text{REFIN}}$	REFIN Voltage Range	REFIN Overdriven (Note 7)	1.25		2.2	V

## REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$V_{\text{REFBUF}}$	Reference Buffer Output Voltage	REFIN Overdriven, $V_{\text{REFIN}} = 2.048\text{V}$	●	4.091	4.096	4.101	V
	REFBUF Voltage Range	REFBUF Overdriven (Notes 7, 15)	●	2.5	5	V	
	REFBUF Input Impedance	$V_{\text{REFIN}} = 0\text{V}$ , Buffer Disabled		13		k $\Omega$	
$I_{\text{REFBUF}}$	REFBUF Load Current	$V_{\text{REFBUF}} = 5\text{V}$ , 4 Channels Enabled (Notes 15, 16) $V_{\text{REFBUF}} = 5\text{V}$ , Acquisition or Nap Mode (Note 15)	●	1.4	1.5	mA	
				0.36		mA	

## DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>CMOS Digital Inputs and Outputs</b>							
$V_{\text{IH}}$	High Level Input Voltage		●	$0.8 \cdot OV_{\text{DD}}$		V	
$V_{\text{IL}}$	Low Level Input Voltage		●		$0.2 \cdot OV_{\text{DD}}$	V	
$I_{\text{IN}}$	Digital Input Current	$V_{\text{IN}} = 0\text{V}$ to $OV_{\text{DD}}$	●	-10	10	$\mu\text{A}$	
$C_{\text{IN}}$	Digital Input Capacitance			5		pF	
$V_{\text{OH}}$	High Level Output Voltage	$I_{\text{OUT}} = -500\mu\text{A}$	●	$OV_{\text{DD}} - 0.2$		V	
$V_{\text{OL}}$	Low Level Output Voltage	$I_{\text{OUT}} = 500\mu\text{A}$	●		0.2	V	
$I_{\text{OZ}}$	Hi-Z Output Leakage Current	$V_{\text{OUT}} = 0\text{V}$ to $OV_{\text{DD}}$	●	-10	10	$\mu\text{A}$	
$I_{\text{SOURCE}}$	Output Source Current	$V_{\text{OUT}} = 0\text{V}$		-50		mA	
$I_{\text{SINK}}$	Output Sink Current	$V_{\text{OUT}} = OV_{\text{DD}}$		50		mA	
<b>LVDS Digital Inputs and Outputs</b>							
$V_{\text{ID}}$	Differential Input Voltage		●	200	350	600	mV
$R_{\text{ID}}$	On-Chip Input Termination Resistance	$\overline{\text{CS}} = 0\text{V}$ , $V_{\text{ICM}} = 1.2\text{V}$ $\overline{\text{CS}} = OV_{\text{DD}}$	●	90	106	125	$\Omega$ M $\Omega$
$V_{\text{ICM}}$	Common-Mode Input Voltage		●	0.3	1.2	2.2	V
$I_{\text{ICM}}$	Common-Mode Input Current	$V_{\text{IN}+} = V_{\text{IN}-} = 0\text{V}$ to $OV_{\text{DD}}$	●	-10	10	$\mu\text{A}$	
$V_{\text{OD}}$	Differential Output Voltage	$R_{\text{L}} = 100\Omega$ Differential Termination	●	275	350	425	mV
$V_{\text{OCM}}$	Common-Mode Output Voltage	$R_{\text{L}} = 100\Omega$ Differential Termination	●	1.1	1.2	1.3	V
$I_{\text{OZ}}$	Hi-Z Output Leakage Current	$V_{\text{OUT}} = 0\text{V}$ to $OV_{\text{DD}}$	●	-10	10	$\mu\text{A}$	

## POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage		●	7.5		38	V
$V_{EE}$	Supply Voltage		●	-16.5		0	V
$V_{CC} - V_{EE}$	Supply Voltage Difference		●	10		38	V
$V_{DD}$	Supply Voltage		●	4.75	5.00	5.25	V
$I_{VCC}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled (Note 17)	●		3.4	3.9	mA
		Acquisition Mode (Note 17)	●		5.7	6.9	mA
		Nap Mode	●		1.5	1.8	mA
		Power Down Mode	●		5	15	$\mu\text{A}$
$I_{VEE}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled (Note 17)	●	-4.1	-3.2		mA
		Acquisition Mode (Note 17)	●	-7.1	-5.6		mA
		Nap Mode	●	-2	-1.4		mA
		Power Down Mode	●	-15	-4		$\mu\text{A}$

### CMOS I/O Mode

$OV_{DD}$	Supply Voltage		●	1.71		5.25	V
$I_{VDD}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled	●		14.3	16	mA
		350ksps Sample Rate, 4 Channels Enabled, $V_{REFBUF} = 5\text{V}$ (Note 15)	●		12.6	14.3	mA
		Acquisition Mode	●		1.8	2.5	mA
		Nap Mode	●		1.6	2.2	mA
		Power Down Mode (C-Grade and I-Grade)	●		84	300	$\mu\text{A}$
	Power Down Mode (H-Grade)	●		84	750	$\mu\text{A}$	
$I_{OVDD}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled ( $C_L = 25\text{pF}$ )	●		1.8	2.6	mA
		Acquisition or Nap Mode	●		1	20	$\mu\text{A}$
		Power Down Mode	●		1	20	$\mu\text{A}$
$P_D$	Power Dissipation	350ksps Sample Rate, 4 Channels Enabled	●		175	207	mW
		Acquisition Mode	●		179	223	mW
		Nap Mode	●		52	68	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.56	2	mW
		Power Down Mode (H-Grade)	●		0.56	4.3	mW

### LVDS I/O Mode

$OV_{DD}$	Supply Voltage		●	2.375		5.25	V
$I_{VDD}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled	●		16.4	18.1	mA
		350ksps Sample Rate, 4 Channels Enabled, $V_{REFBUF} = 5\text{V}$ (Note 15)	●		14.9	16.7	mA
		Acquisition Mode	●		3.4	4.2	mA
		Nap Mode	●		3.2	4	mA
		Power Down Mode (C-Grade and I-Grade)	●		84	300	$\mu\text{A}$
	Power Down Mode (H-Grade)	●		84	750	$\mu\text{A}$	
$I_{OVDD}$	Supply Current	350ksps Sample Rate, 4 Channels Enabled ( $R_L = 100\Omega$ )	●		7.5	8.7	mA
		Acquisition or Nap Mode ( $R_L = 100\Omega$ )	●		7	8.2	mA
		Power Down Mode	●		1	20	$\mu\text{A}$
$P_D$	Power Dissipation	350ksps Sample Rate, 4 Channels Enabled	●		200	232	mW
		Acquisition Mode	●		204	252	mW
		Nap Mode	●		77	98	mW
		Power Down Mode (C-Grade and I-Grade)	●		0.56	2	mW
		Power Down Mode (H-Grade)	●		0.56	4.3	mW

## ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 9)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$f_{\text{SAMPL}}$	Maximum Sampling Frequency	4 Channels Enabled	●		350	ksps
		3 Channels Enabled	●		425	ksps
		2 Channels Enabled	●		550	ksps
		1 Channel Enabled	●		800	ksps
$t_{\text{CYC}}$	Time Between Conversions	4 Channels Enabled, $f_{\text{SAMPL}} = 350\text{ksps}$	●	2855		ns
		3 Channels Enabled, $f_{\text{SAMPL}} = 425\text{ksps}$	●	2350		ns
		2 Channels Enabled, $f_{\text{SAMPL}} = 550\text{ksps}$	●	1815		ns
		1 Channel Enabled, $f_{\text{SAMPL}} = 800\text{ksps}$	●	1250		ns
$t_{\text{CONV}}$	Conversion Time	N Channels Enabled, $1 \leq N \leq 4$	●	$450 \cdot N$	$500 \cdot N$ $550 \cdot N$	ns
$t_{\text{ACQ}}$	Acquisition Time ( $t_{\text{ACQ}} = t_{\text{CYC}} - t_{\text{CONV}} - t_{\text{BUSY LH}}$ )	4 Channels Enabled, $f_{\text{SAMPL}} = 350\text{ksps}$	●	625	835	ns
		3 Channels Enabled, $f_{\text{SAMPL}} = 425\text{ksps}$	●	670	830	ns
		2 Channels Enabled, $f_{\text{SAMPL}} = 550\text{ksps}$	●	685	795	ns
		1 Channel Enabled, $f_{\text{SAMPL}} = 800\text{ksps}$	●	670	730	ns
$t_{\text{CNVH}}$	CNV High Time		●	40		ns
$t_{\text{CNVL}}$	CNV Low Time		●	750		ns
$t_{\text{BUSY LH}}$	CNV $\uparrow$ to BUSY Delay	$C_L = 25\text{pF}$	●		30	ns
$t_{\text{QUIET}}$	Digital I/O Quiet Time from CNV $\uparrow$		●	20		ns
$t_{\text{PDH}}$	PD High Time		●	40		ns
$t_{\text{PDL}}$	PD Low Time		●	40		ns
$t_{\text{WAKE}}$	REFBUF Wake-Up Time	$C_{\text{REFBUF}} = 47\mu\text{F}$ , $C_{\text{REFIN}} = 0.1\mu\text{F}$			200	ms

### CMOS I/O Mode

$t_{\text{SCKI}}$	SCKI Period	(Notes 18, 19)	●	10		ns
$t_{\text{SCKIH}}$	SCKI High Time		●	4		ns
$t_{\text{SCKIL}}$	SCKI Low Time		●	4		ns
$t_{\text{SSDISCKI}}$	SDI Setup Time from SCKI $\uparrow$	(Note 18)	●	2		ns
$t_{\text{HSDISCKI}}$	SDI Hold Time from SCKI $\uparrow$	(Note 18)	●	1		ns
$t_{\text{DSDOSCKI}}$	SDO Data Valid Delay from SCKI $\uparrow$	$C_L = 25\text{pF}$ (Note 18)	●		7.5	ns
$t_{\text{HSDOSCKI}}$	SDO Remains Valid Delay from SCKI $\uparrow$	$C_L = 25\text{pF}$ (Note 18)	●	1.5		ns
$t_{\text{SKEW}}$	SDO to SCKO Skew	(Note 18)	●	-1	0	1
$t_{\text{DSDOBUSYL}}$	SDO Data Valid Delay from BUSY $\downarrow$	$C_L = 25\text{pF}$ (Note 18)	●	0		ns
$t_{\text{EN}}$	Bus Enable Time After $\overline{\text{CS}}\downarrow$	(Note 18)	●		15	ns
$t_{\text{DIS}}$	Bus Relinquish Time After $\overline{\text{CS}}\uparrow$	(Note 18)	●		15	ns

### LVDS I/O Mode

$t_{\text{SCKI}}$	SCKI Period	(Note 20)	●	4		ns
$t_{\text{SCKIH}}$	SCKI High Time	(Note 20)	●	1.5		ns
$t_{\text{SCKIL}}$	SCKI Low Time	(Note 20)	●	1.5		ns
$t_{\text{SSDISCKI}}$	SDI Setup Time from SCKI	(Notes 11, 20)	●	1.2		ns
$t_{\text{HSDISCKI}}$	SDI Hold Time from SCKI	(Notes 11, 20)	●	-0.2		ns
$t_{\text{DSDOSCKI}}$	SDO Data Valid Delay from SCKI	(Notes 11, 20)	●		6	ns
$t_{\text{HSDOSCKI}}$	SDO Remains Valid Delay from SCKI	(Notes 11, 20)	●	1		ns
$t_{\text{SKEW}}$	SDO to SCKO Skew	(Note 11)	●	-0.4	0	0.4
$t_{\text{DSDOBUSYL}}$	SDO Data Valid Delay from BUSY $\downarrow$	(Note 11)	●	0		ns
$t_{\text{EN}}$	Bus Enable Time After $\overline{\text{CS}}\downarrow$		●		50	ns
$t_{\text{DIS}}$	Bus Relinquish Time After $\overline{\text{CS}}\uparrow$		●		15	ns



## ADC TIMING CHARACTERISTICS

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:**  $V_{DDLBYP}$  is the output of an internal voltage regulator, and should only be connected to a 2.2 $\mu$ F ceramic capacitor to bypass the pin to GND, as described in the Pin Functions section. Do not connect this pin to any external circuitry.

**Note 4:** When these pin voltages are taken below  $V_{EE}$  or above  $V_{CC}$ , they will be clamped by internal diodes. This product can handle input currents of up to 100mA below  $V_{EE}$  or above  $V_{CC}$  without latchup.

**Note 5:** When these pin voltages are taken below GND or above  $V_{DD}$  or  $OV_{DD}$ , they will be clamped by internal diodes. This product can handle currents of up to 100mA below GND or above  $V_{DD}$  or  $OV_{DD}$  without latchup.

**Note 6:**  $-16.5V \leq V_{EE} \leq 0V$ ,  $7.5V \leq V_{CC} \leq 38V$ ,  $10V \leq (V_{CC} - V_{EE}) \leq 38V$ ,  $V_{DD} = 5V$ , unless otherwise specified.

**Note 7:** Recommended operating conditions.

**Note 8:** Exceeding these limits on any channel may corrupt conversion results on other channels. Driving an analog input above  $V_{CC}$  on any channel up to 10mA will not affect conversion results on other channels. Driving an analog input below  $V_{EE}$  may corrupt conversion results on other channels. Refer to Applications Information section for further details. Refer to Absolute Maximum Ratings section for pin voltage limits related to device reliability.

**Note 9:**  $V_{CC} = 15V$ ,  $V_{EE} = -15V$ ,  $V_{DD} = 5V$ ,  $OV_{DD} = 2.5V$ ,  $f_{SAMPL} = 350ksps$ , internal reference and buffer, true bipolar input signal drive in bipolar SoftSpan ranges, unipolar signal drive in unipolar SoftSpan ranges, unless otherwise specified.

**Note 10:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 11:** Guaranteed by design, not subject to test.

**Note 12:** For bipolar SoftSpan ranges 7, 6, 3, and 2, zero-scale error is the offset voltage measured from  $-0.5LSB$  when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Full-scale error for these SoftSpan ranges is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. For unipolar SoftSpan ranges 5, 4, and 1, zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001. Full-scale error for these SoftSpan ranges is the worst-case deviation of the last code transition from ideal and includes the effect of offset error.

**Note 13:** All specifications in dB are referred to a full-scale input in the relevant SoftSpan input range, except for crosstalk, which is referred to the crosstalk injection signal amplitude.

**Note 14:** Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

**Note 15:** When REFBUF is overdriven, the internal reference buffer must be disabled by setting REFIN = 0V.

**Note 16:**  $I_{REFBUF}$  varies proportionally with sample rate and the number of active channels.

**Note 17:** Portions of the analog input circuitry are powered down during conversion, reducing  $I_{VCC}$  and  $I_{VEE}$ . Refer to Applications Information section for more details.

**Note 18:** Parameter tested and guaranteed at  $OV_{DD} = 1.71V$ ,  $OV_{DD} = 2.5V$ , and  $OV_{DD} = 5.25V$ .

**Note 19:** A  $t_{SCKI}$  period of 10ns minimum allows a shift clock frequency of up to 100MHz for rising edge capture.

**Note 20:**  $V_{ICM} = 1.2V$ ,  $V_{ID} = 350mV$  for LVDS differential input pairs.

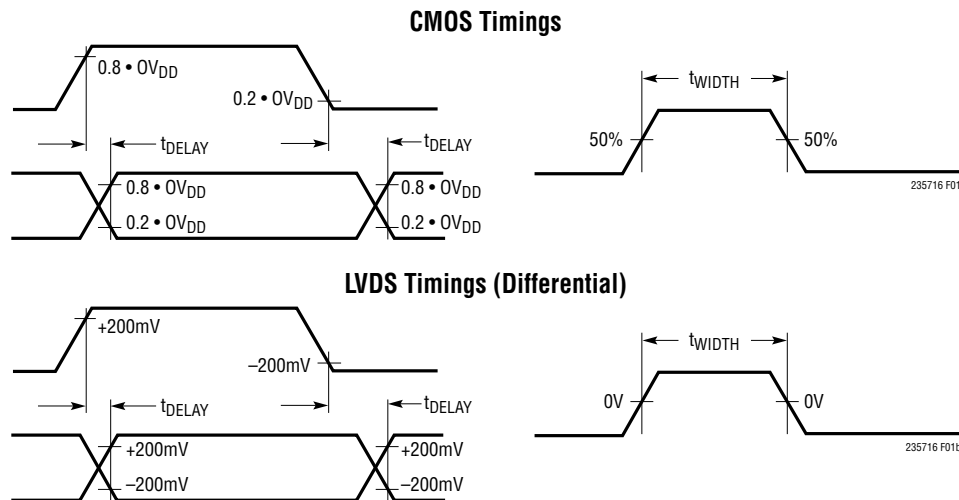
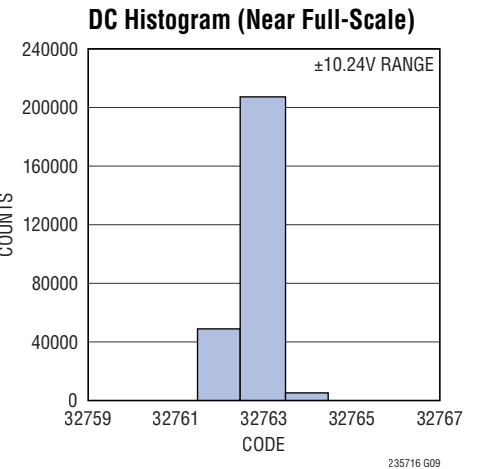
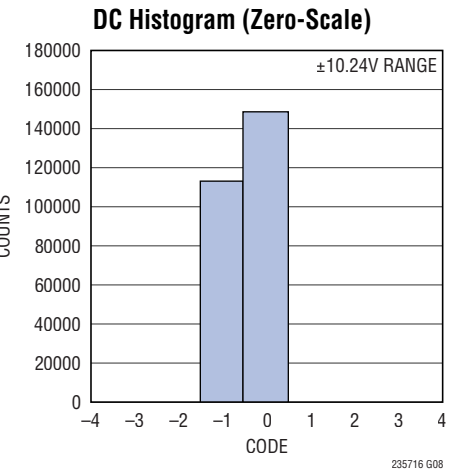
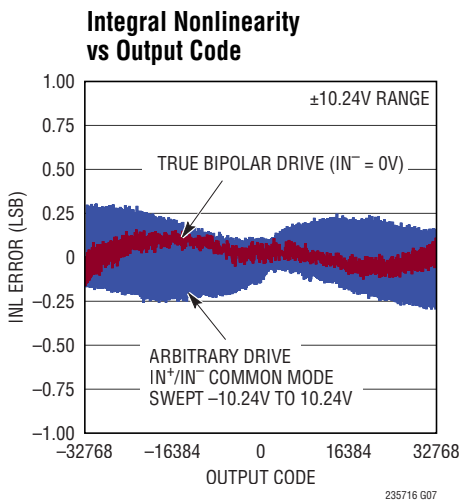
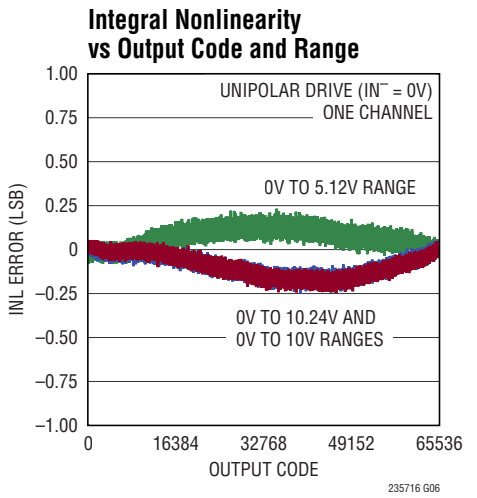
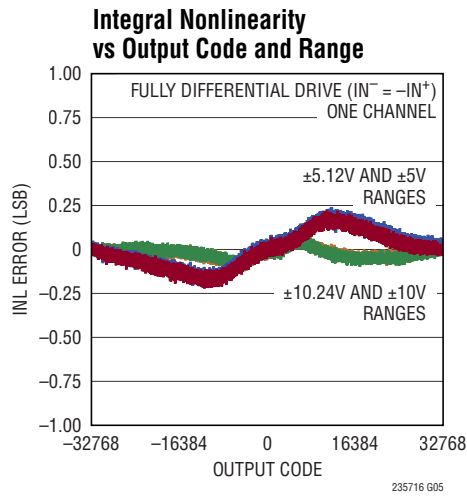
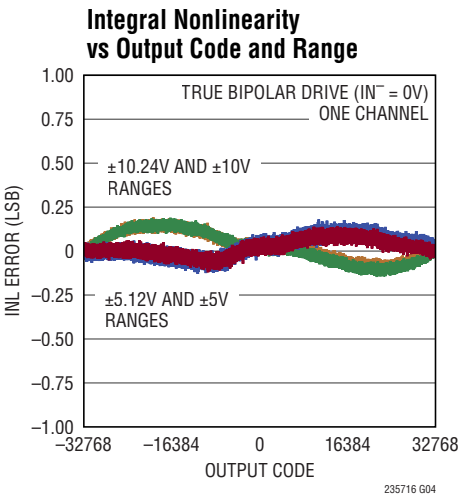
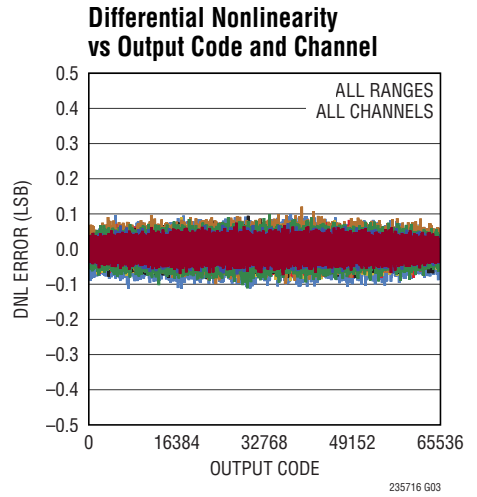
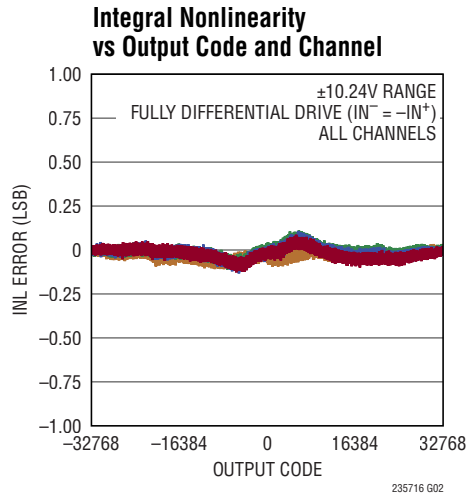
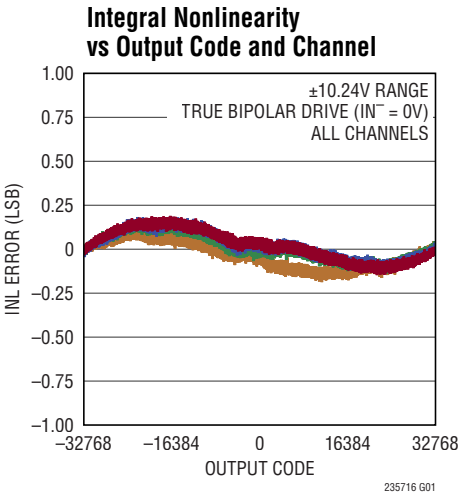


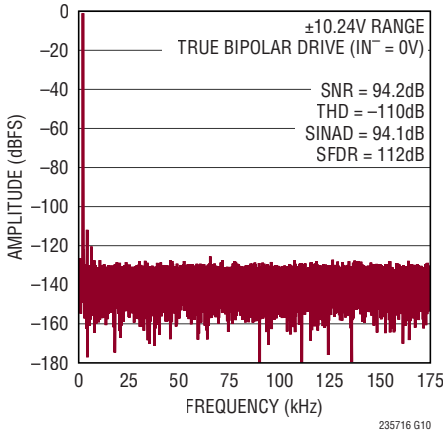
Figure 1. Voltage Levels for Timing Specifications

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $OV_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ),  $f_{SAMPL} = 350\text{ksps}$ , unless otherwise noted.



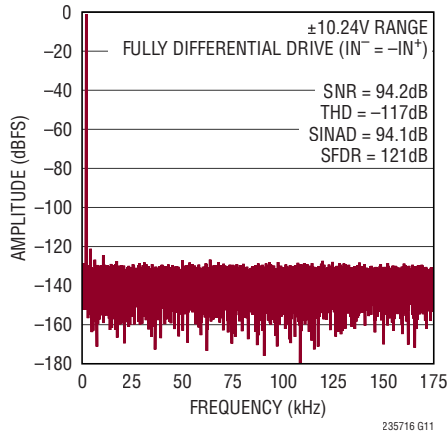
## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{CC} = +15\text{V}$ , $V_{EE} = -15\text{V}$ , $V_{DD} = 5\text{V}$ , $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ), $f_{SMPL} = 350\text{ksps}$ , unless otherwise noted.

**32k Point FFT  $f_{SMPL} = 350\text{ksps}$ ,  $f_{IN} = 2\text{kHz}$**



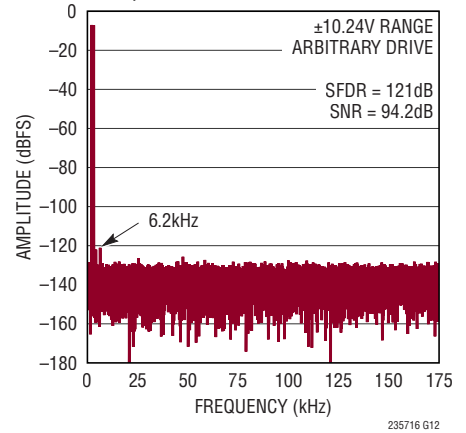
235716 G10

**32k Point FFT  $f_{SMPL} = 350\text{ksps}$ ,  $f_{IN} = 2\text{kHz}$**



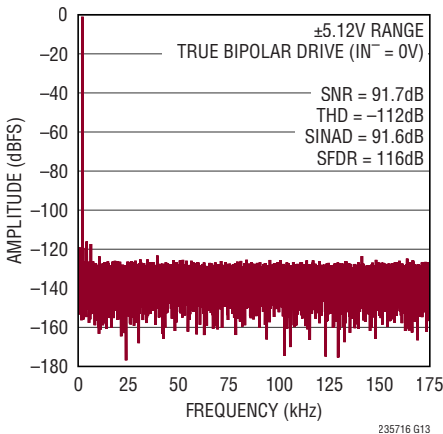
235716 G11

**32k Point Arbitrary Two-Tone FFT  $f_{SMPL} = 350\text{ksps}$ ,  $IN^+ = -7\text{dBFS}$  2kHz Sine,  $IN^- = -7\text{dBFS}$  3.1kHz Sine**



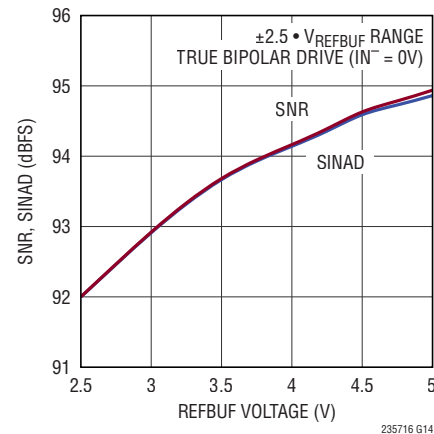
235716 G12

**32k Point FFT  $f_{SMPL} = 350\text{ksps}$ ,  $f_{IN} = 2\text{kHz}$**



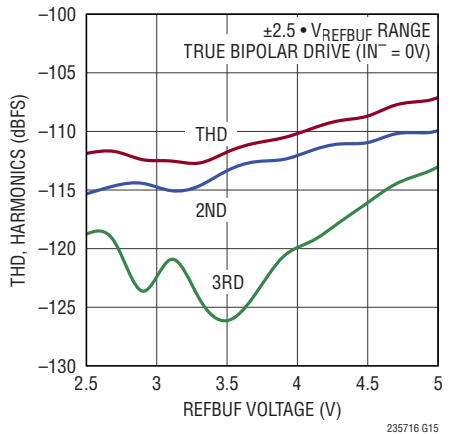
235716 G13

**SNR, SINAD vs  $V_{REFBUF}$ ,  $f_{IN} = 2\text{kHz}$**



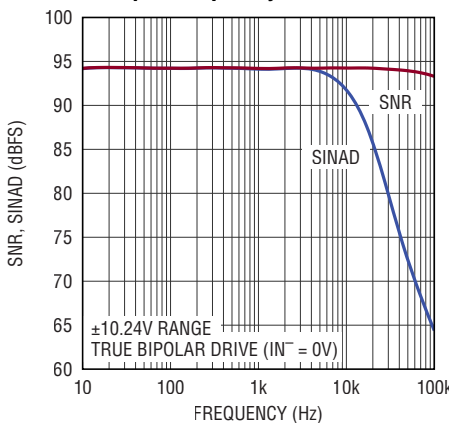
235716 G14

**THD, Harmonics vs  $V_{REFBUF}$ ,  $f_{IN} = 2\text{kHz}$**



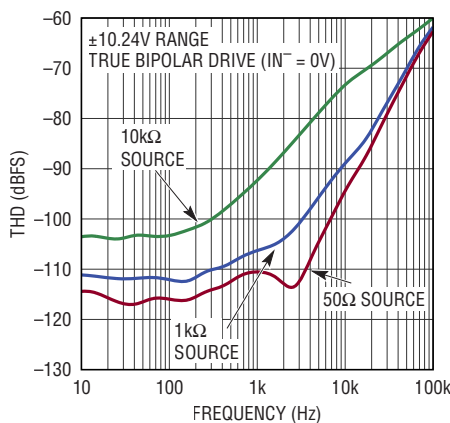
235716 G15

**SNR, SINAD vs Input Frequency**



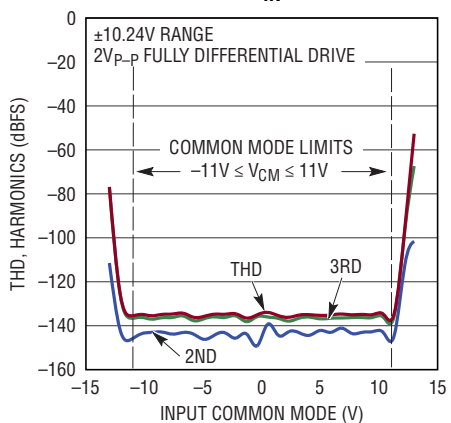
235716 G16

**THD vs Input Frequency and Source Resistance**



235716 G17

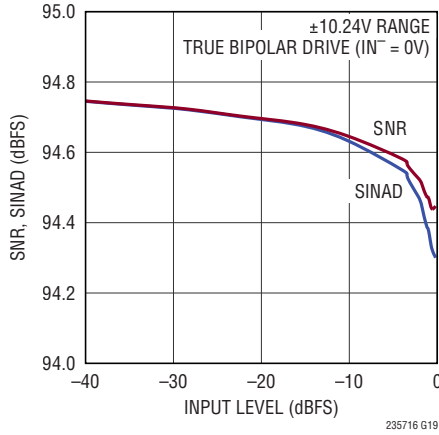
**THD, Harmonics vs Input Common Mode,  $f_{IN} = 2\text{kHz}$**



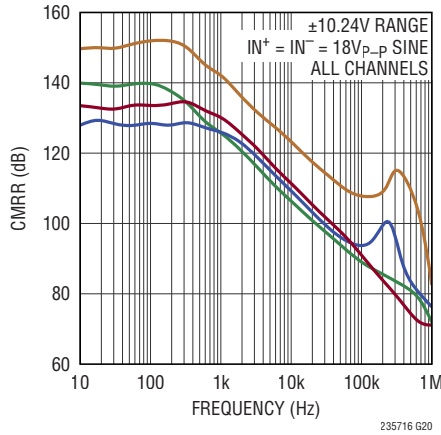
235716 G18

**TYPICAL PERFORMANCE CHARACTERISTICS**  $T_A = 25^\circ\text{C}$ ,  $V_{CC} = +15\text{V}$ ,  $V_{EE} = -15\text{V}$ ,  $V_{DD} = 5\text{V}$ ,  $0V_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ),  $f_{SAMPL} = 350\text{ksps}$ , unless otherwise noted.

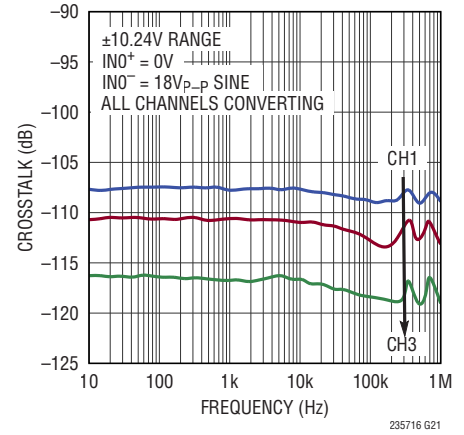
**SNR, SINAD vs Input Level,**  
 $f_{IN} = 2\text{kHz}$



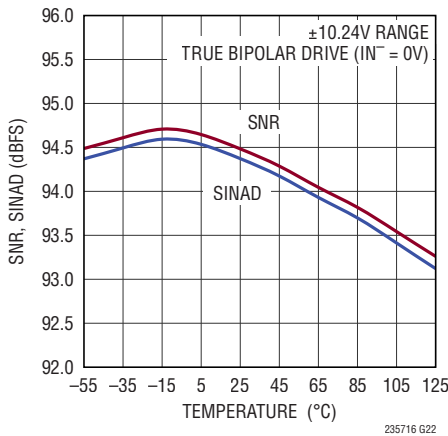
**CMRR vs Input Frequency and Channel**



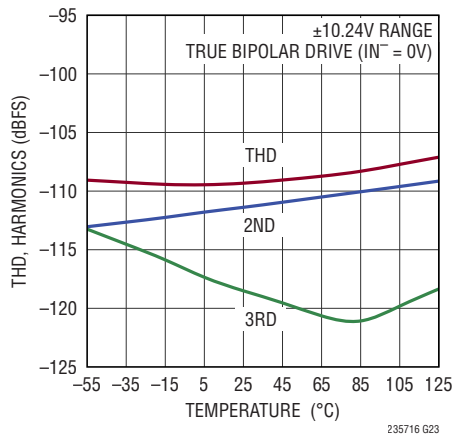
**Crosstalk vs Input Frequency and Channel**



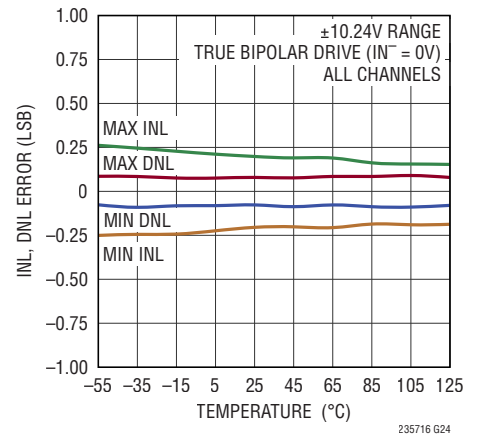
**SNR, SINAD vs Temperature,**  
 $f_{IN} = 2\text{kHz}$



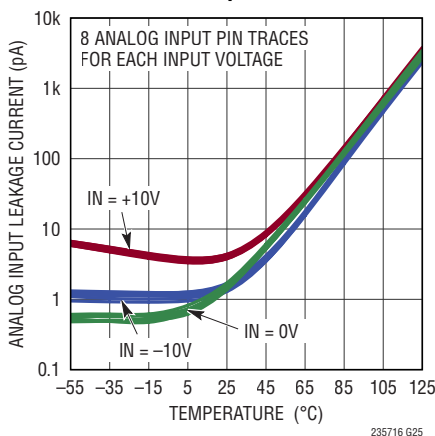
**THD, Harmonics vs Temperature,**  
 $f_{IN} = 2\text{kHz}$



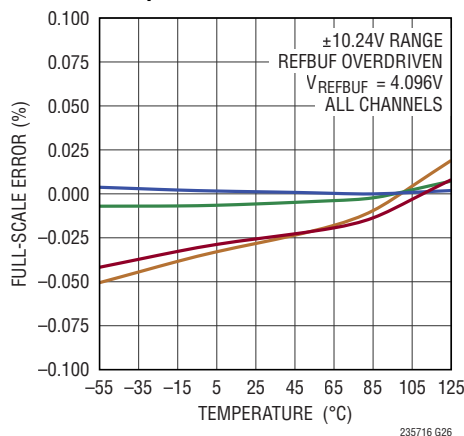
**INL, DNL vs Temperature**



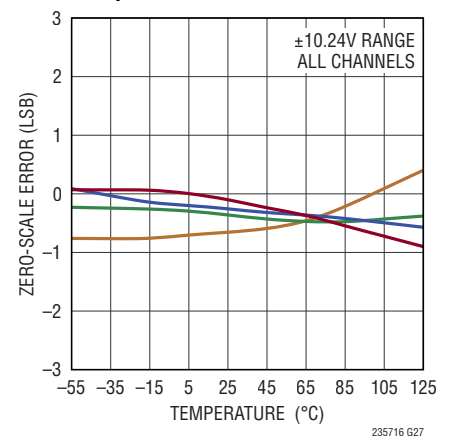
**Analog Input Leakage Current vs Temperature**



**Positive Full-Scale Error vs Temperature and Channel**

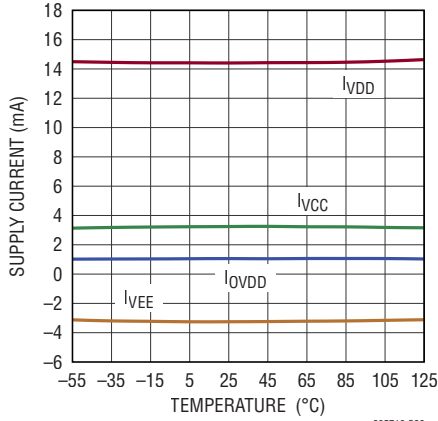


**Zero-Scale Error vs Temperature and Channel**

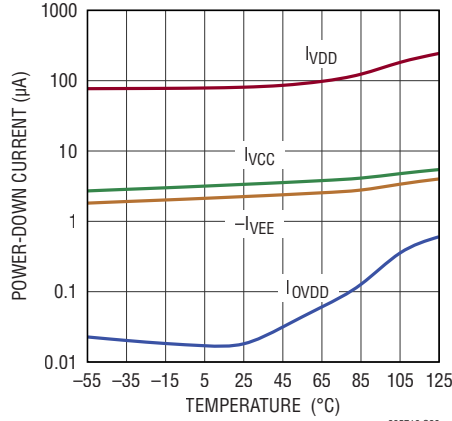


## TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25^\circ\text{C}$ , $V_{CC} = +15\text{V}$ , $V_{EE} = -15\text{V}$ , $V_{DD} = 5\text{V}$ , $OV_{DD} = 2.5\text{V}$ , Internal Reference and Buffer ( $V_{REFBUF} = 4.096\text{V}$ ), $f_{SMPL} = 350\text{kpsps}$ , unless otherwise noted.

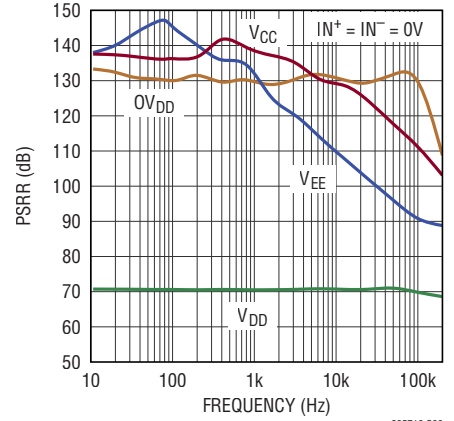
**Supply Current vs Temperature**



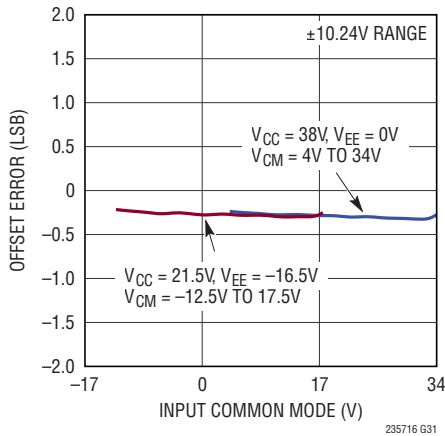
**Power-Down Current vs Temperature**



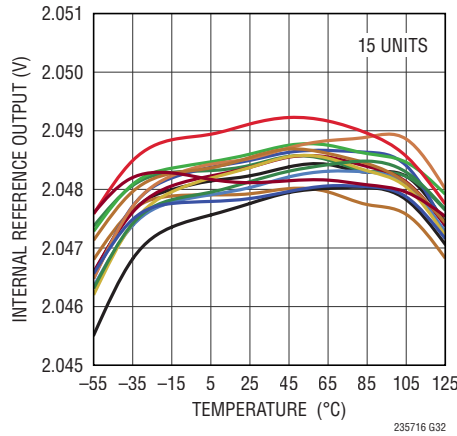
**PSRR vs Frequency**



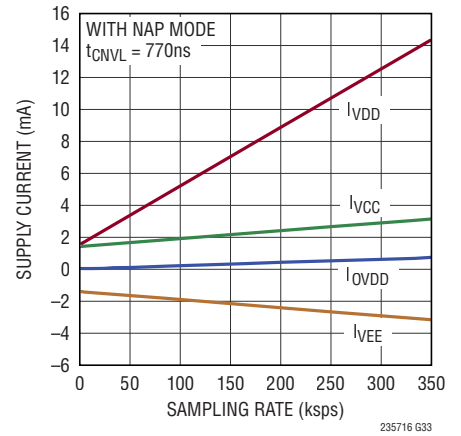
**Offset Error vs Input Common Mode**



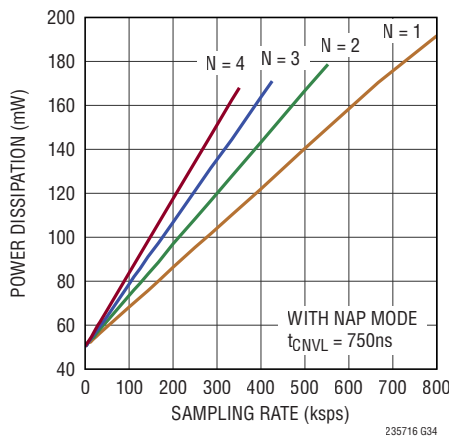
**Internal Reference Output vs Temperature**



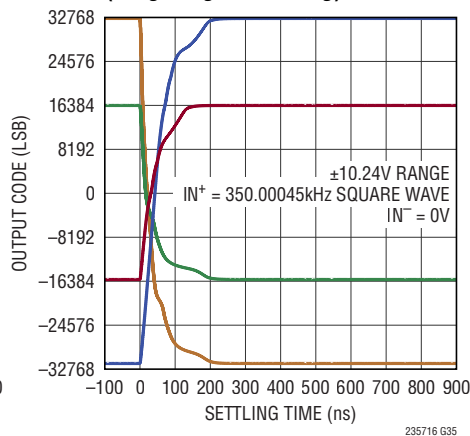
**Supply Current vs Sampling Rate**



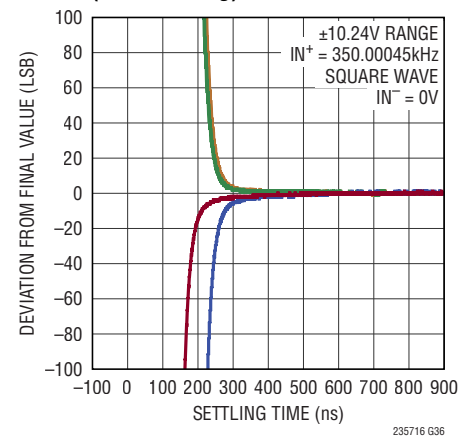
**Power Dissipation vs Sampling Rate, N-Channels Enabled**



**Step Response (Large-Signal Settling)**



**Step Response (Fine Settling)**



## PIN FUNCTIONS

### Pins that are the Same for All Digital I/O Modes

#### IN0<sup>+</sup>/IN0<sup>-</sup> to IN3<sup>+</sup>/IN3<sup>-</sup> (Pins 14/13, 10/9, 4/3 and 48/47):

Positive and Negative Analog Inputs, Channels 0 to 3. The converter simultaneously samples and digitizes ( $V_{IN+} - V_{IN-}$ ) for all channels. Wide input common mode range ( $V_{EE} + 4V \leq V_{CM} \leq V_{CC} - 4V$ ) and high common mode rejection allow the inputs to accept a wide variety of signal swings. Full-scale input range is determined by the channel's SoftSpan configuration.

**GND (Pins 1, 2, 5, 6, 7, 8, 11, 12, 15, 18, 20, 25, 30, 36, 41, 44, 46):** Ground. Solder all GND pins to a solid ground plane.

**V<sub>CC</sub> (Pin 16):** Positive High Voltage Power Supply. The range of  $V_{CC}$  is 7.5V to 38V with respect to GND and 10V to 38V with respect to  $V_{EE}$ . Bypass  $V_{CC}$  to GND close to the pin with a 0.1 $\mu$ F ceramic capacitor.

**V<sub>EE</sub> (Pins 17, 45):** Negative High Voltage Power Supply. The range of  $V_{EE}$  is 0V to -16.5V with respect to GND and -10V to -38V with respect to  $V_{CC}$ . Connect Pins 17 and 45 together and bypass the  $V_{EE}$  network to GND close to Pin 17 with a 0.1 $\mu$ F ceramic capacitor. In applications where  $V_{EE}$  is shorted to GND, this capacitor may be omitted.

**REFIN (Pin 19):** Bandgap Reference Output/Reference Buffer Input. An internal bandgap reference nominally outputs 2.048V on this pin. An internal reference buffer amplifies  $V_{REFIN}$  to create the converter master reference voltage  $V_{REFBUF} = 2 \cdot V_{REFIN}$  on the REFBUF pin. When using the internal reference, bypass REFIN to GND (Pin 20) close to the pin with a 0.1 $\mu$ F ceramic capacitor to filter the bandgap output noise. If more accuracy is desired, overdrive REFIN with an external reference in the range of 1.25V to 2.2V. Do not load this pin when internal reference is used.

**REFBUF (Pin 21):** Internal Reference Buffer Output. An internal reference buffer amplifies  $V_{REFIN}$  to create the converter master reference voltage  $V_{REFBUF} = 2 \cdot V_{REFIN}$  on this pin, nominally 4.096V when using the internal bandgap reference. Bypass REFBUF to GND (Pin 20) close to the pin with a 47 $\mu$ F ceramic capacitor. The internal ref-

erence buffer may be disabled by grounding its input at REFIN. With the buffer disabled, overdrive REFBUF with an external reference voltage in the range of 2.5V to 5V. When using the internal reference buffer, limit the loading of any external circuitry connected to REFBUF to less than 200 $\mu$ A. Using a high input impedance amplifier to buffer  $V_{REFBUF}$  to any external circuits is recommended.

**PD (Pin 22):** Power Down Input. When this pin is brought high, the LTC2357-16 is powered down and subsequent conversion requests are ignored. If this occurs during a conversion, the device powers down once the conversion completes. If this pin is brought high twice without an intervening conversion, an internal global reset is initiated, equivalent to a power-on-reset event. Logic levels are determined by  $OV_{DD}$ .

**LVDS/CMOS (Pin 23):** I/O Mode Select. Tie this pin to  $OV_{DD}$  to select LVDS I/O mode, or to ground to select CMOS I/O mode. Logic levels are determined by  $OV_{DD}$ .

**CNV (Pin 24):** Conversion Start Input. A rising edge on this pin puts the internal sample-and-holds into the hold mode and initiates a new conversion. CNV is not gated by  $\overline{CS}$ , allowing conversions to be initiated independent of the state of the serial I/O bus.

**BUSY (Pin 38):** Busy Output. The BUSY signal indicates that a conversion is in progress. This pin transitions low-to-high at the start of each conversion and stays high until the conversion is complete. Logic levels are determined by  $OV_{DD}$ .

**V<sub>DDLBY</sub>P (Pin 40):** Internal 2.5V Regulator Bypass Pin. The voltage on this pin is generated via an internal regulator operating off of  $V_{DD}$ . This pin must be bypassed to GND close to the pin with a 2.2 $\mu$ F ceramic capacitor. Do not connect this pin to any external circuitry.

**V<sub>DD</sub> (Pins 42, 43):** 5V Power Supply. The range of  $V_{DD}$  is 4.75V to 5.25V. Connect Pins 42 and 43 together and bypass the  $V_{DD}$  network to GND with a shared 0.1 $\mu$ F ceramic capacitor close to the pins.

## PIN FUNCTIONS

### CMOS I/O Mode

**SDI<sup>+</sup>, SDO<sup>-</sup> (Pins 26 and 35):** LVDS Input and Output. In CMOS I/O mode, these pins are Hi-Z.

**SDO0 to SDO3 (Pins 27, 28, 33 and 34):** CMOS Serial Data Outputs, Channels 0 to 3. The most recent conversion result along with channel configuration information is clocked out onto the SDO pins on each rising edge of SCKI. Output data formatting is described in the Digital Interface section. Leave unused SDO outputs unconnected. Logic levels are determined by  $OV_{DD}$ .

**SCKI (Pin 29):** CMOS Serial Clock Input. Drive SCKI with the serial I/O clock. SCKI rising edges latch serial data in on SDI and clock serial data out on SDO0 to SDO3. For standard SPI bus operation, capture output data at the receiver on rising edges of SCKI. SCKI is allowed to idle either high or low. Logic levels are determined by  $OV_{DD}$ .

**$OV_{DD}$  (Pin 31):** I/O Interface Power Supply. In CMOS I/O mode, the range of  $OV_{DD}$  is 1.71V to 5.25V. Bypass  $OV_{DD}$  to GND (Pin 30) close to the pin with a 0.1 $\mu$ F ceramic capacitor.

**SCKO (Pin 32):** CMOS Serial Clock Output. SCKI rising edges trigger transitions on SCKO that are skew-matched to the serial output data streams on SDO0 to SDO3. The resulting SCKO frequency is half that of SCKI. Rising and falling edges of SCKO may be used to capture SDO data at the receiver (FPGA) in double data rate (DDR) fashion. For standard SPI bus operation, SCKO is not used and should be left unconnected. SCKO is forced low at the falling edge of BUSY. Logic levels are determined by  $OV_{DD}$ .

**SDI (Pin 37):** CMOS Serial Data Input. Drive this pin with the desired 12-bit SoftSpan configuration word (see Table 1a), latched on the rising edges of SCKI. If all channels will be configured to operate only in SoftSpan 7, tie SDI to  $OV_{DD}$ . Logic levels are determined by  $OV_{DD}$ .

**$\overline{CS}$  (Pin 39):** Chip Select Input. The serial data I/O bus is enabled when  $\overline{CS}$  is low and is disabled and Hi-Z when  $\overline{CS}$  is high.  $\overline{CS}$  also gates the external shift clock, SCKI. Logic levels are determined by  $OV_{DD}$ .

### LVDS I/O Mode

**SDI<sup>+</sup>/SDI<sup>-</sup> (Pins 26/27):** LVDS Positive and Negative Serial Data Input. Differentially drive SDI<sup>+</sup>/SDI<sup>-</sup> with the desired 12-bit SoftSpan configuration word (see Table 1a), latched on both the rising and falling edges of SCKI<sup>+</sup>/SCKI<sup>-</sup>. The SDI<sup>+</sup>/SDI<sup>-</sup> input pair is internally terminated with a 100 $\Omega$  differential resistor when  $\overline{CS}$  is low.

**SCKI<sup>+</sup>/SCKI<sup>-</sup> (Pins 28/29):** LVDS Positive and Negative Serial Clock Input. Differentially drive SCKI<sup>+</sup>/SCKI<sup>-</sup> with the serial I/O clock. SCKI<sup>+</sup>/SCKI<sup>-</sup> rising and falling edges latch serial data in on SDI<sup>+</sup>/SDI<sup>-</sup> and clock serial data out on SDO<sup>+</sup>/SDO<sup>-</sup>. Idle SCKI<sup>+</sup>/SCKI<sup>-</sup> low, including when transitioning  $\overline{CS}$ . The SCKI<sup>+</sup>/SCKI<sup>-</sup> input pair is internally terminated with a 100 $\Omega$  differential resistor when  $\overline{CS}$  is low.

**$OV_{DD}$  (Pin 31):** I/O Interface Power Supply. In LVDS I/O mode, the range of  $OV_{DD}$  is 2.375V to 5.25V. Bypass  $OV_{DD}$  to GND (Pin 30) close to the pin with a 0.1 $\mu$ F ceramic capacitor.

**SCKO<sup>+</sup>/SCKO<sup>-</sup> (Pins 32/33):** LVDS Positive and Negative Serial Clock Output. SCKO<sup>+</sup>/SCKO<sup>-</sup> outputs a copy of the input serial I/O clock received on SCKI<sup>+</sup>/SCKI<sup>-</sup>, skew-matched with the serial output data stream on SDO<sup>+</sup>/SDO<sup>-</sup>. Use the rising and falling edges of SCKO<sup>+</sup>/SCKO<sup>-</sup> to capture SDO<sup>+</sup>/SDO<sup>-</sup> data at the receiver (FPGA). The SCKO<sup>+</sup>/SCKO<sup>-</sup> output pair must be differentially terminated with a 100 $\Omega$  resistor at the receiver (FPGA).

**SDO<sup>+</sup>/SDO<sup>-</sup> (Pins 34/35):** LVDS Positive and Negative Serial Data Output. The most recent conversion result along with channel configuration information is clocked out onto SDO<sup>+</sup>/SDO<sup>-</sup> on both rising and falling edges of SCKI<sup>+</sup>/SCKI<sup>-</sup>, beginning with channel 0. The SDO<sup>+</sup>/SDO<sup>-</sup> output pair must be differentially terminated with a 100 $\Omega$  resistor at the receiver (FPGA).

**SDI (Pin 37):** CMOS Serial Data. In LVDS I/O mode, this pin is Hi-Z.

**$\overline{CS}$  (Pin 39):** Chip Select Input. The serial data I/O bus is enabled when  $\overline{CS}$  is low, and is disabled and Hi-Z when  $\overline{CS}$  is high.  $\overline{CS}$  also gates the external shift clock, SCKI<sup>+</sup>/SCKI<sup>-</sup>. The internal 100 $\Omega$  differential termination resistors on the SCKI<sup>+</sup>/SCKI<sup>-</sup> and SDI<sup>+</sup>/SDI<sup>-</sup> input pairs are disabled when  $\overline{CS}$  is high. Logic levels are determined by  $OV_{DD}$ .

## CONFIGURATION TABLES

**Table 1a. SoftSpan Configuration Table. Use This Table with Table 1b to Choose Independent Binary SoftSpan Codes SS[2:0] for Each Channel Based on Desired Analog Input Range. Combine SoftSpan Codes to Form 12-Bit SoftSpan Configuration Word S[11:0]. Use Serial Interface to Write SoftSpan Configuration Word to LTC2357-16, as shown in Figure 18**

BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE	FULL SCALE RANGE	BINARY FORMAT OF CONVERSION RESULT
111	$\pm 2.5 \cdot V_{REFBUF}$	$5 \cdot V_{REFBUF}$	Two's Complement
110	$\pm 2.5 \cdot V_{REFBUF}/1.024$	$5 \cdot V_{REFBUF}/1.024$	Two's Complement
101	0V to $2.5 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Straight Binary
100	0V to $2.5 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Straight Binary
011	$\pm 1.25 \cdot V_{REFBUF}$	$2.5 \cdot V_{REFBUF}$	Two's Complement
010	$\pm 1.25 \cdot V_{REFBUF}/1.024$	$2.5 \cdot V_{REFBUF}/1.024$	Two's Complement
001	0V to $1.25 \cdot V_{REFBUF}$	$1.25 \cdot V_{REFBUF}$	Straight Binary
000	Channel Disabled	Channel Disabled	All Zeros

**Table 1b. Reference Configuration Table. The LTC2357-16 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage,  $V_{REFBUF}$**

REFERENCE CONFIGURATION	$V_{REFIN}$	$V_{REFBUF}$	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
Internal Reference with Internal Buffer	2.048V	4.096V	111	$\pm 10.24V$
			110	$\pm 10V$
			101	0V to 10.24V
			100	0V to 10V
			011	$\pm 5.12V$
			010	$\pm 5V$
			001	0V to 5.12V
External Reference with Internal Buffer (REFIN Pin Externally Overdriven)	1.25V (Min Value)	2.5V	111	$\pm 6.25V$
			110	$\pm 6.104V$
			101	0V to 6.25V
			100	0V to 6.104V
			011	$\pm 3.125V$
			010	$\pm 3.052V$
			001	0V to 3.125V
	2.2V (Max Value)	4.4V	111	$\pm 11V$
			110	$\pm 10.742V$
			101	0V to 11V
			100	0V to 10.742V
			011	$\pm 5.5V$
			010	$\pm 5.371V$
			001	0V to 5.5V



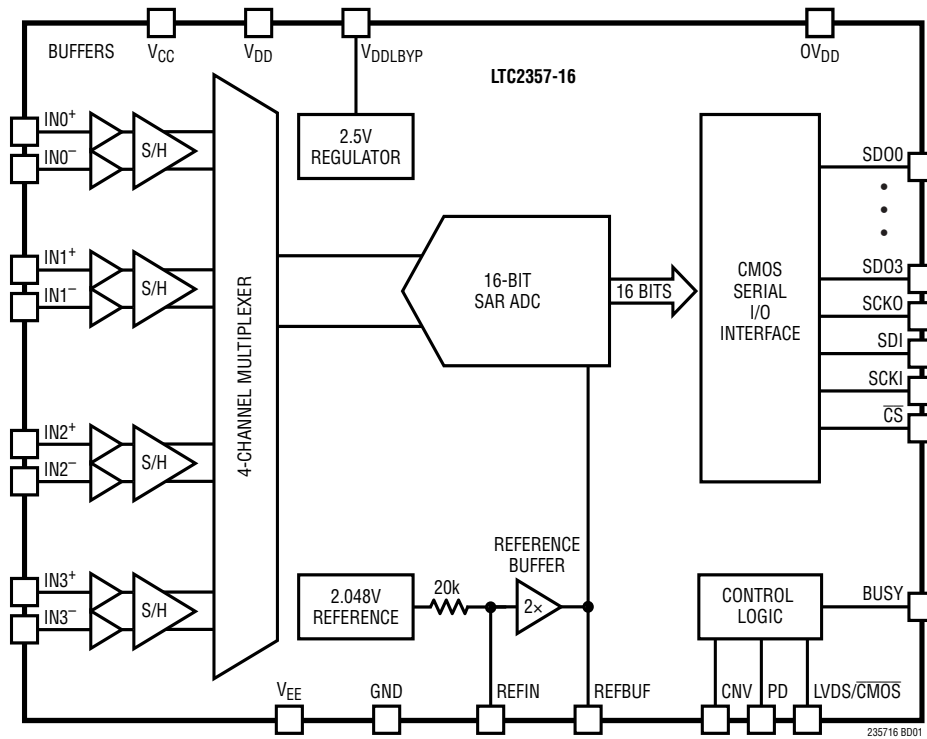
## CONFIGURATION TABLES

Table 1b. Reference Configuration Table (Continued). The LTC2357-16 Supports Three Reference Configurations. Analog Input Range Scales with the Converter Master Reference Voltage,  $V_{REFBUF}$

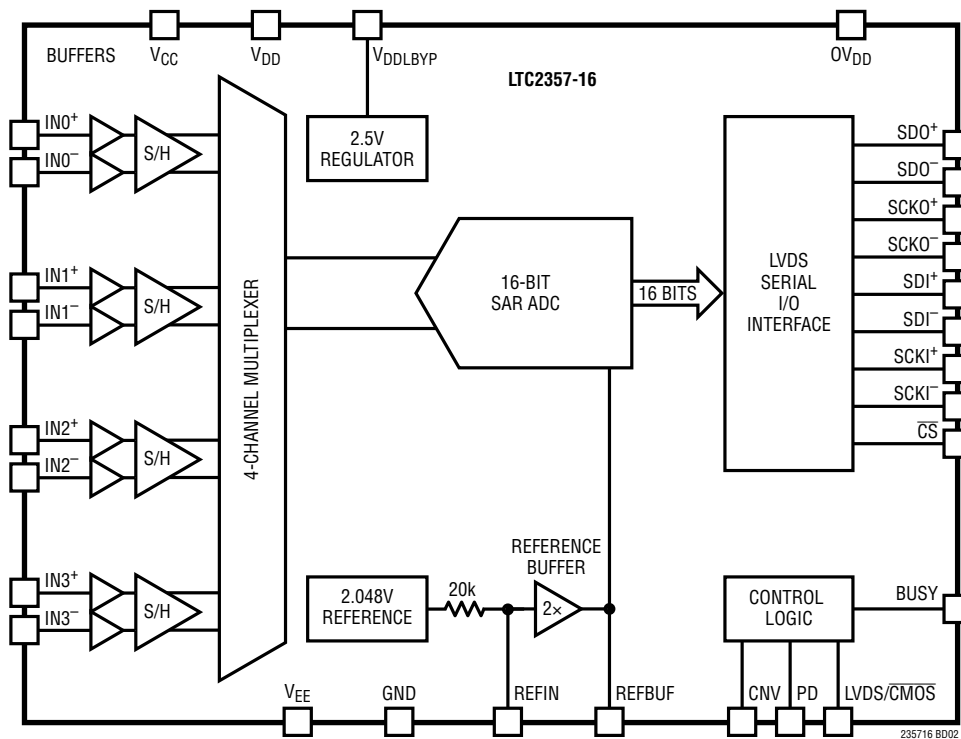
REFERENCE CONFIGURATION	$V_{REFIN}$	$V_{REFBUF}$	BINARY SoftSpan CODE SS[2:0]	ANALOG INPUT RANGE
External Reference Unbuffered (REFBUF Pin Externally Overdriven, REFIN Pin Grounded)	0V	2.5V (Min Value)	111	$\pm 6.25V$
			110	$\pm 6.104V$
			101	0V to 6.25V
			100	0V to 6.104V
			011	$\pm 3.125V$
			010	$\pm 3.052V$
			001	0V to 3.125V
	0V	5V (Max Value)	111	$\pm 12.5V$
			110	$\pm 12.207V$
			101	0V to 12.5V
			100	0V to 12.207V
			011	$\pm 6.25V$
			010	$\pm 6.104V$
			001	0V to 6.25V

# FUNCTIONAL BLOCK DIAGRAM

CMOS I/O Mode

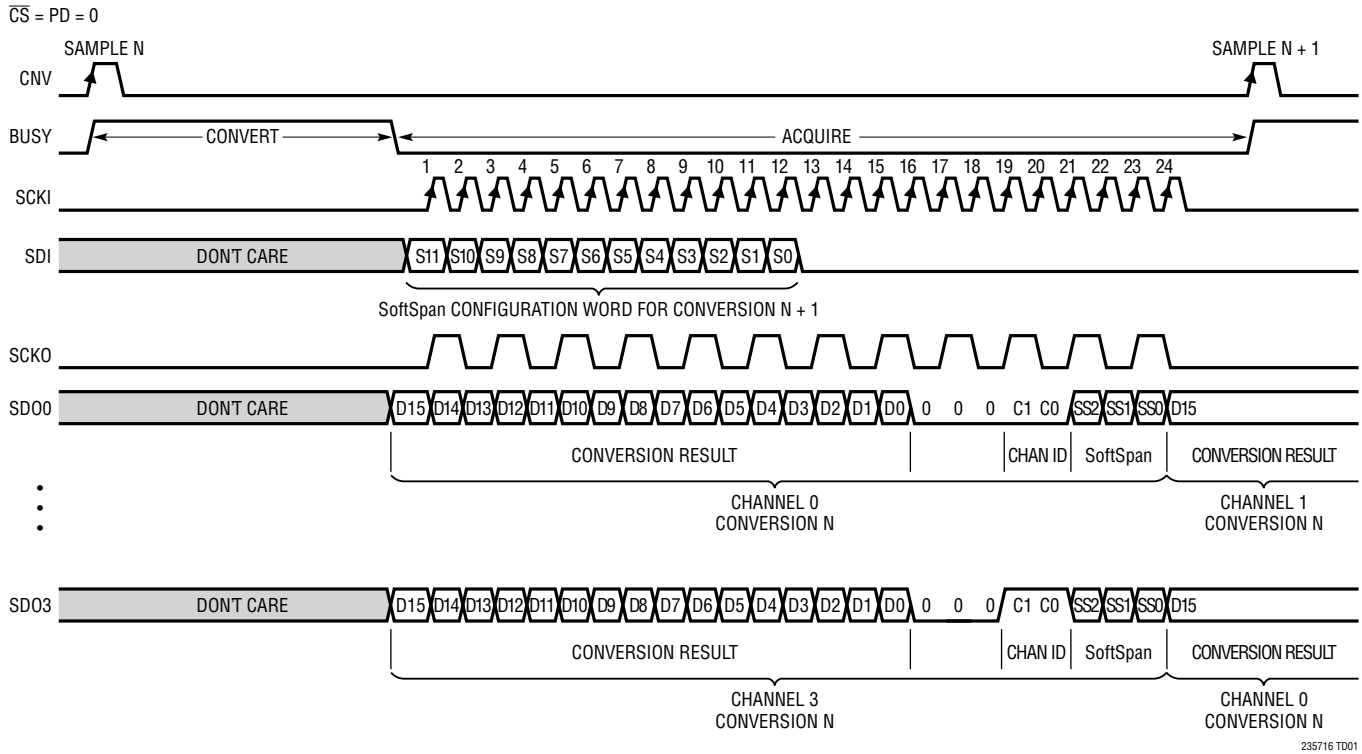


LVDS I/O Mode

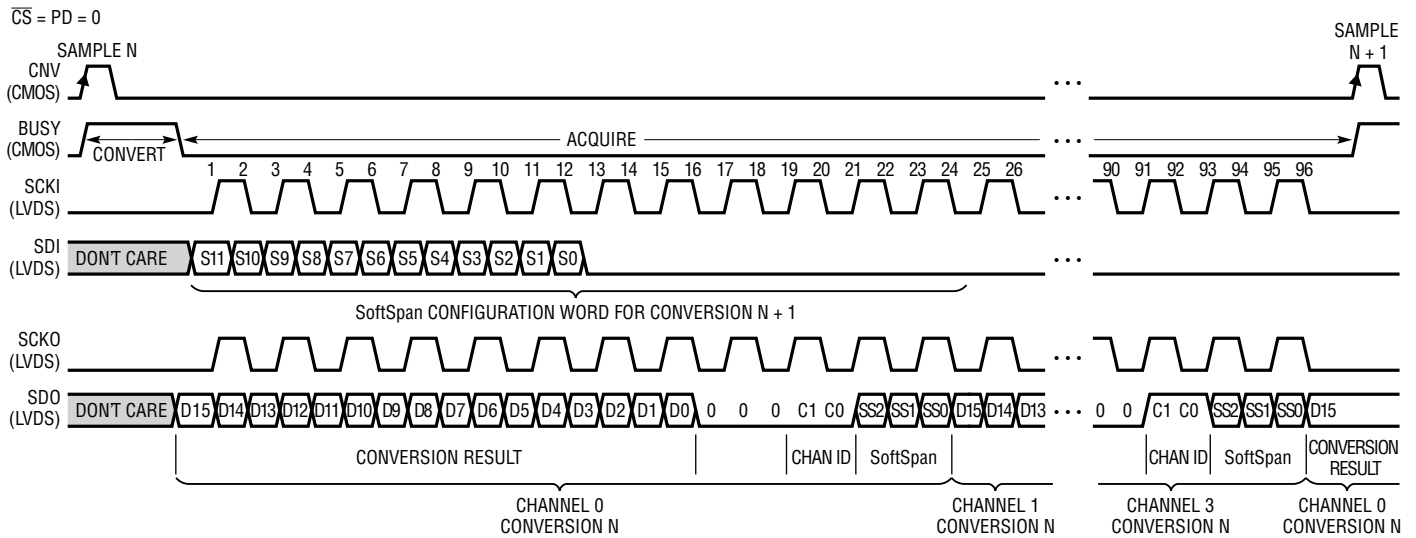


# TIMING DIAGRAM

## CMOS I/O Mode



## LVDS I/O Mode



## APPLICATIONS INFORMATION

### OVERVIEW

The LTC2357-16 is a 16-bit, low noise 4-channel simultaneous sampling successive approximation register (SAR) ADC with buffered differential, wide common mode range picoamp inputs. The ADC operates from a 5V low voltage supply and flexible high voltage supplies, nominally  $\pm 15V$ . Using the integrated low-drift reference and buffer ( $V_{REFBUF} = 4.096V$  nominal), each channel of this SoftSpan ADC can be independently configured on a conversion-by-conversion basis to accept  $\pm 10.24V$ ,  $0V$  to  $10.24V$ ,  $\pm 5.12V$ , or  $0V$  to  $5.12V$  signals. The input signal range may be expanded up to  $\pm 12.5V$  using an external 5V reference. Individual channels may also be disabled to increase throughput on the remaining channels.

The integrated picoamp-input analog buffers, wide input common mode range, and 128dB CMRR of the LTC2357-16 allow the ADC to directly digitize a variety of signals using minimal board space and power. This input signal flexibility, combined with  $\pm 1LSB$  INL, no missing codes at 16 bits, and 94.2dB SNR, makes the LTC2357-16 an ideal choice for many high voltage applications requiring wide dynamic range.

The absolute common mode input range ( $V_{EE} + 4V$  to  $V_{CC} - 4V$ ) is determined by the choice of high voltage supplies. These supplies may be biased asymmetrically around ground and include the ability for  $V_{EE}$  to be tied directly to ground.

The LTC2357-16 supports pin-selectable SPI CMOS (1.8V to 5V) and LVDS serial interfaces, enabling it to communicate equally well with legacy microcontrollers and modern FPGAs. In CMOS mode, applications may employ between one and four lanes of serial output data, allowing the user to optimize bus width and data throughput. The LTC2357-16 typically dissipates 175mW when converting four channels simultaneously at 350ksps per channel. Optional nap and power down modes may be employed to further reduce power consumption during inactive periods.

### CONVERTER OPERATION

The LTC2357-16 operates in two phases. During the acquisition phase, the sampling capacitors in each channel's sample-and-hold (S/H) circuit connect to their respective analog input buffers, which track the differential analog input voltage ( $V_{IN+} - V_{IN-}$ ). A rising edge on the CNV pin transitions all channels' S/H circuits from track mode to hold mode, simultaneously sampling the input signals on all channels and initiating a conversion. During the conversion phase, each channel's sampling capacitors are connected, one channel at a time, to a 16-bit charge redistribution capacitor D/A converter (CDAC). The CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input voltage with binary-weighted fractions of the channel's SoftSpan full-scale range (e.g.,  $V_{FSR}/2$ ,  $V_{FSR}/4$  ...  $V_{FSR}/65536$ ) using a differential comparator. At the end of this process, the CDAC output approximates the channel's sampled analog input. Once all channels have been converted in this manner, the ADC control logic prepares the 16-bit digital output codes from each channel for serial transfer.

### TRANSFER FUNCTION

The LTC2357-16 digitizes each channel's full-scale voltage range into  $2^{16}$  levels. In conjunction with the ADC master reference voltage,  $V_{REFBUF}$ , a channel's SoftSpan configuration determines its input voltage range, full-scale range, LSB size, and the binary format of its conversion result, as shown in Tables 1a and 1b. For example, employing the internal reference and buffer ( $V_{REFBUF} = 4.096V$  nominal), SoftSpan 7 configures a channel to accept a  $\pm 10.24V$  bipolar analog input voltage range, which corresponds to a 20.48V full-scale range with a  $312.5\mu V$  LSB. Other SoftSpan configurations and reference voltages may be employed to convert both larger and smaller bipolar and unipolar input ranges. Conversion results are output in two's complement binary format for all bipolar SoftSpan ranges, and in straight binary format for all unipolar SoftSpan ranges.

## APPLICATIONS INFORMATION

The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3.

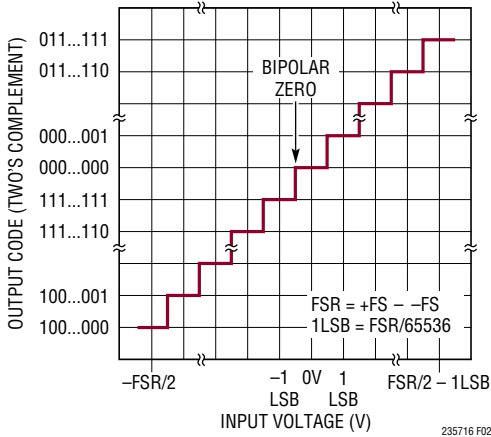


Figure 2. LTC2357-16 Two's Complement Transfer Function

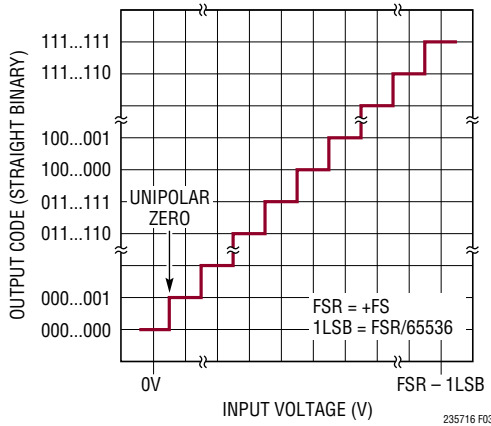


Figure 3. LTC2357-16 Straight Binary Transfer Function

### BUFFERED ANALOG INPUTS

Each channel of the LTC2357-16 simultaneously samples the voltage difference ( $V_{IN+} - V_{IN-}$ ) between its analog input pins over a wide common mode input range while attenuating unwanted signals common to both input pins by the common-mode rejection ratio (CMRR) of the ADC. Wide common mode input range coupled with high CMRR allows the  $IN^+/IN^-$  analog inputs to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{EE} + 4V)$  and  $(V_{CC} - 4V)$ . This feature of the

LTC2357-16 enables it to accept a wide variety of signal swings, including traditional classes of analog input signals such as pseudo-differential unipolar, pseudo-differential true bipolar, and fully differential, simplifying signal chain design. For conversion of signals extending to  $V_{EE}$ , the unbuffered LTC2348-16 ADC is recommended.

The wide operating range of the high voltage supplies offers further input common mode flexibility. As long as the voltage difference limits of  $10V \leq (V_{CC} - V_{EE}) \leq 38V$  are observed,  $V_{CC}$  and  $V_{EE}$  may be independently biased anywhere within their own individually allowed operating ranges, including the ability for  $V_{EE}$  to be tied directly to ground. This feature enables the common mode input range of the LTC2357-16 to be tailored to specific application requirements.

In all SoftSpan ranges, each channel's analog inputs can be modeled by the equivalent circuit shown in Figure 4. At the start of acquisition, the sampling capacitors ( $C_{SAMP}$ ) connect to the integrated buffers  $BUFFER^+/BUFFER^-$  through the sampling switches. The sampled voltage is reset during the conversion process and is therefore re-acquired for each new conversion.

The diodes between the inputs and the  $V_{CC}$  and  $V_{EE}$  supplies provide input ESD protection. While within the supply voltages, the analog inputs of the LTC2357-16 draw only 5pA typical DC leakage current and the ESD protection diodes don't turn on. This offers a significant advantage over external op amp buffers, which often have diode protection that turns on during transients and corrupts the voltage on any filter capacitors at their inputs.

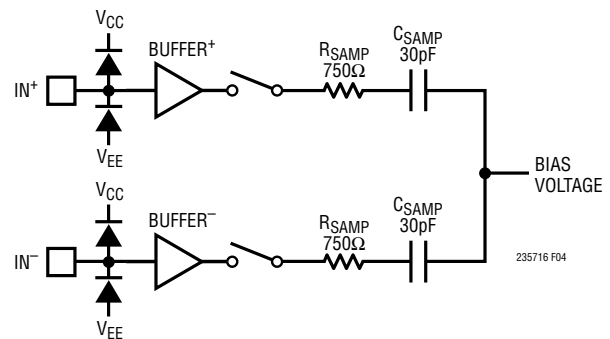


Figure 4. Equivalent Circuit for Differential Analog Inputs, Single Channel Shown

## APPLICATIONS INFORMATION

### Bipolar SoftSpan Input Ranges

For channels configured in SoftSpan ranges 7, 6, 3, or 2, the LTC2357-16 digitizes the differential analog input voltage ( $V_{IN+} - V_{IN-}$ ) over a bipolar span of  $\pm 2.5 \cdot V_{REFBUF}$ ,  $\pm 2.5 \cdot V_{REFBUF}/1.024$ ,  $\pm 1.25 \cdot V_{REFBUF}$ , or  $\pm 1.25 \cdot V_{REFBUF}/1.024$ , respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where  $IN^+$  and  $IN^-$  swing above and below each other. Traditional examples include fully differential input signals, where  $IN^+$  and  $IN^-$  are driven 180 degrees out-of-phase with respect to each other centered around a common mode voltage  $(V_{IN+} + V_{IN-})/2$ , and pseudo-differential true bipolar input signals, where  $IN^+$  swings above and below a ground reference level, driven on  $IN^-$ . Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the  $IN^+/IN^-$  analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $(V_{EE} + 4V)$ . The output data format for all bipolar SoftSpan ranges is two's complement.

### Unipolar SoftSpan Input Ranges

For channels configured in SoftSpan ranges 5, 4, or 1, the LTC2357-16 digitizes the differential analog input voltage ( $V_{IN+} - V_{IN-}$ ) over a unipolar span of  $0V$  to  $2.5 \cdot V_{REFBUF}$ ,  $0V$  to  $2.5 \cdot V_{REFBUF}/1.024$ , or  $0V$  to  $1.25 \cdot V_{REFBUF}$ , respectively, as shown in Table 1a. These SoftSpan ranges are useful for digitizing input signals where  $IN^+$  remains above  $IN^-$ . A traditional example includes pseudo-differential unipolar input signals, where  $IN^+$  swings above a ground reference level, driven on  $IN^-$ . Regardless of the chosen SoftSpan range, the wide common mode input range and high CMRR of the  $IN^+/IN^-$  analog inputs allow them to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $(V_{EE} + 4V)$ . The output data format for all unipolar SoftSpan ranges is straight binary.

### INPUT DRIVE CIRCUITS

The CMOS buffer input stage offers a very high degree of transient isolation from the sampling process. Most sensors, signal conditioning amplifiers and filter networks with

less than  $10k\Omega$  of impedance can drive the passive  $3pF$  analog input capacitance directly. For higher impedances and slow-settling circuits, add a  $680pF$  capacitor at the pins to maintain the full DC accuracy of the LTC2357-16.

The very high input impedance of the unity gain buffers in the LTC2357-16 greatly reduces the input drive requirements and makes it possible to include optional RC filters with  $k\Omega$  impedance and arbitrarily slow time constants for anti-aliasing or other purposes. Micro-power op amps with limited drive capability are also well suited to drive the high impedance analog inputs directly.

The LTC2357-16 features proprietary circuitry to achieve exceptional internal crosstalk isolation between channels ( $-109dB$  typical). The PCB board wiring to the analog inputs should be short and shielded to prevent external capacitive crosstalk between channels. The capacitance between adjacent package pins is  $0.16pF$ . Low source resistance and/or high source capacitance help reduce external capacitively coupled crosstalk. Single ended input drive also enjoys additional external crosstalk isolation because every other input pin is grounded, or at a low impedance DC source, and serves as a shield between channels.

### INPUT OVERDRIVE TOLERANCE

Driving an analog input above  $V_{CC}$  on any channel up to  $10mA$  will not affect conversion results on other channels. Approximately 70% of this overdrive current will flow out of the  $V_{CC}$  pin and the remaining 30% will flow out of  $V_{EE}$ . This current flowing out of  $V_{EE}$  will produce heat across the  $V_{CC} - V_{EE}$  voltage drop and must be taken into account for the total Absolute Maximum power dissipation of  $500mW$ . Driving an analog input below  $V_{EE}$  may corrupt conversion results on other channels. This product can handle input currents of up to  $100mA$  below  $V_{EE}$  or above  $V_{CC}$  without latchup.

Keep in mind that driving the inputs above  $V_{CC}$  or below  $V_{EE}$  may reverse the normal current flow from the external power supplies driving these pins.

## APPLICATIONS INFORMATION

### Input Filtering

The true high impedance analog inputs can accommodate a very wide range of passive or active signal conditioning filters. The buffered ADC inputs have an analog bandwidth of 6MHz, and impose no particular bandwidth requirement on external filters. The external input filters can therefore be optimized independent of the ADC to reduce signal chain noise and interference. A common filter configuration is the simple anti-aliasing and noise reducing RC filter with its pole at half the sampling frequency. For example, 175kHz with  $R = 1.33k\Omega$  and  $C = 680pF$  as shown in Figure 5.

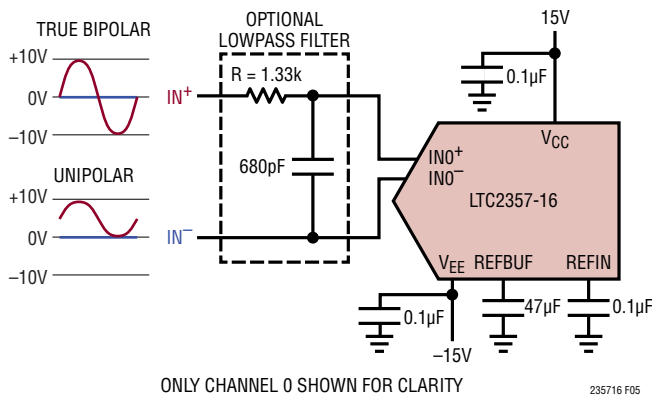


Figure 5. Filtering Single-Ended Input Signals

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO/COG and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self-heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

### Arbitrary and Fully Differential Analog Input Signals

The wide common mode input range and high CMRR of the LTC2357-16 allow each channel's  $IN^+$  and  $IN^-$  pins to swing with an arbitrary relationship to each other, provided each pin remains between  $(V_{CC} - 4V)$  and  $(V_{EE} + 4V)$ . This

feature of the LTC2357-16 enables it to accept a wide variety of signal swings, simplifying signal chain design.

The two-tone test shown in Figure 6b demonstrates the arbitrary input drive capability of the LTC2357-16. This test simultaneously drives  $IN^+$  with a  $-7dBFS$  2kHz single-ended sine wave and  $IN^-$  with a  $-7dBFS$  3.1kHz single-ended sine wave. Together, these signals sweep the analog inputs across a wide range of common mode and differential mode voltage combinations, similar to the more general arbitrary input signal case. They also have a simple spectral representation. An ideal differential converter with no common-mode sensitivity will digitize this signal as two  $-7dBFS$  spectral tones, one at each sine wave frequency. The FFT plot in Figure 6b demonstrates the LTC2357-16 response approaches this ideal, with 121dB of SFDR limited by the converter's second harmonic distortion response to the 3.1kHz sine wave on  $IN^-$ .

The ability of the LTC2357-16 to accept arbitrary signal swings over a wide input common mode range with high CMRR can simplify application solutions. In practice, many sensors produce a differential sensor voltage riding on top of a large common mode signal. Figure 7a depicts one way of using the LTC2357-16 to digitize signals of this type. The amplifier stage provides a differential gain of approximately 10V/V to the desired sensor signal while the unwanted common mode signal is attenuated by the ADC CMRR. The circuit employs the  $\pm 5V$  SoftSpan range of the ADC. Figure 7b shows measured CMRR performance of this solution, which is competitive with the best commercially available instrumentation amplifiers. Figure 7c shows measured AC performance of this solution.

In Figure 8, another application circuit is shown which uses two channels of the LTC2357-16 to simultaneously sense the voltage and bidirectional current through a sense resistor over a wide common mode range.

APPLICATIONS INFORMATION

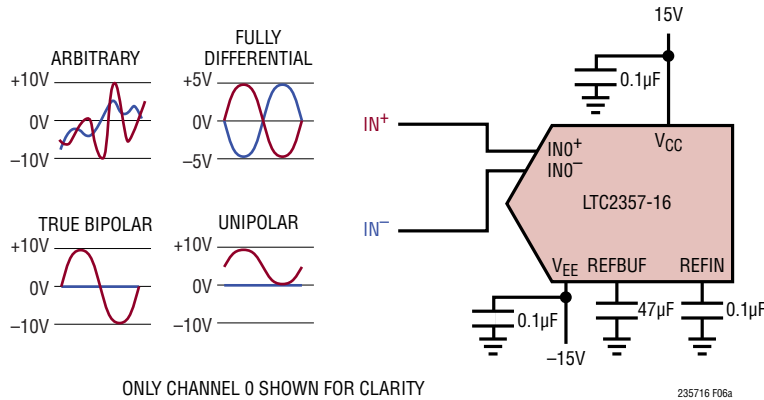


Figure 6a. Input Arbitrary, Fully Differential, True Bipolar, and Unipolar Signals

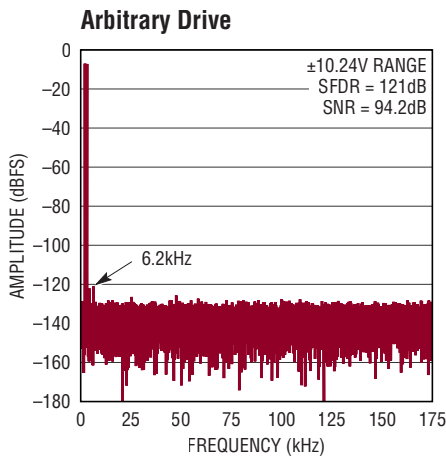


Figure 6b. Two-Tone Test.  $IN^+ = -7\text{dBFS}$  2kHz Sine,  $IN^- = -7\text{dBFS}$  3.1kHz Sine, 32k Point FFT,  $f_{\text{SAMPL}} = 350\text{kpsps}$ . Circuit Shown in Figure 6a

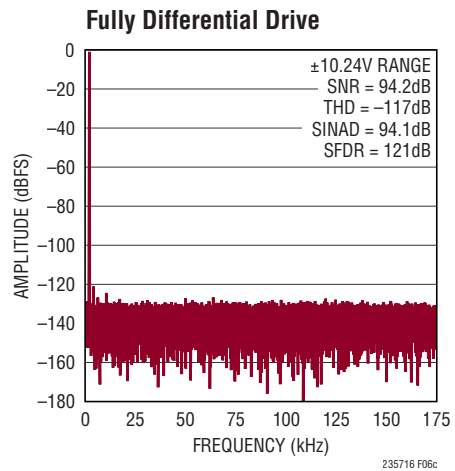


Figure 6c.  $IN^+/IN^- = -1\text{dBFS}$  2kHz Fully Differential Sine,  $V_{\text{CM}} = 0\text{V}$ , 32k Point FFT,  $f_{\text{SAMPL}} = 350\text{kpsps}$ . Circuit Shown in Figure 6a

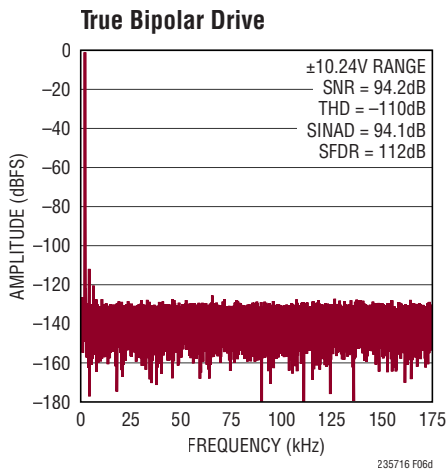


Figure 6d.  $IN^+ = -1\text{dBFS}$  2kHz True Bipolar Sine,  $IN^- = 0\text{V}$ , 32k Point FFT,  $f_{\text{SAMPL}} = 350\text{kpsps}$ . Circuit Shown in Figure 6a

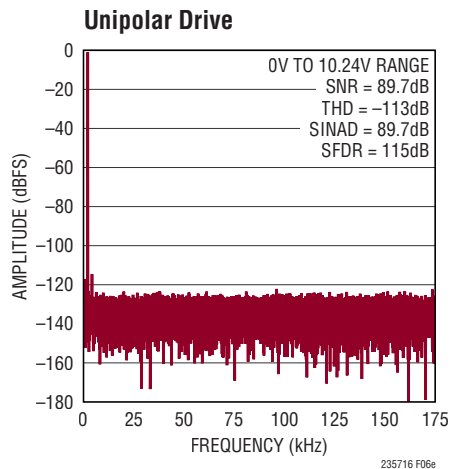


Figure 6e.  $IN^+ = -1\text{dBFS}$  2kHz Unipolar Sine,  $IN^- = 0\text{V}$ , 32k Point FFT,  $f_{\text{SAMPL}} = 350\text{kpsps}$ . Circuit Shown in Figure 6a



APPLICATIONS INFORMATION

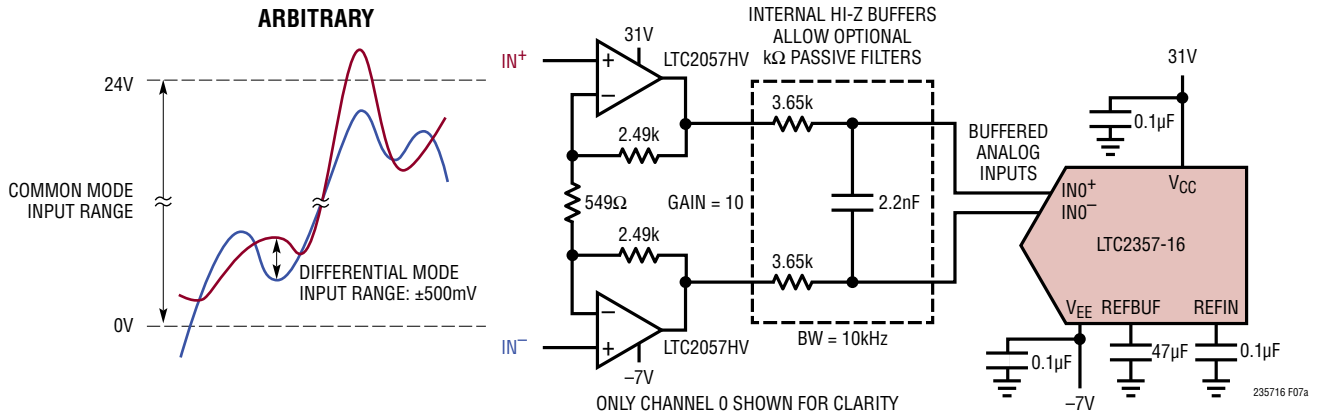


Figure 7a. Amplify Differential Signals with Gain of 10 Over a Wide Common Mode Range with Buffered Analog Inputs

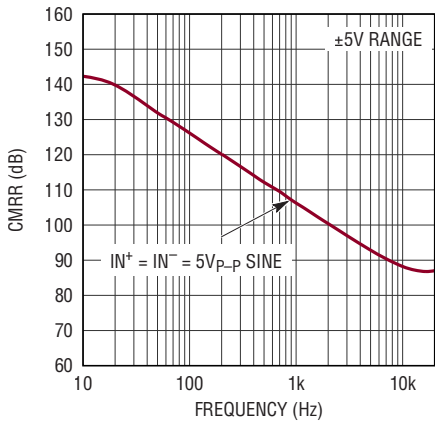


Figure 7b. CMRR vs Input Frequency. Circuit Shown in Figure 7a

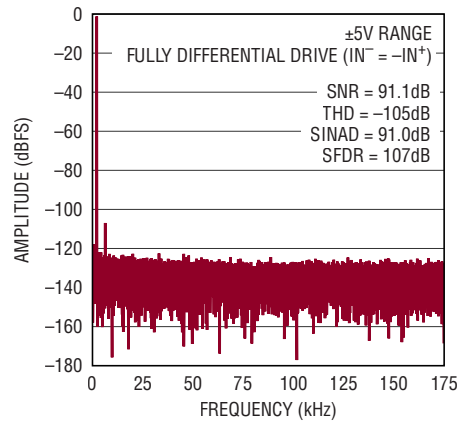


Figure 7c.  $IN^+/IN^- = 450\text{mV}$  200Hz Fully Differential Sine,  $0\text{V} \leq V_{CM} \leq 24\text{V}$ , 32k Point FFT,  $f_{SMPL} = 350\text{kpsps}$ . Circuit Shown in Figure 7a

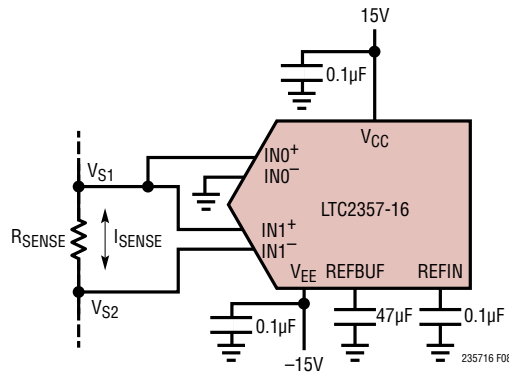


Figure 8. Simultaneously Sense Voltage (CH0) and Current (CH1) Over a Wide Common Mode Range

## APPLICATIONS INFORMATION

### ADC REFERENCE

As shown previously in Table 1b, the LTC2357-16 supports three reference configurations. The first uses both the internal bandgap reference and reference buffer. The second externally overdrives the internal reference but retains the internal buffer, which isolates the external reference from ADC conversion transients. This configuration is ideal for sharing a single precision external reference across multiple ADCs. The third disables the internal buffer and overdrives the REFBUF pin externally.

#### Internal Reference with Internal Buffer

The LTC2357-16 has an on-chip, low noise, low drift (20ppm/°C maximum), temperature compensated bandgap reference that is factory trimmed to 2.048V. The reference output connects through a 20kΩ resistor to the REFIN pin, which serves as the input to the on-chip reference buffer, as shown in Figure 9a. When employing the internal bandgap reference, the REFIN pin should be bypassed to GND (Pin 20) close to the pin with a 0.1μF ceramic capacitor to filter wideband noise. The reference buffer amplifies  $V_{REFIN}$  to create the converter master reference voltage  $V_{REFBUF} = 2 \cdot V_{REFIN}$  on the REFBUF pin, nominally 4.096V when using the internal bandgap reference. Bypass REFBUF to GND (Pin 20) close to the pin with at least a 47μF ceramic capacitor (X7R, 10V, 1210 size or X5R, 10V, 0805 size) to compensate the reference buffer, absorb transient conversion currents, and minimize noise.

#### External Reference with Internal Buffer

If more accuracy and/or lower drift is desired, REFIN can be easily overdriven by an external reference since 20kΩ of resistance separates the internal bandgap reference output from the REFIN pin, as shown in Figure 9b. The valid range of external reference voltage overdrive on the REFIN pin is 1.25V to 2.2V, resulting in converter master reference voltages  $V_{REFBUF}$  between 2.5V and 4.4V, respectively. Linear Technology offers a portfolio of high performance references designed to meet the needs of many applications. With its small size, low power, and high accuracy, the LTC6655-2.048 is well suited for use with the LTC2357-16 when overdriving the internal reference. The

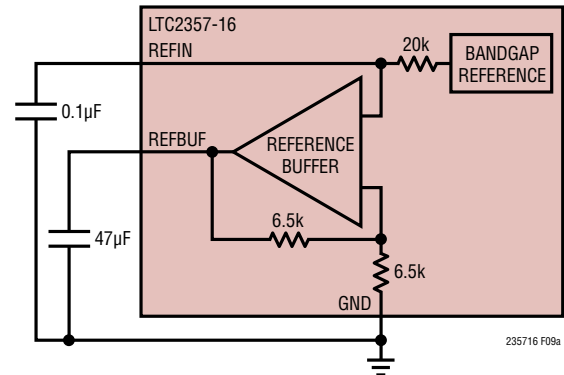


Figure 9a. Internal Reference with Internal Buffer Configuration

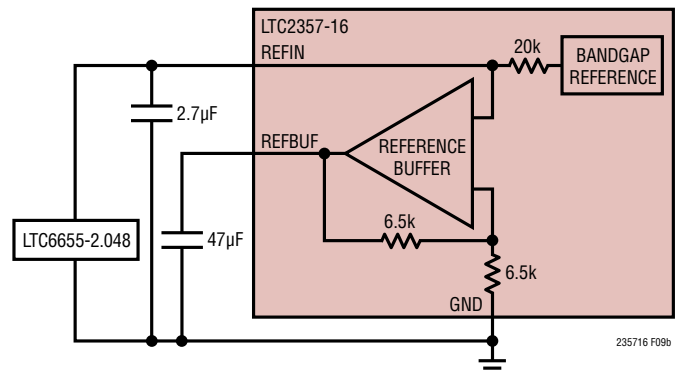


Figure 9b. External Reference with Internal Buffer Configuration

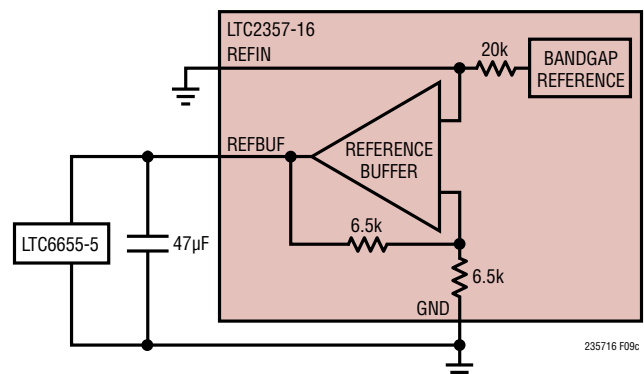


Figure 9c. External Reference with Disabled Internal Buffer Configuration