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16-Bit, 1Msps, 8-Channel SAR ADC with 96dB SNR

FEATURES

- **1Msps Throughput Rate**
- **16-Bit Resolution with No Missing Codes**
- **8-Channel Multiplexer with Selectable Input Range**
  - **Fully Differential (±4.096V)**
  - **Pseudo-Differential Unipolar (0V to 4.096V)**
  - **Pseudo-Differential Bipolar (±2.048V)**
- **INL: ±1LSB (Maximum)**
- **SNR: 96dB (Fully Differential)/93.4dB (Pseudo-Differential) (Typical) at f_{IN} = 1kHz**
- **THD: –110dB (Typical) at f_{IN} = 1kHz**
- Programmable Sequencer
- Selectable Digital Gain Compression
- Single 5V Supply with 1.8V to 5V I/O Voltages
- SPI-Compatible Serial I/O
- Onboard 2.048V Reference and Reference Buffer
- No Pipeline Delay, No Cycle Latency
- Power Dissipation 40mW (Typical)
- Guaranteed Operation to 125°C
- 32-Lead 5mm × 5mm QFN Package

APPLICATIONS

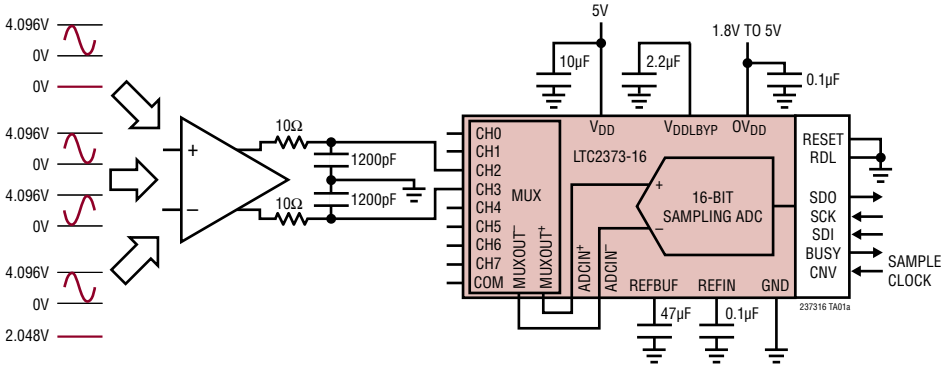
- Programmable Logic Controllers
- Industrial Process Control
- High Speed Data Acquisition
- Portable or Compact Instrumentation
- ATE

DESCRIPTION

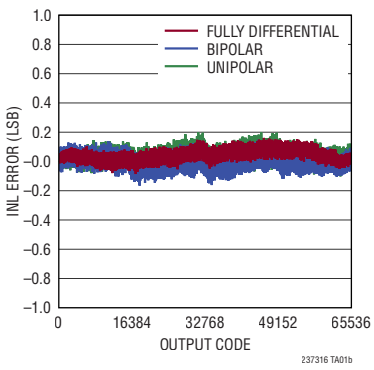
The LTC®2373-16 is a low noise, high speed, 8-channel 16-bit successive approximation register (SAR) ADC. Operating from a single 5V supply, the LTC2373-16 has a highly configurable, low crosstalk 8-channel input multiplexer, supporting fully differential, pseudo-differential unipolar and pseudo-differential bipolar analog input ranges. The LTC2373-16 achieves ±1LSB INL (maximum) in all input ranges, no missing codes at 16-bits and 96dB (fully differential)/ 93.4dB (pseudo-differential) SNR (typical).

The LTC2373-16 has an onboard low drift (20ppm/°C max) 2.048V temperature-compensated reference and a single-shot capable reference buffer. The LTC2373-16 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic through which a sequencer with a depth of 16 may be programmed. An internal oscillator sets the conversion time, easing external timing considerations. The LTC2373-16 dissipates only 40mW and automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided to reduce the power consumption of the LTC2373-16 to 300µW for further power savings during inactive periods.

TYPICAL APPLICATION



Integral Nonlinearity vs Output Code

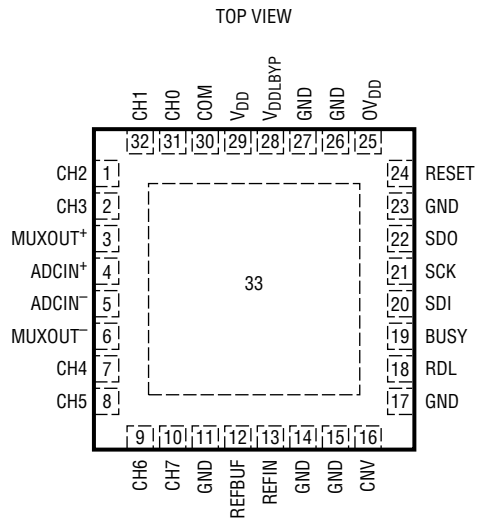


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{DD}) 6V
Supply Voltage (OV_{DD}) 6V
Analog Input Voltage (Note 3)
CH0 to CH7, COM ..... (GND – 0.3V) to (V_{DD} + 0.3V)
REFBUF ..... (GND – 0.3V) to (V_{DD} + 0.3V)
REFIN 2.8V
Digital Input Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Digital Output Voltage
(Note 3) ..... (GND –0.3V) to (OV_{DD} + 0.3V)
Power Dissipation 500mW
Operating Temperature Range
LTC2373C ..... 0°C to 70°C
LTC2373I ..... –40°C to 85°C
LTC2373H ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 44°C/W
EXPOSED PAD IS GND (PIN 33) MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2373-16#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2373CUH-16#PBF	LTC2373CUH-16#TRPBF	237316	32-Lead (5mm × 5mm) Plastic QFN	0°C to 70°C
LTC2373IUH-16#PBF	LTC2373IUH-16#TRPBF	237316	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC2373HUH-16#PBF	LTC2373HUH-16#TRPBF	237316	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}^+	Absolute Input Range (CH0 to CH7)	(Note 5)	●	–0.1		V_{REFBUF} + 0.1	V
V_{IN}^-	Absolute Input Range (CH0 to CH7, COM)	Fully Differential (Note 5)	●	–0.1		V_{REFBUF} + 0.1	V
		Pseudo-Differential Unipolar (Note 5)	●	–0.1	0	0.1	V
		Pseudo-Differential Bipolar (Note 5)	●	$V_{REFBUF}/2$ – 0.1	$V_{REFBUF}/2$	$V_{REFBUF}/2$ + 0.1	V
$V_{IN}^+ – V_{IN}^-$	Input Differential Voltage Range	Fully Differential	●	$–V_{REFBUF}$		V_{REFBUF}	V
		Pseudo-Differential Unipolar	●	0		V_{REFBUF}	V
		Pseudo-Differential Bipolar	●	$–V_{REFBUF}/2$		$V_{REFBUF}/2$	V
V_{CM}	Common Mode Input Range	Pseudo-Differential Bipolar and Fully Differential (Note 6)	●	$–V_{REFBUF}/2$ – 0.1	$V_{REFBUF}/2$	$V_{REFBUF}/2$ + 0.1	V
I_{IN}	Analog Input Leakage Current		●	–1		1	µA
C_{IN}	Analog Input Capacitance	Sample Mode			75		pF
		Hold Mode			5		pF
CMRR	Input Common Mode Rejection Ratio	Fully Differential, f_{IN} = 500kHz			67		dB
		Pseudo-Differential Unipolar, f_{IN} = 500kHz			66		dB
		Pseudo-Differential Bipolar, f_{IN} = 500kHz			66		dB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Resolution		●	16			Bits
	No Missing Codes		●	16			Bits
	Transition Noise	Fully Differential			0.3		LSB_{RMS}
		Pseudo-Differential Unipolar			0.6		LSB_{RMS}
		Pseudo-Differential Bipolar			0.6		LSB_{RMS}
INL	Integral Linearity Error	Fully Differential (Note 7)	●	–1	0.1	1	LSB
		Pseudo-Differential Unipolar (Note 7)	●	–1	0.1	1	LSB
		Pseudo-Differential Bipolar (Note 7)	●	–1	0.1	1	LSB
DNL	Differential Linearity Error	Fully Differential (Note 6)	●	–0.5	0.1	0.5	LSB
		Pseudo-Differential Unipolar (Note 6)	●	–0.5	0.1	0.5	LSB
		Pseudo-Differential Bipolar (Note 6)	●	–0.5	0.1	0.5	LSB
ZSE	Zero-Scale Error	Fully Differential (Note 8)	●	–6	±0.5	6	LSB
		Pseudo-Differential Unipolar (Note 8)	●	–6	±0.5	6	LSB
		Pseudo-Differential Bipolar (Note 8)	●	–8	±0.5	8	LSB
	Zero-Scale Error Drift	Fully Differential			1		mLSB/°C
		Pseudo-Differential Unipolar			2		mLSB/°C
		Pseudo-Differential Bipolar			2		mLSB/°C
	Zero-Scale Error Match	Fully Differential	●	–6	±0.5	6	LSB
		Pseudo-Differential Unipolar	●	–7	±1	7	LSB
		Pseudo-Differential Bipolar	●	–8	±1	8	LSB
FSE	Full-Scale Error	Fully Differential					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–15	±2	15	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–25	±3	25	LSB
		Pseudo-Differential Unipolar					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–20	±1	20	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–45	±4	45	LSB
		Pseudo-Differential Bipolar					
		REFBUF = 4.096V (REFBUF Overdriven) (Notes 8, 9)	●	–15	±2	15	LSB
		REFIN = 2.048V (REFIN Overdriven) (Note 8)	●	–30	±3	30	LSB

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Full-Scale Error Drift	Fully Differential REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9)			0.2 0.2 0.2		ppm/°C ppm/°C ppm/°C
	Full-Scale Error Match	Fully Differential REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar REFBUF = 4.096V (REFBUF Overdriven) (Note 9)	 ● ● ●	 –6 –7 –8	 ±0.5 ±1 ±1	 6 7 8	 LSB LSB LSB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
SINAD	Signal-to-(Noise + Distortion) Ratio	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●	 93 90.5 90.5	 96 93.4 93.4		 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			97 94.5 94.5		dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			95 91.5		dB dB
SNR	Signal-to-Noise Ratio	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●	 93 90.5 90.5	 96 93.4 93.4		 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			97 94.5 94.5		dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			95 91.5		dB dB

DYNAMIC ACCURACY

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and A_{IN} = –1dBFS. (Notes 4, 10)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
THD	Total Harmonic Distortion	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●		 –114 –110 –110	 –101 –100 –100	 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			 –111 –110 –110		 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			 –113 –110		 dB dB
SFDR	Spurious Free Dynamic Range	Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven)	 ● ● ●	 101 100 100	 114 110 110		 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Unipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9) Pseudo-Differential Bipolar f_{IN} = 1kHz, REFBUF = 5V (REFBUF Overdriven) (Note 9)			 112 112 112		 dB dB dB
		Fully Differential f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1 Pseudo-Differential Bipolar f_{IN} = 1kHz, REFIN = 2.048V (REFIN Overdriven), SEL = 1			 112.5 113.5		 dB dB
	Channel-to-Channel Crosstalk	f_{IN} = 100kHz, Signal Applied to an OFF Channel			–107		dB
	–3dB Input Linear Bandwidth				22		MHz
	Aperture Delay				500		ps
	Aperture Jitter				4		ps_{RMS}
	Transient Response	Full-Scale Step			460		ns

INTERNAL REFERENCE CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFIN}	Internal Reference Output Voltage			2.043	2.048	2.053	V
	V_{REFIN} Temperature Coefficient	(Note 11)	●		4	20	ppm/°C
	REFIN Output Impedance				15		kΩ
	V_{REFIN} Line Regulation	V_{DD} = 4.75V to 5.25V			0.06		mV/V
	REFIN Input Voltage Range	(REFIN Overdriven) (Note 5)		1.25		2.4	V

REFERENCE BUFFER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{REFBUF}	Reference Buffer Output Voltage	V_{REFIN} = 2.048V	●	4.088	4.096	4.104	V
	REFBUF Input Voltage Range	(REFBUF Overdriven) (Notes 5, 9)	●	2.5		5	V
	REFBUF Output Impedance	V_{REFIN} = 0V (Buffer Disabled)			13		kΩ
I_{REFBUF}	REFBUF Load Current	V_{REFBUF} = 5V (REFBUF Overdriven) (Notes 9, 12) V_{REFBUF} = 5V, Nap Mode (REFBUF Overdriven) (Note 9)	●		1 0.38	1.2	mA mA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage		●	0.8 • OV_{DD}			V
V_{IL}	Low Level Input Voltage		●			0.2 • OV_{DD}	V
I_{IN}	Digital Input Current	V_{IN} = 0V to OV_{DD}	●	–10		10	µA
C_{IN}	Digital Input Capacitance				5		pF
V_{OH}	High Level Output Voltage	I_O = –500µA	●	OV_{DD} – 0.2			V
V_{OL}	Low Level Output Voltage	I_O = 500µA	●			0.2	V
I_{OZ}	Hi-Z Output Leakage Current	V_{OUT} = 0V to OV_{DD}	●	–10		10	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–10		mA
I_{SINK}	Output Sink Current	V_{OUT} = OV_{DD}			10		mA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD}	Supply Voltage		●	4.75	5	5.25	V
OV_{DD}	Supply Voltage		●	1.71		5.25	V
I_{VDD}	Supply Current	1Msps Sample Rate	●		8	11	mA
I_{OVDD}	Supply Current	1Msps Sample Rate (C_L = 20pF)	●		0.7		mA
I_{NAP}	Nap Mode Current	Conversion Done (I_{VDD} + I_{OVDD})	●		1.25	1.5	mA
I_{SLEEP}	Sleep Mode Current	Sleep Mode (I_{VDD} + I_{OVDD})	●		60	120	µA
P_D	Power Dissipation	1Msps Sample Rate			40	55	mW
	Nap Mode	Conversion Done (I_{VDD} + I_{OVDD})			6.25	7.5	mW
	Sleep Mode	Sleep Mode (I_{VDD} + I_{OVDD})			300	600	µW

ADC TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{SMPL}	Maximum Sampling Frequency		●			1	Msps
t_{CONV}	Conversion Time		●	460		527	ns
t_{ACQ}	Acquisition Time	t_{ACQ} = t_{CYC} – t_{CONV} – t_{BUSYLH} (Note 6)	●	460			ns
t_{CYC}	Time Between Conversions		●	1			µs
t_{CNVH}	CNV High Time		●	20			ns
t_{CNVL}	Minimum Low Time for CNV	(Note 13)	●	20			ns
t_{BUSYLH}	CNV↑ to BUSY↑ Delay	C_L = 20pF	●			13	ns
t_{RESETH}	RESET Pulse Width		●	200			ns
t_{QUIET}	SCK, SDI and RDL Quiet Time from CNV↑	(Note 6)	●	20			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 4)

t_{SCK}	SCK Period	(Notes 13, 14)	●	10		ns
t_{SCKH}	SCK High Time		●	4		ns
t_{SCKL}	SCK Low Time		●	4		ns
$t_{SSDISCK}$	SDI Setup Time From SCK↑	(Note 13)	●	4		ns
$t_{HSDISCK}$	SDI Hold Time From SCK↑	(Note 13)	●	1		ns
t_{DSDO}	SDO Data Valid Delay from SCK↑	C_L = 20pF, OV_{DD} = 5.25V C_L = 20pF, OV_{DD} = 2.5V C_L = 20pF, OV_{DD} = 1.71V	● ● ●		7.5 8 9.5	ns ns ns
t_{HSDO}	SDO Data Remains Valid Delay from SCK↑	C_L = 20pF (Note 6)	●	1		ns
$t_{DSDOBUSYL}$	SDO Data Valid Delay from BUSY↓	C_L = 20pF (Note 6)	●		5	ns
t_{EN}	Bus Enable Time After RDL↓	(Note 13)	●		16	ns
t_{DIS}	Bus Relinquish Time After RDL↑	(Note 13)	●		13	ns
t_{WAKE}	REFBUF Wake-Up Time	C_{REFBUF} = 47µF, C_{REFIN} = 0.1µF		200		ms
$t_{CNVMRST}$	CNV↑ to MUX Starts Resetting Delay		●		38	ns
t_{MRST1}	MUX Reset Time During Conversion		●		36	ns
$t_{VLDMRST}$	8th SCK↑ to MUX Starts Resetting Delay After Programming 1st Valid Configuration Word		●		40	ns
t_{MRST2}	MUX Reset Time During Acquisition After Programming 1st Valid Configuration Word		●		42	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to ground.

Note 3: When these pin voltages are taken below ground or above V_{DD} or OV_{DD}, they will be clamped by internal diodes. This product can handle input currents up to 100mA below ground or above V_{DD} or OV_{DD} without latchup.

Note 4: V_{DD} = 5V, OV_{DD} = 2.5V, f_{SMPL} = 1MHz, REFIN = 2.048V unless otherwise noted.

Note 5: Recommended operating conditions.

Note 6: Guaranteed by design, not subject to test.

Note 7: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 8: Fully differential zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0111 1111 1111 1111 and 1000 0000 0000 0000 in straight binary format and 0000 0000 0000 0000 and 1111 1111 1111 1111 in two's complement format. Unipolar zero-scale error is the offset voltage measured from 0.5LSB when the output code flickers between 0000 0000 0000 0000 and 0000 0000 0000 0001. Bipolar zero-scale error is the offset voltage measured from –0.5LSB when the output code flickers between 0000 0000 0000 0000 and 1111 1111 1111 1111. Fully differential full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error. Unipolar full-scale error is the deviation of the last code transition from the ideal and includes the effect of offset error. Bipolar full-scale error is the worst-case deviation of the first and last code transitions from ideal and includes the effect of offset error.

Note 9: When REFBUF is overdriven, the internal reference buffer must be turned off by setting REFIN = 0V.

Note 10: All specifications in dB are referred to a full-scale $\pm V_{REFBUF}$ (fully differential), 0V to V_{REFBUF} (pseudo-differential unipolar), or $\pm V_{REFBUF}/2$ (pseudo-differential bipolar) input.

Note 11: Temperature coefficient is calculated by dividing the maximum change in output voltage by the specified temperature range.

Note 12: f_{SMPL} = 1MHz, I_{REFBUF} varies proportionally with sample rate.

Note 13: Parameter tested and guaranteed at OV_{DD} = 1.71V, OV_{DD} = 2.5V and OV_{DD} = 5.25V.

Note 14: t_{SCK} of 10ns maximum allows a shift clock frequency up to 100MHz for rising edge capture.

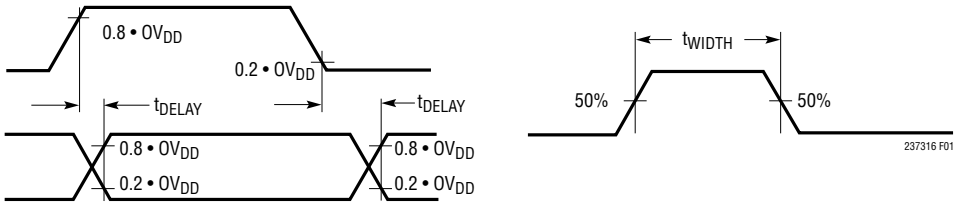
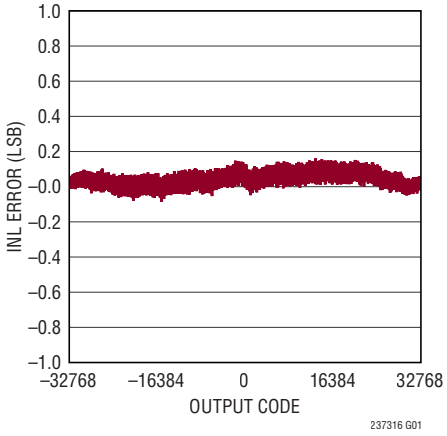


Figure 1. Voltage Levels for Timing Specifications

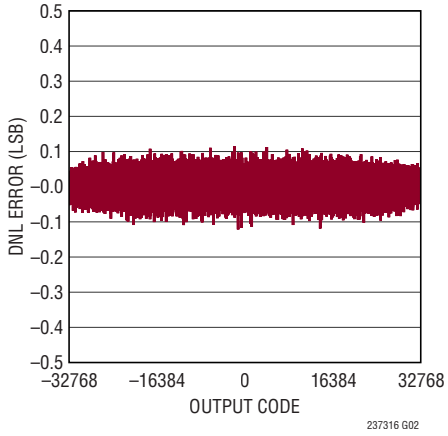
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Fully Differential Range, V_{CM} = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

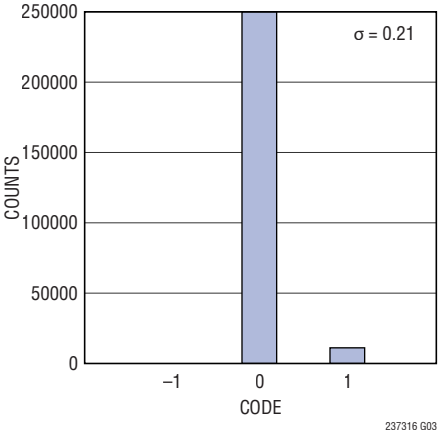
Integral Nonlinearity vs Output Code



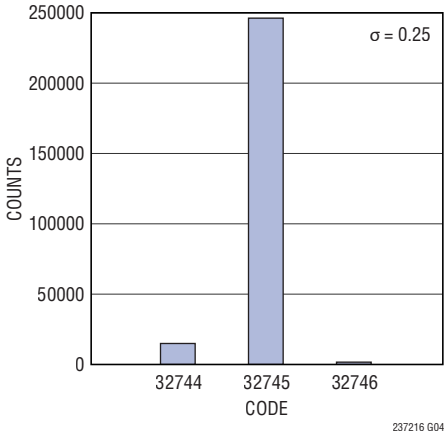
Differential Nonlinearity vs Output Code



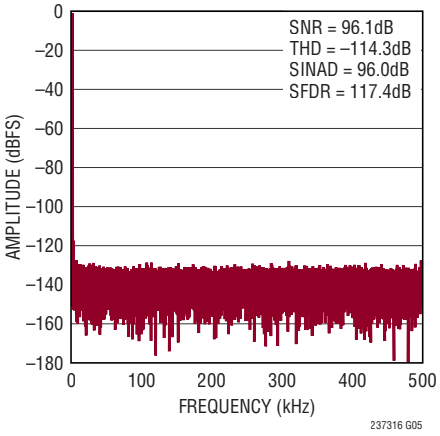
DC Histogram (Zero-Scale)



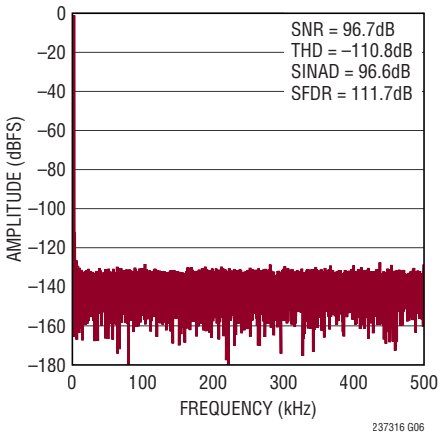
DC Histogram (Near Full-Scale)



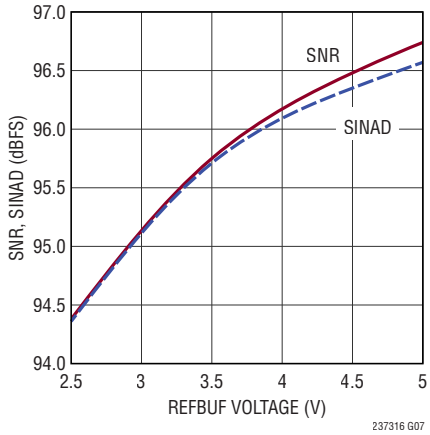
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



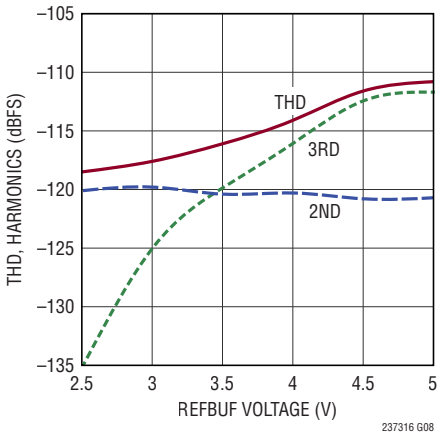
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



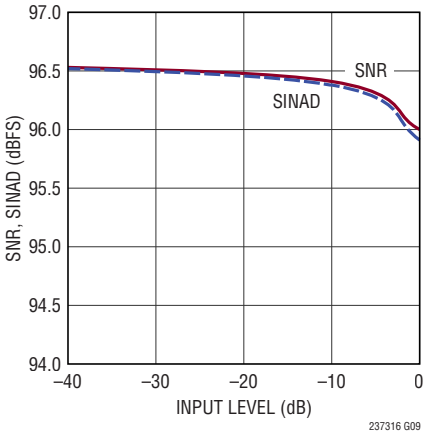
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



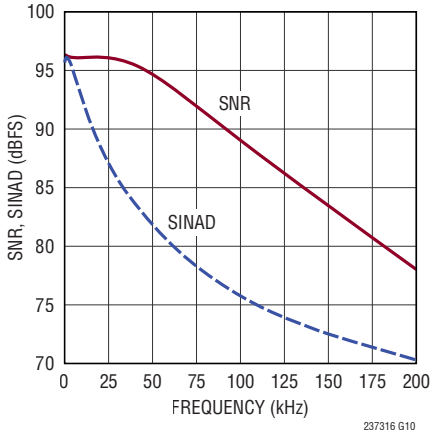
SNR, SINAD vs Input Level, f_{IN} = 1kHz



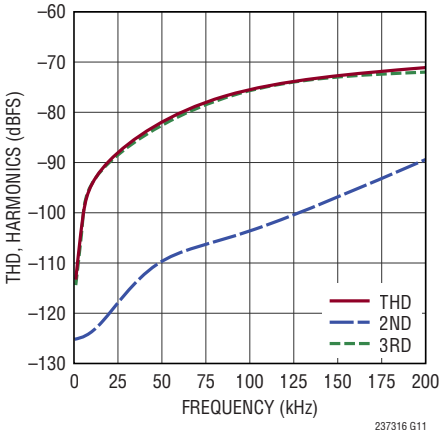
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Fully Differential Range, V_{CM} = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

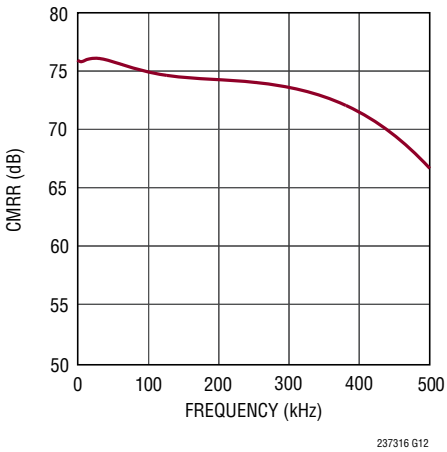
SNR, SINAD vs Input Frequency



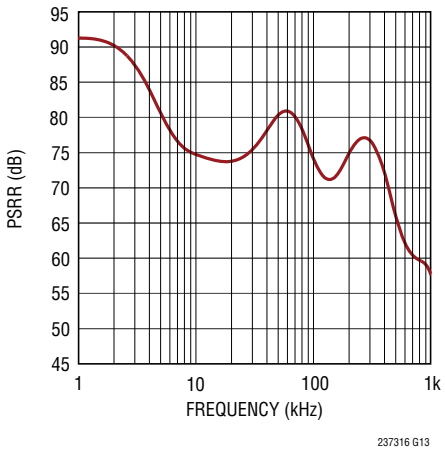
THD, Harmonics vs Input Frequency



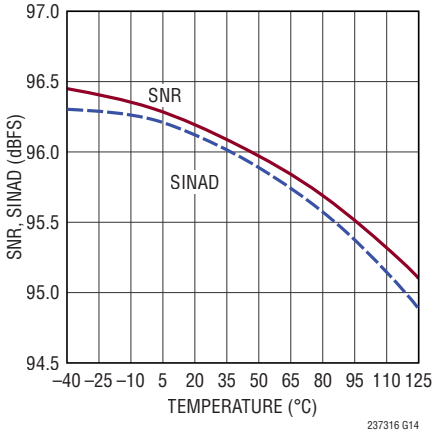
CMRR vs Input Frequency



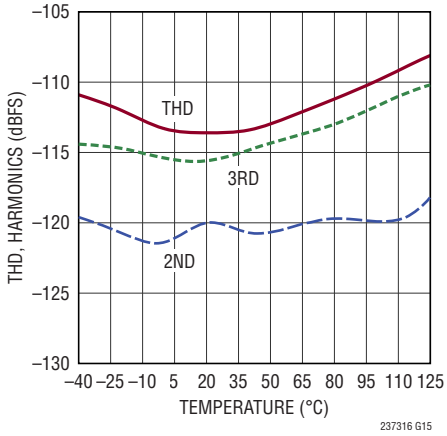
PSRR vs Frequency



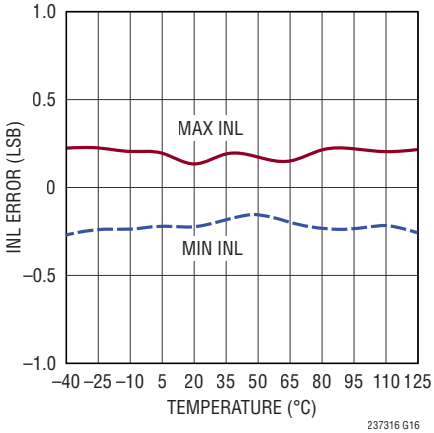
SNR, SINAD vs Temperature, f_{IN} = 1kHz



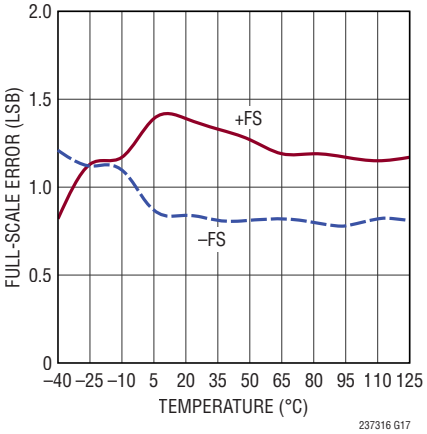
THD, Harmonics vs Temperature, f_{IN} = 1kHz



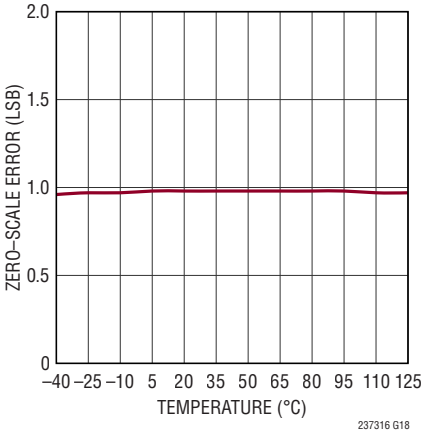
INL vs Temperature



Full-Scale Error vs Temperature REFBUF = 4.096V



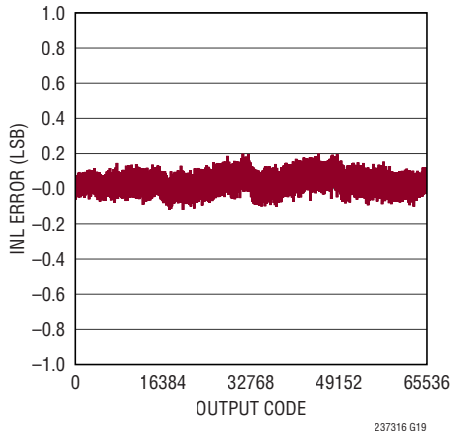
Zero-Scale Error vs Temperature



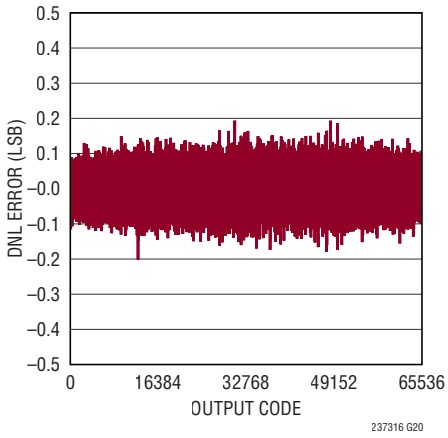
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Unipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

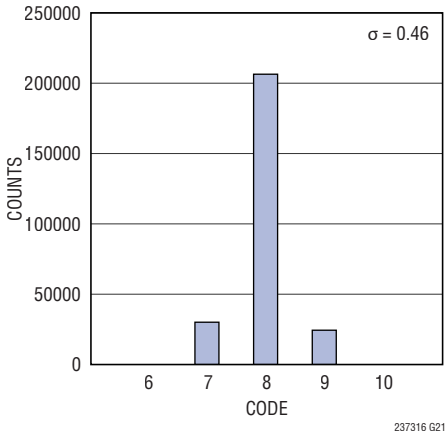
Integral Nonlinearity vs Output Code



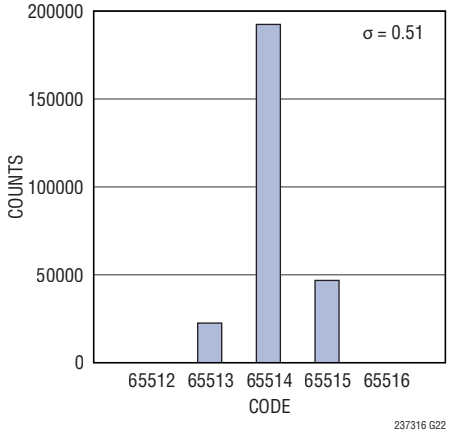
Differential Nonlinearity vs Output Code



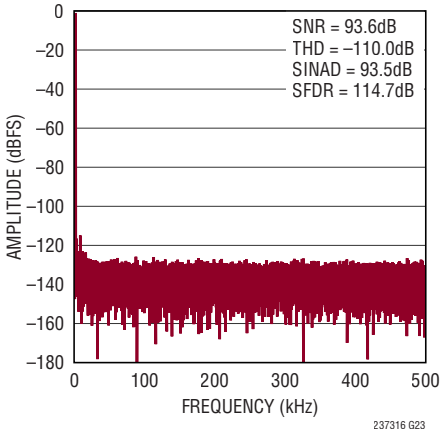
DC Histogram (Zero-Scale)



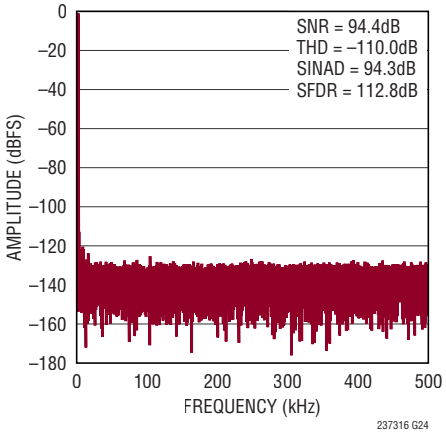
DC Histogram (Near Full-Scale)



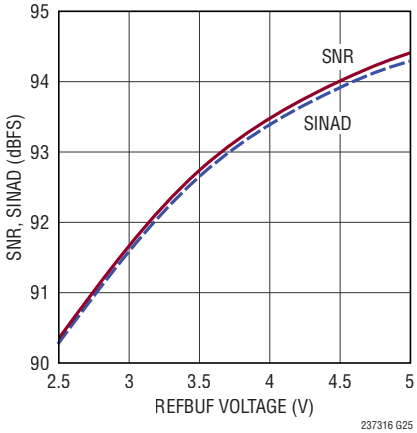
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



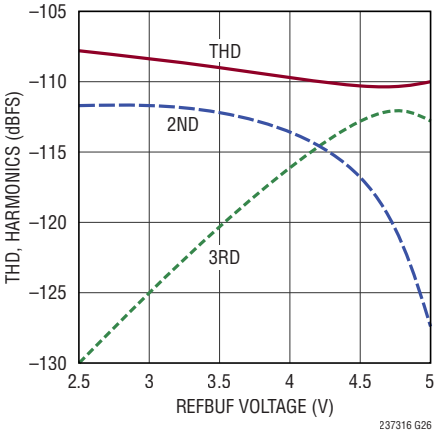
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



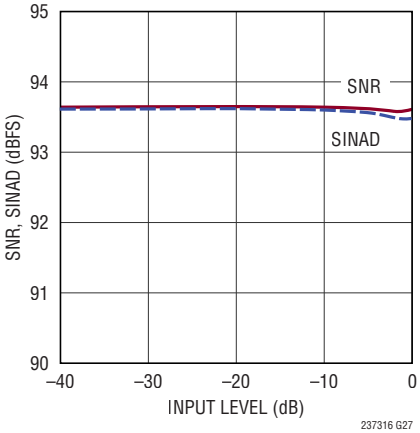
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



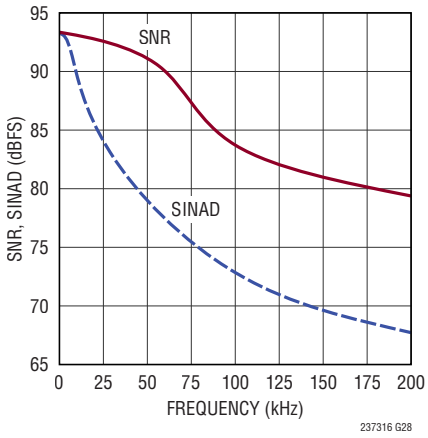
SNR, SINAD vs Input Level, f_{IN} = 1kHz



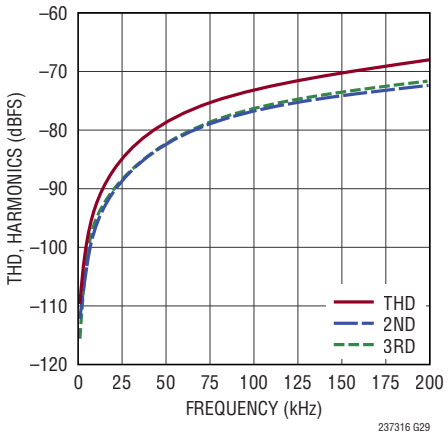
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Unipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

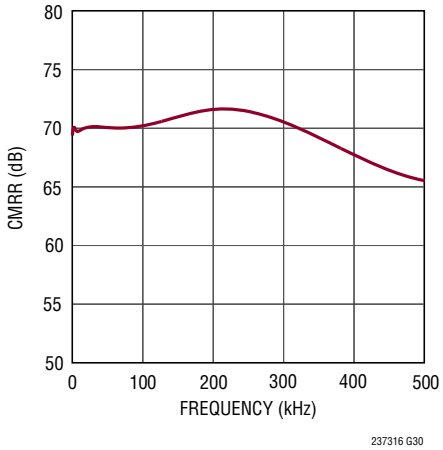
SNR, SINAD vs Input Frequency



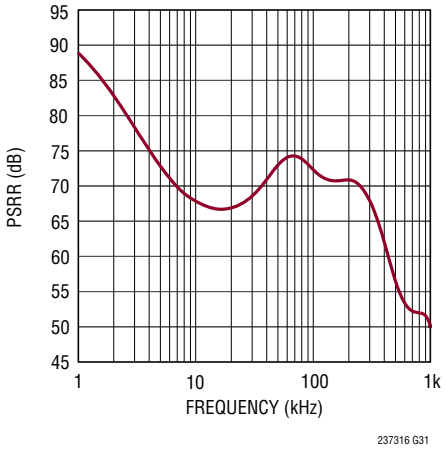
THD, Harmonics vs Input Frequency



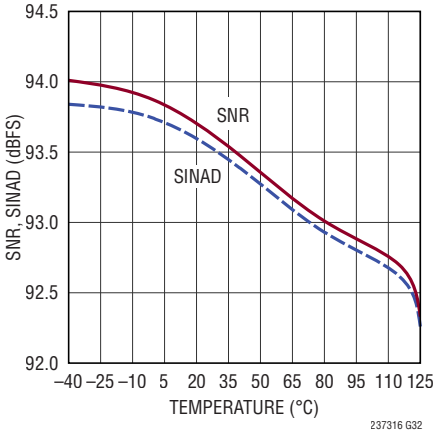
CMRR vs Input Frequency



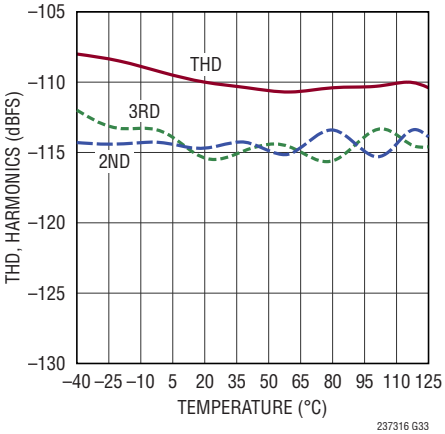
PSRR vs Frequency



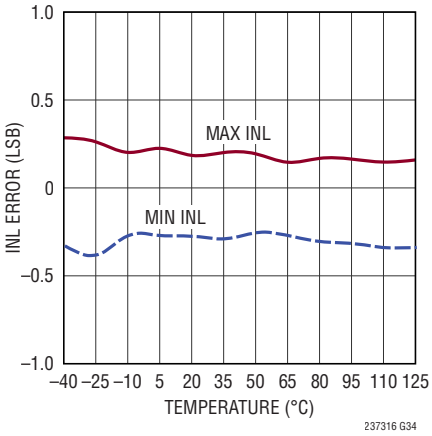
SNR, SINAD vs Temperature, f_{IN} = 1kHz



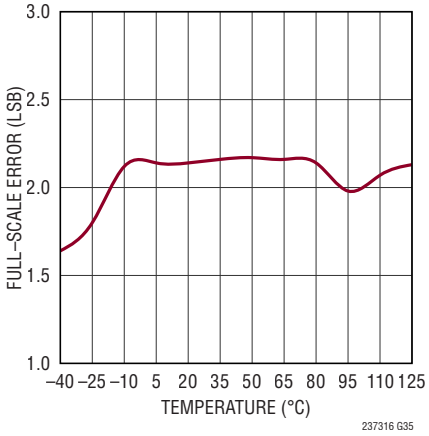
THD, Harmonics vs Temperature, f_{IN} = 1kHz



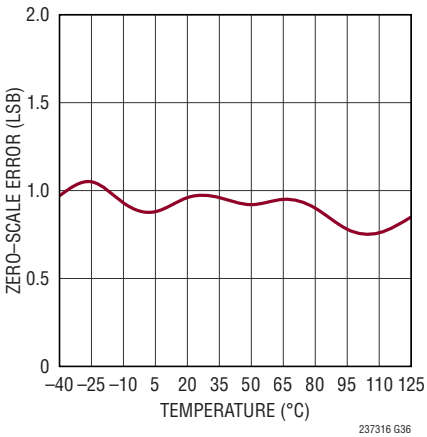
INL vs Temperature



Full-Scale Error vs Temperature REFBUF = 4.096V



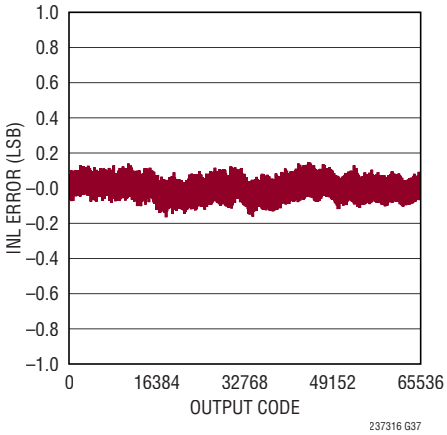
Zero-Scale Error vs Temperature



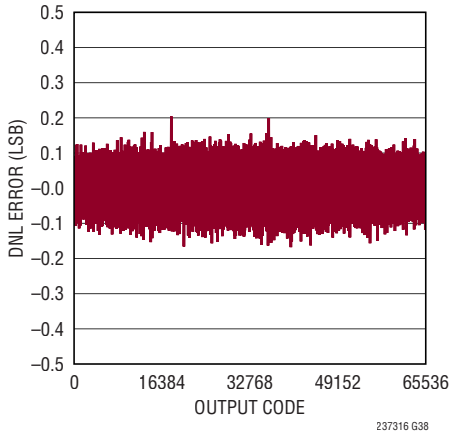
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Bipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

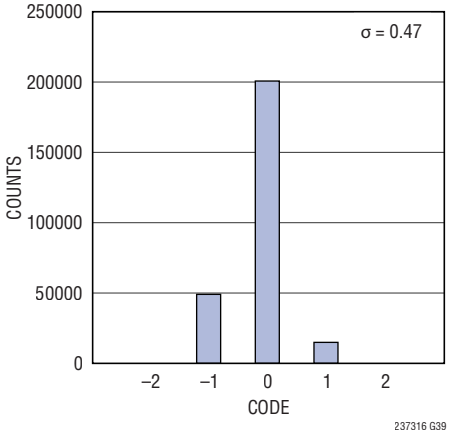
Integral Nonlinearity vs Output Code



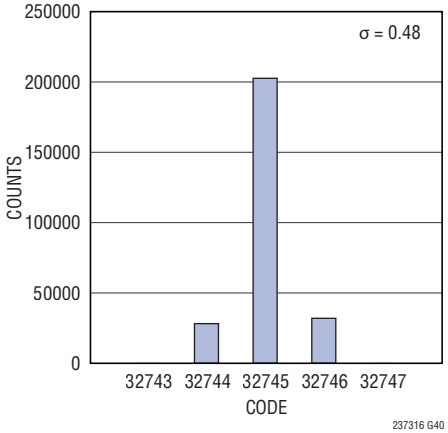
Differential Nonlinearity vs Output Code



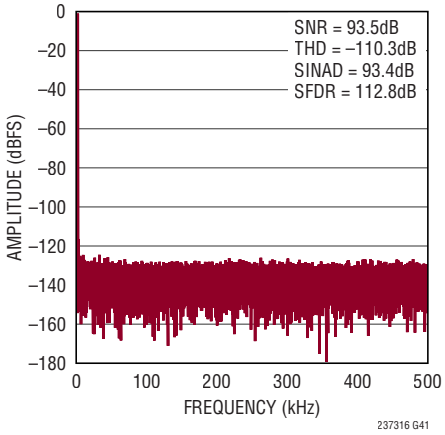
DC Histogram (Zero-Scale)



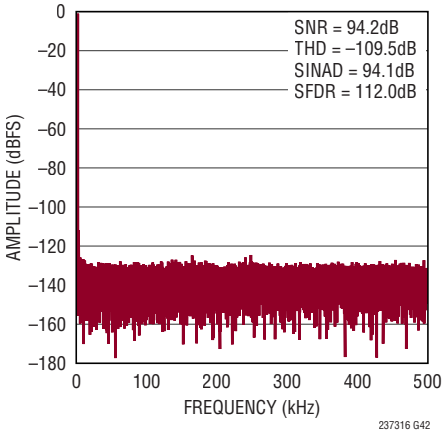
DC Histogram (Near Full-Scale)



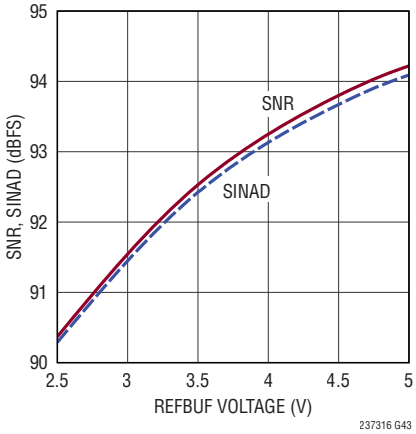
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz



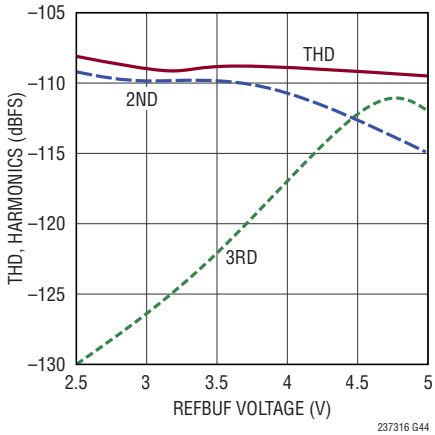
32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz, REFBUF = 5V



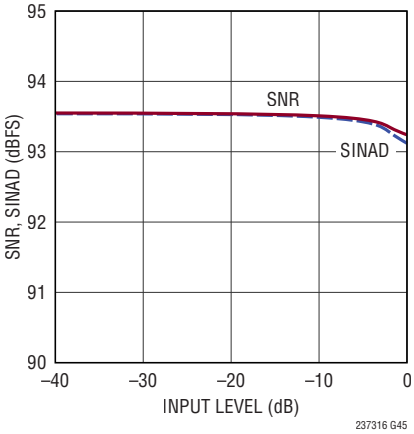
SNR, SINAD vs REFBUF, f_{IN} = 1kHz



THD, Harmonics vs REFBUF, f_{IN} = 1kHz



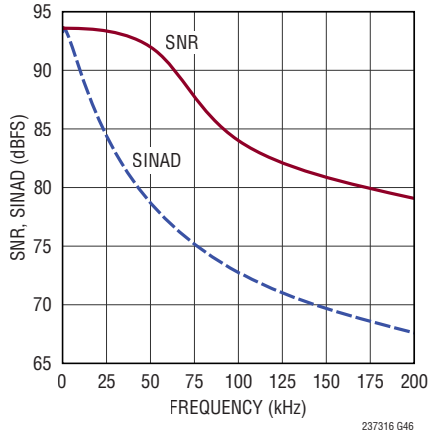
SNR, SINAD vs Input Level, f_{IN} = 1kHz



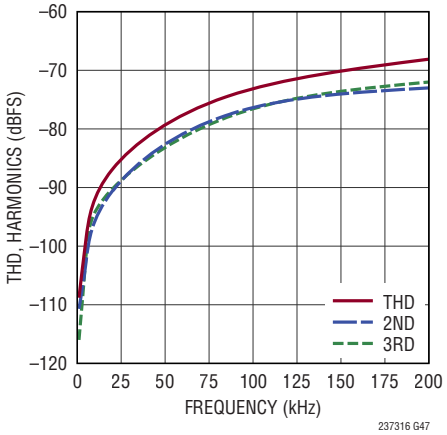
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, Pseudo-Differential Bipolar Range, f_{SMPL} = 1Msps, unless otherwise noted.

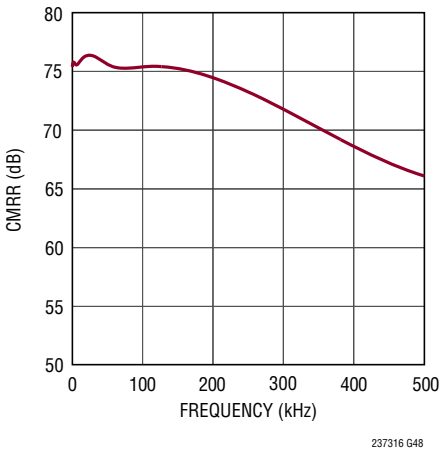
SNR, SINAD vs Input Frequency



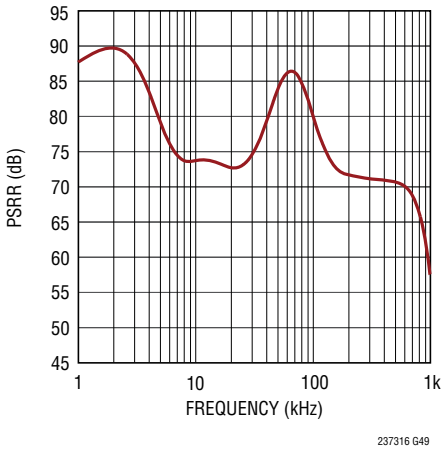
THD, Harmonics vs Input Frequency



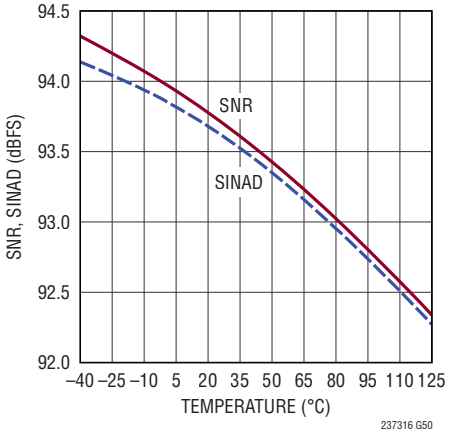
CMRR vs Input Frequency



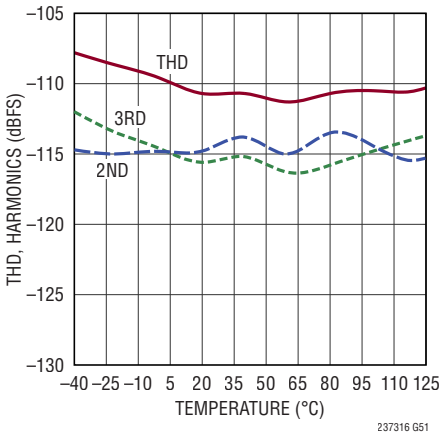
PSRR vs Frequency



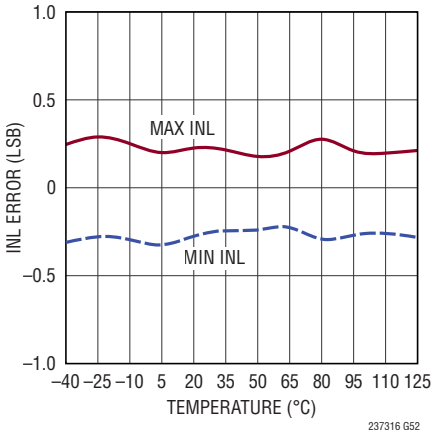
SNR, SINAD vs Temperature, f_{IN} = 1kHz



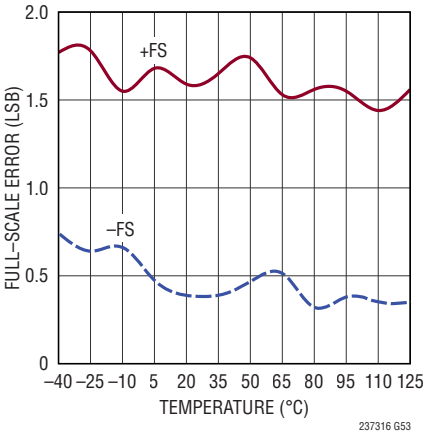
THD, Harmonics vs Temperature, f_{IN} = 1kHz



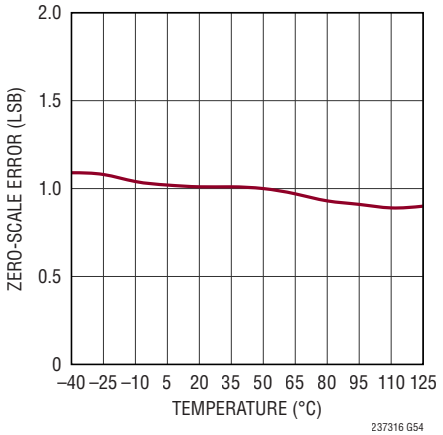
INL vs Temperature



Full-Scale Error vs Temperature REFBUF = 4.096V



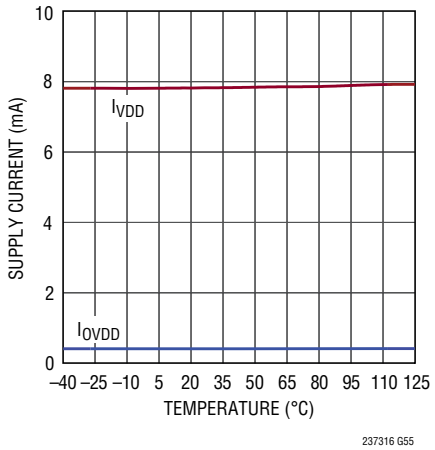
Zero-Scale Error vs Temperature



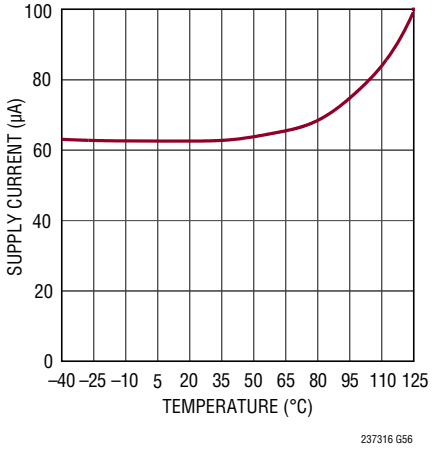
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_{DD} = 5V, OV_{DD} = 2.5V, REFIN = 2.048V, f_{SMPL} = 1Msps, unless otherwise noted.

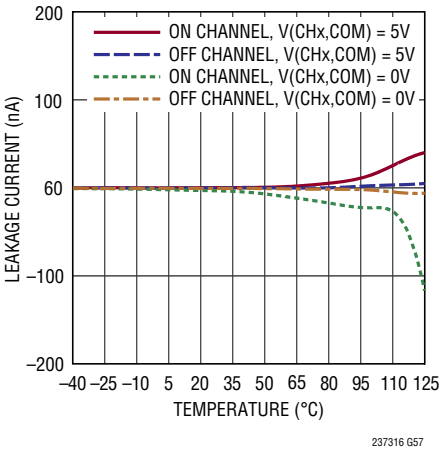
Supply Current vs Temperature



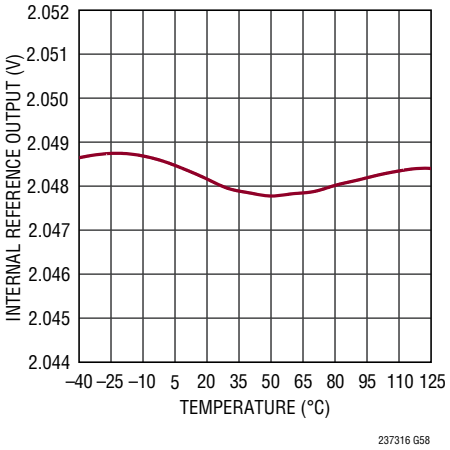
Sleep Current vs Temperature



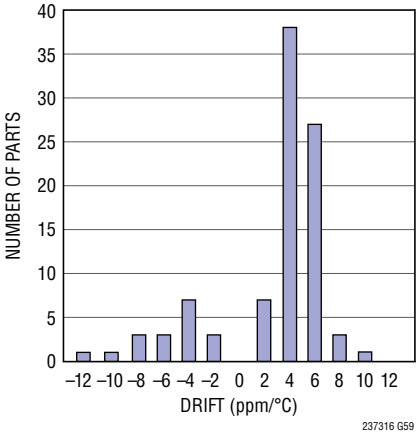
Input Leakage Current vs Temperature (MUXOUT± Shorted to ADCIN±)



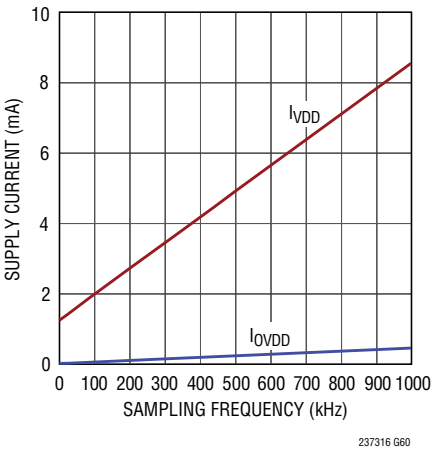
Internal Reference Output vs Temperature



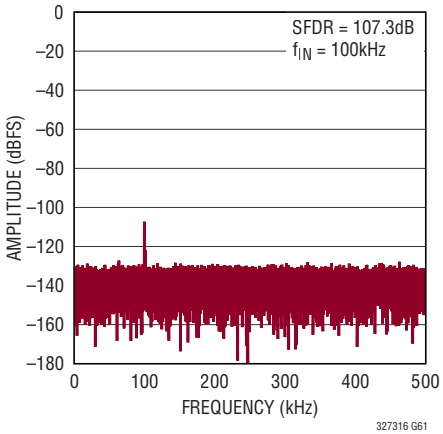
Internal Reference Output Temperature Coefficient Distribution



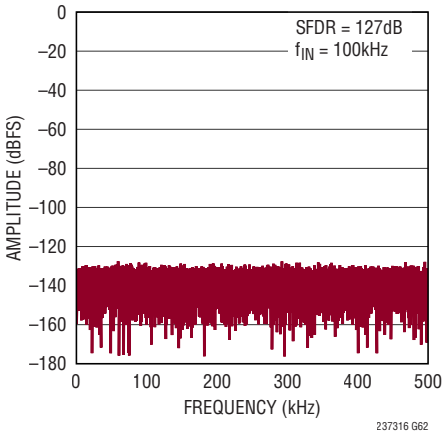
Supply Current vs Sampling Rate



Crosstalk FFT (AC Crosstalk-Channel Adjacent to MUXOUT)



Crosstalk FFT (AC Crosstalk-Channel NOT Adjacent to MUXOUT)



PIN FUNCTIONS

CH0 to CH7 (Pins 1, 2, 7, 8, 9, 10, 31 and 32): Analog Inputs. CH0 to CH7 can be configured as single-ended inputs relative to COM, or as pairs of differential input channels. See the Analog Input Multiplexer section. Unused analog inputs should be tied to a DC voltage within the analog input voltage range of (GND – 0.3V) to (V_{DD} + 0.3V) as specified in Absolute Maximum Ratings.

MUXOUT$^+$, MUXOUT$^-$ (Pin 3, Pin 6): Analog Output Pins of MUX.

ADCIN$^+$, ADCIN$^-$ (Pin 4, Pin 5): Analog Input Pins of ADC Core.

GND (Pins 11, 14, 15, 17, 23, 26, 27 and Exposed Pad Pin 33): Ground.

REFBUF (Pin 12): Reference Buffer Output. An onboard buffer nominally outputs 4.096V to this pin. This pin is referred to GND and should be decoupled closely to the pin with a 47µF ceramic capacitor. The internal buffer driving this pin may be disabled by grounding its input at REFIN. Once the buffer is disabled, an external reference may overdrive this pin in the range of 2.5V to 5V. A resistive load greater than 500k can be placed on the reference buffer output.

REFIN (Pin 13): Reference Output/Reference Buffer Input. An onboard bandgap reference nominally outputs 2.048V at this pin. Bypass this pin with a 0.1µF ceramic capacitor to GND to limit the reference output noise. If more accuracy is desired, this pin may be overdriven by an external reference in the range of 1.25V to 2.4V.

CNV (Pin 16): Convert Input. A rising edge on this input powers up the part and initiates a new conversion. Logic levels are determined by OV_{DD}.

RDL (Pin 18): Read Low Input. When RDL is low, the serial data I/O bus is enabled. When RDL is high, the serial data I/O bus becomes Hi-Z. RDL also gates the external shift clock. Logic levels are determined by OV_{DD}.

BUSY (Pin 19): BUSY Indicator. Goes high at the start of a new conversion and returns low when the conversion has finished. Logic levels are determined by OV_{DD}.

SDI (Pin 20): Serial Data Input. Data provided on this pin in synchrony with SCK can be used to program the MUX channel configuration, converter input range and digital gain compression setting via the sequencer. Input data on SDI is latched on rising edges of SCK when the serial data I/O bus is enabled. Logic levels are determined by OV_{DD}.

SCK (Pin 21): Serial Data Clock Input. When the serial data I/O bus is enabled, the conversion result followed by configuration information is shifted out at SDO on the rising edges of this clock MSB first. Serial input data is latched on the rising edges of this clock at SDI. Logic levels are determined by OV_{DD}.

SDO (Pin 22): Serial Data Output. The conversion result followed by configuration information is output on this pin on each rising edge of SCK MSB first when the serial data I/O bus is enabled. The output data format is determined by the converter operating mode. Logic levels are determined by OV_{DD}.

RESET (Pin 24): Reset Input. When this pin is brought high, the LTC2373-16 is reset. If this occurs during a conversion, the conversion is halted and the data bus becomes Hi-Z. Logic levels are determined by OV_{DD}.

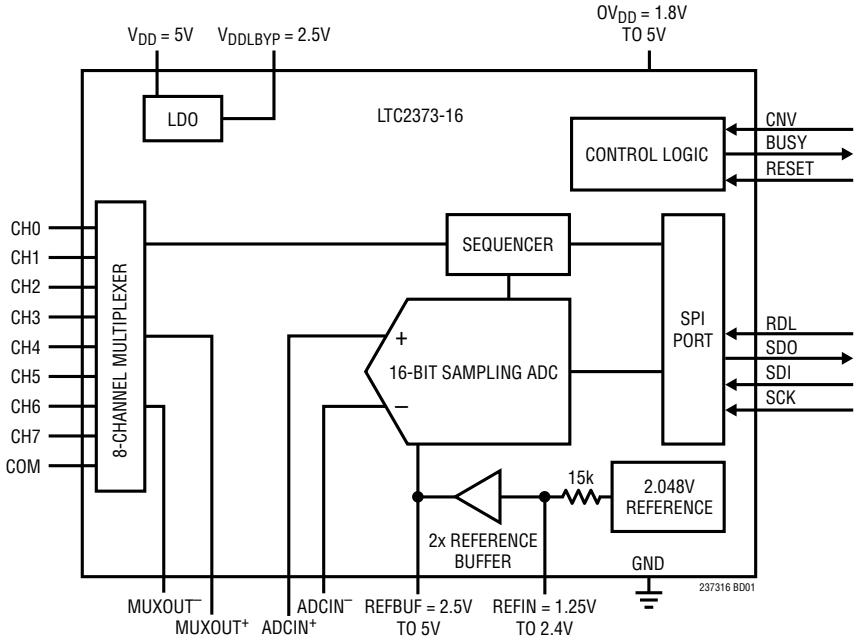
OV_{DD} (Pin 25): I/O Interface Digital Power. The range of OV_{DD} is 1.71V to 5.25V. This supply is nominally set to the same supply as the host interface (1.8V, 2.5V, 3.3V, or 5V). Bypass OV_{DD} to GND with a 0.1µF capacitor.

V_{DDLBYP} (Pin 28): 2.5V Supply Bypass Pin. The voltage on this pin is generated via an onboard regulator off of V_{DD}. This pin must be bypassed with a 2.2µF ceramic capacitor to GND. Applying an external voltage to this pin can cause damage to the IC or improper operation.

V_{DD} (Pin 29): 5V Power Supply. The range of V_{DD} is 4.75V to 5.25V. Bypass V_{DD} to GND with a 10µF ceramic capacitor.

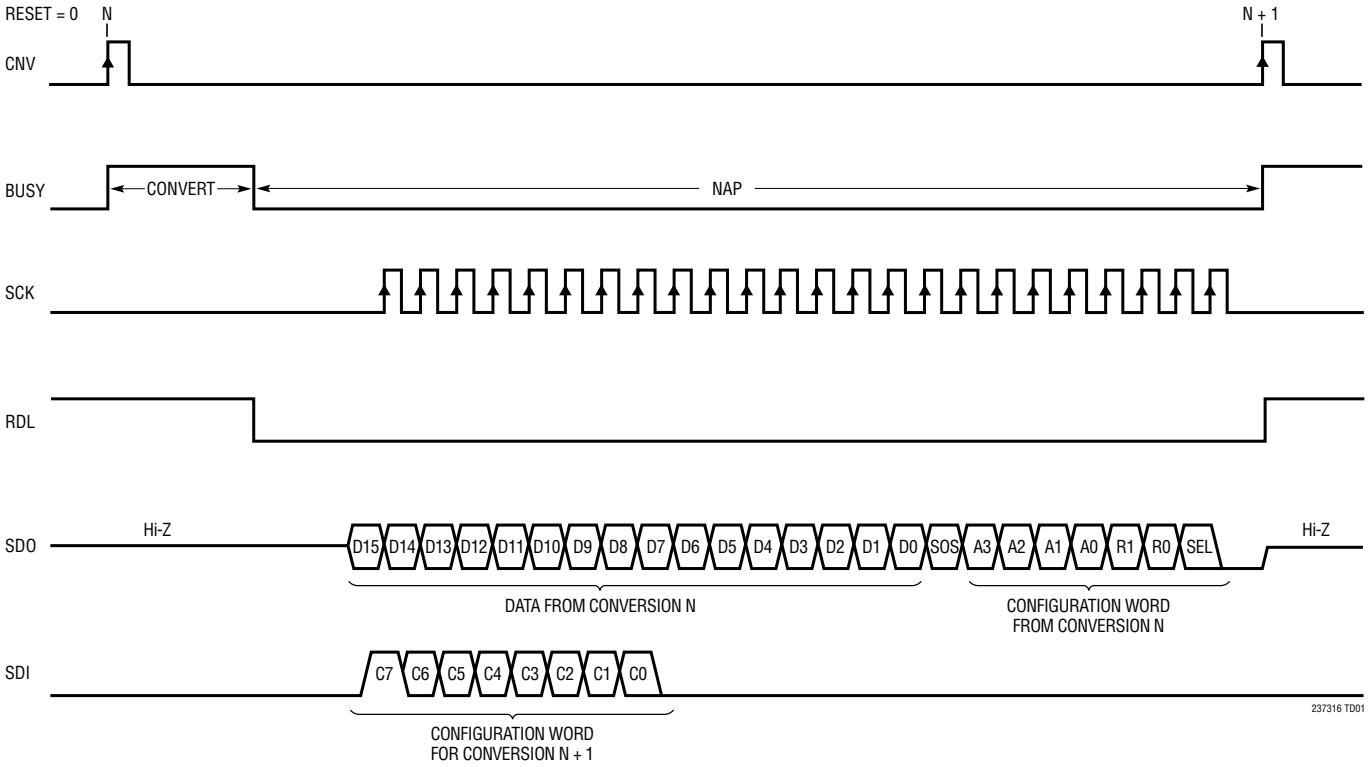
COM (Pin 30): Common Input. This is the reference point for all single-ended inputs. It must be free of noise and connected to GND for unipolar conversions and REFBUF/2 for bipolar conversions. If unused, this input should be tied to a DC voltage within the analog input voltage range of (GND – 0.3V) to (V_{DD} + 0.3V) as specified in Absolute Maximum Ratings.

FUNCTIONAL BLOCK DIAGRAM



TIMING DIAGRAM

Typical Conversion and Serial Interface Timing



APPLICATIONS INFORMATION

OVERVIEW

The LTC2373-16 is a low noise, high speed, highly configurable 8-channel 16-bit successive approximation register (SAR) ADC. The LTC2373-16 features a low crosstalk 8-channel input multiplexer (MUX) and a high performance 16-bit accurate ADC core that can be configured to accept fully-differential, pseudo-differential unipolar and pseudo-differential bipolar input signals. The input range of the ADC core can be set independently of the MUX input channel configuration. The outputs of the MUX and inputs of the ADC core are pinned out, allowing flexibility in how the MUX is connected to the ADC core. The MUX may be wired directly to the ADC core or signal conditioning circuitry may be inserted between the MUX and ADC core, depending on the application. The LTC2373-16 also has a selectable digital gain compression (DGC) feature. The LTC2373-16 has a programmable sequencer that can be programmed with configuration words ranging from a depth of one up to a maximum depth of 16 configuration words.

The LTC2373-16 has an onboard low drift reference and a single-shot capable reference buffer. The LTC2373-16 also has a high speed SPI-compatible serial interface that supports 1.8V, 2.5V, 3.3V and 5V logic. The LTC2373-16 automatically naps between conversions, leading to reduced power dissipation that scales with the sampling rate. A sleep mode is also provided for further power savings during inactive periods.

CONVERTER OPERATION

The LTC2373-16 operates in two phases. During the acquisition phase when $MUXOUT^{+/-}$ is wired to $ADCIN^{+/-}$, the charge redistribution capacitor D/A converter (CDAC) is connected through the MUX to the selected MUX analog input pins. A rising edge on the CNV pin initiates a conversion. During the conversion phase, the 16-bit CDAC is sequenced through a successive approximation algorithm, effectively comparing the sampled input with binary-weighted fractions of the reference voltage (e.g. $V_{REFBUF}/2$, $V_{REFBUF}/4$ … $V_{REFBUF}/65536$) using a differential comparator. At the end of conversion, the CDAC output approximates the sampled analog input. The ADC control logic then prepares the 16-bit digital output code for serial transfer.

TRANSFER FUNCTION

The LTC2373-16 digitizes the full-scale voltage of 2 × REFBUF in fully differential mode and REFBUF in pseudo-differential mode into 2^{16} levels. With REFBUF = 4.096V, the resulting LSB sizes in fully differential and pseudo-differential modes are 125µV and 62.5µV, respectively. The binary format of the conversion result depends on the converter input range as described in Table 6. The ideal two's complement transfer function is shown in Figure 2, while the ideal straight binary transfer function is shown in Figure 3. The ideal straight binary transfer function can be obtained from the two's complement transfer function by inverting the most significant bit (MSB) of each output code.

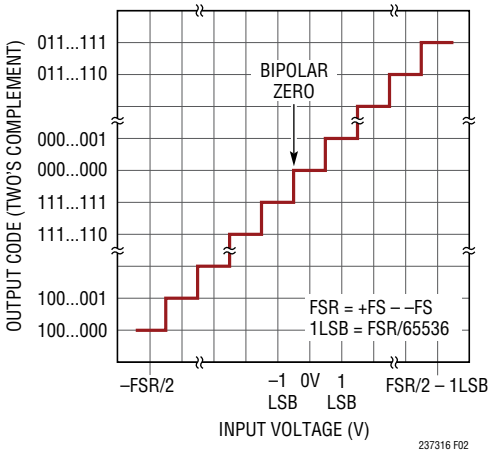


Figure 2. LTC2373-16 Two's Complement Transfer Function. Straight Binary Transfer Function Can Be Obtained by Inverting the Most Significant Bit (MSB) of Each Output Code

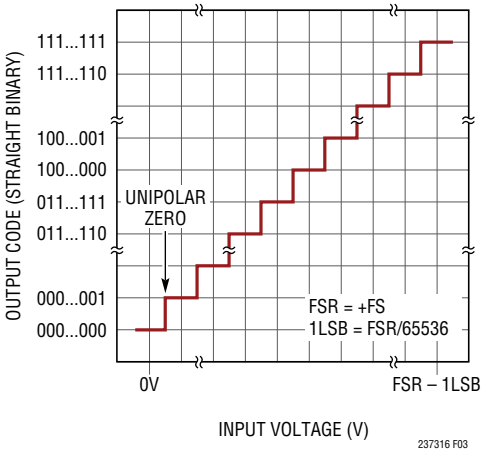


Figure 3. LTC2373-16 Straight Binary Transfer Function.

APPLICATIONS INFORMATION

ANALOG INPUTS

The LTC2373-16 can be configured to accept one of three voltage ranges: fully differential (±4.096V), pseudo-differential unipolar (0V to 4.096V), and pseudo-differential bipolar (±2.048V). In all three ranges, the ADC samples and digitizes the voltage difference between the two ADC core analog input pins ($ADCIN^+ – ADCIN^–$), and any unwanted signal that is common to both inputs is reduced by the common mode rejection ratio (CMRR) of the ADC. The MUX outputs the voltages of the selected MUX analog input channels to $MUXOUT^{+/–}$, according to the MUX configuration. $MUXOUT^{+/–}$ may be wired directly to $ADCIN^{+/–}$ or connected through a buffer. Refer to the Configuring the LTC2373-16 section for details on how to select the analog input range and MUX channel configuration.

Independent of the selected range or channel configuration, the MUX analog inputs can be modeled by the equivalent circuit shown in Figure 4. CHx and CHy are distinct input pins selected from the CH0 to CH7 MUX analog inputs, depending on the MUX configuration. Each pin has ESD protection diodes. The ADC core analog inputs, $ADCIN^{+/–}$, each see a sampling network consisting of approximately 50pF (C_{IN}) from the sampling CDAC in series with 40Ω (R_{ON}) from the on-resistance of the sampling switch. The MUX is modeled by a 40Ω resistor representing the MUX switch on-resistance (R_{SW}) and a capacitance to ground, C_{PAR}, at the output summing node of the MUX. C_{PAR} is a lumped capacitance on the order of 20pF formed primarily by pin parasitics and diode junctions. Parasitic capacitances from the PCB will also contribute to C_{PAR}. This capacitance is discharged through a switch to ground every conversion cycle or when a first new configuration is programmed to minimize crosstalk due to charge sharing between channels.

During acquisition, each active MUX analog input sees a cascade of two first order lowpass filters formed by R_{SW}, C_{PAR} and the ADC sampling network when $MUXOUT^{+/–}$ is wired directly to $ADCIN^{+/–}$. If a buffer is inserted between $MUXOUT^{+/–}$ and $ADCIN^{+/–}$, then each active MUX analog input only sees a first order lowpass filter formed by R_{SW} and C_{PAR} that is loaded with the input impedance of the buffer.

Both C_{IN} and C_{PAR} draw current spikes while being charged during acquisition. If $MUXOUT^{+/–}$ is wired directly to $ADCIN^{+/–}$, the current spikes from the charging of both capacitors are drawn from the active MUX analog inputs. A buffer inserted between $MUXOUT^{+/–}$ and $ADCIN^{+/–}$ will absorb the current spike from C_{IN}, leaving the current spike from C_{PAR} to be drawn from the active MUX analog inputs. During conversion and sleep, the MUX analog inputs and ADC core analog inputs draw only a small leakage current.

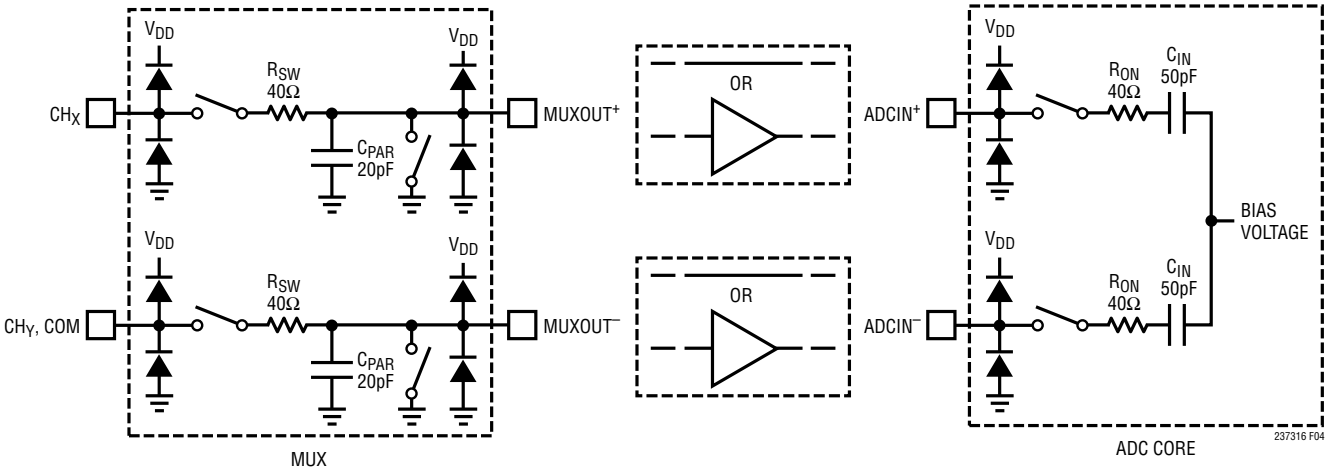


Figure 4. Equivalent Circuit for the Differential Analog Inputs of the LTC2373-16

APPLICATIONS INFORMATION

Fully Differential Input Range

The fully differential input range provides the widest input signal swing, configuring the ADC to digitize the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of $\pm V_{REFBUF}$. In this range, the $ADCIN^+$ and $ADCIN^-$ pins should be driven 180 degrees out-of-phase with respect to each other, centered around a common mode voltage ($(ADCIN^+ + ADCIN^-)/2$ that is restricted to ($V_{REFBUF}/2 \pm 0.1V$). Both the $ADCIN^+$ and $ADCIN^-$ pins are allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format may be selected as straight binary or two's complement.

Pseudo-Differential Unipolar Input Range

In the pseudo-differential unipolar input range, the ADC digitizes the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of (0V to V_{REFBUF}). In this range, a single-ended unipolar input signal, driven on the $ADCIN^+$ pin, is measured with respect to the signal ground reference level, driven on the $ADCIN^-$ pin. The $ADCIN^+$ pin is allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$), while the $ADCIN^-$ pin is restricted to (GND ± 0.1V). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format is straight binary.

Pseudo-Differential Bipolar Input Range

In the pseudo-differential bipolar input range, the ADC digitizes the differential analog input voltage to the ADC core ($ADCIN^+ - ADCIN^-$) provided through the selected MUX analog inputs over a span of ($\pm V_{REFBUF}/2$). In this range, a single-ended bipolar input signal, driven on the $ADCIN^+$ pin, is measured with respect to the signal mid-scale reference level, driven on the $ADCIN^-$ pin. The $ADCIN^+$ pin is allowed to swing from (GND – 0.1V) to ($V_{REFBUF} + 0.1V$), while the $ADCIN^-$ pin is restricted to ($V_{REFBUF}/2 \pm 0.1V$). Unwanted signals common to both inputs are reduced by the CMRR of the ADC. The output data format is two's complement.

INPUT DRIVE CIRCUITS

Whether $MUXOUT^{+/-}$ is wired directly to $ADCIN^{+/-}$ or through a buffer with high input impedance, the MUX analog inputs of the LTC2373-16 are high impedance. In either case, a low impedance source can directly drive the MUX analog inputs without gain error. A high impedance source should be buffered in both cases to minimize settling time during acquisition and to optimize ADC linearity.

For best performance, a buffer amplifier should be used to drive the MUX analog inputs of the LTC2373-16 with $MUXOUT^{+/-}$ wired directly to $ADCIN^{+/-}$. The amplifier provides low output impedance, which produces fast settling of the analog signal during the acquisition phase. It also provides isolation between the signal source and the current spikes drawn by the MUX analog inputs when entering acquisition.

Noise and Distortion

The noise and distortion of the buffer amplifiers and signal sources must be considered since they add to the ADC noise and distortion. Noisy input signals should be filtered prior to the inputs of the buffers driving the MUX analog inputs with an appropriate filter to minimize noise. The simple 1-pole RC lowpass filter (LPF1) shown in Figure 5 is sufficient for many applications.

Buffer amplifiers with low noise density must be selected to minimize SNR degradation. Coupling filter networks (LPF2) should be placed between the buffer outputs and MUX analog inputs to both minimize the noise contribution of the buffers and reduce disturbances reflected into the buffer from MUX analog input sampling transients. If a buffer amplifier is used between $MUXOUT^{+/-}$ and $ADCIN^{+/-}$, a coupling filter network (LPF3) should be placed between the buffer output and ADC core analog inputs to both minimize the noise contribution of the buffer and reduce disturbances reflected into the buffer from the ADC core analog input sampling transients. Long RC time constants at the MUX or ADC core analog inputs will slow down the settling of those inputs. Therefore, LPF2 and LPF3 typically require wider bandwidths than LPF1.

APPLICATIONS INFORMATION

Table 1 lists typical recommended values for the R and C of each LPF mentioned.

Table 1. Recommended R and C Values for Each Lowpass Filter

	Rx(Ω)	Cx(pF)	BANDWIDTH
LPF1	50	100000	31.8kHz
LPF2	10	1200	13MHz
LPF3	25	2700	2.4MHz

High quality capacitors and resistors should be used in the RC filters since these components can add distortion. NPO and silver mica type dielectric capacitors have excellent linearity. Carbon surface mount resistors can generate distortion from self heating and from damage that may occur during soldering. Metal film surface mount resistors are much less susceptible to both problems.

Input Currents

One of the biggest challenges in coupling an amplifier to the LTC2373-16 is in dealing with current spikes drawn by the MUX and ADC core analog inputs at the start of each acquisition phase. LPF2 and LPF3 are examples of coupling filters that are used to both filter noise and reduce sampling transients due to the current spikes.

The MUX and ADC core analog inputs may be modeled as a switched capacitor load on the drive circuit. A drive circuit may rely partially on attenuating switched-capacitor current spikes with small filter capacitors C_{FILT} placed directly at the ADC inputs and partially on the driver amplifier having sufficient bandwidth to recover from the residual disturbance. Amplifiers optimized for DC performance may not have sufficient bandwidth to fully recover at the ADC's maximum conversion rate, which can produce nonlinearity and other errors. Coupling filter circuits may be classified in three broad categories:

Fully Settled: This case is characterized by filter time constants and an overall settling time that are considerably shorter than the sample period. When acquisition begins, the coupling filter is disturbed. For a typical first order RC filter, the disturbance will look like an initial step with an exponential decay. The amplifier will have its own response to the disturbance, which may include ringing. If the input settles completely (to within the accuracy of the LTC2373-16), the disturbance will not contribute any error.

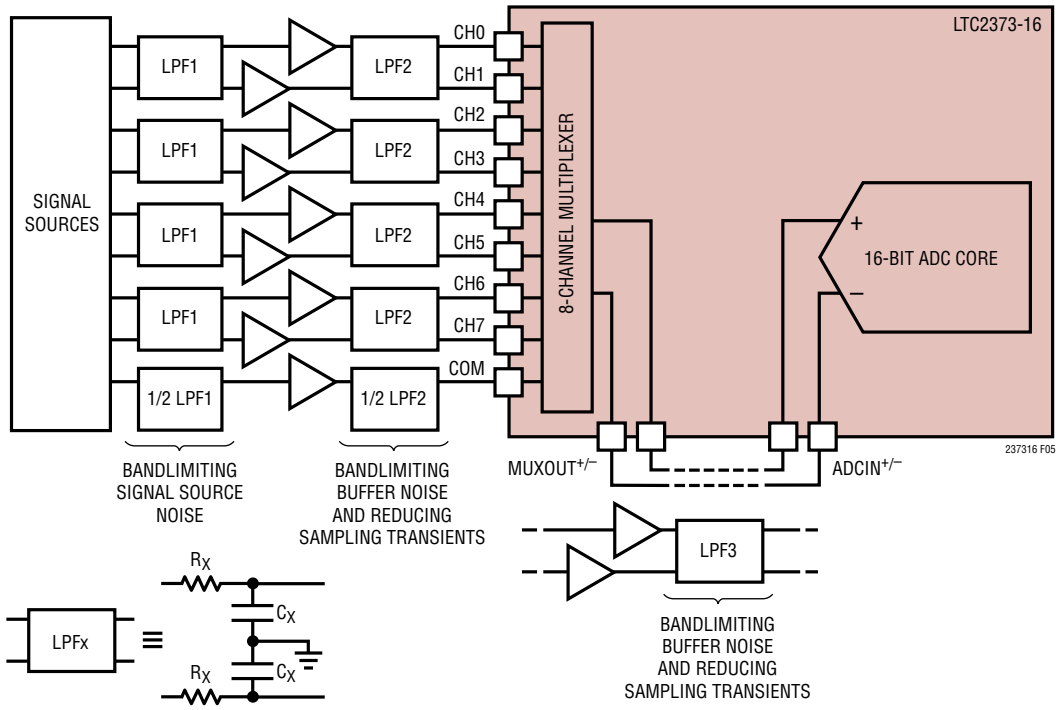


Figure 5. Input Signal Chain

APPLICATIONS INFORMATION

Partially Settled: In this case, the beginning of acquisition causes a disturbance of the coupling filter, which then begins to settle out towards the nominal input voltage. However, acquisition ends (and the conversion begins) before the input settles to its final value. This generally produces a gain error, but as long as the settling is linear, no distortion is produced. The coupling filter's response is affected by the amplifier's output impedance and other parameters. A linear settling response to fast switched-capacitor current spikes can NOT always be assumed for precision, low bandwidth amplifiers. The coupling filter serves to attenuate the current spikes' high frequency energy before it reaches the amplifier.

Fully Averaged: Consider the case where MUXOUT$^{+/-}$ is directly wired to ADCIN$^{+/-}$. If the coupling filter's capacitors (C_{FILT}) at the MUX analog inputs are much larger than the sum of the ADC's sample capacitors (50pF) and the MUX's output summing node capacitances (20pF), then the sampling glitch is greatly attenuated. The driving amplifier effectively only sees the average sampling current, which is quite small. At 1Msps, the equivalent input resistance is approximately 14k (as shown in Figure 6), a benign resistive load for most precision amplifiers. However, resistive voltage division will occur between the coupling filter's DC resistance and MUX's equivalent (switched-capacitor) input resistance, thus producing a gain error.

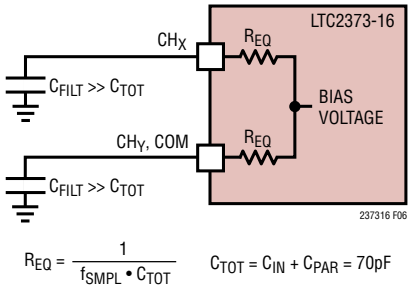


Figure 6. Equivalent Circuit for the MUX Analog Inputs of the LTC2373-16 at 1Msps

Crosstalk

Crosstalk is a typical concern in systems that employ multiplexers. The LTC2373-16 features a low crosstalk 8-channel MUX. There are two forms of crosstalk in the LTC2373-16 that potentially allow the signal from one channel to corrupt the signal from another channel being sampled.

The first form of crosstalk is often referred to as static crosstalk. In static crosstalk, a signal applied to an OFF channel, $V_{INTERFERER}$, couples capacitively into the input signal path, thus corrupting the input signal of the ON channel, V_{SIGNAL}. Figure 7 shows an RC model of two MUX input channels and the associated parasitic capacitances. Capacitive coupling from an OFF channel into the input signal path can occur through C_{SW} of an OFF switch to the MUXOUT$^{+/-}$ output pins or through C_{PIN} to an adjacent input pin or the MUXOUT$^{+/-}$ output pins. Coupling through C_{PIN} to the MUXOUT$^{+/-}$ pins is the dominant coupling mechanism that limits the crosstalk to –107dB with a 100kHz input signal applied to an OFF CH3 or CH4. These pins sit adjacent to the MUXOUT^{+} and MUXOUT^{-} pins, respectively.

The second form of crosstalk is referred to as adjacent channel crosstalk, which has to do with memory from the input of one channel affecting the sampled value of another channel. In this case, C_{PAR} at the output summing nodes of the MUX, MUXOUT$^{+/-}$, can act as memory storage elements if not dealt with properly. The potential crosstalk mechanism here is through charge sharing. C_{PAR} is charged approximately to the voltage of each channel that is sampled. If that charge is not cleared when switching from one channel to the next, then charge sharing between the charge on the filter capacitor (C_{FILT}) of one channel will occur with the charge from another channel stored on C_{PAR}. The unwanted charge from C_{PAR} can take a long time to settle out depending on the input filter bandwidth. C_{PAR} is discharged through a low impedance switch to ground every conversion cycle or when a first new configuration is programmed to mitigate this effect.

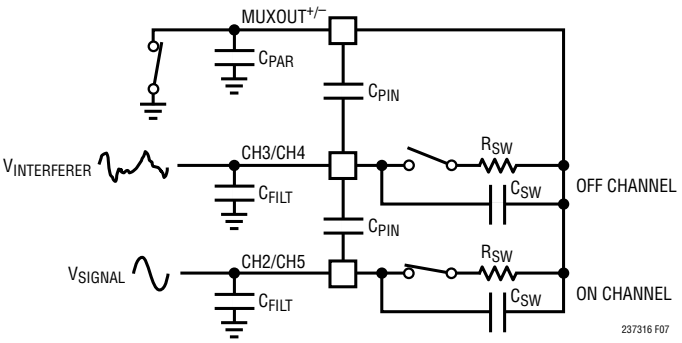


Figure 7. RC Equivalent Circuit for Two MUX Analog Input Channels

APPLICATIONS INFORMATION

Driving the MUX Analog Inputs

The LTC2373-16 can be programmed to accept fully differential or pseudo-differential input signals. In most applications, it is recommended that the LTC2373-16 be driven using the LT6237 ADC driver configured as two unity-gain buffers regardless of the input range, as shown in Figure 8a. The LT6237 combines fast settling and good DC linearity with a 1.1nV/$\sqrt{\text{Hz}}$ input-referred noise density, enabling it to achieve the full ADC data sheet SNR and THD specifications for all input ranges, as shown in the FFT plots in Figures 8b, 8c and 8d. The RC filter time constant is chosen to allow for sufficient transient settling of the LTC2373-16 MUX analog inputs during acquisition. With a maximum supply current of 7.8mA, the LT6237 is a perfect complement to the low power LTC2373-16.

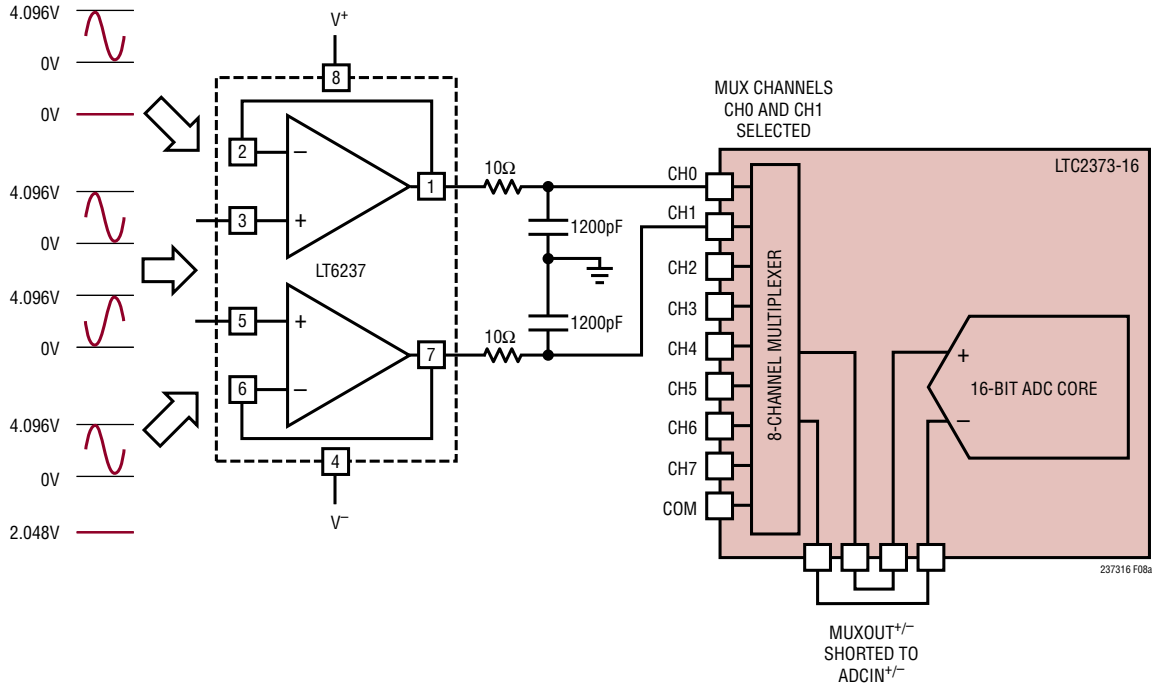


Figure 8a. LT6237 Buffering a Fully Differential or Pseudo-Differential Signal Source

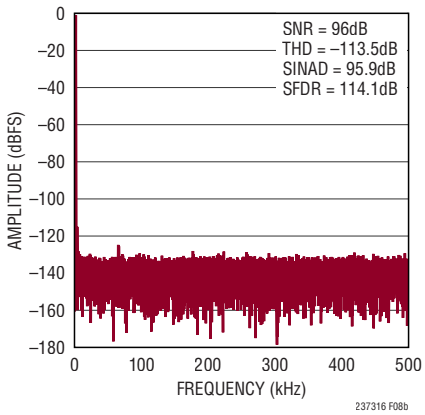


Figure 8b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Fully Differential Inputs

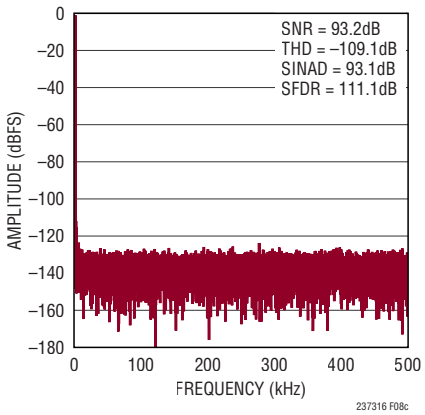


Figure 8c. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Unipolar Inputs

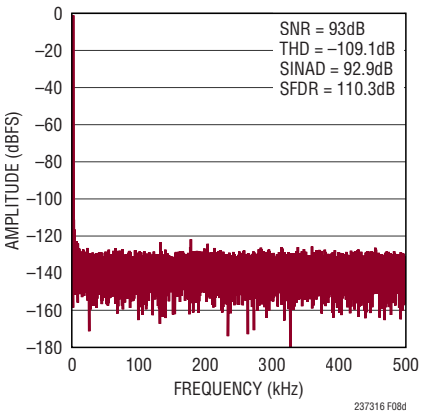


Figure 8d. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 8a; Driven with Bipolar Inputs

APPLICATIONS INFORMATION

Maximizing SNR with a Single-Ended to Differential Conversion

A single-ended input signal may be converted to a fully differential signal prior to driving the MUX analog inputs of the LTC2373-16 to take advantage of the higher SNR of the LTC2373-16 in the fully differential input range. The LT6350 ADC driver shown in Figure 9a can be used to convert a 0V to 4.096V input signal to a fully differential ±4.096V output signal. The RC time constant is larger in this case to limit the high frequency noise contribution of the LT6350. This topology provides a 3dB increase in SNR over single-ended operation and achieves the full data sheet SNR performance of the fully differential input range of 96dB as shown in the FFT plot in Figure 9b. The maximum supply current of 10.4mA makes the LT6350 a good companion to the low power LTC2373-16.

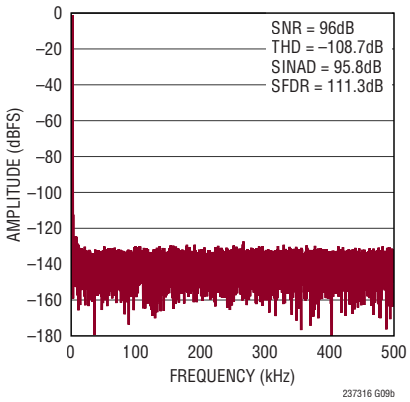


Figure 9b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 9a

Maximizing SNR for Eight Single-Ended Inputs Using a Shared Amplifier Between MUXOUT+/– and ADCIN+/–

While converting a single-ended signal to a fully differential signal offers the benefit of higher SNR, two input channels are required per single-ended input, leading to a reduced number of single-ended input signals that can be interfaced to the LTC2373-16. Performing the single-ended to differential conversion using the LT6237

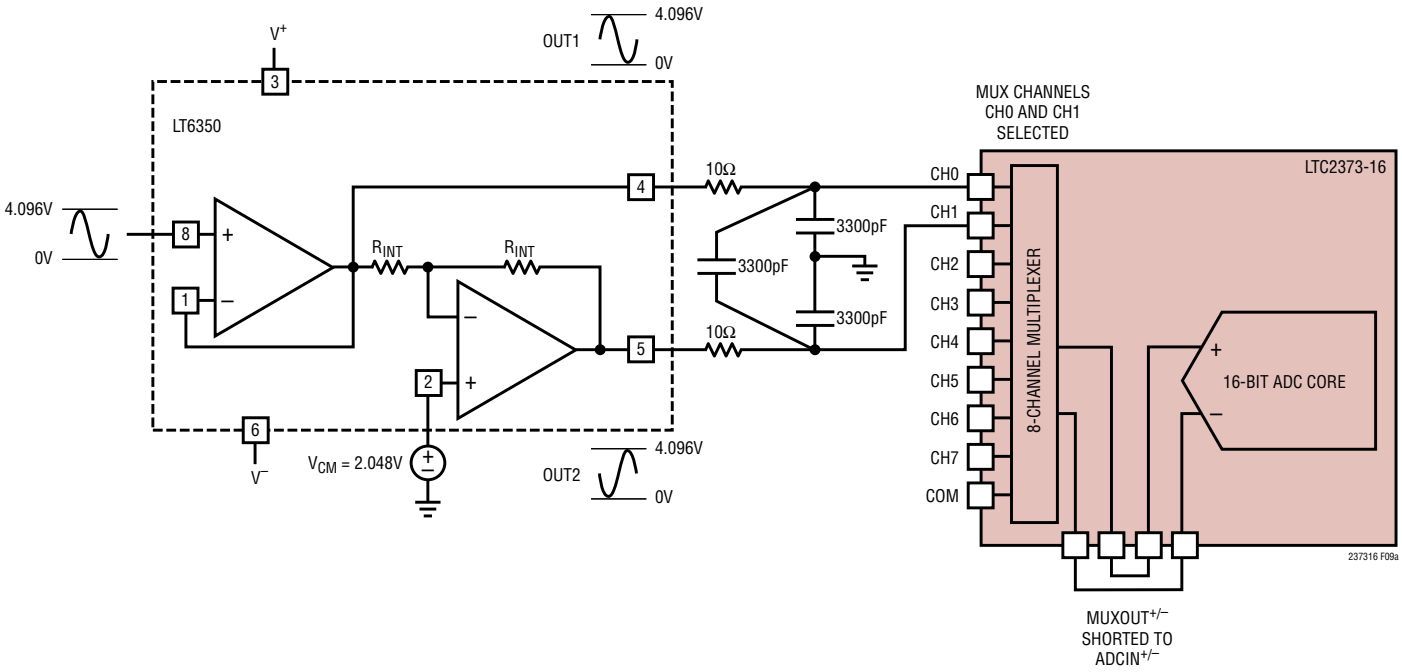


Figure 9a. LT6350 Converting a 0V to 4.096V Single-Ended Signal to a ±4.096V Fully Differential Signal

APPLICATIONS INFORMATION

between MUXOUT$^{+/-}$ and ADCIN$^{+/-}$ as shown in Figure 10a provides the SNR benefits of the fully differential range without sacrificing additional MUX inputs to do so. Using the MUX configurations where CH0 to CH7 is output to MUXOUT^{+} and COM to MUXOUT^{-} enables eight single-ended inputs to be converted with the fully differential input range. The COM MUX input channel is used in the feedback connection of the buffer amplifier connected in a follower configuration to improve the distortion performance of the circuit. THD degradation would otherwise occur due to the non-linear voltage drop across the MUX switch from the input current of the buffer and the non-linear on-resistance of the MUX switch. The 1k resistor between COM and MUXOUT^{-} maintains negative feedback around the buffer when the MUX turns OFF, so that the buffer output does not rail. Eight single-ended inputs achieve an SNR of 96dB with this circuit as shown in Figure 10b, which is a 3dB improvement in SNR over single-ended operation.

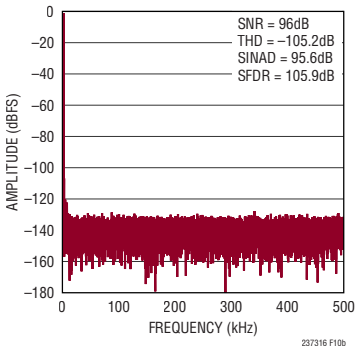


Figure 10b. 32k Point FFT f_{SMPL} = 1Msps, f_{IN} = 1kHz for Circuit Shown in Figure 10a

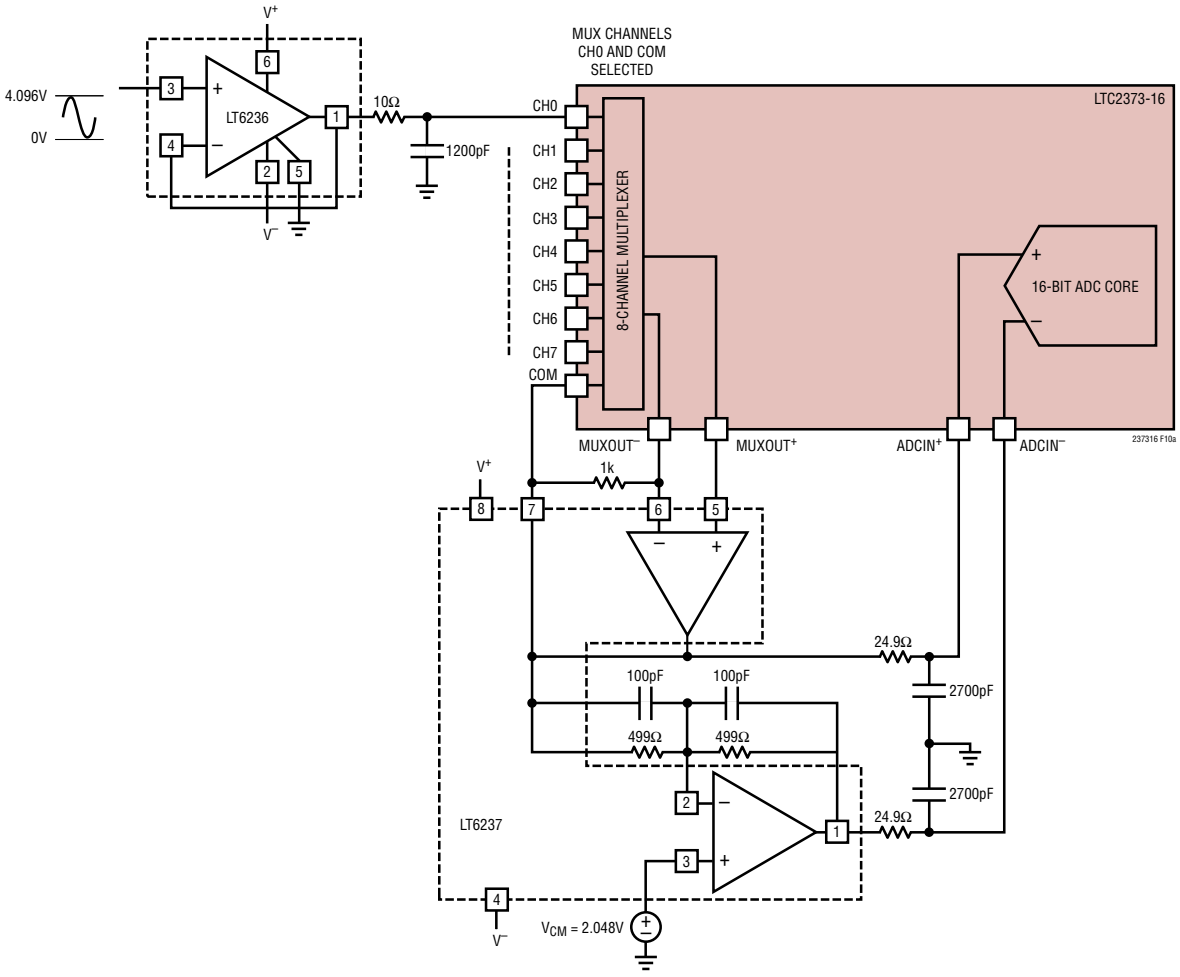


Figure 10a. LT6236 Buffering a Single-Ended 0V to 4.096V Input Signal and the LT6237 Configured to Perform a Single-Ended to Differential Conversion to the ±4.096V Fully Differential Input Range