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## FEATURES

- Pin Compatible 4-/8-Channel 24-Bit ADCs
- Single Conversion Digital Filter Settling Time Simplifies Multiplexing
- 4ppm INL, No Missing Codes
- 4ppm Full-Scale Error
- 0.5ppm Offset
- 0.3ppm Noise
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to  $V_{CC}$
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200 $\mu$ A) and Auto Shutdown

## APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain Gauge Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 6-Digit DVMs

## DESCRIPTION

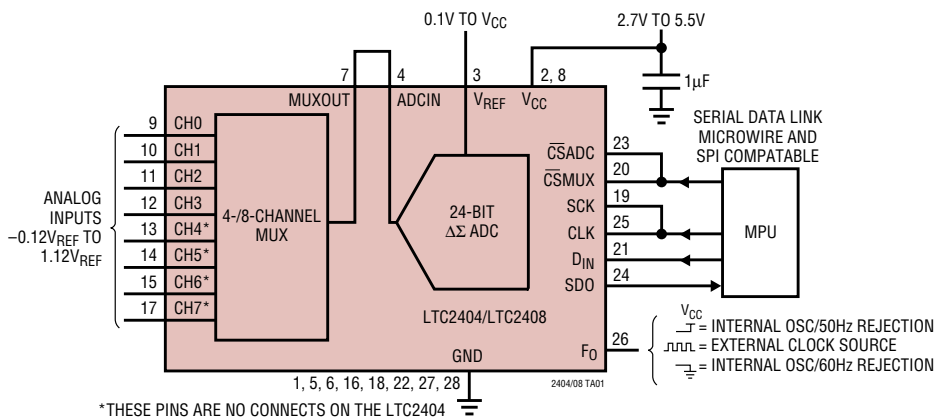
The LTC<sup>®</sup>2404/LTC2408 are 4-/8-channel 2.7V to 5.5V micropower 24-bit A/D converters with an integrated oscillator, 4ppm INL and 0.3ppm RMS noise. They use delta-sigma technology and provide single cycle digital filter settling time (no latency delay) for multiplexed applications. The first conversion after the channel is changed is always valid. Through a single pin the LTC2404/LTC2408 can be configured for better than 110dB rejection at 50Hz or 60Hz  $\pm$ 2%, or can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 120Hz. The internal oscillator requires no external frequency setting components.

The converters accept any external reference voltage from 0.1V to  $V_{CC}$ . With their extended input conversion range of  $-12.5\% V_{REF}$  to  $112.5\% V_{REF}$  the LTC2404/LTC2408 smoothly resolve the offset and overrange problems of preceding sensors or signal conditioning circuits.

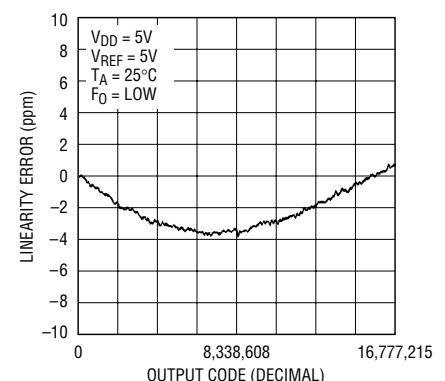
The LTC2404/LTC2408 communicate through a flexible 4-wire digital interface which is compatible with SPI and MICROWIRE<sup>™</sup> protocols.

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 No Latency  $\Delta\Sigma$  is a trademark of Linear Technology Corporation.  
 MICROWIRE is a trademark of National Semiconductor Corporation.

## TYPICAL APPLICATION



Total Unadjusted Error vs Output Code



# LTC2404/LTC2408

## ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage ( $V_{CC}$ ) to GND ..... -0.3V to 7V  
 Analog Input Voltage to GND ..... -0.3V to ( $V_{CC} + 0.3V$ )  
 Reference Input Voltage to GND .. -0.3V to ( $V_{CC} + 0.3V$ )  
 Digital Input Voltage to GND ..... -0.3V to ( $V_{CC} + 0.3V$ )  
 Digital Output Voltage to GND ..... -0.3V to ( $V_{CC} + 0.3V$ )

Operating Temperature Range  
 LTC2404C/LTC2408C ..... 0°C to 70°C  
 LTC2404I/LTC2408I ..... -40°C to 85°C  
 Storage Temperature Range ..... -65°C to 150°C  
 Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION

TOP VIEW	ORDER PART NUMBER	TOP VIEW	ORDER PART NUMBER
<p>G PACKAGE                  28-LEAD PLASTIC SSOP  <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	LTC2404CG LTC2404IG	<p>G PACKAGE                  28-LEAD PLASTIC SSOP  <math>T_{JMAX} = 125^{\circ}C, \theta_{JA} = 130^{\circ}C/W</math></p>	LTC2408CG LTC2408IG

Consult factory for Military grade parts.

## CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^{\circ}C$ . (Notes 3, 4)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	$0.1V \leq V_{REF} \leq V_{CC}$ , (Note 5)	●	24		Bits
Integral Nonlinearity	$V_{REF} = 2.5V$ (Note 6)	●	2	10	ppm of $V_{REF}$
	$V_{REF} = 5V$ (Note 6)	●	4	15	ppm of $V_{REF}$
Offset Error	$2.5V \leq V_{REF} \leq V_{CC}$	●	0.5	2	ppm of $V_{REF}$
Offset Error Drift	$2.5V \leq V_{REF} \leq V_{CC}$		0.01		ppm of $V_{REF}/^{\circ}C$
Full-Scale Error	$2.5V \leq V_{REF} \leq V_{CC}$	●	4	10	ppm of $V_{REF}$
Full-Scale Error Drift	$2.5V \leq V_{REF} \leq V_{CC}$		0.02		ppm of $V_{REF}/^{\circ}C$
Total Unadjusted Error	$V_{REF} = 2.5V$		5		ppm of $V_{REF}$
	$V_{REF} = 5V$		10		ppm of $V_{REF}$
Output Noise	$V_{IN} = 0V$ (Note 13)		1.5		$\mu V_{RMS}$
Normal Mode Rejection 60Hz $\pm 2\%$	(Note 7)	●	110	130	dB

## CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Normal Mode Rejection 50Hz $\pm 2\%$	(Note 8)	●	110	130		dB
Power Supply Rejection DC	$V_{REF} = 2.5\text{V}$ , $V_{IN} = 0\text{V}$			100		dB
Power Supply Rejection 60Hz $\pm 2\%$	$V_{REF} = 2.5\text{V}$ , $V_{IN} = 0\text{V}$ , (Note 7)			110		dB
Power Supply Rejection 50Hz $\pm 2\%$	$V_{REF} = 2.5\text{V}$ , $V_{IN} = 0\text{V}$ , (Note 8)			110		dB

## ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN}$	Input Voltage Range	(Note 14)	●	$-0.125 \cdot V_{REF}$		$1.125 \cdot V_{REF}$	V
$V_{REF}$	Reference Voltage Range		●	0.1		$V_{CC}$	V
$C_{S(IN)}$	Input Sampling Capacitance				10		pF
$C_{S(REF)}$	Reference Sampling Capacitance				15		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS} = V_{CC}$	●	-10	1	10	nA
$I_{REF(LEAK)}$	Reference Leakage Current	$V_{REF} = 2.5\text{V}$ , $\overline{CS} = V_{CC}$	●	-12	1	12	nA
$I_{IN(MUX)}$	On Channel Leakage Current	$V_S = 2.5\text{V}$ (Note 15)	●			$\pm 20$	nA
$R_{ON}$	MUX On-Resistance	$I_{OUT} = 1\text{mA}$ , $V_{CC} = 2.7\text{V}$ $I_{OUT} = 1\text{mA}$ , $V_{CC} = 5\text{V}$	● ●		250 120	300 250	$\Omega$ $\Omega$
	MUX $\Delta R_{ON}$ vs Temperature				0.5		%/ $^\circ\text{C}$
	$\Delta R_{ON}$ vs $V_S$ (Note 15)				20		%
$I_{S(OFF)}$	MUX Off Input Leakage	Channel Off, $V_S = 2.5\text{V}$	●			$\pm 20$	nA
$I_{D(OFF)}$	MUX Off Output Leakage	Channel Off, $V_D = 2.5\text{V}$	●			$\pm 20$	nA
$t_{OPEN}$	MUX Break-Before-Make Interval				290		ns
$t_{ON}$	Enable Turn-On Time	$V_S = 1.5\text{V}$ , $R_L = 3.4\text{k}$ , $C_L = 15\text{pF}$			490		ns
$t_{OFF}$	Enable Turn-Off Time	$V_S = 1.5\text{V}$ , $R_L = 3.4\text{k}$ , $C_L = 15\text{pF}$			190		ns
QIRR	MUX Off Isolation	$V_{IN} = 2V_{P-P}$ , $R_L = 1\text{k}$ , $f = 100\text{kHz}$			70		dB
QINJ	Charge Injection	$R_S = 0\Omega$ , $C_L = 1000\text{pF}$ , $V_S = 1\text{V}$			$\pm 1$		pC
$C_{S(OFF)}$	Input Off Capacitance (MUX)				10		pF
$C_{D(OFF)}$	Output Off Capacitance (MUX)				10		pF

## DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IH}$	High Level Input Voltage $\overline{CS}$ , $F_0$	$2.7V \leq V_{CC} \leq 5.5V$	●	2.5			V
		$2.7V \leq V_{CC} \leq 3.3V$		2.0			V
$V_{IL}$	Low Level Input Voltage $\overline{CS}$ , $F_0$	$4.5V \leq V_{CC} \leq 5.5V$	●			0.8	V
		$2.7V \leq V_{CC} \leq 5.5V$				0.6	V
$V_{IH}$	High Level Input Voltage SCK	$2.7V \leq V_{CC} \leq 5.5V$ (Note 9)	●	2.5			V
		$2.7V \leq V_{CC} \leq 3.3V$ (Note 9)		2.0			V
$V_{IL}$	Low Level Input Voltage SCK	$4.5V \leq V_{CC} \leq 5.5V$ (Note 9)	●			0.8	V
		$2.7V \leq V_{CC} \leq 5.5V$ (Note 9)				0.6	V
$I_{IN}$	Digital Input Current $\overline{CS}$ , $F_0$	$0V \leq V_{IN} \leq V_{CC}$	●	-10		10	$\mu\text{A}$
$I_{IN}$	Digital Input Current SCK	$0V \leq V_{IN} \leq V_{CC}$ (Note 9)	●	-10		10	$\mu\text{A}$
$C_{IN}$	Digital Input Capacitance $\overline{CS}$ , $F_0$				10		pF
$C_{IN}$	Digital Input Capacitance SCK	(Note 9)			10		pF
$V_{OH}$	High Level Output Voltage SDO	$I_O = -800\mu\text{A}$	●	$V_{CC} - 0.5V$			V
$V_{OL}$	Low Level Output Voltage SDO	$I_O = 1.6\text{mA}$	●			0.4V	V
$V_{OH}$	High Level Output Voltage SCK	$I_O = -800\mu\text{A}$ (Note 10)	●	$V_{CC} - 0.5V$			V
$V_{OL}$	Low Level Output Voltage SCK	$I_O = 1.6\text{mA}$ (Note 10)	●			0.4V	V
$I_{OZ}$	High-Z Output Leakage SDO		●	-10		10	$\mu\text{A}$
$V_{IN\ HMUX}$	MUX High Level Input Voltage	$V^+ = 3V$	●	2			V
$V_{IN\ LMUX}$	MUX Low Level Input Voltage	$V^+ = 2.4V$	●			0.8	V

## POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC}$	Supply Voltage		●	2.7		5.5	V
$I_{CC}$	Supply Current Conversion Mode	$\overline{CS} = 0V$ (Note 12)	●		200	300	$\mu\text{A}$
		$\overline{CS} = V_{CC}$ (Note 12)	●		20	30	$\mu\text{A}$
$I_{CC(MUX)}$	Multiplexer Supply Current	All Logic Inputs Tied Together $V_{IN} = 0V$ or $5V$	●		15	40	$\mu\text{A}$

## TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ . (Note 3)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
$f_{\text{EOSC}}$	External Oscillator Frequency Range	●	2.56		307.2	kHz	
$t_{\text{HEO}}$	External Oscillator High Period	●	0.5		390	$\mu\text{s}$	
$t_{\text{LEO}}$	External Oscillator Low Period	●	0.5		390	$\mu\text{s}$	
$t_{\text{CONV}}$	Conversion Time	$F_0 = 0\text{V}$	●	130.66	133.33	136	ms
		$F_0 = V_{\text{CC}}$	●	156.80	160	163.20	ms
		External Oscillator (Note 11)	●	20480/ $f_{\text{EOSC}}$ (in kHz)			ms
$f_{\text{ISCK}}$	Internal SCK Frequency	Internal Oscillator (Note 10)		19.2		kHz	
		External Oscillator (Notes 10, 11)		$f_{\text{EOSC}}/8$		kHz	
$D_{\text{ISCK}}$	Internal SCK Duty Cycle	(Note 10)	45		55	%	
$f_{\text{ESCK}}$	External SCK Frequency Range	(Note 9)			2000	kHz	
$t_{\text{LESCK}}$	External SCK Low Period	(Note 9)	250			ns	
$t_{\text{HESCK}}$	External SCK High Period	(Note 9)	250			ns	
$t_{\text{DOUT\_ISCK}}$	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 12)	●	1.64	1.67	1.70	ms
		External Oscillator (Notes 10, 11)	●	$256/f_{\text{EOSC}}$ (in kHz)			ms
$t_{\text{DOUT\_ESCK}}$	External SCK 32-Bit Data Output Time	(Note 9)		$32/f_{\text{ESCK}}$ (in kHz)		ms	
$t_1$	$\overline{\text{CS}} \downarrow$ to SDO Low Z	●	0		150	ns	
$t_2$	$\overline{\text{CS}} \uparrow$ to SDO High Z	●	0		150	ns	
$t_3$	$\overline{\text{CS}} \downarrow$ to SCK $\downarrow$	(Note 10)	●	0	150	ns	
$t_4$	$\overline{\text{CS}} \downarrow$ to SCK $\uparrow$	(Note 9)	●	50		ns	
$t_{\text{KQMAX}}$	SCK $\downarrow$ to SDO Valid	●			200	ns	
$t_{\text{KQMIN}}$	SDO Hold After SCK $\downarrow$	(Note 5)	●	15		ns	
$t_5$	SCK Set-Up Before $\overline{\text{CS}} \downarrow$	●	50			ns	
$t_6$	SCK Hold After $\overline{\text{CS}} \downarrow$	●			50	ns	

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:**  $V_{\text{CC}} = 2.7$  to  $5.5\text{V}$  unless otherwise specified, source input is  $0\Omega$ .

**Note 4:** Internal Conversion Clock source with the  $F_0$  pin tied to GND or to  $V_{\text{CC}}$  or to external conversion clock source with  $f_{\text{EOSC}} = 153600\text{Hz}$  unless otherwise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:**  $F_0 = 0\text{V}$  (internal oscillator) or  $f_{\text{EOSC}} = 153600\text{Hz} \pm 2\%$  (external oscillator).

**Note 8:**  $F_0 = V_{\text{CC}}$  (internal oscillator) or  $f_{\text{EOSC}} = 128000\text{Hz} \pm 2\%$  (external oscillator).

**Note 9:** The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is  $f_{\text{ESCK}}$  and is expressed in kHz.

**Note 10:** The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance  $C_{\text{LOAD}} = 20\text{pF}$ .

**Note 11:** The external oscillator is connected to the  $F_0$  pin. The external oscillator frequency,  $f_{\text{EOSC}}$ , is expressed in kHz.

**Note 12:** The converter uses the internal oscillator.  $F_0 = 0\text{V}$  or  $F_0 = V_{\text{CC}}$ .

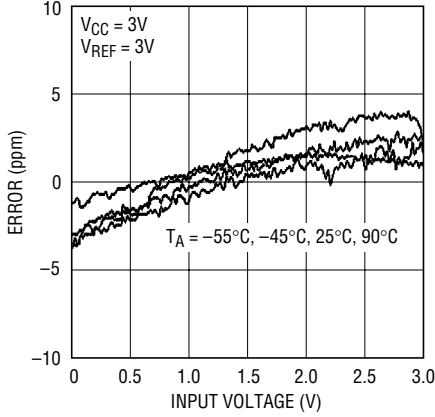
**Note 13:** The output noise includes the contribution of the internal calibration operations.

**Note 14:** For reference voltage values  $V_{\text{REF}} > 2.5\text{V}$  the extended input of  $-0.125 \cdot V_{\text{REF}}$  to  $1.125 \cdot V_{\text{REF}}$  is limited by the absolute maximum rating of the Analog Input Voltage pin (Pin 3). For  $2.5\text{V} < V_{\text{REF}} \leq 0.267\text{V} + 0.89 \cdot V_{\text{CC}}$  the input voltage range is  $-0.3\text{V}$  to  $1.125 \cdot V_{\text{REF}}$ . For  $0.267\text{V} + 0.89 \cdot V_{\text{CC}} < V_{\text{REF}} \leq V_{\text{CC}}$  the input voltage range is  $-0.3\text{V}$  to  $V_{\text{CC}} + 0.3\text{V}$ .

**Note 15:**  $V_S$  is the voltage applied to a channel input.  $V_D$  is the voltage applied to the MUX output.

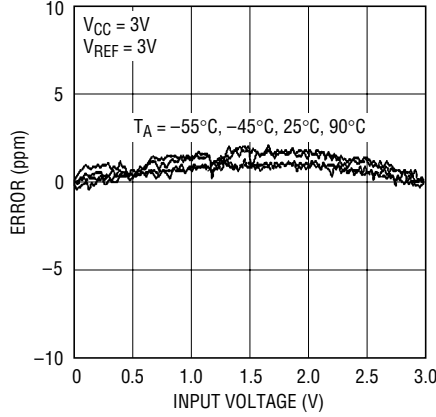
**TYPICAL PERFORMANCE CHARACTERISTICS**

**Total Unadjusted Error (3V Supply)**



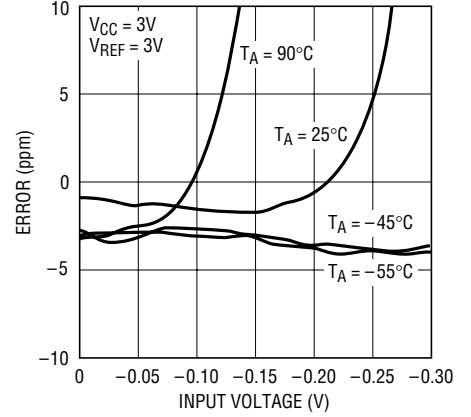
24048 G01

**INL (3V Supply)**



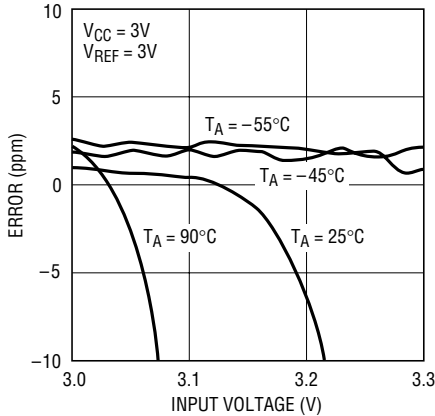
24048 G02

**Negative Extended Input Range Total Unadjusted Error (3V Supply)**



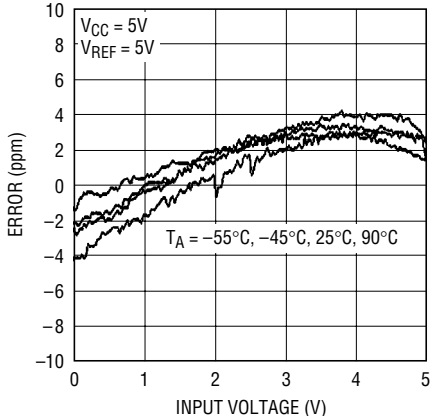
24048 G03

**Positive Extended Input Range Total Unadjusted Error (3V Supply)**



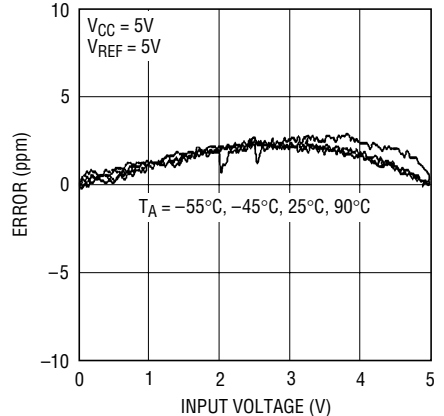
24048 G04

**Total Unadjusted Error (5V Supply)**



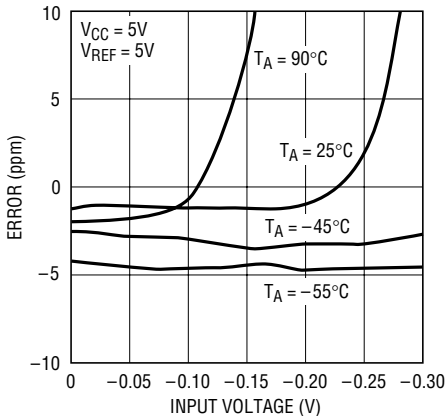
24048 G05

**INL (5V Supply)**



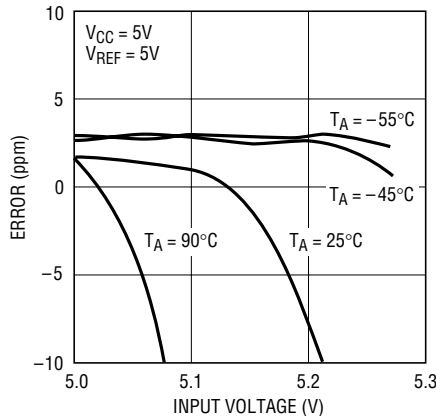
24048 G06

**Negative Extended Input Range Total Unadjusted Error (5V Supply)**



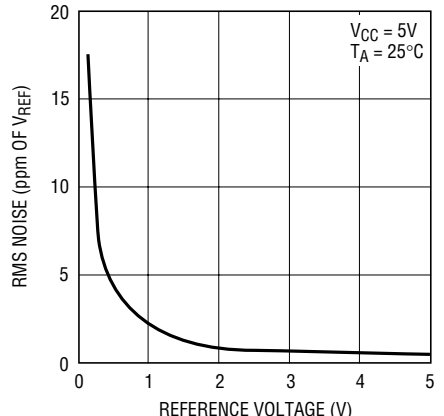
24048 G07

**Positive Extended Input Range Total Unadjusted Error (5V Supply)**



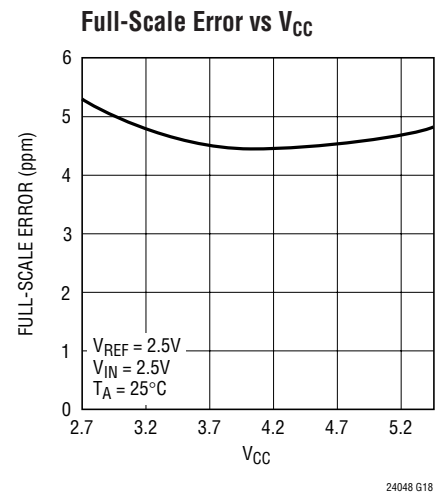
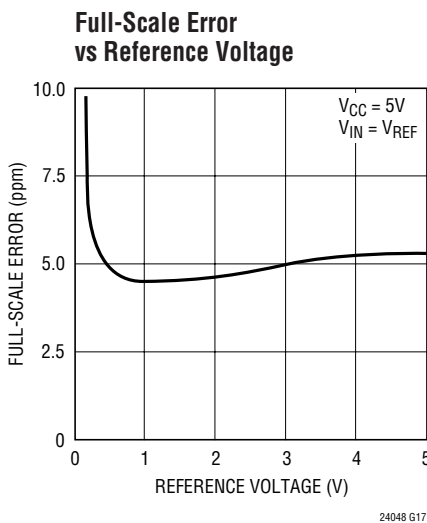
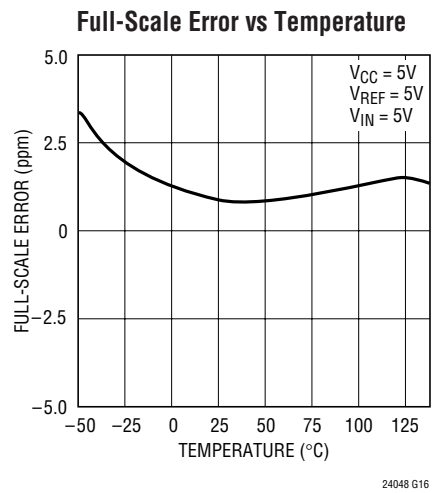
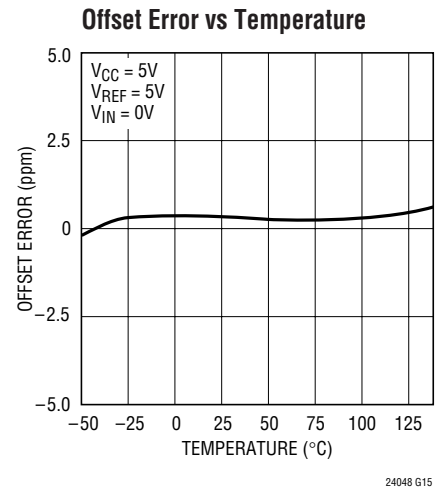
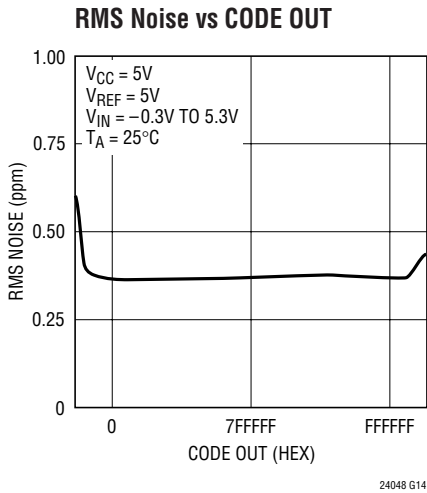
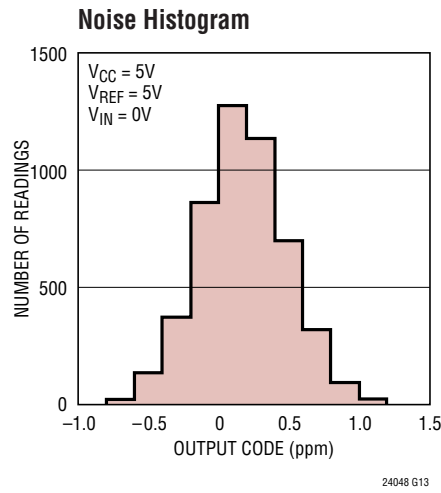
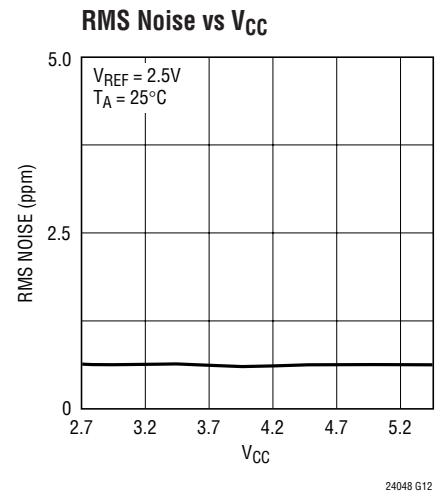
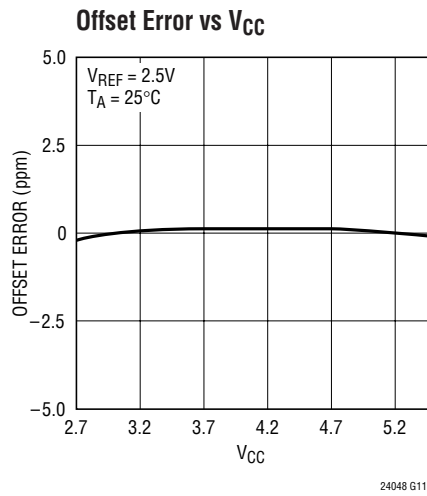
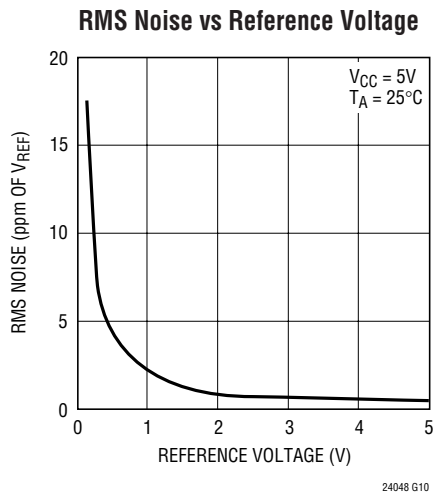
24048 G08

**Offset Error vs Reference Voltage**



24048 G10

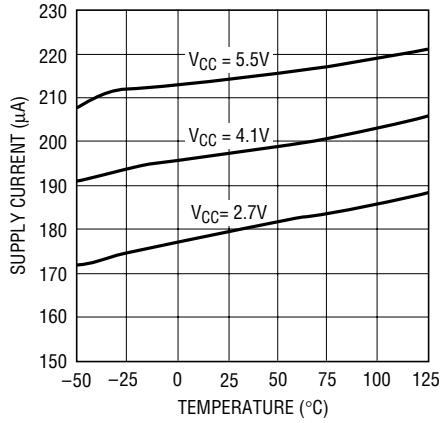
# TYPICAL PERFORMANCE CHARACTERISTICS



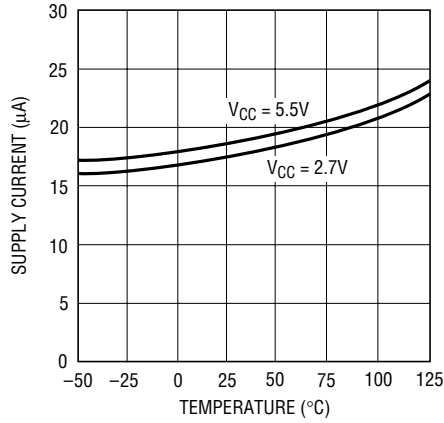


# TYPICAL PERFORMANCE CHARACTERISTICS

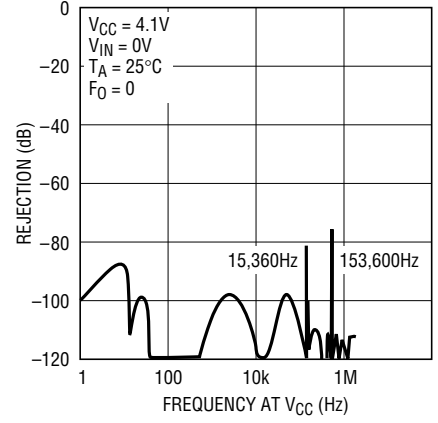
Conversion Current vs Temperature



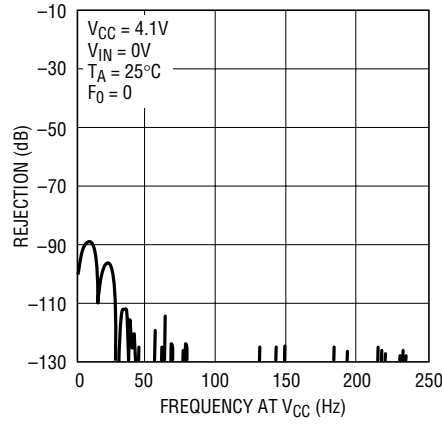
Sleep Current vs Temperature



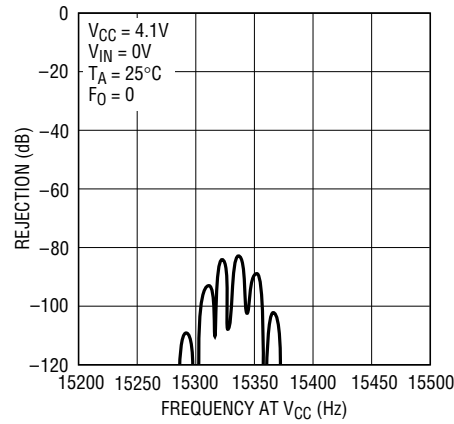
PSRR vs Frequency at V<sub>CC</sub>



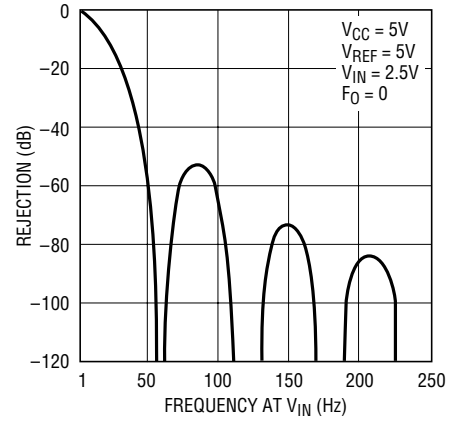
PSRR vs Frequency at V<sub>CC</sub>



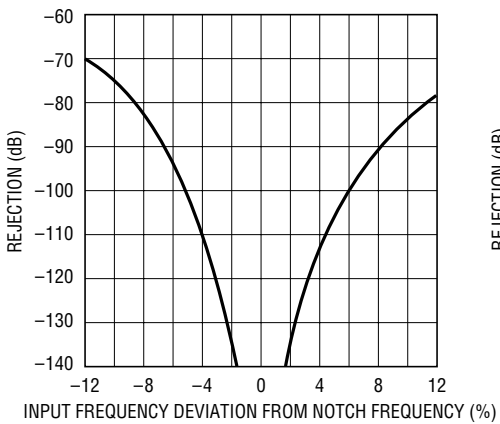
PSRR vs Frequency at V<sub>CC</sub>



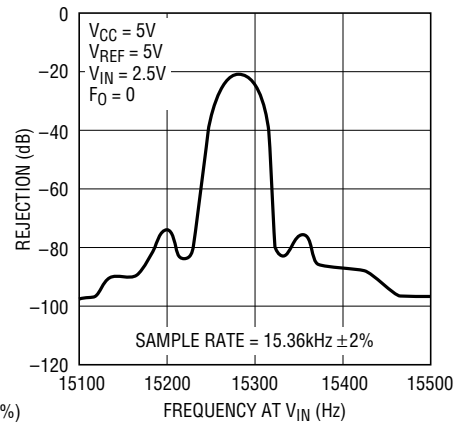
Rejection vs Frequency at V<sub>IN</sub>



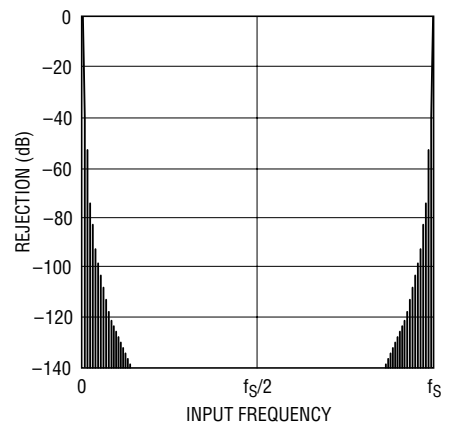
Rejection vs Frequency at V<sub>IN</sub>



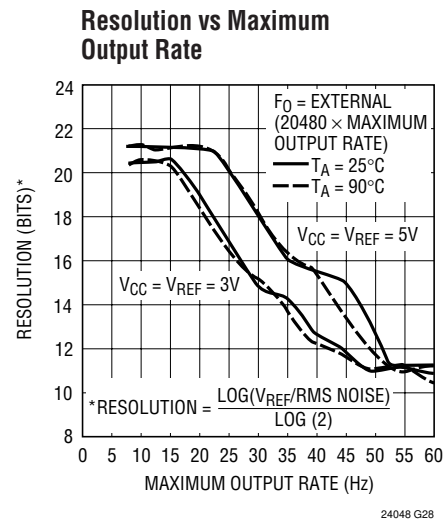
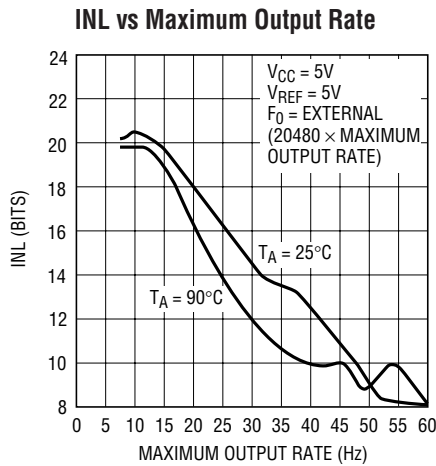
Rejection vs Frequency at V<sub>IN</sub>



Rejection vs Frequency at V<sub>IN</sub>



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**GND (Pins 1, 5, 6, 16, 18, 22, 27, 28):** Ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single point grounding system.

**$V_{CC}$  (Pins 2, 8):** Positive Supply Voltage.  $2.7V \leq V_{CC} \leq 5.5V$ . Bypass to GND with a  $10\mu\text{F}$  tantalum capacitor in parallel with  $0.1\mu\text{F}$  ceramic capacitor as close to the part as possible.

**$V_{REF}$  (Pin 3):** Reference Input. The reference voltage range is  $0.1V$  to  $V_{CC}$ .

**ADCIN (Pin 4):** Analog Input. The input voltage range is  $-0.125 \cdot V_{REF}$  to  $1.125 \cdot V_{REF}$ . For  $V_{REF} > 2.5V$  the input voltage range may be limited by the pin absolute maximum rating of  $-0.3V$  to  $V_{CC} + 0.3V$ .

**MUXOUT (Pin 7):** MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

**CH0 (Pin 9):** Analog Multiplexer Input.

**CH1 (Pin 10):** Analog Multiplexer Input.

**CH2 (Pin 11):** Analog Multiplexer Input.

**CH3 (Pin 12):** Analog Multiplexer Input.

**CH4 (Pin 13):** Analog Multiplexer Input. No connect on the LTC2404.

**CH5 (Pin 14):** Analog Multiplexer Input. No connect on the LTC2404.

**CH6 (Pin 15):** Analog Multiplexer Input. No connect on the LTC2404.

**CH7 (Pin 17):** Analog Multiplexer Input. No connect on the LTC2404.

**CLK (Pin 19):** Shift Clock for Data In. This clock synchronizes the serial data transfer into the MUX. For normal operation, drive this pin in parallel with SCK.

**CSMUX (Pin 20):** MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with  $\overline{\text{CSADC}}$ .

**$D_{IN}$  (Pin 21):** Digital Data Input. The multiplexer address is shifted into this input on the last four rising CLK edges before  $\overline{\text{CSMUX}}$  goes low.

**$\overline{\text{CSADC}}$  (Pin 23):** ADC Chip Select Input. A low on this pin enables the SDO digital output and following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as  $\overline{\text{CSADC}}$  is high. A high on this pin also disables the SDO digital output. A low-to-high transition on  $\overline{\text{CSADC}}$  during the Data Output

## PIN FUNCTIONS

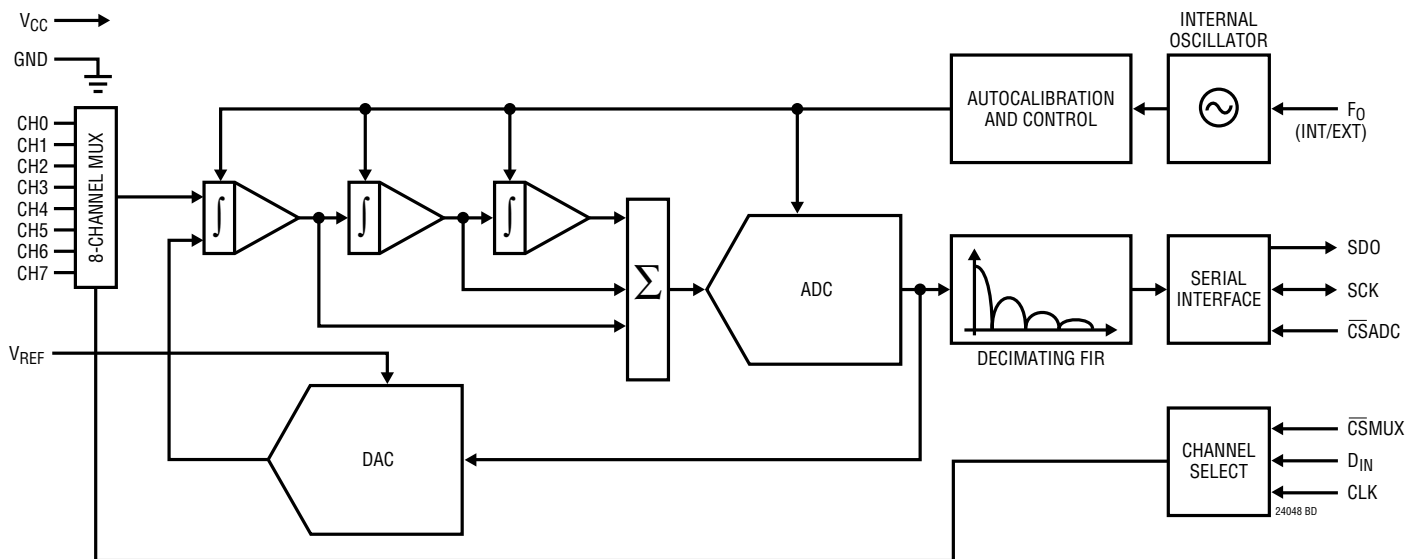
state aborts the data transfer and starts a new conversion. For normal operation, drive this pin in parallel with  $\overline{\text{CSMUX}}$ .

**SDO (Pin 24):** Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select  $\overline{\text{CSADC}}$  is high ( $\overline{\text{CSADC}} = V_{\text{CC}}$ ), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling  $\overline{\text{CSADC}}$  low.

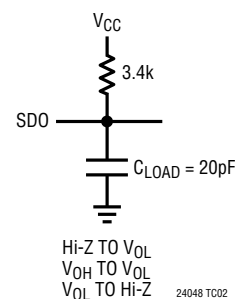
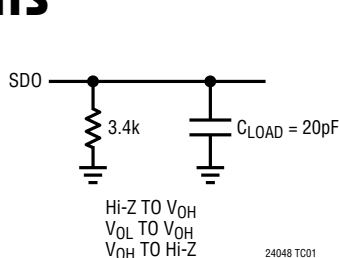
**SCK (Pin 25):** Shift Clock for Data Out. This clock synchronizes the serial data transfer of the ADC data output. Data is shifted out of SDO on the falling edge of SCK. For normal operation, drive this pin in parallel with CLK.

**F<sub>0</sub> (Pin 26):** Digital input which controls the ADC's notch frequencies and conversion time. When the F<sub>0</sub> pin is connected to V<sub>CC</sub> (F<sub>0</sub> = V<sub>CC</sub>), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F<sub>0</sub> pin is connected to GND (F<sub>0</sub> = 0V), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F<sub>0</sub> is driven by an external clock signal with a frequency f<sub>EOSC</sub>, the converter uses this signal as its clock and the digital filter first null is located at a frequency f<sub>EOSC</sub>/2560. The resulting output word rate is f<sub>EOSC</sub>/20480.

## FUNCTIONAL BLOCK DIAGRAM



## TEST CIRCUITS



## APPLICATIONS INFORMATION

### Converter Operation Cycle

The LTC2404/LTC2408 are low power, 4-/8-channel delta-sigma analog-to-digital converters with easy-to-use 4-wire interfaces. Their operation is simple and made up of four states. The converter operation begins with the conversion, followed by a low power sleep state and concluded with the data output (see Figure 1). Channel selection may be performed while the device is in the sleep state or at the conclusion of the data output state. The interface consists of serial data output (SDO), serial clock (CLK/SCK), chip select ( $\overline{\text{CSADC}}/\overline{\text{CSMUX}}$ ) and data input ( $\text{D}_{\text{IN}}$ ). By tying SCK to CLK and  $\overline{\text{CSADC}}$  to  $\overline{\text{CSMUX}}$ , the interface requires only four wires.

Initially, the LTC2404 or LTC2408 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as  $\overline{\text{CSADC}}$  is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Channel selection for the next conversion cycle is performed while the device is in the sleep state or at the end of the data output state. A specific channel is selected by applying a 4-bit serial word to the  $\text{D}_{\text{IN}}$  pin on the rising edge of CLK while  $\overline{\text{CSMUX}}$  is HIGH, see Figure 3 and Table 3. The channel is selected based on the last four bits clocked into the  $\text{D}_{\text{IN}}$  pin before  $\overline{\text{CSMUX}}$  goes low. If  $\text{D}_{\text{IN}}$  is all 0's, the previous channel remains selected.

In the example, Figure 3, the MUX channel is selected during the sleep state, just before the data output state begins. Once the channel selection is complete, the device remains in the sleep state as long as  $\overline{\text{CSADC}}$  remains HIGH.

Once  $\overline{\text{CSADC}}$  is pulled low, the device begins outputting the conversion result. There is no latency in the conversion result. Since there is no latency, the first conversion following a change in input channel is valid and corresponds to that channel. The data output corresponds to the conversion just performed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising

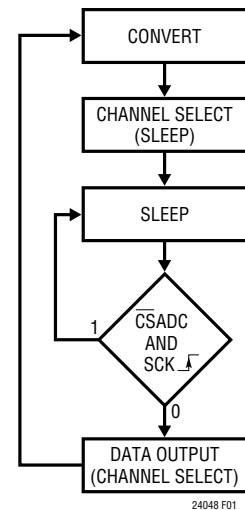


Figure 1. LTC2408 State Transition Diagram

edge of SCK, see Figure 3. The data output state is concluded once 32 bits are read out of the ADC or when  $\overline{\text{CSADC}}$  is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the  $\overline{\text{CSADC}}$  and SCK pins, the LTC2404/LTC2408 offer two modes of operation: internal or external SCK. These modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

### Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2404/LTC2408 incorporate an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2404/LTC2408 reject line frequencies (50 or 60Hz  $\pm 2\%$ ) a minimum of 110dB.

## APPLICATIONS INFORMATION

### Ease of Use

The LTC2404/LTC2408 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2404/LTC2408 perform offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

### Power-Up Sequence

The LTC2404/LTC2408 automatically enter an internal reset state when the power supply voltage  $V_{CC}$  drops below approximately 2.2V. When the  $V_{CC}$  voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers within the ADC and initiates a conversion. At power-up, the multiplexer channel is disabled and should be programmed once the device enters the sleep state. The results of the first conversion following a POR are not valid since a multiplexer channel was disabled.

### Reference Voltage Range

The LTC2404/LTC2408 can accept a reference voltage from 0V to  $V_{CC}$ . The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2404/LTC2408 voltage reference is 100mV to  $V_{CC}$ .

### Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 2.

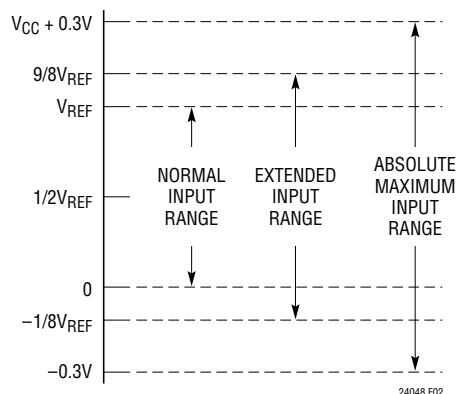


Figure 2. LTC2404/LTC2408 Input Range

The LTC2404/LTC2408 converts input signals within the extended input range of  $-0.125 \cdot V_{REF}$  to  $1.125 \cdot V_{REF}$ .

For large values of  $V_{REF}$  this range is limited to a voltage range of  $-0.3V$  to  $(V_{CC} + 0.3V)$ . Beyond this range the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to  $V_{IN}$  may extend below ground by  $-300mV$  and above  $V_{CC}$  by  $300mV$ . In order to limit any fault current, a resistor of up to 5k may be added in series with any channel input pin (CH0 to CH7) without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the channel input pin as low as possible; therefore, the resistor should be located as close as practical to the channel input pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition, a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if  $V_{REF} = 5V$ . This error has a very strong temperature dependency.

### Output Data Format

The LTC2404/LTC2408 serial output data stream is 32 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 4 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

## APPLICATIONS INFORMATION

Bit 31 (first output bit) is the end of conversion ( $\overline{\text{EOC}}$ ) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the  $\overline{\text{CSADC}}$  pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If  $V_{\text{IN}}$  is  $>0$ , this bit is HIGH. If  $V_{\text{IN}}$  is  $<0$ , this bit is LOW. The sign bit changes state during the zero code.

Bit 28 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range  $0 \leq V_{\text{IN}} \leq V_{\text{REF}}$ , this bit is LOW. If the input is outside the normal input range,  $V_{\text{IN}} > V_{\text{REF}}$  or  $V_{\text{IN}} < 0$ , this bit is HIGH.

The function of these bits is summarized in Table 1.

**Table 1. LTC2404/LTC2408 Status Bits**

Input Range	Bit 31 $\overline{\text{EOC}}$	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR
$V_{\text{IN}} > V_{\text{REF}}$	0	0	1	1
$0 < V_{\text{IN}} \leq V_{\text{REF}}$	0	0	1	0
$V_{\text{IN}} = 0^+/0^-$	0	0	1/0	0
$V_{\text{IN}} < 0$	0	0	0	1

Bit 27 (fifth output bit) is the most significant bit (MSB).

Bits 27-4 are the 24-bit conversion result MSB first.

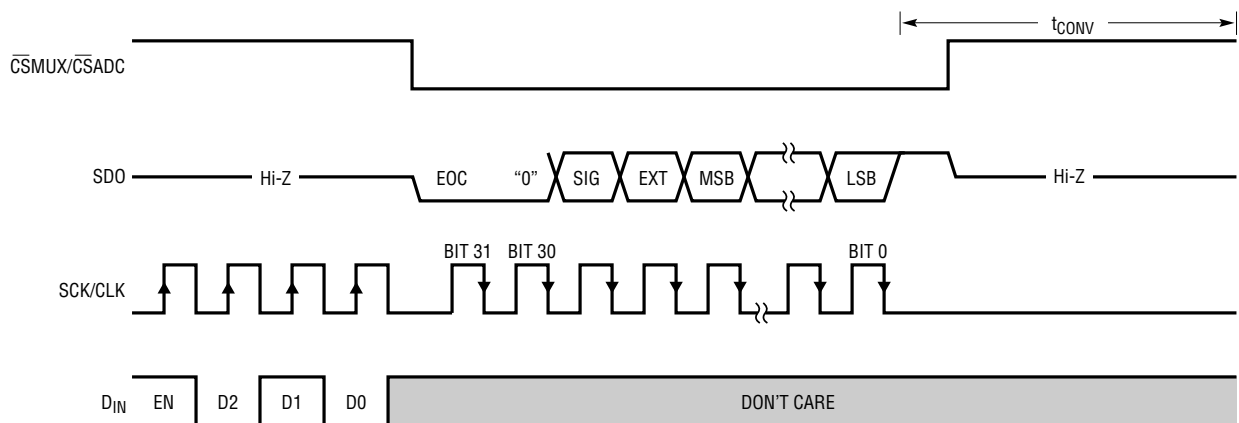
Bit 4 is the least significant bit (LSB).

Bits 3-0 are sub LSBs below the 24-bit level. Bits 3-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever  $\overline{\text{CSADC}}$  is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device,  $\overline{\text{CSADC}}$  must first be driven LOW.  $\overline{\text{EOC}}$  is seen at the SDO pin of the device once  $\overline{\text{CSADC}}$  is pulled LOW.  $\overline{\text{EOC}}$  changes in real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ( $\overline{\text{EOC}}$ ) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as  $\overline{\text{EOC}}$  (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the  $V_{\text{IN}}$  pin is maintained within the  $-0.3\text{V}$  to  $(V_{\text{CC}} + 0.3\text{V})$  absolute maximum operating range, a conversion result is generated for any input value from  $-0.125 \cdot V_{\text{REF}}$  to  $1.125 \cdot V_{\text{REF}}$ . For input voltages greater than  $1.125 \cdot V_{\text{REF}}$ , the conversion result is clamped to the value corresponding to  $1.125 \cdot V_{\text{REF}}$ . For input voltages below  $-0.125 \cdot V_{\text{REF}}$ , the conversion result is clamped to the value corresponding to  $-0.125 \cdot V_{\text{REF}}$ .



**Figure 3. Typical Data Input/Output Timing**

## APPLICATIONS INFORMATION

### Channel Selection

Typically,  $\overline{\text{CSADC}}$  and  $\overline{\text{CSMUX}}$  are tied together or  $\overline{\text{CSADC}}$  is inverted and drives  $\overline{\text{CSMUX}}$ . SCK and CLK are tied together and driven with a common clock signal. During channel selection,  $\overline{\text{CSMUX}}$  is HIGH. Data is shifted into the  $D_{\text{IN}}$  pin on the rising edge of CLK, see Figure 3. Table 3 shows the bit combinations for channel selection. In order to enable the multiplexer output,  $\overline{\text{CSMUX}}$  must be pulled LOW. The multiplexer should be programmed after the previous conversion is complete. In order to guarantee the conversion is complete, the multiplexer addressing should be delayed a minimum  $t_{\text{CONV}}$  (approximately 133ms for a 60Hz notch) after the data out is read.

While the multiplexer is being programmed, the ADC is in a low power sleep state. Once the MUX addressing is complete, the data from the preceding conversion can be read. A new conversion cycle is initiated following the data read cycle with the analog input tied to the newly selected channel.

Table 3. Logic Table for Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4*	1	1	0	0
CH5*	1	1	0	1
CH6*	1	1	1	0
CH7*	1	1	1	1

\*Not used for the LTC2404.

### Frequency Rejection Selection ( $F_0$ Pin Connection)

The LTC2404/LTC2408 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz  $\pm 2\%$  or 60Hz  $\pm 2\%$ . For 60Hz rejection,  $F_0$  (Pin 26) should be connected to GND (Pin 1) while for 50Hz rejection the  $F_0$  pin should be connected to  $V_{\text{CC}}$  (Pin 2).

Table 2. LTC2404/LTC2408 Output Data Format

Input Voltage	Bit 31 EOC	Bit 30 DMY	Bit 29 SIG	Bit 28 EXR	Bit 27 MSB	Bit 26	Bit 25	Bit 24	Bit 23	...	Bit 4 LSB	Bit 3-0 SUB LSBs*
$V_{\text{IN}} > 9/8 \cdot V_{\text{REF}}$	0	0	1	1	0	0	0	1	1	...	1	X
$9/8 \cdot V_{\text{REF}}$	0	0	1	1	0	0	0	1	1	...	1	X
$V_{\text{REF}} + 1\text{LSB}$	0	0	1	1	0	0	0	0	0	...	0	X
$V_{\text{REF}}$	0	0	1	0	1	1	1	1	1	...	1	X
$3/4V_{\text{REF}} + 1\text{LSB}$	0	0	1	0	1	1	0	0	0	...	0	X
$3/4V_{\text{REF}}$	0	0	1	0	1	0	1	1	1	...	1	X
$1/2V_{\text{REF}} + 1\text{LSB}$	0	0	1	0	1	0	0	0	0	...	0	X
$1/2V_{\text{REF}}$	0	0	1	0	0	1	1	1	1	...	1	X
$1/4V_{\text{REF}} + 1\text{LSB}$	0	0	1	0	0	1	0	0	0	...	0	X
$1/4V_{\text{REF}}$	0	0	1	0	0	0	1	1	1	...	1	X
$0^+/0^-$	0	0	1/0**	0	0	0	0	0	0	...	0	X
-1LSB	0	0	0	1	1	1	1	1	1	...	1	X
$-1/8 \cdot V_{\text{REF}}$	0	0	0	1	1	1	1	0	0	...	0	X
$V_{\text{IN}} < -1/8 \cdot V_{\text{REF}}$	0	0	0	1	1	1	1	0	0	...	0	X

\*The sub LSBs are valid conversion results beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

\*\*The sign bit changes state during the 0 code.

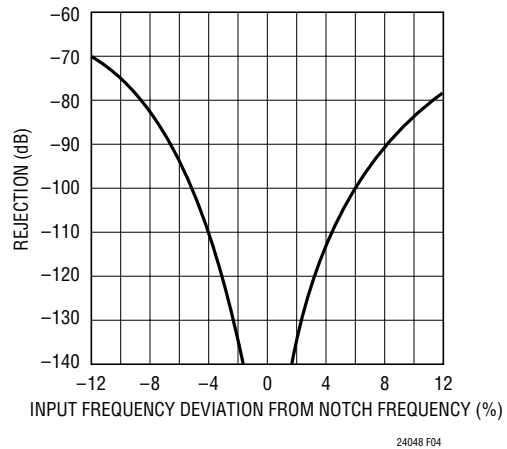
## APPLICATIONS INFORMATION

The selection of 50Hz or 60Hz rejection can also be made by driving  $F_0$  to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2404/LTC2408 can operate with an external conversion clock. The converter automatically detects the presence of an external clock signal at the  $F_0$  pin and turns off the internal oscillator. The frequency  $f_{EOSC}$  of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods  $t_{HEO}$  and  $t_{LEO}$  are observed.

While operating with an external conversion clock of a frequency  $f_{EOSC}$ , the LTC2404/LTC2408 provide better than 110dB normal mode rejection in a frequency range  $f_{EOSC}/2560 \pm 4\%$  and its harmonics. The normal mode rejection as a function of the input frequency deviation from  $f_{EOSC}/2560$  is shown in Figure 4.

Whenever an external clock is not present at the  $F_0$  pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The



**Figure 4. LTC2404/LTC2408 Normal Mode Rejection When Using an External Oscillator of Frequency  $f_{EOSC}$**

LTC2404/LTC2408 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 4 summarizes the duration of each state as a function of  $F_0$ .

**Table 4. LTC2404/LTC2408 State Duration**

State	Operating Mode		Duration
CONVERT	Internal Oscillator	$F_0 = \text{LOW}$ (60Hz Rejection)	133ms
		$F_0 = \text{HIGH}$ (50Hz Rejection)	160ms
	External Oscillator	$F_0 = \text{External Oscillator}$ with Frequency $f_{EOSC}$ kHz ( $f_{EOSC}/2560$ Rejection)	$20480/f_{EOSC}$ (In Seconds)
SLEEP			As Long As $\overline{CS} = \text{HIGH}$ Until $\overline{CS} = 0$ and $SCK \uparrow$
DATA OUTPUT	Internal Serial Clock	$F_0 = \text{LOW/HIGH}$ (Internal Oscillator)	As Long As $\overline{CS} = \text{LOW}$ But Not Longer Than 1.67ms (32 SCK cycles)
		$F_0 = \text{External Oscillator}$ with Frequency $f_{EOSC}$ kHz	As Long As $\overline{CS} = \text{LOW}$ But Not Longer Than $256/f_{EOSC}$ ms (32 SCK cycles)
	External Serial Clock with Frequency $f_{SCK}$ kHz		As Long As $\overline{CS} = \text{LOW}$ But Not Longer Than $32/f_{SCK}$ ms (32 SCK cycles)
MAXIMUM OUTPUT WORD RATE			$\text{OWR} = \frac{1}{t_{\text{CONVERT}} + t_{\text{DATAOUTPUT}}} \text{ in Hz}$



## APPLICATIONS INFORMATION

### Using an External Clock for Faster Conversion Times

The conversion time of the LTC2404/LTC2408 is determined by the conditions on the  $F_0$  pin. If  $F_0$  is connected to GND for 60Hz rejection, the conversion time is 133 $\mu$ s. If  $F_0$  is connected to  $V_{CC}$ , the conversion time is 160 $\mu$ s. For an externally supplied frequency of  $f_{EOSC}$ (kHz), the conversion time is:

$$t_{CONV} = 20480/f_{EOSC} \text{ (kHz)}$$

The resulting frequency rejection is:

$$\text{Notch Frequency} = 8/t_{CONV}$$

The maximum output word rate is:

$$OWR = \frac{1}{t_{CONVERT} + t_{DATAOUTPUT}} \text{ in Hz}$$

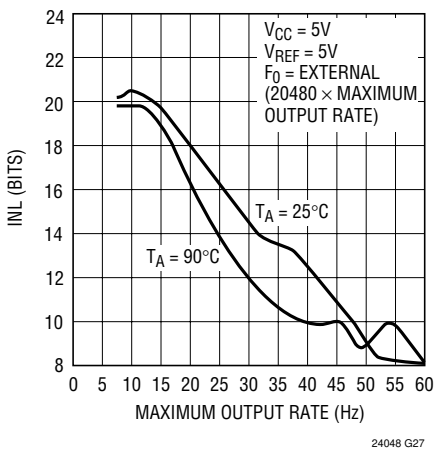


Figure 5. INL vs Maximum Output Rate

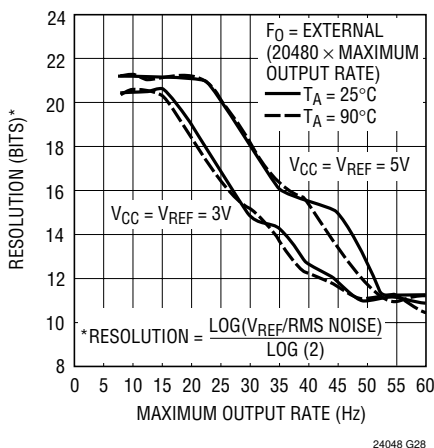


Figure 6. Resolution vs Maximum Output Rate

The DC specifications are guaranteed for  $f_{EOSC}$  up to a maximum of 307.2kHz, resulting in a maximum output word rate of approximately 15Hz. However, for faster rates at reduced performance, frequencies up to 1.22MHz can be used on the  $F_0$  pin. Figures 5 and 6 show the INL and Resolution vs Output Rate.

### SERIAL INTERFACE

The LTC2404/LTC2408 transmit the conversion results, program the channel selection, and receive the start of conversion command through a synchronous 4-wire interface (SCK = CLK,  $\overline{CSADC}$  =  $\overline{CSMUX}$ ). During the conversion and sleep states, this interface can be used to assess the converter status. While in the sleep state this interface may be used to program an input channel. During the data output state it is used to read the conversion result.

### ADC Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 25) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2404/LTC2408 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the  $\overline{CSADC}$  pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

### Multiplexer Serial Input Clock (CLK)

Generally, this pin is externally tied to SCK for 4-wire operation. On the rising edge of CLK (Pin 19) with  $\overline{CSMUX}$  held HIGH, data is serially shifted into the multiplexer. If  $\overline{CSMUX}$  is LOW the CLK input will be disabled and the channel selection unchanged.

### Serial Data Output (SDO)

The serial data output pin, SDO (Pin 24), drives the serial data during the data output state. In addition, the SDO pin

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is used as an end of conversion indicator during the conversion and sleep states.

When  $\overline{\text{CSADC}}$  (Pin 23) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If  $\overline{\text{CSADC}}$  is LOW during the convert or sleep state, SDO will output  $\overline{\text{EOC}}$ . If  $\overline{\text{CSADC}}$  is LOW during the conversion phase, the  $\overline{\text{EOC}}$  bit appears HIGH on the SDO pin. Once the conversion is complete,  $\overline{\text{EOC}}$  goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while  $\overline{\text{CSADC}} = 0$ .

### ADC Chip Select Input ( $\overline{\text{CSADC}}$ )

The active LOW chip select,  $\overline{\text{CSADC}}$  (Pin 23), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the  $\overline{\text{CSADC}}$  signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2404/LTC2408 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the  $\overline{\text{CSADC}}$  pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with  $\overline{\text{CSADC}} = 0$ ).

### Multiplexer Chip Select ( $\overline{\text{CSMUX}}$ )

For 4-wire operation, this pin is tied directly to  $\overline{\text{CSADC}}$  or the output of an inverter tied to  $\overline{\text{CSADC}}$ .  $\overline{\text{CSMUX}}$  (Pin 20) is driven HIGH during selection of a multiplexer channel. On the falling edge of  $\overline{\text{CSMUX}}$ , the selected channel is enabled and drives MUXOUT.

### Data Input ( $D_{\text{IN}}$ )

The data input to the multiplexer,  $D_{\text{IN}}$  (Pin 21), is used to program the multiplexer. The input channel is selected by serially shifting a 4-bit input word into the  $D_{\text{IN}}$  pin under the control of the multiplexer clock, CLK. Data is shifted into the multiplexer on the rising edge of CLK. Table 3

shows the logic table for channel selection. In order to select or change a previously programmed channel, an enable bit ( $D_{\text{IN}} = 1$ ) must proceed the 3-bit channel select serial data. The user may set  $D_{\text{IN}} = 0$  to continually convert on the previously selected channel.

### SERIAL INTERFACE TIMING MODES

The LTC2404/LTC2408's 4-wire interface is SPI and MICROWIRE compatible. This interface offers two modes of operation. These include an internal or external serial clock. The following sections describe both of these serial interface timing modes in detail. For both cases the converter can use the internal oscillator ( $F_0 = \text{LOW}$  or  $F_0 = \text{HIGH}$ ) or an external oscillator connected to the  $F_0$  pin. Refer to Table 5 for a summary.

#### External Serial Clock (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock (SCK) to shift out the conversion result, see Figure 7. This same external clock signal drives the CLK pin in order to program the multiplexer. A single CS signal drives both the multiplexer  $\overline{\text{CSMUX}}$  and converter  $\overline{\text{CSADC}}$  inputs. This common signal is used to monitor and control the state of the conversion as well as enable the channel selection.

The serial clock mode is selected on the falling edge of  $\overline{\text{CSADC}}$ . To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each  $\overline{\text{CSADC}}$  falling edge.

The serial data output pin (SDO) is Hi-Z as long as  $\overline{\text{CSADC}}$  is HIGH. At any time during the conversion cycle,  $\overline{\text{CSADC}}$  may be pulled LOW in order to monitor the state of the converter. While  $\overline{\text{CSADC}}$  is LOW,  $\overline{\text{EOC}}$  is output to the SDO pin.  $\overline{\text{EOC}} = 1$  while a conversion is in progress and  $\overline{\text{EOC}} = 0$  if the device is in the sleep state. Independent of  $\overline{\text{CSADC}}$ , the device automatically enters the low power sleep state once the conversion is complete.

Table 5. LTC2404/LTC2408 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK	External	$\overline{\text{CS}}$ and SCK	$\overline{\text{CS}}$ and SCK	Figures 7, 8, 9
Internal SCK	Internal	$\overline{\text{CS}} \downarrow$	$\overline{\text{CS}} \downarrow$	Figures 10, 11

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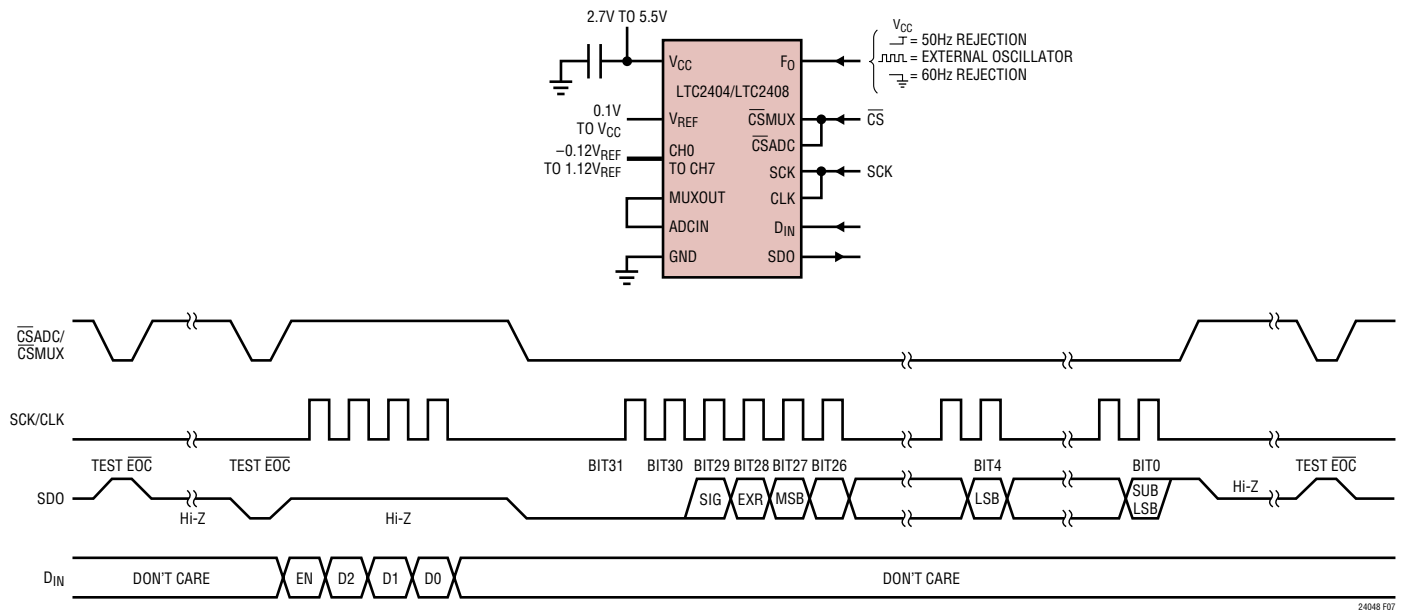


Figure 7. External Serial Clock Timing Diagram

While the device is in the sleep state, prior to entering the data output state, the user may program the multiplexer. As shown in Figure 7, the multiplexer channel is selected by serial shifting a 4-bit word into the  $D_{IN}$  pin on the rising edge of CLK (CLK is tied to SCK). The first bit is an enable bit that must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the falling edge of  $\overline{CSMUX}$ , the new channel is selected and will be valid for the first conversion performed following the data output state. Clock signals applied to the CLK pin while  $\overline{CSMUX}$  is LOW (during the data output state) will have no effect on the channel selection. Furthermore, if  $D_{IN}$  is held LOW or CLK is held LOW during the sleep state, the channel selection is unchanged.

When the device is in the sleep state ( $\overline{EOC} = 0$ ), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while  $\overline{CSADC}$  is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. EOC can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ( $\overline{EOC} = 1$ ) indicating a conversion is in progress.

At the conclusion of the data cycle,  $\overline{CSADC}$  may remain LOW and  $\overline{EOC}$  monitored as an end-of-conversion interrupt. Alternatively,  $\overline{CSADC}$  may be driven HIGH setting SDO to Hi-Z. As described above,  $\overline{CSADC}$  may be pulled LOW at any time in order to monitor the conversion status. For each of these operations,  $\overline{CSMUX}$  may be tied to  $\overline{CSADC}$  without affecting the selected channel.

At the conclusion of the data output cycle, the converter enters a user transparent calibration cycle prior to actually performing a conversion on the selected input channel. This enables a 66ms (for 60Hz notch frequency) look ahead time for the multiplexer input. Following the data output cycle, the multiplexer input channel may be selected any time in this 66ms window by pulling  $\overline{CSADC}$  HIGH and serial shifting data into the  $D_{IN}$  pin, see Figure 8.

While the device is performing the internal calibration, it is sensitive to ground current disturbances. Error currents flowing in the ground pin may lead to offset errors. If the SCK pin is toggling during the calibration, these ground disturbances will occur. The solution is to either drive the multiplexer clock input (CLK) separately from the ADC clock input (SCK), or program the multiplexer in the first 1ms following the data output cycle. The remaining 65ms may be used to allow the input signal to settle.

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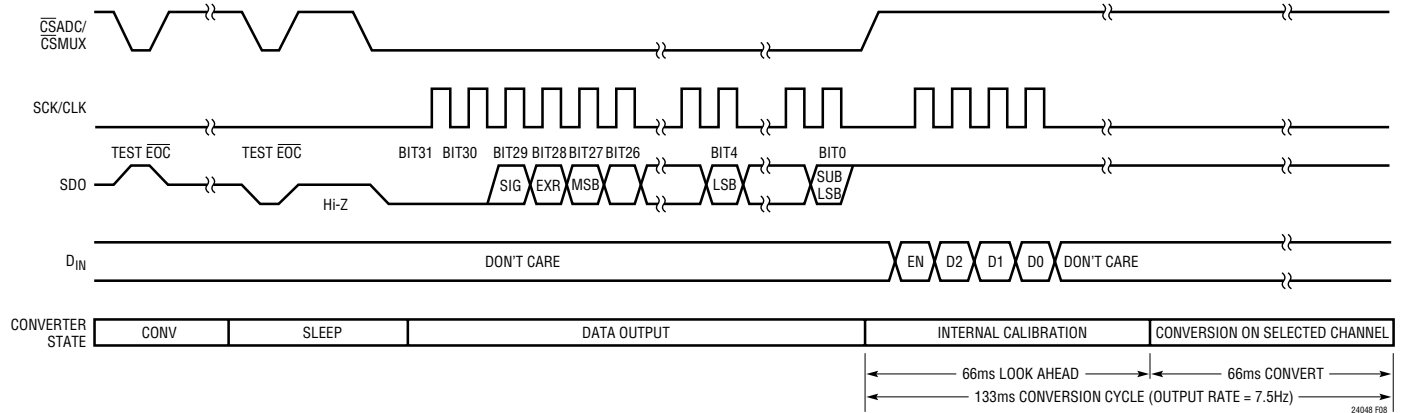


Figure 8. Use of Look Ahead to Program Multiplexer After Data Output

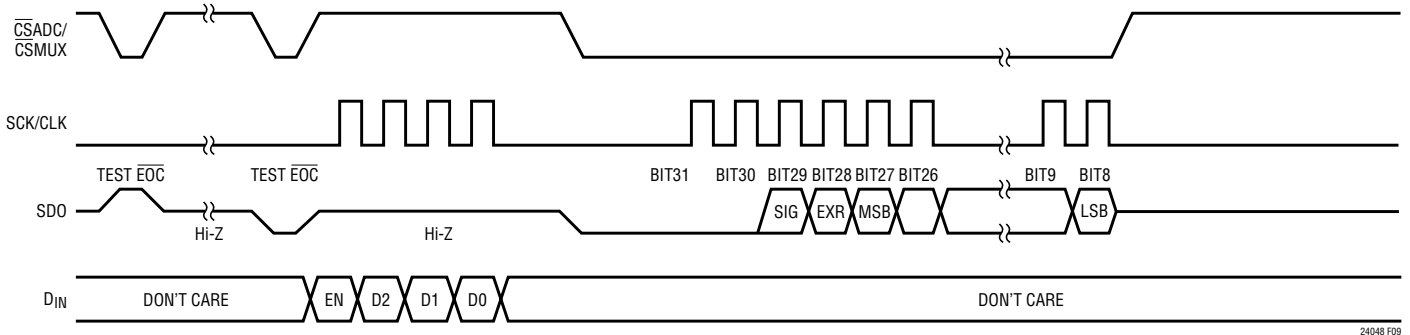
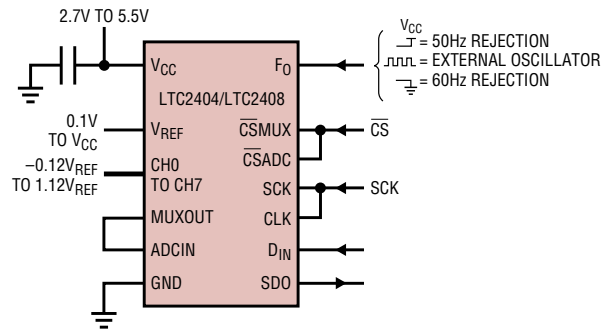


Figure 9. External Serial Clock with Reduced Data Output Length Timing Diagram

Typically,  $\overline{\text{CSADC}}$  remains LOW during the data output state. However, the data output state may be aborted by pulling  $\overline{\text{CSADC}}$  HIGH anytime between the first rising edge and the 32nd falling edge of SCK, see Figure 9. On the rising edge of  $\overline{\text{CSADC}}$ , the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

### Internal Serial Clock

This timing mode uses an internal serial clock to shift out the conversion result and program the multiplexer, see Figure 10. A  $\overline{\text{CS}}$  signal directly drives the  $\overline{\text{CSADC}}$  input, while the inverse of  $\overline{\text{CS}}$  drives the  $\overline{\text{CSMUX}}$  input. The  $\overline{\text{CS}}$  signal is used to monitor and control the state of the conversion cycles as well as enable the channel selection. The multiplexer is programmed during the data output

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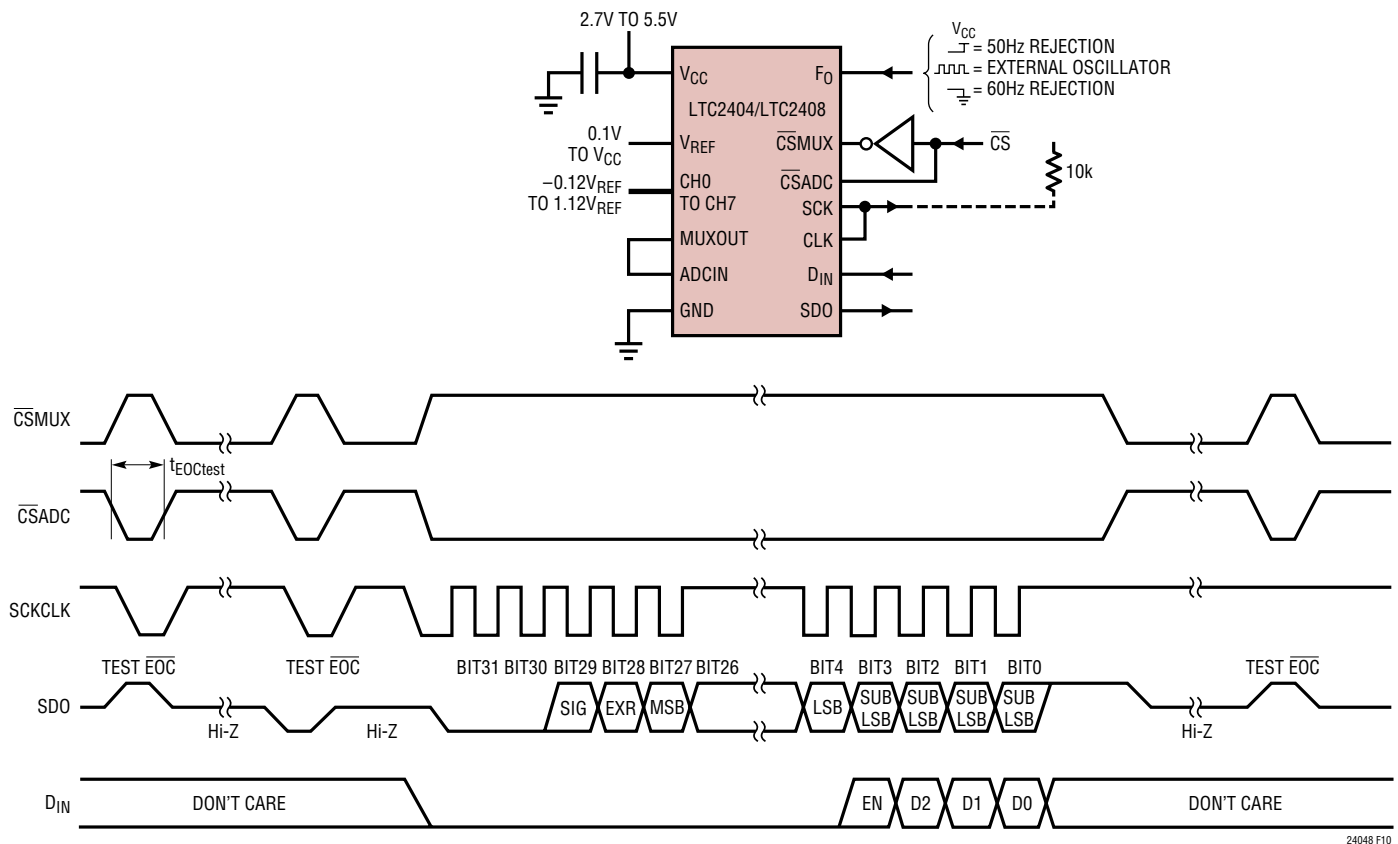


Figure 10. Internal Serial Clock Timing Diagram

state. The internal serial clock (SCK) generated by the ADC is applied to the multiplexer clock input (CLK).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of  $\overline{\text{CSADC}}$ . The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of  $\overline{\text{CSADC}}$ . An internal weak pull-up resistor is active on the SCK pin during the falling edge of  $\overline{\text{CSADC}}$ ; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as  $\overline{\text{CSADC}}$  is HIGH. At any time during the conversion cycle,  $\overline{\text{CSADC}}$  may be pulled LOW in order to monitor the state of the converter. Once  $\overline{\text{CSADC}}$  is pulled LOW, SCK goes LOW and  $\overline{\text{EOC}}$  is output to the SDO pin.  $\overline{\text{EOC}} = 1$  while a conversion is in progress and  $\overline{\text{EOC}} = 0$  if the device is in the sleep state.

When testing  $\overline{\text{EOC}}$ , if the conversion is complete ( $\overline{\text{EOC}} = 0$ ), the device will exit the sleep state and enter the data output

state if  $\overline{\text{CSADC}}$  remains LOW. In order to prevent the device from exiting the low power sleep state,  $\overline{\text{CSADC}}$  must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time  $t_{\text{EOCtest}}$  after the falling edge of  $\overline{\text{CSADC}}$  (if  $\overline{\text{EOC}} = 0$ ) or  $t_{\text{EOCtest}}$  after  $\overline{\text{EOC}}$  goes LOW (if  $\overline{\text{CSADC}}$  is LOW during the falling edge of  $\overline{\text{EOC}}$ ). The value of  $t_{\text{EOCtest}}$  is  $23\mu\text{s}$  if the device is using its internal oscillator ( $F_0 = \text{logic LOW or HIGH}$ ). If  $F_0$  is driven by an external oscillator of frequency  $f_{\text{EOSC}}$ , then  $t_{\text{EOCtest}}$  is  $3.6/f_{\text{EOSC}}$ . If  $\overline{\text{CSADC}}$  is pulled HIGH before time  $t_{\text{EOCtest}}$ , the device remains in the sleep state. The conversion result is held in the internal static shift register.

If  $\overline{\text{CSADC}}$  remains LOW longer than  $t_{\text{EOCtest}}$ , the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output

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to the SCK pin. This signal may be used to shift the conversion result into external circuitry.  $\overline{EOC}$  can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ( $\overline{EOC} = 1$ ), SCK stays HIGH, and a new conversion starts.

While operating in the internal serial clock mode, the SCK output of the ADC may be used as the multiplexer clock (CLK).  $D_{IN}$  is latched into the multiplexer on the rising edge of CLK. As shown in Figure 10, the multiplexer channel is selected by serial shifting a 4-bit word into the  $D_{IN}$  pin on the rising edge of CLK. The first bit is an enable bit which must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the rising edge of  $\overline{CSADC}$  (falling edge of  $\overline{CSMUX}$ ), the new channel is selected and will be valid for the next conversion. If  $D_{IN}$  is held LOW during the data output state, the previous channel selection remains valid.

Typically,  $\overline{CSADC}$  remains LOW during the data output state. However, the data output state may be aborted by pulling  $\overline{CSADC}$  HIGH anytime between the first and 32nd rising edge of SCK, see Figure 11. On the rising edge of  $\overline{CSADC}$ , the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If  $\overline{CSADC}$  is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of  $\overline{CSADC}$ . This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling  $\overline{CSADC}$  HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2404/LTC2408's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing

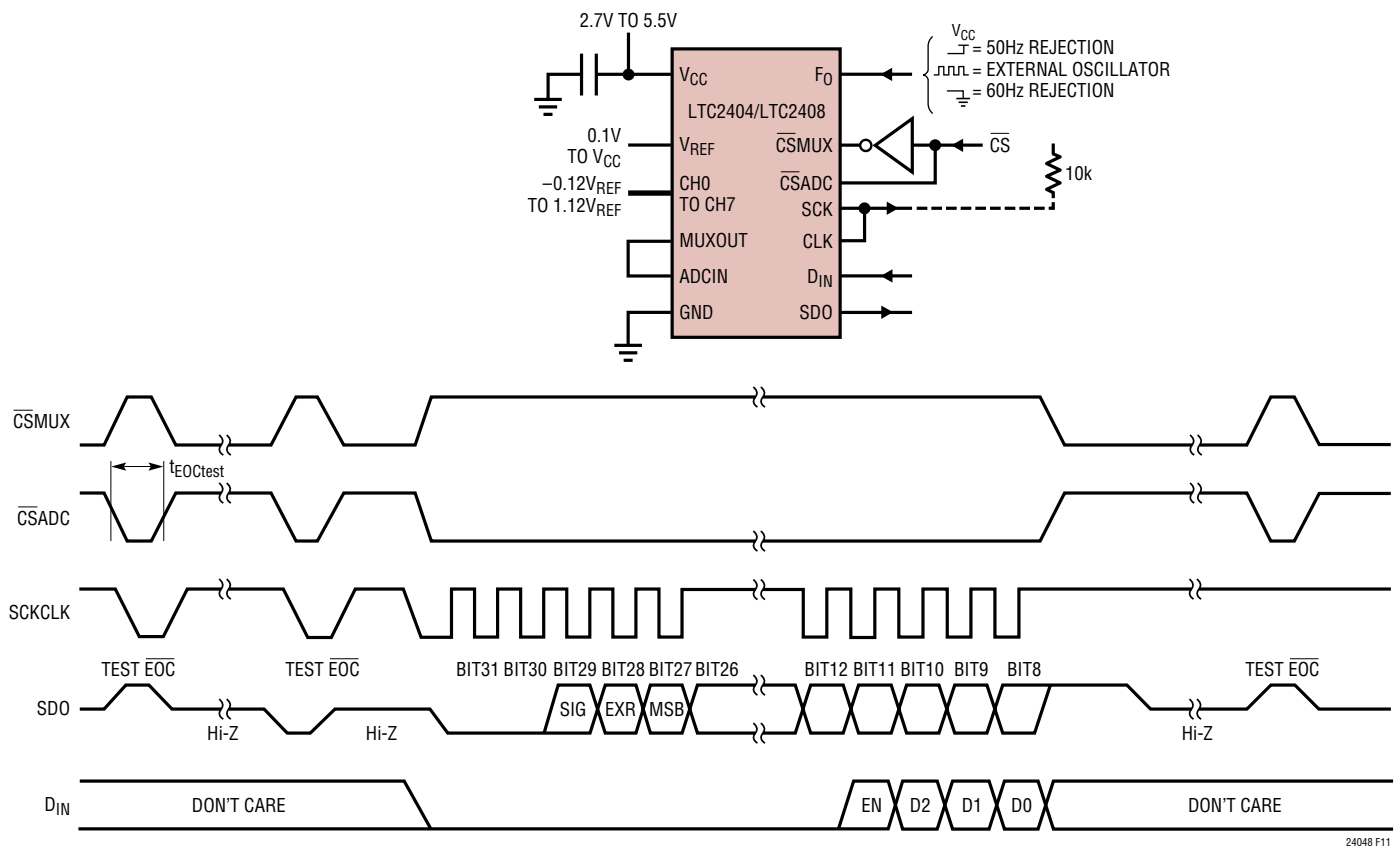


Figure 11. Internal Serial Clock with Reduced Data Output Length Timing Diagram

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mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2404/LTC2408's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of  $\overline{\text{CSADC}}$ , the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next  $\overline{\text{CSADC}}$  falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when  $\overline{\text{CSADC}}$  is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ( $\text{EOC} = 0$ ), SCK will go LOW. Once  $\overline{\text{CSADC}}$  goes HIGH (within the time period defined above as  $t_{\text{EOCtest}}$ ), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before  $\overline{\text{CSADC}}$  goes LOW again. This is not a concern under normal conditions where  $\overline{\text{CSADC}}$  remains LOW after detecting  $\text{EOC} = 0$ . This situation is easily avoided by adding an external 10k pull-up resistor to the SCK pin.

### DIGITAL SIGNAL LEVELS

The LTC2404/LTC2408's digital interface is easy to use. Its digital inputs ( $F_0$ ,  $\overline{\text{CSADC}}$ ,  $\overline{\text{CSMUX}}$ , CLK,  $D_{\text{IN}}$  and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and can tolerate edge rates as slow as 100 $\mu\text{s}$ . However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the accuracy of the LTC2404/LTC2408, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. Pin 6 (GND) should be connected to a low resistance ground plane through a minimum length trace. The use of multiple via holes is recommended to further reduce the connection resistance. The LTC2404/LTC2408's power supply current flowing through the 0.01 $\Omega$  resistance of the common ground pin will develop

a 2.5 $\mu\text{V}$  offset signal. For a reference voltage  $V_{\text{REF}} = 2.5\text{V}$ , this represents a 1ppm offset error.

In an alternative configuration, Pin 6 (GND) of the converter can be the single-point-ground in a single point grounding system. The input signal ground, the reference signal ground, the digital drivers ground (usually the digital ground) and the power supply ground (the analog ground) should be connected in a star configuration with the common point located as close to Pin 6 as possible.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

While a digital input signal is in the 0.5V to ( $V_{\text{CC}} - 0.5\text{V}$ ) range, the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals ( $F_0$ ,  $\overline{\text{CSADC}}$ ,  $\overline{\text{CSMUX}}$ ,  $D_{\text{IN}}$ , CLK and SCK in External SCK mode of operation) is within this range, the LTC2404/LTC2408 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [ $V_{\text{IL}} < 0.4\text{V}$  and  $V_{\text{OH}} > (V_{\text{CC}} - 0.4\text{V})$ ].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2404/LTC2408. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2404/LTC2408 input pins will eliminate this problem but will increase the driver

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power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2404/LTC2408 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

### Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (ADCIN), ground and the reference (V<sub>REF</sub>). The result is small current spikes seen at both ADCIN and V<sub>REF</sub>. A simplified input equivalent circuit is shown in Figure 12.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the internal switched capacitor network of the LTC2404/LTC2408 is clocked at 153,600Hz corresponding to a 6.5μs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V<sub>IN</sub> and V<sub>REF</sub> should be less than 6.5μs/14 = 460ns in order to achieve 1ppm accuracy.

### Input Current (V<sub>IN</sub>)

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. If the settling is incomplete, it does not degrade the linearity

performance of the device. It simply results in an offset/full-scale shift, see Figure 13. To simplify the analysis of input dynamic current, two separate cases are assumed: large capacitance at V<sub>IN</sub> (C<sub>IN</sub> > 0.01μF) and small capacitance at V<sub>IN</sub> (C<sub>IN</sub> < 0.01μF).

If the total capacitance at V<sub>IN</sub> (see Figure 14) is small (< 0.01μF), relatively large external source resistances (up to 20k for 20pF parasitic capacitance) can be tolerated without any offset/full-scale error. Figures 15 and 16 show a family of offset and full-scale error curves for various

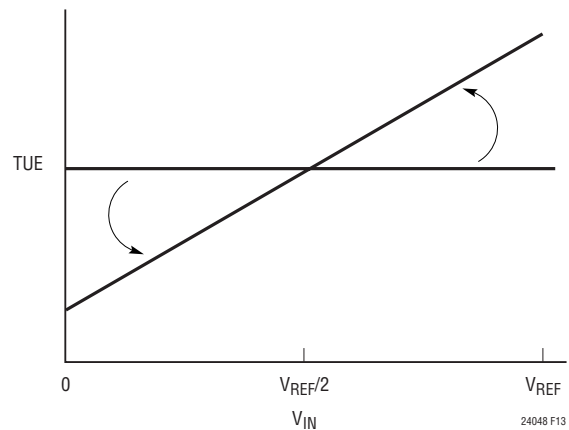


Figure 13. Offset/Full-Scale Shift

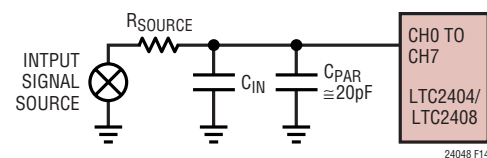


Figure 14. An RC Network at CH0 to CH7

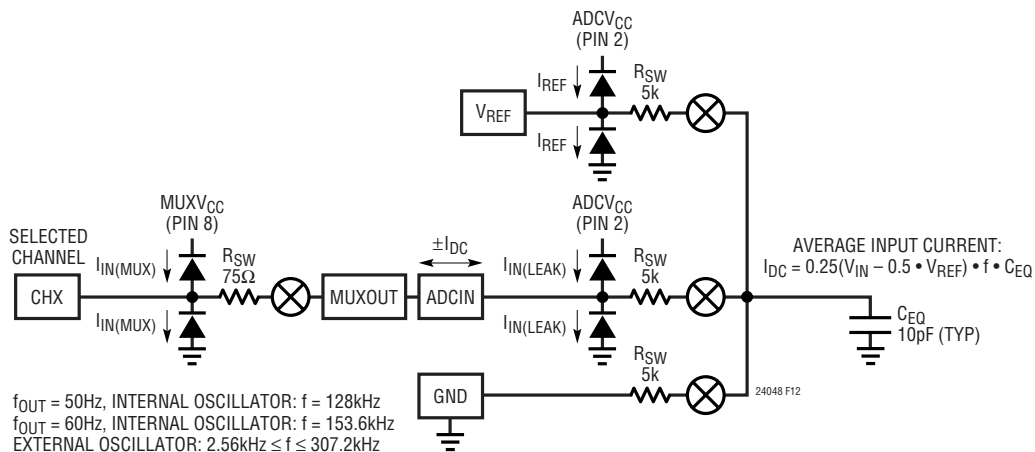
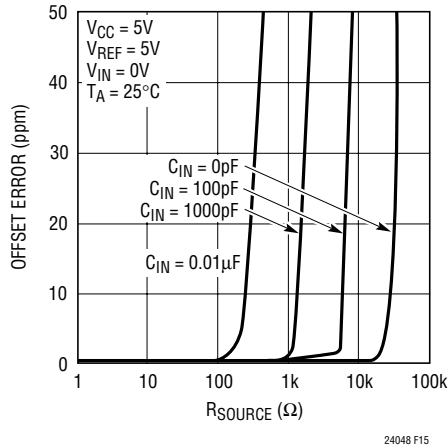
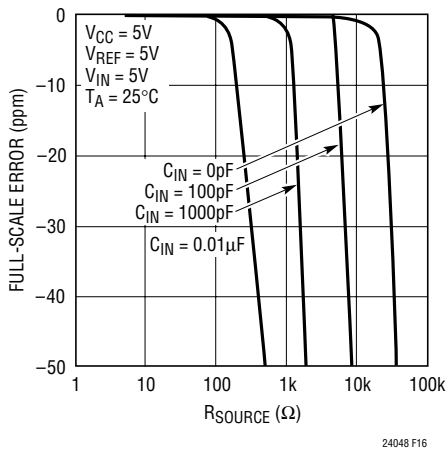


Figure 12. LTC2404/LTC2408 Equivalent Analog Input Circuit



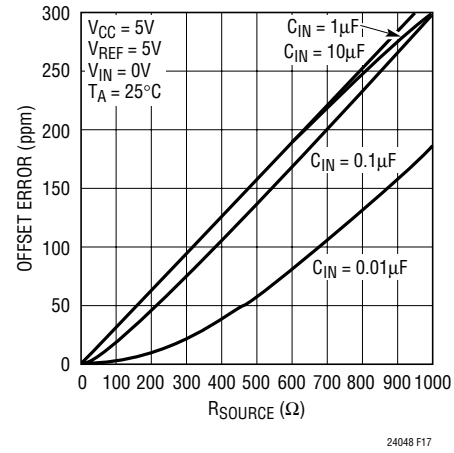
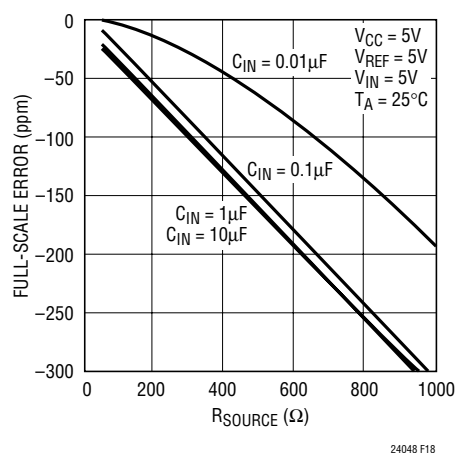
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Figure 15. Offset vs  $R_{SOURCE}$  (Small C)Figure 16. Full-Scale Error vs  $R_{SOURCE}$  (Small C)

small valued input capacitors ( $C_{IN} < 0.01\mu\text{F}$ ) as a function of input source resistance.

For large input capacitor values ( $C_{IN} > 0.01\mu\text{F}$ ), the input spikes are averaged by the capacitor into a DC current. The gain shift becomes a linear function of input source resistance independent of input capacitance, see Figures 17 and 18. The equivalent input impedance is  $1.66\text{M}\Omega$ . This results in  $\pm 1.5\mu\text{A}$  of input dynamic current at the extreme values of  $V_{IN}$  ( $V_{IN} = 0\text{V}$  and  $V_{IN} = V_{REF}$ , when  $V_{REF} = 5\text{V}$ ). This corresponds to a  $0.3\text{ppm}$  shift in offset and full-scale readings for every  $1\Omega$  of input source resistance.

While large capacitance applied to one of the multiplexer channel inputs may result in offset/full-scale shifts, large

Figure 17. Offset vs  $R_{SOURCE}$  (Large C)Figure 18. Full-Scale Error vs  $R_{SOURCE}$  (Large C)

capacitance applied to the MUXOUT/ADCIN results in linearity errors. The  $75\Omega$  on-resistance of the multiplexer switch is nonlinear with input voltage. If the capacitance at node MUXOUT/ADCIN is less than  $0.01\mu\text{F}$ , the linearity is not degraded. On the other hand, excessive capacitance ( $>0.01\mu\text{F}$ ) results in incomplete settling as a function of the multiplexer on-resistance. Hence, the nonlinearity of the multiplexer switch is seen in the overall transfer characteristic.

In addition to the input current spikes, the input ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally  $1\text{nA}$  ( $\pm 10\text{nA}$  max), results in a fixed offset shift of  $10\mu\text{V}$  for a  $10\text{k}$  source resistance.

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### Reference Current ( $V_{REF}$ )

Similar to the analog input, the reference input has a dynamic input current. This current has negligible effect on the offset. However, the reference current at  $V_{IN} = V_{REF}$  is similar to the input current at full-scale. For large values of reference capacitance ( $C_{VREF} > 0.01\mu\text{F}$ ), the full-scale error shift is  $0.3\text{ppm}/\Omega$  of external reference resistance independent of the capacitance at  $V_{REF}$ , see Figure 19. If the capacitance tied to  $V_{REF}$  is small ( $C_{VREF} < 0.01\mu\text{F}$ ), an input resistance of up to  $20\text{k}$  ( $20\text{pF}$  parasitic capacitance at  $V_{REF}$ ) may be tolerated, see Figure 20.

Unlike the analog input, the integral nonlinearity of the device can be degraded with excessive external RC time

constants tied to the reference input. If the capacitance at node  $V_{REF}$  is small ( $C_{VREF} < 0.01\mu\text{F}$ ), the reference input can tolerate large external resistances without reduction in INL, see Figure 21. If the external capacitance is large ( $C_{VREF} > 0.01\mu\text{F}$ ), the linearity will be degraded by  $0.15\text{ppm}/\Omega$  independent of capacitance at  $V_{REF}$ , see Figure 22.

In addition to the dynamic reference current, the  $V_{REF}$  ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally  $1\text{nA}$  ( $\pm 10\text{nA}$  max), results in a fixed full-scale shift of  $10\mu\text{V}$  for a  $10\text{k}$  source resistance.

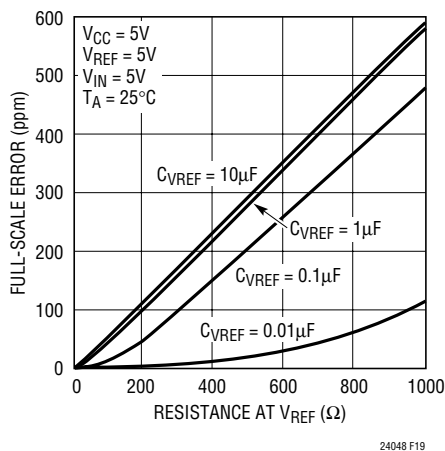


Figure 19. Full-Scale Error vs  $R_{VREF}$  (Large C)

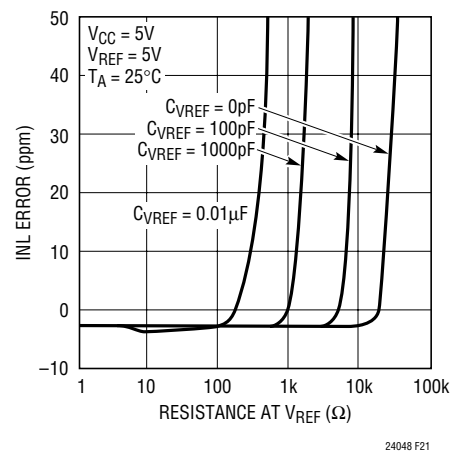


Figure 21. INL Error vs  $R_{VREF}$  (Small C)

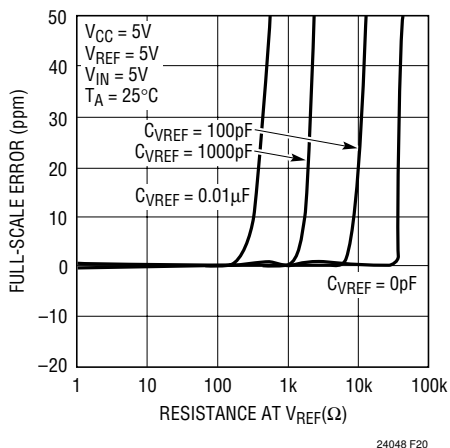


Figure 20. Full-Scale Error vs  $R_{VREF}$  (Small C)

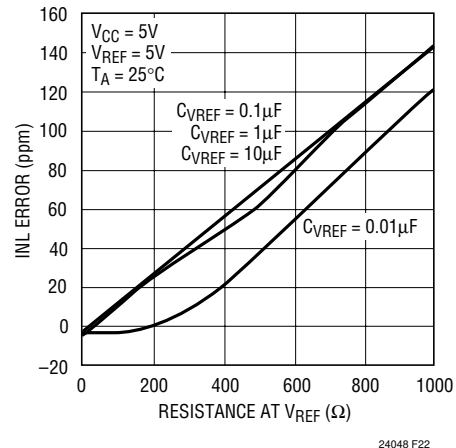


Figure 22. INL Error vs  $R_{VREF}$  (Large C)