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4-/8-Channel 20-Bit µPower No Latency ΔΣ™ ADCs

FEATURES

- **Pin Compatible 4-/8-Channel 20-Bit ADCs**
- **8ppm INL, No Missing Codes at 20 Bits**
- **4ppm Full-Scale Error and 0.5ppm Offset**
- **1.2ppm Noise**
- **Digital Filter Settles in a Single Cycle. Each Conversion is Accurate, Even After Changing Channels**
- **Fast Mode: 16-Bit Noise, 12-Bit TUE at 100sps**
- Internal Oscillator—No External Components Required
- 110dB Min, 50Hz/60Hz Notch Filter
- Reference Input Voltage: 0.1V to V_{CC}
- Live Zero—Extended Input Range Accommodates 12.5% Overrange and Underrange
- Single Supply 2.7V to 5.5V Operation
- Low Supply Current (200µA) and Auto Shutdown
- Can Be Interchanged with 24-Bit LTC2404/LTC2408 if ZS_{SET} Pin is Grounded

APPLICATIONS

- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control
- 4-Digit DVMs

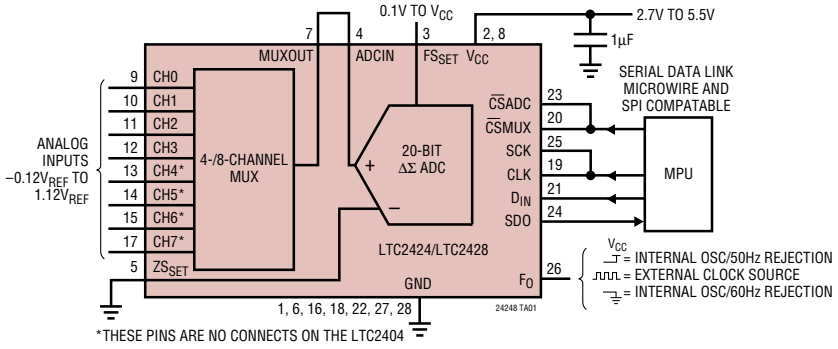
DESCRIPTION

The LTC®2424/LTC2428 are 4-/8-channel 2.7V to 5.5V micropower 20-bit A/D converters with an integrated oscillator, 8ppm INL and 1.2ppm RMS noise. They use delta-sigma technology and provide single cycle digital filter settling time (no latency delay) for multiplexed applications. The first conversion after the channel is changed is always valid. Through a single pin the LTC2424/LTC2428 can be configured for better than 110dB rejection at 50Hz or 60Hz ±2%, or can be driven by an external oscillator for a user defined rejection frequency in the range 1Hz to 800Hz. The internal oscillator requires no external frequency setting components.

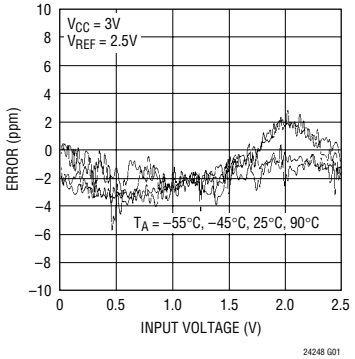
The converters accept any external reference voltage from 0.1V to V_{CC}. With their extended input conversion range of –12.5% V_{REF} to 112.5% V_{REF} ($V_{REF} = FS_{SET} – ZS_{SET}$) the LTC2424/LTC2428 smoothly resolve the offset and overrange problems of preceding sensors or signal conditioning circuits.

The LTC2424/LTC2428 communicate through a flexible 4-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.

TYPICAL APPLICATION



Total Unadjusted Error (3V Supply)



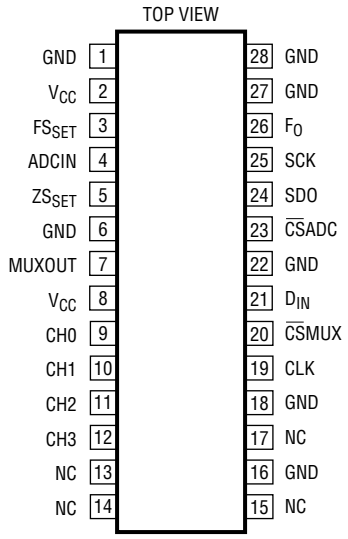
ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) to GND ..... –0.3V to 7V
Analog Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Voltage to GND .. –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)

Operating Temperature Range
LTC2424C/LTC2428C ..... 0°C to 70°C
LTC2424I/LTC2428I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION

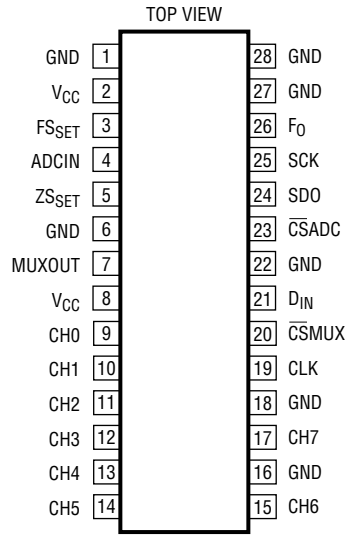


G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC2424CG
LTC2424IG



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 130°C/W

ORDER PART NUMBER

LTC2428CG
LTC2428IG

Consult factory for parts specified with wider operating temperature ranges.

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, (Note 5)	●	20			Bits
Integral Nonlinearity	V_{REF} = 2.5V (Note 6) V_{REF} = 5V (Note 6)	● ●		4 8	10 20	ppm of V_{REF} ppm of V_{REF}
Integral Nonlinearity (Fast Mode)	2.5V < V_{REF} < V_{CC}, 100 Samples/Second, f_O = 2.051MHz	●		40	250	ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		0.5	10	ppm of V_{REF}
Offset Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.051MHz			3		ppm of V_{REF}
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C
Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}	●		4	15	ppm of V_{REF}
Full-Scale Error (Fast Mode)	2.5V < V_{REF} < 5V, 100 Samples/Second, f_O = 2.051MHz			10		ppm of V_{REF}
Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}			0.04		ppm of V_{REF}/°C

CONVERTER CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Total Unadjusted Error	V_{REF} = 2.5V V_{REF} = 5V			8 16		ppm of V_{REF} ppm of V_{REF}
Output Noise	V_{IN} = 0V, V_{REF} = 5V (Note 13)			6		μV_{RMS}
Output Noise (Fast Mode)	V_{REF} = 5V, 100 Samples/Second, f_O = 2.051MHz			20		μV_{RMS}
Normal Mode Rejection 60Hz ±2%	(Note 7)	●	110	130		dB
Normal Mode Rejection 50Hz ±2%	(Note 8)	●	110	130		dB
Power Supply Rejection, DC	V_{REF} = 2.5V, V_{IN} = 0V			100		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 7, 16)			110		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, V_{IN} = 0V, (Notes 8, 16)			110		dB

ANALOG INPUT AND REFERENCE

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Input Voltage Range	(Note 14)	●	−0.125 • V_{REF}		1.125 • V_{REF}	V
V_{REF}	Reference Voltage Range		●	0.1		V_{CC}	V
$C_{S(IN)}$	Input Sampling Capacitance				1		pF
$C_{S(REF)}$	Reference Sampling Capacitance				1.5		pF
$I_{IN(LEAK)}$	Input Leakage Current	$\overline{CS}$ = V_{CC}	●	−100	1	100	nA
$I_{REF(LEAK)}$	Reference Leakage Current	V_{REF} = 2.5V, $\overline{CS}$ = V_{CC}	●	−100	1	100	nA
$I_{IN(MUX)}$	On Channel Leakage Current	V_S = 2.5V (Note 15)	●			±20	nA
R_{ON}	MUX On-Resistance	I_{OUT} = 1mA, V_{CC} = 2.7V I_{OUT} = 1mA, V_{CC} = 5V	● ●		250 120	300 250	Ω Ω
	MUX ΔR_{ON} vs Temperature				0.5		%/°C
	ΔR_{ON} vs V_S (Note 15)				20		%
$I_{S(OFF)}$	MUX Off Input Leakage	Channel Off, V_S = 2.5V	●			±20	nA
$I_{D(OFF)}$	MUX Off Output Leakage	Channel Off, V_D = 2.5V	●			±20	nA
t_{OPEN}	MUX Break-Before-Make Interval				290		ns
t_{ON}	Enable Turn-On Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF			490		ns
t_{OFF}	Enable Turn-Off Time	V_S = 1.5V, R_L = 3.4k, C_L = 15pF			190		ns
$C_{S(OFF)}$	Input Off Capacitance (MUX)				10		pF
$C_{D(OFF)}$	Output Off Capacitance (MUX)				10		pF
	MUX OFF Isolation Channel-to-Channel	DC at 1Hz at f_S = 15,360Hz			120 120 120		dB dB dB

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O	2.7V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 3.3V	● 	2.5 2.0			V V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O	4.5V ≤ V_{CC} ≤ 5.5V 2.7V ≤ V_{CC} ≤ 5.5V	● 			0.8 0.6	V V
V_{IH}	High Level Input Voltage SCK	2.7V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 3.3V (Note 9)	● 	2.5 2.0			V V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 9) 2.7V ≤ V_{CC} ≤ 5.5V (Note 9)	● 			0.8 0.6	V V
I_{IN}	Digital Input Current $\overline{CS}$, F_O	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 9)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 9)			10		pF
V_{OH}	High Level Output Voltage SDO	I_O = –800µA	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SDO	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 10)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 10)	●			0.4	V
I_{OZ}	High-Z Output Leakage SDO		●	–10		10	µA
V_{IN} H_{MUX}	MUX High Level Input Voltage	V^+ = 3V	●	2			V
V_{IN} L_{MUX}	MUX Low Level Input Voltage	V^+ = 2.4V	●			0.8	V

POWER REQUIREMENTS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current (Pin 2) Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 12) $\overline{CS}$ = V_{CC} (Note 12)	 ● ●		 200 20	 300 30	 µA µA
$I_{CC(MUX)}$	Multiplexer Supply Current (Pin 8)	All Logic Inputs Tied Together V_{IN} = 0V or 5V	●		15	40	µA

TIMING CHARACTERISTICS

The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	20-Bit Effective Resolution 12-Bit Effective Resolution	● ●	2.56 2.56k		307.2 2.048M	kHz Hz
t_{HEO}	External Oscillator High Period		●	0.5		390	µs
t_{LEO}	External Oscillator Low Period		●	0.5		390	µs
t_{CONV}	Conversion Time	F_O = 0V F_O = V_{CC} External Oscillator (Note 11)	● ● ●	130.86 157.03 20510/f_{EOSC} (in kHz)	133.53 160.23	136.20 163.44	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 10) External Oscillator (Notes 10, 11)		19.2 f_{EOSC}/8			kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Note 10)		45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 9)	●			2000	kHz
t_{LESCK}	External SCK Low Period	(Note 9)	●	250			ns
t_{HESCK}	External SCK High Period	(Note 9)	●	250			ns
t_{DOUT_ISCK}	Internal SCK 24-Bit Data Output Time	Internal Oscillator (Notes 10, 12) External Oscillator (Notes 10, 11)	● ●	1.23 192/f_{EOSC} (in kHz)	1.25	1.28	ms ms
t_{DOUT_ESCK}	External SCK 24-Bit Data Output Time	(Note 9)	●	24/f_{ESCK} (in kHz)			ms
t_1	$\overline{CS}$ ↓ to SDO Low Z		●	0		150	ns
t_2	$\overline{CS}$ ↑ to SDO High Z		●	0		150	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 10)	●	0		150	ns
t_4	$\overline{CS}$ ↓ to SCK ↑	(Note 9)	●	50			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Set-Up Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns

Note 1: Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 2.7 to 5.5V unless otherwise specified, source input is 0Ω. $\overline{CS}$ADC = $\overline{CS}$MUX = $\overline{CS}$. V_{REF} = FS_{SET} – ZS_{SET}.

Note 4: Internal Conversion Clock source with the F_O pin tied to GND or to V_{CC} or to external conversion clock source with f_{EOSC} = 153600Hz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: F_O = 0V (internal oscillator) or f_{EOSC} = 153600Hz ±2% (external oscillator).

Note 8: F_O = V_{CC} (internal oscillator) or f_{EOSC} = 128000Hz ±2% (external oscillator).

Note 9: The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in kHz.

Note 10: The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance C_{LOAD} = 20pF.

Note 11: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses the internal oscillator. F_O = 0V or F_O = V_{CC}.

Note 13: The output noise includes the contribution of the internal calibration operations.

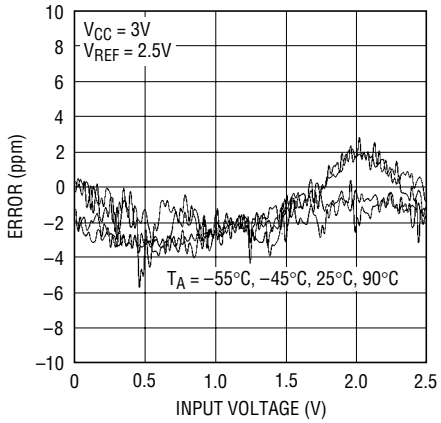
Note 14: V_{REF} = FS_{SET} – ZS_{SET}. The minimum input voltage is limited to –0.3V and the maximum to V_{CC} + 0.3V.

Note 15: V_S is the voltage applied to a channel input. V_D is the voltage applied to the MUX output.

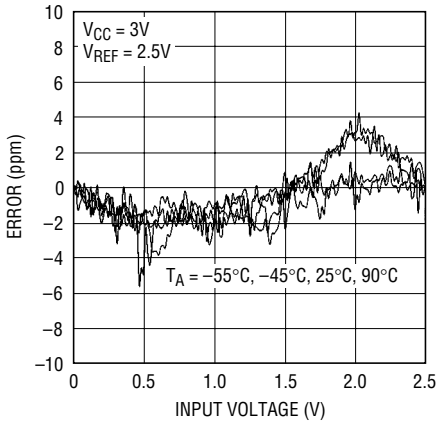
Note 16: $V_{CC(DC)}$ = 4.1V, $V_{CC(AC)}$ = 2.8V_{P-P}.

TYPICAL PERFORMANCE CHARACTERISTICS

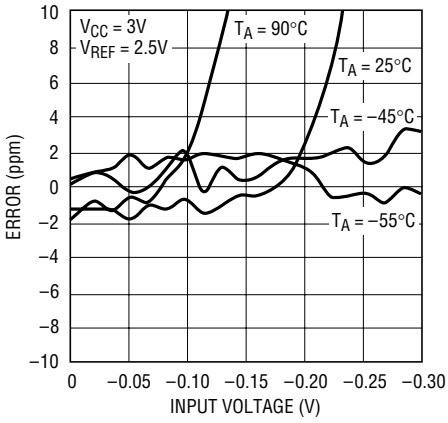
Total Unadjusted Error (3V Supply)



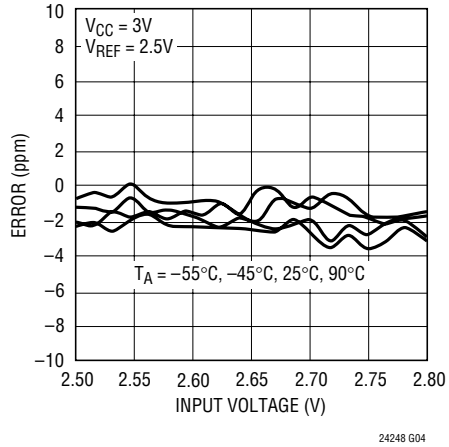
INL (3V Supply)



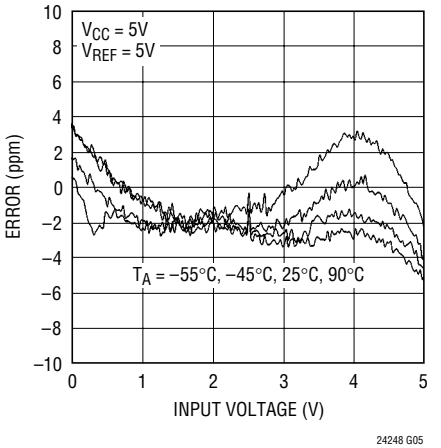
Negative Input Extended Total Unadjusted Error (3V Supply)



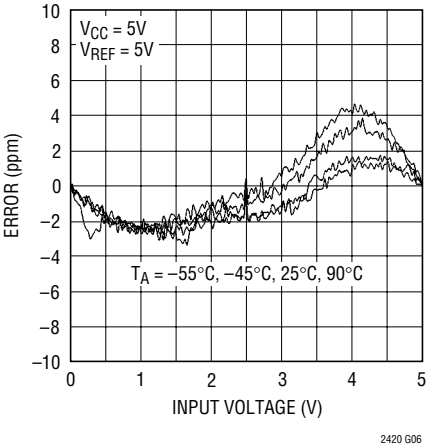
Positive Input Extended Total Unadjusted Error (3V Supply)



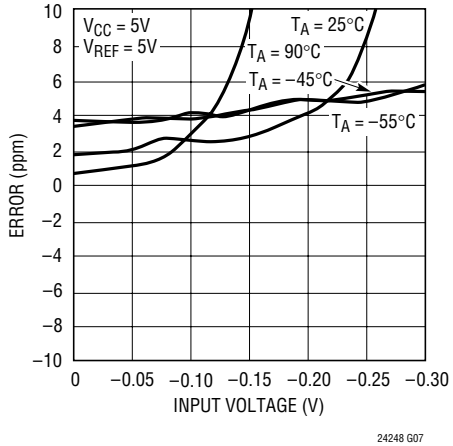
Total Unadjusted Error (5V Supply)



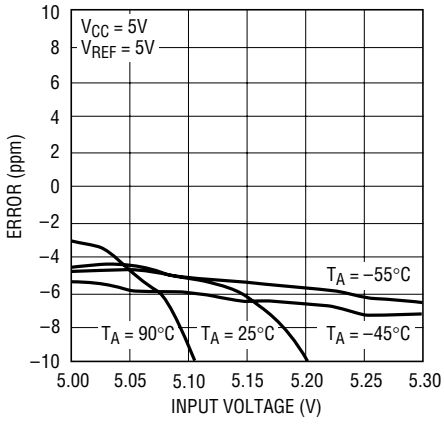
INL (5V Supply)



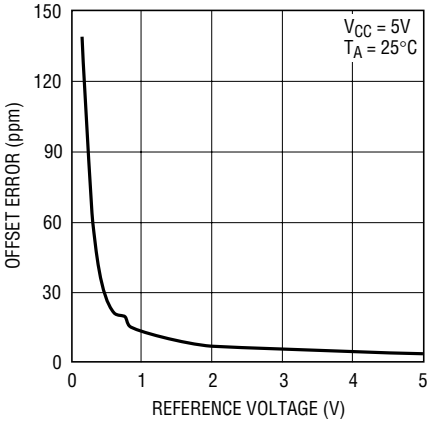
Negative Input Extended Total Unadjusted Error (5V Supply)



Positive Input Extended Total Unadjusted Error (5V Supply)

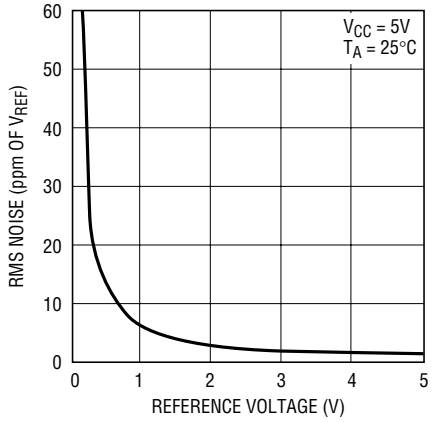


Offset Error vs Reference Voltage



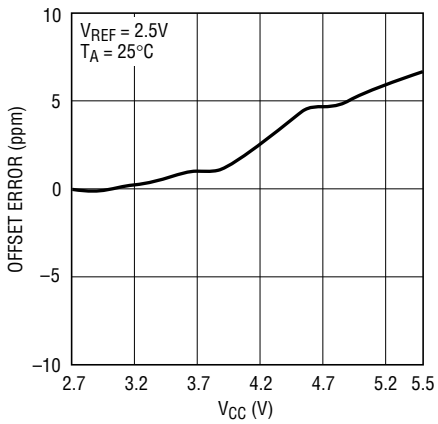
TYPICAL PERFORMANCE CHARACTERISTICS

RMS Noise vs Reference Voltage



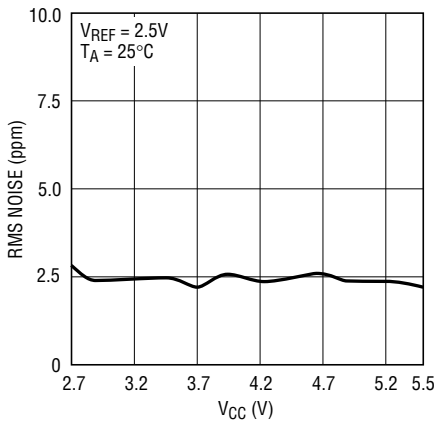
24248 G10

Offset Error vs V_{CC}



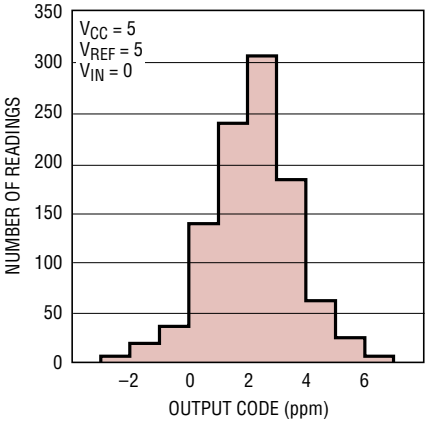
24248 G11

RMS Noise vs V_{CC}



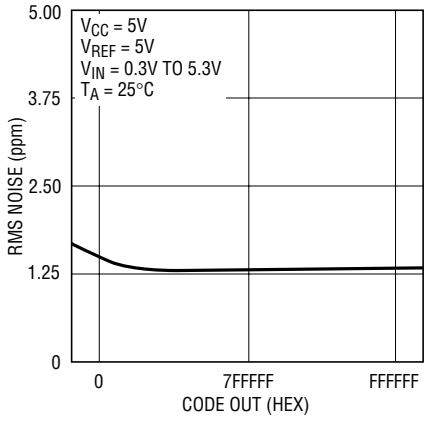
24248 G12

Noise Histogram



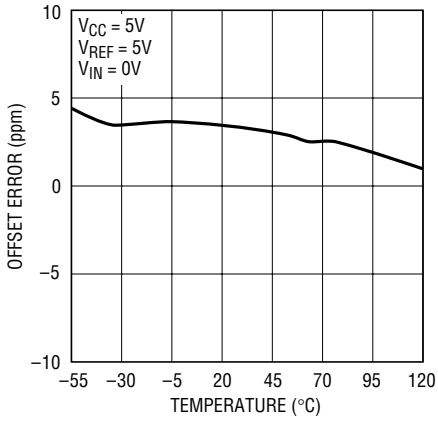
24248G13

RMS Noise vs Code Out



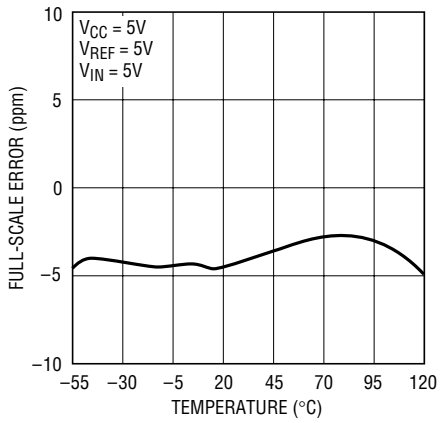
24248 G14

Offset Error vs Temperature



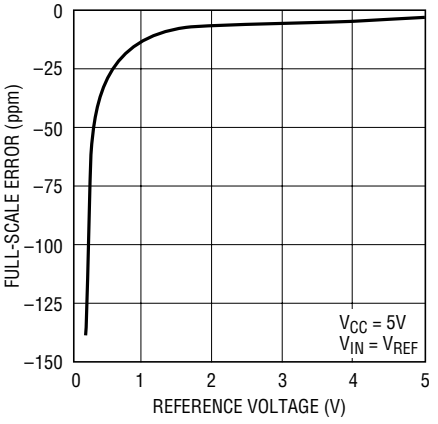
24248 G15

Full-Scale Error vs Temperature



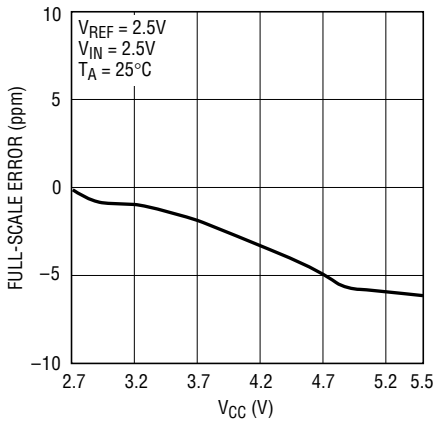
24248 G16

Full-Scale Error vs Reference Voltage



24248 G17

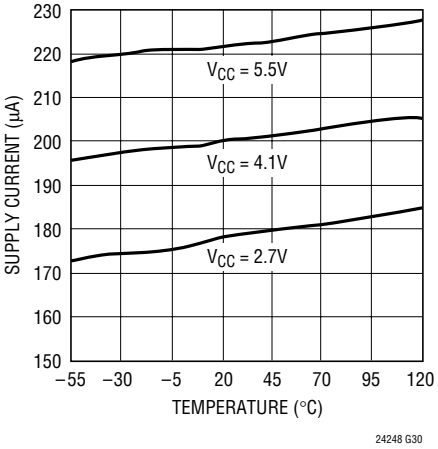
Full-Scale Error vs V_{CC}



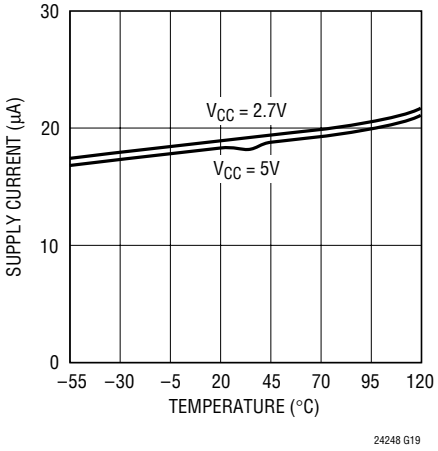
24248 G18

TYPICAL PERFORMANCE CHARACTERISTICS

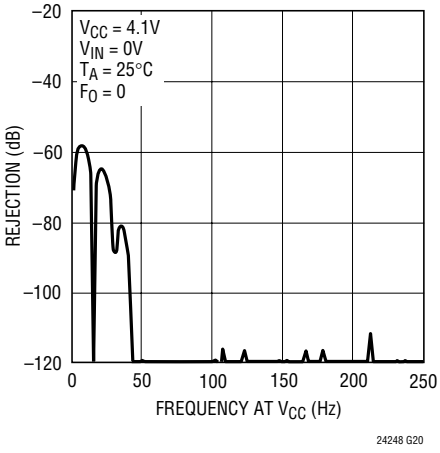
Conversion Current vs Temperature



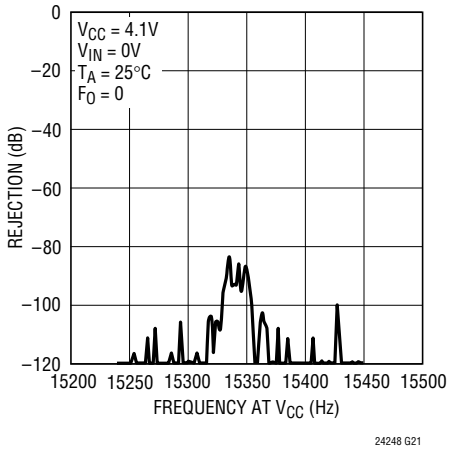
Sleep Current vs Temperature



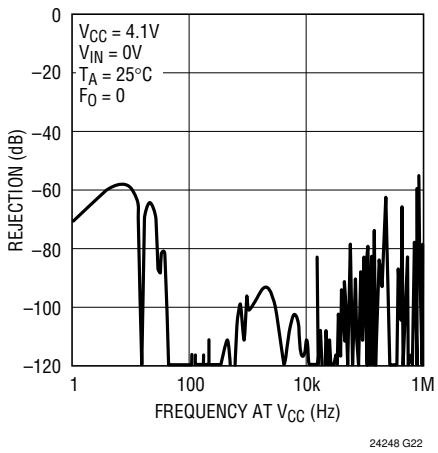
Rejection vs Frequency at V_{CC}



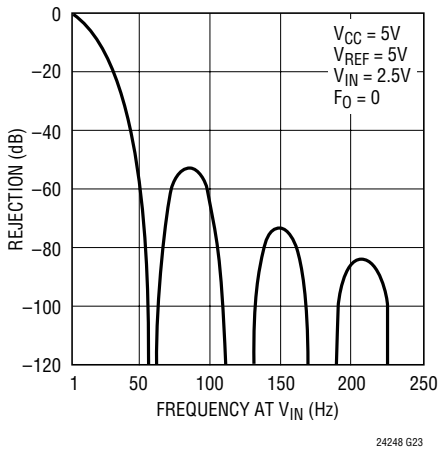
Rejection vs Frequency at V_{CC}



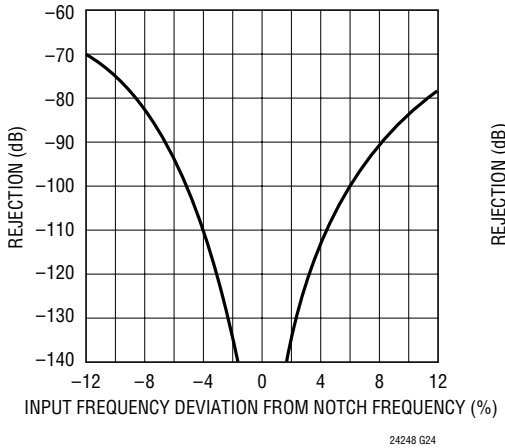
Rejection vs Frequency at V_{CC}



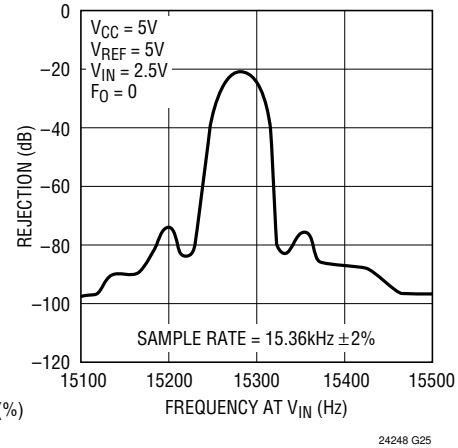
Rejection vs Frequency at V_{IN}



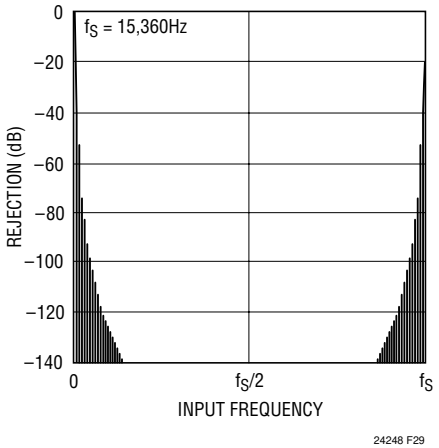
Rejection vs Frequency at V_{IN}



Rejection vs Frequency at V_{IN}

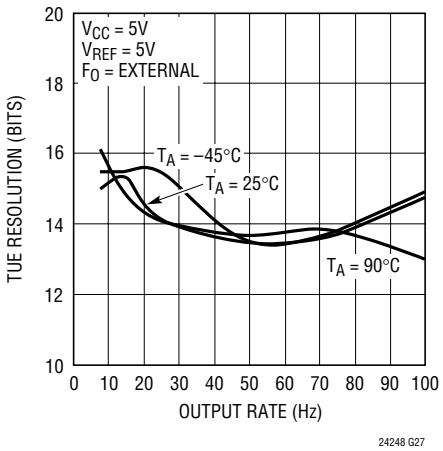


Rejection vs Frequency at V_{IN}

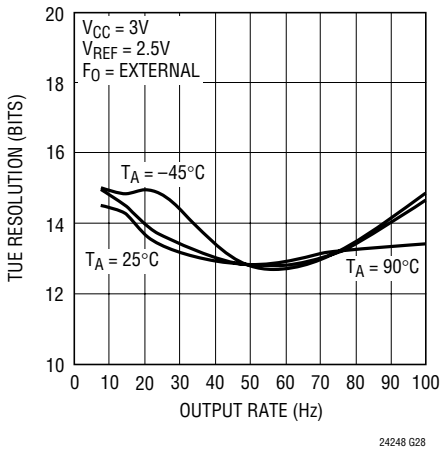


TYPICAL PERFORMANCE CHARACTERISTICS

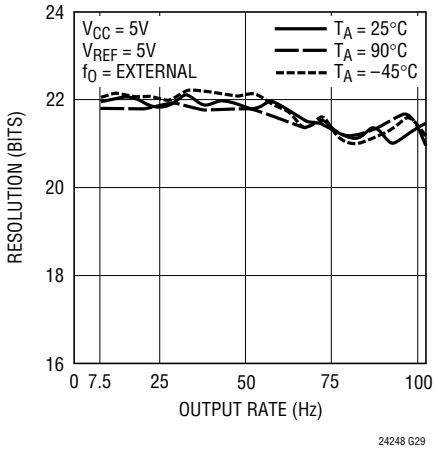
INL vs Output Rate



INL vs Output Rate



Resolution vs Output Rate



PIN FUNCTIONS

GND (Pins 1, 6, 16, 18, 22, 27, 28): Ground. Should be connected directly to a ground plane through a minimum length trace or it should be the single-point-ground in a single-point grounding system.

V_{CC} (Pins 2, 8): Positive Supply Voltage. 2.7V ≤ V_{CC} ≤ 5.5V. Bypass to GND with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

FS_{SET} (Pin 3): Full-Scale Set Input. This pin defines the full-scale input value. When $V_{IN} = FS_{SET}$, the ADC outputs full scale ($FFFFF_H$). The total reference voltage (V_{REF}) is $FS_{SET} – ZS_{SET}$.

ADCIN (Pin 4): Analog Input. The input voltage range is –0.125 • V_{REF} to 1.125 • V_{REF}. For V_{REF} > 2.5V the input voltage range may be limited by the pin absolute maximum rating of –0.3V to V_{CC} + 0.3V.

ZS_{SET} (Pin 5): Zero-Scale Set Input. This pin defines the zero-scale input value. When $V_{IN} = ZS_{SET}$, the ADC outputs zero scale (00000_H). For pin compatibility with the LTC2404/LTC2408 this pin must be grounded.

MUXOUT (Pin 7): MUX Output. This pin is the output of the multiplexer. Tie to ADCIN for normal operation.

CH0 (Pin 9): Analog Multiplexer Input.

CH1 (Pin 10): Analog Multiplexer Input.

CH2 (Pin 11): Analog Multiplexer Input.

CH3 (Pin 12): Analog Multiplexer Input.

CH4 (Pin 13): Analog Multiplexer Input. No connect on the LTC2424.

CH5 (Pin 14): Analog Multiplexer Input. No connect on the LTC2424.

CH6 (Pin 15): Analog Multiplexer Input. No connect on the LTC2424.

CH7 (Pin 17): Analog Multiplexer Input. No connect on the LTC2424.

CLK (Pin 19): Shift Clock for Data In. This clock synchronizes the serial data transfer into the MUX. For normal operation, drive this pin in parallel with SCK.

$\overline{CS}$MUX (Pin 20): MUX Chip Select Input. A logic high on this input allows the MUX to receive a channel address. A logic low enables the selected MUX channel and connects it to the MUXOUT pin for A/D conversion. For normal operation, drive this pin in parallel with $\overline{CS}$ADC.

D_{IN} (Pin 21): Digital Data Input. The multiplexer address is shifted into this input on the last four rising CLK edges before $\overline{CS}$MUX goes low.

PIN FUNCTIONS

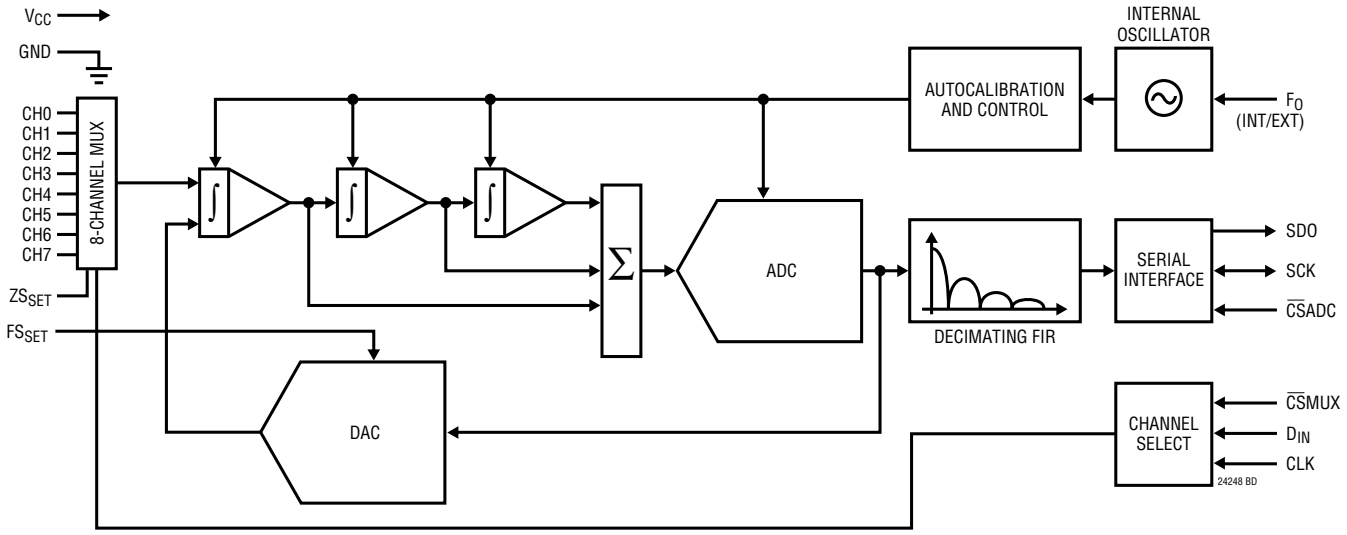
$\overline{CS}$ADC (Pin 23): ADC Chip Select Input. A low on this pin enables the SDO digital output and following each conversion, the ADC automatically enters the Sleep mode and remains in a low power state as long as $\overline{CS}$ADC is high. If $\overline{CS}$ADC is low during the sleep state, the device draws normal power. A high on this pin also disables the SDO digital output. A low-to-high transition on $\overline{CS}$ADC during the Data Output state aborts the data transfer and starts a new conversion. For normal operation, drive this pin in parallel with $\overline{CS}$MUX.

SDO (Pin 24): Three-State Digital Output. During the data output period this pin is used for serial data output. When the chip select $\overline{CS}$ADC is high ($\overline{CS}$ADC = V_{CC}), the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin can be used as a conversion status output. The conversion status can be observed by pulling $\overline{CS}$ADC low.

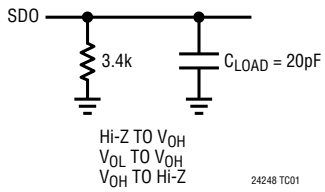
SCK (Pin 25): Shift Clock for Data Out. This clock synchronizes the serial data transfer of the ADC data output. Data is shifted out of SDO on the falling edge of SCK. For normal operation, drive this pin in parallel with CLK.

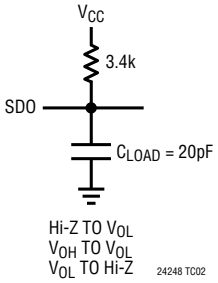
F_O (Pin 26): Digital input which controls the ADC's notch frequencies and conversion time. When the F_O pin is connected to V_{CC} ($F_O = V_{CC}$), the converter uses its internal oscillator and the digital filter first null is located at 50Hz. When the F_O pin is connected to GND (F_O = OV), the converter uses its internal oscillator and the digital filter first null is located at 60Hz. When F_O is driven by an external clock signal with a frequency f_{EOSC}, the converter uses this signal as its clock and the digital filter first null is located at a frequency $f_{EOSC}/2560$. The resulting output word rate is $f_{EOSC}/20510$.

FUNCTIONAL BLOCK DIAGRAM



TEST CIRCUITS





APPLICATIONS INFORMATION

Converter Operation Cycle

The LTC2424/LTC2428 are low power, 4-/8-channel delta-sigma analog-to-digital converters with easy-to-use 4-wire interfaces. Their operation is simple and made up of four states. The converter operation begins with the conversion, followed by a sleep state and concluded with the data output (see Figure 1). Channel selection may be performed while the device is in the sleep state or at the conclusion of the data output state. The interface consists of serial data output (SDO), serial clock (CLK/SCK), chip select ($\overline{CS}$ADC/$\overline{CS}$MUX) and data input (D_{IN}). By tying SCK to CLK and $\overline{CS}$ADC to $\overline{CS}$MUX, the interface requires only four wires.

Initially, the LTC2424 or LTC2428 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state if $\overline{CS}$ADC is high, power consumption is reduced by an order of magnitude. The part remains in the sleep state as long as $\overline{CS}$ADC is logic HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Channel selection for the next conversion cycle is performed while the device is in the sleep state or at the end of the data output state. A specific channel is selected by applying a 4-bit serial word to the D_{IN} pin on the rising edge of CLK while $\overline{CS}$MUX is HIGH, see Figure 4 and Table 3. The channel is selected based on the last four bits clocked into the D_{IN} pin before $\overline{CS}$MUX goes low. If D_{IN} is all 0's, the previous channel remains selected.

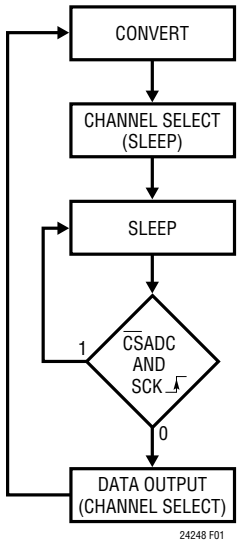


Figure 1. LTC2428 State Transition Diagram

In the example, Figure 4, the MUX channel is selected during the sleep state, just before the data output state begins. Once the channel selection is complete, the device remains in the sleep state as long as $\overline{CS}$ADC remains HIGH.

Once $\overline{CS}$ADC is pulled low, the device begins outputting the conversion result. There is no latency in the conversion result. Since there is no latency, the first conversion following a change in input channel is valid and corresponds to that channel. The data output corresponds to the conversion just performed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK, see Figure 4. The data output state is concluded once 24 bits are read out of the ADC or when $\overline{CS}$ADC is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the $\overline{CS}$ADC and SCK pins, the LTC2424/LTC2428 offer two modes of operation: internal or external SCK. These modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Conversion Clock

A major advantage delta-sigma converters offer over conventional type converters is an on-chip digital filter (commonly known as Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50 or 60Hz plus their harmonics. In order to reject these frequencies in excess of 110dB, a highly accurate conversion clock is required. The LTC2424/LTC2428 incorporate an on-chip highly accurate oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2424/LTC2428 reject line frequencies (50 or 60Hz ±2%) a minimum of 110dB.

APPLICATIONS INFORMATION

Ease of Use

The LTC2424/LTC2428 data output has no latency, filter settling or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing an analog input voltage is easy.

The LTC2424/LTC2428 perform offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2424/LTC2428 automatically enter an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with duration of approximately 0.5ms. The POR signal clears all internal registers within the ADC and initiates a conversion. At power-up, the multiplexer channel is disabled and should be programmed once the device enters the sleep state. The results of the first conversion following a POR are not valid since a multiplexer channel was disabled.

Reference Voltage Range

The LTC2424/LTC2428 can accept a reference voltage ($V_{REF} = FS_{SET} – ZS_{SET}$) from 0V to V_{CC}. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the overall converter INL performance. The recommended range for the LTC2424/LTC2428 voltage reference is 100mV to V_{CC}.

Input Voltage Range

The converter is able to accommodate system level offset and gain errors as well as system level overrange situations due to its extended input range, see Figure 2.

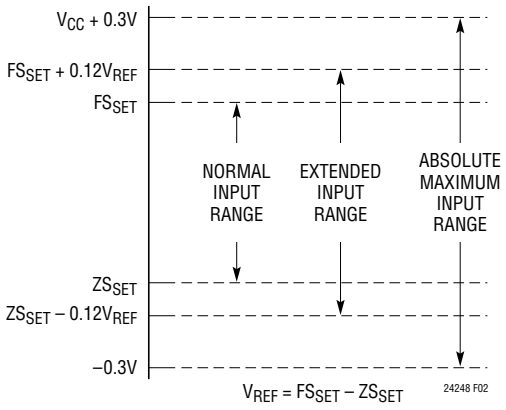


Figure 2. LTC2424/LTC2428 Input Range

The LTC2424/LTC2428 converts input signals within the extended input range of $–0.125 • V_{REF}$ to $1.125 • V_{REF}$ ($V_{REF} = FS_{SET} – ZS_{SET}$).

For large values of V_{REF} this range is limited to a voltage range of –0.3V to (V_{CC} + 0.3V). Beyond this range the input ESD protection devices begin to turn on and the errors due to the input leakage current increase rapidly.

Input signals applied to V_{IN} may extend below ground by –300mV and above V_{CC} by 300mV. In order to limit any fault current, a resistor of up to 5k may be added in series with any channel input pin (CH0 to CH7) without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between this series resistance and the channel input pin as low as possible; therefore, the resistor should be located as close as practical to the channel input pin. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Analog Input/Reference Current section. In addition, a series resistor will introduce a temperature dependent offset error due to the input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

Output Data Format

The LTC2424/LTC2428 serial output data stream is 24 bits long. The first 4 bits represent status information indicating the sign, input range and conversion state. The next 20 bits are the conversion result, MSB first.

APPLICATIONS INFORMATION

The LTC2424/LTC2428 can be interchanged with the LTC2404/LTC2408. The two devices are designed to allow the user to incorporate either device in the same design as long as ZS_{SET} (Pin 5) of the LTC2424/LTC2428 is tied to ground. While the LTC2424/LTC2428 output word lengths are 24 bits (as opposed to the 32-bit output of the LTC2404/LTC2408), their output clock timing can be identical to the LTC2404/LTC2408. As shown in Figure 3, the LTC2424/LTC2428 data output is concluded on the falling edge of the 24th serial clock (SCK). In order to maintain drop-in compatibility with the LTC2404/LTC2408, it is possible to clock the LTC2424/LTC2428 with an additional 8 serial clock pulses. This results in 8 additional output bits which are logic HIGH.

Bit 23 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 22 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 21 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW. The sign bit changes state during the zero code.

Bit 20 (forth output bit) is the extended input range (EXR) indicator. If the input is within the normal input range $0 \le V_{IN} \le V_{REF}$, this bit is LOW. If the input is outside the normal input range, $V_{IN} > V_{REF}$ or $V_{IN} < 0$, this bit is HIGH.

The function of these bits is summarized in Table 1.

Table 1. LTC2424/LTC2428 Status Bits

Input Range	Bit 23 $\overline{EOC}$	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR
$V_{IN} > V_{REF}$	0	0	1	1
$0 < V_{IN} \le V_{REF}$	0	0	1	0
$V_{IN} = 0^+/0^-$	0	0	1/0	0
$V_{IN} < 0$	0	0	0	1

Bit 19 (fifth output bit) is the most significant bit (MSB).

Bits 19-0 are the 20-bit conversion result MSB first.

Bit 0 is the least significant bit (LSB).

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 4. Whenever $\overline{CS}$ADC is HIGH, SDO remains high impedance and any SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ADC must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ADC is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 23 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 22 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 23rd SCK and may be latched on the rising edge of the 24th SCK pulse. On the falling edge of the 24th SCK pulse, SDO goes HIGH indicating a new conversion cycle has been initiated. This bit serves as $\overline{EOC}$ (Bit 23) for the next conversion cycle. Table 2 summarizes the output data format.

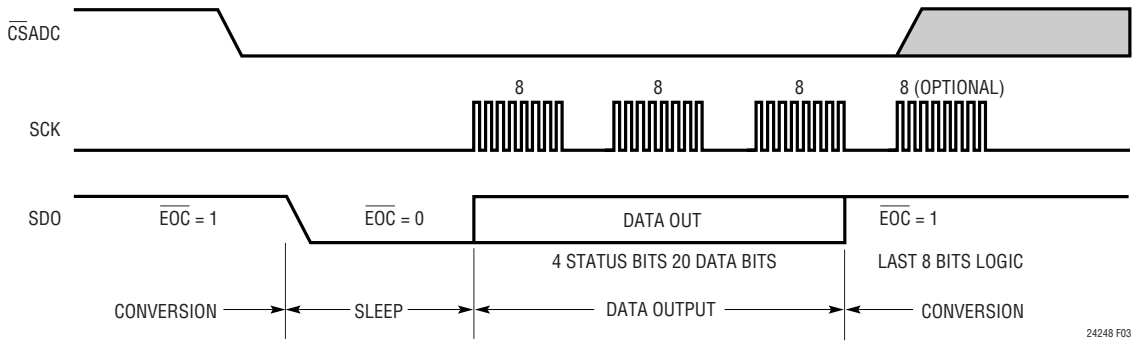


Figure 3. LTC2424/LTC2428 Compatible Timing with the LTC2404/LTC2408

APPLICATIONS INFORMATION

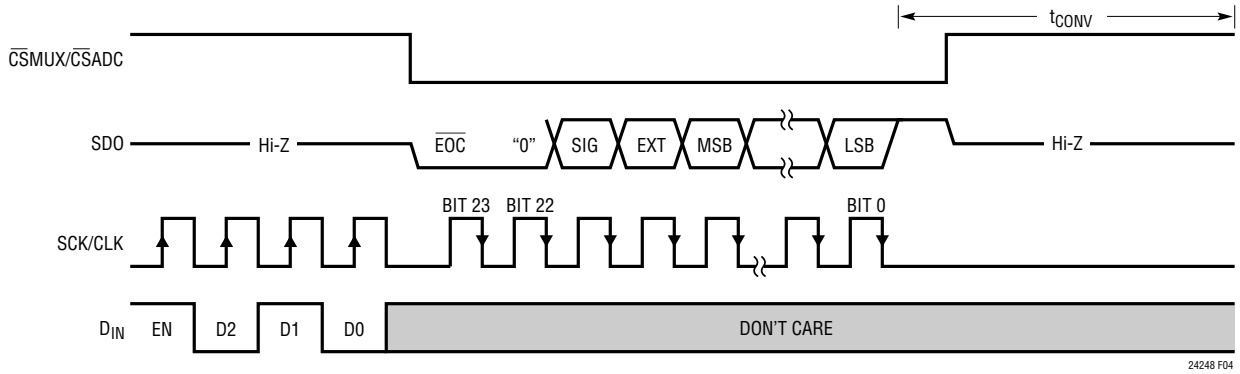


Figure 4. Typical Data Input/Output Timing

Table 2. LTC2424/LTC2428 Output Data Format

Input Voltage	Bit 23 EOC	Bit 22 DMY	Bit 21 SIG	Bit 20 EXR	Bit 19 MSB	Bit 18	Bit 17	Bit 16	Bit 15	...	Bit 0 LSB
$V_{IN} > 9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
$9/8 \cdot V_{REF}$	0	0	1	1	0	0	0	1	1	...	1
V_{REF} + 1LSB	0	0	1	1	0	0	0	0	0	...	0
V_{REF}	0	0	1	0	1	1	1	1	1	...	1
$3/4V_{REF}$ + 1LSB	0	0	1	0	1	1	0	0	0	...	0
$3/4V_{REF}$	0	0	1	0	1	0	1	1	1	...	1
$1/2V_{REF}$ + 1LSB	0	0	1	0	1	0	0	0	0	...	0
$1/2V_{REF}$	0	0	1	0	0	1	1	1	1	...	1
$1/4V_{REF}$ + 1LSB	0	0	1	0	0	1	0	0	0	...	0
$1/4V_{REF}$	0	0	1	0	0	0	1	1	1	...	1
$0^+/0^-$	0	0	1/0*	0	0	0	0	0	0	...	0
–1LSB	0	0	0	1	1	1	1	1	1	...	1
$-1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0
$V_{IN} < -1/8 \cdot V_{REF}$	0	0	0	1	1	1	1	0	0	...	0

*The sign bit changes state during the 0 code.

As long as the voltage on the V_{IN} pin is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any input value from $-0.125 \cdot V_{REF}$ to $1.125 \cdot V_{REF}$. For input voltages greater than $1.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $1.125 \cdot V_{REF}$. For input voltages below $-0.125 \cdot V_{REF}$, the conversion result is clamped to the value corresponding to $-0.125 \cdot V_{REF}$.

Channel Selection

Typically, $\overline{CS}$ADC and $\overline{CS}$MUX are tied together or $\overline{CS}$ADC is inverted and drives $\overline{CS}$MUX. SCK and CLK are tied together and driven with a common clock signal. During channel selection, $\overline{CS}$MUX is HIGH. Data is shifted into the D_{IN} pin on the rising edge of CLK, see Figure 4. Table 3 shows the bit combinations for channel selection. In order to enable the multiplexer output, $\overline{CS}$MUX must be pulled

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LOW. The multiplexer should be programmed after the previous conversion is complete. In order to guarantee the conversion is complete, the multiplexer addressing should be delayed a minimum t_{CONV} (approximately 133ms for a 60Hz notch) after the data out is read.

While the multiplexer is being programmed, the ADC is in the sleep state. Once the MUX addressing is complete, the data from the preceding conversion can be read. A new conversion cycle is initiated following the data read cycle with the analog input tied to the newly selected channel.

Table 3. Logic Table for Channel Selection

CHANNEL STATUS	EN	D2	D1	D0
All Off	0	X	X	X
CH0	1	0	0	0
CH1	1	0	0	1
CH2	1	0	1	0
CH3	1	0	1	1
CH4*	1	1	0	0
CH5*	1	1	0	1
CH6*	1	1	1	0
CH7*	1	1	1	1

*Not used for the LTC2424.

Frequency Rejection Selection (F_O Pin Connection)

The LTC2424/LTC2428 internal oscillator provides better than 110dB normal mode rejection at the line frequency and all its harmonics for 50Hz ±2% or 60Hz ±2%. For 60Hz rejection, F_O (Pin 26) should be connected to GND (Pin 1) while for 50Hz rejection the F_O pin should be connected to V_{CC} (Pin 2).

The selection of 50Hz or 60Hz rejection can also be made by driving F_O to an appropriate logic level. A selection change during the sleep or data output states will not disturb the converter operation. If the selection is made during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected.

When a fundamental rejection frequency different from 50Hz or 60Hz is required or when the converter must be synchronized with an outside source, the LTC2424/LTC2428 can operate with an external conversion clock.

The converter automatically detects the presence of an external clock signal at the F_O pin and turns off the internal oscillator. The frequency f_{EOSC} of the external signal must be at least 2560Hz (1Hz notch frequency) to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods t_{HEO} and t_{LEO} are observed.

While operating with an external conversion clock of a frequency f_{EOSC}, the LTC2424/LTC2428 provide better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4% and its harmonics. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 5.

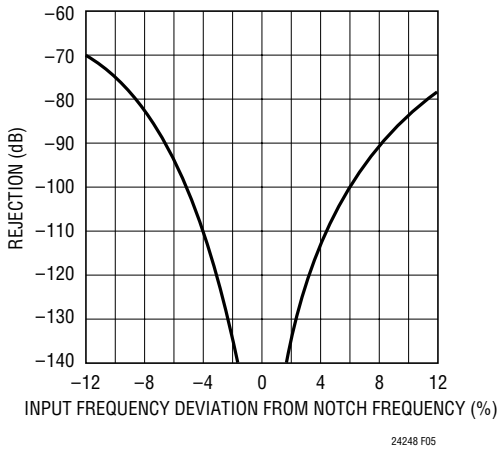

Figure 5. LTC2424/LTC2428 Normal Mode Rejection When Using an External Oscillator of Frequency f_{EOSC}

Whenever an external clock is not present at the F_O pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2424/LTC2428 operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

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Table 4 summarizes the duration of each state as a function of F_O.

Operation at Higher Data Output Rates

The LTC2424/LTC2428 typically operate with an internal oscillator of 153.6kHz. This corresponds to a notch frequency of 60Hz and an output rate of 7.5 samples/second. The internal oscillator is enabled if the F_O pin is logic LOW (logic HIGH for a 50Hz notch). It is possible to drive the F_O pin with an external oscillator for higher data output rates.

As shown in Figure 6, an external clock of 2.051MHz applied to the F_O pin results in a notch frequency of 800Hz with a data output rate of 100 samples/second.

Figure 7 shows the total unadjusted error (Offset Error + Full-Scale Error + INL + DNL) as a function of the output data rate with a 5V reference. The relationship between the output data rate (ODR) and the frequency applied to the F_O pin (F_O) is:

$$ODR = F_O/20510$$

Table 4. LTC2424/LTC2428 State Duration

State	Operating Mode		Duration
CONVERT	Internal Oscillator	F_O = LOW (60Hz Rejection)	133ms
		F_O = HIGH (50Hz Rejection)	160ms
	External Oscillator	F_O = External Oscillator with Frequency f_{EOSC} kHz (f_{EOSC}/2560 Rejection)	20510/f_{EOSC} (In Seconds)
SLEEP			As Long As $\overline{CS}$ADC = HIGH Until $\overline{CS}$ADC = 0 and SCK ⌐
DATA OUTPUT	Internal Serial Clock	F_O = LOW/HIGH (Internal Oscillator)	As Long As $\overline{CS}$ADC = LOW But Not Longer Than 1.67ms (32 SCK cycles)
		F_O = External Oscillator with Frequency f_{EOSC} kHz	As Long As $\overline{CS}$ADC = LOW But Not Longer Than 256/f_{EOSC}ms (32 SCK cycles)
	External Serial Clock with Frequency f_{SCK} kHz		As Long As $\overline{CS}$ADC = LOW But Not Longer Than 32/f_{SCK}ms (32 SCK cycles)
MAXIMUM OUTPUT WORD RATE (OWR)			$OWR = \frac{1}{t_{CONVERT} + t_{DATAOUTPUT}}$ in Hz

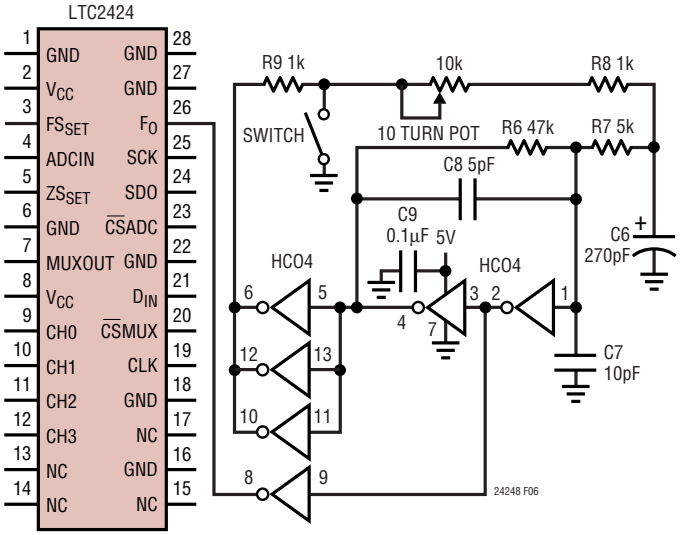

Figure 6. Selectable 100 Sample/Second Turbo Mode

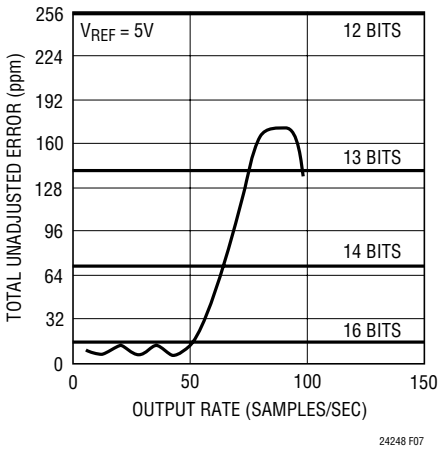

Figure 7. Total Error vs Output Rate (V_{REF} = 5V)

APPLICATIONS INFORMATION

For output data rates up to 50 samples/second, the total unadjusted error (TUE) is better than 16 bits, and better than 12 bits at 100 samples/second. As shown in Figure 8, for output data rates of 100 samples/second, the TUE is better than 15 bits for V_{REF} below 2.5V. Figure 9 shows an unaveraged total unadjusted error for the LTC2424 or LTC2428 operating at 100 samples/second with V_{REF} = 2.5V. Figure 10 shows the same device operating with a 5V reference and an output data rate of 7.5 samples/second.

At 100 samples/second, the LTC2424/LTC2428 can be used to capture transient data. This is useful for monitoring settling or auto gain ranging in a system. The LTC2424/LTC2428 can monitor signals at an output rate of 100 samples/second. After acquiring 100 samples/second data, the F_O pin may be driven LOW enabling 60Hz rejection to 110dB and the highest possible DC accuracy. The no latency architecture of the LTC2424/LTC2428 allows consecutive readings (one at 100 samples/second the next at 7.5 samples/second) without interaction between the two readings.

As shown in Figure 11, the LTC2424/LTC2428 can capture transient data with 90dB of dynamic range (with a 300mV_{P-P} input signal at 2Hz). The exceptional DC performance of the LTC2424/LTC2428 enables signals to be digitized independent of a large DC offset. Figures 12a and 12b show the dynamic performance with a 15Hz signal superimposed on a 2V DC level. The same signal with no DC level is shown in Figures 12c and 12d.

SERIAL INTERFACE

The LTC2424/LTC2428 transmit the conversion results, program the channel selection, and receive the start of conversion command through a synchronous 4-wire interface (SCK = CLK, $\overline{CS}$ADC = $\overline{CS}$MUX). During the conversion and sleep states, this interface can be used to assess the converter status. While in the sleep state this interface may be used to program an input channel. During the data output state, it is used to read the conversion result.

ADC Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 25) is used to synchronize the data transfer. Each bit of data is shifted out of the SDO pin on the falling edge of the serial clock.

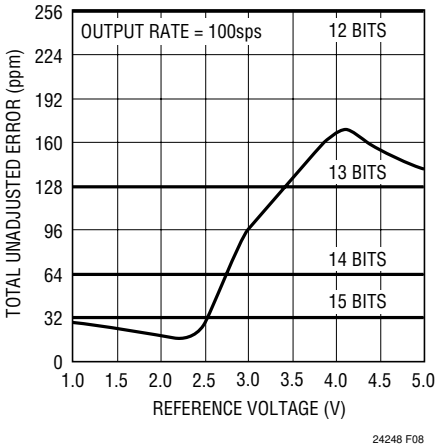

Figure 8. Total Error vs V_{REF} (Output Rate = 100sps)

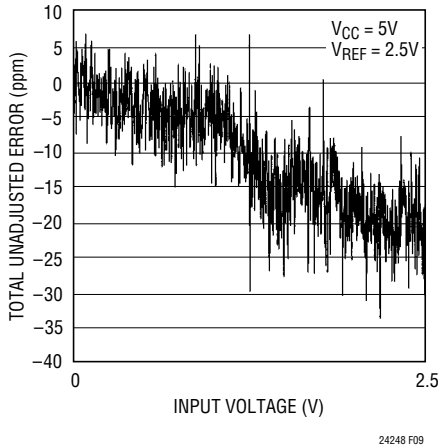

Figure 9. Total Unadjusted Error at 100 Samples/Second (No Averaging)

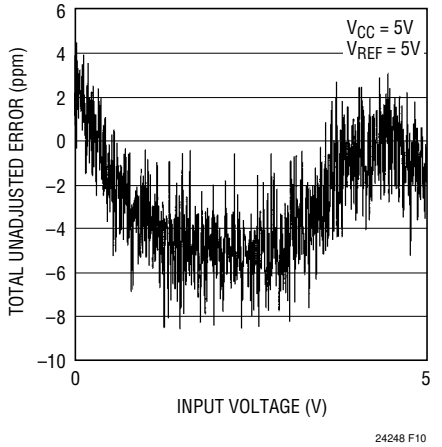

Figure 10. Total Unadjusted Error at 7.5 Samples/Second (No Averaging)

APPLICATIONS INFORMATION

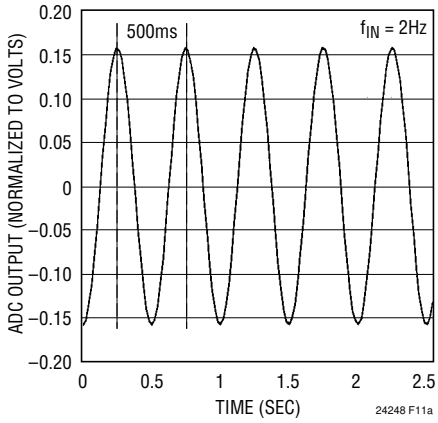

Figure 11a. Digitized Waveform

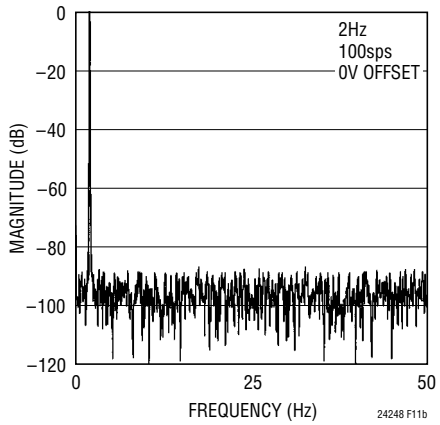

Figure 11b. Output FFT

Figure 11. Transient Signal Acquisition

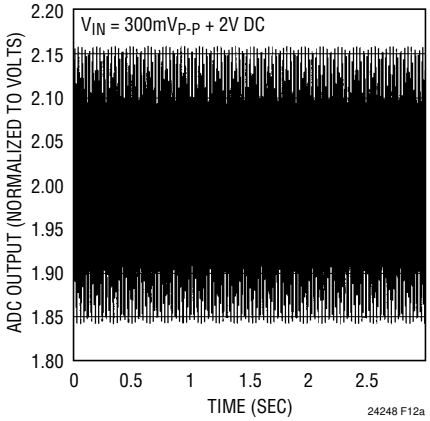

Figure 12a. Digitized Waveform with 2V DC Offset

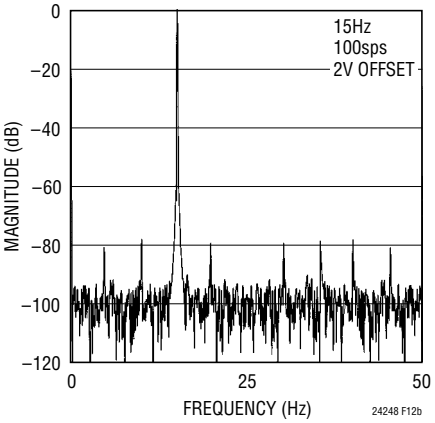

Figure 12b. FFT Waveform with 2V DC Offset

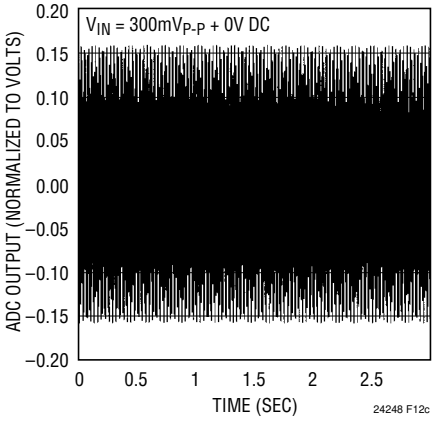

Figure 12c. Digitized Waveform with No Offset

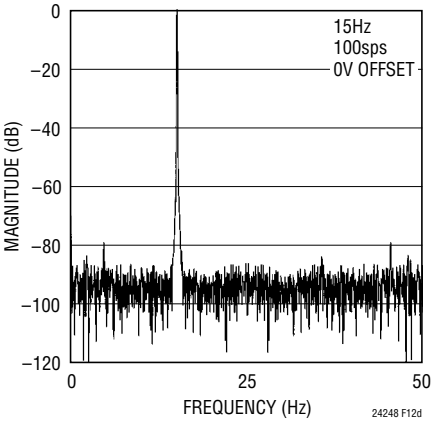

Figure 12d. FFT Waveform with No Offset

Figure 12. Using the LTC2424/LTC2428's High Accuracy Wide Dynamic Range to Digitize a 300mV_{P-P} 15Hz Waveform with a Large DC Offset (V_{CC} = 5V, V_{REF} = 5V)

APPLICATIONS INFORMATION

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2424/LTC2428 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ADC pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

Multiplexer Serial Input Clock (CLK)

Generally, this pin is externally tied to SCK for 4-wire operation. On the rising edge of CLK (Pin 19) with $\overline{CS}$MUX held HIGH, data is serially shifted into the multiplexer. If $\overline{CS}$MUX is LOW the CLK input will be disabled and the channel selection unchanged.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 24), drives the serial data during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ADC (Pin 23) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ADC is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ADC is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ADC = 0.

ADC Chip Select Input ($\overline{CS}$ADC)

The active LOW chip select, $\overline{CS}$ADC (Pin 23), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ADC signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2424/LTC2428 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ADC pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ADC = 0).

Multiplexer Chip Select ($\overline{CS}$MUX)

For 4-wire operation, this pin is tied directly to $\overline{CS}$ADC or the output of an inverter tied to $\overline{CS}$ADC. $\overline{CS}$MUX (Pin 20) is driven HIGH during selection of a multiplexer channel. On the falling edge of $\overline{CS}$MUX, the selected channel is enabled and drives MUXOUT.

Data Input (D_{IN})

The data input to the multiplexer, D_{IN} (Pin 21), is used to program the multiplexer. The input channel is selected by serially shifting a 4-bit input word into the D_{IN} pin under the control of the multiplexer clock, CLK. Data is shifted into the multiplexer on the rising edge of CLK. Table 3 shows the logic table for channel selection. In order to select or change a previously programmed channel, an enable bit (D_{IN} = 1) must proceed the 3-bit channel select serial data. The user may set D_{IN} = 0 to continually convert on the previously selected channel.

SERIAL INTERFACE TIMING MODES

The LTC2424/LTC2428's 4-wire interface is SPI and MICROWIRE compatible. This interface offers two modes of operation. These include an internal or external serial clock. The following sections describe both of these serial interface timing modes in detail. For both cases the converter can use the internal oscillator (F_O = LOW or F_O = HIGH) or an external oscillator connected to the F_O pin. Refer to Table 5 for a summary.

Table 5. LTC2424/LTC2428 Interface Timing Modes

Configuration	SCK Source	Conversion Cycle Control	Data Output Control	Connection and Waveforms
External SCK	External	$\overline{CS}$ADC and SCK	$\overline{CS}$ADC and SCK	Figures 13, 14, 15
Internal SCK	Internal	$\overline{CS}$ADC ↓	$\overline{CS}$ADC ↓	Figures 16, 17

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External Serial Clock (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock (SCK) to shift out the conversion result, see Figure 13. This same external clock signal drives the CLK pin in order to program the multiplexer. A single $\overline{CS}$ signal drives both the multiplexer $\overline{CS}$MUX and converter $\overline{CS}$ADC inputs. This common signal is used to monitor and control the state of the conversion as well as enable the channel selection.

The serial clock mode is selected on the falling edge of $\overline{CS}$ADC. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ADC falling edge.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ADC is HIGH. At any time during the conversion cycle, $\overline{CS}$ADC may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ADC is LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Independent of $\overline{CS}$ADC, the device automatically enters the sleep state once the conversion is complete. While the device is in the sleep state and $\overline{CS}$ADC is HIGH, the power consumption is reduced an order of magnitude.

While the device is in the sleep state, prior to entering the data output state, the user may program the multiplexer. As shown in Figure 13, the multiplexer channel is selected by serial shifting a 4-bit word into the D_{IN} pin on the rising edge of CLK (CLK is tied to SCK). The first bit is an enable bit that must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the falling edge of $\overline{CS}$MUX, the new channel is selected and will be valid for the first conversion performed following the data output state. Clock signals applied to the CLK pin while $\overline{CS}$MUX is LOW (during the data output state) will have no effect on the channel selection. Furthermore, if D_{IN} is held LOW or CLK is held LOW during the sleep state, the channel selection is unchanged.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ADC is LOW. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on

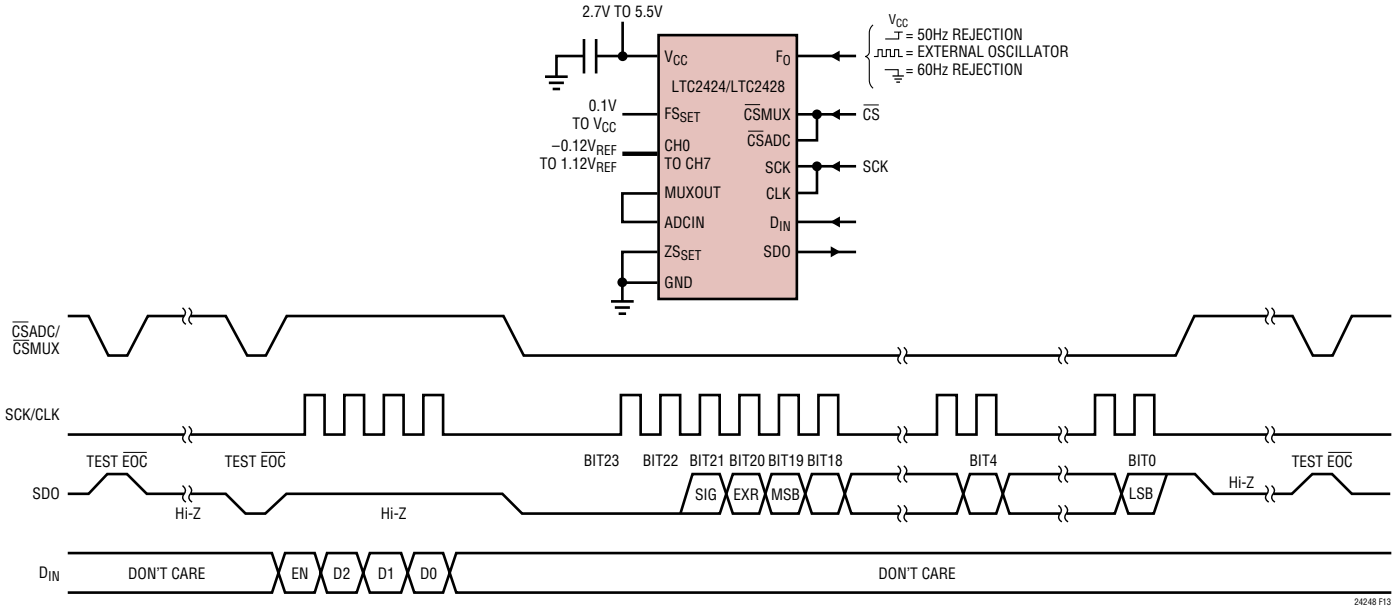

Figure 13. External Serial Clock Timing Diagram

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the 24th rising edge of SCK. On the 24th falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ADC may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ADC may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ADC may be pulled LOW at any time in order to monitor the conversion status. For each of these operations, $\overline{CS}$MUX may be tied to $\overline{CS}$ADC without affecting the selected channel.

At the conclusion of the data output cycle, the converter enters a user transparent calibration cycle prior to actually performing a conversion on the selected input channel. This allows a 66ms (for 60Hz notch frequency) settling time for the multiplexer input. Following the data output cycle, the multiplexer input channel may be selected any time in this 66ms window by pulling $\overline{CS}$ADC HIGH and serial shifting data into the D_{IN} pin, see Figure 14.

While the device is performing the internal calibration, it is sensitive to ground current disturbances. Error currents flowing in the ground pin may lead to offset errors. If the SCK pin is toggling during the calibration, these ground disturbances will occur. The solution is to either drive the multiplexer clock input (CLK) separately from the ADC clock input (SCK), or program the multiplexer in the first 1ms following the data output cycle. The remaining 65ms may be used to allow the input signal to settle.

Typically, $\overline{CS}$ADC remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ADC HIGH anytime between the first rising edge and the 24th falling edge of SCK, see Figure 15. On the rising edge of $\overline{CS}$ADC, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion.

Internal Serial Clock

This timing mode uses an internal serial clock to shift out the conversion result and program the multiplexer, see Figure 16. A $\overline{CS}$ signal directly drives the $\overline{CS}$ADC input, while the inverse of $\overline{CS}$ drives the $\overline{CS}$MUX input. The $\overline{CS}$ signal is used to monitor and control the state of the conversion cycles as well as enable the channel selection. The multiplexer is programmed during the data output state. The internal serial clock (SCK) generated by the ADC is applied to the multiplexer clock input (CLK).

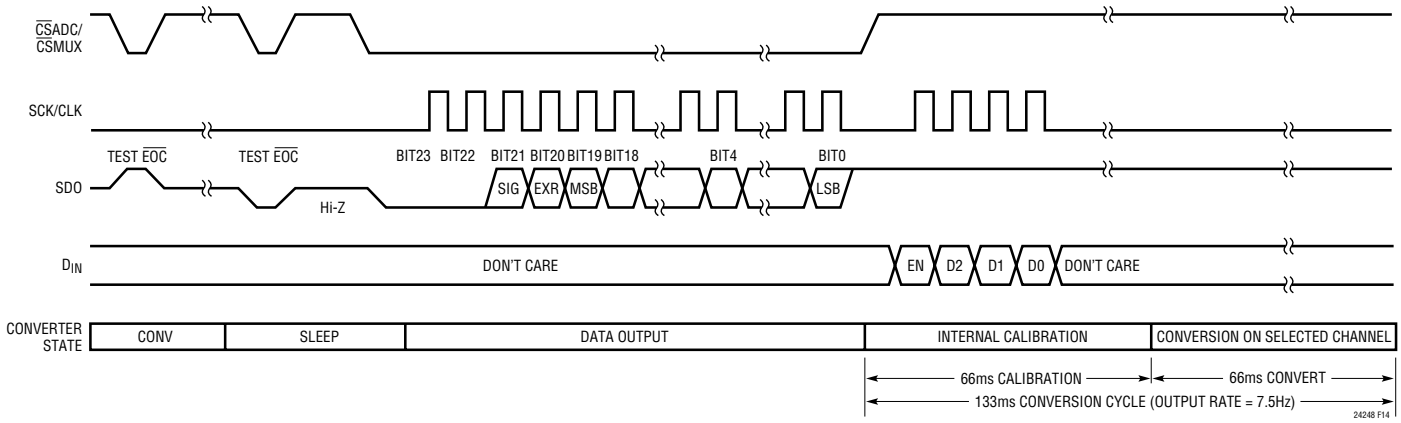

Figure 14. Use of Look Ahead to Program Multiplexer After Data Output

APPLICATIONS INFORMATION

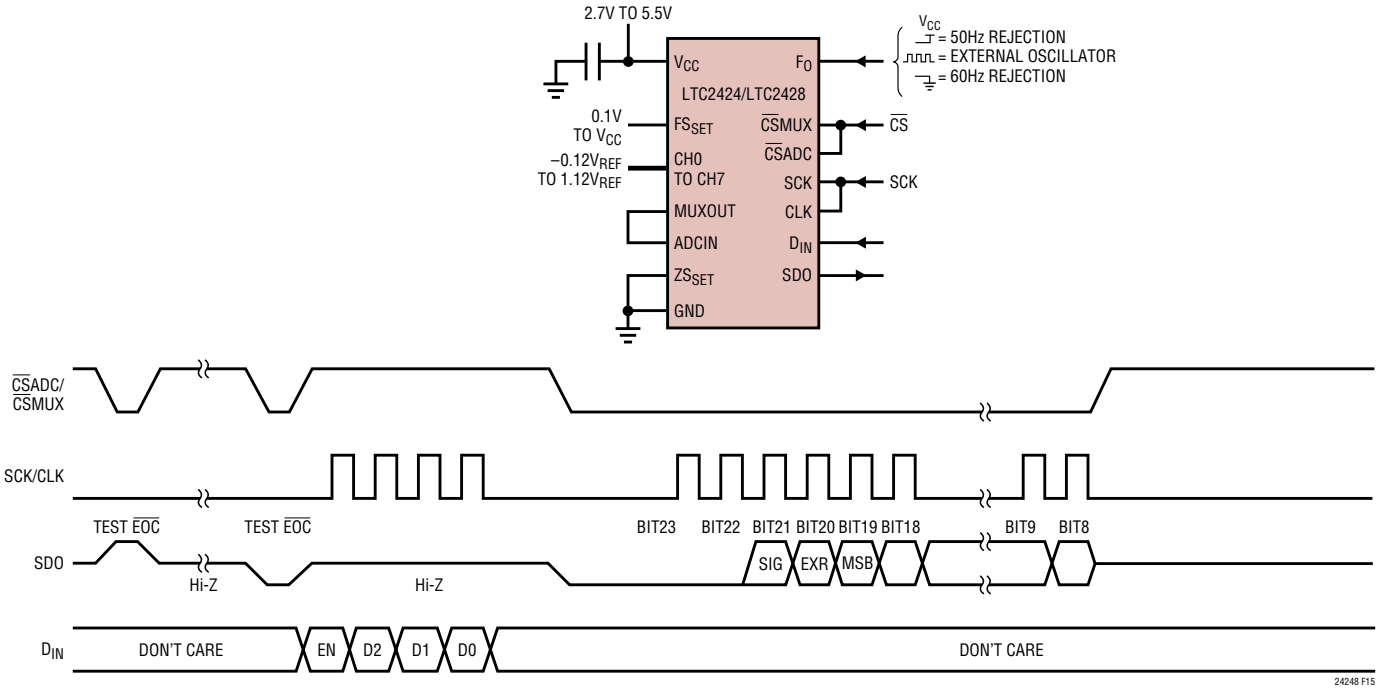

Figure 15. External Serial Clock with Reduced Data Output Length Timing Diagram

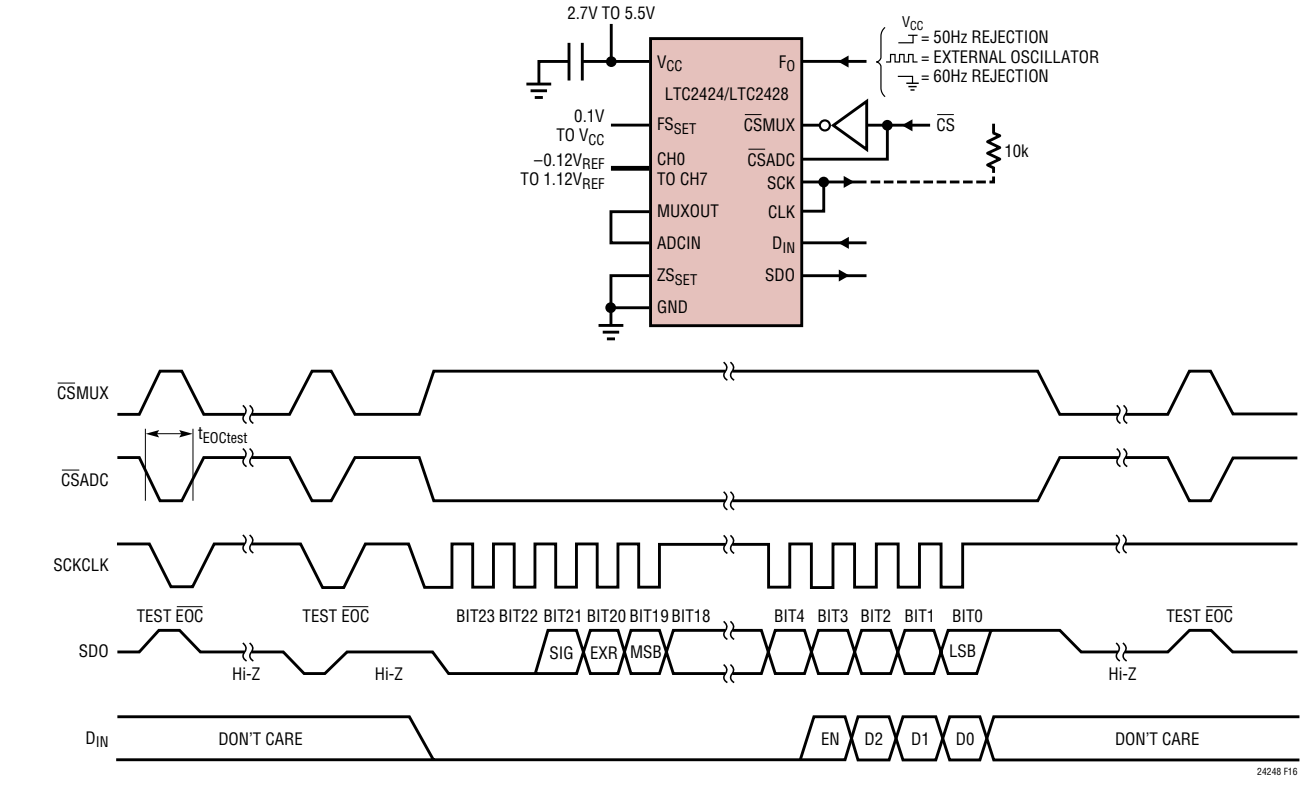

Figure 16. Internal Serial Clock Timing Diagram

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In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$/ADC. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$/ADC. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$/ADC; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$/ADC is HIGH. At any time during the conversion cycle, $\overline{CS}$/ADC may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$/ADC is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$/ADC remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$/ADC must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$/ADC (if EOC = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$/ADC is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator (F_O = logic LOW or HIGH). If F_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$/ADC is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state and the power consumption is reduced an order of magnitude. The conversion result is held in the internal static shift register.

If $\overline{CS}$/ADC remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 24th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 24th rising edge of SCK. After the 24th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH, and a new conversion starts.

While operating in the internal serial clock mode, the SCK output of the ADC may be used as the multiplexer clock (CLK). D_{IN} is latched into the multiplexer on the rising edge of CLK. As shown in Figure 16, the multiplexer channel is selected by serial shifting a 4-bit word into the D_{IN} pin on the rising edge of CLK. The first bit is an enable bit which must be HIGH in order to program a channel. The next three bits determine which channel is selected, see Table 3. On the rising edge of $\overline{CS}$/ADC (falling edge of $\overline{CS}$/MUX), the new channel is selected and will be valid for the next conversion. If D_{IN} is held LOW during the data output state, the previous channel selection remains valid.

Typically, $\overline{CS}$/ADC remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$/ADC HIGH anytime between the first and 24th rising edge of SCK, see Figure 17. On the rising edge of $\overline{CS}$/ADC, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 24 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$/ADC is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$/ADC. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$/ADC HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2424/LTC2428's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2424/LTC2428's internal pull-up remains disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$/ADC, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$/ADC falling edge, the device will remain in the internal SCK timing mode.

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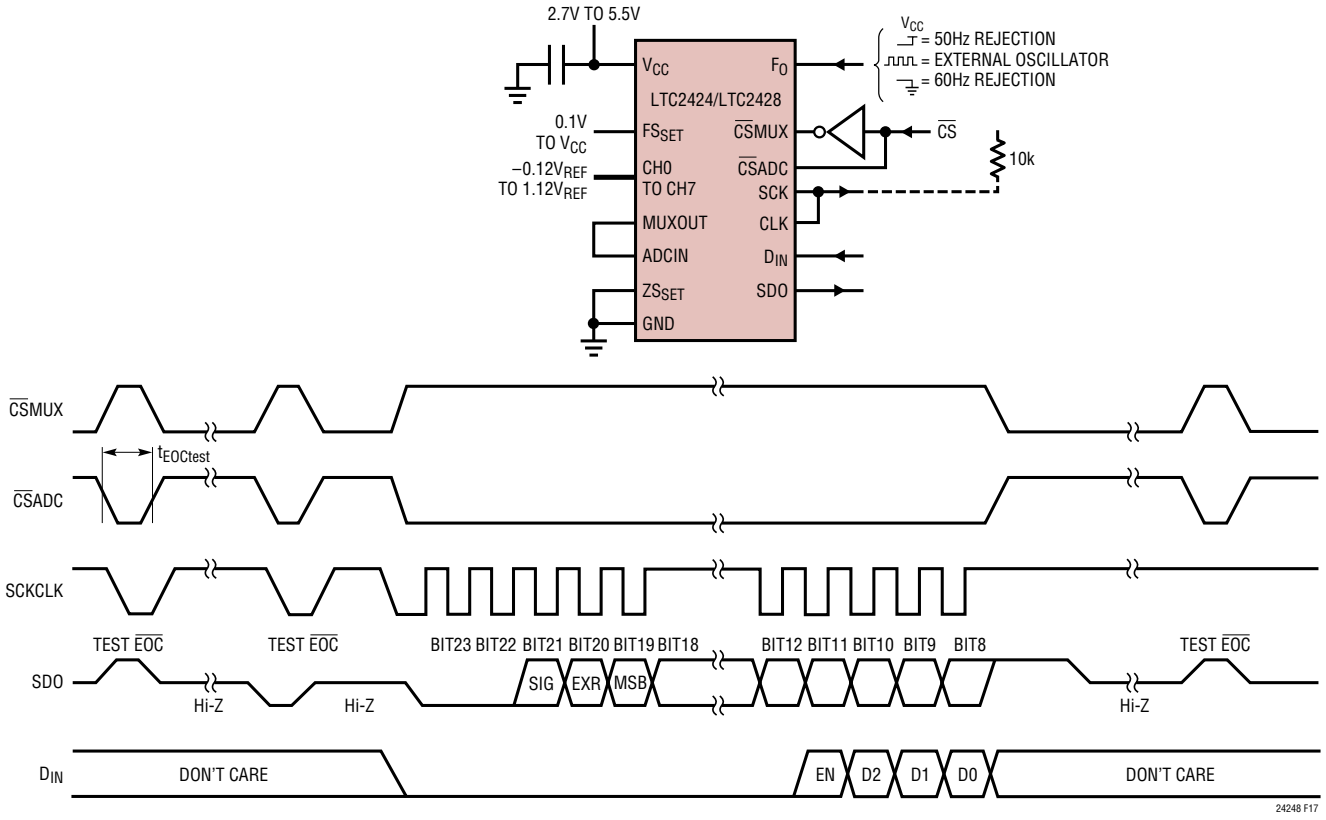

Figure 17. Internal Serial Clock with Reduced Data Output Length Timing Diagram

A similar situation may occur during the sleep state when $\overline{CS}$ADC is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ADC goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ADC goes LOW again. This is not a concern under normal conditions where $\overline{CS}$ADC remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily avoided by adding an external 10k pull-up resistor to the SCK pin.

DIGITAL SIGNAL LEVELS

The LTC2424/LTC2428's digital interface is easy to use. Its digital inputs (F_O, $\overline{CS}$ADC, $\overline{CS}$MUX, CLK, D_{IN} and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of exceptional accuracy and low supply current.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

In order to preserve the accuracy of the LTC2424/LTC2428, it is very important to minimize the ground path impedance which may appear in series with the input and/or reference signal and to reduce the current which may flow through this path. The ZS_{SET} pin (Pin 5) should be connected directly to the signal ground.

The power supply current during the conversion state should be kept to a minimum. This is achieved by restricting the number of digital signal transitions occurring during this period.

APPLICATIONS INFORMATION

While a digital input signal is in the 0.5V to (V_{CC} – 0.5V) range, the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals (F_O, $\overline{CS}$ADC, $\overline{CS}$MUX, D_{IN}, CLK and SCK in External SCK mode of operation) is within this range, the LTC2424/LTC2428 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation and in order to minimize the potential errors due to additional ground pin current, it is recommended to drive all digital input signals to full CMOS levels [V_{IL} < 0.4V and V_{OH} > (V_{CC} – 0.4V)].

Severe ground pin current disturbances can also occur due to the undershoot of fast digital input signals. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2424/LTC2428. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2424/LTC2428 input pins will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver or near the LTC2424/LTC2428 pin will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

Driving the Input and Reference

The analog input and reference of the typical delta-sigma analog-to-digital converter are applied to a switched capacitor network. This network consists of capacitors switching between the analog input (ADCIN), ZS_{SET} (Pin 5) and the reference (FS_{SET}). The result is small current spikes seen at both ADCIN and V_{REF}. A simplified input equivalent circuit is shown in Figure 18.

The key to understanding the effects of this dynamic input current is based on a simple first order RC time constant model. Using the internal oscillator, the internal switched capacitor network of the LTC2424/LTC2428 is clocked at 153,600Hz corresponding to a 6.5µs sampling period. Fourteen time constants are required each time a capacitor is switched in order to achieve 1ppm settling accuracy.

Therefore, the equivalent time constant at V_{IN} and V_{REF} should be less than 6.5µs/14 = 460ns in order to achieve 1ppm accuracy.

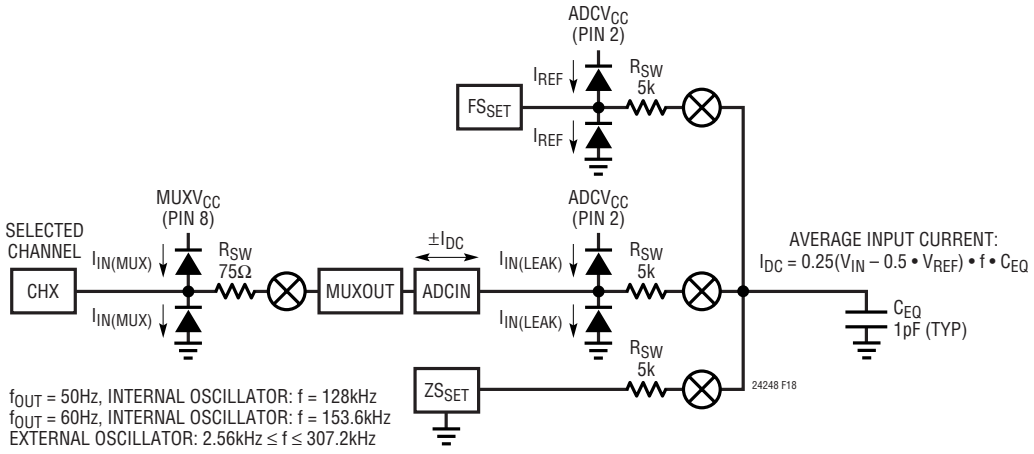

Figure 18. LTC2424/LTC2428 Equivalent Analog Input Circuit