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# Differential Input 16-Bit No Latency ΔΣ ADC

## FEATURES

- **16-Bit Differential ADC in a Tiny MSOP**
- **Low Supply Current: 200μA, 4μA in Autosleep**
- **Rail-to-Rail Differential Input/Reference**
- **0.12LSB INL, No Missing Codes**
- **0.16LSB Full-Scale Error and 5μV Offset**
- **1.45μV RMS Noise, Independent of $V_{REF}$**
- **Very Low Transition Noise: <0.02LSB**
- Operates with a Reference as Low as 100mV with 16-Bit Resolution
- Internal Oscillator—No External Components Required
- 87dB Min, Simultaneous 50Hz and 60Hz Notch Filter
- Single Supply 2.7V to 5.5V Operation
- Pin Compatible with the 20/24-Bit LTC2431/LTC2411
- Available in 10-Lead MSOP Package

## APPLICATIONS

- Direct Sensor Digitizer
- Weight Scales
- Direct Temperature Measurement
- Gas Analyzers
- Strain-Gage Transducers
- Instrumentation
- Data Acquisition
- Industrial Process Control

## DESCRIPTION

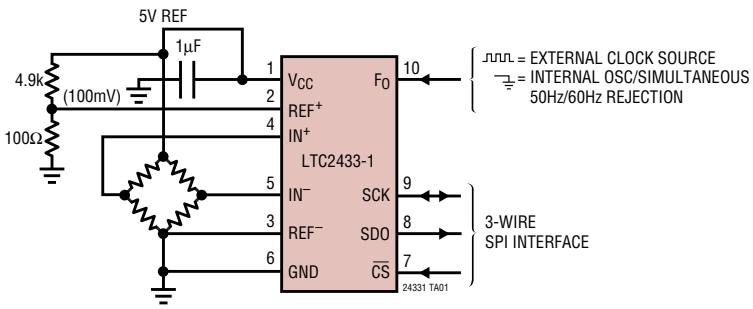
The LTC®2433-1 is a differential input micropower 16-bit No Latency ΔΣ™ analog-to-digital converter with an integrated oscillator. It provides 0.12LSB INL and 1.45μV RMS noise independent of $V_{REF}$. It uses delta-sigma technology and provides single conversion settling of the digital filter. Through a single pin, the LTC2433-1 can be configured for better than 87dB input differential mode rejection at 50Hz and 60Hz ±2%, or it can be driven by an external oscillator for a user defined rejection frequency. The internal oscillator requires no external frequency setting components.

The converter accepts any external differential reference voltage from 0.1V to $V_{CC}$ for flexible ratiometric and remote sensing measurement configurations. The full-scale differential input range is from $-0.5 \cdot V_{REF}$ to $0.5 \cdot V_{REF}$. The reference common mode voltage, $V_{REFCM}$, and the input common mode voltage, $V_{INCM}$, may be independently set anywhere between GND and $V_{CC}$. The DC common mode input rejection is better than 140dB.

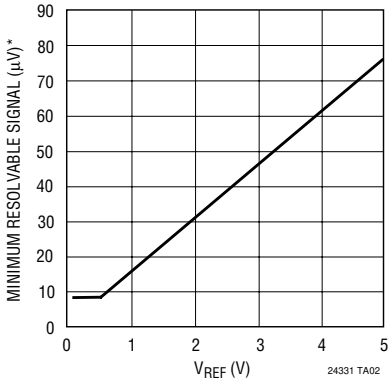
The LTC2433-1 communicates through a flexible 3-wire digital interface which is compatible with SPI and MICROWIRE™ protocols.



## TYPICAL APPLICATION




**Minimum Resolvable Signal vs $V_{REF}$**



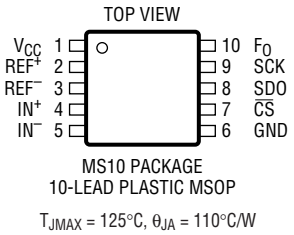

*FOR $V_{REF} \geq 0.5V$ THE RESOLUTION IS LIMITED BY STEP SIZE

## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

Supply Voltage ($V_{CC}$) to GND ..... –0.3V to 7V
Analog Input Voltage
to GND ..... –0.3V to ($V_{CC}$ + 0.3V)
Reference Input Voltage
to GND ..... –0.3V to ($V_{CC}$ + 0.3V)
Digital Input Voltage to GND ..... –0.3V to ($V_{CC}$ + 0.3V)
Digital Output Voltage to GND ..... –0.3V to ($V_{CC}$ + 0.3V)
Operating Temperature Range
LTC2433-1C ..... 0°C to 70°C
LTC2433-1I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

## PACKAGE/ORDER INFORMATION




MS10 PACKAGE
10-LEAD PLASTIC MSOP

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 110°C/W

| ORDER PART NUMBER |
|---|
| LTC2433-1CMS<br>LTC2433-1IMS |
| **MS PART MARKING** |
| LTAEY<br>LTAEZ |

Consult LTC Marketing for parts specified with wider operating temperature ranges.

## ELECTRICAL CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Notes 3, 4, 6)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution (No Missing Codes) | 0.1V ≤ $V_{REF}$ ≤ $V_{CC}$, –0.5 • $V_{REF}$ ≤ $V_{IN}$ ≤ 0.5 • $V_{REF}$, (Note 5) | ● | 16 | | | Bits |
| Integral Nonlinearity (Note 15) | 5V ≤ $V_{CC}$ ≤ 5.5V, $REF^+$ = 2.5V, $REF^-$ = GND, $V_{INCM}$ = 1.25V, (Note 6)<br>5V ≤ $V_{CC}$ ≤ 5.5V, $REF^+$ = 5V, $REF^-$ = GND, $V_{INCM}$ = 2.5V, (Note 6)<br>$REF^+$ = 2.5V, $REF^-$ = GND, $V_{INCM}$ = 1.25V, (Note 6) | <br>●<br> | <br><br> | 0.06<br>0.12<br>0.30 | <br>1.25<br> | LSB<br>LSB<br>LSB |
| Offset Error (Note 15) | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$, (Note 13) | ● | | 5 | 20 | µV |
| Offset Error Drift | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ | | | 20 | | nV/°C |
| Positive Full-Scale Error (Note 15) | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>$IN^+$ = 0.75$REF^+$, $IN^-$ = 0.25 • $REF^+$ | ● | | 0.16 | 1.25 | LSB |
| Positive Full-Scale Error Drift | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>$IN^+$ = 0.75$REF^+$, $IN^-$ = 0.25 • $REF^+$ | | | 0.04 | | ppm of $V_{REF}$/°C |
| Negative Full-Scale Error (Note 15) | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>$IN^+$ = 0.25 • $REF^+$, $IN^-$ = 0.75 • $REF^+$ | ● | | 0.16 | 1.25 | LSB |
| Negative Full-Scale Error Drift | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND,<br>$IN^+$ = 0.25 • $REF^+$, $IN^-$ = 0.75 • $REF^+$ | | | 0.04 | | ppm of $V_{REF}$/°C |
| Total Unadjusted Error | 5V ≤ $V_{CC}$ ≤ 5.5V, $REF^+$ = 2.5V, $REF^-$ = GND, $V_{INCM}$ = 1.25V<br>5V ≤ $V_{CC}$ ≤ 5.5V, $REF^+$ = 5V, $REF^-$ = GND, $V_{INCM}$ = 2.5V<br>$REF^+$ = 2.5V, $REF^-$ = GND, $V_{INCM}$ = 1.25V, (Note 6) | | | 0.20<br>0.20<br>0.25 | | LSB<br>LSB<br>LSB |
| Output Noise | 5V ≤ $V_{CC}$ ≤ 5.5V, $REF^+$ = 5V, $REF^-$ = GND,<br>GND ≤ $IN^-$ = $IN^+$ ≤ $V_{CC}$, (Note 12) | | | 1.45 | | $\mu V_{RMS}$ |

## CONVERTER CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Notes 3, 4)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Common Mode Rejection DC | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND, GND ≤ $IN^-$ = $IN^+$ ≤ $V_{CC}$ (Note 5) | ● | 130 | 140 | | dB |
| Input Common Mode Rejection 49Hz to 61.2Hz | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, $REF^-$ = GND, GND ≤ $IN^-$ = $IN^+$ ≤ $V_{CC}$, (Notes 5, 7) | ● | 140 | | | dB |
| Input Normal Mode Rejection 49Hz to 61.2Hz | (Note 5, 7) | ● | 87 | | | dB |
| Reference Common Mode Rejection DC | 2.5V ≤ $REF^+$ ≤ $V_{CC}$, GND ≤ $REF^-$ ≤ 2.5V, $V_{REF}$ = 2.5V, $IN^-$ = $IN^+$ = GND (Note 5) | ● | 130 | 140 | | dB |
| Power Supply Rejection, DC | $REF^+$ = 2.5V, $REF^-$ = GND, $IN^-$ = $IN^+$ = GND | | | 120 | | dB |
| Power Supply Rejection, Simultaneous 50Hz/60Hz ±2% | $REF^+$ = 2.5V, $REF^-$ = GND, $IN^-$ = $IN^+$ = GND, (Note 7) | | | 120 | | dB |

## ANALOG INPUT AND REFERENCE

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $IN^+$ | Absolute/Common Mode $IN^+$ Voltage | | ● | GND – 0.3 | | $V_{CC}$ + 0.3 | V |
| $IN^-$ | Absolute/Common Mode $IN^-$ Voltage | | ● | GND – 0.3 | | $V_{CC}$ + 0.3 | V |
| $V_{IN}$ | Input Differential Voltage Range ($IN^+$ – $IN^-$) | | ● | $-V_{REF}/2$ | | $V_{REF}/2$ | V |
| $REF^+$ | Absolute/Common Mode $REF^+$ Voltage | | ● | 0.1 | | $V_{CC}$ | V |
| $REF^-$ | Absolute/Common Mode $REF^-$ Voltage | | ● | GND | | $V_{CC}$ – 0.1 | V |
| $V_{REF}$ | Reference Differential Voltage Range ($REF^+$ – $REF^-$) | | ● | 0.1 | | $V_{CC}$ | V |
| $C_S$ ($IN^+$) | $IN^+$ Sampling Capacitance | | | | 6 | | pF |
| $C_S$ ($IN^-$) | $IN^-$ Sampling Capacitance | | | | 6 | | pF |
| $C_S$ ($REF^+$) | $REF^+$ Sampling Capacitance | | | | 6 | | pF |
| $C_S$ ($REF^-$) | $REF^-$ Sampling Capacitance | | | | 6 | | pF |
| $I_{DC\_LEAK}$ ($IN^+$) | $IN^+$ DC Leakage Current | $\overline{CS}$ = $V_{CC}$ = 5V, $IN^+$ = GND | ● | –100 | 1 | 100 | nA |
| $I_{DC\_LEAK}$ ($IN^-$) | $IN^-$ DC Leakage Current | $\overline{CS}$ = $V_{CC}$ = 5V, $IN^-$ = 5.5V | ● | –100 | 1 | 100 | nA |
| $I_{DC\_LEAK}$ ($REF^+$) | $REF^+$ DC Leakage Current | $\overline{CS}$ = $V_{CC}$ = 5V, $REF^+$ = 5.5V | ● | –100 | 1 | 100 | nA |
| $I_{DC\_LEAK}$ ($REF^-$) | $REF^-$ DC Leakage Current | $\overline{CS}$ = $V_{CC}$ = 5V, $REF^-$ = GND | ● | –100 | 1 | 100 | nA |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage<br>$\overline{CS}$, $F_O$ | 2.7V ≤ $V_{CC}$ ≤ 5.5V<br>2.7V ≤ $V_{CC}$ ≤ 3.3V | ●<br>● | 2.5<br>2.0 | | | V<br>V |
| $V_{IL}$ | Low Level Input Voltage<br>$\overline{CS}$, $F_O$ | 4.5V ≤ $V_{CC}$ ≤ 5.5V<br>2.7V ≤ $V_{CC}$ ≤ 5.5V | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $V_{IH}$ | High Level Input Voltage<br>SCK | 2.7V ≤ $V_{CC}$ ≤ 5.5V (Note 8)<br>2.7V ≤ $V_{CC}$ ≤ 3.3V (Note 8) | ●<br>● | 2.5<br>2.0 | | | V<br>V |
| $V_{IL}$ | Low Level Input Voltage<br>SCK | 4.5V ≤ $V_{CC}$ ≤ 5.5V (Note 8)<br>2.7V ≤ $V_{CC}$ ≤ 5.5V (Note 8) | ●<br>● | | | 0.8<br>0.6 | V<br>V |
| $I_{IN}$ | Digital Input Current<br>$\overline{CS}$, $F_O$ | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | ● | –10 | | 10 | µA |
| $I_{IN}$ | Digital Input Current<br>SCK | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ (Note 8) | ● | –10 | | 10 | µA |
| $C_{IN}$ | Digital Input Capacitance<br>$\overline{CS}$, $F_O$ | | | | 10 | | pF |
| $C_{IN}$ | Digital Input Capacitance<br>SCK | (Note 8) | | | 10 | | pF |
| $V_{OH}$ | High Level Output Voltage<br>SDO | $I_O$ = –800µA | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{OL}$ | Low Level Output Voltage<br>SDO | $I_O$ = 1.6mA | ● | | | 0.4 | V |
| $V_{OH}$ | High Level Output Voltage<br>SCK | $I_O$ = –800µA (Note 9) | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{OL}$ | Low Level Output Voltage<br>SCK | $I_O$ = 1.6mA (Note 9) | ● | | | 0.4 | V |
| $I_{OZ}$ | Hi-Z Output Leakage<br>SDO | | ● | –10 | | 10 | µA |

## POWER REQUIREMENTS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current<br>Conversion Mode<br>Sleep Mode<br>Sleep Mode | <br>$\overline{CS}$ = 0V (Note 14)<br>$\overline{CS}$ = $V_{CC}$ (Notes 11, 14)<br>$\overline{CS}$ = $V_{CC}$, 2.7V ≤ $V_{CC}$ ≤ 3.3V (Notes 11, 14) | <br>●<br>●<br> | | <br>200<br>4<br>2 | <br>300<br>13<br> | <br>µA<br>µA<br>µA |

## TIMING CHARACTERISTICS

**The ● denotes specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{EOSC}$ | External Oscillator Frequency Range | | ● | 2.56 | | 2000 | kHz |
| $t_{HEO}$ | External Oscillator High Period | | ● | 0.25 | | 390 | µs |
| $t_{LEO}$ | External Oscillator Low Period | | ● | 0.25 | | 390 | µs |
| $t_{CONV}$ | Conversion Time | $F_O$ = 0V<br>External Oscillator (Note 10) | ●<br>● | 143.8<br>20510/$f_{EOSC}$ (in kHz) | 146.7 | 149.6 | ms<br>ms |
| $f_{ISCK}$ | Internal SCK Frequency | Internal Oscillator (Note 9)<br>External Oscillator (Notes 9, 10) | | | 17.5<br>$f_{EOSC}$/8 | | kHz<br>kHz |
| $D_{ISCK}$ | Internal SCK Duty Cycle | (Note 9) | ● | 45 | | 55 | % |
| $f_{ESCK}$ | External SCK Frequency Range | (Note 8) | ● | | | 2000 | kHz |
| $t_{LESCK}$ | External SCK Low Period | (Note 8) | ● | 250 | | | ns |
| $t_{HESCK}$ | External SCK High Period | (Note 8) | ● | 250 | | | ns |
| $t_{DOUT\_ISCK}$ | Internal SCK 19-Bit Data Output Time | Internal Oscillator (Notes 9, 11)<br>External Oscillator (Notes 9, 10) | ●<br>● | 1.06<br>152/$f_{EOSC}$ (in kHz) | 1.09 | 1.11 | ms<br>ms |
| $t_{DOUT\_ESCK}$ | External SCK 19-Bit Data Output Time | (Note 8) | ● | 19/$f_{ESCK}$ (in kHz) | | | ms |
| $t_1$ | $\overline{CS}$ ↓ to SDO Low Z | | ● | 0 | | 200 | ns |
| t2 | $\overline{CS}$ ↑ to SDO High Z | | ● | 0 | | 200 | ns |
| t3 | $\overline{CS}$ ↓ to SCK ↓ | (Note 9) | ● | 0 | | 200 | ns |
| t4 | $\overline{CS}$ ↓ to SCK ↑ | (Note 8) | ● | 50 | | | ns |
| $t_{KQMAX}$ | SCK ↓ to SDO Valid | | ● | | | 220 | ns |
| $t_{KQMIN}$ | SDO Hold After SCK ↓ | (Note 5) | ● | 15 | | | ns |
| $t_5$ | SCK Set-Up Before $\overline{CS}$ ↓ | | ● | 50 | | | ns |
| $t_6$ | SCK Hold After $\overline{CS}$ ↓ | | ● | | | 50 | ns |

**Note 1:** Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** $V_{CC}$ = 2.7V to 5.5V unless otherwise specified.
$V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$; $V_{IN} = IN^+ – IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

**Note 4:** $F_O$ pin tied to GND or to an external conversion clock source with $f_{EOSC}$ = 139,800Hz unless otherwise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a precise analog input voltage. Maximum specifications are limited by the LSB step size ($V_{REF}/2^{16}$) and the single shot measurement. Typical specifications are measured from the center of the quantization band.

**Note 7:** $F_O$ = GND (internal oscillator) or $f_{EOSC}$ = 139,800Hz ±2% (external oscillator).

**Note 8:** The converter is in external SCK mode of operation such that the SCK pin is used as digital input. The frequency of the clock signal driving SCK during the data output is $f_{ESCK}$ and is expressed in kHz.

**Note 9:** The converter is in internal SCK mode of operation such that the SCK pin is used as digital output. In this mode of operation the SCK pin has a total equivalent load capacitance $C_{LOAD}$ = 20pF.

**Note 10:** The external oscillator is connected to the $F_O$ pin. The external oscillator frequency, $f_{EOSC}$, is expressed in kHz.

**Note 11:** The converter uses the internal oscillator.
$F_O$ = 0V.

**Note 12:** 1.45µV RMS noise is independent of $V_{REF}$. Since the noise performance is limited by the quantization, lowering $V_{REF}$ improves the effective resolution.

**Note 13:** Guaranteed by design and test correlation.

**Note 14:** The low sleep mode current is valid only when $\overline{CS}$ is high.

**Note 15:** These parameters are guaranteed by design over the full supply and temperature range. Automated testing procedures are limited by the LSB step size ($V_{REF}$/65,536).

## PIN FUNCTIONS

**$V_{CC}$ (Pin 1):** Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with 0.1µF ceramic capacitor as close to the part as possible.

**$REF^+$ (Pin 2), $REF^-$ (Pin 3):** Differential Reference Input. The voltage on these pins can have any value between GND and $V_{CC}$ as long as the reference positive input, $REF^+$, is maintained more positive than the reference negative input, $REF^-$, by at least 0.1V.

**$IN^+$ (Pin 4), $IN^-$ (Pin 5):** Differential Analog Input. The voltage on these analog inputs can have any value between GND and $V_{CC}$. Within these limits the converter bipolar input range ($V_{IN} = IN^+ – IN^–$) extends from $–0.5 • (V_{REF})$ to $0.5 • (V_{REF})$. Outside this input range the converter produces unique overrange and underrange output codes.

**GND (Pin 6):** Ground. Connect this pin to a ground plane through a low impedance connection.

**$\overline{CS}$ (Pin 7):** Active LOW Digital Input. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output transfer aborts the data transfer and starts a new conversion.

**SDO (Pin 8):** Three-State Digital Output. During the Data Output period, this pin is used as serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the Conversion and Sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW.

**SCK (Pin 9):** Bidirectional Digital Clock Pin. In Internal Serial Clock Operation mode, SCK is used as digital output for the internal serial interface clock during the Data Output period. In External Serial Clock Operation mode, SCK is used as digital input for the external serial interface clock during the Data Output period. A weak internal pull-up is automatically activated in Internal Serial Clock Operation mode. The Serial Clock Operation mode is determined by the logic level applied to the SCK pin at power up or during the most recent falling edge of $\overline{CS}$.

**$F_O$ (Pin 10):** Frequency Control Pin. Digital input that controls the ADC's notch frequencies and conversion time. When the $F_O$ pin is connected to GND ($F_O = 0V$), the converter uses its internal oscillator and rejects 50Hz and 60Hz simultaneously. When $F_O$ is driven by an external clock signal with a frequency $f_{EOSC}$, the converter uses this signal as its system clock and the digital filter has 87dB minimum rejection in the range $f_{EOSC}/2560$ ±14% and 110dB minimum rejection at $f_{EOSC}/2560$ ±4%.

## FUNCTIONAL DIAGRAM

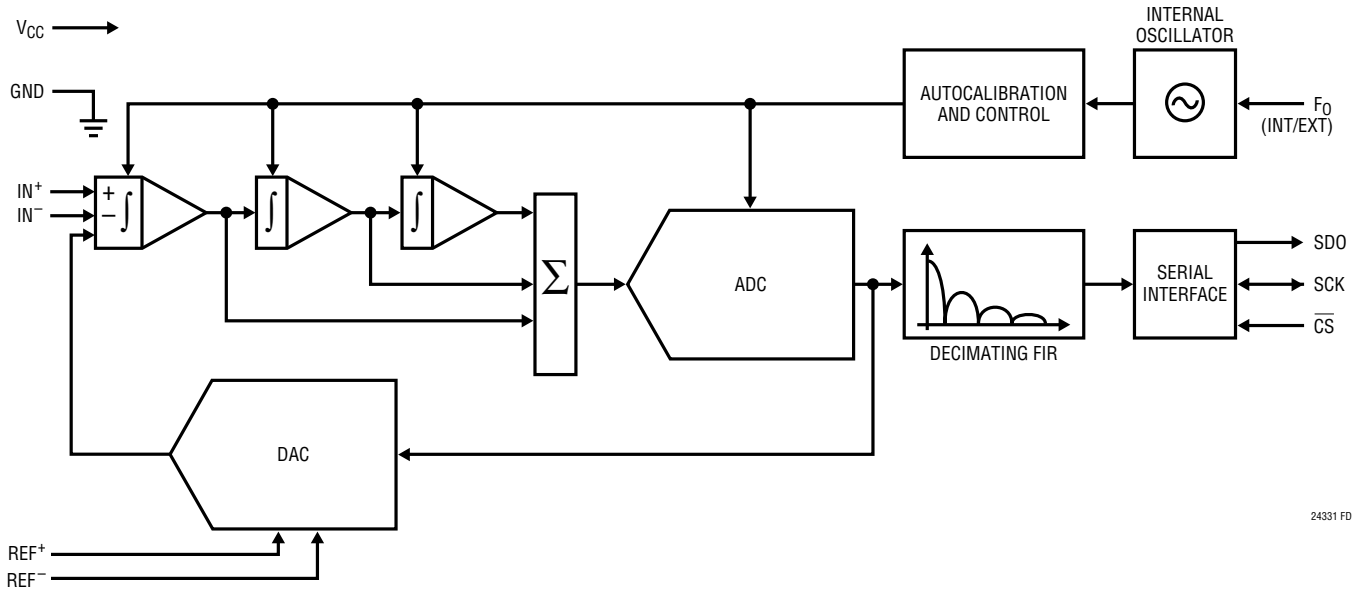
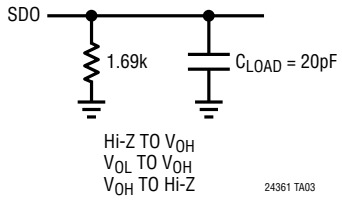
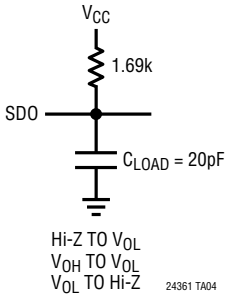



**Figure 1. Functional Block Diagram**

## TEST CIRCUITS



# APPLICATIONS INFORMATION

## CONVERTER OPERATION

### Converter Operation Cycle

The LTC2433-1 is a low power, ΔΣ ADC with differential input/reference and an easy-to-use 3-wire serial interface (see Figure 1). Its operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output (see Figure 2). The 3-wire interface consists of serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$).

Initially, the LTC2433-1 performs a conversion. Once the conversion is complete, the device enters the sleep state. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. While in this sleep state, power consumption is reduced by nearly two orders of magnitude. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device exits the low power mode and enters the data output state. If $\overline{CS}$ is pulled HIGH before the first rising edge of SCK, the device returns to the low power sleep mode and the conversion result is still held in the internal static shift register. If $\overline{CS}$ remains LOW after the first rising edge of SCK, the device begins outputting the conversion result. Taking $\overline{CS}$ high at this point will terminate the data output state and start a new conversion. There is no latency in the conversion result. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 19 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats. In order to maintain compatibility with 24-/32-bit data transfers, it is possible to clock the LTC2433-1 with additional serial clock pulses. This results in additional data bits which are logic HIGH.

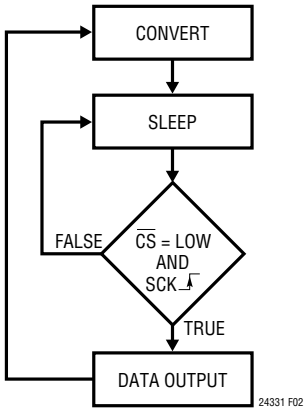



**Figure 2. LTC2433-1 State Transition Diagram**

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2433-1 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

### Conversion Clock

A major advantage the delta-sigma converter offers over conventional type converters is an on-chip digital filter (commonly implemented as a Sinc or Comb filter). For high resolution, low frequency applications, this filter is typically designed to reject line frequencies of 50Hz and 60Hz plus their harmonics. The filter rejection performance is directly related to the accuracy of the converter system clock. The LTC2433-1 incorporates a highly accurate on-chip oscillator. This eliminates the need for external frequency setting components such as crystals or oscillators. Clocked by the on-chip oscillator, the LTC2433-1 achieves a minimum of 87dB rejection over the range 49Hz to 61.2Hz.

### Ease of Use

The LTC2433-1 data output has no latency, filter settling delay or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages is easy.

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The LTC2433-1 performs offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

### Power-Up Sequence

The LTC2433-1 automatically enters an internal reset state when the power supply voltage $V_{CC}$ drops below approximately 2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection. (See the 2-wire I/O sections in the Serial Interface Timing Modes section.)

When the $V_{CC}$ voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a typical duration of 1ms. The POR signal clears all internal registers. Following the POR signal, the LTC2433-1 starts a normal conversion cycle and follows the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (2.7V to 5.5V) before the end of the POR time interval.

### Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage specification for the $REF^+$ and $REF^-$ pins covers the entire range from GND to $V_{CC}$. For correct converter operation, the $REF^+$ pin must always be more positive than the $REF^-$ pin.

The LTC2433-1 can accept a differential reference voltage from 0.1V to $V_{CC}$. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will significantly improve the converter's effective resolution, since the thermal noise (1.45µV) is well below the quantization level of the device (75.6µV for a 5V reference). At the minimum reference (100mV) the thermal noise remains constant at 1.45µV RMS (or $8.7\mu V_{P-P}$), while the quantization is reduced to 1.5µV per LSB. As a result, lowering the reference improves the effective resolution for low level input voltages.

### Input Voltage Range

The analog input is truly differential with an absolute/common mode range for the $IN^+$ and $IN^-$ input pins extending from GND – 0.3V to $V_{CC}$ + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2433-1 converts the bipolar differential input signal, $V_{IN} = IN^+ – IN^-$, from $–FS = –0.5 \bullet V_{REF}$ to $+FS = 0.5 \bullet V_{REF}$ where $V_{REF} = REF^+ – REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

Input signals applied to the analog input pins may extend by 300mV below ground and above $V_{CC}$. In order to limit any fault current, resistors of up to 5k may be added in series with the pins without affecting the performance of the device. In the physical layout, it is important to maintain the parasitic capacitance of the connection between these series resistors and the corresponding pins as low as possible; therefore, the resistors should be located as close as practical to the pins. The effect of the series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent offset error due to the input leakage current. A 10nA input leakage current will develop a 1LSB offset error on an 8k resistor if $V_{REF}$ = 5V. This error has a very strong temperature dependency.

### Output Data Format

The LTC2433-1 serial output data stream is 19 bits long. The first 3 bits represent status information indicating the conversion state and sign. The next 16 bits are the conversion result, MSB first. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

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Bit 18 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 17 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 16 (third output bit) is the conversion result sign indicator (SIG). If $V_{IN}$ is >0, this bit is HIGH. If $V_{IN}$ is <0, this bit is LOW.

Bit 15 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 16 also provides the underrange or overrange indication. If both Bit 16 and Bit 15 are HIGH, the differential input voltage is above +FS. If both Bit 16 and Bit 15 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

**Table 1. LTC2433-1 Status Bits**

| Input Range | Bit 18 $\overline{EOC}$ | Bit 17 DMY | Bit 16 SIG | Bit 15 MSB |
|---|---|---|---|---|
| $V_{IN} \geq 0.5 \cdot V_{REF}$ | 0 | 0 | 1 | 1 |
| $0V \leq V_{IN} < 0.5 \cdot V_{REF}$ | 0 | 0 | 1 | 0 |
| $-0.5 \cdot V_{REF} \leq V_{IN} < 0V$ | 0 | 0 | 0 | 1 |
| $V_{IN} < -0.5 \cdot V_{REF}$ | 0 | 0 | 0 | 0 |

Bits 15-0 are the 16-Bit conversion result MSB first.

Bit 0 is the least significant bit (LSB).

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and any externally generated SCK clock pulses are ignored by the internal data out shift register.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 18 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 17 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the falling edge of the 18th SCK and may be latched on the rising edge of the 19th SCK pulse. On the falling edge of the 19th SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 18) for the next conversion cycle. Table 2 summarizes the output data format.

In order to remain compatible with some SPI microcontrollers, more than 19 SCK clock pulses may be applied. As long as these clock edges are complete before the conversion ends, they will not effect the serial data. However, switching SCK during a conversion may generate ground currents in the device leading to extra offset and noise error sources.

As long as the voltage on the analog input pins is maintained within the –0.3V to ($V_{CC}$ + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage $V_{IN}$ from –FS = –0.5 • $V_{REF}$ to +FS = 0.5 • $V_{REF}$. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

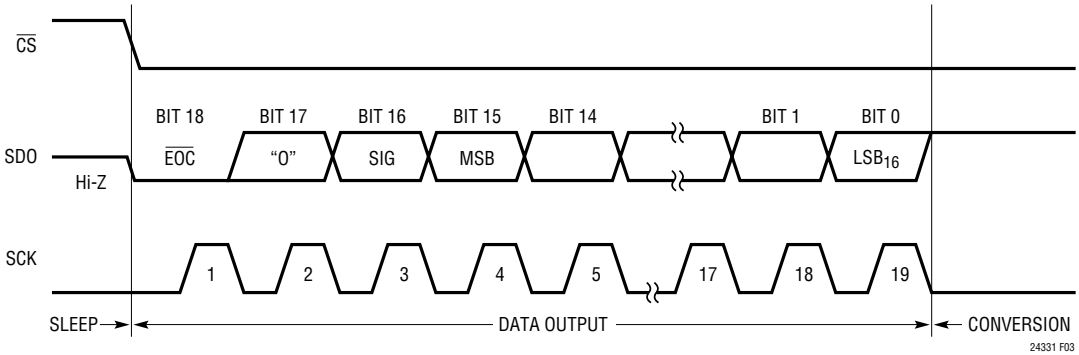


**Figure 3. Output Data Timing**

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**Table 2. LTC2433-1 Output Data Format**

| Differential Input Voltage $V_{IN}$* | Bit 18 $\overline{EOC}$ | Bit 17 DMY | Bit 16 SIG | Bit 15 MSB | Bit 14 | Bit 13 | Bit 12 | … | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| $V_{IN}$* ≥ 0.5 • $V_{REF}$** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | … | 0 |
| 0.5 • $V_{REF}$** – 1LSB | 0 | 0 | 1 | 0 | 1 | 1 | 1 | … | 1 |
| 0.25 • $V_{REF}$** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | … | 0 |
| 0.25 • $V_{REF}$** – 1LSB | 0 | 0 | 1 | 0 | 0 | 1 | 1 | … | 1 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | … | 0 |
| –1LSB | 0 | 0 | 0 | 1 | 1 | 1 | 1 | … | 1 |
| –0.25 • $V_{REF}$** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | … | 0 |
| –0.25 • $V_{REF}$** – 1LSB | 0 | 0 | 0 | 1 | 0 | 1 | 1 | … | 1 |
| –0.5 • $V_{REF}$** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | … | 0 |
| $V_{IN}$* < –0.5 • $V_{REF}$** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | … | 1 |

*The differential input voltage $V_{IN} = IN^+ – IN^–$.

**The differential reference voltage $V_{REF} = REF^+ – REF^–$.

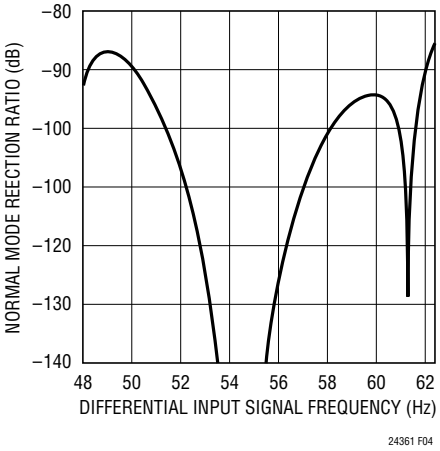


**Figure 4. LTC2433-1 Normal Mode Rejection When Using an Internal Oscillator**

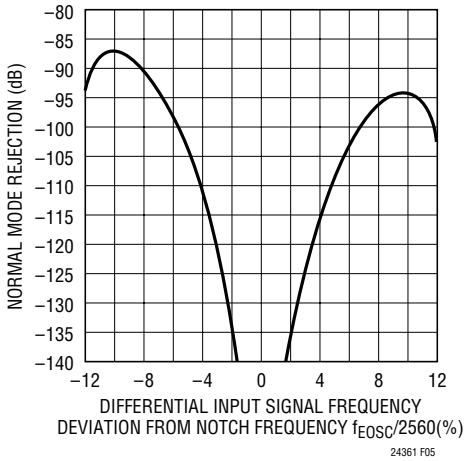


**Figure 5. LTC2433-1 Normal Mode Rejection When Using an External Oscillator of Frequency $f_{EOSC}$**

### Simultaneous Frequency Rejection

The LTC2433-1 internal oscillator provides better than 87dB normal mode rejection over the range of 49Hz to 61.2Hz as shown in Figure 4. For this simultaneous 50Hz/60Hz rejection, $F_O$ should be connected to GND.

When a fundamental rejection frequency different from the range 49Hz to 61.2Hz is required or when the converter must be sychronized with an outside source, the LTC2433-1 can operate with an external conversion clock. The conveter automatically detects the presence of an external clock signal at the $F_O$ pin and turns off the internal oscillator. The frequency $f_{EOSC}$ of the external signal must be at least 2560Hz to be detected. The external clock signal duty cycle is not significant as long as the minimum and maximum specifications for the high and low periods, $t_{HEO}$ and $t_{LEO}$, are observed.

While operating with an external conversion clock of a frequency $f_{EOSC}$, the LTC2433-1 provides better than 110dB normal mode rejection in a frequency range $f_{EOSC}/2560$ ±4%. The normal mode rejection as a function of the input frequency deviation from $f_{EOSC}/2560$ is shown in Figure 5.

Whenever an external clock is not present at the $F_O$ pin the converter automatically activates its internal oscillator and enters the Internal Conversion Clock mode. The LTC2433-1

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operation will not be disturbed if the change of conversion clock source occurs during the sleep state or during the data output state while the converter uses an external serial clock. If the change occurs during the conversion state, the result of the conversion in progress may be outside specifications but the following conversions will not be affected. If the change occurs during the data output state and the converter is in the Internal SCK mode, the serial clock duty cycle may be affected but the serial data stream will remain valid.

Table 3 summarizes the duration of each state and the achievable output data rate as a function of $F_O$.

### SERIAL INTERFACE PINS

The LTC2433-1 transmits the conversion results and receives the start of conversion command through a synchronous 3-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result.

### Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 9) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2433-1 creates its own serial clock by dividing the internal conversion clock by 8. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected on power-up and then reselected every time a HIGH-to-LOW transition is detected at the $\overline{CS}$ pin. If SCK is HIGH or floating at power-up or during this transition, the converter enters the internal SCK mode. If SCK is LOW at power-up or during this transition, the converter enters the external SCK mode.

### Serial Data Output (SDO)

The serial data output pin, SDO (Pin 8), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 7) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW.

### Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 7), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

**Table 3. LTC2433-1 State Duration**

| State | Operating Mode | | Duration |
|---|---|---|---|
| CONVERT | Internal Oscillator | $F_O$ = LOW<br>Simultaneous 50Hz/60Hz Rejection | 147ms, Output Data Rate ≤ 6.8 Readings/s |
| | External Oscillator | $F_O$ = External Oscillator<br>with Frequency $f_{EOSC}$ kHz<br>($f_{EOSC}$/2560 Rejection) | 20510/$f_{EOSC}$s, Output Data Rate ≤ $f_{EOSC}$/20510 Readings/s |
| SLEEP | | | As Long As $\overline{CS}$ = HIGH Until $\overline{CS}$ = LOW and SCK ↓ |
| DATA OUTPUT | Internal Serial Clock | $F_O$ = LOW<br>(Internal Oscillator) | As Long As $\overline{CS}$ = LOW But Not Longer Than 1.09ms<br>(19 SCK cycles) |
| | | $F_O$ = External Oscillator with<br>Frequency $f_{EOSC}$ kHz | As Long As $\overline{CS}$ = LOW But Not Longer Than 152/$f_{EOSC}$ms<br>(19 SCK cycles) |
| | External Serial Clock with<br>Frequency $f_{SCK}$ kHz | | As Long As $\overline{CS}$ = LOW But Not Longer Than 19/$f_{SCK}$ms<br>(19 SCK cycles) |

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In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2433-1 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state (i.e., after the first rising edge of SCK occurs with $\overline{CS}$ = LOW).

Finally, $\overline{CS}$ can be used to control the free-running modes of operation, see Serial Interface Timing Modes section. Grounding $\overline{CS}$ will force the ADC to continuously convert at the maximum output rate selected by $F_O$.

### SERIAL INTERFACE TIMING MODES

The LTC2433-1's 3-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 2- or 3-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator ($F_O$ = LOW) or an external oscillator connected to the $F_O$ pin. Refer to Table 4 for a summary.

### External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 6.

The serial clock mode is selected on the falling edge of $\overline{CS}$. To select the external serial clock mode, the serial clock pin (SCK) must be LOW during each $\overline{CS}$ falling edge.

**Table 4. LTC2433-1 Interface Timing Modes**

| Configuration | SCK Source | Conversion Cycle Control | Data Output Control | Connection and Waveforms |
|---|---|---|---|---|
| External SCK, Single Cycle Conversion | External | $\overline{CS}$ and SCK | $\overline{CS}$ and SCK | Figures 6, 7 |
| External SCK, 2-Wire I/O | External | SCK | SCK | Figure 8 |
| Internal SCK, Single Cycle Conversion | Internal | $\overline{CS}\downarrow$ | $\overline{CS}\downarrow$ | Figures 9, 10 |
| Internal SCK, 2-Wire I/O, Continuous Conversion | Internal | Continuous | Internal | Figure 11 |

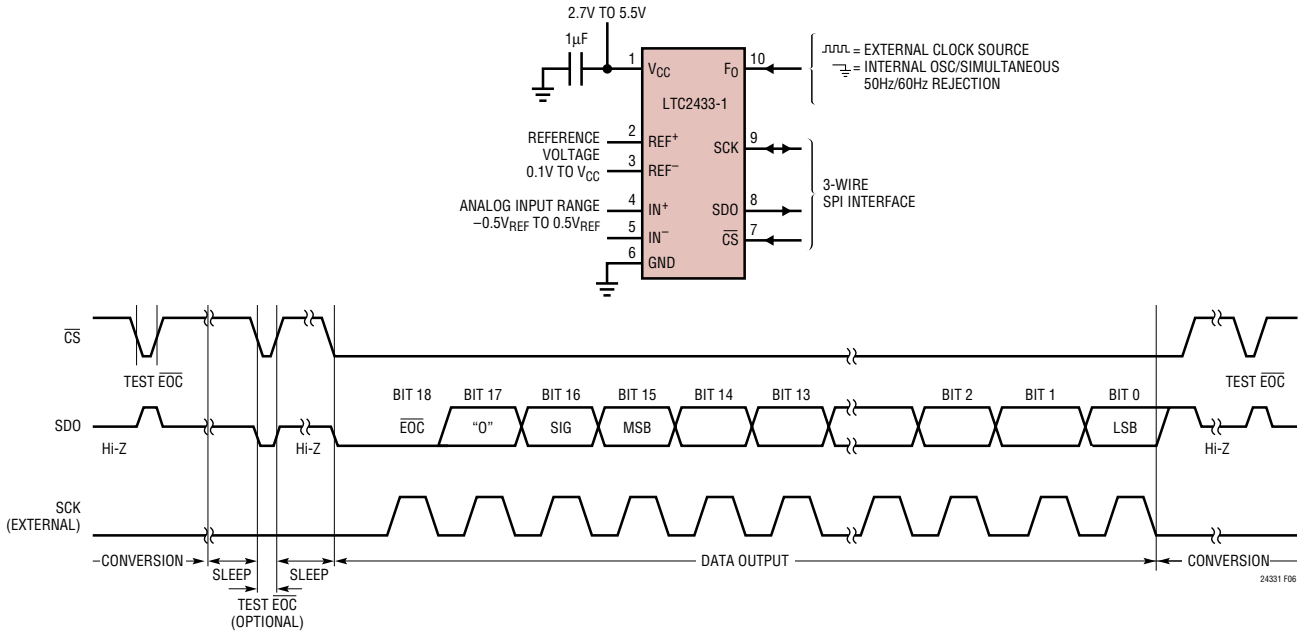


**Figure 6. External Serial Clock, Single Cycle Operation**

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The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. With $\overline{CS}$ high, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 19th rising edge of SCK. On the 19th falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z. As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first rising edge and the 19th falling edge of SCK, see Figure 7. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for aborting an invalid conversion cycle or synchronizing the start of a conversion.

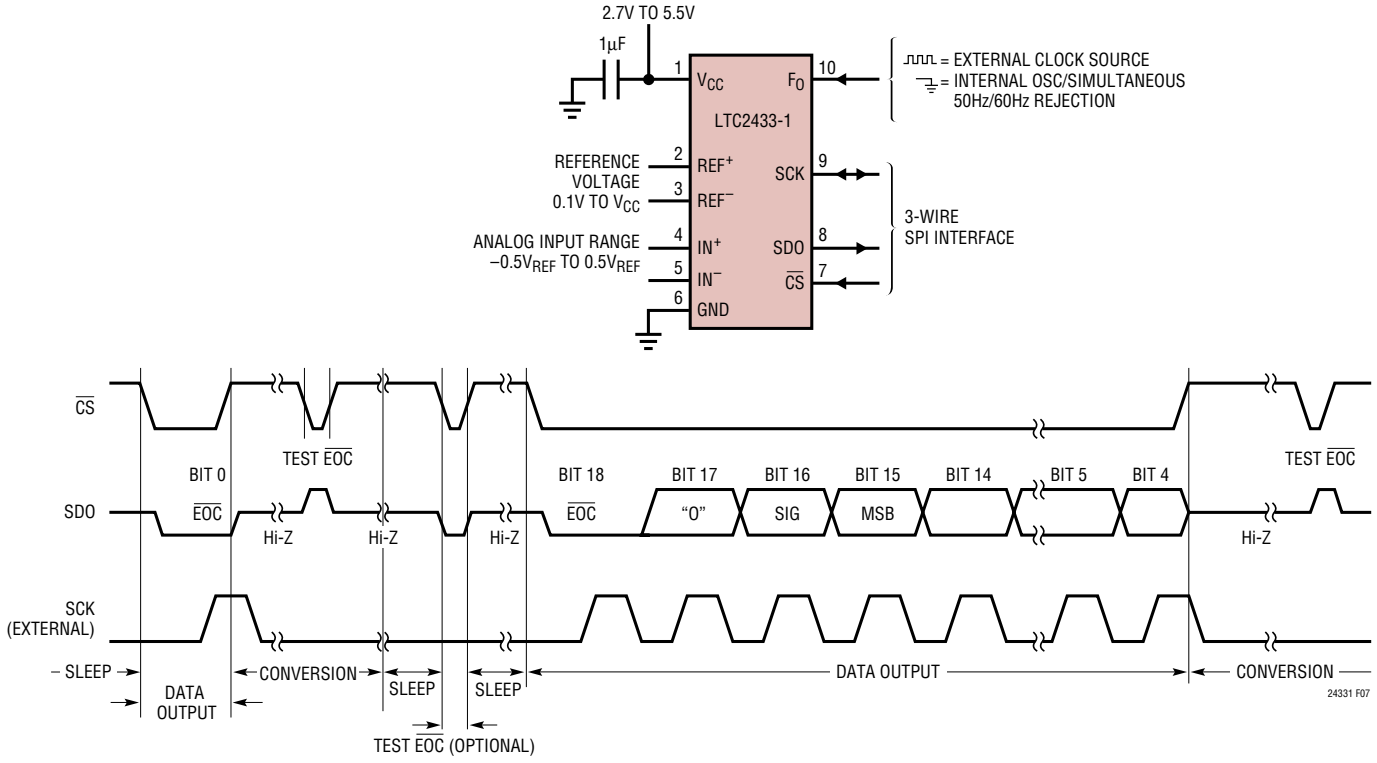


**Figure 7. External Serial Clock, Reduced Data Output Length**

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### External Serial Clock, 2-Wire I/O

This timing mode utilizes a 2-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 8. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded typically 1ms after $V_{CC}$ exceeds 2V. The level applied to SCK at this time determines if SCK is internal or external. SCK must be driven LOW prior to the end of POR in order to enter the external serial clock timing mode.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion ends. On the falling edge of $\overline{EOC}$, the conversion result is loaded into an internal static shift register. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 19th falling edge of SCK, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

### Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 9.

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating (Hi-Z) or pulled HIGH prior to the falling edge of $\overline{CS}$. The device will not enter the internal serial clock mode if SCK is driven LOW on the falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state during the $\overline{EOC}$ test. In order to allow the device to return to the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH

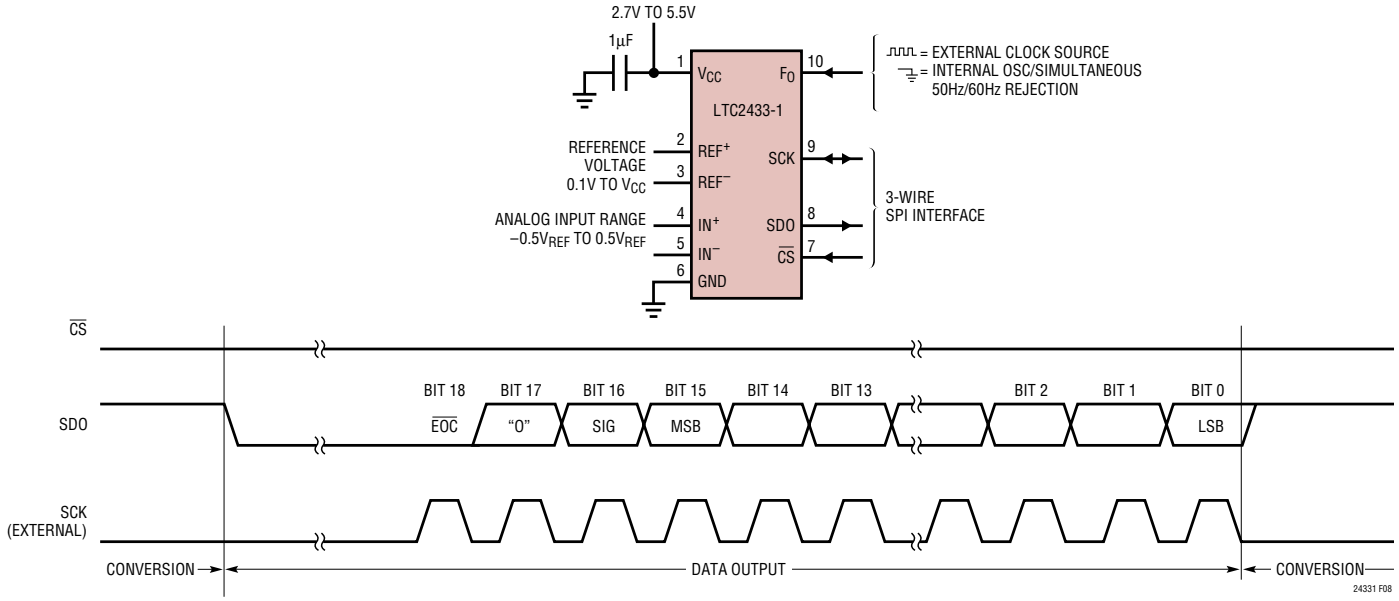


**Figure 8. External Serial Clock, $\overline{CS}$ = 0 Operation (2-Wire)**

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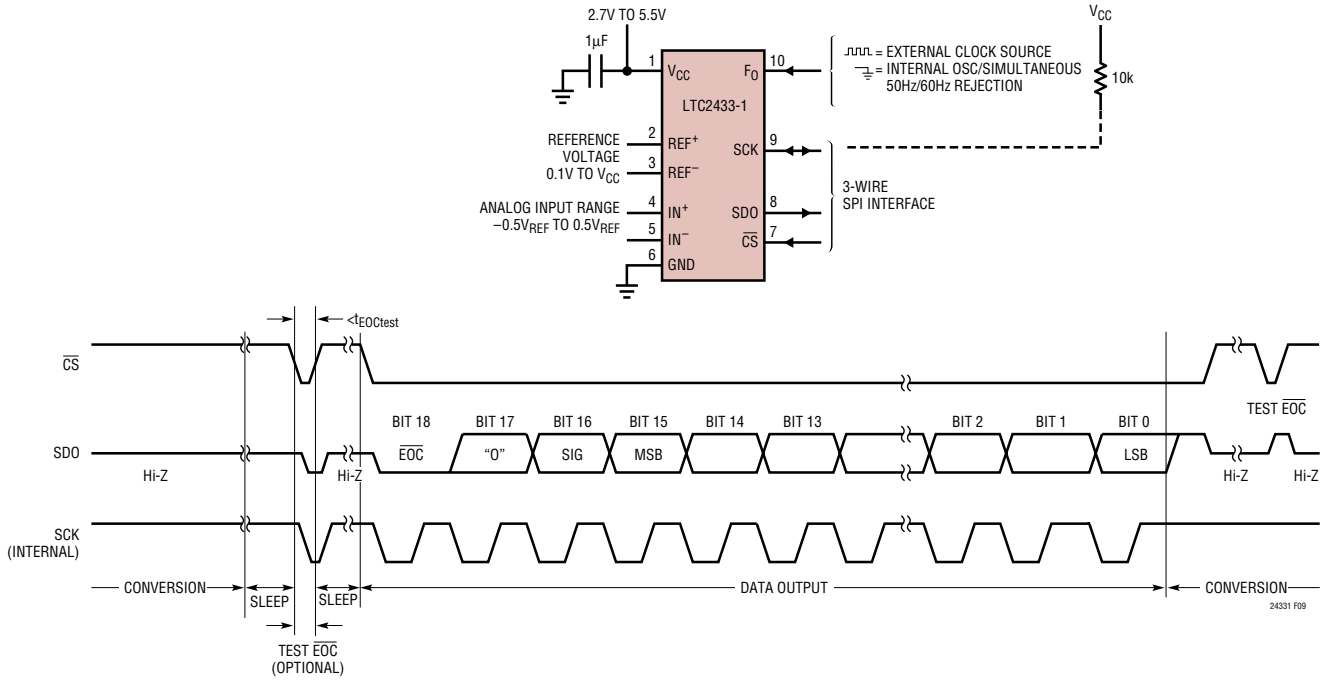


**Figure 9. Internal Serial Clock, Single Cycle Operation**

and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC} = 0$) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 23µs if the device is using its internal oscillator ($F_O$ = logic LOW). If $F_O$ is driven by an external oscillator of frequency $f_{EOSC}$, then $t_{EOCtest}$ is $3.6/f_{EOSC}$. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device returns to the sleep state and the conversion result is held in the internal static shift register.

If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle concludes after the 19th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 19th rising edge of SCK. After the 19th rising edge, SDO goes HIGH ($\overline{EOC} = 1$), SCK stays HIGH and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 19th rising edge of SCK, see Figure 10. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for aborting an invalid conversion cycle, or synchronizing the start of a conversion. If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state. This will cause the device to exit the internal serial clock mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin or by never pulling $\overline{CS}$ HIGH when SCK is LOW.

Whenever SCK is LOW, the LTC2433-1's internal pull-up at pin SCK is disabled. Normally, SCK is not externally driven if the device is in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If this driver goes Hi-Z after outputting a LOW signal, the LTC2433-1's internal pull-up remains

## APPLICATIONS INFORMATION

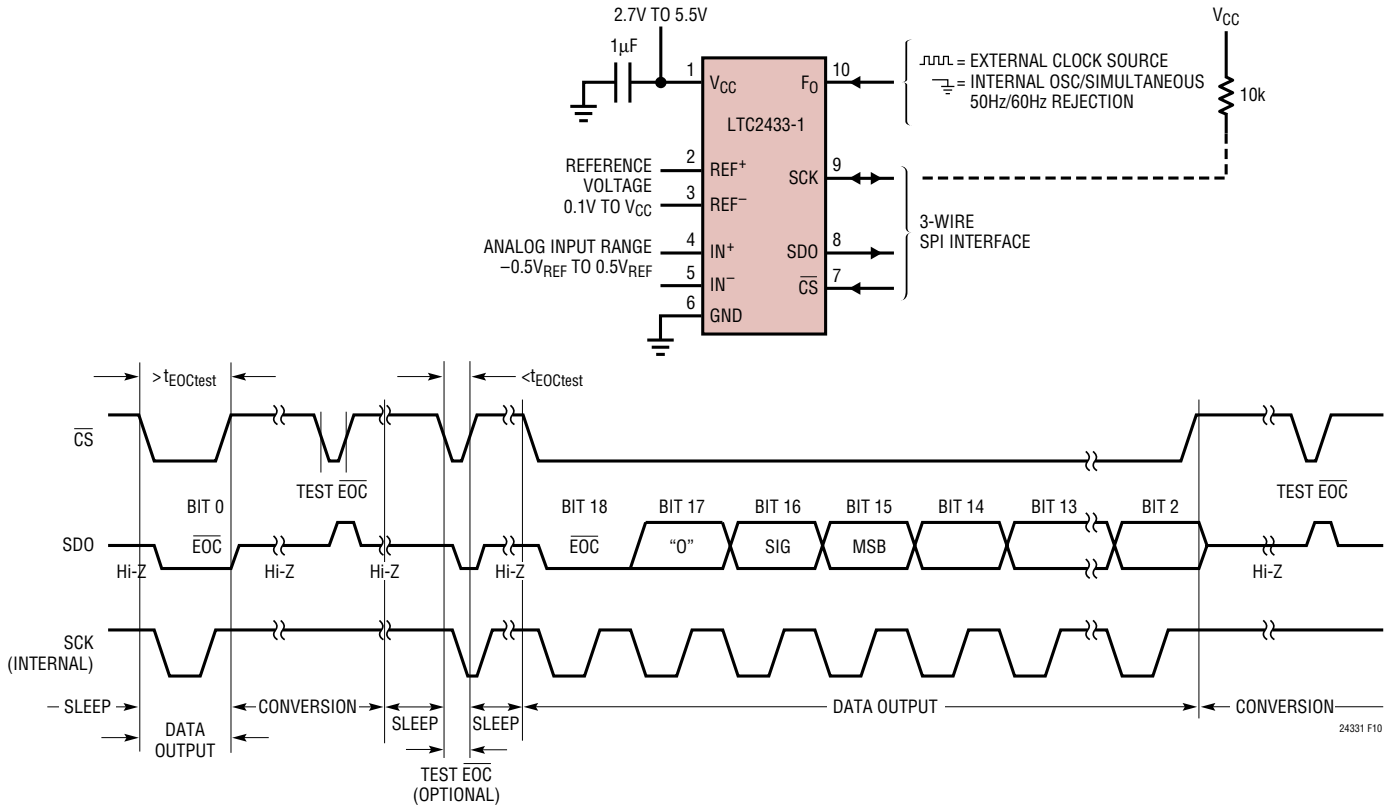


**Figure 10. Internal Serial Clock, Reduced Data Output Length**

disabled. Hence, SCK remains LOW. On the next falling edge of $\overline{CS}$, the device is switched to the external SCK timing mode. By adding an external 10k pull-up resistor to SCK, this pin goes HIGH once the external driver goes Hi-Z. On the next $\overline{CS}$ falling edge, the device will remain in the internal SCK timing mode.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. Once $\overline{CS}$ goes HIGH (within the time period defined above as $t_{EOCtest}$), the internal pull-up is activated. For a heavy capacitive load on the SCK pin, the internal pull-up may not be adequate to return SCK to a HIGH level before $\overline{CS}$ goes low again. This is not a concern under normal conditions where $\overline{CS}$ remains LOW after detecting $\overline{EOC}$ = 0. This situation is easily overcome by adding an external 10k pull-up resistor to the SCK pin.

### Internal Serial Clock, 2-Wire I/O, Continuous Conversion

This timing mode uses a 2-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 11. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 1ms after $V_{CC}$ exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is not externally driven LOW (if SCK is loaded such that the internal pull-up cannot pull the pin HIGH, the external SCK mode will be selected).

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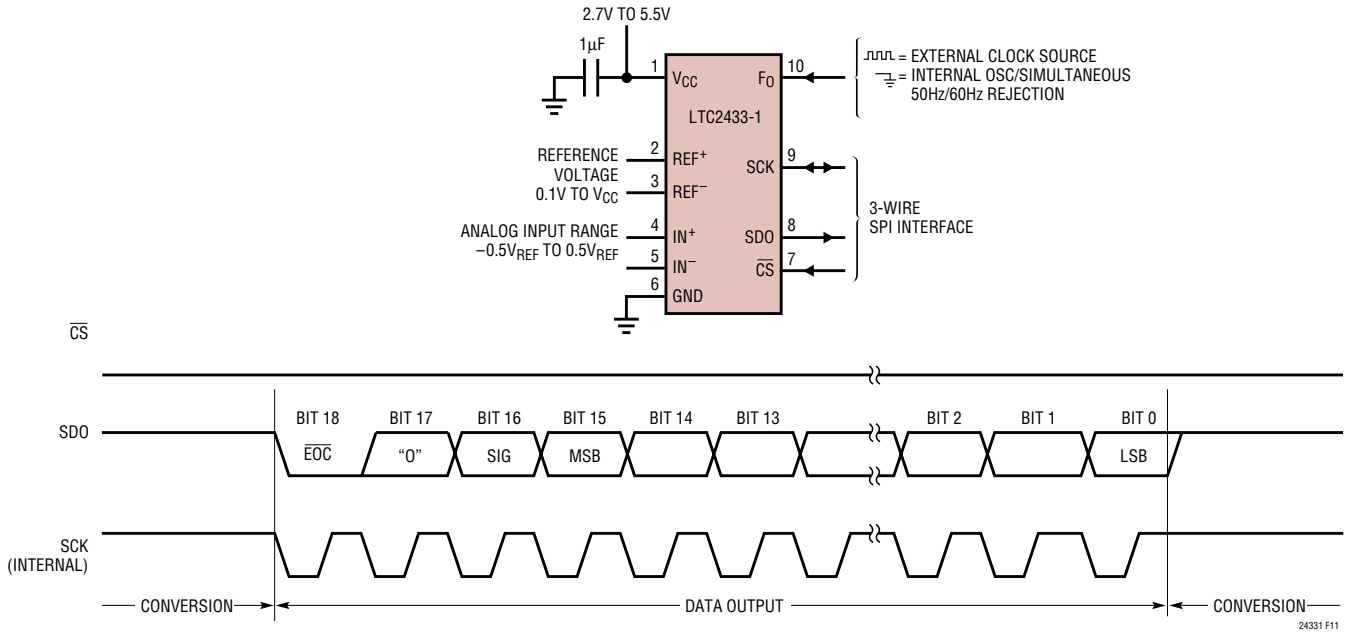



**Figure 11. Internal Serial Clock, Continuous Operation**

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the data output state. The data output cycle begins on the first rising edge of SCK and ends after the 19th rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 19th rising edge of SCK. After the 19th rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

### PRESERVING THE CONVERTER ACCURACY

The LTC2433-1 is designed to reduce as much as possible the conversion result sensitivity to device decoupling, PCB layout, antialiasing circuits, line frequency perturbations and so on. Nevertheless, in order to preserve the accuracy capability of this part, some simple precautions are desirable.

### Digital Signal Levels

The LTC2433-1's digital interface is easy to use. Its digital inputs ($F_O$, $\overline{CS}$ and SCK in External SCK mode of operation) accept standard TTL/CMOS logic levels and the internal hysteresis receivers can tolerate edge rates as slow as 100µs. However, some considerations are required to take advantage of the exceptional accuracy and low supply current of this converter.

The digital output signals (SDO and SCK in Internal SCK mode of operation) are less of a concern because they are not generally active during the conversion state.

While a digital input signal is in the range 0.5V to ($V_{CC}$ – 0.5V), the CMOS input receiver draws additional current from the power supply. It should be noted that, when any one of the digital input signals ($F_O$, $\overline{CS}$ and SCK in External SCK mode of operation) is within this range, the LTC2433-1 power supply current may increase even if the signal in question is at a valid logic level. For micropower operation, it is recommended to drive all digital input signals to full CMOS levels [$V_{IL}$ < 0.4V and $V_{OH}$ > ($V_{CC}$ – 0.4V)].

## APPLICATIONS INFORMATION

During the conversion period, the undershoot and/or overshoot of a fast digital signal connected to the LTC2433-1 pins may severely disturb the analog to digital conversion process. Undershoot and overshoot can occur because of the impedance mismatch at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to LTC2433-1. For reference, on a regular FR-4 board, signal propagation velocity is approximately 183ps/inch for internal traces and 170ps/inch for surface traces. Thus, a driver generating a control signal with a minimum transition time of 1ns must be connected to the converter pin through a trace shorter than 2.5 inches. This problem becomes particularly difficult when shared control lines are used and multiple reflections may occur. The solution is to carefully terminate all transmission lines close to their characteristic impedance.

Parallel termination near the LTC2433-1 pin will eliminate this problem but will increase the driver power dissipation. A series resistor between 27Ω and 56Ω placed near the driver will also eliminate this problem without additional power dissipation. The actual resistor value depends upon the trace impedance and connection topology.

An alternate solution is to reduce the edge rate of the control signals. It should be noted that using very slow edges will increase the converter power supply current during the transition time. The multiple ground pins used in this package configuration, as well as the differential input and reference architecture, reduce substantially the converter's sensitivity to ground currents.

Particular attention must be given to the connection of the $F_O$ signal when the LTC2433-1 is used with an external conversion clock. This clock is active during the conversion time and the normal mode rejection provided by the internal digital filter is not very high at this frequency. A normal mode signal of this frequency at the converter reference terminals may result in DC gain and INL errors. A normal mode signal of this frequency at the converter input terminals may result in a DC offset error. Such perturbations may occur due to asymmetric capacitive coupling between the $F_O$ signal trace and the converter input and/or reference connection traces. An immediate solution is to maintain maximum possible separation between the $F_O$ signal trace and the input/reference signals. When the $F_O$ signal is parallel terminated near the converter, substantial AC current is flowing in the loop formed by the $F_O$ connection trace, the termination and the ground return path. Thus, perturbation signals may be inductively coupled into the converter input and/or reference. In this situation, the user must reduce to a minimum the loop area for the $F_O$ signal as well as the loop area for the differential input and reference connections.

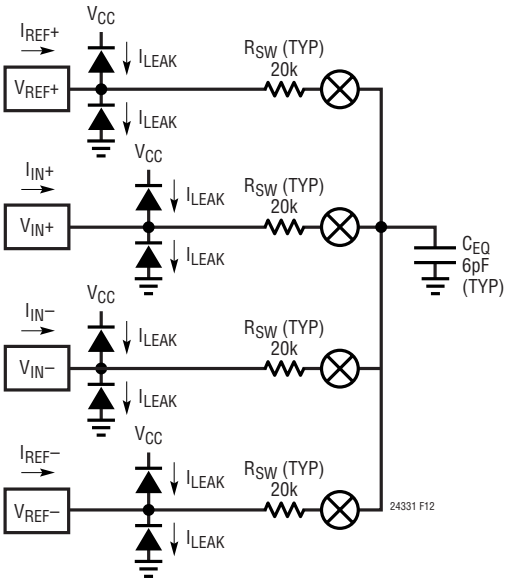
### Driving the Input and Reference

The input and reference pins of the LTC2433-1 converter are directly connected to a network of sampling capacitors. Depending upon the relation between the differential input voltage and the differential reference voltage, these capacitors are switching between these four pins transfering small amounts of charge in the process. A simplified equivalent circuit is shown in Figure 12, where $IN^+$ and $IN^-$ refer to the selected differential channel and the unselected channel is omitted for simplicity.

For a simple approximation, the source impedance $R_S$ driving an analog input pin ($IN^+$, $IN^-$, $REF^+$ or $REF^-$) can be considered to form, together with $R_{SW}$ and $C_{EQ}$ (see Figure 12), a first order passive network with a time constant $\tau = (R_S + R_{SW}) \bullet C_{EQ}$. The converter is able to sample the input signal with better than 1LSB accuracy if the sampling period is at least 11 times greater than the input circuit time constant $\tau$. The sampling process on the four input analog pins is quasi-independent so each time constant should be considered by itself and, under worst-case circumstances, the errors may add.

When using the internal oscillator ($F_O$ = LOW), the LTC2433-1's front-end switched-capacitor network is clocked at 69900Hz corresponding to a 14.3μs sampling

## APPLICATIONS INFORMATION




SWITCHING FREQUENCY
$f_{SW}$ = 69900Hz INTERNAL OSCILLATOR ($F_O$ = LOW)
$f_{SW}$ = 0.5 • $f_{EOSC}$ EXTERNAL OSCILLATOR

$$I\left(IN^+\right)_{AVG} = \frac{V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \bullet R_{EQ}}$$

$$I\left(IN^-\right)_{AVG} = \frac{-V_{IN} + V_{INCM} - V_{REFCM}}{0.5 \bullet R_{EQ}}$$

$$I\left(REF^+\right)_{AVG} = \frac{1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

$$I\left(REF^-\right)_{AVG} = \frac{-1.5 \bullet V_{REF} - V_{INCM} + V_{REFCM}}{0.5 \bullet R_{EQ}} + \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$$V_{REF} = REF^+ - REF^-$$

$$V_{REFCM} = \left(\frac{REF^+ + REF^-}{2}\right)$$

$$V_{IN} = IN^+ - IN^-$$

$$V_{INCM} = \left(\frac{IN^+ - IN^-}{2}\right)$$

$R_{EQ}$ = 11.9MΩ INTERNAL OSCILLATOR 50Hz / 60Hz Notch ($F_O$ = LOW)

$R_{EQ} = \left(1.67 \bullet 10^{12}\right) / f_{EOSC}$ EXTERNAL OSCILLATOR

**Figure 12. LTC2433-1 Equivalent Analog Input Circuit**

period. Thus, for settling errors of less than 1LSB, the driving source impedance should be chosen such that $\tau \leq$ 14.3µs/11 = 1.3µs. When an external oscillator of frequency $f_{EOSC}$ is used, the sampling period is $2/f_{EOSC}$ and, for a settling error of less than 1LSB, $\tau \leq 0.18/f_{EOSC}$.

### Input Current

If complete settling occurs on the input, conversion results will be unaffected by the dynamic input current. An incomplete settling of the input signal sampling process may result in gain and offset errors, but it will not degrade the INL performance of the converter. Figure 12 shows the mathematical expressions for the average bias currents flowing through the $IN^+$ and $IN^-$ pins as a result of the sampling charge transfers when integrated over a substantial time period (longer than 64 internal clock cycles).

The effect of this input dynamic current can be analyzed using the test circuit of Figure 13. The $C_{PAR}$ capacitor includes the LTC2433-1 pin capacitance (5pF typical) plus the capacitance of the test fixture used to obtain the results shown in Figures 14 and 15. A careful implementation can bring the total input capacitance ($C_{IN} + C_{PAR}$) closer to 5pF thus achieving better performance than the one predicted

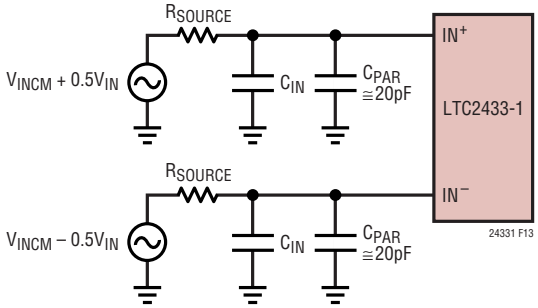



**Figure 13. An RC Network at $IN^+$ and $IN^-$**

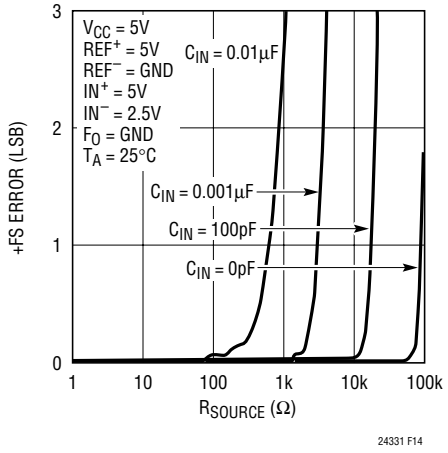



**Figure 14. +FS Error vs $R_{SOURCE}$ at $IN^+$ or $IN^-$ (Small $C_{IN}$)**

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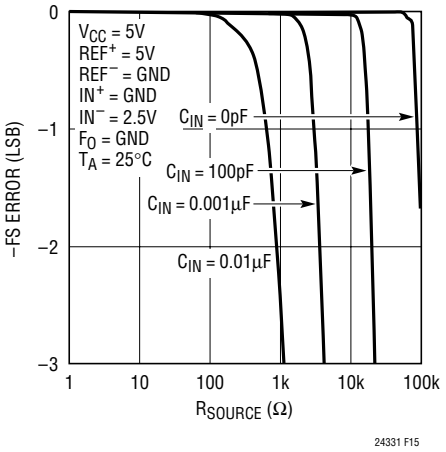


Figure 15. –FS Error vs $R_{SOURCE}$ at $IN^+$ or $IN^-$ (Small $C_{IN}$)

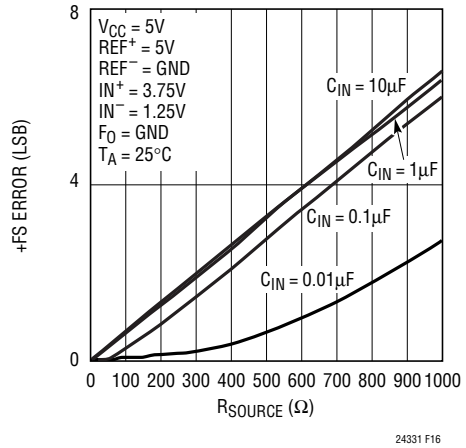


Figure 16. +FS Error vs $R_{SOURCE}$ at $IN^+$ or $IN^-$ (Large $C_{IN}$)

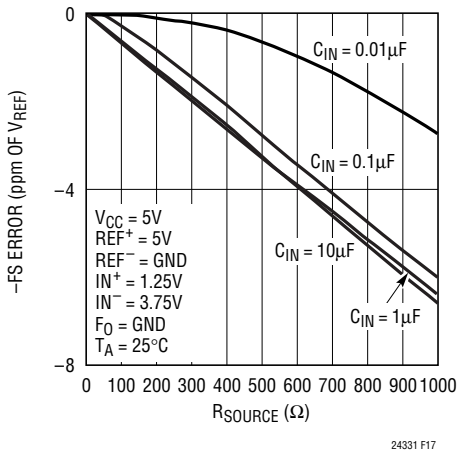


Figure 17. –FS Error vs $R_{SOURCE}$ at $IN^+$ or $IN^-$ (Large $C_{IN}$)

by Figures 14 and 15. For simplicity, two distinct situations can be considered.

For relatively small values of input capacitance ($C_{IN}$ < 0.01µF), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for $C_{IN}$ will deteriorate the converter offset and gain performance without significant benefits of signal filtering and the user is advised to avoid them. Nevertheless, when small values of $C_{IN}$ are unavoidably present as parasitics of input multiplexers, wires, connectors or sensors, the LTC2433-1 can maintain its accuracy while operating with relative large values of source resistance as shown in Figures 14 and 15. These measured results may be slightly different from the first order approximation suggested earlier because they include the effect of the actual second order input network together with the nonlinear settling process of the input amplifiers. For small $C_{IN}$ values, the settling on $IN^+$ and $IN^-$ occurs almost independently and there is little benefit in trying to match the source impedance for the two pins.

Larger values of input capacitors ($C_{IN}$ > 0.01µF) may be required in certain configurations for antialiasing or general input signal filtering. Such capacitors will average the input sampling charge and the external source resistance will see a quasi constant input differential impedance. When $F_O$ = LOW (internal oscillator and 50Hz/60Hz notch), the typical differential input resistance is 6MΩ which will generate a gain error of approximately 1LSB at full scale for each 180Ω of source resistance driving $IN^+$ or $IN^-$. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$ (external conversion clock operation), the typical differential input resistance is $0.84 \bullet 10^{12}/f_{EOSC}\Omega$ and each ohm of source resistance driving $IN^+$ or $IN^-$ will result in $3.7 \bullet 10^{-8} \bullet f_{EOSC}$LSB gain error at full scale. The effect of the source resistance on the two input pins is additive with respect to this gain error. The typical +FS and –FS errors as a function of the sum of the source resistance seen by $IN^+$ and $IN^-$ for large values of $C_{IN}$ are shown in Figures 16 and 17.

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In addition to this gain error, an offset error term may also appear. The offset error is proportional with the mismatch between the source impedance driving the two input pins $IN^+$ and $IN^-$ and with the difference between the input and reference common mode voltages. While the input drive circuit nonzero source impedance combined with the converter average input current will not degrade the INL performance, indirect distortion may result from the modulation of the offset error by the common mode component of the input signal. Thus, when using large $C_{IN}$ capacitor values, it is advisable to carefully match the source impedance seen by the $IN^+$ and $IN^-$ pins. When $F_O$ = LOW (internal oscillator and 50Hz/60Hz notch), every 180Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of 1LSB. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$, every 1Ω mismatch in source impedance transforms a full-scale common mode input signal into a differential mode input signal of $3.7 \cdot 10^{-8} \cdot f_{EOSC}$LSB. Figure 18 shows the typical offset error due to input common mode voltage for various values of source resistance imbalance between the $IN^+$ and $IN^-$ pins when large $C_{IN}$ values are used.

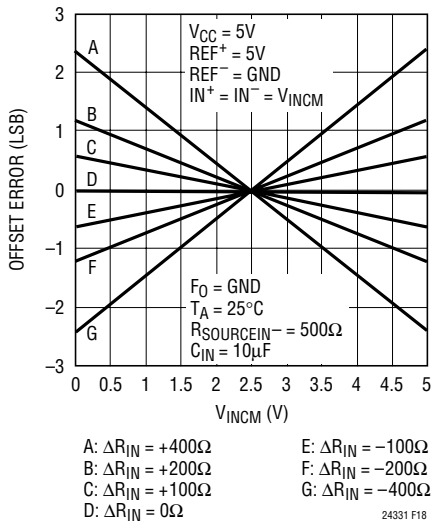


**Figure 18. Offset Error vs Common Mode Voltage ($V_{INCM} = IN^+ = IN^-$) and Input Source Resistance Imbalance ($\Delta R_{IN} = R_{SOURCEIN+} - R_{SOURCEIN-}$) for Large $C_{IN}$ Values ($C_{IN} \geq 1\mu F$)**

If possible, it is desirable to operate with the input signal common mode voltage very close to the reference signal common mode voltage as is the case in the ratiometric measurement of a symmetric bridge. This configuration eliminates the offset error caused by mismatched source impedances.

The magnitude of the dynamic input current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typically better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by $IN^+$ and $IN^-$, the expected drift of the dynamic current, offset and gain errors will be insignificant (about 1% of their respective values over the entire temperature and voltage range). Even for the most stringent applications, a one-time calibration operation may be sufficient.

In addition to the input sampling charge, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA max), results in a small offset shift. A 15k source resistance will create a 0LSB typical and 1LSB maximum offset voltage.

### Reference Current

In a similar fashion, the LTC2433-1 samples the differential reference pins $REF^+$ and $REF^-$ transfering small amount of charge to and from the external driving circuits thus producing a dynamic reference current. This current does not change the converter offset, but it may degrade the gain and INL performance. The effect of this current can be analyzed in the same two distinct situations.

For relatively small values of the external reference capacitors ($C_{REF} < 0.01\mu F$), the voltage on the sampling capacitor settles almost completely and relatively large values for the source impedance result in only small errors. Such values for $C_{REF}$ will deteriorate the converter offset and gain performance without significant benefits of reference filtering and the user is advised to avoid them.

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Larger values of reference capacitors ($C_{REF}$ > 0.01µF) may be required as reference filters in certain configurations. Such capacitors will average the reference sampling charge and the external source resistance will see a quasi constant reference differential impedance. When $F_O$ = LOW (internal oscillator and 50Hz/60Hz notch), the typical differential reference resistance is 4.2MΩ which will generate a gain error of approximately 1LSB full scale for each 120Ω of source resistance driving $REF^+$ or $REF^-$. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$ (external conversion clock operation), the typical differential reference resistance is $0.60 \cdot 10^{12}/f_{EOSC}\Omega$ and each ohm of source resistance drving $REF^+$ or $REF^-$ will result in $5.1 \cdot 10^{-8} \cdot f_{EOSC}$LSB gain error at full scale. The effect of the source resistance on the two reference pins is additive with respect to this gain error. The typical +FS and –FS errors for various combinations of source resistance seen by the $REF^+$ and $REF^-$ pins and external capacitance $C_{REF}$ connected to these pins are shown in Figures 19, 20, 21 and 22.

In addition to this gain error, the converter INL performance is degraded by the reference source impedance. When $F_O$ = LOW (internal oscillator and 50Hz/60Hz notch), every 1000Ω of source resistance driving $REF^+$ or $REF^-$ translates into about 1LSB additional INL error. When $F_O$ is driven by an external oscillator with a frequency $f_{EOSC}$, every 1000Ω of source resistance driving $REF^+$ or $REF^-$

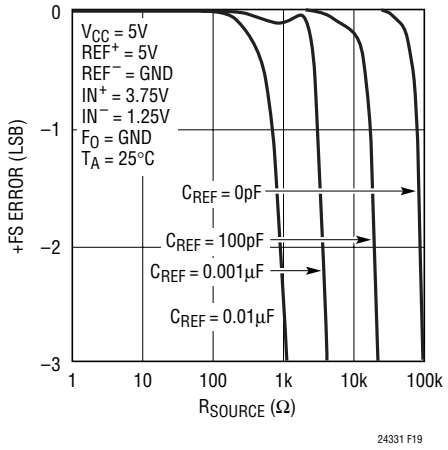


**Figure 19. +FS Error vs $R_{SOURCE}$ at $REF^+$ or $REF^-$ (Small $C_{IN}$)**

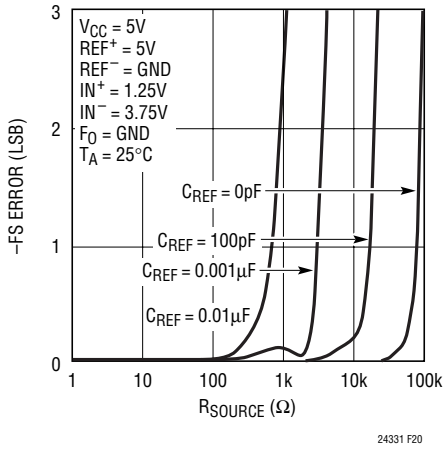


**Figure 20. –FS Error vs $R_{SOURCE}$ at $REF^+$ or $REF^-$ (Small $C_{IN}$)**

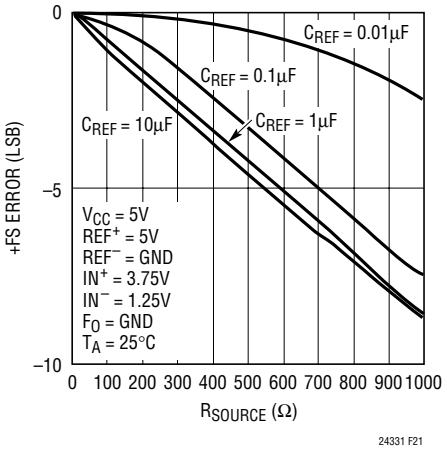


**Figure 21. +FS Error vs $R_{SOURCE}$ at $REF^+$ and $REF^-$ (Large $C_{REF}$)**

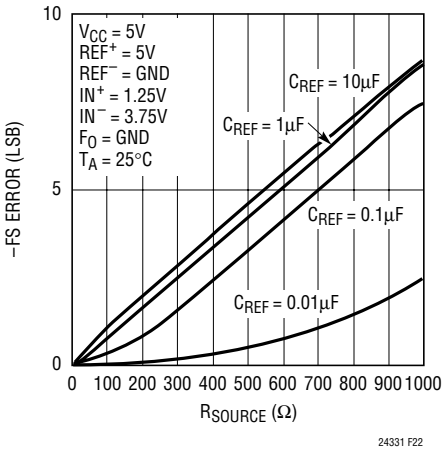


**Figure 22. –FS Error vs $R_{SOURCE}$ at $REF^+$ and $REF^-$ (Large $C_{REF}$)**

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translates into about $7.15 \cdot 10^{-6} \cdot f_{EOSC}$LSB additional INL error. Figure 23 shows the typical INL error due to the source resistance driving the $REF^+$ or $REF^-$ pins when large $C_{REF}$ values are used. The effect of the source resistance on the two reference pins is additive with respect to this INL error. In general, matching of source impedance for the $REF^+$ and $REF^-$ pins does not help the gain or the INL error. The user is thus advised to minimize the combined source impedance driving the $REF^+$ and $REF^-$ pins rather than to try to match it.

The magnitude of the dynamic reference current depends upon the size of the very stable internal sampling capacitors and upon the accuracy of the converter sampling clock. The accuracy of the internal clock over the entire temperature and power supply range is typical better than 0.5%. Such a specification can also be easily achieved by an external clock. When relatively stable resistors (50ppm/°C) are used for the external source impedance seen by $REF^+$ and $REF^-$, the expected drift of the dynamic current gain error will be insignificant (about 1% of its value over the entire temperature and voltage range). Even for the most stringent applications a one-time calibration operation may be sufficient.

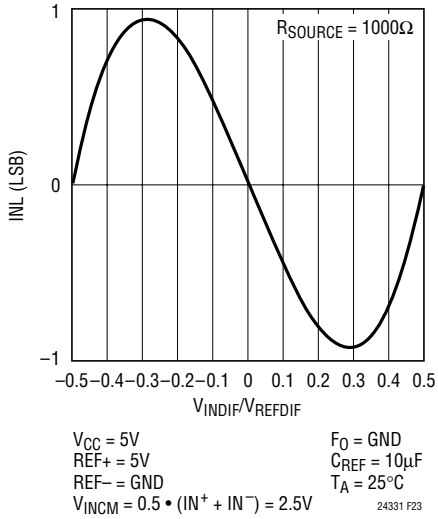


**Figure 23. INL vs Differential Input Voltage ($V_{IN} = IN^+ – IN^-$) and Reference Source Resistance ($R_{SOURCE}$ at $REF^+$ and $REF^-$ for Large $C_{REF}$ Values ($C_{REF} \geq 1\mu F$)**

In addition to the reference sampling charge, the reference pins ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max), results in a small gain error. A 100Ω source resistance will create a 0.05µV typical and 0.5µV maximum full-scale error.

### Output Data Rate

When using its internal oscillator, the LTC2433-1 can produce up to 6.8 readings per second. The actual output data rate will depend upon the length of the sleep and data output phases which are controlled by the user and which can be made insignificantly short. When operated with an external conversion clock ($F_O$ connected to an external oscillator), the LTC2433-1 output data rate can be increased as desired. The duration of the conversion phase is $20510/f_{EOSC}$. If $f_{EOSC}$ = 139,800Hz, the converter behaves as if the internal oscillator is used with simultaneous 50Hz/60Hz. There is no significant difference in the LTC2433-1 performance between these two operation modes.

An increase in $f_{EOSC}$ over the nominal 139,800Hz will translate into a proportional increase in the maximum output data rate. This substantial advantage is nevertheless accompanied by three potential effects, which must be carefully considered.

First, a change in $f_{EOSC}$ will result in a proportional change in the internal notch position and in a reduction of the converter differential mode rejection at the power line frequency. In many applications, the subsequent performance degradation can be substantially reduced by relying upon the LTC2433-1's exceptional common mode rejection and by carefully eliminating common mode to differential mode conversion sources in the input circuit. The user should avoid single-ended input filters and should maintain a very high degree of matching and symmetry in the circuits driving the $IN^+$ and $IN^-$ pins.

Second, the increase in clock frequency will increase proportionally the amount of sampling charge transferred through the input and the reference pins. If large external

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input and/or reference capacitors ($C_{IN}$, $C_{REF}$) are used, the previous section provides formulae for evaluating the effect of the source resistance upon the converter performance for any value of $f_{EOSC}$. If small external input and/or reference capacitors ($C_{IN}$, $C_{REF}$) are used, the effect of the external source resistance upon the LTC2433-1 typical performance can be inferred from Figures 14, 15, 19 and 20 in which the horizontal axis is scaled by 139,800/$f_{EOSC}$.

Third, an increase in the frequency of the external oscillator above 460800Hz (a more than 3× increase in the output data rate) will start to decrease the effectiveness of the internal autocalibration circuits. This will result in a progressive degradation in the converter accuracy and linearity. Typical measured performance curves for output data rates up to 100 readings per second are shown in Figures 24, 25, 26, 27, 28 and 29. In order to obtain the

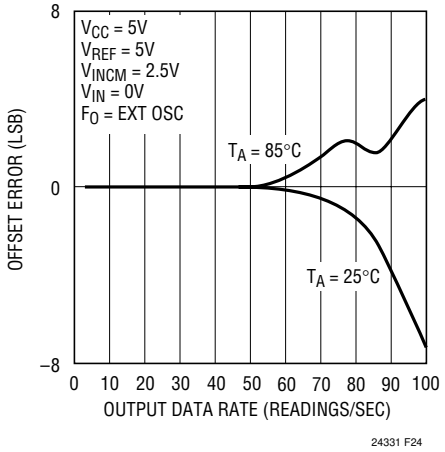


**Figure 24. Offset Error vs Output Data Rate and Temperature**

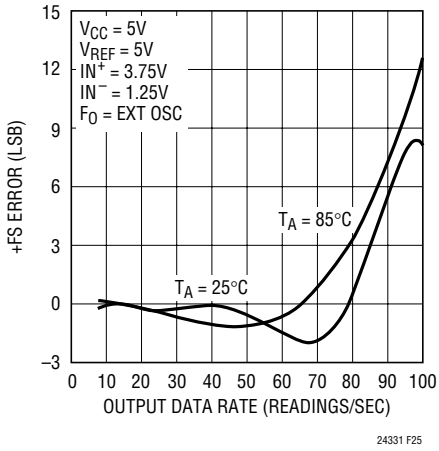


**Figure 25. +FS Error vs Output Data Rate and Temperature**

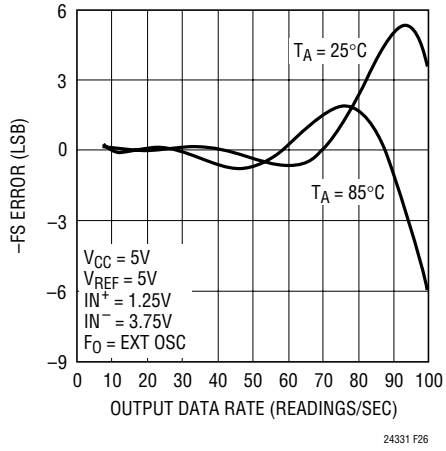


**Figure 26. –FS Error vs Output Data Rate and Temperature**

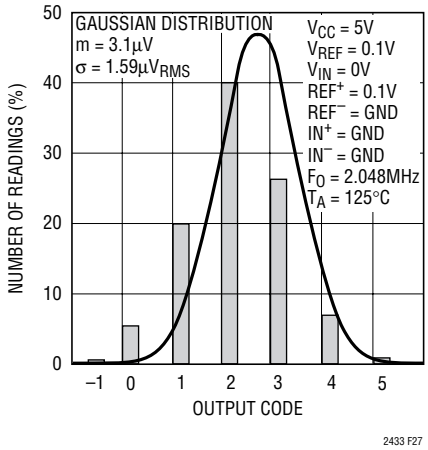


**Figure 27. Noise Histogram (Output Rate = 100Hz, $V_{CC}$ = 5V, $V_{REF}$ = 100mV, 125°C)**