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24-Bit High Speed 8-Channel ΔΣ ADCs with Selectable Multiple Reference Inputs

FEATURES

- **Five Selectable Differential Reference Inputs**
- **Four Differential/Eight Single-Ended Inputs**
- **4-Way MUX for Multiple Ratiometric Measurements**
- **Up to 8kHz Output Rate (External f_O)**
- **Up to 4kHz Multiplexing Rate (External f_O)**
- **Selectable Speed/Resolution:**
  - **2μV_{RMS} Noise at 1.76kHz Output Rate**
  - **200nV_{RMS} Noise at 13.8Hz Output Rate with Simultaneous 50/60Hz Rejection**
- **Guaranteed Modulator Stability and Lock-Up Immunity for any Input and Reference Conditions**
- **0.0005% INL, No Missing Codes**
- **Autosleep Enables 20μA Operation at 6.9Hz**
- **<5μV Offset (4.5V < V_{CC} < 5.5V, –40°C to 85°C)**
- **Differential Input and Differential Reference with GND to V_{CC} Common Mode Range**
- No Latency Mode, Each Conversion is Accurate Even After a New Channel is Selected
- Internal Oscillator—No External Components
- LTC2447 Includes MUXOUT/ADCIN for External Buffering or Gain
- Tiny QFN 5mm × 7mm Package

APPLICATIONS

- Flow
- Weight Scales
- Pressure
- Direct Temperature Measurement
- Gas Chromatography

DESCRIPTION

The LTC®2446/LTC2447 4-terminal switching enables multiplexed ratiometric measurements. Four sets of selectable differential inputs coupled with four sets of differential reference inputs allow multiple RTDs, bridges and other sensors to be digitized by a single converter. A fifth differential reference input can be selected for any input channel not requiring ratiometric measurements (thermocouples, voltages, current sense, etc.). The flexible input multiplexer allows single-ended or differential inputs coupled with a slaved reference input or a universal reference input.

A proprietary delta-sigma architecture results in absolute accuracy (offset, full-scale, linearity) of 15ppm, noise as low as 200nV_{RMS} and speeds as high as 8kHz. Through a simple 4-wire interface, ten speed/resolution combinations can be selected. The first conversion following a speed, resolution, channel change or reference change is valid since there is no settling time between conversions, enabling scan rates of up to 4kHz. Additionally, a 2× mode can be selected for any speed-enabling output rates up to 8kHz with one cycle of latency.

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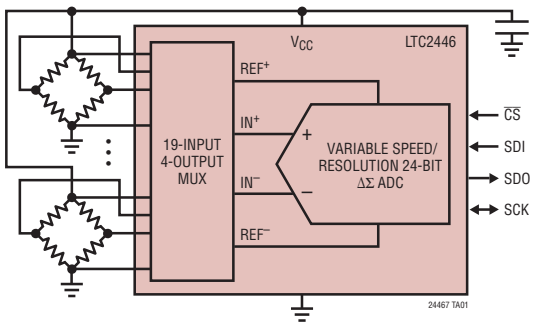
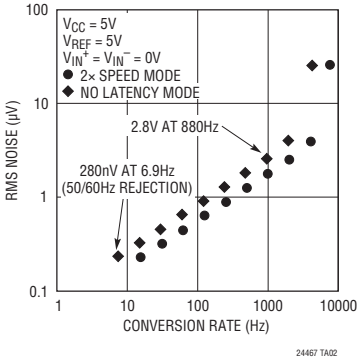
TYPICAL APPLICATION

Multiple Ratiometric Measurement System



LTC2446 RMS Noise vs Speed

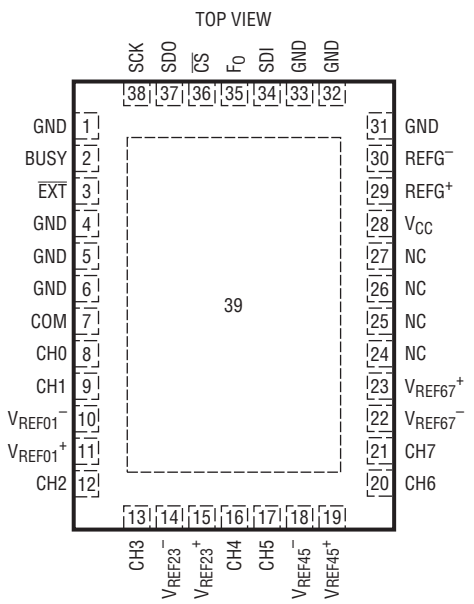


ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC}) to GND ..... –0.3V to 6V
Analog Input Pins Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Reference Input Pins Voltage
to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage to GND ..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2446C/LTC2447C ..... 0°C to 70°C
LTC2446I/LTC2447I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 125°C

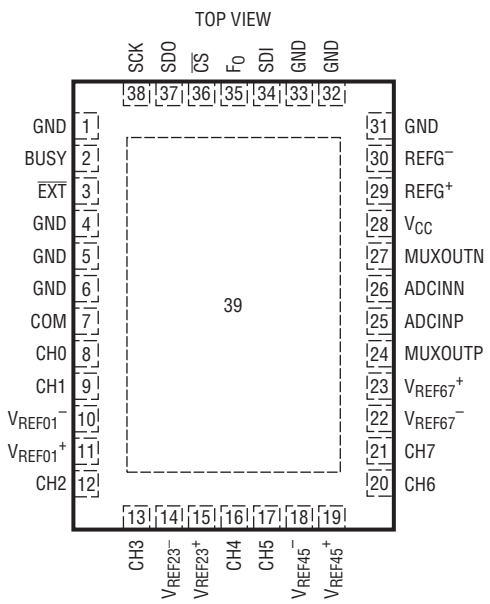
PIN CONFIGURATION

LTC2446



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

LTC2447



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2446#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2446CUHF#PBF	LTC2446CUHF#TRPBF	2446	38-LEAD (5mm × 7mm) PLASTIC QFN	0°C to 70°C
LTC2446IUHF#PBF	LTC2446IUHF#TRPBF	2446	38-LEAD (5mm × 7mm) PLASTIC QFN	–40°C to 85°C
LTC2447CUHF#PBF	LTC2447CUHF#TRPBF	2447	38-LEAD (5mm × 7mm) PLASTIC QFN	0°C to 70°C
LTC2447IUHF#PBF	LTC2447IUHF#TRPBF	2447	38-LEAD (5mm × 7mm) PLASTIC QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –0.5 • V_{REF} ≤ V_{IN} ≤ 0.5 • V_{REF}, (Note 5)	●	24			Bits
Integral Nonlinearity	V_{CC} = 5V, REF^+ = 5V, REF^- = GND, V_{INCM} = 2.5V, (Note 6) REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V, (Note 6)	● 		5 3	15 	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 12)	●		2.5	5	µV
Offset Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^+ = IN^- ≤ V_{CC}			20		nV/°C
Positive Full-Scale Error	REF^+ = 5V, REF^- = GND, IN^+ = 3.75V, IN^- = 1.25V REF^+ = 2.5V, REF^- = GND, IN^+ = 1.875V, IN^- = 0.625V	● ●		10 10	50 50	ppm of V_{REF} ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, IN^+ = 0.75REF^+, IN^- = 0.25 • REF^+			0.2		ppm of V_{REF}/°C
Negative Full-Scale Error	REF^+ = 5V, REF^- = GND, IN^+ = 1.25V, IN^- = 3.75V REF^+ = 2.5V, REF^- = GND, IN^+ = 0.625V, IN^- = 1.875V	● ●		10 10	50 50	ppm of V_{REF} ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, IN^+ = 0.25 • REF^+, IN^- = 0.75 • REF^+			0.2		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V 5V ≤ V_{CC} ≤ 5.5V, REF^+ = 5V, REF^- = GND, V_{INCM} = 2.5V REF^+ = 2.5V, REF^- = GND, V_{INCM} = 1.25V, (Note 6)			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Input Common Mode Rejection DC	2.5V ≤ REF^+ ≤ V_{CC}, REF^- = GND, GND ≤ IN^- = IN^+ ≤ V_{CC}			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage		●	GND – 0.3V		V_{CC} + 0.3V	V
IN^-	Absolute/Common Mode IN^- Voltage		●	GND – 0.3V		V_{CC} + 0.3V	V
V_{IN}	Input Differential Voltage Range (IN^+ – IN^-)		●	–V_{REF}/2		V_{REF}/2	V
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		V_{CC} – 0.1V	V
V_{REF}	Reference Differential Voltage Range (REF^+ – REF^-)		●	0.1		V_{CC}	V
$C_{S(IN+)}$	IN^+ Sampling Capacitance				2		pF
$C_{S(IN-)}$	IN^- Sampling Capacitance				2		pF
$C_{S(REF+)}$	REF^+ Sampling Capacitance				2		pF
$C_{S(REF-)}$	REF^- Sampling Capacitance				2		pF
$I_{DC\_LEAK(IN+, IN-, REF+, REF-)}$	Leakage Current, Inputs and Reference	$\overline{CS}$ = V_{CC}, IN^+ = GND, IN^- = GND, REF^+ = 5V, REF^- = GND	●	–15	1	15	nA
$I_{SAMPLE(IN+, IN-, REF+, REF-)}$	Average Input/Reference Current During Sampling			Varies, See Applications Section			nA
t_{OPEN}	MUX Break-Before-Make				50		ns
QIRR	MUX Off Isolation	V_{IN} = $2V_{P-P}$ DC to 1.8MHz			120		dB

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage $\overline{CS}$, F_O, SDI	4.5V ≤ V_{CC} ≤ 5.5V	●	2.5			V
V_{IL}	Low Level Input Voltage $\overline{CS}$, F_O, SDI	4.5V ≤ V_{CC} ≤ 5.5V	●			0.8	V
V_{IH}	High Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 8)	●	2.5			V
V_{IL}	Low Level Input Voltage SCK	4.5V ≤ V_{CC} ≤ 5.5V (Note 8)	●			0.8	V
I_{IN}	Digital Input Current $\overline{CS}$, F_O, EXT, SDI	0V ≤ V_{IN} ≤ V_{CC}	●	–10		10	µA
I_{IN}	Digital Input Current SCK	0V ≤ V_{IN} ≤ V_{CC} (Note 8)	●	–10		10	µA
C_{IN}	Digital Input Capacitance $\overline{CS}$, F_O, SDI				10		pF
C_{IN}	Digital Input Capacitance SCK	(Note 8)			10		pF
V_{OH}	High Level Output Voltage SDO, BUSY	I_O = –800µA	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SDO, BUSY	I_O = 1.6mA	●			0.4	V
V_{OH}	High Level Output Voltage SCK	I_O = –800µA (Note 9)	●	V_{CC} – 0.5V			V
V_{OL}	Low Level Output Voltage SCK	I_O = 1.6mA (Note 9)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage SDO		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	4.5		5.5	V
I_{CC}	Supply Current Conversion Mode Sleep Mode	 $\overline{CS}$ = 0V (Note 7) $\overline{CS}$ = V_{CC} (Note 7)	 ● ●		 8 8	 11 30	 mA µA

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range		●	0.1		12	MHz
t_{HEO}	External Oscillator High Period		●	25		10000	ns
t_{LEO}	External Oscillator Low Period		●	25		10000	ns
t_{CONV}	Conversion Time	OSR = 256 OSR = 32768 External Oscillator, 1× Mode (Notes 10, 13)	● ● ●	0.99 126 	1.13 145 $\frac{40 \cdot OSR + 178}{f_{EOSC}\ (KHz)}$	1.33 170 	ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Note 9) External Oscillator (Notes 9, 10)	●	0.8	0.9 f_{EOSC}/10	1	MHz Hz

TIMING CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
D_{ISCK}	Internal SCK Duty Cycle	(Note 9)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Note 8)	●			20	MHz
t_{LESCK}	External SCK Low Period	(Note 8)	●	25			ns
t_{HESCK}	External SCK High Period	(Note 8)	●	25			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 9, 11) External Oscillator (Notes 9, 10)	● ●	41.6	35.3 $320/f_{EOSC}$	30.9	µs s
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Note 8)	●		$32/f_{ESCK}$		s
t_1	$\overline{CS}$ ↓ to SDO Low Z	(Note 12)	●	0		25	ns
t_2	$\overline{CS}$ ↑ to SDO High Z	(Note 12)	●	0		25	ns
t_3	$\overline{CS}$ ↓ to SCK ↓	(Note 9)			5		µs
t_4	$\overline{CS}$ ↓ to SCK ↑	(Notes 8, 12)	●	25			ns
t_{KQMAX}	SCK ↓ to SDO Valid		●			25	ns
t_{KQMIN}	SDO Hold After SCK ↓	(Note 5)	●	15			ns
t_5	SCK Setup Before $\overline{CS}$ ↓		●	50			ns
t_6	SCK Hold After $\overline{CS}$ ↓		●			50	ns
t_7	SDI Setup Before SCK ↑	(Note 5)	●	10			ns
t_8	SDI Hold After SCK ↑	(Note 5)	●	10			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: V_{CC} = 4.5V to 5.5V unless otherwise specified. $V_{REF} = REF^+ – REF^–$, $V_{REFCM} = (REF^+ + REF^–)/2$; REF^+ is the positive reference input, $REF^–$ is the negative reference input; $V_{IN} = IN^+ – IN^–$, $V_{INCM} = (IN^+ + IN^–)/2$.

Note 4: F_O pin tied to GND or to external conversion clock source with f_{EOSC} = 10MHz unless otherwise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: The converter uses the internal oscillator.

Note 8: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

Note 9: The converter is in internal SCK mode of operation such that the SCK pin is used as a digital output. In this mode of operation, the SCK pin has a total equivalent load capacitance of C_{LOAD} = 20pF.

Note 10: The external oscillator is connected to the F_O pin. The external oscillator frequency, f_{EOSC}, is expressed in Hz.

Note 11: The converter uses the internal oscillator. F_O = 0V.

Note 12: Guaranteed by design and test correlation.

Note 13: There is an internal reset that adds an additional 5 to 15 f_O cycles to the conversion time.

PIN FUNCTIONS

GND (Pins 1, 4, 5, 6, 31, 32, 33): Ground. Multiple ground pins internally connected for optimum ground current flow and V_{CC} decoupling. Connect each one of these pins to a common ground plane through a low impedance connection. All seven pins must be connected to ground for proper operation.

BUSY (Pin 2): Conversion in Progress Indicator. This pin is HIGH while the conversion is in progress and goes LOW indicating the conversion is complete and data is ready. It remains LOW during the sleep and data output states. At the conclusion of the data output state, it goes HIGH indicating a new conversion has begun.

$\overline{EXT}$ (Pin 3): Internal/External SCK Selection Pin. This pin is used to select internal or external SCK for outputting/inputting data. If $\overline{EXT}$ is tied low, the device is in the external SCK mode and data is shifted out of the device under the control of a user applied serial clock. If $\overline{EXT}$ is tied high, the internal serial clock mode is selected. The device generates its own SCK signal and outputs this on the SCK pin. A framing signal BUSY (Pin 2) goes low indicating data is being output.

PIN FUNCTIONS

COM (Pin 7): The common negative input (IN^-) for all single-ended multiplexer configurations. The voltage on CH0-CH7 and COM pins can have any value between GND – 0.3V to V_{CC} + 0.3V. Within these limits, the two selected inputs (IN^+ and IN^-) provide a bipolar input range ($V_{IN} = IN^+ – IN^-$) from –0.5 • V_{REF} to 0.5 • V_{REF}. Outside this input range, the converter produces unique over-range and under-range output codes.

CH0 to CH7 (Pins 8, 9, 12, 13, 16, 17, 20, 21): Analog Inputs. May be programmed for Single-ended or Differential mode.

V_{REF01}^+ (Pin 11), V_{REF01}^- (Pin 10) V_{REF23}^+ (Pin 15), V_{REF23}^- (Pin 14), V_{REF45}^+ (Pin 19), V_{REF45}^- (Pin 18), V_{REF67}^+ (Pin 23), V_{REF67}^- (Pin 22): Differential Reference Inputs. The voltage on these pins can be anywhere between 0V and V_{CC} as long as the positive reference input (V_{EF01}^+, V_{REF23}^+, V_{REF45}^+, V_{REF67}^+) is greater than the corresponding negative reference input (V_{REF01}^-, V_{REF23}^-, V_{REF45}^-, V_{REF67}^-) by at least 100mV.

NC (Pins 24, 25, 26, 27): LTC2446 No Connect. These pins can either be tied to ground or left floating.

MUXOUTP (Pin 24): LTC2447 Positive Input Channel Multiplexer Output. Used to drive the input to an external buffer/amplifier for the selected positive input signal (IN^+).

ADCINP (Pin 25): LTC2447 Positive ADC Input. Tie to output of buffer/amplifier driven by MUXOUTP.

ADCINN (Pin 26): LTC2447 Negative ADC Input. Tie to output of buffer/amplifier driven by MUXOUTN.

MUXOUTN (Pin 27): LTC2447 Negative Input Channel Multiplexer Output. Used to drive the input to an external buffer/amplifier for the selected negative input signal (IN^-).

V_{CC} (Pin 28): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

V_{REFG}^+ (Pin 29), V_{REFG}^- (Pin 30): Global Reference Input. This differential reference input can be used for any input channel selected through a single bit in the digital input word.

SDI (Pin 34): Serial Data Input. This pin is used to select the speed, 1× or 2× mode, resolution, input channel and reference input for the next conversion cycle. At initial power-up, the default mode of operation is CH0-CH1, V_{REF01}, OSR of 256, and 1× mode. The serial data input contains an enable bit which determines if a new channel/speed is selected. If this bit is low the following conversion remains at the same speed and selected channel. The serial data input is applied to the device under control of the serial clock (SCK) during the data output cycle. The first conversion following a new channel/speed is valid.

F_O (Pin 35): Frequency Control Pin. Digital input that controls the internal conversion clock. When F_O is connected to V_{CC} or GND, the converter uses its internal oscillator.

$\overline{CS}$ (Pin 36): Active Low Chip Select. A LOW on this pin enables the SDO digital output and wakes up the ADC. Following each conversion the ADC automatically enters the sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the Data Output aborts the data transfer and starts a new conversion.

SDO (Pin 37): Three-State Digital Output. During the data output period, this pin is used as serial data output. When the chip select $\overline{CS}$ is HIGH ($\overline{CS} = V_{CC}$) the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. The conversion status can be observed by pulling $\overline{CS}$ LOW. This signal is HIGH while the conversion is in progress and goes LOW once the conversion is complete.

SCK (Pin 38): Bidirectional Digital Clock Pin. In internal serial clock operation mode, SCK is used as a digital output for the internal serial interface clock during the data output period. In the external serial clock operation mode, SCK is used as the digital input for the external serial interface clock during the data output period. The serial clock operation mode is determined by the logic level applied to the $\overline{EXT}$ pin.

Exposed Pad (Pin 39): Ground. The exposed pad on the bottom of the package must be soldered to the PCB ground. For Prototyping purposes, this pin may remain floating.

FUNCTIONAL BLOCK DIAGRAM

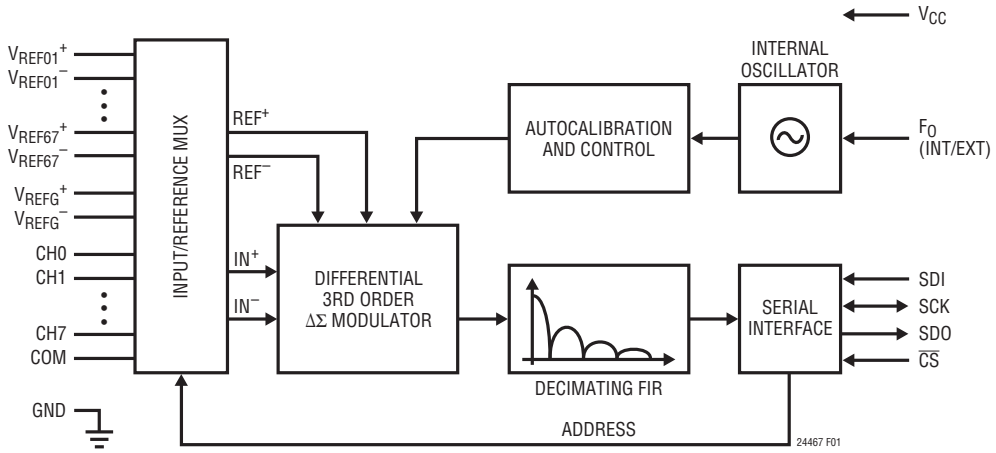
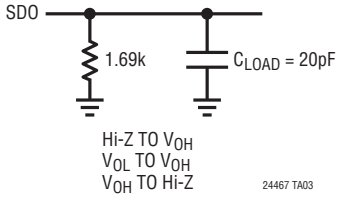
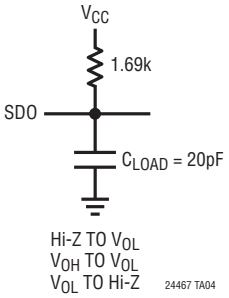


Figure 1. Functional Block Diagram

TEST CIRCUITS





APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2446/LTC2447 are multichannel, multireference high speed, delta-sigma analog-to-digital converters with an easy to use 3- or 4-wire serial interface (see Figure 1). Their operation is made up of three states. The converter operating cycle begins with the conversion, followed by the low power sleep state and ends with the data output/input (see Figure 2). The 4-wire interface consists of serial data input (SDI), serial data output (SDO), serial clock (SCK) and chip select ($\overline{CS}$). The interface, timing, operation cycle and data out format is compatible with Linear's entire family of ΔΣ converters.

Initially, the LTC2446/LTC2447 perform a conversion. Once the conversion is complete, the device enters thesleep state.

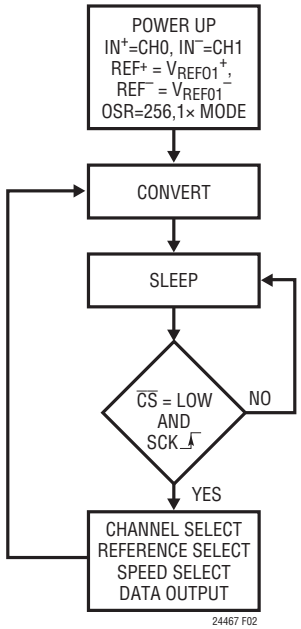


Figure 2. LTC2446/LTC2447 State Transition Diagram

APPLICATIONS INFORMATION

While in this sleep state, power consumption is reduced below 10µA. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. The conversion result is held indefinitely in a static shift register while the converter is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device begins outputting the conversion result. There is no latency in the conversion result while operating in the 1× mode. The data output corresponds to the conversion just performed. This result is shifted out on the serial data out pin (SDO) under the control of the serial clock (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (see Figure 3). The data output state is concluded once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

Through timing control of the $\overline{CS}$, SCK and $\overline{EXT}$ pins, the LTC2446/LTC2447 offer several flexible modes of operation (internal or external SCK). These various modes do not require programming configuration registers; moreover, they do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Ease of Use

The LTC2446/LTC2447 data output has no latency, filter settling delay or redundant data associated with the conversion cycle while operating in the 1× mode. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog voltages and references is easy. Speed/resolution adjustments may be made seamlessly between two conversions without settling errors.

The LTC2446/LTC2447 perform offset and full-scale calibrations every conversion cycle. This calibration is transparent to the user and has no effect on the cyclic operation described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage change and temperature drift.

Power-Up Sequence

The LTC2446/LTC2447 automatically enter an internal reset state when the power supply voltage V_{CC} drops below approximately 2.2V. This feature guarantees the integrity of the conversion result and of the serial interface mode selection.

When the V_{CC} voltage rises above this critical threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 0.5ms. The POR signal clears all internal registers. The conversion immediately following a POR is performed on the input channel IN^+ = CH0, IN^- = CH1, $REF^+ = V_{REF01}{}^+$, $REF^- \ V_{REF01}{}^-$ at an OSR = 256 in the 1× mode. Following the POR signal, the LTC2446/LTC2447 start a normal conversion cycle and follow the succession of states described above. The first conversion result following POR is accurate within the specifications of the device if the power supply voltage is restored within the operating range (4.5V to 5.5V) before the end of the POR time interval.

Reference Voltage Range

These converters accept truly differential external reference voltages. Each set of five reference inputs may be independently driven to any common mode voltage over the entire supply range of the device (GND to V_{CC}). For correct converter operation, each positive reference pin REF^+ ($V_{REF01}{}^+$, $V_{REF23}{}^+$, $V_{REF45}{}^+$, $V_{REF67}{}^+$, $V_{REFG}{}^+$) must be more positive than its corresponding negative reference pin REF^- ($V_{REF01}{}^-$, $V_{REF23}{}^-$, $V_{REF45}{}^-$, $V_{REF67}{}^-$, $V_{REFG}{}^-$) by at least 100mV.

The LTC2446/LTC2447 can accept a differential reference from 0.1V to V_{CC} on each set of reference input pins. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in microvolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a reduced reference voltage will improve the converter's overall INL performance.

Input Voltage Range

Refer to Figure 4. The analog input is truly differential with an absolute/common mode range for the CH0-CH7 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase

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rapidly. Within these limits, the LTC2446/LTC2447 convert the bipolar differential input signal, $V_{IN} = IN^+ – IN^–$ (where IN^+ and $IN^–$ are the selected input channels), from $–FS = –0.5 • V_{REF}$ to $+FS = 0.5 • V_{REF}$ where $V_{REF} = REF^+ – REF^–$ (REF^+ and $REF^–$ are the selected references). Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes.

MUXOUT/ADCIN

There are two differences between the LTC2446 and the LTC2447. The first is the RMS noise performance. For a given OSR, the LTC2447 noise level is approximately $\sqrt{2}$ times lower (0.5 effective bits) than that of the LTC2446.

The second difference is the LTC2447 includes MUXOUT/ADCIN pins. These pins enable an external buffer or gain block to be inserted between the selected input channel of the multiplexer and the input to the ADC. Since the buffer is driven by the output of the multiplexer, only one circuit is required for all 8 input channels. Additionally, the transparent calibration feature of the LTC244X family automatically removes the offset errors of the external buffer.

In order to achieve optimum performance, the MUXOUT and ADCIN pins should not be shorted together. In applications where the MUXOUT and ADCIN need to be shorted together, the LTC2446 should be used because the MUXOUT and ADCIN are internally connected for optimum performance.

Output Data Format

The LTC2446/LTC2447 serial output data stream is 32 bits long. The first 3 bits represent status information indicating the sign and conversion state. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution. In the case of ultrahigh resolution modes, more than 24 effective bits of performance are possible (see Table 4). Under these conditions, sub LSBs are included in the conversion result and represent useful information beyond the 24-bit level. The third and fourth bit together are also used to indicate an underrange condition (the differential input voltage is below –FS) or an overrange condition (the differential input voltage is above +FS).

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available at the SDO pin during the conversion and sleep states whenever the $\overline{CS}$ pin is LOW. This bit is HIGH during the conversion and goes LOW when the conversion is complete.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If V_{IN} is >0, this bit is HIGH. If V_{IN} is <0, this bit is LOW.

Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides the underrange or overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above +FS. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS.

The function of these bits is summarized in Table 1.

Table 1. LTC2446/LTC2447 Status Bits

INPUT RANGE	BIT 31 $\overline{EOC}$	BIT 30 DMY	BIT 29 SIG	BIT 28 MSB
$V_{IN} \geq 0.5 • V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 • V_{REF}$	0	0	1	0
$–0.5 • V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < –0.5 • V_{REF}$	0	0	0	0

Bits 28-5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB).

Bits 4-0 are sub LSBs below the 24-bit level. Bits 4-0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK), see Figure 3. Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and SCK is ignored.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes real time from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is-

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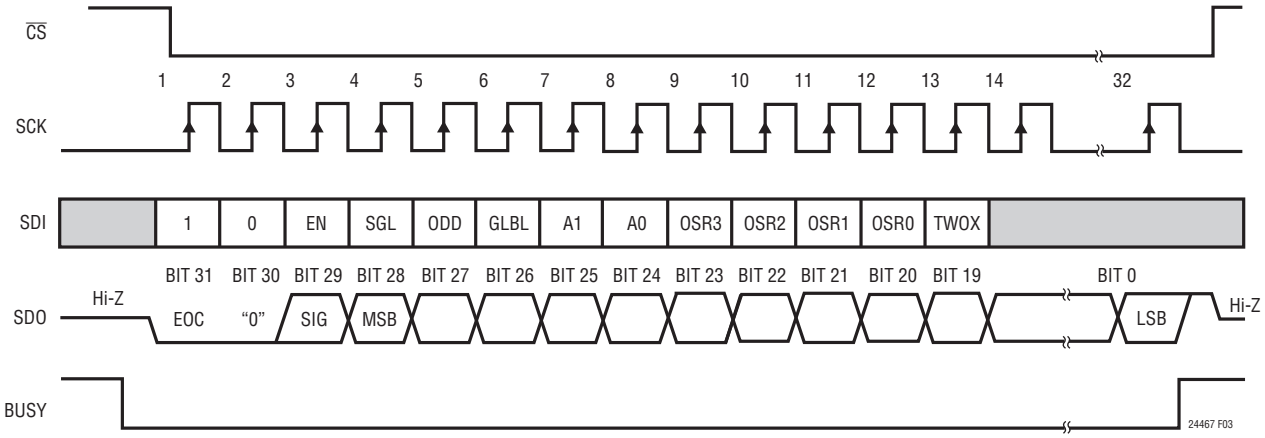

Figure 3. SDI Speed/Resolution, Channel Selection, and Data Output Timing

shifted out on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN^+ and IN^- pins is maintained within the –0.3V to (V_{CC} + 0.3V) absolute maximum operating range, a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to the +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value corresponding to –FS – 1LSB.

SERIAL INTERFACE PINS

The LTC2446/LTC2447 transmit the conversion results and receive the start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to assess the converter status and during the data output state it is used to read the conversion result and program the speed, resolution and input channel.

Table 2. LTC2446/LTC2447 Output Data Format

Differential Input Voltage V_{IN}*	Bit 31 $\overline{EOC}$	Bit 30 DMY	Bit 29 SIG	Bit 28 MSB	Bit 27	Bit 26	Bit 25	…	Bit 0
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	…	0
0.5 • V_{REF}** – 1LSB	0	0	1	0	1	1	1	…	1
0.25 • V_{REF}**	0	0	1	0	1	0	0	…	0
0.25 • V_{REF}** – 1LSB	0	0	1	0	0	1	1	…	1
0	0	0	1	0	0	0	0	…	0
–1LSB	0	0	0	1	1	1	1	…	1
–0.25 • V_{REF}**	0	0	0	1	1	0	0	…	0
–0.25 • V_{REF}** – 1LSB	0	0	0	1	0	1	1	…	1
–0.5 • V_{REF}**	0	0	0	1	0	0	0	…	0
V_{IN}* < –0.5 • V_{REF}**	0	0	0	0	1	1	1	…	1

*The differential input voltage $V_{IN} = IN^+ – IN^-$. **The differential reference voltage $V_{REF} = REF^+ – REF^-$.

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Serial Clock Input/Output (SCK)

The serial clock signal present on SCK (Pin 38) is used to synchronize the data transfer. Each bit of data is shifted out the SDO pin on the falling edge of the serial clock.

In the Internal SCK mode of operation, the SCK pin is an output and the LTC2446/LTC2447 create their own serial clock. In the External SCK mode of operation, the SCK pin is used as input. The internal or external SCK mode is selected by tying $\overline{EXT}$ (Pin 3) LOW for external SCK and HIGH for internal SCK.

Serial Data Output (SDO)

The serial data output pin, SDO (Pin 37), provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ (Pin 36) is HIGH, the SDO driver is switched to a high impedance state. This allows sharing the serial interface with other devices. If $\overline{CS}$ is LOW during the convert or sleep state, SDO will output $\overline{EOC}$. If $\overline{CS}$ is LOW during the conversion phase, the $\overline{EOC}$ bit appears HIGH on the SDO pin. Once the conversion is complete, $\overline{EOC}$ goes LOW. The device remains in the sleep state until the first rising edge of SCK occurs while $\overline{CS}$ = LOW.

Chip Select Input ($\overline{CS}$)

The active LOW chip select, $\overline{CS}$ (Pin 36), is used to test the conversion status and to enable the data output transfer as described in the previous sections.

In addition, the $\overline{CS}$ signal can be used to trigger a new conversion cycle before the entire serial data transfer has been completed. The LTC2446/LTC2447 will abort any serial data transfer in progress and start a new conversion cycle anytime a LOW-to-HIGH transition is detected at the $\overline{CS}$ pin after the converter has entered the data output state.

Serial Data Input (SDI)

The serial data input (SDI, Pin 34) is used to select the speed/resolution input channel and reference of the LTC2446/LTC2447. SDI is programmed by a serial input data stream under the control of SCK during the data output cycle, see Figure 3.

Initially, after powering up, the device performs a conversion with IN^+ = CH0, IN^- = CH1, $REF^+ = V_{REF01}{}^+$, $REF^- = V_{REF01}{}^-$, OSR = 256 (output rate nominally 880Hz), and 1× speed mode (no latency). Once this first conversion is complete, the device enters the sleep state and is ready to output the conversion result and receive the serial data input stream programming the speed/resolution, input channel and reference for the next conversion. At the conclusion of each conversion cycle, the device enters this state.

In order to change the speed/resolution, reference or input channel, the first 3 bits shifted into the device are 101. This is compatible with the programming sequence of the LTC2414/LTC2418/LTC2444/LTC2445/LTC2448/LTC2449. If the sequence is set to 000 or 100, the following input data is ignored (don't care) and the previously selected speed/resolution, channel and reference remain valid for the next conversion. Combinations other than 101, 100, and 000 of the 3 control bits should be avoided.

If the first 3 bits shifted into the device are 101, then the following 5 bits select the input channel/reference for the following conversion (see Table 3). The next 5 bits select the speed/resolution and mode 1× (no latency) 2× (double output rate with one conversion latency), see Table 4. If these 5 bits are set to all 0's, the previous speed remains selected for the next conversion. This is useful in applications requiring a fixed output rate/resolution but need to change the input channel or reference. In this case, the timing and input sequence is compatible with the LTC2414/LTC2418.

When an update operation is initiated (the first 3 bits are 101) the next 5 bits are the channel/reference address. The first bit, SGL, determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of 8 channels is selected as the positive input. The negative input is COM for all single ended operations. The global V_{REF} bit (GLBL) is used to determine which reference is selected. GLBL = 0 selects the individual reference slaved to a given channel. Each set of channels has a corresponding differential input reference. If GLBL = 1, a global reference $V_{REFG}{}^+/V_{REFG}{}^-$ is selected. The global reference input may be used for any input channel selected. Table 3 shows a summary of input/reference selection. The remaining bits (ODD, A1, A0) determine which channel is selected.

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Table 3. Channel Selection for the LTC2446/LTC2447

MUX ADDRESS					CHANNEL INPUT									REFERENCE INPUT									
SGL	ODD/ SIGN	GLBL	A1	A0	0	1	2	3	4	5	6	7	COM	01+	01–	23+	23–	45+	45–	67+	67–	G+	G–
0*	0	0	0	0	IN+	IN–								REF+	REF–								
0	0	0	0	1			IN+	IN–								REF+	REF–						
0	0	0	1	0					IN+	IN–								REF+	REF–				
0	0	0	1	1							IN+	IN–								REF+	REF–		
0	1	0	0	0	IN–	IN+								REF+	REF–								
0	1	0	0	1			IN–	IN+								REF+	REF–						
0	1	0	1	0					IN–	IN+								REF+	REF–				
0	1	0	1	1							IN–	IN+								REF+	REF–		
1	0	0	0	0	IN+								IN–	REF+	REF–								
1	0	0	0	1			IN+						IN–			REF+	REF–						
1	0	0	1	0					IN+				IN–					REF+	REF–				
1	0	0	1	1							IN+		IN–							REF+	REF–		
1	1	0	0	0		IN+							IN–	REF+	REF–								
1	1	0	0	1				IN+					IN–			REF+	REF–						
1	1	0	1	0						IN+			IN–					REF+	REF–				
1	1	0	1	1								IN+	IN–							REF+	REF–		
0	0	1	0	0	IN+	IN–																REF+	REF–
0	0	1	0	1			IN+	IN–														REF+	REF–
0	0	1	1	0					IN+	IN–												REF+	REF–
0	0	1	1	1							IN+	IN–										REF+	REF–
0	1	1	0	0	IN–	IN+																REF+	REF–
0	1	1	0	1			IN–	IN+														REF+	REF–
0	1	1	1	0					IN–	IN+												REF+	REF–
0	1	1	1	1							IN–	IN+										REF+	REF–
1	0	1	0	0	IN+								IN–									REF+	REF–
1	0	1	0	1			IN+						IN–									REF+	REF–
1	0	1	1	0					IN+				IN–									REF+	REF–
1	0	1	1	1							IN+		IN–									REF+	REF–
1	1	1	0	0		IN+							IN–									REF+	REF–
1	1	1	0	1				IN+					IN–									REF+	REF–
1	1	1	1	0						IN+			IN–									REF+	REF–
1	1	1	1	1								IN+	IN–									REF+	REF–

*Default at power up

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Table 4. LTC2446/LTC2447 Speed/Resolution Selection

OSR3	OSR2	OSR1	OSR0	TWOX	RMS NOISE LTC2446	RMS NOISE LTC2447	ENOB LTC2446	ENOB LTC2447	OSR	LATENCY
0	0	0	0	0	Keep Previous Speed/Resolution					
0	0	0	1	0	23µV	23µV	17	17	64	None
0	0	1	0	0	4.4µV	3.5µV	20.1	20.1	128	None
0	0	1	1	0	2.8µV	2µV	20.8	21.3	256	None
0	1	0	0	0	2µV	1.4µV	21.3	21.8	512	None
0	1	0	1	0	1.4µV	1µV	21.8	22.4	1024	None
0	1	1	0	0	1.1µV	750nV	22.1	22.9	2048	None
0	1	1	1	0	720nV	510nV	22.7	23.4	4096	None
1	0	0	0	0	530nV	375nV	23.2	24	8192	None
1	0	0	1	0	350nV	250nV	23.8	24.4	16384	None
1	1	1	1	0	280nV	200nV	24.1	24.6	32768	none
0	0	0	0	1	Keep Previous Speed/Resolution					
0	0	0	1	1	23µV	23µV	17	17	64	1 Cycle
0	0	1	0	1	4.4µV	3.5µV	20.1	20.1	128	1 Cycle
0	0	1	1	1	2.8µV	2µV	20.8	21.3	256	1 Cycle
0	1	0	0	1	2µV	1.4µV	21.3	21.8	512	1 Cycle
0	1	0	1	1	1.4µV	1µV	21.8	22.4	1024	1 Cycle
0	1	1	0	1	1.1µV	750nV	22.1	22.9	2048	1 Cycle
0	1	1	1	1	720nV	510nV	22.7	23.4	4096	1 Cycle
1	0	0	0	1	530nV	375nV	23.2	24	8192	1 Cycle
1	0	0	1	1	350nV	250nV	23.8	24.4	16384	1 Cycle
1	1	1	1	1	280nV	200nV	24.1	24.6	32768	1 Cycle

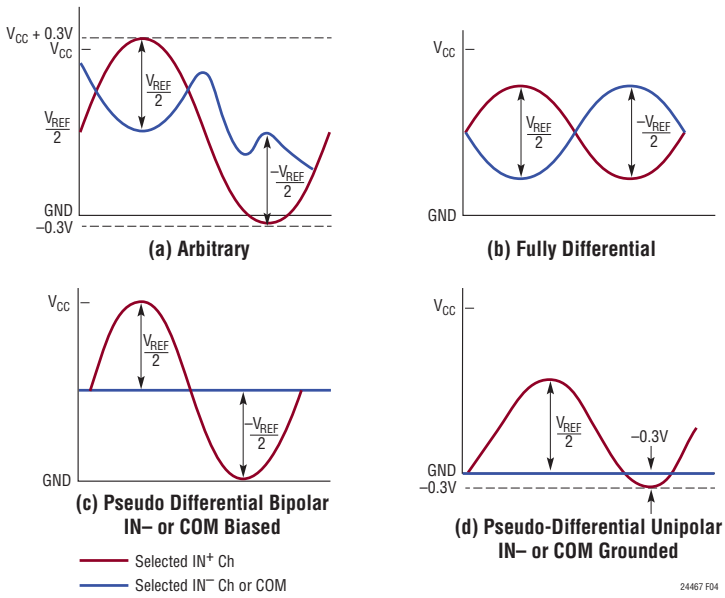

Figure 4. Input Range

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Speed Multiplier Mode

In addition to selecting the speed/resolution, a speed multiplier mode is used to double the output rate while maintaining the selected resolution. The last bit of the 5-bit speed/resolution control word (TWOX, see Table 4) determines if the output rate is 1× (no speed increase) or 2× (double the selected speed).

While operating in the 1× mode, the device combines two internal conversions for each conversion result in order to remove the ADC offset. Every conversion cycle, the offset and offset drift are transparently calibrated greatly simplifying the user interface. The conversion result has no latency. The first conversion following a newly selected speed/resolution and/or input/reference is valid. This is identical to the operation of the LTC2440, LTC2444, LTC2445, LTC2448, LTC2449, LTC2414 and LTC2418.

While operating in the 2× mode, the device performs a running average of the last two conversion results. This automatically removes the offset and drift of the device while increasing the output rate by 2×. The resolution (noise) remains the same as the 1× mode. If a new channel/reference is selected, the conversion result is valid for all conversions after the first conversion (one cycle latency). If a new speed/resolution is selected, the first conversion result is valid but the resolution (noise) is a function of the running average. All subsequent conversion results are valid. If the mode is changed from either 1× to 2× or 2× to 1× without changing the resolution or channel, the first conversion result is valid.

If an external buffer/amplifier circuit is used for the LTC2447, the 2× mode can be used to increase the settling time of the amplifier between readings. While operating in the 2× mode, the multiplexer output (input to the external buffer/amplifier) is switched at the end of each conversion cycle. Prior to concluding the data out/in cycle, the analog multiplexer output is switched. This occurs at the end of the conversion cycle (just prior to the data output cycle) for auto calibration. The time required to read the conversion enables more settling time for the external buffer/amplifier. The offset/offset drift of the external amplifiers are automatically removed by the converter's auto calibration sequence for both the 1× and 2× speed modes.

While operating in the 1× mode, if a new input channel/reference is selected the multiplexer is switched on the falling edge of the 14th SCK (once the complete data input word is programmed). The remaining data output sequence time can be used to allow the external buffer/amplifier to settle.

BUSY

The BUSY output (Pin 2) is used to monitor the state of conversion, data output and sleep cycle. While the part is converting, the BUSY pin is HIGH. Once the conversion is complete, BUSY goes LOW indicating the conversion is complete and data out is ready. The part now enters the LOW power sleep state. BUSY remains LOW while data is shifted out of the device and SDI is shifted into the device. It goes HIGH at the conclusion of the data input/output cycle indicating a new conversion has begun. This rising edge may be used to flag the completion of the data read cycle.

SERIAL INTERFACE TIMING MODES

The LTC2446/LTC2447's 3- or 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle conversion and autostart. The following sections describe each of these serial interface timing modes in detail. In all these cases, the converter can use the internal oscillator (F_O = LOW) or an external oscillator connected to the F_O pin. Refer to Table 5 for a summary.

Table 5. LTC2446/LTC2447 Interface Timing Modes

CONFIGURATION	SCK SOURCE	CONVERSION CYCLE CONTROL	DATA OUTPUT CONTROL	CONNECTION AND WAVEFORMS
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 4, 5
External SCK, 3-Wire I/O	External	SCK	SCK	Figure 6
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}$ ↓	$\overline{CS}$ ↓	Figures 7, 8
Internal SCK, 3-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 9

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External Serial Clock, Single Cycle Operation (SPI/MICROWIRE Compatible)

This timing mode uses an external serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 5.

The serial clock mode is selected by the EXT pin. To select the external serial clock mode, EXT must be tied low.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is pulled LOW, $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 (BUSY = 1) while a conversion is in progress and $\overline{EOC}$ = 0 (BUSY = 0) if the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the low power sleep state once the conversion is complete.

When the device is in the sleep state ($\overline{EOC}$ = 0), its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen. Data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion. SDO goes HIGH ($\overline{EOC}$ = 1) and BUSY goes HIGH indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt. Alternatively, $\overline{CS}$ may be driven HIGH setting SDO to Hi-Z and BUSY monitored for the completion of a conversion.

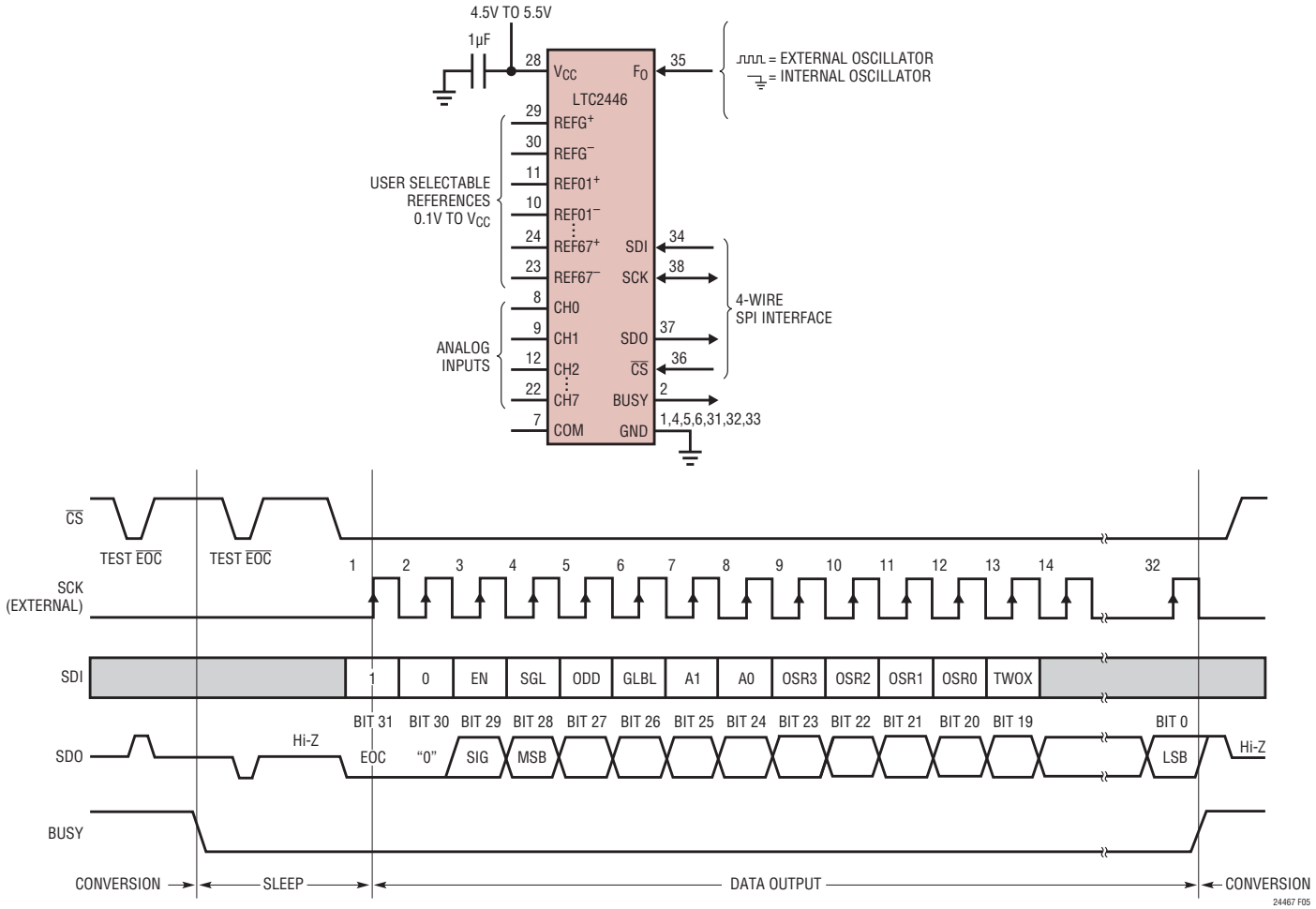

Figure 5. External Serial Clock, Single Cycle Operation

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As described above, $\overline{CS}$ may be pulled LOW at any time in order to monitor the conversion status on the SDO pin.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the fifth falling edge and the 32nd falling edge of SCK, see Figure 6. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. Thirteen serial input data bits are required in order to properly program the speed/resolution and input/reference channel. If the data output sequence is aborted prior to the 13th rising edge of SCK, the new input data is ignored, and the previously selected speed/resolution and channel are used for the next conversion cycle. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle or synchronizing the start of a conversion. If a new channel is being programmed, the rising edge of $\overline{CS}$ must come after the 14th falling edge of SCK in order to store the data input sequence.

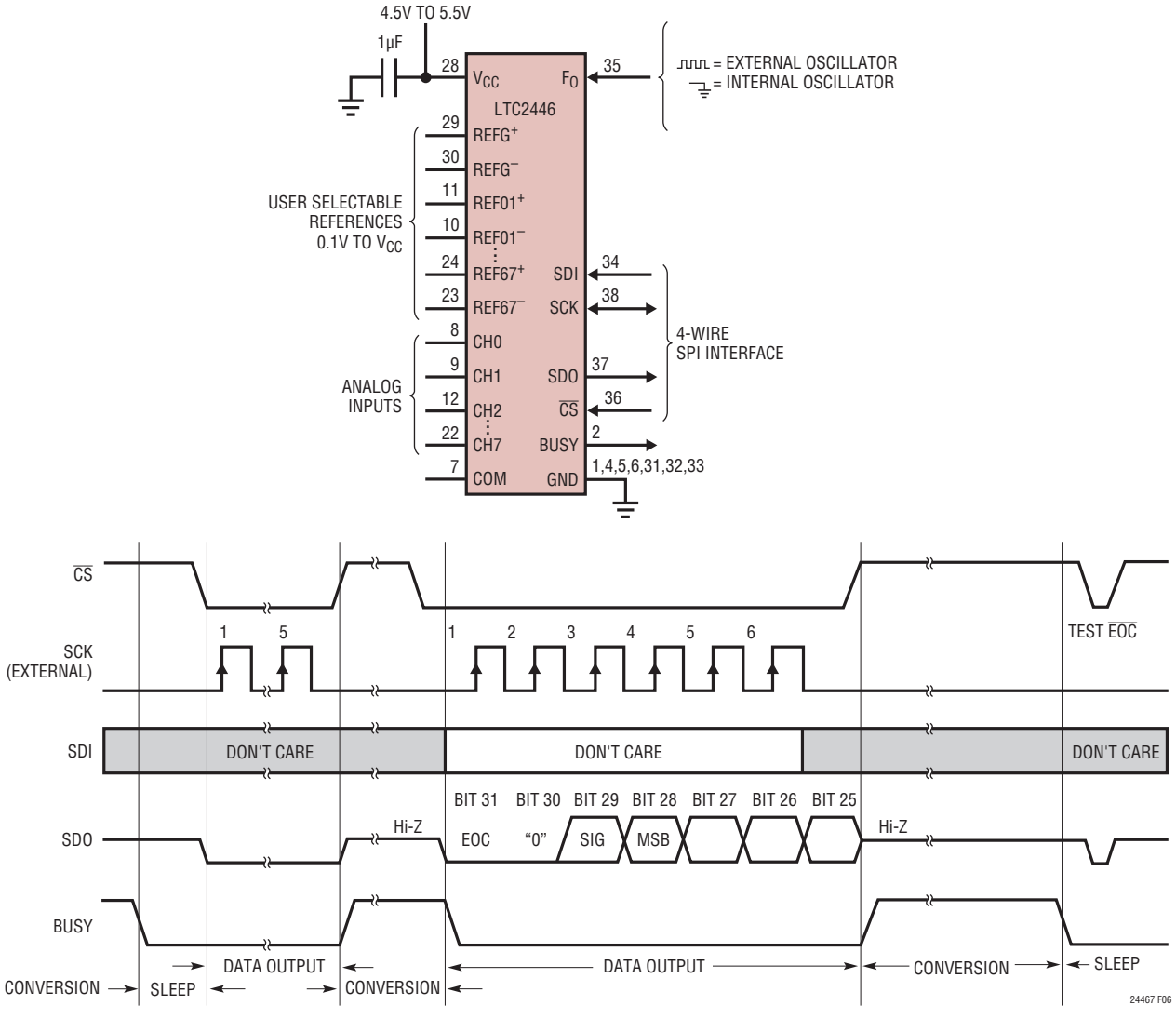

Figure 6. External Serial Clock, Reduced Output Data Length

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External Serial Clock, 3-Wire I/O

This timing mode utilizes a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal, see Figure 6. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier. The external serial clock mode is selected by tying $\overline{EXT}$ LOW.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. Conversely, BUSY (Pin 2) may be used to monitor the status of the conversion cycle. $\overline{EOC}$ or BUSY may be used as an interrupt to an external controller indicating the conversion result is ready. $\overline{EOC}$ = 1 (BUSY = 1) while the conversion is in progress and $\overline{EOC}$ = 0 (BUSY = 0) once the conversion enters the low power sleep state. On the falling edge of $\overline{EOC}$/BUSY, the conversion result is loaded into an internal static shift register. The device remains in the sleep state until the first rising edge of SCK. Data is shifted out the SDO pin on each falling edge of SCK enabling external circuitry to latch data on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK. On the 32nd falling edge of SCK, SDO and BUSY go HIGH ($\overline{EOC}$ = 1) indicating a new conversion has begun.

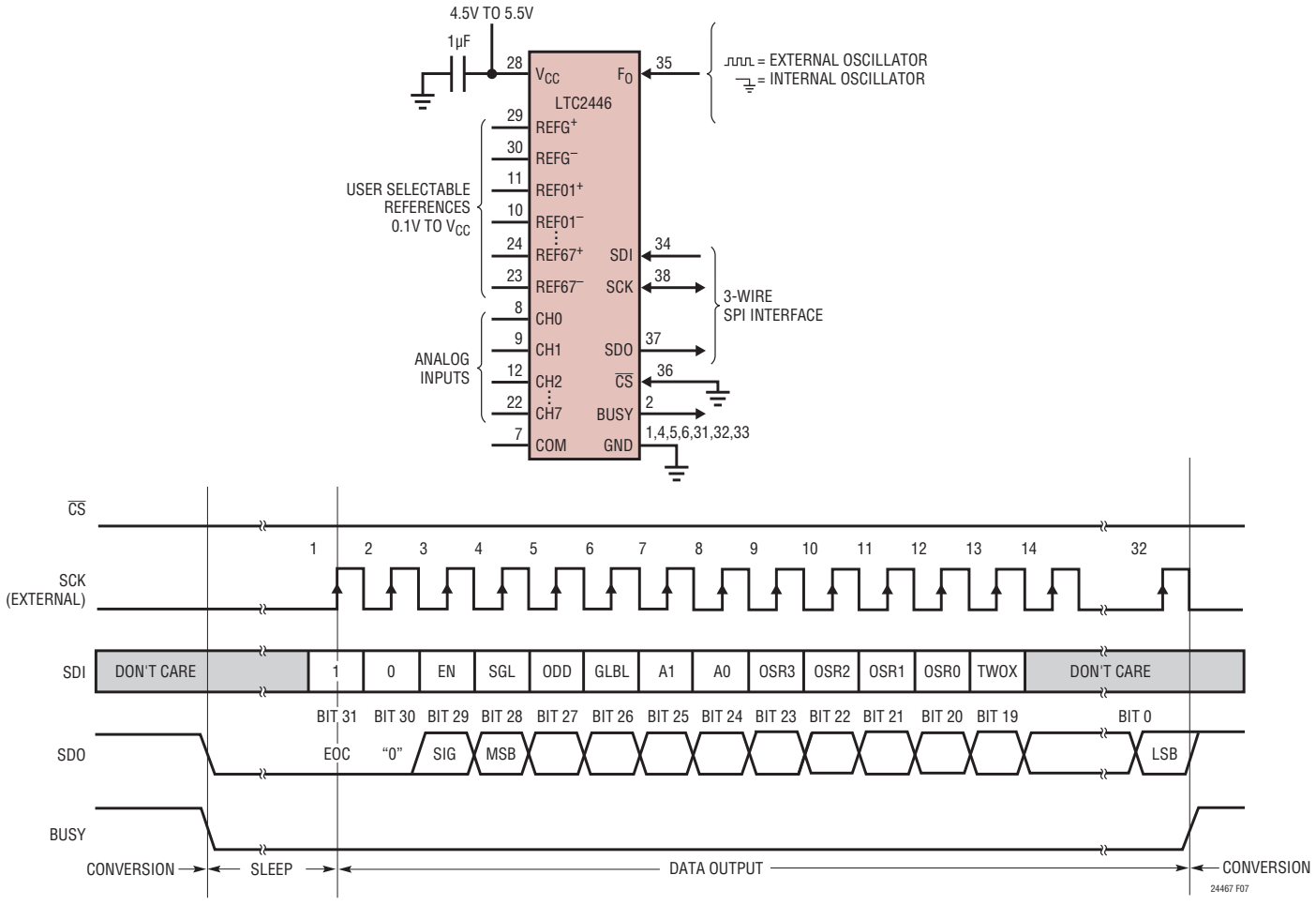

Figure 7. External Serial Clock, $\overline{CS}$ = 0 Operation (3-Wire)

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Internal Serial Clock, Single Cycle Operation

This timing mode uses an internal serial clock to shift out the conversion result and a $\overline{CS}$ signal to monitor and control the state of the conversion cycle, see Figure 8.

In order to select the internal serial clock timing mode, the $\overline{EXT}$ pin must be tied HIGH.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state. Alternatively, BUSY (Pin 2) may be used to monitor the status of the conversion in progress. BUSY is HIGH during the conversion and goes LOW at the conclusion. It remains LOW until the result is read from the device.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit the sleep state and enter the data output state if $\overline{CS}$ remains LOW. In order to prevent the device from exiting the low power sleep state, $\overline{CS}$ must be pulled HIGH before the first rising edge of SCK. In the internal SCK timing mode, SCK goes HIGH and the device begins outputting data at time $t_{EOCtest}$ after the falling edge of $\overline{CS}$ (if $\overline{EOC}$ = 0) or $t_{EOCtest}$ after $\overline{EOC}$ goes LOW (if $\overline{CS}$ is LOW during the falling edge of $\overline{EOC}$). The value of $t_{EOCtest}$ is 500ns. If $\overline{CS}$ is pulled HIGH before time $t_{EOCtest}$, the device remains in the sleep state. The conversion result is held in the internal static shift register.

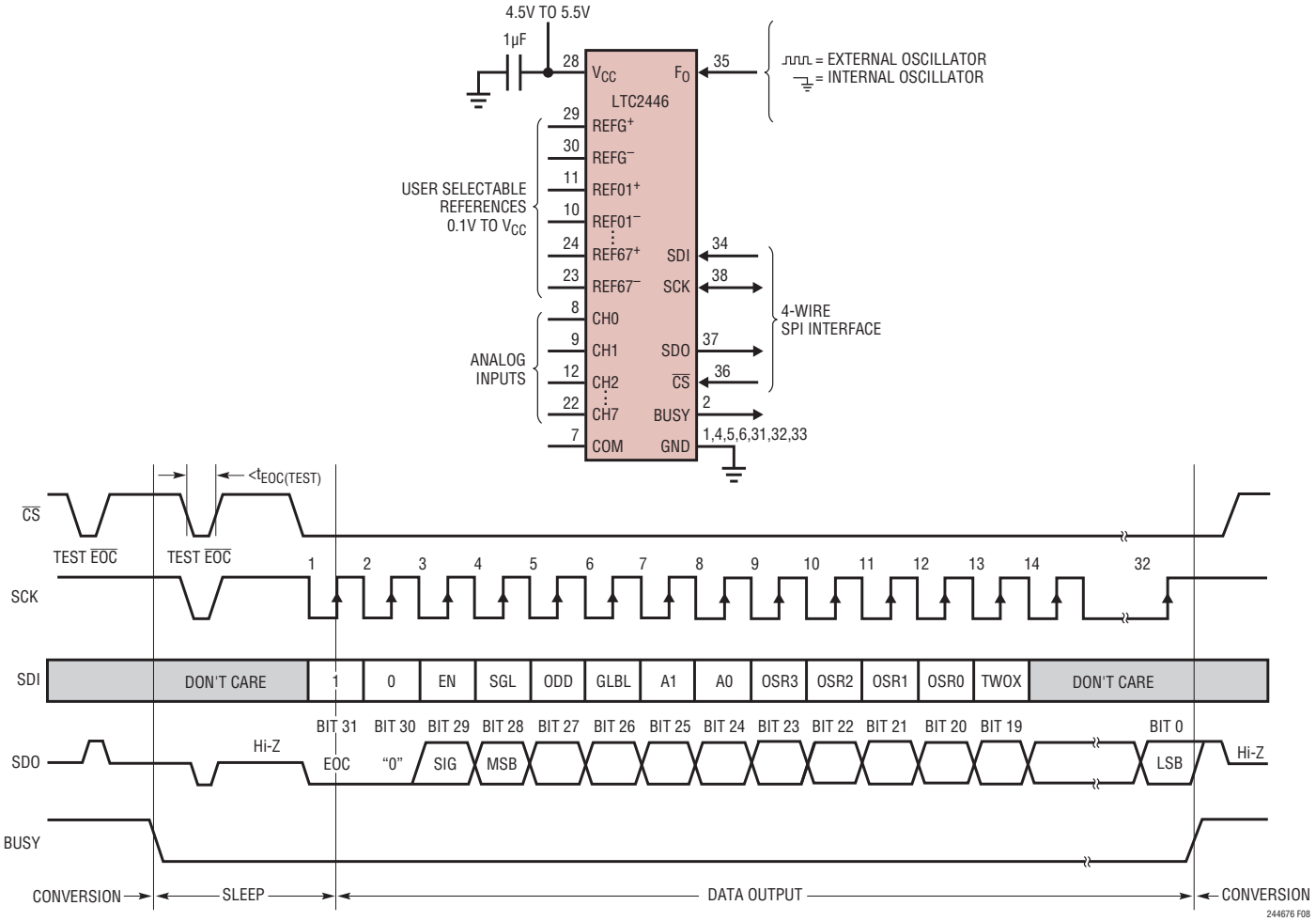

Figure 8. Internal Serial Clock, Single Cycle Operation

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If $\overline{CS}$ remains LOW longer than $t_{EOCtest}$, the first rising edge of SCK will occur and the conversion result is serially shifted out of the SDO pin. The data output cycle begins on this first rising edge of SCK and concludes after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1), SCK stays HIGH and a new conversion starts.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH anytime between the first and 32nd rising edge of SCK, see Figure 9. On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. This is useful for systems not requiring all 32 bits of output data, aborting an invalid conversion cycle, or synchronizing the start of a conversion. Thirteen serial input data bits are required in order to properly program the speed/resolution and input channel. If the data output sequence is aborted prior to the 13th rising edge of SCK, the new input data is ignored, and the previously selected speed/resolution and channel are used for the next conversion cycle. If a new channel is being programmed, the rising edge of $\overline{CS}$ must come after the 14th falling edge of SCK in order to store the data input sequence.

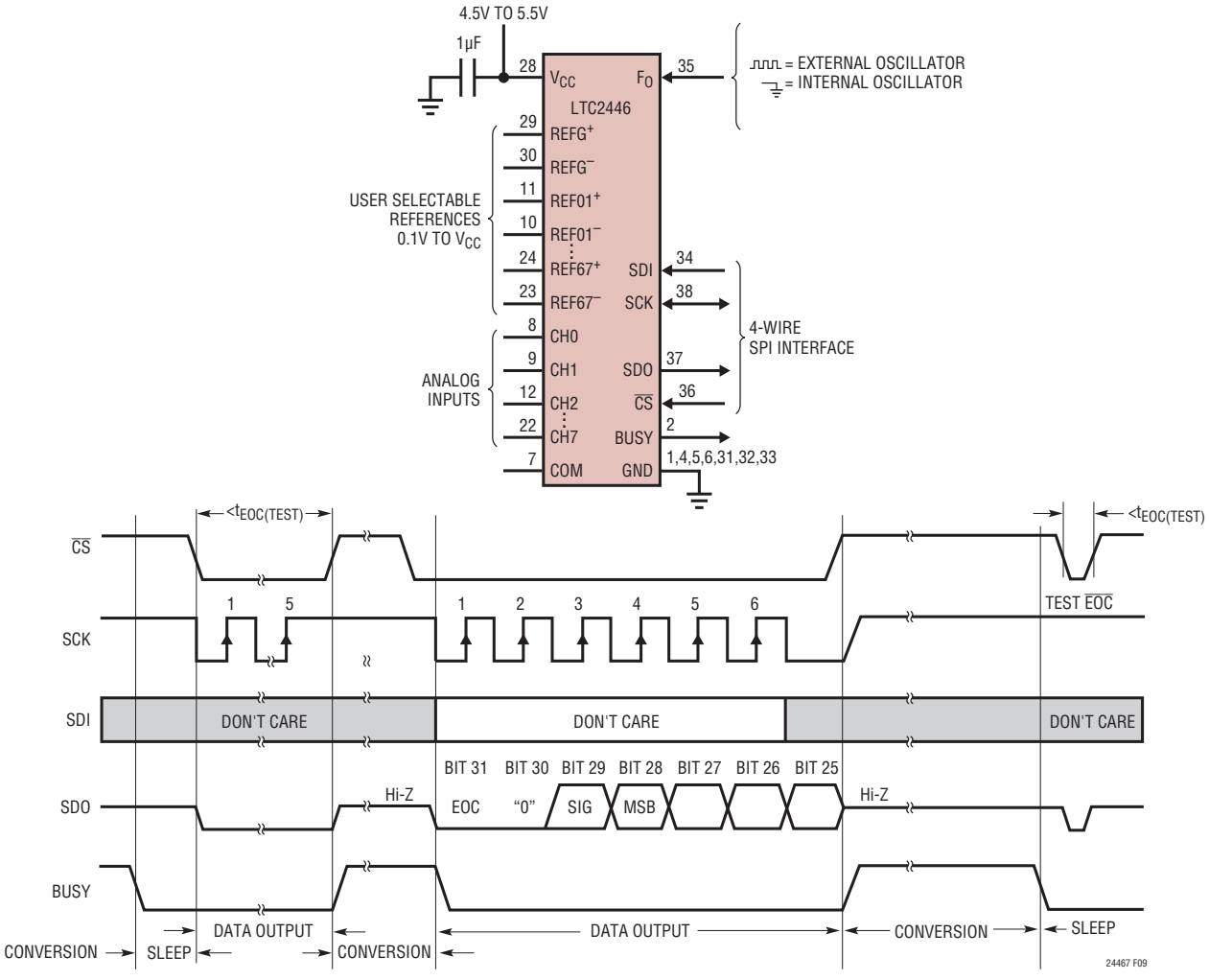

Figure 9. Internal Serial Clock, Reduced Data Output Length

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Internal Serial Clock, 3-Wire I/O, Continuous Conversion

This timing mode uses a 3-wire, all output (SCK and SDO) interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal, see Figure 10. $\overline{CS}$ may be permanently tied to ground, simplifying the user interface or isolation barrier. The internal serial clock mode is selected by tying $\overline{EXT}$ HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1) and BUSY = 1. Once the conversion is complete, SCK, BUSY and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the low power sleep state. The part remains in the sleep state a minimum amount of time (≈500ns) then immediately begins outputting data. The data output cycle begins on the first rising edge of SCK and ends after the 32nd rising edge. Data is shifted out the SDO pin on each falling edge of SCK. The internally generated serial clock is output to the SCK pin. This signal may be used to shift the conversion result into external circuitry. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. After the 32nd rising edge, SDO goes HIGH ($\overline{EOC}$ = 1) indicating a new conversion is in progress. SCK remains HIGH during the conversion.

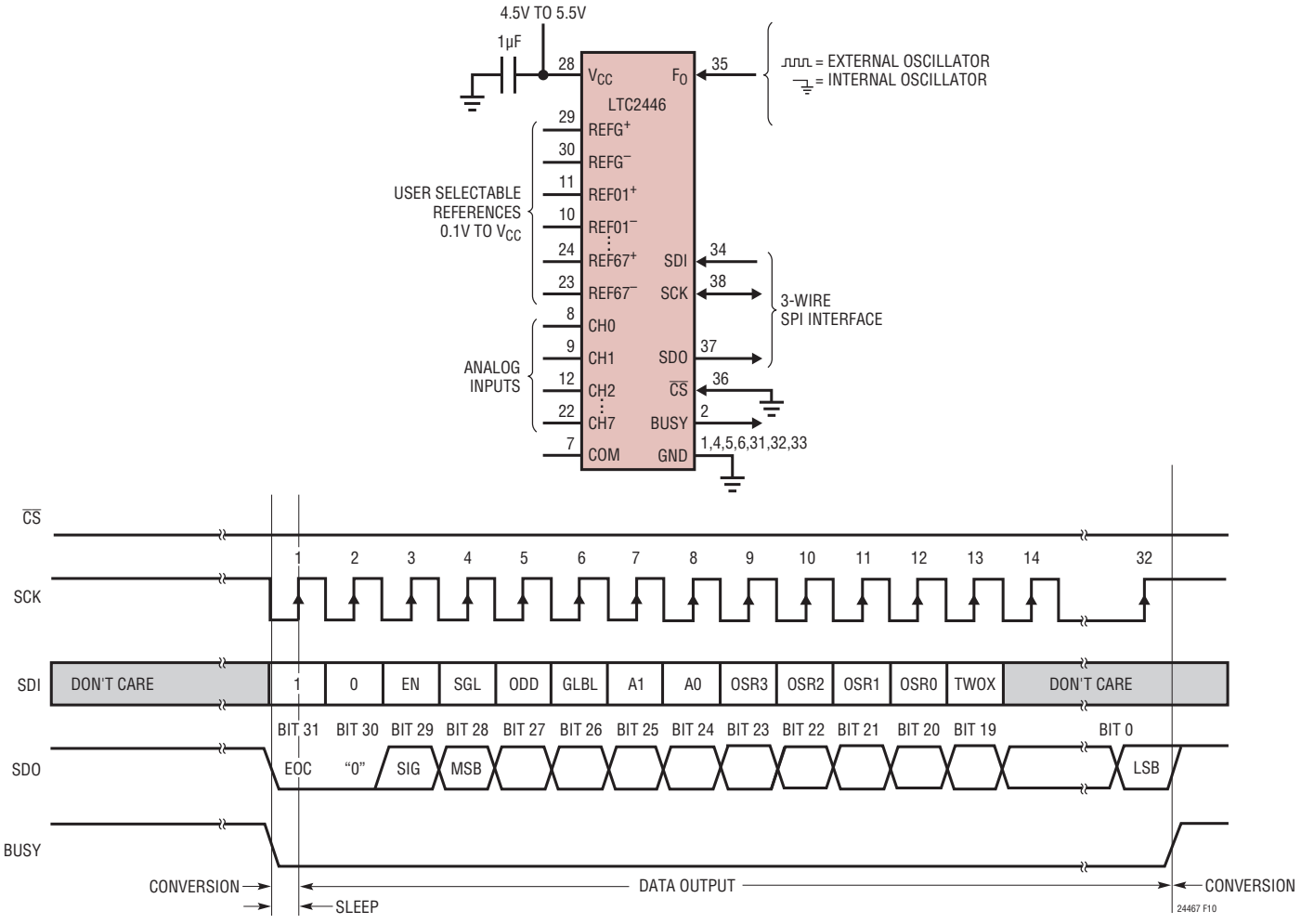

Figure 10. Internal Serial Clock, Continuous Operation

APPLICATIONS INFORMATION

Normal Mode Rejection and Anti-aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversampling ratio, the LTC2446/LTC2447 significantly simplify anti-aliasing filter requirements.

The LTC2446/LTC2447's speed/resolution is determined by the over sample ratio (OSR) of the on-chip digital filter. The OSR ranges from 64 for 3.5kHz output rate to 32,768 for 6.9Hz (in 1× mode) output rate. The value of OSR and the sample rate f_S determine the filter characteristics of the device. The first NULL of the digital filter is at f_N and multiples of f_N where $f_N = f_S/OSR$, see Figure 11 and Table 6. The rejection at the frequency f_N ±14% is better than 80dB, see Figure 12.

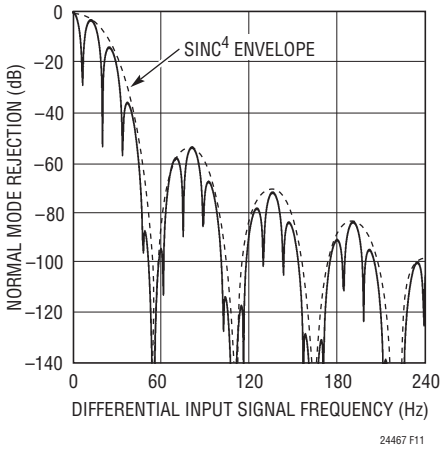

Figure 11. LTC2446/LTC2447 Normal Mode Rejection (Internal Oscillator)

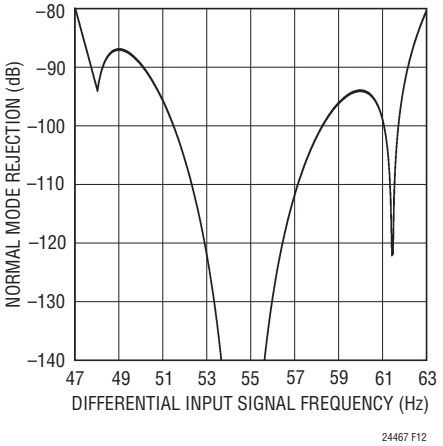

Figure 12. LTC2446/LTC2447 Normal Mode Rejection (Internal Oscillator)

Table 6. OSR vs Notch Frequency (f_N) (with Internal Oscillator)

OSR	NOTCH (f_N)
64	28.16kHz
128	14.08kHz
256	7.04kHz
512	3.52kHz
1024	1.76kHz
2048	880Hz
4096	440Hz
8192	220Hz
16384	110Hz
32768*	55Hz

*Simultaneous 50/60Hz rejection

If F_O is grounded, f_S is set by the on-chip oscillator at 1.8MHz (over supply and temperature variations). At an OSR of 32,768, the first NULL is at f_N = 55Hz and the no latency output rate is $f_N/8$ = 6.9Hz. At the maximum OSR, the noise performance of the device is 280nV$_{RMS}$ (LTC2446) and 200nV$_{RMS}$ (LTC2447) with better than 80dB rejection of 50Hz ±2% and 60Hz ±2%. Since the OSR is large (32,768) the wide band rejection is extremely large and the anti-aliasing requirements are simple. The first multiple of f_S occurs at 55Hz • 32,768 = 1.8MHz, see Figure 13.

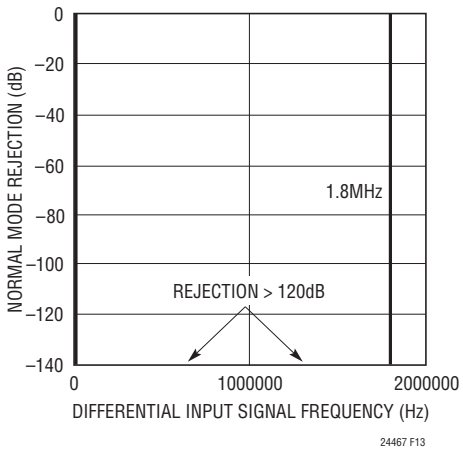

Figure 13. LTC2446/LTC2447 Normal Mode Rejection (Internal Oscillator)

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The first NULL becomes f_N = 7.04kHz with an OSR of 256 (an output rate of 880Hz) and F_O grounded. While the NULL has shifted, the sample rate remains constant. As a result of constant modulator sampling rate, the linearity, offset and full-scale performance remain unchanged as does the first multiple of f_S.

The sample rate f_S and NULL f_N, may also be adjusted by driving the F_O pin with an external oscillator. The sample rate is $f_S = f_{EOSC}/5$, where f_{EOSC} is the frequency of the clock applied to F_O. Combining a large OSR with a reduced sample rate leads to notch frequencies fN near DC while maintaining simple anti-aliasing requirements. A 100kHz clock applied to F_O results in a NULL at 0.6Hz plus all harmonics up to 20kHz, see Figure 14. This is useful in applications requiring digitalization of the DC component of a noisy input signal and eliminates the need of placing a 0.6Hz filter in front of the ADC.

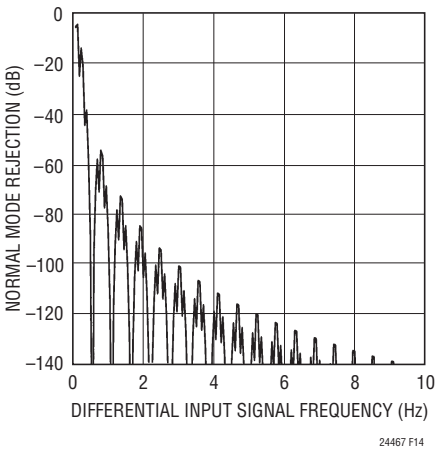

Figure 14. LTC2446/LTC2447 Normal Mode Rejection (External Oscillator at 90kHz)

An external oscillator operating from 100kHz to 12MHz can be implemented using the LTC1799 (resistor set SOT-23 oscillator), see Figure 15. By floating pin 4 (DIV) of the LTC1799, the output oscillator frequency is:

$$f_{OSC} = 10MHz \bullet \left(\frac{10k}{10 \bullet R_{SET}} \right)$$

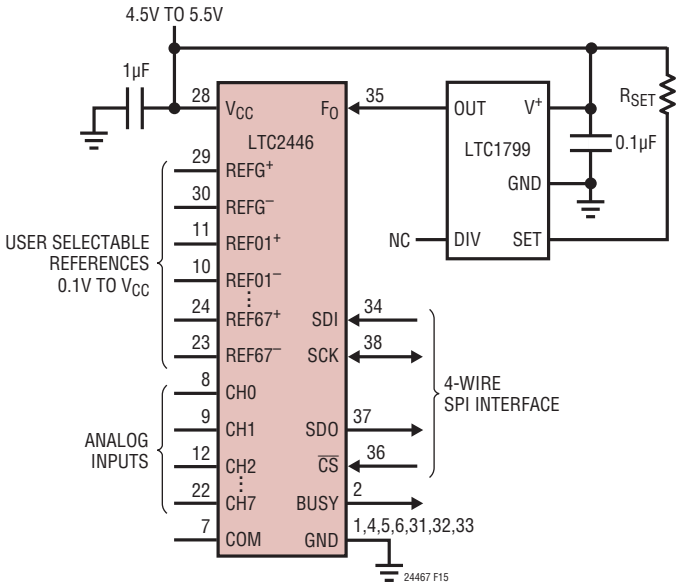

Figure 15. Simple External Clock Source

The normal mode rejection characteristic shown in Figure 14 is achieved by applying the output of the LTC1799 (with R_{SET} = 100k) to the F_O pin on the LTC2446/LTC2447 with SDI tied HIGH (OSR = 32768).

Multiple Ratiometric and Absolute Measurements

The LTC2446/LTC2447 combine a high precision, high speed delta-sigma converter with a versatile front-end multiplexer. The unique no latency architecture allows seamless changes in both input channel and reference while the absolute accuracy ensures excellent matching between both analog input channels and reference channels. Any set of inputs (differential or single-ended) can perform a conversion with one of two references. For Bridges, RTDs and other ratiometric devices, each set of channels can perform a conversion with respect to a unique reference voltage. For Thermocouples, voltage sense, current sense and other absolute sensors, each set of channels can perform a conversion with respect to a single global reference voltage (see Figure 16). This allows users to measure both multiple absolute and multiple ratio metric sensors with the same device in such applications as flow, gas chromatography, multiple RTDs or bridges, or universal data acquisition.

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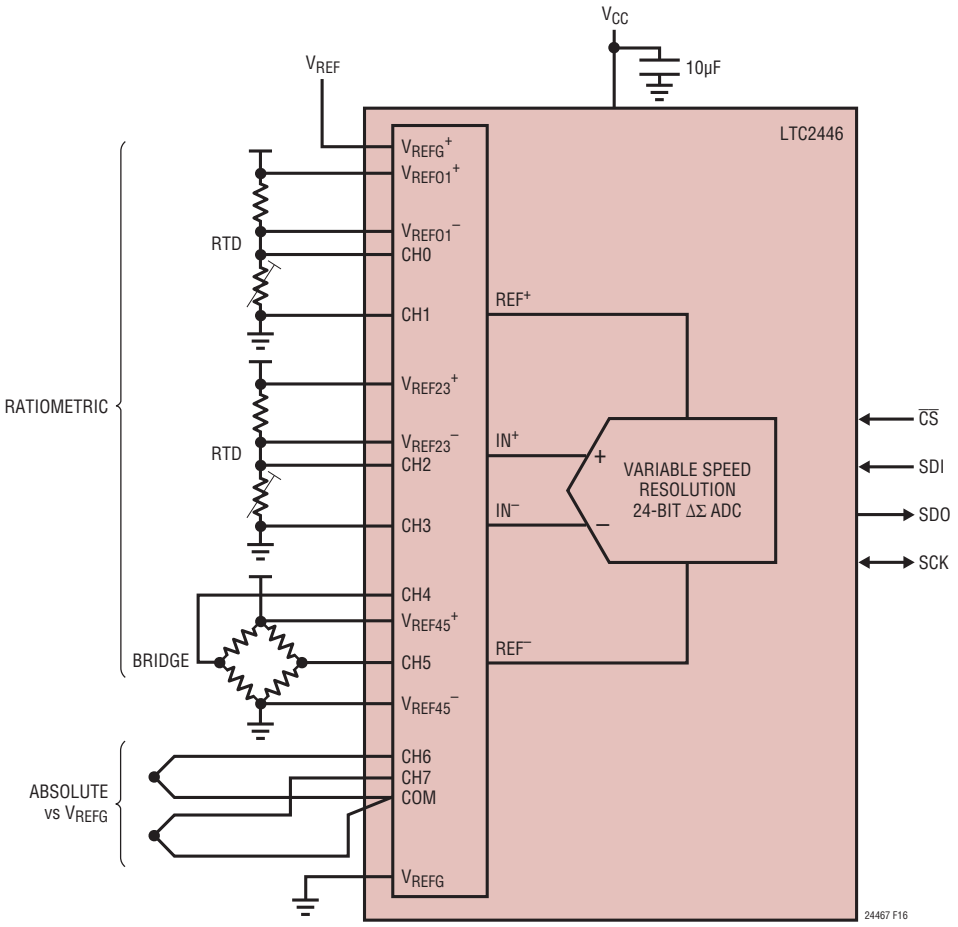

Figure 16. Versatile 4-Way Multiplexer Measures Multiple Ratiometric/Absolute Sensors

Average Input Current

The LTC2446 switches the input and reference to a 2pF capacitor at a frequency of 1.8MHz. A simplified equivalent circuit is shown in Figure 17. The sample capacitor for the LTC2447 is 4pF, and its average input current is externally buffered from the input source.

The average input and reference currents can be expressed in terms of the equivalent input resistance of the sample capacitor, where: Req = $1/(f_{SW} \bullet C_{EQ})$.

When using the internal oscillator, f_{SW} is 1.8MHz and the equivalent resistance is approximately 110kΩ.

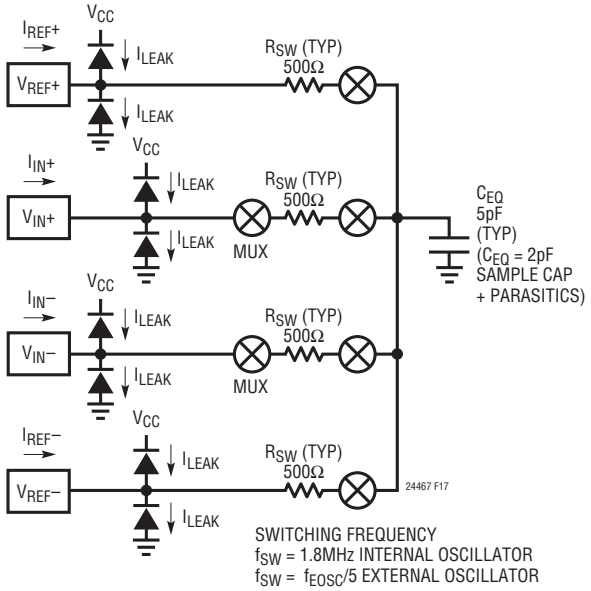

Figure 17. LTC2446 Input Structure

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Input Bandwidth and Frequency Rejection

The combined effect of the internal SINC^4 digital filter and the digital and analog auto-calibration circuits determines the LTC2446/LTC2447 input bandwidth and rejection characteristics. The digital filter's response can be adjusted by setting the oversample ratio (OSR) through the SPI interface or by supplying an external conversion clock to the F_O pin.

Table 7 lists the properties of the LTC2446/LTC2447 with various combinations of oversample ratio and clock frequency. Understanding these properties is the key to fine tuning the characteristics of the LTC2446/LTC2447 to the application.

Maximum Conversion Rate

The maximum conversion rate is the fastest possible rate at which conversions can be performed.

First Notch Frequency

This is the first notch in the SINC^4 portion of the digital filter and depends on the F_O clock frequency and the oversample ratio. Rejection at this frequency and its multiples (up to the modulator sample rate of 1.8MHz) exceeds 120dB. This is 8 times the maximum conversion rate.

Effective Noise Bandwidth

The LTC2446/LTC2447 has extremely good input noise rejection from the first notch frequency all the way out to the modulator sample rate (typically 1.8MHz). Effective noise bandwidth is a measure of how the ADC will reject wideband input noise up to the modulator sample rate. The example on the following page shows how the noise rejection of the LTC2446/LTC2447 reduces the effective noise of an amplifier driving its input.

Example:
If an amplifier (e.g. LT1219) driving the input of an LTC2446/LTC2447 has wideband noise of 33nV/$\sqrt{Hz}$, band-limited to 1.8MHz, the total noise entering the ADC input is:

$$33nV/\sqrt{Hz} \bullet \sqrt{1.8MHz} = 44.3\mu V.$$

When the ADC digitizes the input, its digital filter rejects the wideband noise from the input signal. The noise reduction depends on the oversample ratio which defines the effective bandwidth of the digital filter.

At an oversample of 256, the noise bandwidth of the ADC is 787Hz which reduces the total amplifier noise to:

$$33nV/\sqrt{Hz} \bullet \sqrt{787Hz} = 0.93\mu V.$$

Table 7. Performance vs Oversample Ratio

Over-sample Ratio (OSR)	*RMS Noise LTC2446	*RMS Noise LTC2447	ENOB (V_{REF} = 5V)		Maximum Conversion Rate (sps)			First Notch Frequency (Hz)		Effective Noise BW (Hz)		–3dB Point (Hz)	
			LTC2446	LTC2447	Internal Clock	External f_O (1× Mode) (f_O/x)	External f_O (2× Mode) (f_O/x)	Internal Clock	External f_O (f_O/x)	Internal 9MHz Clock	External f_O (f_O/x)	Internal Clock	External f_O (f_O/x)
64	23µV	23µV	17	17	2816.35	f_O/2738	f_O/1458	28125	f_O/320	3148	f_O/2860	1696	f_O/5310
128	4.5µV	3.5µV	20.1	20	1455.49	f_O/5298	f_O/2738	14062.5	f_O/640	1574	f_O/5720	848	f_O/10600
256	2.8µV	2µV	20.8	21.3	740.18	f_O/10418	f_O/5298	7031.3	f_O/1280	787	f_O/11440	424	f_O/21200
512	2µV	1.4µV	21.3	21.8	373.28	f_O/20658	f_O/10418	3515.6	f_O/2560	394	f_O/22840	212	f_O/42500
1024	1.4µV	1µV	21.8	22.4	187.45	f_O/41138	f_O/20658	1757.8	f_O/5120	197	f_O/45690	106	f_O/84900
2048	1.1µV	750nV	22.1	22.9	93.93	f_O/82098	f_O/41138	878.9	f_O/10200	98.4	f_O/91460	53	f_O/170000
4096	720nV	510nV	22.7	23.4	47.01	f_O/164018	f_O/82098	439.5	f_O/20500	49.2	f_O/183000	26.5	f_O/340000
8192	530nV	375nV	23.2	24	23.52	f_O/327858	f_O/164018	219.7	f_O/41000	24.6	f_O/366000	13.2	f_O/679000
16384	350nV	250nV	23.8	24.4	11.76	f_O/655538	f_O/327858	109.9	f_O/81900	12.4	f_O/731000	6.6	f_O/1358000
32768	280nV	200nV	24.1	24.6	5.88	f_O/1310898	f_O/655538	54.9	f_O/163800	6.2	f_O/1463000	3.3	f_O/2717000

*ADC noise increases by approximately $\sqrt{2}$ when OSR is decreased by a factor of 2 for OSR 32768 to OSR 256. The ADC noise at OSR 128 and OSR 64 include effects from internal modulator quantization noise.

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The total noise is the RMS sum of this noise with the 2µV noise of the ADC at OSR = 256.

$$\sqrt{(0.93\mu V)^2 + (2\mu V)^2} = 2.2\mu V.$$

Increasing the oversample ratio to 32768 reduces the noise bandwidth of the ADC to 6.2Hz which reduces the total amplifier noise to:

$$33nV/\sqrt{Hz} \bullet \sqrt{6.2Hz} = 82nV.$$

The total noise is the RMS sum of this noise with the 200nV noise of the ADC at OSR = 32768.

$$\sqrt{(82nV)^2 + (200nV)^2} = 216nV.$$

In this way, the digital filter with its variable oversampling ratio can greatly reduce the effects of external noise sources.

Automatic Offset Calibration of External Buffers/Amplifiers

The LTC2447 enables an external amplifier to be inserted between the multiplexer output and the ADC input. This enables one external buffer/amplifier circuit to be shared between all nine analog inputs (eight single-ended or four differential). The LTC2447 performs an internal offset calibration every conversion cycle in order to remove the offset and drift of the ADC. This calibration is performed through a combination of front end switching and digital processing. Since the external amplifier is placed between the multiplexer and the ADC, it is inside the correction loop. This results in automatic offset correction and offset drift removal of the external amplifier.

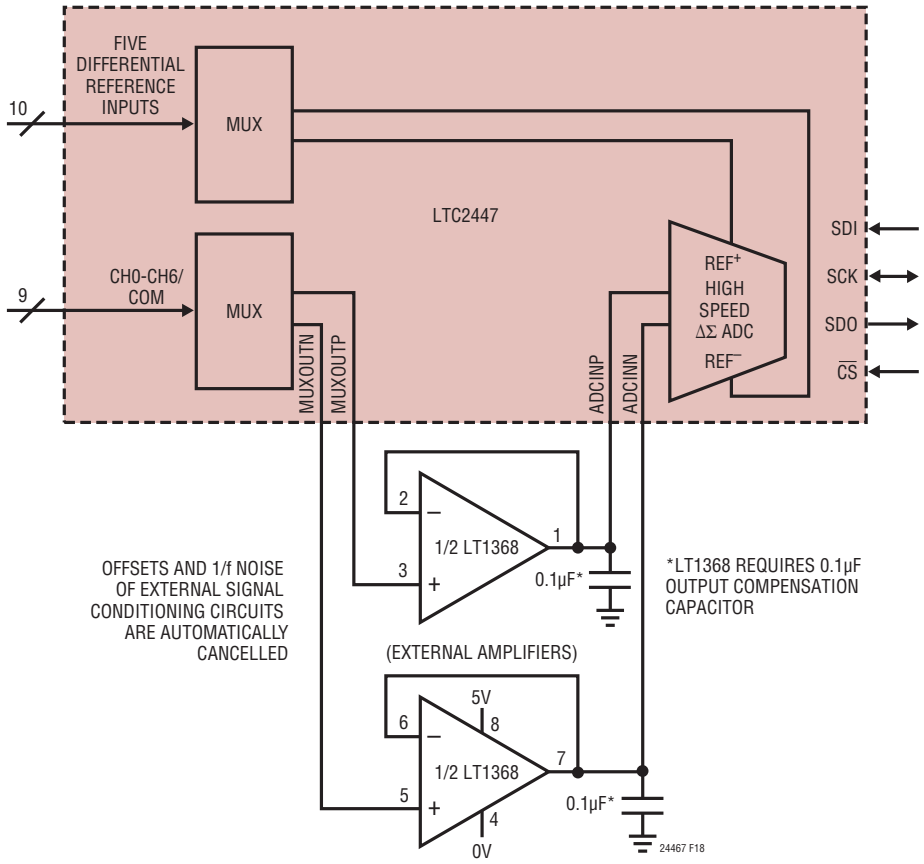

Figure 18. External Buffers Provide High Impedance Inputs and Amplifier Offsets are Cancelled