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# 16-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Input Current Cancellation

## FEATURES

- **Up to 2 Differential or 4 Single-Ended Inputs**
- **Easy Drive Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current**
- **Directly Digitizes High Impedance Sensors with Full Accuracy**
- **600nV RMS Noise (0.02LSB Transition Noise)**
- **GND to $V_{CC}$ Input/Reference Common Mode Range**
- Simultaneous 50Hz/60Hz Rejection
- 2ppm INL, No Missing Codes
- 1ppm Offset and 15ppm Full-Scale Error
- No Latency: Digital Filter Settles in a Single Cycle, Even After a New Channel is Selected
- Single Supply 2.7V to 5.5V Operation (0.8mW)
- Internal Oscillator
- Tiny 4mm × 3mm DFN Package

## APPLICATIONS

- Direct Sensor Digitizer
- Direct Temperature Measurement
- Instrumentation
- Industrial Process Control

## DESCRIPTION

The LTC®2488 is a 4-channel (2-channel differential), 16-bit, No Latency ΔΣ™ ADC with Easy Drive™ technology. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and rail-to-rail input signals to be directly digitized while maintaining exceptional DC accuracy.

The LTC2488 includes an integrated oscillator. This device can be configured to measure an external signal from combinations of 4 analog input channels operating in single ended or differential modes. It automatically rejects line frequencies of 50Hz and 60Hz simultaneously.

The LTC2488 allows a wide common mode, input range (0V to $V_{CC}$), independent of the reference voltage. Any combination of single-ended or differential inputs can be selected and the first conversion after a new channel selection is valid.

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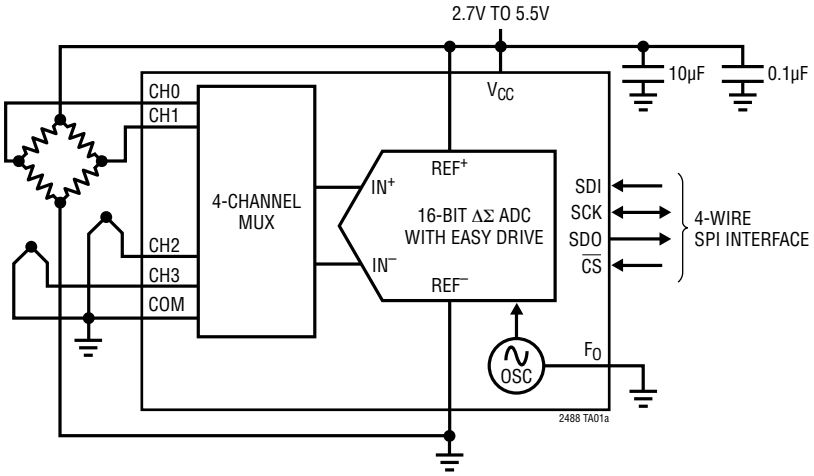
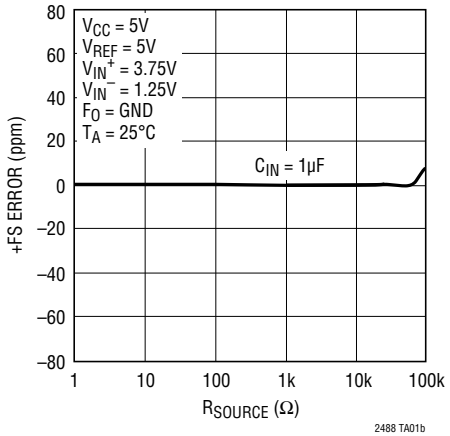
## TYPICAL APPLICATION

**Data Acquisition System**




**Fullscale Error vs Source Resistance**

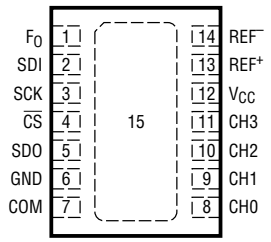


## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

Supply Voltage ($V_{CC}$) ..... –0.3V to 6V
Analog Input Voltage
(CH0 to CH3, COM).....–0.3V to ($V_{CC}$ + 0.3V)
$REF^+$, $REF^-$.....–0.3V to ($V_{CC}$ + 0.3V)
Digital Input Voltage.....–0.3V to ($V_{CC}$ + 0.3V)
Digital Output Voltage.....–0.3V to ($V_{CC}$ + 0.3V)
Operating Temperature Range
LTC2488C ..... 0°C to 70°C
LTC2488I ..... –40°C to 85°C
Storage Temperature Range ..... –65°C to 150°C

## PIN CONFIGURATION




DE PACKAGE
14-LEAD (4mm x 3mm) PLASTIC DFN

$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 37°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2488CDE#PBF | LTC2488CDE#TRPBF | 2488 | 14-Lead (4mm × 3mm) Plastic DFN | 0°C to 70°C |
| LTC2488IDE#PBF | LTC2488IDE#TRPBF | 2488 | 14-Lead (4mm × 3mm) Plastic DFN | –40°C to 85°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *Temperature grades are identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Notes 3, 4)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Resolution (No Missing Codes) | 0.1V ≤ $V_{REF}$ ≤ $V_{CC}$, –FS ≤ $V_{IN}$ ≤ +FS (Note 5) | | 16 | | | Bits |
| Integral Nonlinearity | 5V ≤ $V_{CC}$ ≤ 5.5V, $V_{REF}$ = 5V, $V_{IN(CM)}$ = 2.5V (Note 6)<br>2.7V ≤ $V_{CC}$ ≤ 5.5V, $V_{REF}$ = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6) | ●<br> | | 2<br>1 | 20<br> | ppm of $V_{REF}$<br>ppm of $V_{REF}$ |
| Offset Error | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 14) | ● | | 0.5 | 5 | µV |
| Offset Error Drift | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ | | | 10 | | nV/°C |
| Positive Full-Scale Error | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, $IN^+$ = 0.75$V_{REF}$, $IN^-$ = 0.25$V_{REF}$ | ● | | | 32 | ppm of $V_{REF}$ |
| Positive Full-Scale Error Drift | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, $IN^+$ = 0.75$V_{REF}$, $IN^-$ = 0.25$V_{REF}$ | | | 0.1 | | ppm of $V_{REF}$/°C |
| Negative Full-Scale Error | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, $IN^+$ = 0.25$V_{REF}$, $IN^-$ = 0.75$V_{REF}$ | ● | | | 32 | ppm of $V_{REF}$ |
| Negative Full-Scale Error Drift | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, $IN^+$ = 0.25$V_{REF}$, $IN^-$ = 0.75$V_{REF}$ | | | 0.1 | | ppm of $V_{REF}$/°C |
| Total Unadjusted Error | 5V ≤ $V_{CC}$ ≤ 5.5V, $V_{REF}$ = 2.5V, $V_{IN(CM)}$ = 1.25V<br>5V ≤ $V_{CC}$ ≤ 5.5V, $V_{REF}$ = 5V, $V_{IN(CM)}$ = 2.5V<br>2.7V ≤ $V_{CC}$ ≤ 5.5V, $V_{REF}$ = 2.5V, $V_{IN(CM)}$ = 1.25V | | | 15<br>15<br>15 | | ppm of $V_{REF}$<br>ppm of $V_{REF}$<br>ppm of $V_{REF}$ |
| Output Noise | 2.7V < $V_{CC}$ < 5.5V, 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$,<br>GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 13) | | | 0.6 | | $\mu V_{RMS}$ |

## CONVERTER CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Input Common Mode Rejection DC | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 5) | ● | 140 | | | dB |
| Input Common Mode Rejection 50Hz ±2% | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 5) | ● | 140 | | | dB |
| Input Common Mode Rejection 60Hz ±2% | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 5) | ● | 140 | | | dB |
| Input Normal Mode Rejection 50Hz ±2% | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Notes 5, 7) | ● | 110 | 120 | | dB |
| Input Normal Mode Rejection 60Hz ±2% | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Notes 5, 8) | ● | 110 | 120 | | dB |
| Input Normal Mode Rejection 50Hz/60Hz ±2% | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Notes 5, 9) | ● | 87 | | | dB |
| Reference Common Mode Rejection DC | 2.5V ≤ $V_{REF}$ ≤ $V_{CC}$, GND ≤ $IN^+$ = $IN^-$ ≤ $V_{CC}$ (Note 5) | ● | 120 | 140 | | dB |
| Power Supply Rejection DC | $V_{REF}$ = 2.5V, $IN^+$ = $IN^-$ = GND | | | 120 | | dB |
| Power Supply Rejection, 50Hz ±2% | $V_{REF}$ = 2.5V, $IN^+$ = $IN^-$ = GND (Notes 7, 9) | | | 120 | | dB |
| Power Supply Rejection, 60Hz ±2% | $V_{REF}$ = 2.5V, $IN^+$ = $IN^-$ = GND (Notes 8, 9) | | | 120 | | dB |

## ANALOG INPUT AND REFERENCE

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $IN^+$ | Absolute/Common Mode $IN^+$ Voltage ($IN^+$ Corresponds to the Selected Positive Input Channel) | | | GND – 0.3V | | $V_{CC}$ + 0.3V | V |
| $IN^-$ | Absolute/Common Mode $IN^-$ Voltage ($IN^-$ Corresponds to the Selected Negative Input Channel or COM) | | | GND – 0.3V | | $V_{CC}$ + 0.3V | V |
| $V_{IN}$ | Input Voltage Range ($IN^+$ – $IN^-$) | Differential/Single-Ended | ● | –FS | | +FS | V |
| FS | Full Scale of the Input ($IN^+$ – $IN^-$) | Differential/Single-Ended | ● | $0.5V_{REF}$ | | | V |
| LSB | Least Significant Bit of the Output Code | | ● | $FS/2^{16}$ | | | |
| $REF^+$ | Absolute/Common Mode $REF^+$ Voltage | | ● | 0.1 | | $V_{CC}$ | V |
| $REF^-$ | Absolute/Common Mode $REF^-$ Voltage | | ● | GND | | $REF^+$ – 0.1V | V |
| $V_{REF}$ | Reference Voltage Range ($REF^+$ – $REF^-$) | | ● | 0.1 | | $V_{CC}$ | V |
| $C_{S(IN+)}$ | $IN^+$ Sampling Capacitance | | | | 11 | | pF |
| $C_{S(IN-)}$ | $IN^-$ Sampling Capacitance | | | | 11 | | pF |
| $C_{S(VREF)}$ | $V_{REF}$ Sampling Capacitance | | | | 11 | | pF |
| $I_{DC\_LEAK(IN^+)}$ | $IN^+$ DC Leakage Current | Sleep Mode, $IN^+$ = GND | ● | –10 | 1 | 10 | nA |
| $I_{DC\_LEAK(IN^-)}$ | $IN^-$ DC Leakage Current | Sleep Mode, $IN^-$ = GND | ● | –10 | 1 | 10 | nA |
| $I_{DC\_LEAK(REF^+)}$ | $REF^+$ DC Leakage Current | Sleep Mode, $REF^+$ = $V_{CC}$ | ● | –100 | 1 | 100 | nA |
| $I_{DC\_LEAK(REF^-)}$ | $REF^-$ DC Leakage Current | Sleep Mode, $REF^-$ = GND | ● | –100 | 1 | 100 | nA |
| $t_{OPEN}$ | MUX Break-Before-Make | | | | 50 | | ns |
| QIRR | MUX Off Isolation | $V_{IN}$ = $2V_{P-P}$ DC to 1.8MHz | | | 120 | | dB |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | High Level Input Voltage ($\overline{CS}$, $F_O$, SDI) | 2.7V ≤ $V_{CC}$ ≤ 5.5V (Note 18) | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{IL}$ | Low Level Input Voltage ($\overline{CS}$, $F_O$, SDI) | 2.7V ≤ $V_{CC}$ ≤ 5.5V | ● | | | 0.5 | V |
| $V_{IH}$ | High Level Input Voltage (SCK) | 2.7V ≤ $V_{CC}$ ≤ 5.5V (Notes 10, 15) | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{IL}$ | Low Level Input Voltage (SCK) | 2.7V ≤ $V_{CC}$ ≤ 5.5V (Notes 10, 15) | ● | | | 0.5 | V |
| $I_{IN}$ | Digital Input Current ($\overline{CS}$, $F_O$, SDI) | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ | ● | –10 | | 10 | µA |
| $I_{IN}$ | Digital Input Current (SCK) | 0V ≤ $V_{IN}$ ≤ $V_{CC}$ (Notes 10, 15) | ● | –10 | | 10 | µA |
| $C_{IN}$ | Digital Input Capacitance ($\overline{CS}$, $F_O$, SDI) | | | | 10 | | pF |
| $C_{IN}$ | Digital Input Capacitance (SCK) | (Notes 10, 15) | | | 10 | | pF |
| $V_{OH}$ | High Level Output Voltage (SDO) | $I_O$ = –800µA | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{OL}$ | Low Level Output Voltage (SDO) | $I_O$ = 1.6mA | ● | | | 0.4 | V |
| $V_{OH}$ | High Level Output Voltage (SCK) | $I_O$ = –800µA (Notes 10, 17) | ● | $V_{CC}$ – 0.5 | | | V |
| $V_{OL}$ | Low Level Output Voltage (SCK) | $I_O$ = 1.6mA (Notes 10, 17) | ● | | | 0.4 | V |
| $I_{OZ}$ | Hi-Z Output Leakage (SDO) | | ● | –10 | | 10 | µA |

## POWER REQUIREMENTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | ● | 2.7 | | 5.5 | V |
| $I_{CC}$ | Supply Current | Conversion Current (Note 12)<br>Sleep Mode (Note 12) | ●<br>● | | 160<br>1 | 275<br>2 | µA<br>µA |

## DIGITAL INPUTS AND DIGITAL OUTPUTS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_A$ = 25°C. (Note 3)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $f_{EOSC}$ | External Oscillator Frequency Range | (Note 16) | ● | 10 | | 1000 | kHz |
| $t_{HEO}$ | External Oscillator High Period | | ● | 0.125 | | 100 | µs |
| $t_{LEO}$ | External Oscillator Low Period | | ● | 0.125 | | 100 | µs |
| $t_{CONV}$ | Conversion Time | Simultaneous 50Hz/60Hz<br>External Oscillator | ● | 144.1 | 146.9<br>41036/$f_{EOSC}$ (in kHz) | 149.9 | ms<br>ms |
| $f_{ISCK}$ | Internal SCK Frequency | Internal Oscillator (Notes 10, 17)<br>External Oscillator (Notes 10, 11, 15) | | | 38.4<br>$f_{EOSC}$/8 | | kHz<br>kHz |
| $D_{ISCK}$ | Internal SCK Duty Cycle | (Notes 10, 17) | ● | 45 | | 55 | % |
| $f_{ESCK}$ | External SCK Frequency Range | (Notes 10, 11, 15) | ● | | | 4000 | kHz |
| $t_{LESCK}$ | External SCK Low Period | (Notes 10, 11, 15) | ● | 125 | | | ns |
| $t_{HESCK}$ | External SCK High Period | (Notes 10, 11, 15) | ● | 125 | | | ns |
| $t_{DOUT\_ISCK}$ | Internal SCK 24-Bit Data Output Time | Internal Oscillator (Notes 10, 17)<br>External Oscillator (Notes 10, 11, 15) | ● | 0.61 | 0.625<br>192/$f_{EOSC}$ (in kHz) | 0.64 | ms<br>ms |
| $t_{DOUT\_ESCK}$ | External SCK 24-Bit Data Output Time | | | | 24/$f_{ESCK}$ (in kHz) | | ms |
| $t_1$ | $\overline{CS}$↓ to SDO Low | | ● | 0 | | 200 | ns |
| $t_2$ | $\overline{CS}$↑ to SDO High Z | | ● | 0 | | 200 | ns |
| $t_3$ | $\overline{CS}$↓ to SCK↓ | Internal SCK Mode | ● | 0 | | 200 | ns |
| $t_4$ | $\overline{CS}$↓ to SCK↑ | External SCK Mode | ● | 50 | | | ns |
| $t_{KQMAX}$ | SCK↓ to SDO Valid | | ● | | | 200 | ns |
| $t_{KQMIN}$ | SDO Hold After SCK↓ | (Note 5) | ● | 15 | | | ns |
| $t_5$ | SCK Set-Up Before $\overline{CS}$↓ | | ● | 50 | | | ns |
| $t_7$ | SDI Setup Before SCK↑ | (Note 5) | ● | 100 | | | ns |
| $t_8$ | SDI Hold After SCK↑ | (Note 5) | ● | 100 | | | ns |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All voltage values are with respect to GND.

**Note 3:** Unless otherwise specified:

$V_{CC}$ = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ – IN^–$, $V_{IN(CM)} = (IN^+ – IN^–)/2$,
where $IN^+$ and $IN^–$ are the selected input channels.

**Note 4:** Use internal conversion clock or external conversion clock source with $f_{EOSC}$ = 307.2kHz unless other wise specified.

**Note 5:** Guaranteed by design, not subject to test.

**Note 6:** Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

**Note 7:** $f_{EOSC}$ = 256kHz ±2% (external oscillator).

**Note 8:** $f_{EOSC}$ = 307.2kHz ±2% (external oscillator).

**Note 9:** Simultaneous 50Hz/60Hz (internal oscillator) or $f_{EOSC}$ = 280kHz ±2% (external oscillator).

**Note 10:** The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is $f_{ESCK}$. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is $f_{ISCK}$.

**Note 11:** The external oscillator is connected to the $F_O$ pin. The external oscillator frequency, $f_{EOSC}$, is expressed in kHz.

**Note 12:** The converter uses its internal oscillator.

**Note 13:** The output noise includes the contribution of the internal calibration operations. $V_{REF} \leq V_{CC}$.

**Note 14:** Guaranteed by design and test correlation.

**Note 15:** The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is $f_{ESCK}$ and is expressed in Hz.

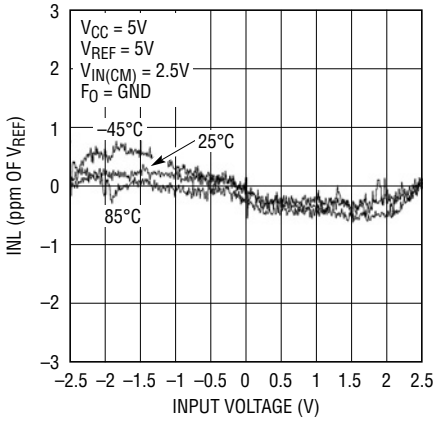
**Note 16:** Refer to Applications Information section for performance vs data rate graphs.

**Note 17:** The converter in internal SCK mode of operation such that the SCK pin is used as a digital output.

**Note 18:** For $V_{CC}$ < 3V, $V_{IH}$ is 2.5V for pin $f_O$.

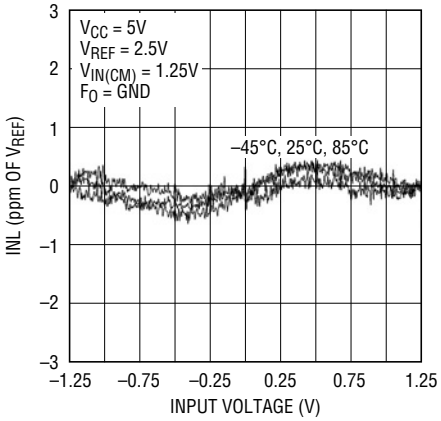
# TYPICAL PERFORMANCE CHARACTERISTICS

### Integral Nonlinearity ($V_{CC}$ = 5V, $V_{REF}$ = 5V)



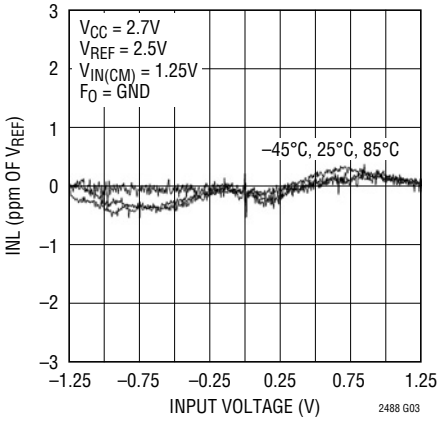

2488 G01

### Integral Nonlinearity ($V_{CC}$ = 5V, $V_{REF}$ = 2.5V)



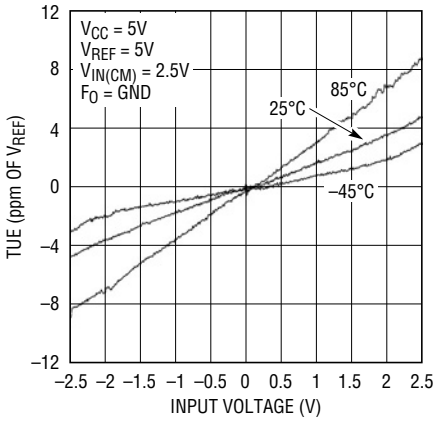

2488 G02

### Integral Nonlinearity ($V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V)



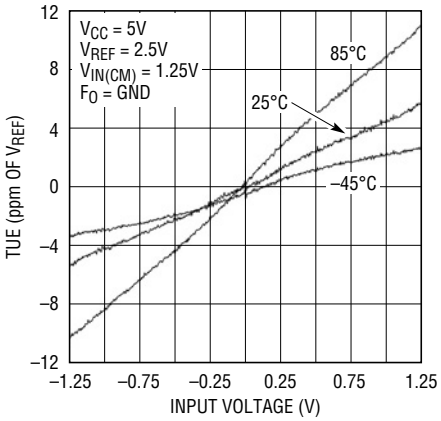

2488 G03

### Total Unadjusted Error ($V_{CC}$ = 5V, $V_{REF}$ = 5V)



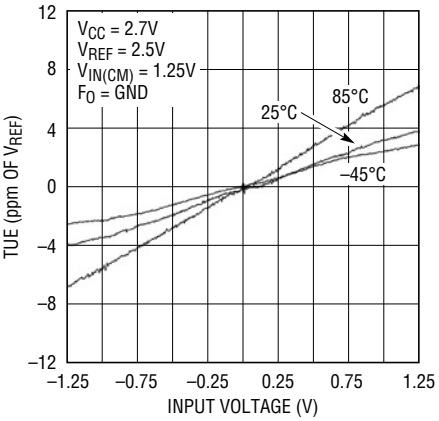

2488 G04

### Total Unadjusted Error ($V_{CC}$ = 5V, $V_{REF}$ = 2.5V)



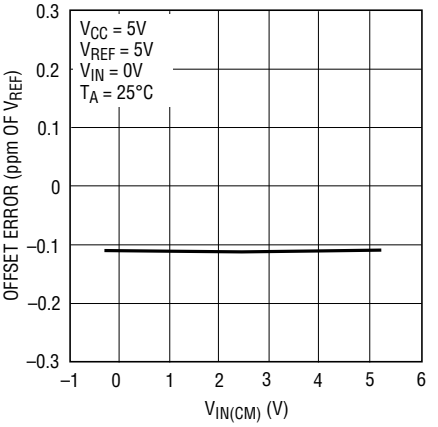

2488 G05

### Total Unadjusted Error ($V_{CC}$ = 2.7V, $V_{REF}$ = 2.5V)



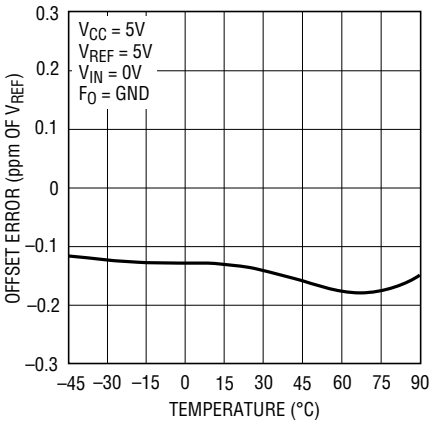

2488 G06

### Offset Error vs $V_{IN(CM)}$



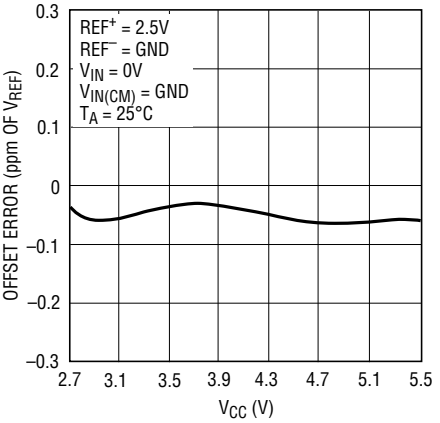

2488 G07

### Offset Error vs Temperature




2488 G08

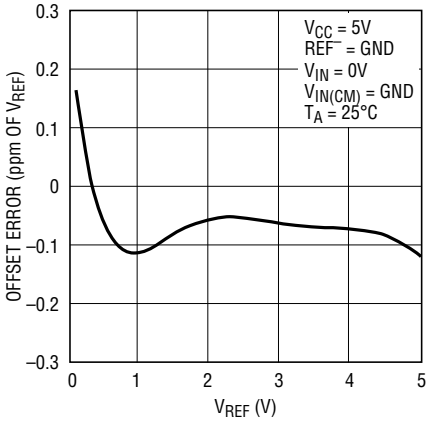
### Offset Error vs $V_{CC}$




2488 G09

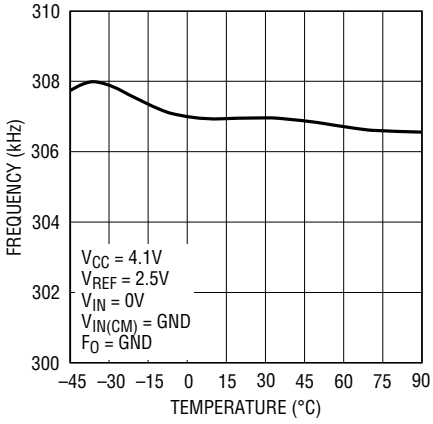
# TYPICAL PERFORMANCE CHARACTERISTICS

### Offset Error vs $V_{REF}$



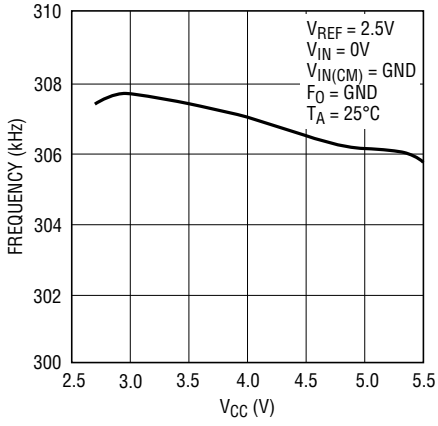

2488 G10

### On-Chip Oscillator Frequency vs Temperature



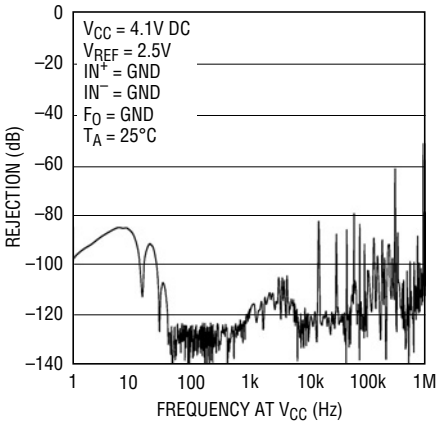

2488 G11

### On-Chip Oscillator Frequency vs $V_{CC}$



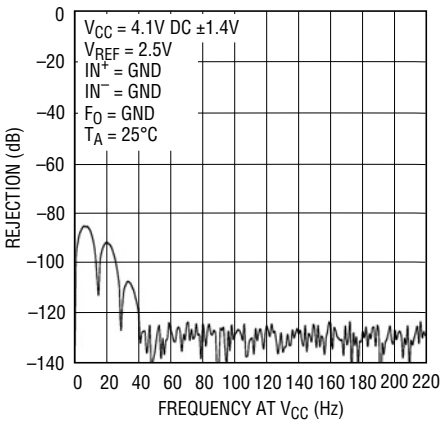

2488 G12

### PSRR vs Frequency at $V_{CC}$



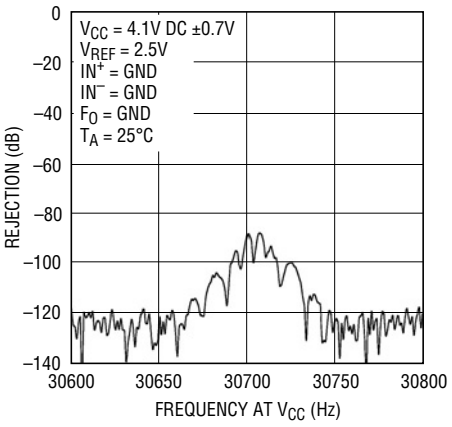

2488 G13

### PSRR vs Frequency at $V_{CC}$



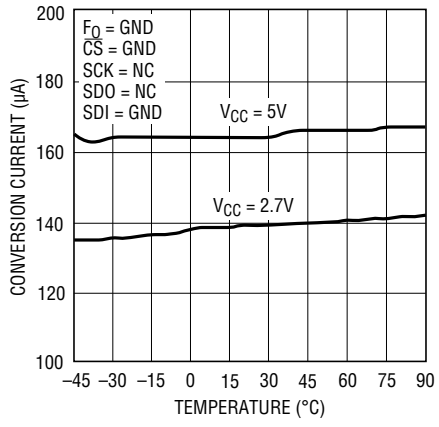

2488 G14

### PSRR vs Frequency at $V_{CC}$



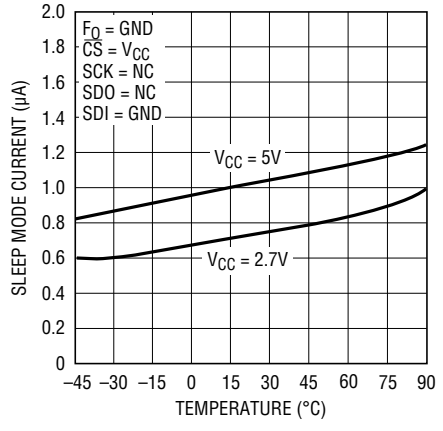

2488 G15

### Conversion Current vs Temperature



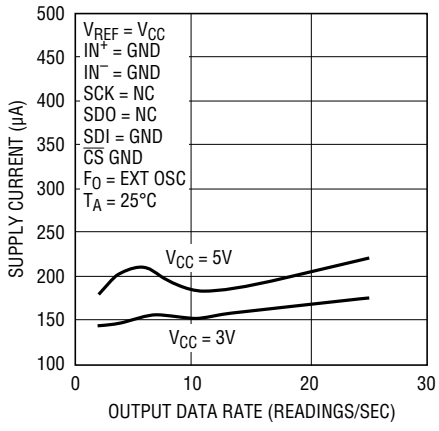

2488 G16

### Sleep Mode Current vs Temperature




2488 G17

### Conversion Current vs Output Data Rate




2488 G18

## PIN FUNCTIONS

**$F_O$ (Pin 1):** Frequency Control Pin. Digital input that controls the internal conversion clock rate. When $F_O$ is connected to ground, the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the $F_O$ pin with an external clock in order to change the output rate and the digital filter rejection null.

**SDI (Pin 2):** Serial Data Input. This pin is used to select the input channel. The serial data input is applied under control of the serial clock (SCK) during the data output/input operation. The first conversion following a new input is valid.

**SCK (Pin 3):** Bidirectional, Digital I/O, Clock Pin. In Internal Serial Clock Operation mode, SCK is generated internally and is seen as an output on the SCK pin. In External Serial Clock Operation mode, the digital I/O clock is externally applied to the SCK pin. The Serial Clock operation mode is determined by the logic level applied to the SCK pin at power up and during the most recent falling edge of $\overline{CS}$.

**$\overline{CS}$ (Pin 4):** Active LOW Chip Select. A LOW on this pin enables the digital input/output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the data output aborts the data transfer and starts a new conversion.

**SDO (Pin 5):** Three-State Digital Output. During the data output period, this pin is used as the serial data output. When the chip select pin is HIGH, the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. When the conversion is in progress this pin is HIGH; once the conversion is complete SDO goes low. The conversion status is monitored by pulling $\overline{CS}$ LOW.

**GND (Pin 6):** Ground. Connect this pin to a common ground plane through a low impedance connection.

**COM (Pin 7):** The common negative input ($IN^-$) for all single ended multiplexer configurations. The voltage on CH0 to CH3 and COM pins can have any value between GND – 0.3V to $V_{CC}$ + 0.3V. Within these limits, the two selected inputs ($IN^+$ and $IN^-$) provide a bipolar input range ($V_{IN} = IN^+ – IN^-$) from $–0.5 • V_{REF}$ to $0.5 • V_{REF}$. Outside this input range, the converter produces unique over-range and under-range output codes.

**CH0 to CH3 (Pins 8-11):** Analog Inputs. May be programmed for single-ended or differential mode.

**$V_{CC}$ (Pin 12):** Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

**$REF^+$ (Pin 13), $REF^-$ (Pin 14):** Differential Reference Input. The voltage on these pins can have any value between GND and $V_{CC}$ as long as the reference positive input, $REF^+$, remains more positive than the negative reference input, $REF^-$, by at least 0.1V. The differential voltage ($V_{REF} = REF^+ – REF^-$) sets the fullscale range for all input channels.

**Exposed Pad (Pin 15):** Ground. This pin is ground and must be soldered to the PCB ground plane. For prototyping purposes, this pin may remain floating.

# FUNCTIONAL BLOCK DIAGRAM

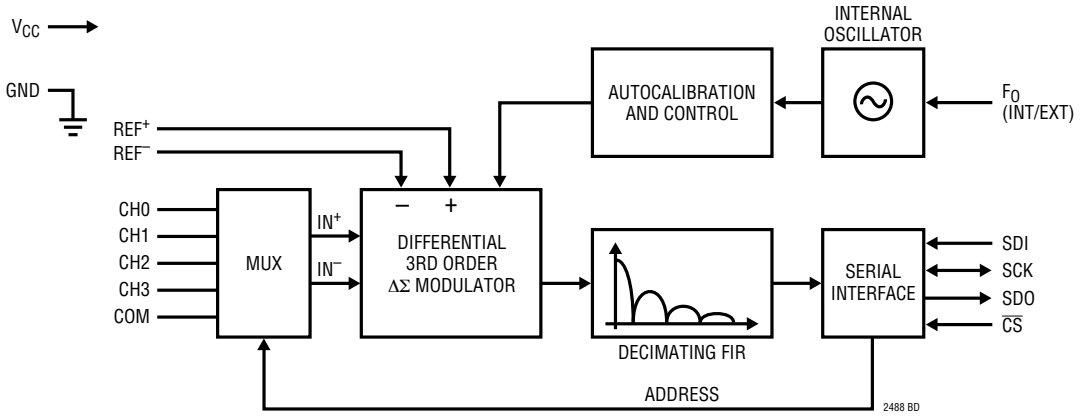
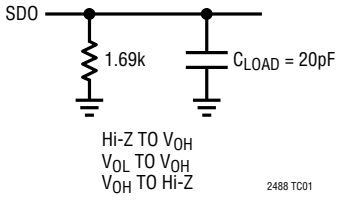
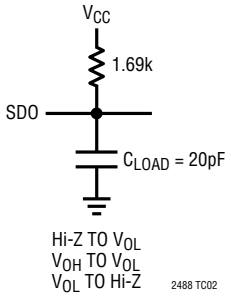



**Figure 1. Functional Block Diagram**

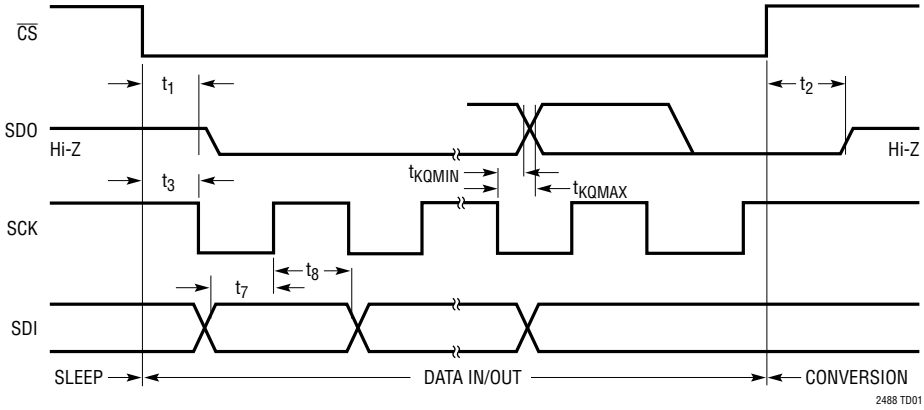
# TEST CIRCUITS



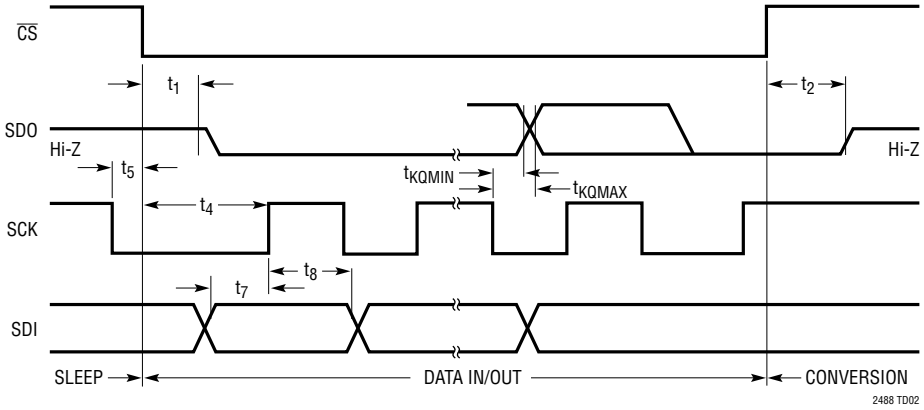



# TIMING DIAGRAMS

**Timing Diagram Using Internal SCK (SCK HIGH with $\overline{CS}\downarrow$)**




**Timing Diagram Using External SCK (SCK LOW with $\overline{CS}\downarrow$)**



# APPLICATIONS INFORMATION

## CONVERTER OPERATION

### Converter Operation Cycle

The LTC2488 is a multi-channel, low power, delta-sigma, analog-to-digital converter with an easy-to-use 4-wire interface and automatic differential input current cancellation. Its operation is made up of four states (See Figure 2). The converter's operating cycle begins with the conversion, followed by the sleep state, and ends with the data input/output cycle. The 4-wire interface consists of serial data output (SDO), serial clock (SCK), chip select ($\overline{CS}$) and serial data input (SDI).The interface, timing, operation cycle, and data output format is compatible with Linear's entire family of SPI $\Delta\Sigma$ converters.

Initially, at power up, the LTC2488 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in the sleep state, if $\overline{CS}$ is HIGH, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device powers up, exits the sleep state, and enters the data input/output state. If $\overline{CS}$ is brought HIGH before the first rising edge of SCK, the device returns to the sleep state and the power is reduced. If $\overline{CS}$ is brought HIGH after the first rising edge of SCK, the data output cycle is aborted and a new conversion cycle begins. The data output corresponds to the conversion just completed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock pin (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (See Figure 3). The channel selection data for the next conversion is also loaded into the device at this time. Data is loaded from the serial data input pin (SDI) on each rising edge of SCK. The data input/output cycle concludes once 24 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

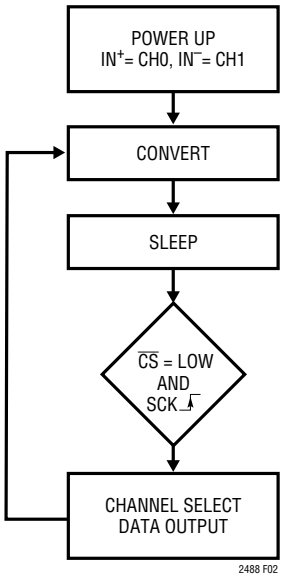



**Figure 2. LTC2488 State Transition Diagram**

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2488 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming and do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

### Ease of Use

The LTC2488 data output has no latency, filter settling delay, or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog inputs is straight forward. Each conversion, immediately following a newly selected input, is valid and accurate to the full specifications of the device.

The LTC2488 automatically performs offset and full scale calibration every conversion cycle independent of the input channel selected. This calibration is transparent to the user and has no effect on the operation cycle described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage variation, input channel, and temperature drift.

### Easy Drive Input Current Cancellation

The LTC2488 combines a high precision, delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to

## APPLICATIONS INFORMATION

directly interface to the LTC2488 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation Section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and $V_{CC}$. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

### Power-Up Sequence

The LTC2488 automatically enters an internal reset state when the power supply voltage $V_{CC}$ drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection, and serial clock mode.

When $V_{CC}$ rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel $IN^+$ = CH0, $IN^-$ = CH1. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel can be programmed into the device during this first data input/output cycle.

### Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for $REF^+$ and $REF^-$ pins covers the entire operating range of the device (GND to $V_{CC}$). For correct converter operation, $V_{REF}$ must be positive ($REF^+ > REF^-$).

The LTC2488 differential reference input range is 0.1V to $V_{CC}$. For the simplest operation, $REF^+$ can be shorted to $V_{CC}$ and $REF^-$ can be shorted to GND. The converter output noise is determined by the thermal noise of the front end circuits. Since the transition noise is well below 1LSB (0.02LSB), a decrease in reference voltage will proportionally improve the converter resolution and improve INL.

### Input Voltage Range

The LTC2488 input measurement range is $-0.5 \cdot V_{REF}$ to $0.5 \cdot V_{REF}$ in both differential and single-ended configurations as shown in Figure 28. Highest linearity is achieved with fully differential drive and a constant common mode voltage (Figure 28b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

The analog inputs are truly differential with an absolute, common mode range for the CH0 to CH3 and COM input pins extending from GND – 0.3V to $V_{CC}$ + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2488 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where $IN^+$ and $IN^-$ are the selected input channels), from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0 to CH3, COM) may extend 300mV below ground and above $V_{CC}$. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if $V_{REF}$ = 5V. This error has a very strong temperature dependency.

### SERIAL INTERFACE PINS

The LTC2488 transmits the conversion result, reads the input channel selection, and receives a start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to access the converter status. During the data output state, it is used to read the conversion result and program the input channel.

### Serial Clock Input/Output (SCK)

The serial clock pin (SCK) is used to synchronize the data input/output transfer. Each bit is shifted out of the SDO

## APPLICATIONS INFORMATION

pin on the falling edge of SCK and data is shifted into the SDI pin on the rising edge of SCK.

The serial clock pin (SCK) can be configured as either a master (SCK is an output generated internally) or a slave (SCK is an input and applied externally). Master mode (Internal SCK) is selected by simply floating the SCK pin. Slave mode (External SCK) is selected by driving SCK low during power up and each falling edge of $\overline{CS}$. Specific details of these SCK modes are described in the Serial Interface Timing Modes section.

### Serial Data Output (SDO)

The serial data output pin (SDO) provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ is HIGH, the SDO driver is switched to a high impedance state in order to share the data output line with other devices. If $\overline{CS}$ is brought LOW during the conversion phase, the $\overline{EOC}$ bit (SDO pin) will be driven HIGH. Once the conversion is complete, if $\overline{CS}$ is brought LOW, $\overline{EOC}$ will be driven LOW indicating the conversion is complete and the result is ready to be shifted out of the device.

### Chip Select ($\overline{CS}$)

The active low $\overline{CS}$ pin is used to test the conversion status, enable I/O data transfer, initiate a new conversion, control the duration of the sleep state, and set the SCK mode.

At the conclusion of a conversion cycle, while $\overline{CS}$ is HIGH, the device remains in a low power sleep state where the supply current is reduced several orders of magnitude. In order to exit the sleep state and enter the data output state, $\overline{CS}$ must be pulled low. Data is now shifted out the SDO pin under control of the SCK pin as described previously.

A new conversion cycle is initiated either at the conclusion of the data output cycle (all 24 data bits read) or by pulling $\overline{CS}$ HIGH any time between the first and 24th rising edges of the serial clock (SCK). In this case, the data output is aborted and a new conversion begins.

### Serial Data Input (SDI)

The serial data input (SDI) is used to select the input channel. Data is shifted into the device during the data output/input state on the rising edge of SCK while $\overline{CS}$ is low.

### OUTPUT DATA FORMAT

The LTC2488 serial output stream is 24 bits long. The first bit indicates the conversion status, the second bit is always zero, and the third bit conveys sign information. The next 17 bits are the conversion result, MSB first. The remaining 4 bits are always LOW.

Bit 23 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available on the SDO pin during the conversion and sleep states whenever $\overline{CS}$ is LOW. This bit is HIGH during the conversion cycle, goes LOW once the conversion is complete, and is HIGH-Z when $\overline{CS}$ is HIGH.

Bit 22 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 21 (third output bit) is the conversion result sign indicator (SIG). If the selected input ($V_{IN} = IN^+ – IN^–$) is greater than or equal to 0V, this bit is HIGH. If $V_{IN} < 0$, this bit is LOW.

Bit 20 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 21 also provides underrange and overrange indication. If both Bit 21 and Bit 20 are HIGH, the differential input voltage is above +FS. If both Bit 21 and Bit 20 are LOW, the differential input voltage is below –FS. The function of these bits is summarized in Table 1.

**Table 1. LTC2488 Status Bits**

| Input Range | Bit 23 $\overline{EOC}$ | Bit 22 DMY | Bit 21 SIG | Bit 20 MSB |
|---|---|---|---|---|
| $V_{IN} \geq 0.5 \cdot V_{REF}$ | 0 | 0 | 1 | 1 |
| $0V \leq V_{IN} < 0.5 \cdot V_{REF}$ | 0 | 0 | 1 | 0 |
| $–0.5 \cdot V_{REF} \leq V_{IN} < 0V$ | 0 | 0 | 0 | 1 |
| $V_{IN} < –0.5 \cdot V_{REF}$ | 0 | 0 | 0 | 0 |

Bits 20 to 4 are the 16-bit plus sign conversion result MSB first.

Bit 4 is the least significant bit ($LSB_{16}$).

Bits 3 to 0 are always LOW.

## APPLICATIONS INFORMATION

Data is shifted out of the SDO pin under control of the serial clock (SCK) (see Figure 3). Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and SCK is ignored.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes in real time as a function of the internal oscillator or the clock applied to the $f_O$ pin from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 23 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 22 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the on the falling edge of the 23rd SCK and may be latched on the rising edge of the 24th SCK pulse. On the falling edge of the 24th SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 23) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the $IN^+$ and $IN^-$ pins remains between –0.3V and $V_{CC}$ + 0.3V (absolute maximum operating range) a conversion result is generated for any differential input voltage $V_{IN}$ from –FS = –0.5 • $V_{REF}$ to +FS = 0.5 • $V_{REF}$. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value –FS – 1LSB.

### INPUT DATA FORMAT

The LTC2488 serial input word is 8 bits long. The input bits (SGL, ODD, A2, A1, A0) are used to select the input channel.

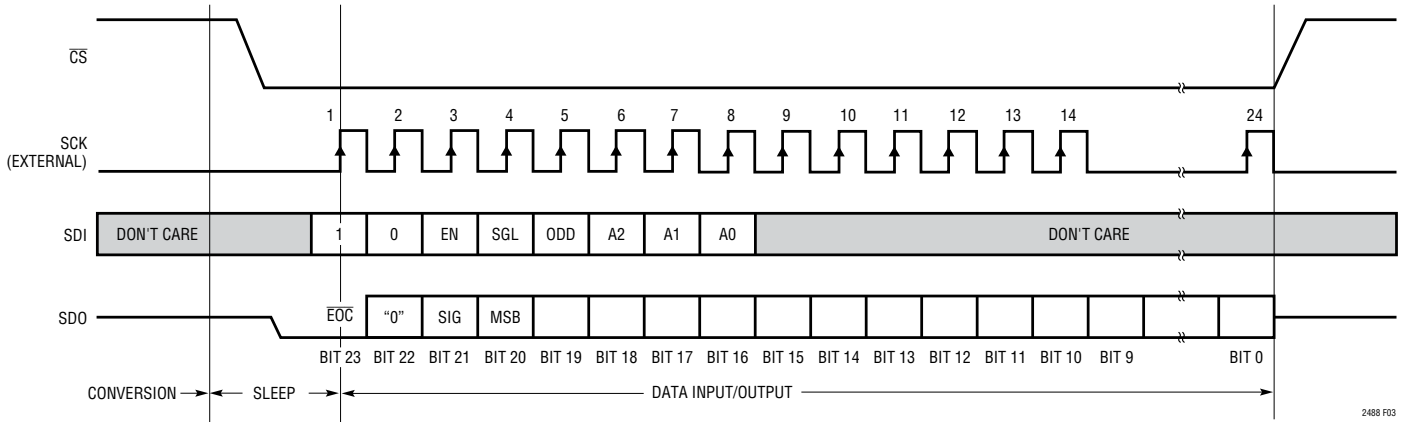



**Figure 3. Channel Selection and Data Output Timing**

**Table 2. Output Data Format**

| Differential Input Voltage $V_{IN}$* | Bit 23 $\overline{EOC}$ | Bit 22 DMY | Bit 21 SIG | Bit 20 MSB | Bit 19 | Bit 18 | Bit 17 | … | Bit 4 LSB | Bits 3 to 0 Always 0 |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{IN}$* ≥ 0.5 • $V_{REF}$** | 0 | 0 | 1 | 1 | 0 | 0 | 0 | … | 0 | 0000 |
| 0.5 • $V_{REF}$** – 1LSB | 0 | 0 | 1 | 0 | 1 | 1 | 1 | … | 1 | 0000 |
| 0.25 • $V_{REF}$** | 0 | 0 | 1 | 0 | 1 | 0 | 0 | … | 0 | 0000 |
| 0.25 • $V_{REF}$** – 1LSB | 0 | 0 | 1 | 0 | 0 | 1 | 1 | … | 1 | 0000 |
| 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | … | 0 | 0000 |
| –1LSB | 0 | 0 | 0 | 1 | 1 | 1 | 1 | … | 1 | 0000 |
| –0.25 • $V_{REF}$** | 0 | 0 | 0 | 1 | 1 | 0 | 0 | … | 0 | 0000 |
| –0.25 • $V_{REF}$** – 1LSB | 0 | 0 | 0 | 1 | 0 | 1 | 1 | … | 1 | 0000 |
| –0.5 • $V_{REF}$** | 0 | 0 | 0 | 1 | 0 | 0 | 0 | … | 0 | 0000 |
| $V_{IN}$* < –0.5 • $V_{REF}$** | 0 | 0 | 0 | 0 | 1 | 1 | 1 | … | 1 | 0000 |

*The differential input voltage $V_{IN} = IN^+ – IN^-$. **The differential reference voltage $V_{REF} = REF^+ – REF^-$.

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After power up, the device initiates an internal reset cycle which sets the input channel to CH0 to CH1 ($IN^+$ = CH0, $IN^-$ = CH1). The first conversion automatically begins at power up using this default input channel. Once the conversion is complete, a new word may be written into the device.

The first three bits of the input word consist of two preamble bits and one enable bit. These three bits are used to enable the input channel selection. Valid settings for these three bits are 000, 100, and 101. Other combinations should be avoided.

If the first three bits are 000 or 100, the following data is ignored (don't care) and the previously selected input channel remains valid for the next conversion.

If the first three bits shifted into the device are 101, then the next five bits select the input channel for the next conversion cycle (see Table 3).

The first input bit (SGL) following the 101 sequence determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of four channels is selected as the positive input. The negative input is COM for all single ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

### SERIAL INTERFACE TIMING MODES

The LTC2488's 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle or continuous conversion. The following sections describe each of these timing modes in detail. In all cases, the converter can use the internal oscillator ($F_O$ = LOW) or an external oscillator connected to the $F_O$ pin. For each mode, the operating cycle, data input format, data output format, and performance remain the same. Refer to Table 4 for a summary.

**Table 3 Channel Selection**

| MUX ADDRESS | | | | | CHANNEL SELECTION | | | | |
|---|---|---|---|---|---|---|---|---|---|
| SGL | ODD/ SIGN | A2 | A1 | A0 | 0 | 1 | 2 | 3 | COM |
| *0 | 0 | 0 | 0 | 0 | $IN^+$ | $IN^-$ | | | |
| 0 | 0 | 0 | 0 | 1 | | | $IN^+$ | $IN^-$ | |
| 0 | 1 | 0 | 0 | 0 | $IN^-$ | $IN^+$ | | | |
| 0 | 1 | 0 | 0 | 1 | | | $IN^-$ | $IN^+$ | |
| 1 | 0 | 0 | 0 | 0 | $IN^+$ | | | | $IN^-$ |
| 1 | 0 | 0 | 0 | 1 | | | $IN^+$ | | $IN^-$ |
| 1 | 1 | 0 | 0 | 0 | | $IN^+$ | | | $IN^-$ |
| 1 | 1 | 0 | 0 | 1 | | | | $IN^+$ | $IN^-$ |

*Default at power up

**Table 4. Serial Interface Timing Modes**

| CONFIGURATION | SCK SOURCE | CONVERSION CYCLE CONTROL | DATA OUTPUT CONTROL | CONNECTION AND WAVEFORMS |
|---|---|---|---|---|
| External SCK, Single Cycle Conversion | External | $\overline{CS}$ and SCK | $\overline{CS}$ and SCK | Figures 4, 5 |
| External SCK, 3-Wire I/O | External | SCK | SCK | Figure 6 |
| Internal SCK, Single Cycle Conversion | Internal | $\overline{CS}\downarrow$ | $\overline{CS}\downarrow$ | Figures 7, 8 |
| Internal SCK, 3-Wire I/O, Continuous Conversion | Internal | Continuous | Internal | Figure 9 |

## APPLICATIONS INFORMATION

### External Serial Clock, Single Cycle Operation

This timing mode uses an external serial clock to shift out the conversion result and $\overline{CS}$ to monitor and control the state of the conversion cycle (see Figure 4).

The external serial clock mode is selected during the power-up sequence and on each falling edge of $\overline{CS}$. In order to enter and remain in the external SCK mode of operation, SCK must be driven LOW both at power up and on each $\overline{CS}$ falling edge. If SCK is HIGH on the falling edge of $\overline{CS}$, the device will switch to the internal SCK mode.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is LOW, $\overline{EOC}$ is output to the SDO pin.

$\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the conversion is complete and the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the sleep state once the conversion is complete; however, in order to reduce the power, $\overline{CS}$ must be HIGH.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is LOW. The input data is then shifted in via the SDI pin on each rising edge of SCK (including the first rising edge). The channel selection will be used for the following conversion cycle. If the input channel is changed during this I/O cycle, the new settings take effect on the conversion cycle following the data input/output cycle. The output data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 24th rising edge of SCK. On the 24th falling edge of SCK, the device begins a new conversion and SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt.

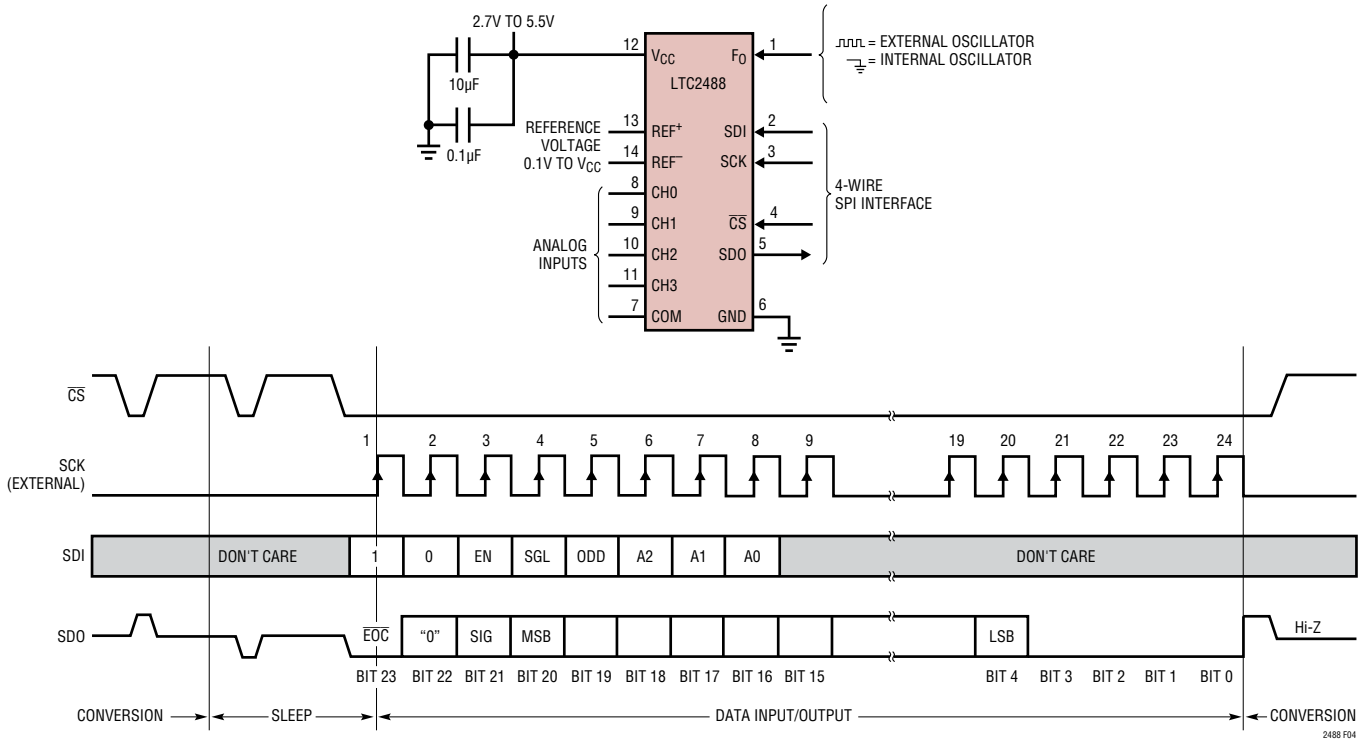


**Figure 4. External Serial Clock, Single Cycle Operation**

## APPLICATIONS INFORMATION

Typically, $\overline{CS}$ remains LOW during the data output/input state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH any time between the 1st falling edge and the 24th falling edge of SCK (see Figure 5). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of $\overline{CS}$ occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle.

### External Serial Clock, 3-Wire I/O

This timing mode uses a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal (see Figure 6). $\overline{CS}$ is permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle typically concludes 4ms after $V_{CC}$ exceeds 2V. The level applied to SCK at this time determines if SCK is internally generated or externally applied. In order to enter the external SCK mode, SCK must be driven LOW prior to the end of the POR cycle.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion is complete. On the falling edge of $\overline{EOC}$, the conversion result is loading into an internal static shift register. The output data can now be shifted out the SDO pin under control of the externally applied SCK signal. Data is updated on the falling edge of SCK. The input data is shifted into the device through the SDI pin on the rising edge of SCK. On the 24th falling edge of SCK, SDO goes HIGH, indicating a new conversion has begun. This data now serves as $\overline{EOC}$ for the next conversion.

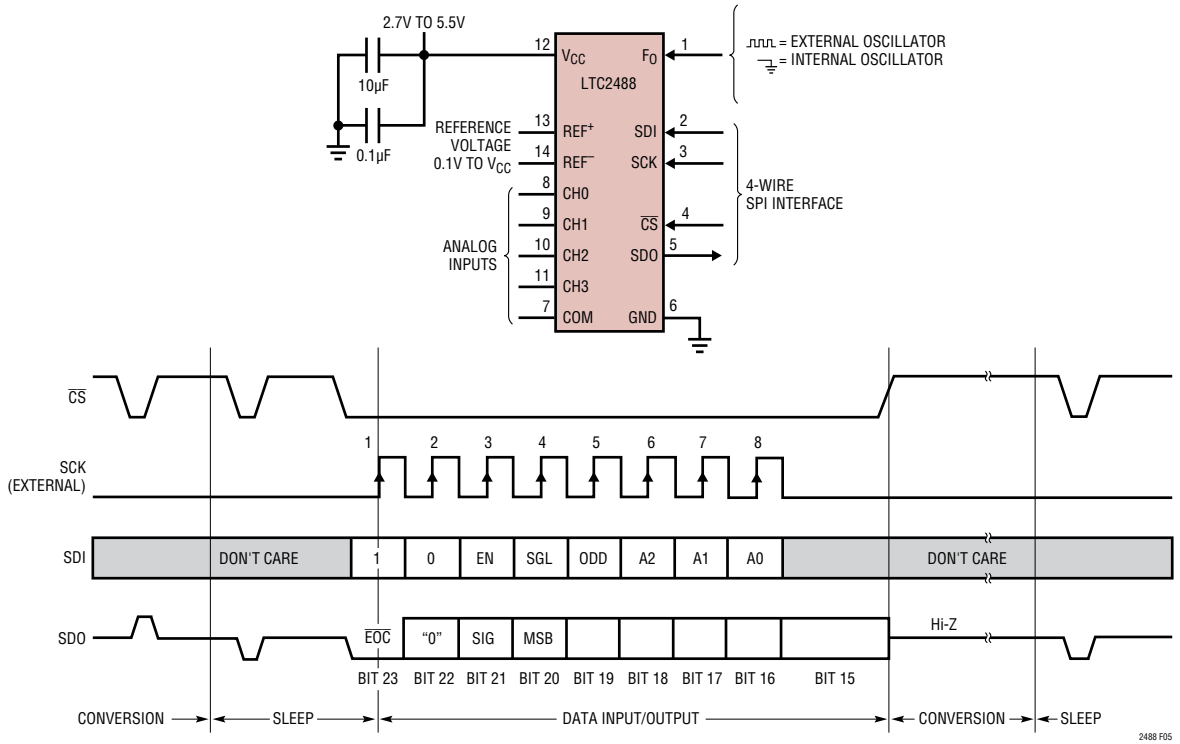


**Figure 5. External Serial Clock, Reduced Output Data Length and Valid Channel Selection**

## APPLICATIONS INFORMATION

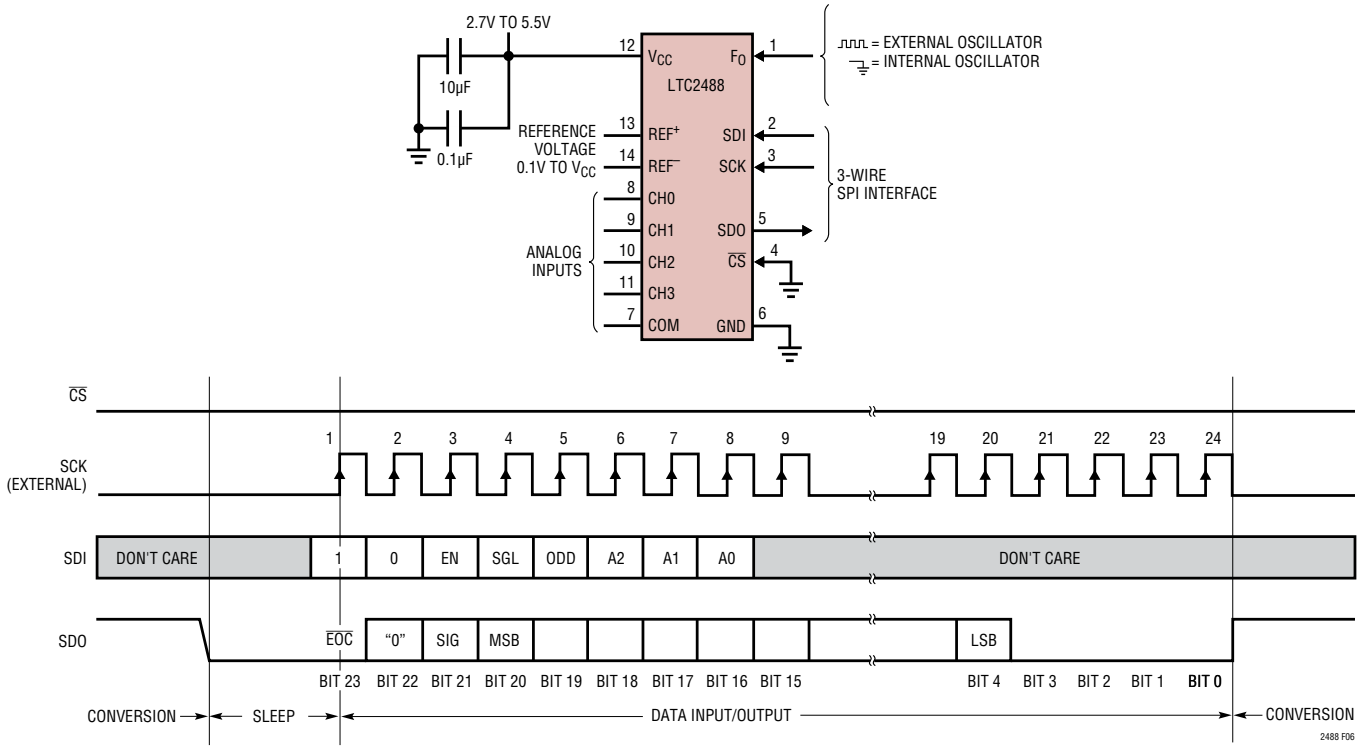


**Figure 6. External Serial Clock, 3-Wire Operation ($\overline{CS}$ = 0)**

### Internal Serial Clock, Single Cycle Operation

This timing mode uses the internal serial clock to shift out the conversion result and $\overline{CS}$ to monitor and control the state of the conversion cycle (see Figure 7).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating or pulled HIGH before the conclusion of the POR cycle and prior to each falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal SCK mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled low in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit sleep state. In order to return to the sleep state and reduce the power consumption, $\overline{CS}$ must be pulled HIGH before the device pulls SCK HIGH. When the device is using its own internal oscillator ($F_O$ is tied LOW), the first rising edge of SCK occurs 12µs ($t_{EOCTEST}$ = 12µs) after the falling edge of $\overline{CS}$. If $F_O$ is driven by an external oscillator of frequency $f_{EOSC}$, then $t_{EOCTEST} = 3.6/f_{EOSC}$.

If $\overline{CS}$ remains LOW longer than $t_{EOCTEST}$, the first rising edge of SCK will occur and the conversion result is shifted out the SDO pin on the falling edge of SCK. The serial input word (SDI) is shifted into the device on the rising edge of SCK.

After the 24th rising edge of SCK a new conversion automatically begins. SDO goes HIGH ($\overline{EOC}$ = 1) and SCK remains HIGH for the duration of the conversion cycle. Once the conversion is complete, the cycle repeats.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH any time between the 1st rising edge and the 24th falling edge of SCK (see Figure 8). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge

## APPLICATIONS INFORMATION

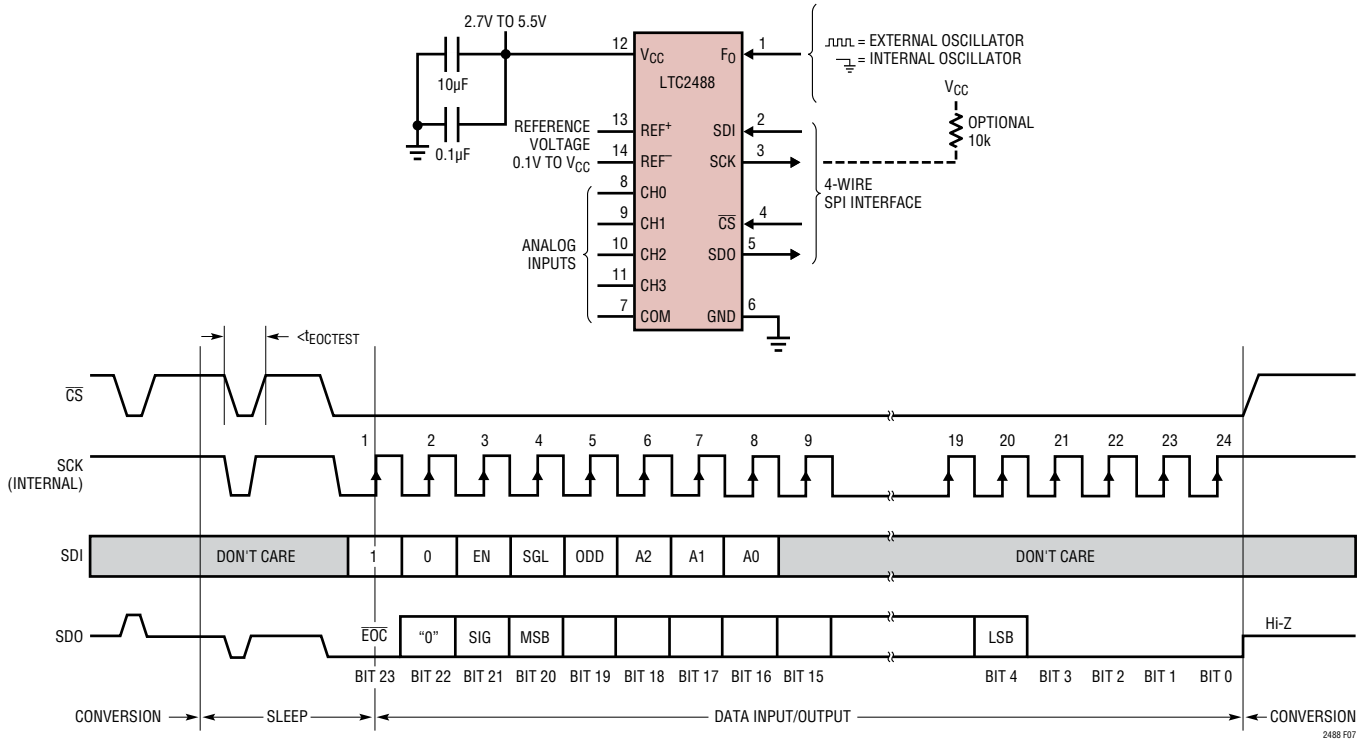


**Figure 7. Internal Serial Clock, Single Cycle Operation**

of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of $\overline{CS}$ occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle.

### Internal Serial Clock, 3-Wire I/O, Continuous Conversion.

This timing mode uses a 3-wire interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal (see Figure 9). In this case, $\overline{CS}$ is permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 4ms after $V_{CC}$ exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is floating or driven HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the sleep state. The device remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting and inputting data. The input data is shifted through the SDI pin on the rising edge of SCK (including the first rising edge) and the output data is shifted out the SDO pin on the falling edge of SCK. The data input/output cycle is concluded and a new conversion automatically begins after the 24th rising edge of SCK. During the next conversion, SCK and SDO remain HIGH until the conversion is complete.

### The Use of a 10k Pull-Up on SCK for Internal SCK Selection

If $\overline{CS}$ is pulled HIGH while the converter is driving SCK LOW, the internal pull-up is not available to restore SCK to a logic HIGH state if SCK is floating. This will cause the device to exit the internal SCK mode on the next falling edge of $\overline{CS}$. This can be avoided by adding an external 10k pull-up resistor to the SCK pin.

## APPLICATIONS INFORMATION

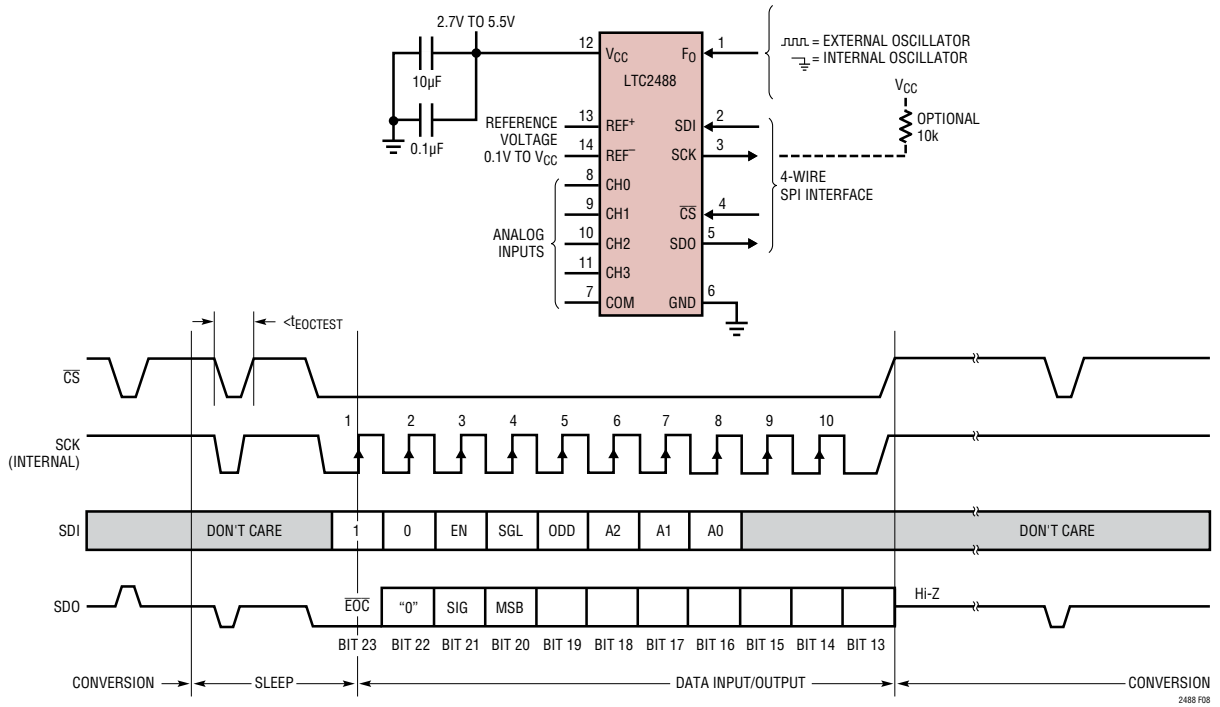


**Figure 8. Internal Serial Clock, Reduced Data Output Length with Valid Channel and Configuration Selection**

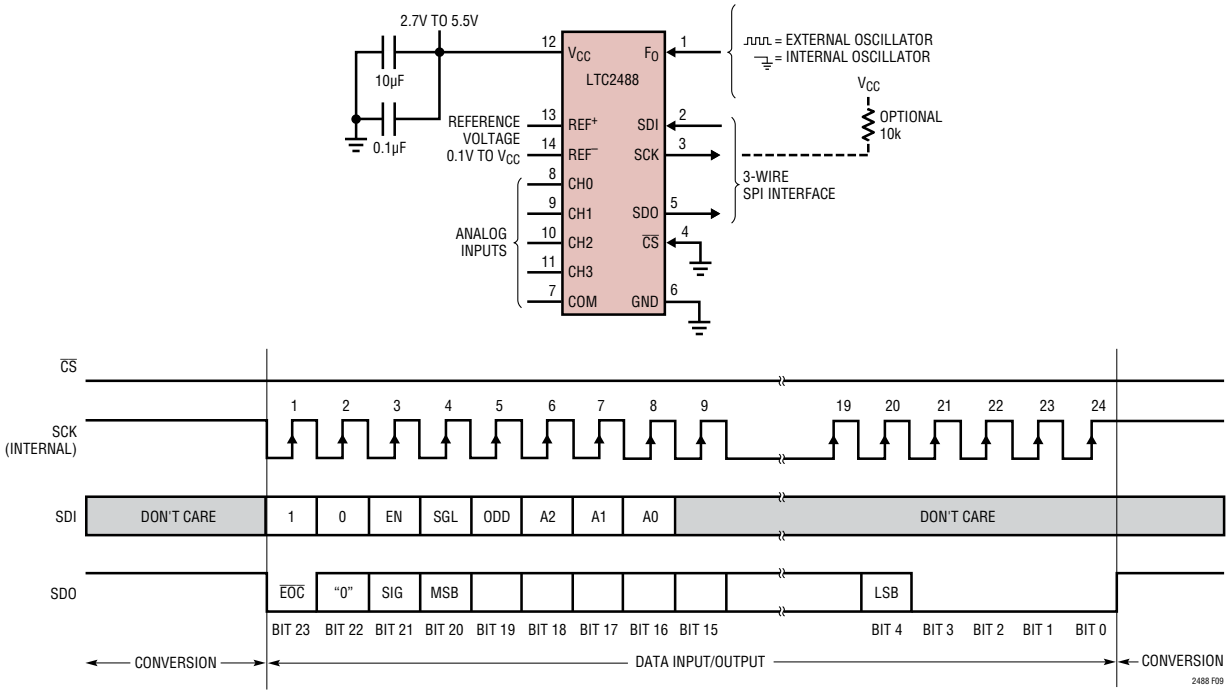


**Figure 9. Internal Serial Clock, Continuous Operation**

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Whenever SCK is LOW, the LTC2488's internal pull-up at SCK is disabled. Normally, SCK is not externally driven if the device is operating in the internal SCK timing mode. However, certain applications may require an external driver on SCK. If the driver goes Hi-Z after outputting a LOW signal, the internal pull-up is disabled. An external 10k pull-up resistor prevents the device from exiting the internal SCK mode under this condition.

A similar situation may occur during the sleep state when $\overline{CS}$ is pulsed HIGH-LOW-HIGH in order to test the conversion status. If the device is in the sleep state ($\overline{EOC}$ = 0), SCK will go LOW. If $\overline{CS}$ goes HIGH before the time $t_{EOCtest}$, the internal pull-up is activated. If SCK is heavily loaded, the internal pull-up may not restore SCK to a HIGH state before the next falling edge of $\overline{CS}$. The external 10k pull-up resistor prevents the device from exiting the internal SCK mode under this condition.

### PRESERVING THE CONVERTER ACCURACY

The LTC2488 is designed to reduce as much as possible sensitivity to device decoupling, PCB layout, anti-aliasing circuits, line frequency perturbations, and temperature sensitivity. In order to achieve maximum performance a few simple precautions should be observed.

#### Digital Signal Levels

The LTC2488's digital interface is easy to use. Its digital inputs SDI, $F_O$, $\overline{CS}$, and SCK (in external serial clock mode) accept standard CMOS logic levels. Internal hysteresis circuits can tolerate edge transition times as slow as 100µs.

The digital input signal range is 0.5V to $V_{CC}$ – 0.5V. During transitions, the CMOS input circuits draw dynamic current. For optimal performance, application of signals to the serial data interface should be reserved for the sleep and data output periods.

During the conversion period, overshoot and undershoot of fast digital signals applied to both the serial digital interface and the external oscillator pin ($F_O$) may degrade the converter performance. Undershoot and overshoot occur due to impedance mismatch of the circuit board trace at the converter pin when the transition time of an external control signal is less than twice the propagation delay from the driver to the input pin. For reference, on a regular FR-4 board, the propagation delay is approximately 183ps/inch. In order to prevent overshoot, a driver with a 1ns transition time must be connected to the converter through a trace shorter than 2.5 inches. This becomes difficult when shared control lines are used and multiple reflections occur.

Parallel termination near the input pin of the LTC2488 will eliminate this problem, but will increase the driver power dissipation. A series resistor from 27Ω to 54Ω (depending on the trace impedance and connection) placed near the driver will also eliminate over/under shoot without additional driver power dissipation.

For many applications, the serial interface pins (SCK, SDI, $\overline{CS}$, $F_O$) remain static during the conversion cycle and no degradation occurs. On the other hand, if an external oscillator is used ($F_O$ driven externally) it is active during the conversion cycle. Moreover, the digital filter rejection is minimal at the clock rate applied to $F_O$. Care must be taken to ensure external inputs and reference lines do not cross this signal or run near it. These issues are avoided when using the internal oscillator.

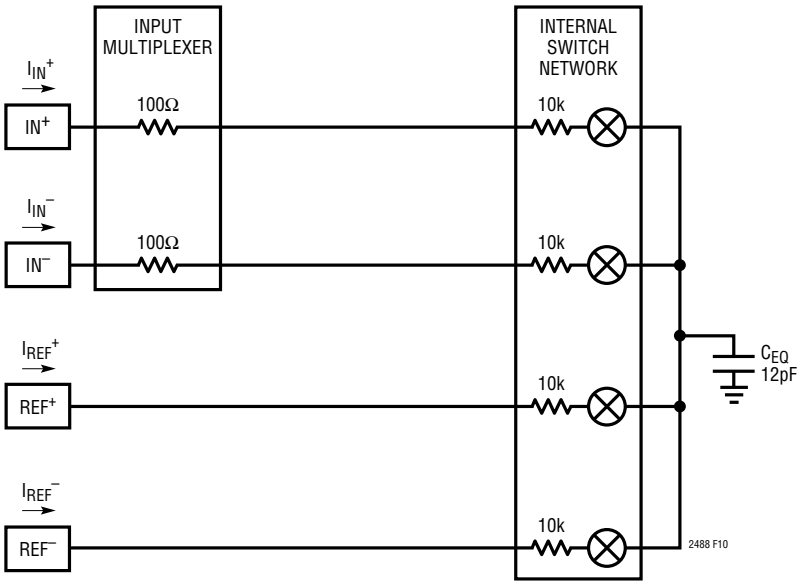
#### Driving the Input and Reference

The input and reference pins of the LTC2488 are connected directly to a switched capacitor network. Depending on the relationship between the differential input voltage and the differential reference voltage, these capacitors are switched between these four pins. Each time a capacitor is switched between two of these pins, a small amount of charge is transferred. A simplified equivalent circuit is shown in Figure 10.

When using the LTC2488's internal oscillator, the input capacitor array is switched at 123kHz. The effect of the charge transfer depends on the circuitry driving the input/reference pins. If the total external RC time constant is less than 580ns the errors introduced by the sampling process are negligible since complete settling occurs.

Typically, the reference inputs are driven from a low impedance source. In this case, complete settling occurs even with large external bypass capacitors. The inputs (CH0 to CH3, COM), on the other hand, are typically driven from

## APPLICATIONS INFORMATION




$$I\left(IN^+\right)_{AVG} = I\left(IN^-\right)_{AVG} = \frac{V_{IN(CM)} - V_{REF(CM)}}{0.5 \bullet R_{EQ}}$$

$$I\left(REF^+\right)_{AVG} \approx \frac{1.5V_{REF} + \left(V_{REF(CM)} - V_{IN(CM)}\right)}{0.5 \bullet R_{EQ}} - \frac{V_{IN}^2}{V_{REF} \bullet R_{EQ}}$$

where:

$V_{REF} = REF^+ - REF^-$

$V_{REF(CM)} = \left(\frac{REF^+ - REF^-}{2}\right)$

$V_{IN} = IN^+ - IN^-$, WHERE $IN^+$ AND $IN^-$ ARE THE SELECTED INPUT CHANNELS

$V_{IN(CM)} = \left(\frac{IN^+ - IN^-}{2}\right)$

$R_{EQ} = 2.98M\Omega$ INTERNAL OSCILLATOR

$R_{EQ} = \left(0.833 \bullet 10^{12}\right)/f_{EOSC}$ EXTERNAL OSCILLATOR

SWITCHING FREQUENCY
$f_{SW}$ = 123kHz INTERNAL OSCILLATOR
$f_{SW} = 0.4 \bullet f_{EOSC}$ EXTERNAL OSCILLATOR

**Figure 10. LTC2488 Equivalent Analog Input Circuit**

larger source resistances. Source resistances up to 10k may interface directly to the LTC2488 and settle completely; however, the addition of external capacitors at the input terminals in order to filter unwanted noise (anti-aliasing) results in incomplete settling.

### Automatic Differential Input Current Cancellation

In applications where the sensor output impedance is low (up to 10kΩ with no external bypass capacitor or up to 500Ω with 0.001µF bypass), complete settling of the input occurs. In this case, no errors are introduced and direct digitization is possible.

For many applications, the sensor output impedance combined with external input bypass capacitors produces RC time constants much greater than the 580ns required for 1ppm accuracy. For example, a 10kΩ bridge driving a 0.1µF capacitor has a time constant an order of magnitude greater than the required maximum.

The LTC2488 uses a proprietary switching algorithm that forces the average differential input current to zero independent of external settling errors. This allows direct digitization of high impedance sensors without the need of buffers.

The switching algorithm forces the average input current on the positive input ($I_{IN}^+$) to be equal to the average input current on the negative input ($I_{IN}^-$). Over the complete conversion cycle, the average differential input current ($I_{IN}^+ - I_{IN}^-$) is zero. While the differential input current is zero, the common mode input current ($I_{IN}^+ + I_{IN}^-$)/2 is proportional to the difference between the common mode input voltage ($V_{IN(CM)}$) and the common mode reference voltage ($V_{REF(CM)}$).

In applications where the input common mode voltage is equal to the reference common mode voltage, as in the case of a balanced bridge, both the differential and common mode input currents are zero. The accuracy of the converter is not compromised by settling errors.

In applications where the input common mode voltage is constant but different from the reference common mode voltage, the differential input current remains zero while the common mode input current is proportional to the difference between $V_{IN(CM)}$ and $V_{REF(CM)}$. For a reference common mode voltage of 2.5V and an input common mode of 1.5V, the common mode input current is approximately 0.74µA. This common mode input current does not degrade the accuracy if the source impedances

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tied to $IN^+$ and $IN^-$ are matched. Mismatches in source impedance lead to a fixed offset error but do not effect the linearity or full scale reading. A 1% mismatch in a 1k source resistance leads to a 74µV shift in offset voltage.

In applications where the common mode input voltage varies as a function of the input signal level (single ended type sensors), the common mode input current varies proportionally with input voltage. For the case of balanced input impedances, the common mode input current effects are rejected by the large CMRR of the LTC2488, leading to little degradation in accuracy. Mismatches in source impedances lead to gain errors proportional to the difference between the common mode input and common mode reference. 1% mismatches in 1k source resistances lead to gain errors on the order of 15ppm. Based on the stability of the internal sampling capacitors and the accuracy of the internal oscillator, a one-time calibration will remove this error.

In addition to the input sampling current, the input ESD protection diodes have a temperature dependent leakage current. This current, nominally 1nA (±10nA Max), results in a small offset shift. A 1k source resistance will create a 1µV typical and a 10µV maximum offset voltage.

### Reference Current

Similar to the analog inputs, the LTC2488 samples the differential reference pins ($REF^+$ and $REF^-$) transferring small amounts of charge to and from these pins, thus producing a dynamic reference current. If incomplete settling occurs (as a function the reference source resistance and reference bypass capacitance) linearity and gain errors are introduced.

For relatively small values of external reference capacitance ($C_{REF}$ < 1nF), the voltage on the sampling capacitor settles for reference impedances of many kΩ (if $C_{REF}$ = 100pF up to 10kΩ will not degrade the performance) (see Figures 11 and 12).

In cases where large bypass capacitors are required on the reference inputs ($C_{REF}$ > 0.01µF) full-scale and linearity errors are proportional to the value of the reference resistance. Every ohm of reference resistance produces a full-scale error of approximately 0.5ppm (while operating with the internal oscillator) (see Figures 13 and 14). If the input common mode voltage is equal to the reference common mode voltage, a linearity error of approximately 0.67ppm per 100Ω of reference resistance results (see Figure 15). In applications where the input and reference common mode voltages are different, the errors increase. A 1V difference in between common mode input and common mode reference results in a 6.7ppm INL error for every 100Ω of reference resistance.

In addition to the reference sampling charge, the reference ESD protection diodes have a temperature dependent leakage current. This leakage current, nominally 1nA (±10nA max) results in a small gain error. A 100Ω reference resistance will create a 0.5µV full scale error.

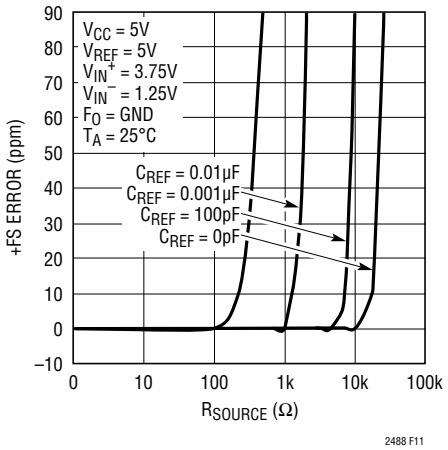


**Figure 11. +FS Error vs $R_{SOURCE}$ at $V_{REF}$ (Small $C_{REF}$)**

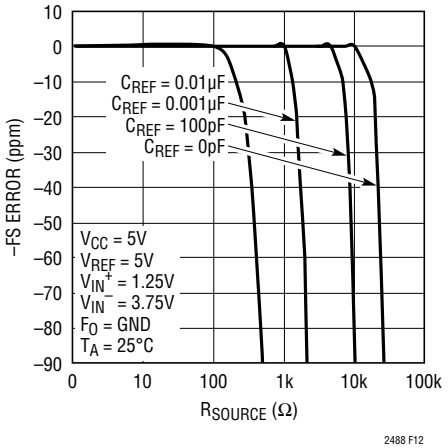


**Figure 12. –FS Error vs $R_{SOURCE}$ at $V_{REF}$ (Small $C_{REF}$)**

## APPLICATIONS INFORMATION

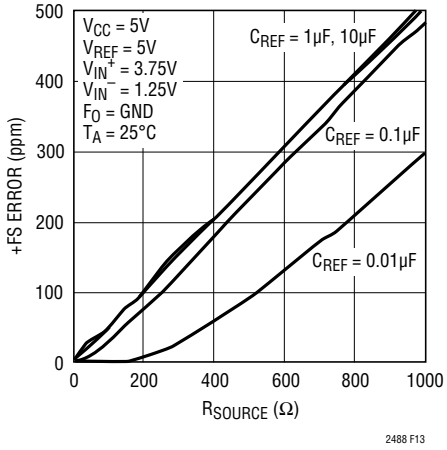


**Figure 13. +FS Error vs $R_{SOURCE}$ at $V_{REF}$ (Large $C_{REF}$)**

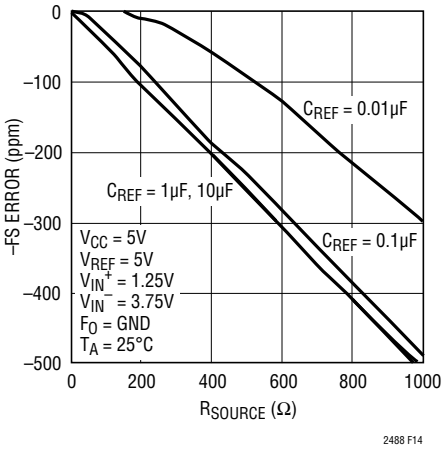


**Figure 14. –FS Error vs $R_{SOURCE}$ at $V_{REF}$ (Large $C_{REF}$)**

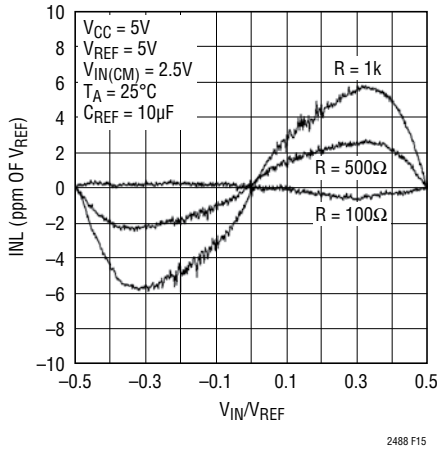


**Figure 15. INL vs Differential Input Voltage and Reference Source Resistance for $C_{REF}$ > 1µF**

### Normal Mode Rejection and Anti-aliasing

One of the advantages delta-sigma ADCs offer over conventional ADCs is on-chip digital filtering. Combined with a large oversample ratio, the LTC2488 significantly simplifies anti-aliasing filter requirements. Additionally, the input current cancellation feature allows external low pass filtering without degrading the DC performance of the device.

The SINC$^4$ digital filter provides excellent normal mode rejection at all frequencies except DC and integer multiples of the modulator sampling frequency ($f_S$). The modulator sampling frequency is $f_S$ = 15,360Hz while operating with its internal oscillator and $f_S = F_{EOSC}/20$ when operating with an external oscillator of frequency $F_{EOSC}$.

When using the internal oscillator, the LTC2488 is designed to reject line frequencies. As shown in Figure 16, rejection nulls occur at multiples of frequency $f_N$, where $f_N$ = 55Hz for simultaneous 50Hz/60Hz rejection. Multiples of the modulator sampling rate ($f_S = f_N \bullet 256$) only reject noise to 15dB (see Figure 17), if noise sources are present at these frequencies anti-aliasing will reduce their effects.

The user can expect to achieve this level of performance using the internal oscillator, as shown in Figure 18. Measured values of normal mode rejection are shown superimposed over the theoretical values.

Traditional high order delta-sigma modulators suffer from potential instabilities at large input signal levels. The

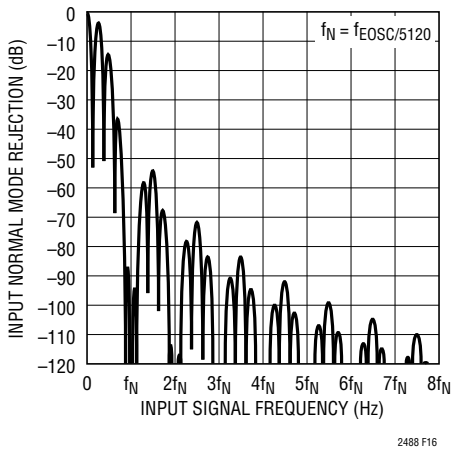


**Figure 16. Input Normal Mode Rejection at DC**

## APPLICATIONS INFORMATION

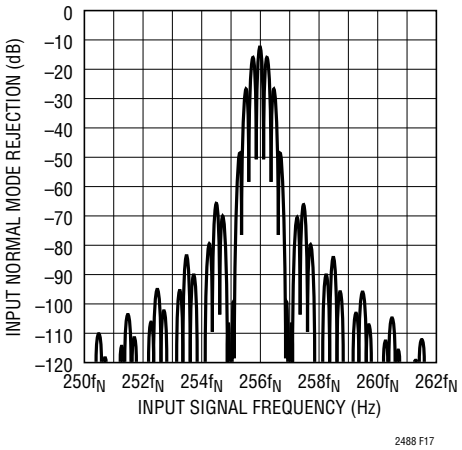


**Figure 17. Input Normal Mode Rejection at $f_S = 256 \bullet f_N$**

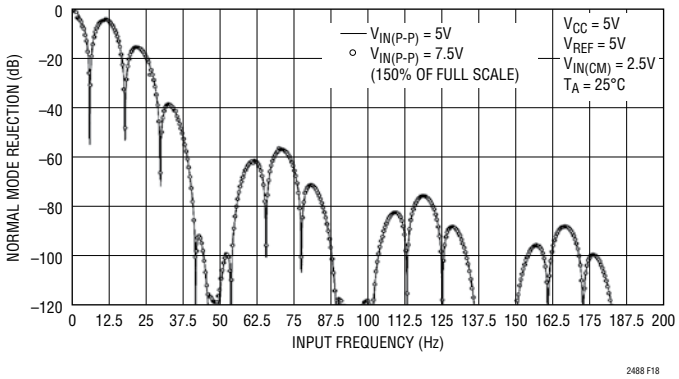


**Figure 18. Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 100% (50Hz/60Hz Notch)**

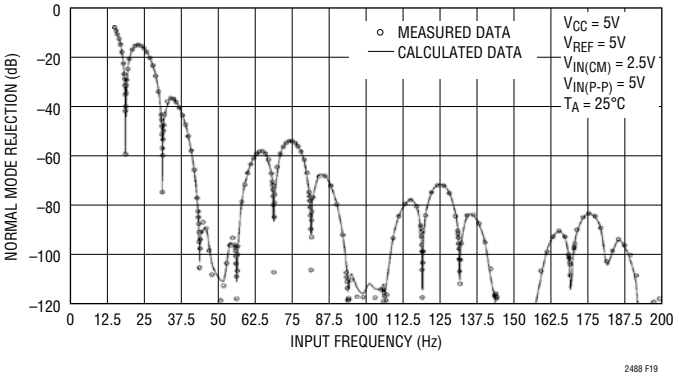


**Figure 19. Measure Input Normal Mode Rejection vs Input Frequency with Input Perturbation of 150% (60Hz Notch)**

proprietary architecture used for the LTC2488 third order modulator resolves this problem and guarantees stability with input signals 150% of full-scale. In many industrial applications, it is not uncommon to have microvolt level signals superimposed over unwanted error sources with several volts of peak-to-peak noise. Figure 19 shows measurement results for the rejection of a 7.5V peak-to-peak noise source (150% of full scale) applied to the LTC2488. From this curve, it is shown that the rejection performance is maintained even in extremely noisy environments.

### Output Data Rate

When using its internal oscillator, the LTC2488 produces up to 6.9 samples per second (sps) with a notch frequency of 55Hz. The actual output data rate depends upon the length of the sleep and data output cycles which are controlled by the user and can be made insignificantly short. When operating with an external conversion clock ($F_O$ connected to an external oscillator), the LTC2488 output data rate can be increased. The duration of the conversion cycle is $41036/f_{EOSC}$. If $f_{EOSC}$ = 307.2kHz, the converter behaves as if the internal oscillator is used.

An increase in $f_{EOSC}$ over the nominal 307.2kHz will translate into a proportional increase in the maximum output data rate (up to a maximum of 100sps). The increase in output rate leads to degradation in offset, full-scale error, and effective resolution as well as a shift in frequency rejection.

A change in $f_{EOSC}$ results in a proportional change in the internal notch position. This leads to reduced differential mode rejection of line frequencies. The common mode rejection of line frequencies remains unchanged, thus fully differential input signals with a high degree of symmetry on both the $IN^+$ and $IN^-$ pins will continue to reject line frequency noise.

An increase in $f_{EOSC}$ also increases the effective dynamic input and reference current. External RC networks will continue to have zero differential input current, but the time required for complete settling (580ns for $f_{EOSC}$ = 307.2kHz) is reduced, proportionally.

Once the external oscillator frequency is increased above 1MHz (a more than 3x increase in output rate) the effectiveness of internal auto calibration circuits begins