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24-Bit 2-/4-Channel ΔΣ ADC with Easy Drive Input Current Cancellation

FEATURES

- **Up to 2 Differential or 4 Single-Ended Inputs**
- **Easy Drive™ Technology Enables Rail-to-Rail Inputs with Zero Differential Input Current**
- **Directly Digitizes High Impedance Sensors with Full Accuracy**
- **600nV$_{RMS}$ Noise**
- **Integrated High Accuracy Temperature Sensor**
- **GND to V$_{CC}$ Input/Reference Common Mode Range**
- Programmable 50Hz, 60Hz, or Simultaneous 50Hz/60Hz Rejection Mode
- 2ppm INL, No Missing Codes
- 1ppm Offset and 15ppm Full-Scale Error
- 2x Speed Mode/Reduced Power Mode (15Hz Using Internal Oscillator and 80μA at 7.5Hz Output)
- No Latency: Digital Filter Settles in a Single Cycle, Even After a New Channel is Selected
- Single Supply 2.7V to 5.5V Operation (0.8mW)
- Internal Oscillator
- Tiny DFN 4mm × 3mm Package

APPLICATIONS

- Direct Sensor Digitizer
- Direct Temperature Measurement
- Instrumentation
- Industrial Process Control

DESCRIPTION

The LTC®2492 is a 4-channel (2-channel differential), 24-bit, No Latency ΔΣ™ ADC with Easy Drive technology. The patented sampling scheme eliminates dynamic input current errors and the shortcomings of on-chip buffering through automatic cancellation of differential input current. This allows large external source impedances and rail-to-rail input signals to be directly digitized while maintaining exceptional DC accuracy.

The LTC2492 includes a high accuracy temperature sensor and an integrated oscillator. This device can be configured to measure an external signal (from combinations of 4 analog input channels operating in single-ended or differential modes) or its internal temperature sensor. It can be programmed to reject line frequencies of 50Hz, 60Hz, or simultaneous 50Hz/60Hz and configured to double its output rate. The integrated temperature sensor offers 1/30th°C resolution and 2°C absolute accuracy.

The LTC2492 allows a wide common mode input range (0V to V_{CC}), independent of the reference voltage. Any combination of single-ended or differential inputs can be selected and the first conversion after a new channel selection is valid.

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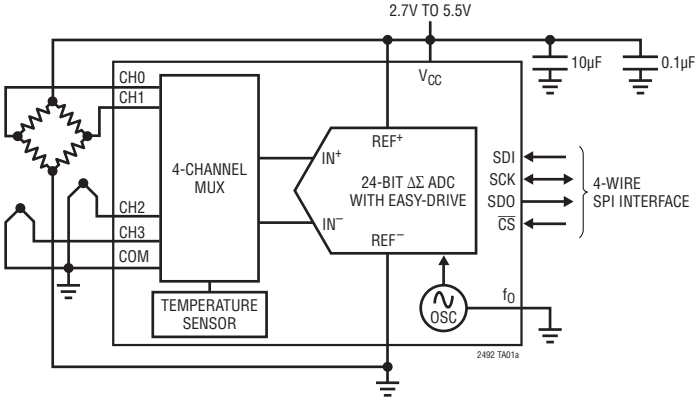
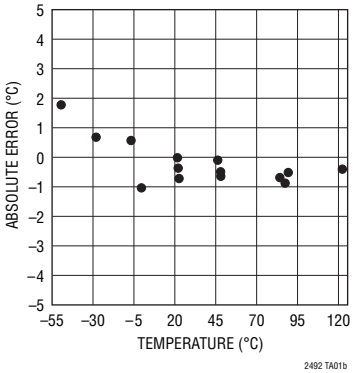
TYPICAL APPLICATION

Data Acquisition System with Temperature Compensation



Absolute Temperature Error

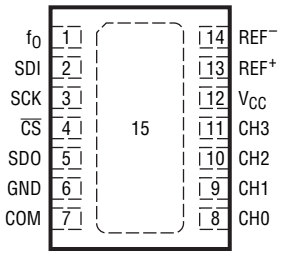


ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltage (V_{CC}) .....–0.3V to 6V
Analog Input Voltage
(CH0 to CH3, COM)..... –0.3V to (V_{CC} + 0.3V)
REF^+, REF^- ..... –0.3V to (V_{CC} + 0.3V)
Digital Input Voltage..... –0.3V to (V_{CC} + 0.3V)
Digital Output Voltage..... –0.3V to (V_{CC} + 0.3V)
Operating Temperature Range
LTC2492C ..... 0°C to 70°C
LTC2492I .....–40°C to 85°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



DE PACKAGE
14-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 15) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2492CDE#PBF	LTC2492CDE#TRPBF	2492	14-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2492IDE#PBF	LTC2492IDE#TRPBF	2492	14-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS (NORMAL SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)		24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V (Note 6)	● 		2 1	10 	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 14)	●		0.5	2.5	µV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			10		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}			0.1		ppm of V_{REF}/°C
Total Unadjusted Error	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V 5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.25V			15 15 15		ppm of V_{REF} ppm of V_{REF} ppm of V_{REF}
Output Noise	5.5V < V_{CC} < 2.7V, 2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 13)			0.6		μV_{RMS}
Internal PTAT Signal	T_A = 27°C (Note 14)		27.8	28.0	28.2	mV
Internal PTAT Temperature Coefficient				93.5		µV/°C

ELECTRICAL CHARACTERISTICS (2X SPEED)

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Notes 3, 4)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Resolution (No Missing Codes)	0.1V ≤ V_{REF} ≤ V_{CC}, –FS ≤ V_{IN} ≤ +FS (Note 5)		24			Bits
Integral Nonlinearity	5V ≤ V_{CC} ≤ 5.5V, V_{REF} = 5V, $V_{IN(CM)}$ = 2.5V (Note 6) 2.7V ≤ V_{CC} ≤ 5.5V, V_{REF} = 2.5V, $V_{IN(CM)}$ = 1.2V (Note 6)	● ●		2 1	10	ppm of V_{REF} ppm of V_{REF}
Offset Error	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 14)	●		0.2	2	mV
Offset Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC}			100		nV/°C
Positive Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}	●			25	ppm of V_{REF}
Positive Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.75V_{REF}, IN^- = 0.25V_{REF}			0.1		ppm of V_{REF}/°C
Negative Full-Scale Error	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}	●			25	ppm of V_{REF}
Negative Full-Scale Error Drift	2.5V ≤ V_{REF} ≤ V_{CC}, IN^+ = 0.25V_{REF}, IN^- = 0.75V_{REF}			0.1		ppm of V_{REF}/°C
Output Noise	5V ≤ V_{CC} ≤ 2.5V, V_{REF} = 5V, GND ≤ IN^+ = IN^- ≤ V_{CC}			0.85		μV_{RMS}

CONVERTER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	140			dB
Input Common Mode Rejection 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	140			dB
Input Common Mode Rejection 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	140			dB
Input Normal Mode Rejection 50Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 7)	●	110	120		dB
Input Normal Mode Rejection 60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 8)	●	110	120		dB
Input Normal Mode Rejection 50Hz/60Hz ±2%	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Notes 5, 9)	●	87			dB
Reference Common Mode Rejection DC	2.5V ≤ V_{REF} ≤ V_{CC}, GND ≤ IN^+ = IN^- ≤ V_{CC} (Note 5)	●	120	140		dB
Power Supply Rejection DC	V_{REF} = 2.5V, IN^+ = IN^- = GND			120		dB
Power Supply Rejection, 50Hz ±2%	V_{REF} = 2.5V, IN^+ = IN^- = GND (Notes 7, 9)			120		dB
Power Supply Rejection, 60Hz ±2%	V_{REF} = 2.5V, IN^+ = IN^- = GND (Notes 8, 9)			120		dB

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
IN^+	Absolute/Common Mode IN^+ Voltage (IN^+ Corresponds to the Selected Positive Input Channel)			GND – 0.3V		V_{CC} + 0.3V	V
IN^-	Absolute/Common Mode IN^- Voltage (IN^- Corresponds to the Selected Negative Input Channel or COM)			GND – 0.3V		V_{CC} + 0.3V	V
V_{IN}	Input Voltage Range (IN^+ – IN^-)	Differential/Single-Ended	●	–FS		+FS	V
FS	Full Scale of the Input (IN^+ – IN^-)	Differential/Single-Ended	●	0.5V_{REF}			V
LSB	Least Significant Bit of the Output Code		●	FS/2^{24}			
REF^+	Absolute/Common Mode REF^+ Voltage		●	0.1		V_{CC}	V
REF^-	Absolute/Common Mode REF^- Voltage		●	GND		REF^+ – 0.1V	V
V_{REF}	Reference Voltage Range (REF^+ – REF^-)		●	0.1		V_{CC}	V
CS(IN^+)	IN^+ Sampling Capacitance				11		pF
CS(IN^-)	IN^- Sampling Capacitance				11		pF

ANALOG INPUT AND REFERENCE

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$CS(V_{REF})$	V_{REF} Sampling Capacitance				11		pF
$I_{DC\_LEAK(IN^+)}$	IN^+ DC Leakage Current	Sleep Mode, $IN^+ = GND$	●	–10	1	10	nA
$I_{DC\_LEAK(IN^-)}$	IN^- DC Leakage Current	Sleep Mode, $IN^- = GND$	●	–10	1	10	nA
$I_{DC\_LEAK(REF^+)}$	REF^+ DC Leakage Current	Sleep Mode, $REF^+ = V_{CC}$	●	–100	1	100	nA
$I_{DC\_LEAK(REF^-)}$	REF^- DC Leakage Current	Sleep Mode, $REF^- = GND$	●	–100	1	100	nA
t_{OPEN}	MUX Break-Before-Make				50		ns
QIRR	MUX Off Isolation	$V_{IN} = 2V_{P-P}$ DC to 1.8MHz			120		dB

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage ($\overline{CS}$, f_O, SDI)	$2.7V \le V_{CC} \le 5.5V$ (Note 18)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage ($\overline{CS}$, f_O, SDI)	$2.7V \le V_{CC} \le 5.5V$	●			0.5	V
V_{IH}	High Level Input Voltage (SCK)	$2.7V \le V_{CC} \le 5.5V$ (Notes 10, 15)	●	V_{CC} – 0.5			V
V_{IL}	Low Level Input Voltage (SCK)	$2.7V \le V_{CC} \le 5.5V$ (Notes 10, 15)	●			0.5	V
I_{IN}	Digital Input Current ($\overline{CS}$, f_O, SDI)	$0V \le V_{IN} \le V_{CC}$	●	–10		10	µA
I_{IN}	Digital Input Current (SCK)	$0V \le V_{IN} \le V_{CC}$ (Notes 10, 15)	●	–10		10	µA
C_{IN}	Digital Input Capacitance ($\overline{CS}$, f_O, SDI)				10		pF
C_{IN}	Digital Input Capacitance (SCK)	(Notes 10, 15)			10		pF
V_{OH}	High Level Output Voltage (SDO)	$I_O = –800µA$	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage (SDO)	$I_O = 1.6mA$	●			0.4	V
V_{OH}	High Level Output Voltage (SCK)	$I_O = –800µA$ (Notes 10, 17)	●	V_{CC} – 0.5			V
V_{OL}	Low Level Output Voltage (SCK)	$I_O = 1.6mA$ (Notes 10, 17)	●			0.4	V
I_{OZ}	Hi-Z Output Leakage (SDO)		●	–10		10	µA

POWER REQUIREMENTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC}	Supply Voltage		●	2.7		5.5	V
I_{CC}	Supply Current	Conversion Current (Note 12)	●		160	275	µA
		Temperature Measurement (Note 12)	●		200	300	µA
		Sleep Mode (Note 12)	●		1	2	µA

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{EOSC}	External Oscillator Frequency Range	(Note 16)	●	10		1000	kHz
t_{HEO}	External Oscillator High Period		●	0.125		100	µs
t_{LEO}	External Oscillator Low Period		●	0.125		100	µs

DIGITAL INPUTS AND DIGITAL OUTPUTS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{CONV_1}	Conversion Time for 1x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	157.2 131 144.1	160.3 133.6 146.9 41036/f_{EOSC} (in kHz)	163.5 136.3 149.9	ms ms ms ms
t_{CONV_2}	Conversion Time for 2x Speed Mode	50Hz Mode 60Hz Mode Simultaneous 50/60Hz Mode External Oscillator	● ● ●	78.7 65.6 72.2	80.3 66.9 73.6 20556/f_{EOSC} (in kHz)	81.9 68.2 75.1	ms ms ms ms
f_{ISCK}	Internal SCK Frequency	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)			38.4 f_{EOSC}/8		kHz kHz
D_{ISCK}	Internal SCK Duty Cycle	(Notes 10, 17)	●	45		55	%
f_{ESCK}	External SCK Frequency Range	(Notes 10, 11, 15)	●			4000	kHz
t_{LESCK}	External SCK Low Period	(Notes 10, 11, 15)	●	125			ns
t_{HESCK}	External SCK High Period	(Notes 10, 11, 15)	●	125			ns
t_{DOUT_ISCK}	Internal SCK 32-Bit Data Output Time	Internal Oscillator (Notes 10, 17) External Oscillator (Notes 10, 11, 15)	●	0.81	0.83 256/f_{EOSC} (in kHz)	0.85	ms ms
t_{DOUT_ESCK}	External SCK 32-Bit Data Output Time	(Notes 10, 11, 15)			32/f_{ESCK} (in kHz)		ms
t_1	$\overline{CS}$↓ to SDO Low		●	0		200	ns
t_2	$\overline{CS}$↑ to SDO Hi-Z		●	0		200	ns
t_3	$\overline{CS}$↓ to SCK↓	Internal SCK Mode	●	0		200	ns
t_4	$\overline{CS}$↓ to SCK↑	External SCK Mode	●	50			ns
t_{KQMAX}	SCK↓ to SDO Valid		●			200	ns
t_{KQMIN}	SDO Hold After SCK↓	(Note 5)	●	15			ns
t_5	SCK Set Up Before $\overline{CS}$↓		●	50			ns
t_7	SDI Set Up Before SCK↑	(Note 5)	●	100			ns
t_8	SDI Hold After SCK↑	(Note 5)	●	100			ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All voltage values are with respect to GND.

Note 3: Unless otherwise specified:

V_{CC} = 2.7V to 5.5V

$V_{REFCM} = V_{REF}/2$, $F_S = 0.5V_{REF}$

$V_{IN} = IN^+ - IN^-$, $V_{IN(CM)} = (IN^+ - IN^-)/2$,

where IN^+ and IN^- are the selected input channels.

Note 4: Use internal conversion clock or external conversion clock source with f_{EOSC} = 307.2kHz unless other wise specified.

Note 5: Guaranteed by design, not subject to test.

Note 6: Integral nonlinearity is defined as the deviation of a code from a straight line passing through the actual endpoints of the transfer curve. The deviation is measured from the center of the quantization band.

Note 7: 50Hz mode (internal oscillator) or f_{EOSC} = 256kHz ±2% (external oscillator).

Note 8: 60Hz mode (internal oscillator) or f_{EOSC} = 307.2kHz ±2% (external oscillator).

Note 9: Simultaneous 50Hz/60Hz mode (internal oscillator) or f_{EOSC} = 280kHz ±2% (external oscillator).

Note 10: The SCK can be configured in external SCK mode or internal SCK mode. In external SCK mode, the SCK pin is used as a digital input and the driving clock is f_{ESCK}. In the internal SCK mode, the SCK pin is used as a digital output and the output clock signal during the data output is f_{ISCK}.

Note 11: The external oscillator is connected to the f_O pin. The external oscillator frequency, f_{EOSC}, is expressed in kHz.

Note 12: The converter uses its internal oscillator.

Note 13: The output noise includes the contribution of the internal calibration operations.

Note 14: Guaranteed by design and test correlation.

Note 15: The converter is in external SCK mode of operation such that the SCK pin is used as a digital input. The frequency of the clock signal driving SCK during the data output is f_{ESCK} and is expressed in Hz.

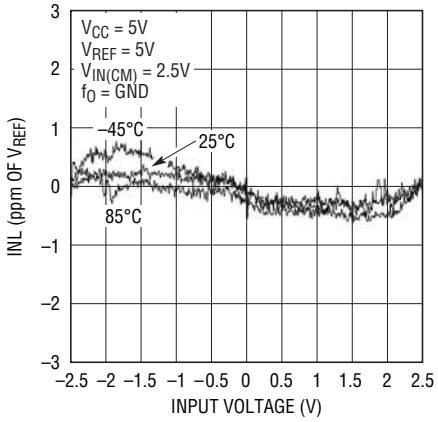
Note 16: Refer to Applications Information section for performance vs data rate graphs.

Note 17: The converter in internal SCK mode of operation such that the SCK pin is used as a digital output.

Note 18: For V_{CC} < 3V, V_{IH} is 2.5V for pin f_O.

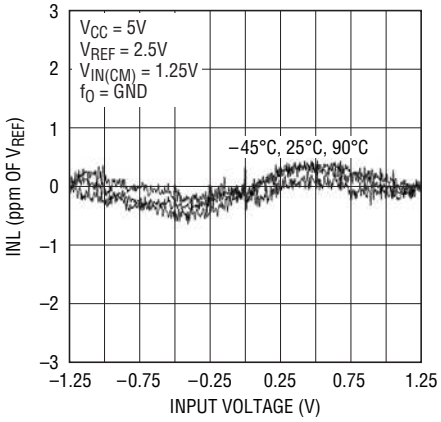
TYPICAL PERFORMANCE CHARACTERISTICS

Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 5V)



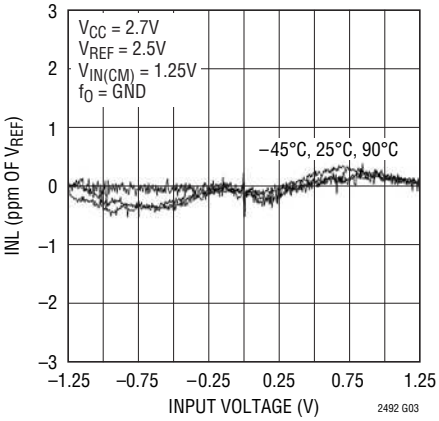
2492 G01

Integral Nonlinearity (V_{CC} = 5V, V_{REF} = 2.5V)



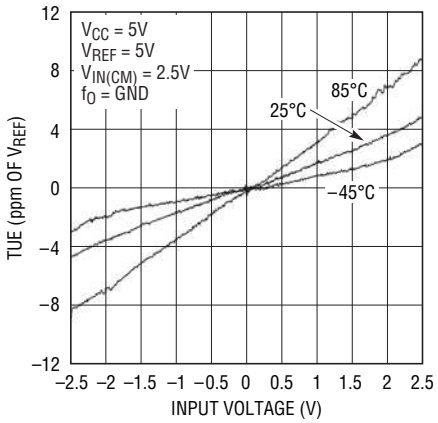
2492 G02

Integral Nonlinearity (V_{CC} = 2.7V, V_{REF} = 2.5V)



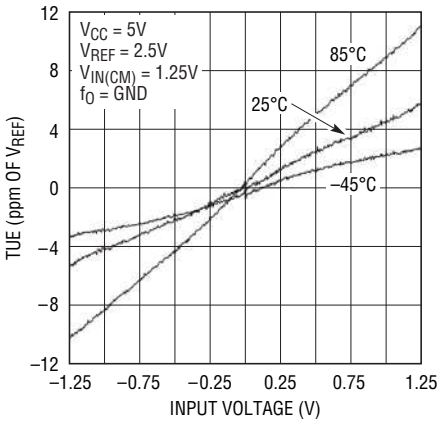
2492 G03

Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 5V)



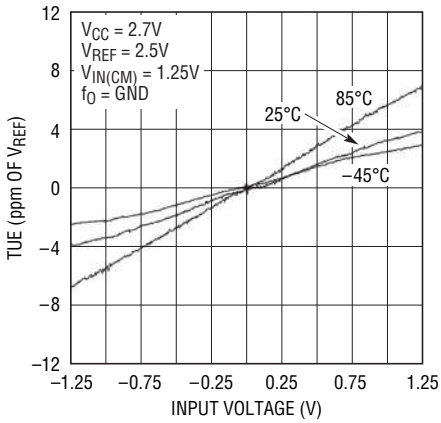
2492 G04

Total Unadjusted Error (V_{CC} = 5V, V_{REF} = 2.5V)



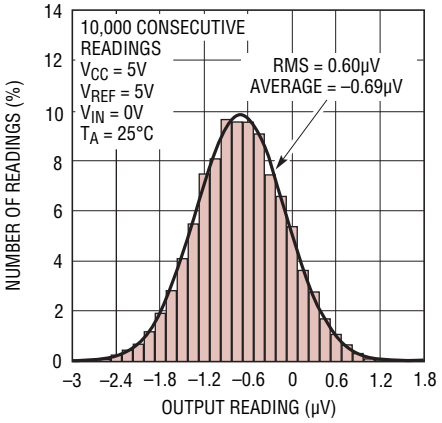
2492 G05

Total Unadjusted Error (V_{CC} = 2.7V, V_{REF} = 2.5V)



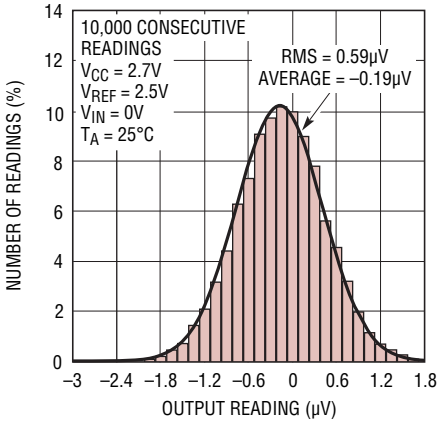
2492 G06

Noise Histogram (6.8sps)



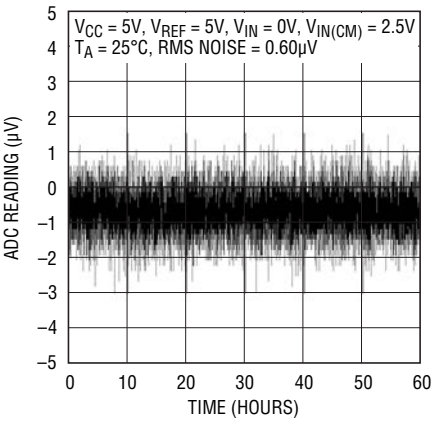
2492 G07

Noise Histogram (7.5sps)



2492 G08

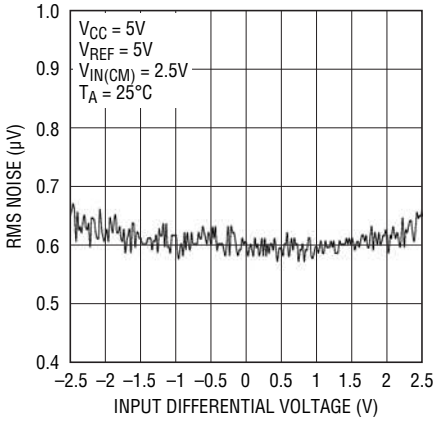
Long-Term ADC Readings



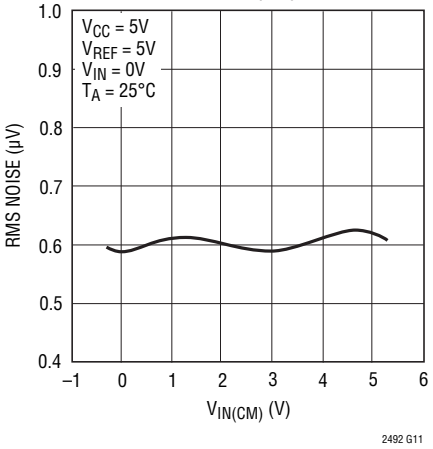
2492 G09

TYPICAL PERFORMANCE CHARACTERISTICS

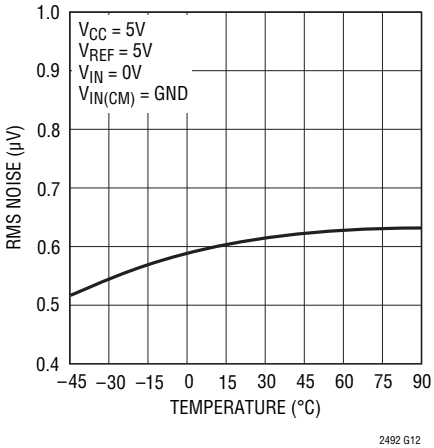
RMS Noise vs Input Differential Voltage



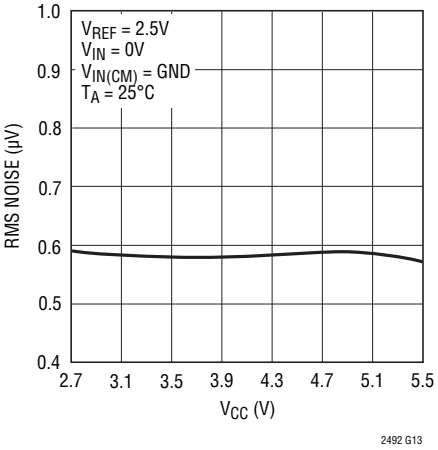
RMS Noise vs $V_{IN(CM)}$



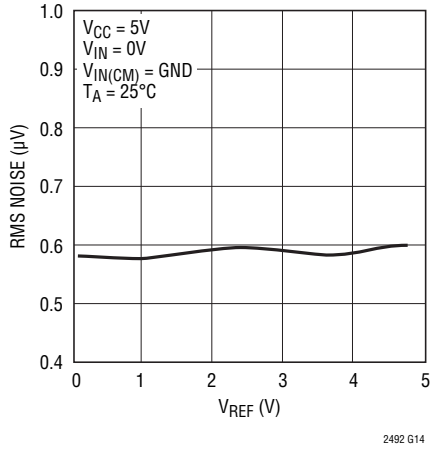
RMS Noise vs Temperature (T_A)



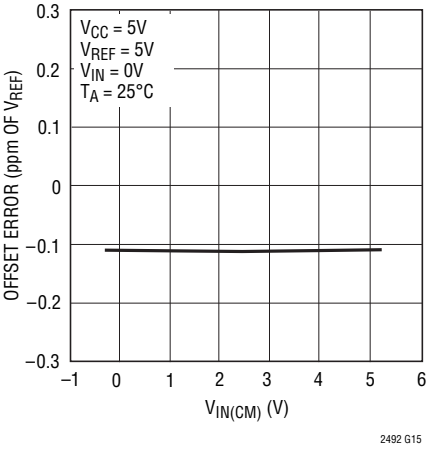
RMS Noise vs V_{CC}



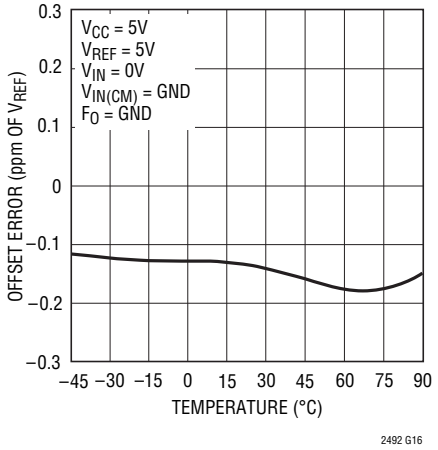
RMS Noise vs V_{REF}



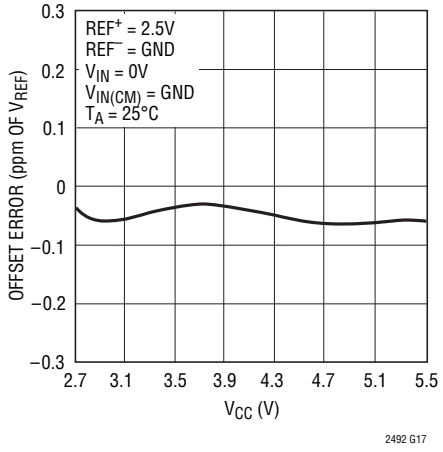
Offset Error vs $V_{IN(CM)}$



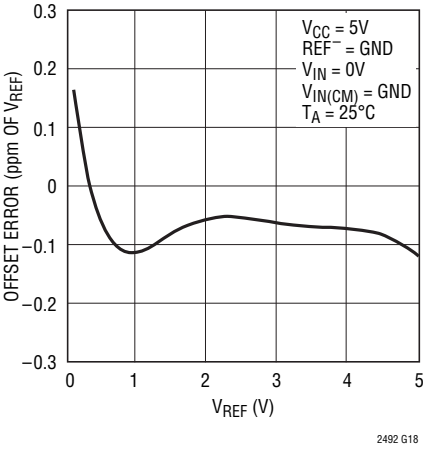
Offset Error vs Temperature



Offset Error vs V_{CC}

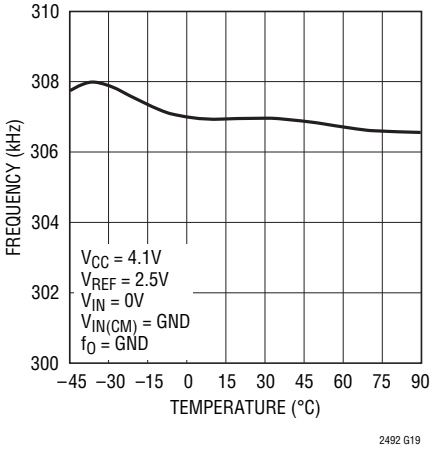


Offset Error vs V_{REF}

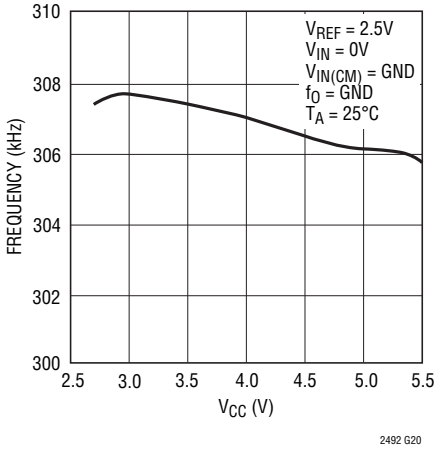


TYPICAL PERFORMANCE CHARACTERISTICS

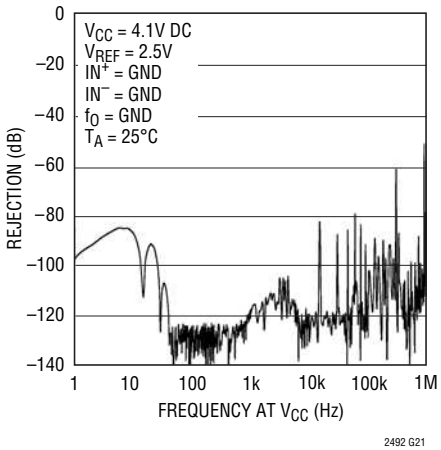
On-Chip Oscillator Frequency vs Temperature



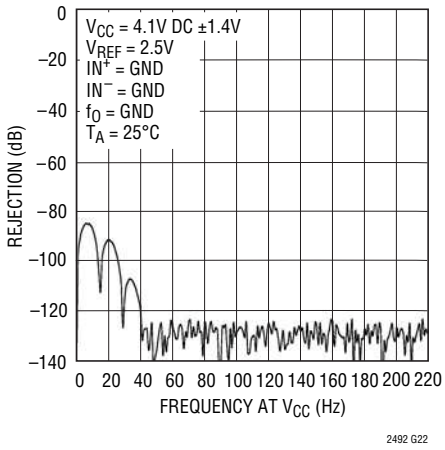
On-Chip Oscillator Frequency vs V_{CC}



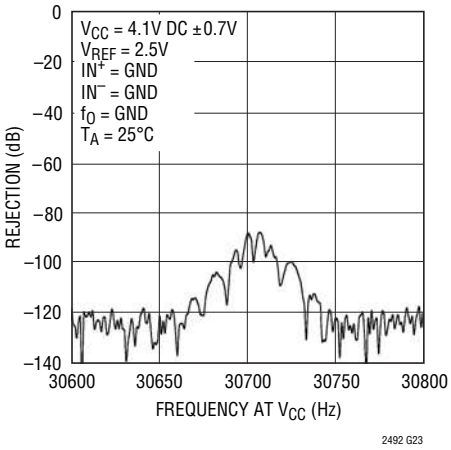
PSRR vs Frequency at V_{CC}



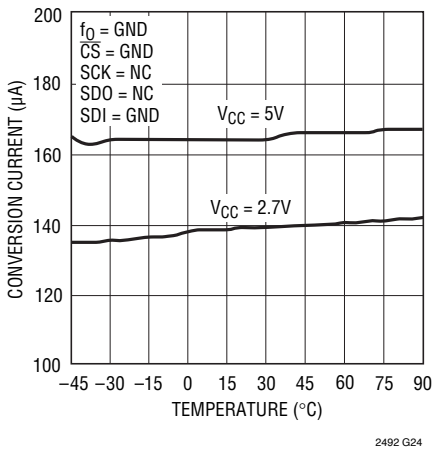
PSRR vs Frequency at V_{CC}



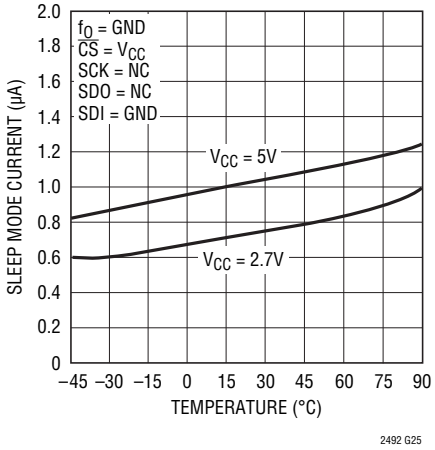
PSRR vs Frequency at V_{CC}



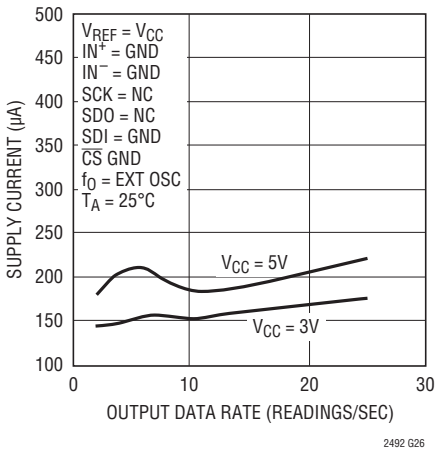
Conversion Current vs Temperature



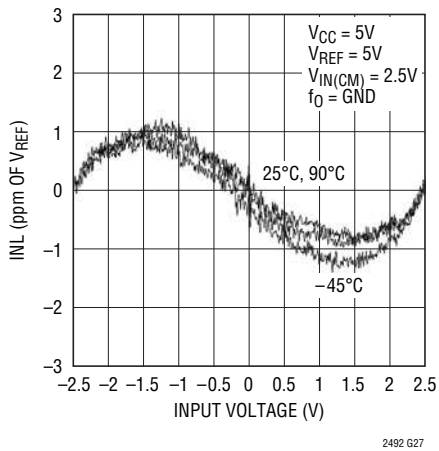
Sleep Mode Current vs Temperature



Conversion Current vs Output Data Rate

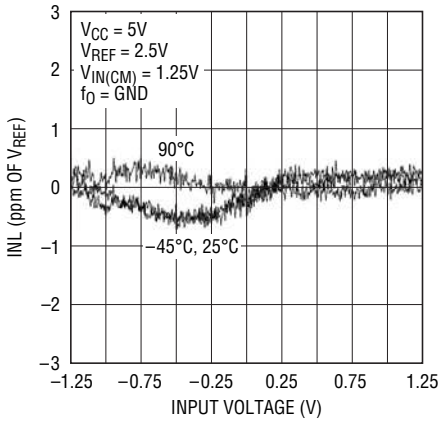


Integral Nonlinearity (2x Speed Mode; V_{CC} = 5V, V_{REF} = 5V)

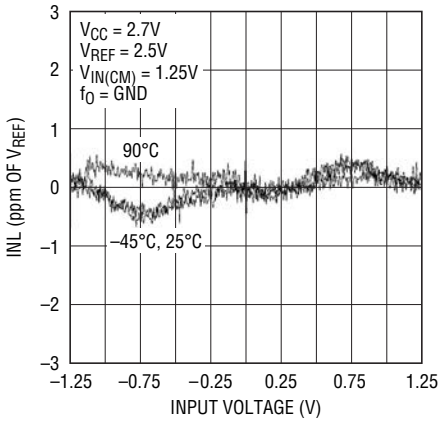


TYPICAL PERFORMANCE CHARACTERISTICS

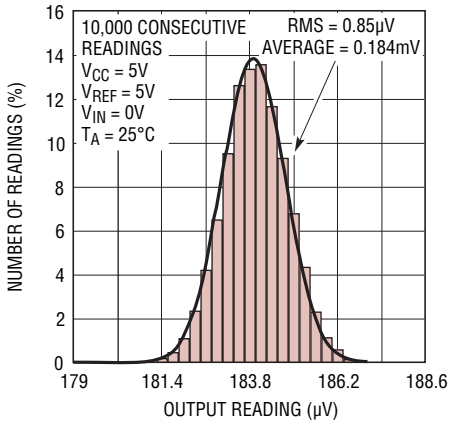
Integral Nonlinearity (2x Speed Mode; V_{CC} = 5V, V_{REF} = 2.5V)



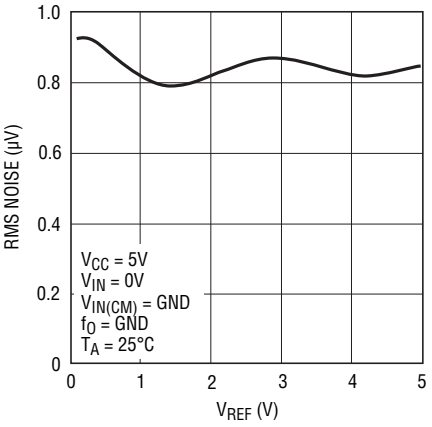
Integral Nonlinearity (2x Speed Mode; V_{CC} = 2.7V, V_{REF} = 2.5V)



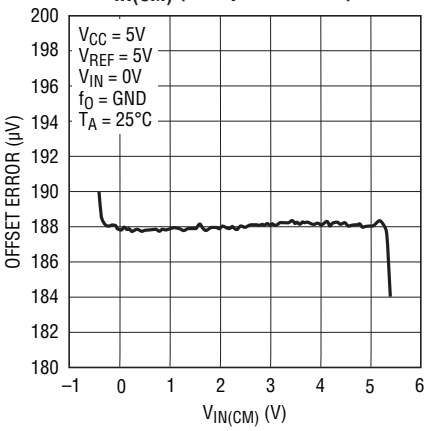
Noise Histogram (2x Speed Mode)



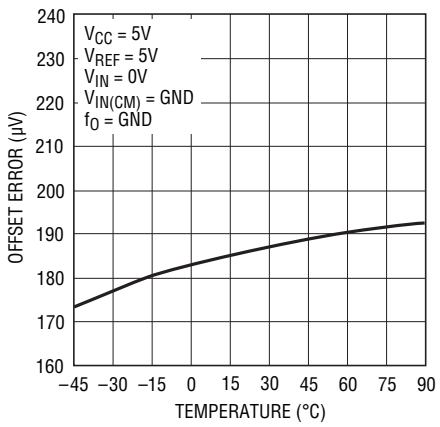
RMS Noise vs V_{REF} (2x Speed Mode)



Offset Error vs $V_{IN(CM)}$ (2x Speed Mode)

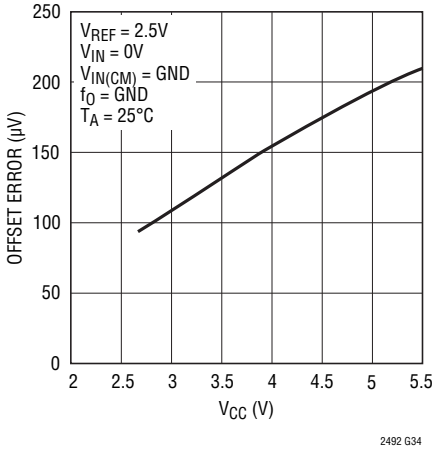


Offset Error vs Temperature (2x Speed Mode)



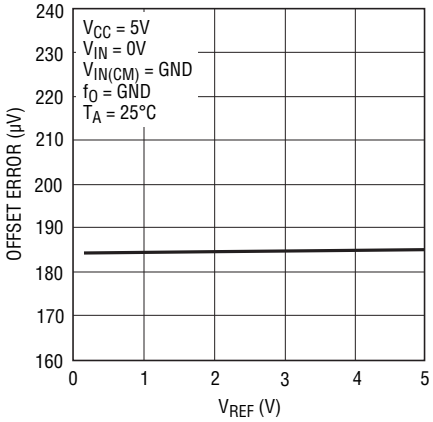
TYPICAL PERFORMANCE CHARACTERISTICS

Offset Error vs V_{CC} (2x Speed Mode)



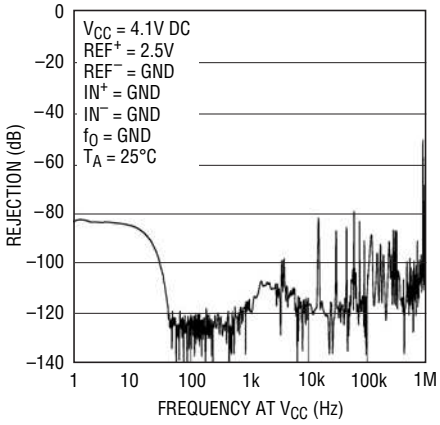
2492 G34

Offset Error vs V_{REF} (2x Speed Mode)



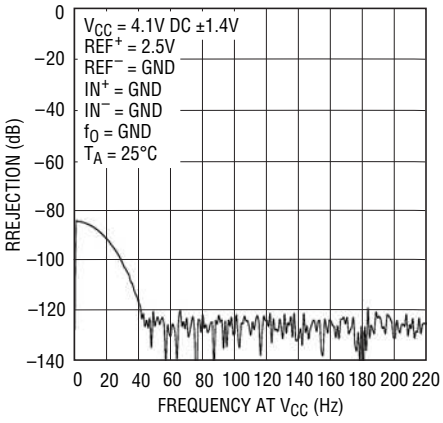
2492 G35

PSRR vs Frequency at V_{CC} (2x Speed Mode)



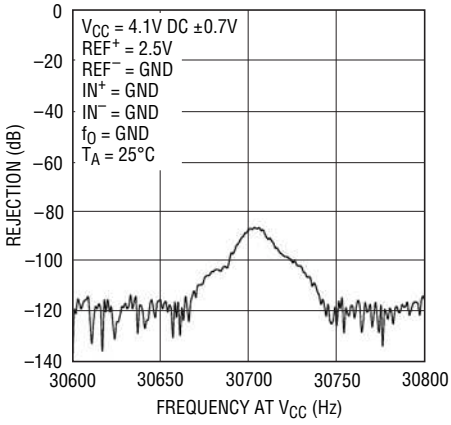
2492 G36

PSRR vs Frequency at V_{CC} (2x Speed Mode)



2492 G37

PSRR vs Frequency at V_{CC} (2x Speed Mode)



2492 G38

PIN FUNCTIONS

f_O (Pin 1): Frequency Control Pin. Digital input that controls the internal conversion clock rate. When f_O is connected to GND, the converter uses its internal oscillator running at 307.2kHz. The conversion clock may also be overridden by driving the f_O pin with an external clock in order to change the output rate and the digital filter rejection null.

SDI (Pin 2): Serial Data Input. This pin is used to select the line frequency rejection mode, 1× or 2× speed mode, temperature sensor, as well as the input channel. The serial data input is applied under control of the serial clock (SCK) during the data output/input operation. The first conversion following a new input or mode change is valid.

SCK (Pin 3): Bidirectional, Digital I/O, Clock Pin. In Internal Serial Clock Operation mode, SCK is generated internally and is seen as an output on the SCK pin. In External Serial Clock Operation mode, the digital I/O clock is externally applied to the SCK pin. The Serial Clock operation mode is determined by the logic level applied to the SCK pin at power up and during the most recent falling edge of $\overline{CS}$.

$\overline{CS}$ (Pin 4): Active LOW Chip Select. A LOW on this pin enables the digital input/output and wakes up the ADC. Following each conversion, the ADC automatically enters the Sleep mode and remains in this low power state as long as $\overline{CS}$ is HIGH. A LOW-to-HIGH transition on $\overline{CS}$ during the data output aborts the data transfer and starts a new conversion.

SDO (Pin 5): Three-State Digital Output. During the data output period, this pin is used as the serial data output. When the chip select pin is HIGH, the SDO pin is in a high impedance state. During the conversion and sleep periods, this pin is used as the conversion status output. When the conversion is in progress this pin is HIGH; once the conversion is complete SDO goes low. The conversion status is monitored by pulling $\overline{CS}$ LOW.

GND (Pin 6): Ground. Connect this pin to a common ground plane through a low impedance connection.

COM (Pin 7): The common negative input (IN^-) for all single-ended multiplexer configurations. The voltage on CH0 to CH3 and COM pins can have any value between GND – 0.3V to V_{CC} + 0.3V. Within these limits, the two selected inputs (IN^+ and IN^-) provide a bipolar input range ($V_{IN} = IN^+ – IN^-$) from $–0.5 • V_{REF}$ to $0.5 • V_{REF}$. Outside this input range, the converter produces unique over-range and under-range output codes.

CH0 to CH3 (Pins 8-11): Analog Inputs. May be programmed for single-ended or differential mode.

V_{CC} (Pin 12): Positive Supply Voltage. Bypass to GND with a 10µF tantalum capacitor in parallel with a 0.1µF ceramic capacitor as close to the part as possible.

REF^+ (Pin 13), REF^- (Pin 14): Differential Reference Input. The voltage on these pins can have any value between GND and V_{CC} as long as the reference positive input, REF^+, remains more positive than the negative reference input, REF^-, by at least 0.1V. The differential voltage ($V_{REF} = REF^+ – REF^-$) sets the full-scale range for all input channels. When performing an on-chip temperature measurement, the minimum value of REF = 2V.

Exposed Pad (Pin 15): Ground. This pin is ground and must be soldered to the PCB ground plane. For prototyping purposes, this pin may remain floating.

FUNCTIONAL BLOCK DIAGRAM

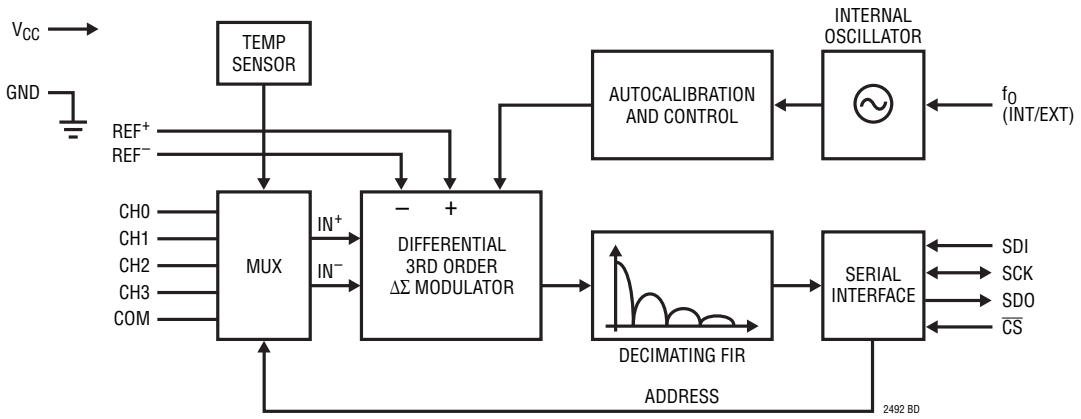
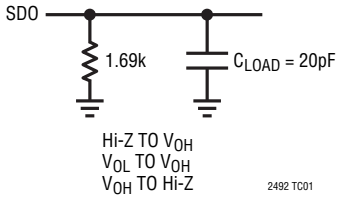
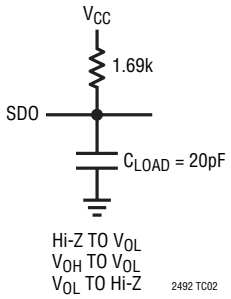


Figure 1. Functional Block Diagram

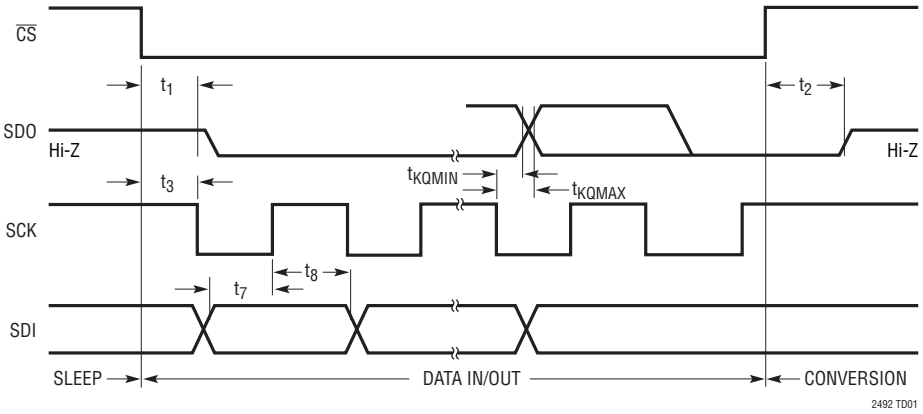
TEST CIRCUITS



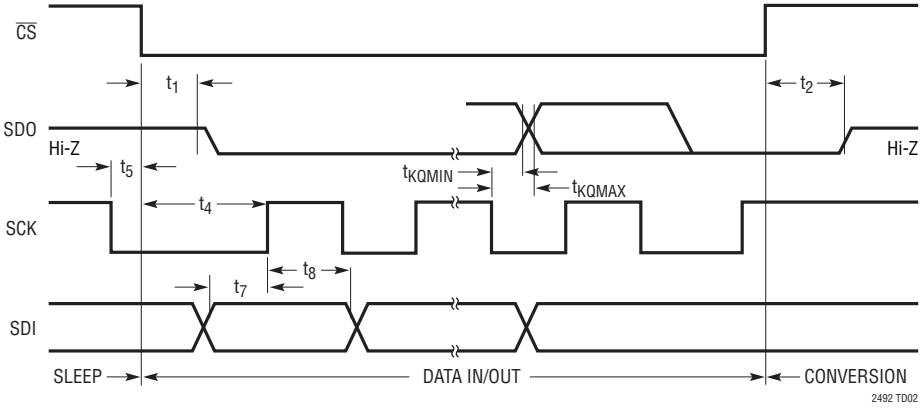


TIMING DIAGRAMS

Timing Diagram Using Internal SCK (SCK HIGH with $\overline{CS}\downarrow$)



Timing Diagram Using External SCK (SCK LOW with $\overline{CS}\downarrow$)



APPLICATIONS INFORMATION

CONVERTER OPERATION

Converter Operation Cycle

The LTC2492 is a multi-channel, low power, delta-sigma analog-to-digital converter with an easy to use 4-wire interface and automatic differential input current cancellation. Its operation is made up of four states (See Figure 2). The converter operating cycle begins with the conversion, followed by the sleep state and ends with the data input/output cycle. The 4-wire interface consists of serial data output (SDO), serial clock (SCK), chip select ($\overline{CS}$) and serial data input (SDI). The interface, timing, operation cycle, and data output format is compatible with Linear's entire family of SPI $\Delta\Sigma$ converters.

Initially, at power up, the LTC2492 performs a conversion. Once the conversion is complete, the device enters the sleep state. While in this sleep state, if $\overline{CS}$ is HIGH, power consumption is reduced by two orders of magnitude. The part remains in the sleep state as long as $\overline{CS}$ is HIGH. The conversion result is held indefinitely in a static shift register while the part is in the sleep state.

Once $\overline{CS}$ is pulled LOW, the device powers up, exits the sleep state, and enters the data input/output state. If $\overline{CS}$ is brought HIGH before the first rising edge of SCK, the device returns to the sleep state and the power is reduced. If $\overline{CS}$ is brought HIGH after the first rising edge of SCK, the data output cycle is aborted and a new conversion cycle begins. The data output corresponds to the conversion just completed. This result is shifted out on the serial data output pin (SDO) under the control of the serial clock pin (SCK). Data is updated on the falling edge of SCK allowing the user to reliably latch data on the rising edge of SCK (See Figure 3). The configuration data for the next conversion is also loaded into the device at this time. Data is loaded from the serial data input pin (SDI) on each rising edge of SCK. The data input/output cycle concludes once 32 bits are read out of the ADC or when $\overline{CS}$ is brought HIGH. The device automatically initiates a new conversion and the cycle repeats.

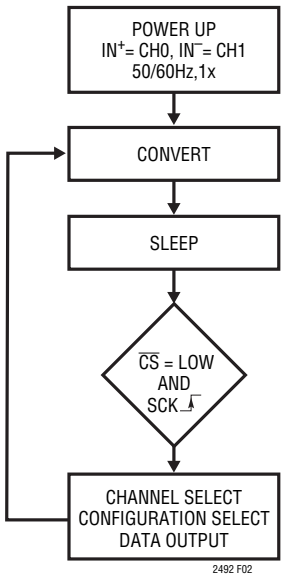


Figure 2. LTC2492 State Transition Diagram

Through timing control of the $\overline{CS}$ and SCK pins, the LTC2492 offers several flexible modes of operation (internal or external SCK and free-running conversion modes). These various modes do not require programming and do not disturb the cyclic operation described above. These modes of operation are described in detail in the Serial Interface Timing Modes section.

Ease of Use

The LTC2492 data output has no latency, filter settling delay, or redundant data associated with the conversion cycle. There is a one-to-one correspondence between the conversion and the output data. Therefore, multiplexing multiple analog inputs is straightforward. Each conversion, immediately following a newly selected input or mode, is valid and accurate to the full specifications of the device.

The LTC2492 automatically performs offset and full scale calibration every conversion cycle independent of the input channel selected. This calibration is transparent to the user and has no effect with the operation cycle described above. The advantage of continuous calibration is extreme stability of offset and full-scale readings with respect to time, supply voltage variation, input channel, and temperature drift.

APPLICATIONS INFORMATION

Easy Drive Input Current Cancellation

The LTC2492 combines a high precision delta-sigma ADC with an automatic, differential, input current cancellation front end. A proprietary front-end passive sampling network transparently removes the differential input current. This enables external RC networks and high impedance sensors to directly interface to the LTC2492 without external amplifiers. The remaining common mode input current is eliminated by either balancing the differential input impedances or setting the common mode input equal to the common mode reference (see Automatic Differential Input Current Cancellation Section). This unique architecture does not require on-chip buffers, thereby enabling signals to swing beyond ground and V_{CC}. Moreover, the cancellation does not interfere with the transparent offset and full-scale auto-calibration and the absolute accuracy (full scale + offset + linearity + drift) is maintained even with external RC networks.

Power-Up Sequence

The LTC2492 automatically enters an internal reset state when the power supply voltage V_{CC} drops below approximately 2V. This feature guarantees the integrity of the conversion result, input channel selection and serial clock mode.

When V_{CC} rises above this threshold, the converter creates an internal power-on-reset (POR) signal with a duration of approximately 4ms. The POR signal clears all internal registers. The conversion immediately following a POR cycle is performed on the input channel IN^+ = CH0, IN^- = CH1, simultaneous 50Hz/60Hz rejection and 1× output rate. The first conversion following a POR cycle is accurate within the specification of the device if the power supply voltage is restored to (2.7V to 5.5V) before the end of the POR interval. A new input channel, rejection mode, speed mode, or temperature selection can be programmed into the device during this first data input/output cycle.

Reference Voltage Range

This converter accepts a truly differential external reference voltage. The absolute/common mode voltage range for REF^+ and REF^- pins covers the entire operating range of the device (GND to V_{CC}). For correct converter operation, V_{REF} must be positive ($REF^+ > REF^-$).

The LTC2492 differential reference input range is 0.1V to V_{CC}. For the simplest operation, REF^+ can be shorted to V_{CC} and REF^- can be shorted to GND. The converter output noise is determined by the thermal noise of the front-end circuits, and as such, its value in nanovolts is nearly constant with reference voltage. A decrease in reference voltage will not significantly improve the converter's effective resolution. On the other hand, a decreased reference will improve the converter's overall INL performance.

Input Voltage Range

The LTC2492 input measurement range is $-0.5 \cdot V_{REF}$ to $+0.5 \cdot V_{REF}$ in both differential and single-ended configurations as shown in Figure 38. Highest linearity is achieved with Fully Differential drive and a constant common-mode voltage (Figure 38b). Other drive schemes may incur an INL error of approximately 50ppm. This error can be calibrated out using a three point calibration and a second-order curve fit.

The analog inputs are truly differential with an absolute, common mode range for the CH0 to CH3 and COM input pins extending from GND – 0.3V to V_{CC} + 0.3V. Outside these limits, the ESD protection devices begin to turn on and the errors due to input leakage current increase rapidly. Within these limits, the LTC2492 converts the bipolar differential input signal $V_{IN} = IN^+ - IN^-$ (where IN^+ and IN^- are the selected input channels), from $-FS = -0.5 \cdot V_{REF}$ to $+FS = 0.5 \cdot V_{REF}$ where $V_{REF} = REF^+ - REF^-$. Outside this range, the converter indicates the overrange or the underrange condition using distinct output codes (see Table 1).

Signals applied to the input (CH0 to CH3, COM) may extend 300mV below ground and above V_{CC}. In order to limit any fault current, resistors of up to 5k may be added in series with the input. The effect of series resistance on the converter accuracy can be evaluated from the curves presented in the Input Current/Reference Current sections. In addition, series resistors will introduce a temperature dependent error due to input leakage current. A 1nA input leakage current will develop a 1ppm offset error on a 5k resistor if V_{REF} = 5V. This error has a very strong temperature dependency.

APPLICATIONS INFORMATION

SERIAL INTERFACE PINS

The LTC2492 transmits the conversion result, reads the input configuration, and receives a start of conversion command through a synchronous 3- or 4-wire interface. During the conversion and sleep states, this interface can be used to access the converter status. During the data output state, it is used to read the conversion result, program the input channel, rejection frequency, speed multiplier, and select the temperature sensor.

Serial Clock Input/Output (SCK)

The serial clock pin (SCK) is used to synchronize the data input/output transfer. Each bit is shifted out of the SDO pin on the falling edge of SCK and data is shifted into the SDI pin on the rising edge of SCK.

The serial clock pin (SCK) can be configured as either a master (SCK is an output generated internally) or a slave (SCK is an input and applied externally). Master mode (Internal SCK) is selected by simply floating the SCK pin. Slave mode (External SCK) is selected by driving SCK low during power up and each falling edge of $\overline{CS}$. Specific details of these SCK modes are described in the Serial Interface Timing Modes section.

Serial Data Output (SDO)

The serial data output pin (SDO) provides the result of the last conversion as a serial bit stream (MSB first) during the data output state. In addition, the SDO pin is used as an end of conversion indicator during the conversion and sleep states.

When $\overline{CS}$ is HIGH, the SDO driver is switched to a high impedance state in order to share the data output line with other devices. If $\overline{CS}$ is brought LOW during the conversion phase, the $\overline{EOC}$ bit (SDO pin) will be driven HIGH. Once the conversion is complete, if $\overline{CS}$ is brought LOW, $\overline{EOC}$ will be driven LOW indicating the conversion is complete and the result is ready to be shifted out of the device.

Chip Select ($\overline{CS}$)

The active low $\overline{CS}$ pin is used to test the conversion status, enable I/O data transfer, initiate a new conversion, control the duration of the sleep state, and set the SCK mode.

At the conclusion of a conversion cycle, while $\overline{CS}$ is HIGH, the device remains in a low power sleep state where the supply current is reduced several orders of magnitude. In order to exit the sleep state and enter the data output state, $\overline{CS}$ must be pulled low. Data is now shifted out the SDO pin under control of the SCK pin as described previously.

A new conversion cycle is initiated either at the conclusion of the data output cycle (all 32 data bits read) or by pulling $\overline{CS}$ HIGH any time between the first and 32nd rising edges of the serial clock (SCK). In this case, the data output is aborted and a new conversion begins.

Serial Data Input (SDI)

The serial data input (SDI) is used to select the input channel, rejection frequency, speed multiplier and to access the integrated temperature sensor. Data is shifted into the device during the data output/input state on the rising edge of SCK while $\overline{CS}$ is low.

OUTPUT DATA FORMAT

The LTC2492 serial output stream is 32 bits long. The first bit indicates the conversion status, the second bit is always zero, and the third bit conveys sign information. The next 24 bits are the conversion result, MSB first. The remaining 5 bits are sub LSBs beyond the 24-bit level that may be included in averaging or discarded without loss of resolution.

Bit 31 (first output bit) is the end of conversion ($\overline{EOC}$) indicator. This bit is available on the SDO pin during the conversion and sleep states whenever $\overline{CS}$ is LOW. This bit is HIGH during the conversion cycle, goes LOW once the conversion is complete, and is Hi-Z when $\overline{CS}$ is HIGH.

Bit 30 (second output bit) is a dummy bit (DMY) and is always LOW.

Bit 29 (third output bit) is the conversion result sign indicator (SIG). If the selected input ($V_{IN} = IN^+ – IN^–$) is greater than 0V, this bit is HIGH. If $V_{IN} < 0$, this bit is LOW.

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Bit 28 (fourth output bit) is the most significant bit (MSB) of the result. This bit in conjunction with Bit 29 also provides underrange and overrange indication. If both Bit 29 and Bit 28 are HIGH, the differential input voltage is above +FS. If both Bit 29 and Bit 28 are LOW, the differential input voltage is below –FS. The function of these bits is summarized in Table 1.

Table 1. LTC2492 Status Bits

INPUT RANGE	BIT 31 $\overline{EOC}$	BIT 30 DMY	BIT 29 SIG	BIT 28 MSB
$V_{IN} \geq 0.5 \cdot V_{REF}$	0	0	1	1
$0V \leq V_{IN} < 0.5 \cdot V_{REF}$	0	0	1/0	0
$-0.5 \cdot V_{REF} \leq V_{IN} < 0V$	0	0	0	1
$V_{IN} < -0.5 \cdot V_{REF}$	0	0	0	0

Bits 28 to 5 are the 24-bit conversion result MSB first.

Bit 5 is the least significant bit (LSB_{24}).

Bits 4 to 0 are sub LSBs below the 24-bit level. Bits 4 to 0 may be included in averaging or discarded without loss of resolution.

Data is shifted out of the SDO pin under control of the serial clock (SCK) (see Figure 3). Whenever $\overline{CS}$ is HIGH, SDO remains high impedance and SCK is ignored.

In order to shift the conversion result out of the device, $\overline{CS}$ must first be driven LOW. $\overline{EOC}$ is seen at the SDO pin of the device once $\overline{CS}$ is pulled LOW. $\overline{EOC}$ changes in real time as a function of the internal oscillator or the clock applied to the f_O pin from HIGH to LOW at the completion of a conversion. This signal may be used as an interrupt for an external microcontroller. Bit 31 ($\overline{EOC}$) can be captured on the first rising edge of SCK. Bit 30 is shifted out of the device on the first falling edge of SCK. The final data bit (Bit 0) is shifted out on the on the falling edge of the 31st SCK and may be latched on the rising edge of the 32nd SCK pulse. On the falling edge of the 32nd SCK pulse, SDO goes HIGH indicating the initiation of a new conversion cycle. This bit serves as $\overline{EOC}$ (Bit 31) for the next conversion cycle. Table 2 summarizes the output data format.

As long as the voltage on the IN^+ and IN^- pins remains between –0.3V and V_{CC} + 0.3V (absolute maximum operating range) a conversion result is generated for any differential input voltage V_{IN} from –FS = –0.5 • V_{REF} to +FS = 0.5 • V_{REF}. For differential input voltages greater than +FS, the conversion result is clamped to the value corresponding to +FS + 1LSB. For differential input voltages below –FS, the conversion result is clamped to the value –FS – 1LSB.

INPUT DATA FORMAT

The LTC2492 serial input word is 13 bits long and contains two distinct sets of data. The first set (SGL, ODD, A2, A1, A0) is used to select the input channel. The second set of data (IM, FA, FB, SPD) is used to select the frequency rejection, speed mode (1×, 2×), and temperature measurement.

After power up, the device initiates an internal reset cycle which sets the input channel to CH0 to CH1 (IN^+ = CH0, IN^- = CH1), the frequency rejection to simultaneous 50Hz/60Hz, and 1× output rate (auto-calibration enabled). The first conversion automatically begins at power up using this

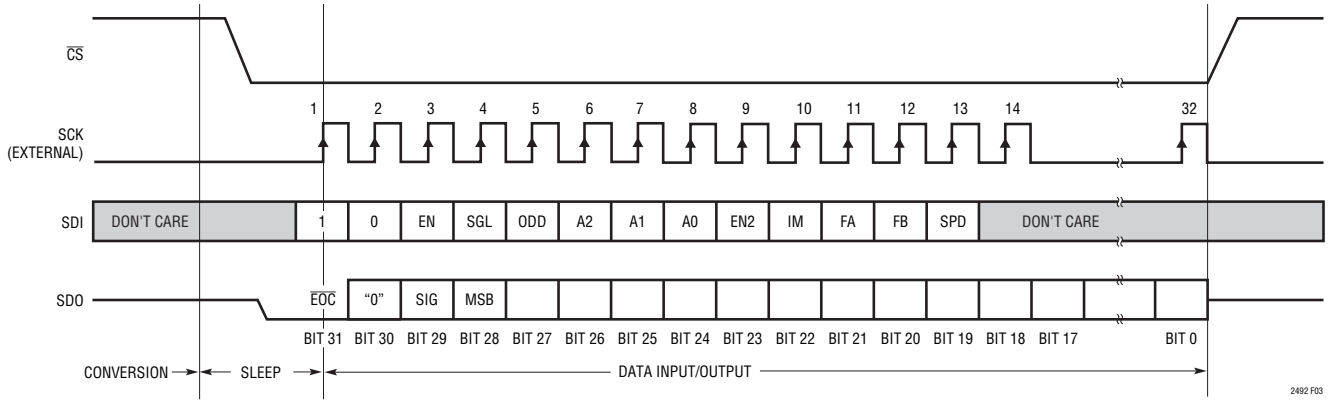

Figure 3. Channel Selection, Configuration Selection and Data Output Timing

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Table 2. Output Data Format

DIFFERENTIAL INPUT VOLTAGE V_{IN}*	BIT 31 $\overline{EOC}$	BIT 30 DMY	BIT 29 SIG	BIT 28 MSB	BIT 27	BIT 26	BIT 25	…	BIT 5 LSB	BITS 4 to 0 SUB LSBs
V_{IN}* ≥ 0.5 • V_{REF}**	0	0	1	1	0	0	0	…	0	00000
0.5 • V_{REF}** – 1LSB	0	0	1	0	1	1	1	…	1	XXXXX
0.25 • V_{REF}**	0	0	1	0	1	0	0	…	0	XXXXX
0.25 • V_{REF}** – 1LSB	0	0	1	0	0	1	1	…	1	XXXXX
0	0	0	1/0†	0	0	0	0	…	0	XXXXX
–1LSB	0	0	0	1	1	1	1	…	1	XXXXX
–0.25 • V_{REF}**	0	0	0	1	1	0	0	…	0	XXXXX
–0.25 • V_{REF}** – 1LSB	0	0	0	1	0	1	1	…	1	XXXXX
–0.5 • V_{REF}**	0	0	0	1	0	0	0	…	0	XXXXX
V_{IN}* < –0.5 • V_{REF}**	0	0	0	0	1	1	1	…	X	XXXXX‡

* The differential input voltage $V_{IN} = IN^+ – IN^–$.
** The differential reference voltage $V_{REF} = REF^+ – REF^–$. Sub LSBs are below the 24-bit level. They may be included in averaging, or discarded without loss of resolution.
† The sign bit changes state during the 0 output code when the device is operating in the 2x speed mode.
‡ The underrange output code is 0X0FFFFXXX in 2x mode.

default configuration. Once the conversion is complete, a new word may be written into the device.

The first three bits shifted into the device consist of two preamble bits and an enable bit. These bits are used to enable the device configuration and input channel selection. Valid settings for these three bits are 000, 100 and 101. Other combinations should be avoided. If the first three bits are 000 or 100, the following data is ignored (don't care) and the previously selected input channel and configuration remain valid for the next conversion.

If the first three bits shifted into the device are 101, then the next five bits select the input channel for the next conversion cycle (see Table 3).

Table 3 Channel Selection

MUX ADDRESS					CHANNEL SELECTION				
SGL	ODD/ SIGN	A2	A1	A0	0	1	2	3	COM
*0	0	0	0	0	IN^+	$IN^–$			
0	0	0	0	1			IN^+	$IN^–$	
0	1	0	0	0	$IN^–$	IN^+			
0	1	0	0	1			$IN^–$	IN^+	
1	0	0	0	0	IN^+				$IN^–$
1	0	0	0	1			IN^+		$IN^–$
1	1	0	0	0		IN^+			$IN^–$
1	1	0	0	1				IN^+	$IN^–$

*Default at power up

The first input bit (SGL) following the 101 sequence determines if the input selection is differential (SGL = 0) or single-ended (SGL = 1). For SGL = 0, two adjacent channels can be selected to form a differential input. For SGL = 1, one of four channels is selected as the positive input. The negative input is COM for all single-ended operations. The remaining four bits (ODD, A2, A1, A0) determine which channel(s) is/are selected and the polarity (for a differential input).

The next serial input bit immediately following the input channel selection is the enable bit for the conversion configuration (EN2). If this bit is set to 0, then the next conversion is performed using the previously selected converter configuration.

A new configuration can be loaded into the device by setting EN2 = 1 (see Table 4). The first bit (IM) is used to select the internal temperature sensor. If IM = 1, the following conversion will be performed on the internal temperature sensor rather than the selected input channel. The next two bits (FA and FB) are used to set the rejection frequency. The final bit (SPD) is used to select either the 1x output rate if SPD = 0 (auto-calibration is enabled and the offset is continuously calibrated and removed from the final conversion result) or the 2x output rate if SPD = 1 (offset calibration disabled, multiplexing output rates up to 15Hz with no latency). When IM = 1 (temperature measurement) SPD will be ignored and the device will

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Table 4. Converter Configuration

1	0	EN	SGL	ODD	A2	A1	A0	EN2	IM	FA	FB	SPD	CONVERTER CONFIGURATION
1	0	0	X	X	X	X	X	X	X	X	X	X	Keep Previous
1	0	1	X	X	X	X	X	0	X	X	X	X	Keep Previous
0	0	0	X	X	X	X	X	X	X	X	X	X	Keep Previous
1	0	1	X	X	X	X	X	1	0	0	0	0	External Input (See Table 3) 50Hz/60Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	0	0	1	0	External Input (See Table 3) 50Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	0	1	0	0	External Input (See Table 3) 60Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	0	0	0	1	External Input (See Table 3) 50Hz/60Hz Rejection, 2x
1	0	1	X	X	X	X	X	1	0	0	1	1	External Input (See Table 3) 50Hz Rejection, 2x
1	0	1	X	X	X	X	X	1	0	1	0	1	External Input (See Table 3) 60Hz Rejection, 2x
1	0	1	X	X	X	X	X	1	1	0	0	X	Measure Temperature 50Hz/60Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	1	0	1	X	Measure Temperature 50Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	1	1	0	X	Measure Temperature 60Hz Rejection, 1x
1	0	1	X	X	X	X	X	1	X	1	1	X	Reserved, Do Not Use

operate in 1× mode. The configuration remains valid until a new input word with EN = 1 (the first three bits are 101) and EN2 = 1 is shifted into the device.

Rejection Mode (FA, FB)

The LTC2492 includes a high accuracy on-chip oscillator with no required external components. Coupled with an integrated 4th order digital lowpass filter, the LTC2492 rejects line frequency noise. In the default mode, the LTC2492 simultaneously rejects 50Hz and 60Hz by at least 87dB. If more rejection is required, the LTC2492 can be configured to reject 50Hz or 60Hz to better than 110dB.

Speed Mode (SPD)

Every conversion cycle, two conversions are combined to remove the offset (default mode). This result is free from offset and drift. In applications where the offset is not critical, the auto-calibration feature can be disabled with the benefit of twice the output rate. While operating in the 2x mode (SPD = 1), the linearity and full-scale errors are unchanged from the 1× mode performance. In both the 1× and 2× mode there is no latency. This enables input steps or multiplexer changes to settle in a single conversion cycle, easing system overhead and increasing the effective conversion rate. During temperature measurements, the 1× mode is always used independent of the value of SPD.

Temperature Sensor

The LTC2492 includes an integrated temperature sensor. The temperature sensor is selected by setting IM = 1. The digital output is proportional to the absolute temperature of the device. This feature allows the converter to perform cold junction compensation for external thermocouples or continuously remove the temperature effects of external sensors.

The internal temperature sensor output is 28mV at 27°C (300°K), with a slope of 93.5µV/°C independent of V_{REF} (see Figures 4 and 5). Slope calibration is not required if the reference voltage (V_{REF}) is known. A 5V reference has a slope of 314 $LSBs_{24}$/°C. The temperature is calculated

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from the output code ($DATAOUT_{24}$) for a 5V reference using the following formula:

$T_K = DATAOUT_{24}/314$ in Kelvin

If a different value of V_{REF} is used, the temperature output is:

$T_K = DATAOUT_{24} \bullet V_{REF}/1570$ in Kelvin

If the value of V_{REF} is not known, the slope is determined by measuring the temperature sensor at a known temperature T_N (in °K) and using the following formula:

$SLOPE = DATAOUT_{24}/T_N$

This value of slope can be used to calculate further temperature readings using:

$T_K = DATAOUT_{24}/SLOPE$

All Kelvin temperature readings can be converted to T_C (°C) using the fundamental equation:

$T_C = T_K – 273$

SERIAL INTERFACE TIMING MODES

The LTC2492's 4-wire interface is SPI and MICROWIRE compatible. This interface offers several flexible modes of operation. These include internal/external serial clock, 3- or 4-wire I/O, single cycle or continuous conversion. The following sections describe each of these timing modes in detail. In all cases, the converter can use the internal oscillator (f_O = LOW) or an external oscillator connected to the f_O pin. For each mode, the operating cycle, data input format, data output format, and performance remain the same. Refer to Table 5 for a summary.

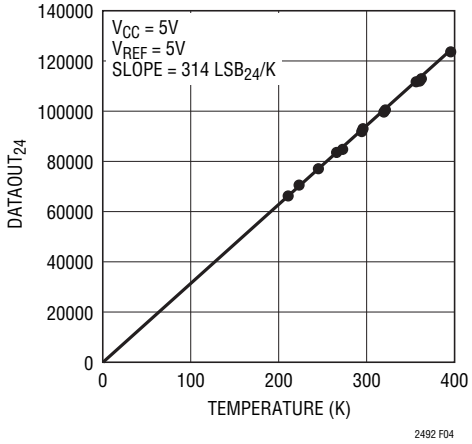

Figure 4. Internal PTAT Digital Output vs Temperature

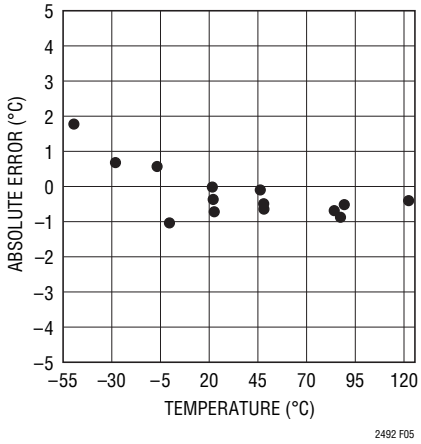

Figure 5. Absolute Temperature Error

Table 5. Serial Interface Timing Modes

CONFIGURATION	SCK SOURCE	CONVERSION CYCLE CONTROL	DATA OUTPUT CONTROL	CONNECTION AND WAVEFORMS
External SCK, Single Cycle Conversion	External	$\overline{CS}$ and SCK	$\overline{CS}$ and SCK	Figures 6, 7
External SCK, 3-Wire I/O	External	SCK	SCK	Figure 8
Internal SCK, Single Cycle Conversion	Internal	$\overline{CS}\downarrow$	$\overline{CS}\downarrow$	Figures 9, 10
Internal SCK, 3-Wire I/O, Continuous Conversion	Internal	Continuous	Internal	Figure 11

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External Serial Clock, Single Cycle Operation

This timing mode uses an external serial clock to shift out the conversion result and $\overline{CS}$ to monitor and control the state of the conversion cycle (see Figure 6).

The external serial clock mode is selected during the power-up sequence and on each falling edge of $\overline{CS}$. In order to enter and remain in the external SCK mode of operation, SCK must be driven LOW both at power up and on each $\overline{CS}$ falling edge. If SCK is HIGH on the falling edge of $\overline{CS}$, the device will switch to the internal SCK mode.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled LOW in order to monitor the state of the converter. While $\overline{CS}$ is LOW, $\overline{EOC}$ is output to the SDO pin.

$\overline{EOC}$ = 1 while a conversion is in progress and $\overline{EOC}$ = 0 if the conversion is complete and the device is in the sleep state. Independent of $\overline{CS}$, the device automatically enters the sleep state once the conversion is complete; however, in order to reduce the power, $\overline{CS}$ must be HIGH.

When the device is in the sleep state, its conversion result is held in an internal static shift register. The device remains in the sleep state until the first rising edge of SCK is seen while $\overline{CS}$ is LOW. The input data is then shifted in via the SDI pin on each rising edge of SCK (including the first rising edge). The channel selection and converter configuration mode will be used for the following conversion cycle. If the input channel or converter configuration is changed during this I/O cycle, the new settings take effect on the conversion cycle following the data input/output cycle. The output data is shifted out the SDO pin on each falling edge of SCK. This enables external circuitry to latch the output on the rising edge of SCK. $\overline{EOC}$ can be latched on the first rising edge of SCK and the last bit of the conversion result can be latched on the 32nd rising edge of SCK. On the 32nd falling edge of SCK, the device begins a new conversion and SDO goes HIGH ($\overline{EOC}$ = 1) indicating a conversion is in progress.

At the conclusion of the data cycle, $\overline{CS}$ may remain LOW and $\overline{EOC}$ monitored as an end-of-conversion interrupt.

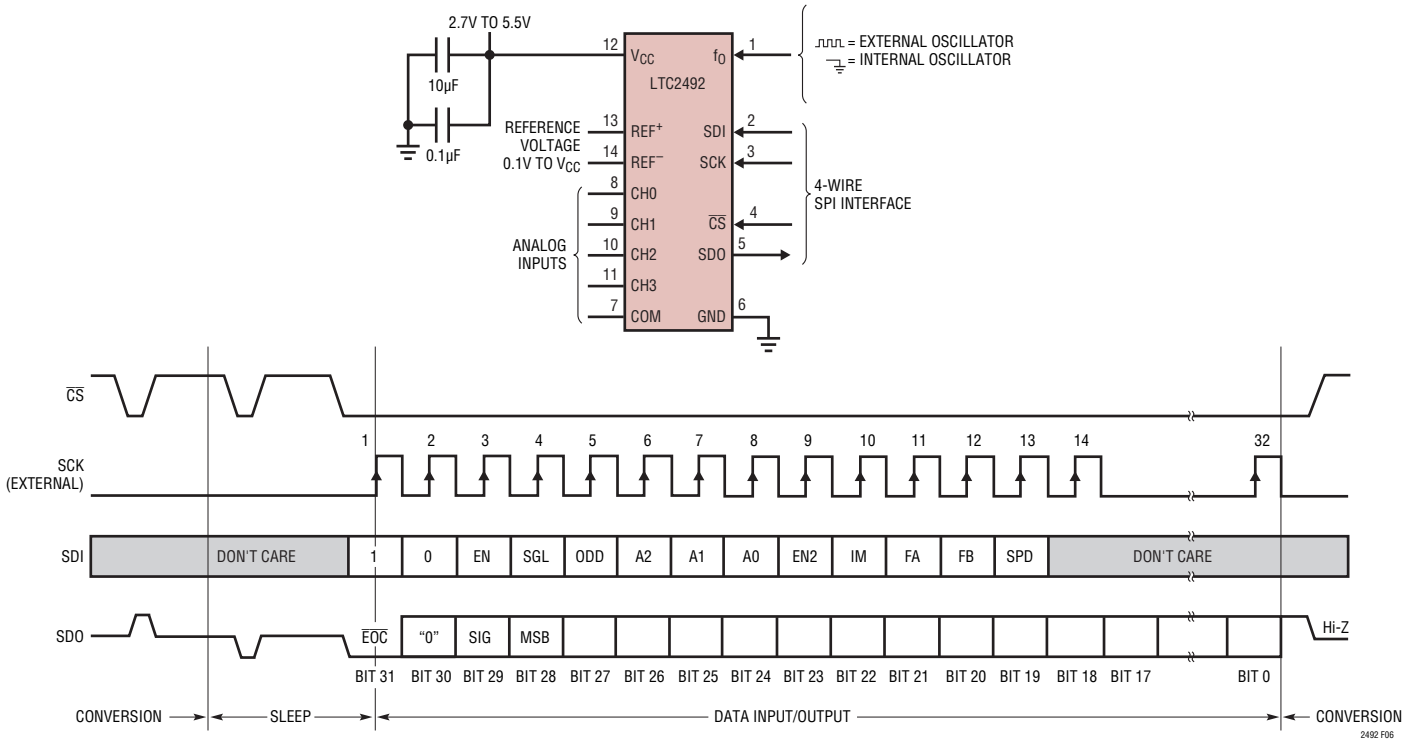

Figure 6. External Serial Clock, Single Cycle Operation

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Typically, $\overline{CS}$ remains LOW during the data output/input state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH any time between the 1st falling edge and the 32nd falling edge of SCK (see Figure 7). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of $\overline{CS}$ occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle. If $\overline{CS}$ goes high between the 8th falling edge and the 16th falling edge of SCK, the new channel is still loaded, but the converter configuration remains unchanged. In order to program both the input channel and converter configuration, $\overline{CS}$ must go high after the 16th falling edge of SCK (at this point all data has been shifted into the device).

External Serial Clock, 3-Wire I/O

This timing mode uses a 3-wire serial I/O interface. The conversion result is shifted out of the device by an externally generated serial clock (SCK) signal (see Figure 8). $\overline{CS}$ is permanently tied to ground, simplifying the user interface or isolation barrier.

The external serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle typically concludes 4ms after V_{CC} exceeds 2V. The level applied to SCK at this time determines if SCK is internally generated or externally applied. In order to enter the external SCK mode, SCK must be driven LOW prior to the end of the POR cycle.

Since $\overline{CS}$ is tied LOW, the end-of-conversion ($\overline{EOC}$) can be continuously monitored at the SDO pin during the convert and sleep states. $\overline{EOC}$ may be used as an interrupt to an external controller. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 once the conversion is complete.

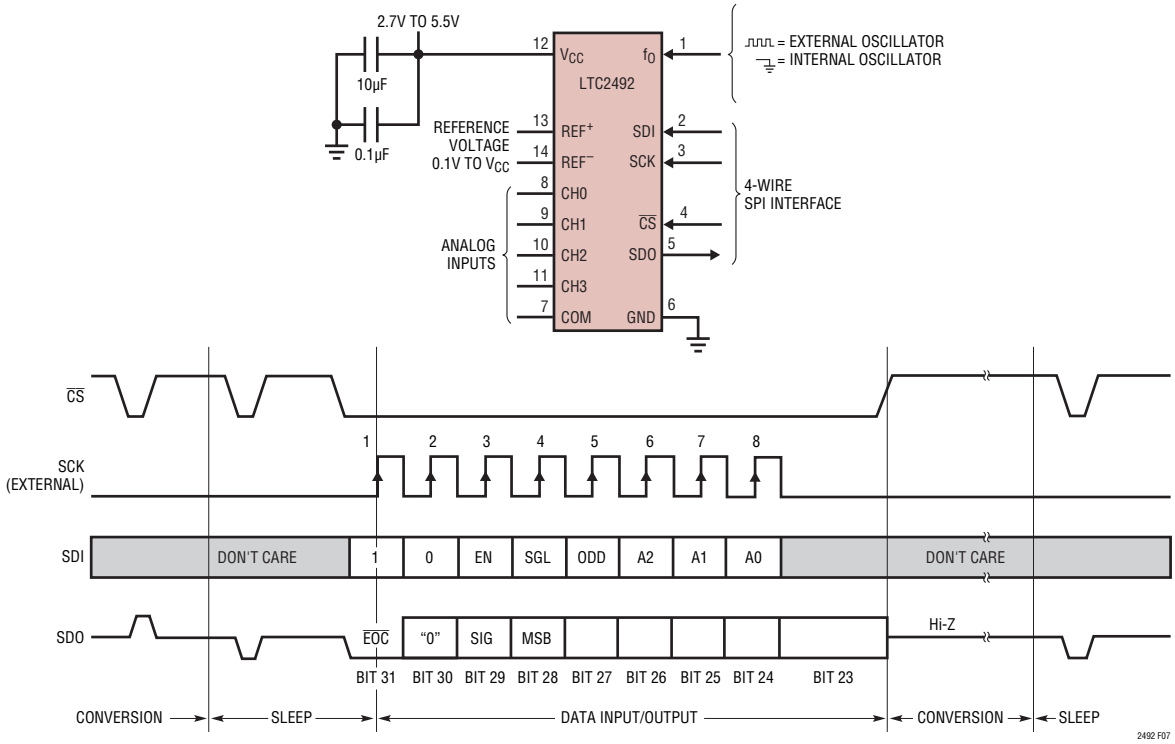

Figure 7. External Serial Clock, Reduced Output Data Length and Valid Channel Selection

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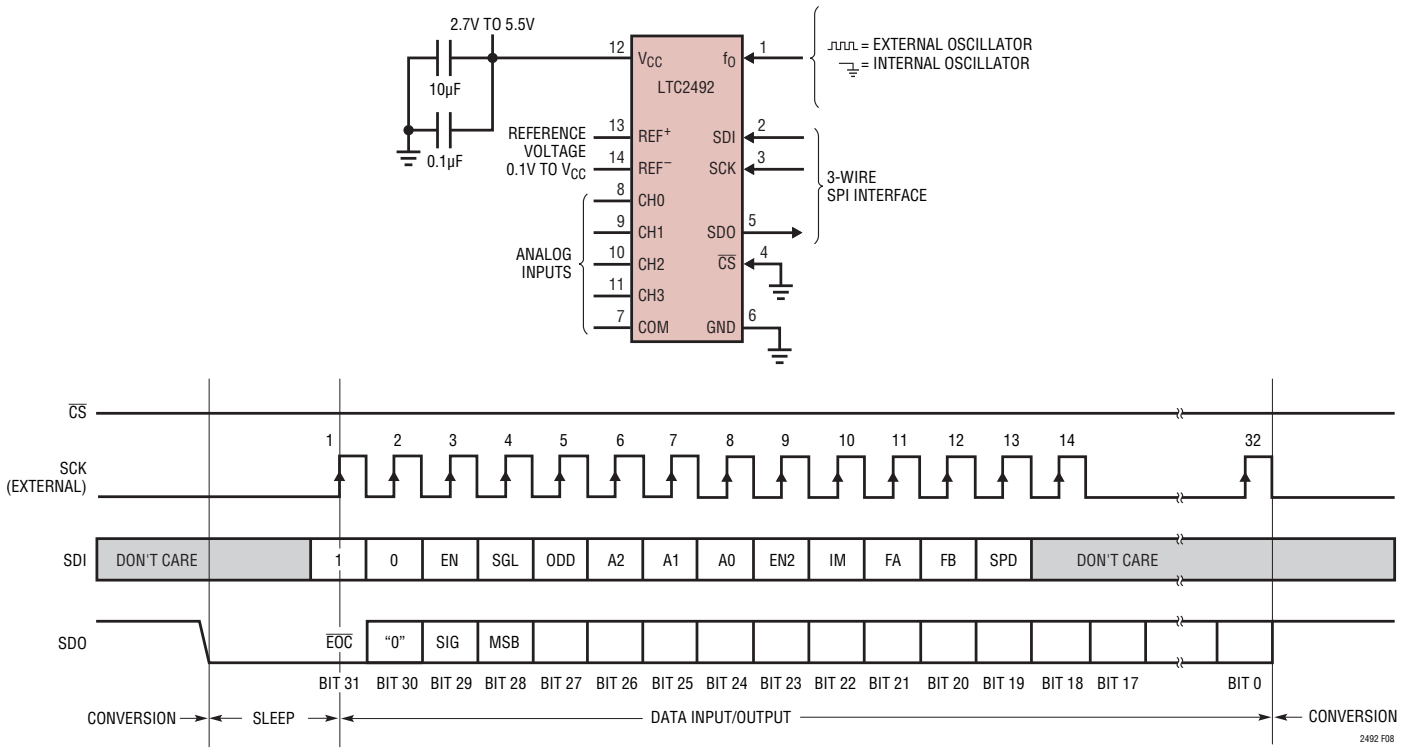

Figure 8. External Serial Clock, 3-Wire Operation (`C`S = 0)

On the falling edge of $\overline{EOC}$, the conversion result is loading into an internal static shift register. The output data can now be shifted out the SDO pin under control of the externally applied SCK signal. Data is updated on the falling edge of SCK. The input data is shifted into the device through the SDI pin on the rising edge of SCK. On the 32nd falling edge of SCK, SDO goes HIGH, indicating a new conversion has begun. This data now serves as $\overline{EOC}$ for the next conversion.

Internal Serial Clock, Single Cycle Operation

This timing mode uses the internal serial clock to shift out the conversion result and $\overline{CS}$ to monitor and control the state of the conversion cycle (see Figure 9).

In order to select the internal serial clock timing mode, the serial clock pin (SCK) must be floating or pulled HIGH before the conclusion of the POR cycle and prior to each falling edge of $\overline{CS}$. An internal weak pull-up resistor is active on the SCK pin during the falling edge of $\overline{CS}$; therefore, the internal SCK mode is automatically selected if SCK is not externally driven.

The serial data output pin (SDO) is Hi-Z as long as $\overline{CS}$ is HIGH. At any time during the conversion cycle, $\overline{CS}$ may be pulled low in order to monitor the state of the converter. Once $\overline{CS}$ is pulled LOW, SCK goes LOW and $\overline{EOC}$ is output to the SDO pin. $\overline{EOC}$ = 1 while the conversion is in progress and $\overline{EOC}$ = 0 if the device is in the sleep state.

When testing $\overline{EOC}$, if the conversion is complete ($\overline{EOC}$ = 0), the device will exit sleep state. In order to return to the sleep state and reduce the power consumption, $\overline{CS}$ must be pulled HIGH before the device pulls SCK HIGH. When the device is using its own internal oscillator (f_O is tied LOW), the first rising edge of SCK occurs 12µs ($t_{EOCTEST}$ = 12µs) after the falling edge of $\overline{CS}$. If f_O is driven by an external oscillator of frequency f_{EOSC}, then $t_{EOCTEST} = 3.6/f_{EOSC}$.

If $\overline{CS}$ remains LOW longer than $t_{EOCTEST}$, the first rising edge of SCK will occur and the conversion result is shifted out the SDO pin on the falling edge of SCK. The serial input word (SDI) is shifted into the device on the rising edge of SCK.

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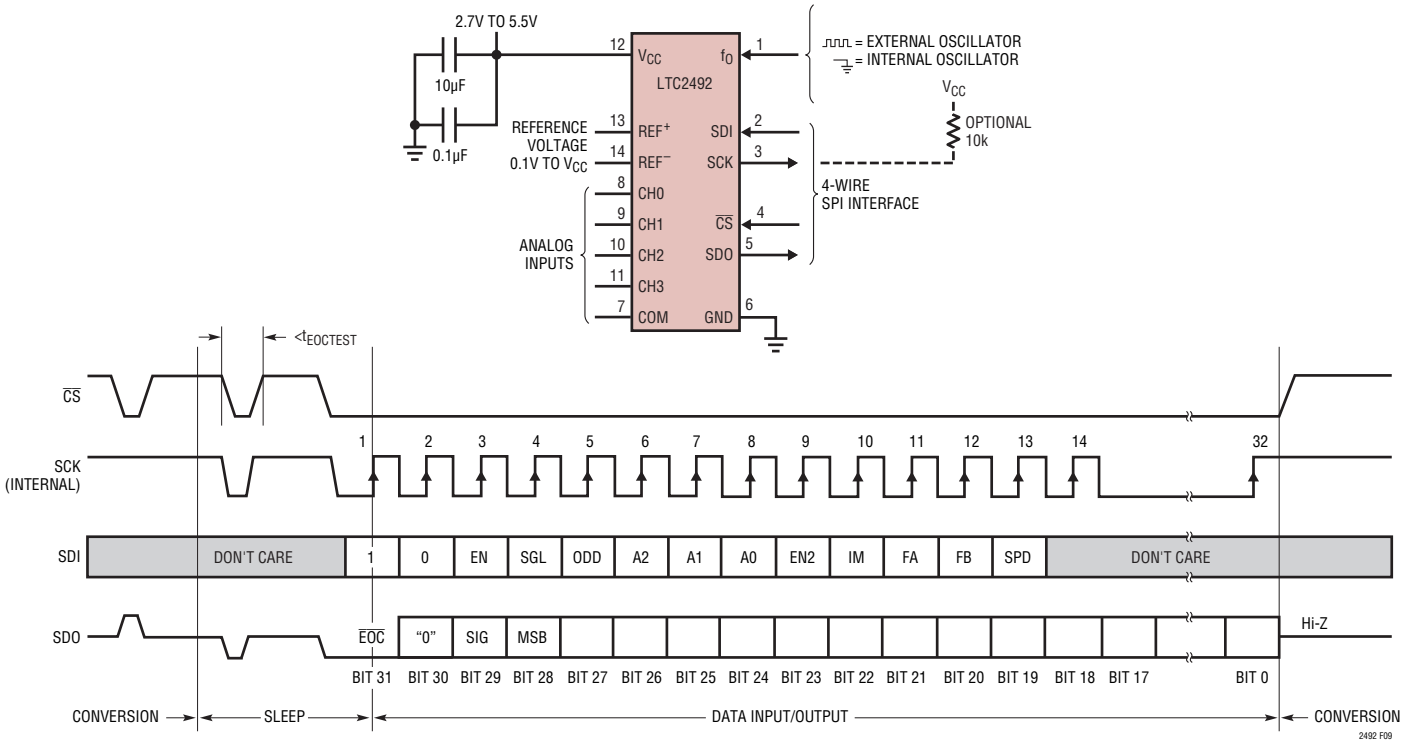

Figure 9. Internal Serial Clock, Single Cycle Operation

After the 32nd rising edge of SCK a new conversion automatically begins. SDO goes HIGH ($\overline{EOC}$ = 1) and SCK remains HIGH for the duration of the conversion cycle. Once the conversion is complete, the cycle repeats.

Typically, $\overline{CS}$ remains LOW during the data output state. However, the data output state may be aborted by pulling $\overline{CS}$ HIGH any time between the 1st rising edge and the 32nd falling edge of SCK (see Figure 10). On the rising edge of $\overline{CS}$, the device aborts the data output state and immediately initiates a new conversion. In order to program a new input channel, 8 SCK clock pulses are required. If the data output sequence is aborted prior to the 8th falling edge of SCK, the new input data is ignored and the previously selected input channel remains valid. If the rising edge of $\overline{CS}$ occurs after the 8th falling edge of SCK, the new input channel is loaded and valid for the next conversion cycle. If $\overline{CS}$ goes high between the 8th falling edge and the 16th falling edge of SCK, the new channel is still loaded, but the converter configuration remains unchanged. In order to program both the input channel and converter configuration, $\overline{CS}$ must go high after the 16th falling edge of SCK (at this point all data has been shifted into the device).

Internal Serial Clock, 3-Wire I/O, Continuous Conversion.

This timing mode uses a 3-wire interface. The conversion result is shifted out of the device by an internally generated serial clock (SCK) signal (see Figure 11). In this case, $\overline{CS}$ is permanently tied to ground, simplifying the user interface or transmission over an isolation barrier.

The internal serial clock mode is selected at the end of the power-on reset (POR) cycle. The POR cycle is concluded approximately 4ms after V_{CC} exceeds 2V. An internal weak pull-up is active during the POR cycle; therefore, the internal serial clock timing mode is automatically selected if SCK is floating or driven HIGH.

During the conversion, the SCK and the serial data output pin (SDO) are HIGH ($\overline{EOC}$ = 1). Once the conversion is complete, SCK and SDO go LOW ($\overline{EOC}$ = 0) indicating the conversion has finished and the device has entered the sleep state. The device remains in the sleep state a minimum amount of time (1/2 the internal SCK period) then immediately begins outputting and inputting data.

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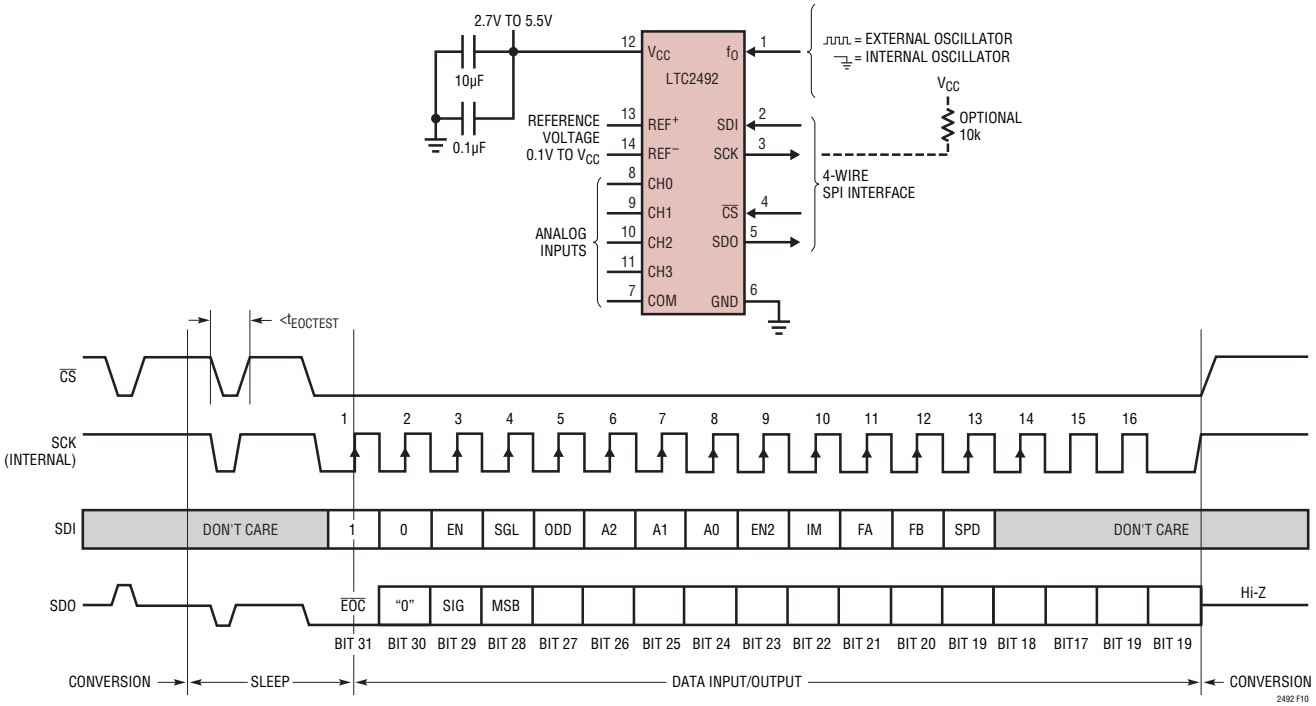

Figure 10. Internal Serial Clock, Reduced Data Output Length with Valid Channel and Configuration Selection

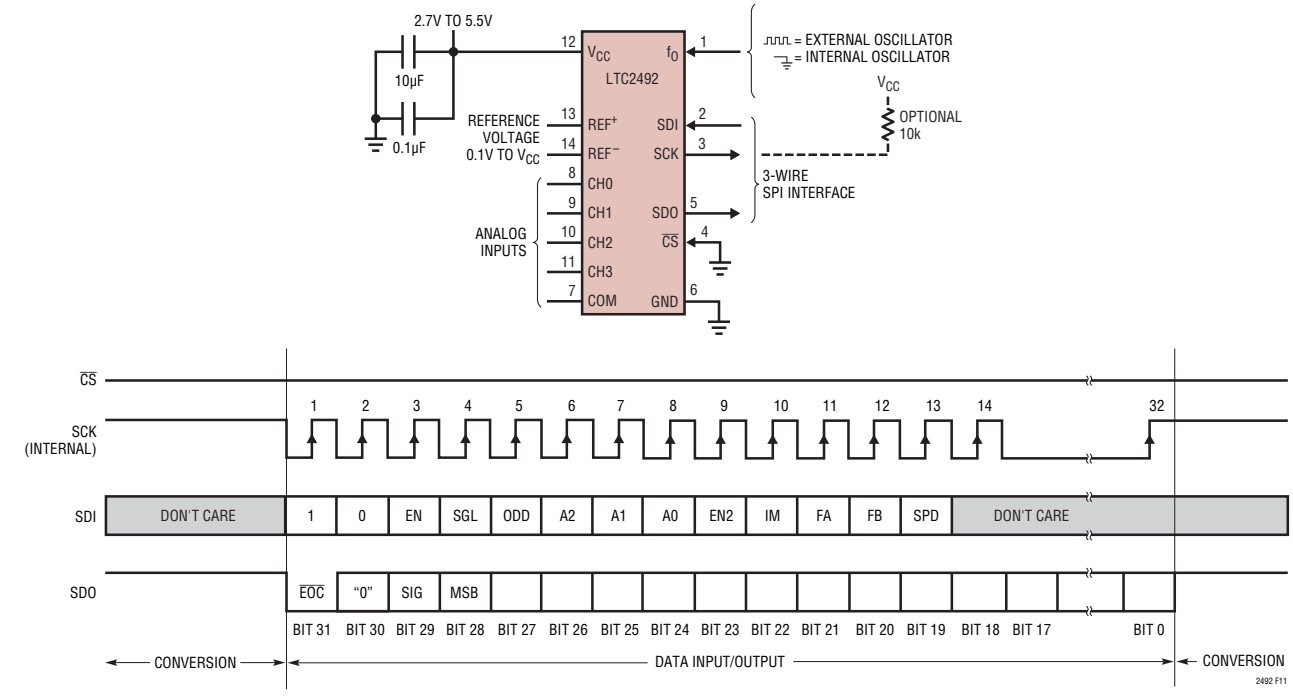

Figure 11. Internal Serial Clock, Continuous Operation