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Precision Triple/Dual Input UV, OV and Negative Voltage Monitor

FEATURES

- **Two Low Voltage Adjustable Inputs (0.5V)**
- **Pin Selectable Input Polarity Allows Negative and OV Monitoring**
- **Guaranteed Threshold Accuracy: ±1.5%**
- **6.5V Shunt Regulator for High Voltage Operation**
- **Low 50µA Quiescent Current**
- Buffered 1V Reference for Negative Supply Offset
- Input Glitch Rejection
- Adjustable Reset Timeout Period
- Selectable Internal Timeout Saves Components
- Open-Drain $\overline{RST}$ Output
- Accurate UVLO for 2.5V, 3.3V, 5V Systems
- Ultralow Voltage Reset: V_{CC} = 0.5V Guaranteed
- Space Saving 8-Lead TSOT-23 and 3mm × 2mm DFN Packages

APPLICATIONS

- Desktop and Notebook Computers
- Handheld Devices
- Network Servers
- Core, I/O Monitor
- Automotive

DESCRIPTION

The LTC®2909 is a dual input monitor intended for a variety of system monitoring applications. Polarity selection and a buffered reference output allow the LTC2909 to monitor positive and negative supplies for undervoltage (UV) and overvoltage (OV) conditions.

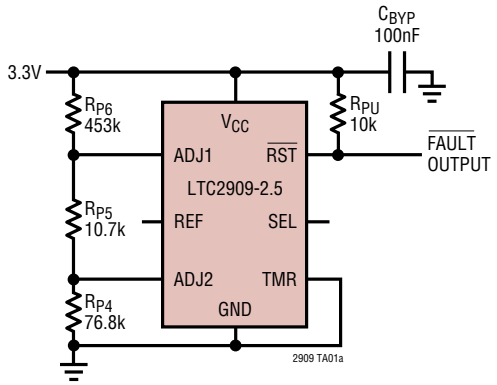
The two inputs have a nominal 0.5V threshold, featuring tight 1.5% threshold accuracy over the entire operating temperature range. Glitch filtering ensures reliable reset operation without false triggering. A third fixed-threshold UVLO monitor on the part's V_{CC} (also 1.5% accuracy) is available for standard logic supplies.

The common reset output has a timeout that may use a preset 200ms, be set by an external capacitor or be disabled. A three-state input pin sets the input polarity of each adjustable input without requiring any external components.

The LTC2909 provides a highly versatile, precise, space-conscious, micropower solution for supply monitoring.

TYPICAL APPLICATION

3.3V UV/OV (Window) Monitor Application with 200ms Internal Timeout (3.3V Logic Out)



SEL Pin Connection for Input Polarity Combinations

POLARITY		
ADJ1	ADJ2	SEL PIN
+	+	V_{CC}
+	–	OPEN
–	–	GND

ABSOLUTE MAXIMUM RATINGS (Notes 1, 2)

Terminal Voltages
- V_{CC} (Note 3) ..... –0.3V to 6V
- SEL, $\overline{RST}$ ..... –0.3V to 7.5V
- ADJ1, ADJ2 ..... –0.3V to 7.5V
- TMR ..... –0.3V to (V_{CC} + 0.3V)

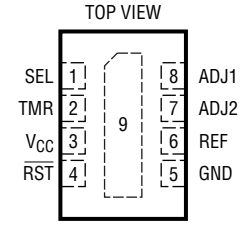
Terminal Currents
- I_{VCC} (Note 3) ..... ±10mA
- I_{REF} ..... ±1mA

Operating Temperature Range
- LTC2909C ..... 0°C to 70°C
- LTC2909I ..... –40°C to 85°C

Storage Temperature Range
- DFN ..... –65°C to 125°C
- TSOT-23 ..... –65°C to 150°C

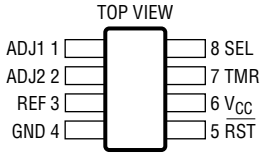
Lead Temperature (Soldering, 10 sec)
- TSOT-23 ..... 300°C

PACKAGE/ORDER INFORMATION



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN
T_{JMAX} = 125°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) MAY BE LEFT OPEN OR TIED TO GND
(PCB CONNECTION REQUIRED FOR STATED θ_{JA})

ORDER PART NUMBER	DDB PART* MARKING
LTC2909CDDB-2.5	LBXG
LTC2909IDDB-2.5	LBXG
LTC2909CDDB-3.3	LBZS
LTC2909IDDB-3.3	LBZS
LTC2909CDDB-5	LBZT
LTC2909IDDB-5	LBZT



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23
T_{JMAX} = 125°C, θ_{JA} = 250°C/W

ORDER PART NUMBER	TS8 PART* MARKING
LTC2909CTS8-2.5	LTBXF
LTC2909ITS8-2.5	LTBXF
LTC2909CTS8-3.3	LTBZV
LTC2909ITS8-3.3	LTBZV
LTC2909CTS8-5	LTBZW
LTC2909ITS8-5	LTBZW

Order Options Tape and Reel: Add #TR Lead Free: Add #PBF Lead Free Tape and Reel: Add #TRPBF
Lead Free Part Marking: http://www.linear.com/leadfree/

*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for parts specified with wider operating temperature ranges.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{CC} = 2.5V (LTC2909-2.5), V_{CC} = 3.3V (LTC2909-3.3), V_{CC} = 5V (LTC2909-5), ADJ1 = ADJ2 = 0.55V, SEL = floating, unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{CC(MIN)}$	Operating Supply Voltage	$\overline{RST}$ in Correct State	●	0.5			V
$V_{CC(SHUNT)}$	V_{CC} Shunt Regulation Voltage	I_{VCC} = 1mA, I_{VREF} = 0	●	6.0	6.5	6.9	V
I_{CC}	V_{CC} Input Current	2.175 < V_{CC} < 6V	●		50	150	µA
V_{RT}	ADJ Input Threshold		●	0.4925	0.5000	0.5075	V
ΔV_{RT}	ADJ Hysteresis (Note 4)	TMR = V_{CC}		1.5	3.5	10.0	mV
I_{ADJ}	ADJ Input Current	V_{ADJ} = 0.55V	●			±15	nA
$V_{CC(UVLO)}$	V_{CC} UVLO Threshold	LTC2909-2.5 LTC2909-3.3 LTC2909-5	● ● ●	2.175 2.871 4.350	2.213 2.921 4.425	2.250 2.970 4.500	V V V
$\Delta V_{CC(UVLO)}$	UVLO Hysteresis (Note 4)	TMR = V_{CC}		0.3	0.7	2.0	%
V_{REF}	Buffered Reference Voltage	V_{CC} > 2.175V, I_{VREF} = ±1mA	●	0.985	1.000	1.015	V
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 1V	●	–1.5	–2.1	–2.7	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1V	●	1.5	2.1	2.7	µA
$t_{\overline{RST}(EXT)}$	Reset Timeout Period, External	C_{TMR} = 2.2nF	●	16	20	25	ms
$t_{\overline{RST}(INT)}$	Reset Timeout Period, Internal	V_{TMR} = 0V	●	150	200	260	ms
$V_{TMR(DIS)}$	Timer Disable Voltage	V_{TMR} Rising	●	V_{CC} – 0.36	V_{CC} – 0.25	V_{CC} – 0.16	V
$\Delta V_{TMR(DIS)}$	Timer Disable Hysteresis	V_{TMR} Falling	●	60	110	150	mV
$V_{TMR(INT)}$	Timer Internal Mode Voltage	V_{TMR} Falling	●	0.14	0.21	0.27	V
$\Delta V_{TMR(INT)}$	Timer Internal Mode Hysteresis	V_{TMR} Rising	●	40	70	110	mV
t_{PROP}	ADJx Comparator Propagation Delay to $\overline{RST}$	ADJx Driven Beyond Reset Threshold (V_{RTX}) by 5mV	●	50	150	500	µs
t_{UV}	V_{CC} Undervoltage Detect to $\overline{RST}$	V_{CC} Less Than UVLO Threshold ($V_{CC(UVLO)}$) by 1%	●	50	150	500	µs
$V_{OL(\overline{RST})}$	$\overline{RST}$ Output Voltage Low	V_{CC} = 0.5V, I = 5µA V_{CC} = 1V, I = 100µA V_{CC} = 3V, I = 2500µA	● ● ●		0.01 0.01 0.10	0.15 0.15 0.30	V V V
$I_{OH(\overline{RST})}$	$\overline{RST}$ Output Voltage High Leakage	$\overline{RST}$ = V_{CC}	●			±1	µA
Three-State Input SEL							
V_{IL}	Low Level Input Voltage		●			0.4	V
V_{IH}	High Level Input Voltage		●	1.4			V
V_Z	Pin Voltage when Left in Open State	I_{SEL} = 0µA			0.9		V
$I_{SEL(Z)}$	Allowable Leakage in Open State		●	±5 ±10			µA µA
I_{SEL}	SEL Input Current	SEL = V_{CC} or SEL = GND	●			±25	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

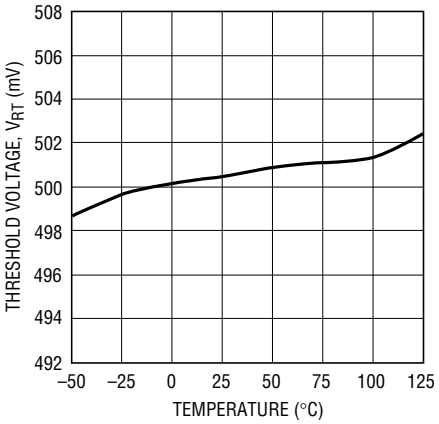
Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: V_{CC} maximum pin voltage is limited by input current. Since the V_{CC} pin has an internal 6.5V shunt regulator, a low impedance supply which exceeds 6V may exceed the rated terminal current. Operation from higher voltage supplies requires a series dropping resistor. See Applications Information.

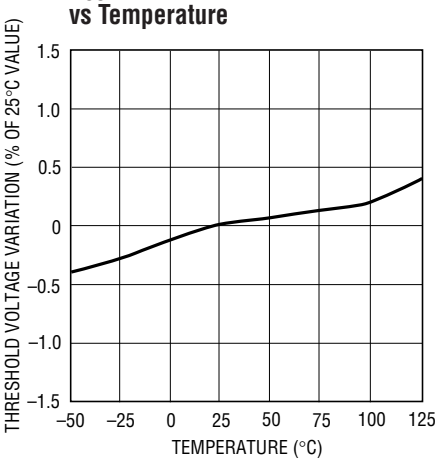
Note 4: Threshold voltages have no hysteresis unless the part is in comparator mode. Hysteresis is one-sided, affecting only invalid-to-valid transitions. See Applications Information.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

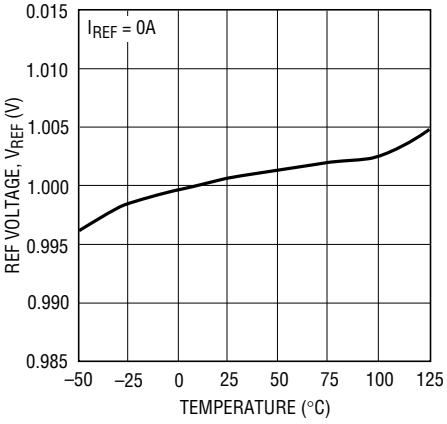
ADJ Threshold Voltage vs Temperature



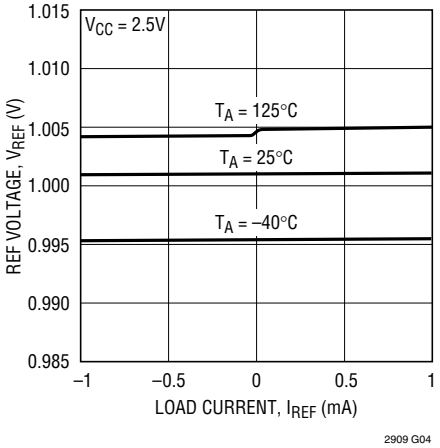
V_{CC} UVLO Threshold Variation vs Temperature



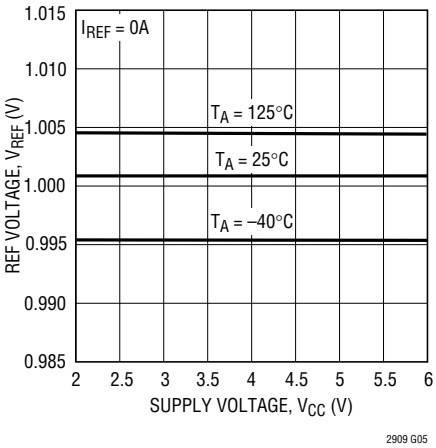
REF Output Voltage vs Temperature



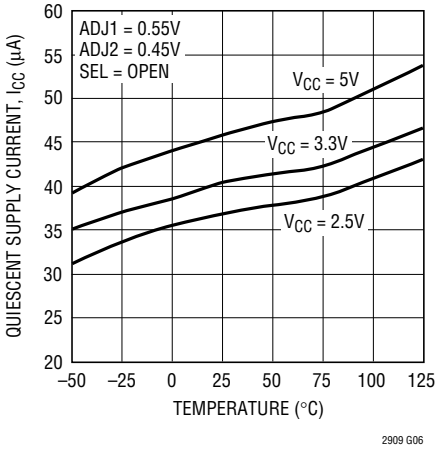
REF Output Load Regulation



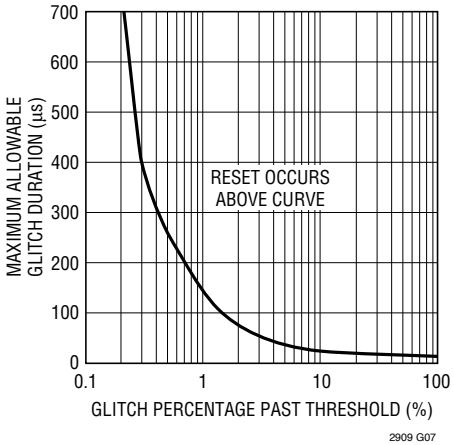
REF Output Line Regulation



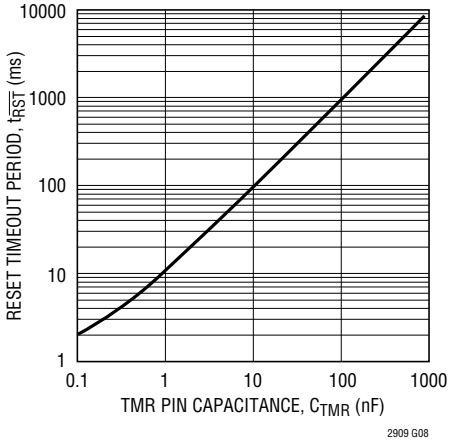
Quiescent Supply Current vs Temperature



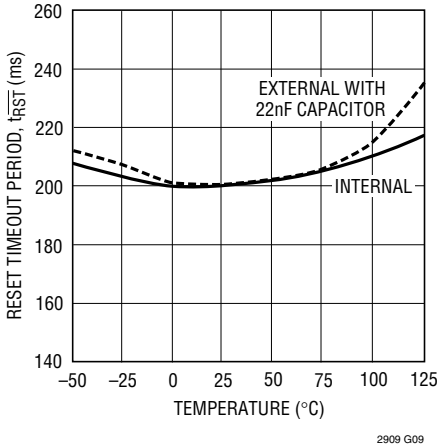
Allowable Glitch Duration vs Magnitude



External Timeout Period vs Capacitance

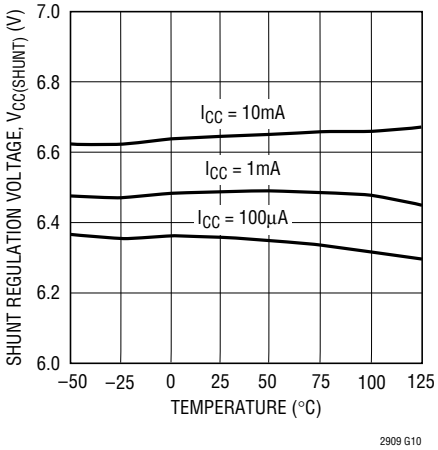


Reset Timeout Period vs Temperature

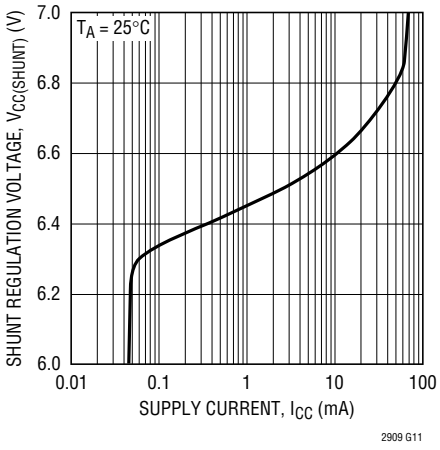


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted

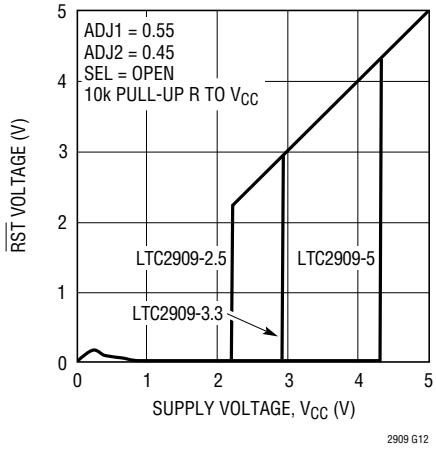
Shunt Regulation Voltage vs Temperature



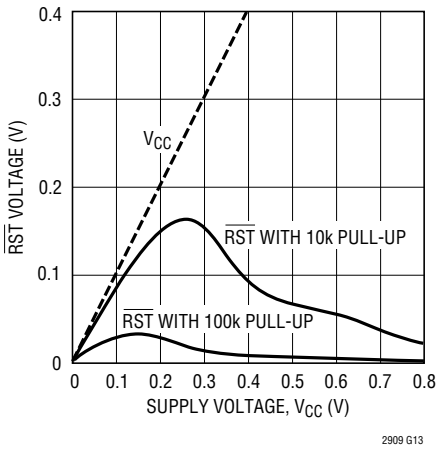
Shunt Regulation Voltage vs Supply Current



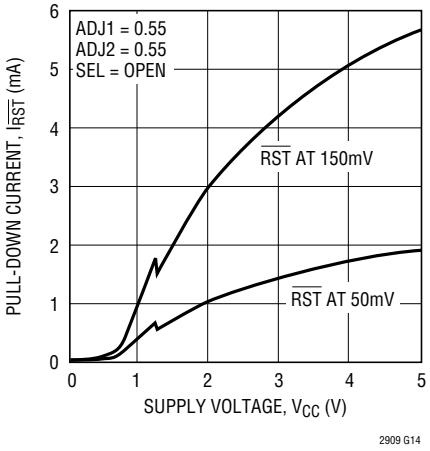
$\overline{RST}$ Output Voltage vs V_{CC}



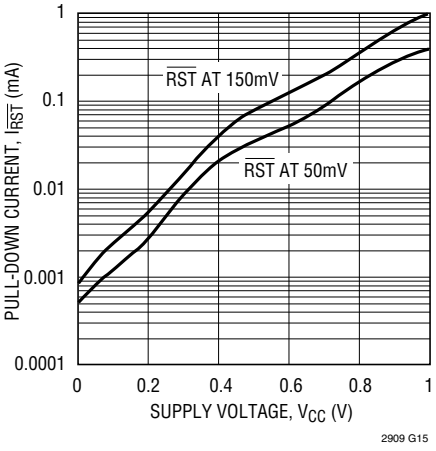
$\overline{RST}$ Output Voltage vs V_{CC}



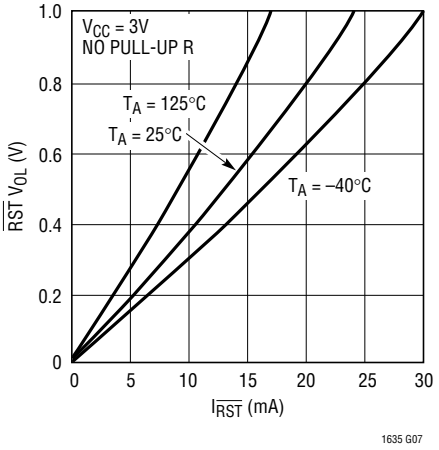
$\overline{RST}$ Pull-Down Current vs V_{CC}



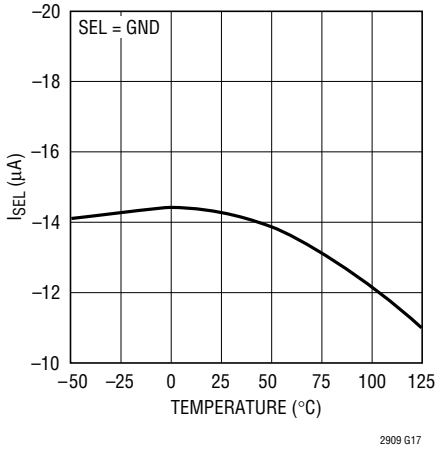
$\overline{RST}$ Pull-Down Current vs V_{CC}



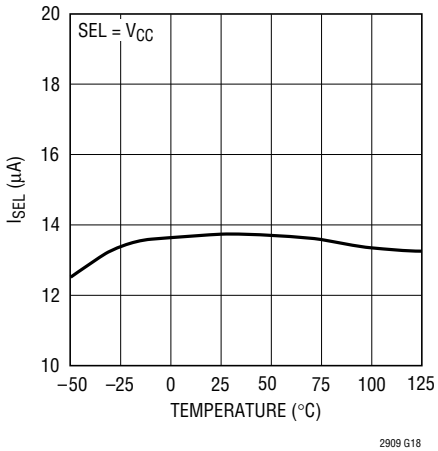
$\overline{RST}$ V_{OL} vs $I_{\overline{RST}}$



I_{SEL} vs Temperature



I_{SEL} vs Temperature



PIN FUNCTIONS (TSOT-23/DFN Package)

ADJ1 (Pin 1/Pin 8): Adjustable Voltage Input 1. Input to voltage monitor comparator 1 (0.5V nominal threshold). The polarity of the input is selected by the state of the SEL pin (refer to Table 1). Tie to REF if unused (with SEL = V_{CC} or Open).

ADJ2 (Pin 2/Pin 7): Adjustable Voltage Input 2. Input to voltage monitor comparator 2 (0.5V nominal threshold). The polarity of the input is selected by the state of the SEL pin (refer to Table 1). Tie to GND if unused (with SEL = GND or Open).

REF (Pin 3/Pin 6): Buffered Reference Output. 1V nominal reference used for the offset of negative-monitoring applications. The buffered reference can source and sink 1mA. The reference can drive a capacitive load of up to 1000pF. Larger capacitance may degrade transient performance. This pin does not require a bypass capacitor, nor is one recommended. Leave open if unused.

GND (Pin 4/Pin 5): Device Ground.

$\overline{RST}$ (Pin 5/Pin 4): Open-Drain Inverted Reset Logic Output. Asserts low when any positive polarity input voltage is below threshold or any negative polarity input voltage is above threshold or V_{CC} is below UVLO threshold. Held low for a timeout after all voltage inputs are valid. Requires an external pull-up resistor and may be pulled above V_{CC}.

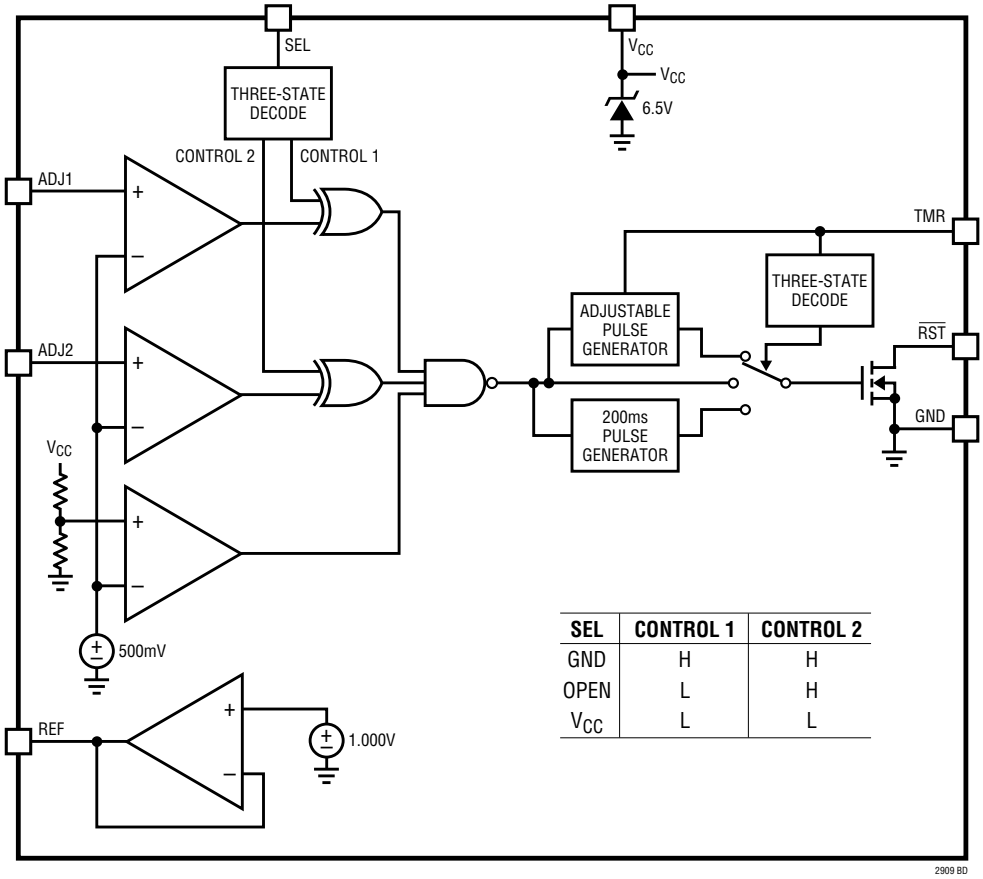
V_{CC} (Pin 6/Pin 3): Power Supply. Bypass this pin to ground with a 0.1µF (or greater) capacitor. Operates as a direct supply input for voltages up to 6V. Operates as a shunt regulator for supply voltages greater than 6V and should have a resistor between this pin and the supply to limit V_{CC} input current to no greater than 10mA. When used without a current-limiting resistor, pin voltage must not exceed 6V. UVLO options allow V_{CC} to be used as an accurate third fixed 10% UV supply monitor.

TMR (Pin 7/Pin 2): Reset Timeout Control. Attach an external capacitor (C_{TMR}) to GND to set a reset timeout of 9ms/nF. A low leakage ceramic capacitor is recommended for timer accuracy. Capacitors larger than 1µF (9 second timeout) are not recommended. See Applications Information for further details. Leaving this pin open generates a minimum timeout of approximately 400µs. A 2.2nF capacitor will generate a 20ms timeout. Tying this pin to ground will enable the internal 200ms timeout. Tying this pin to V_{CC} will disable the reset timer and put the part in comparator mode. Signals from the comparator outputs will then go directly to $\overline{RST}$.

SEL (Pin 8/Pin 1): Input Polarity Select Three-State Input. Connect to V_{CC}, GND or leave unconnected in open state to select one of three possible input polarity combinations (refer to Table 1).

Exposed Pad (Pin 9, DFN Only): The Exposed Pad may be left unconnected. For better thermal contact, tie to a PCB trace. This trace must be grounded or unconnected.

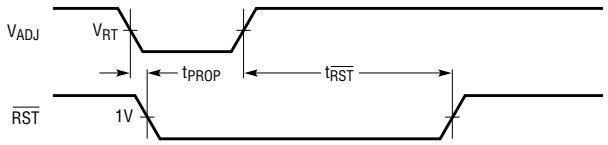
BLOCK DIAGRAM



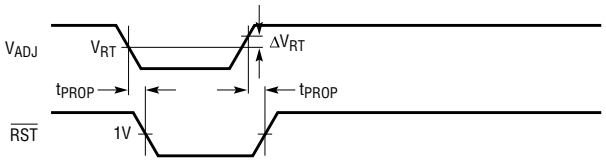
SEL	CONTROL 1	CONTROL 2
GND	H	H
OPEN	L	H
V_{CC}	L	L

TIMING DIAGRAMS

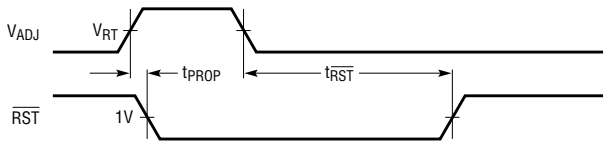
Normal Positive Polarity Input Timing



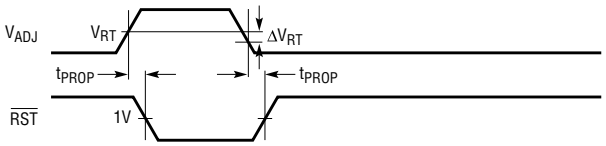
Comparator Mode Positive Polarity Input Timing



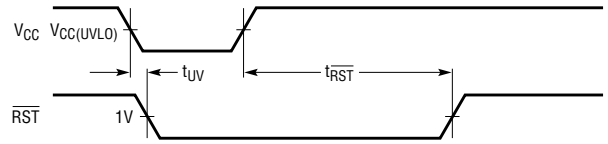
Normal Negative Polarity Input Timing



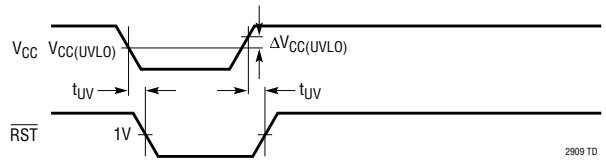
Comparator Mode Negative Polarity Input Timing



Normal UVLO Timing



Comparator Mode UVLO Timing



APPLICATIONS INFORMATION

The LTC2909 is a low power, high accuracy dual/triple supply monitor with two adjustable inputs and an accurate UVLO. Reset timeout may be selected with an external capacitor, set to an internally generated 200ms, or disabled entirely.

The three-state polarity select pin (SEL) chooses one of three possible polarity combinations for the adjustable input thresholds, as described in Table 1. Both input voltages (V_{ADJ1} and V_{ADJ2}) must be valid (above threshold if configured for positive polarity, below threshold if configured for negative polarity), and V_{CC} above the UVLO threshold for the reset timeout before $\overline{RST}$ is released. The LTC2909 asserts the reset output during power-up, power-down and brownout conditions on any of the voltage inputs.

Power-Up

The LTC2909 uses proprietary low voltage drive circuitry for the $\overline{RST}$ pin which holds $\overline{RST}$ low with as little as 200mV of V_{CC}. This helps prevent an unknown voltage on the $\overline{RST}$ line during power-up.

In applications where the low voltage pull-down capability is important, the supply to which the external pull-up resistor connects should be the same supply which powers the part. Using the same supply for both ensures that $\overline{RST}$ never floats above 200mV during power-up, as the pull-down ability of the pin will then increase as the required pull-down current to maintain a logic low increases.

Once V_{CC} passes the UVLO threshold, polarity selection and timer initialization will occur. If the monitored supplies (ADJ1 and ADJ2) are valid, the appropriate timeout delay will begin, after which $\overline{RST}$ will be released. Otherwise, the part will wait until all supplies are valid (including V_{CC} above the UVLO threshold) before beginning the timeout.

Power-Down

On power-down, once V_{CC} drops below the UVLO threshold or either V_{ADJ} becomes invalid, $\overline{RST}$ asserts logic low. V_{CC} of at least 0.5V guarantees a logic low of 0.15V at $\overline{RST}$.

Shunt Regulator

The LTC2909 contains an internal 6.5V shunt regulator on the V_{CC} pin to allow operation from a high voltage supply. To operate the part from a supply higher than 6V, the V_{CC} pin must have a series resistor, R_{CC}, to the supply. This resistor should be sized according to the following equation:

$$\frac{V_{S(MAX)} - 6.2V}{10mA} \leq R_{CC} \leq \frac{V_{S(MIN)} - 6.8V}{200\mu A + I_{VREF}}$$

where $V_{S(MIN)}$ and $V_{S(MAX)}$ are the operating minimum and maximum of the supply, and I_{VREF} is the maximum current the user expects to draw from the reference output.

As an example, consider operation from an automobile battery which might dip as low as 10V or spike to 60V. Assume that the user will be drawing 100µA from the reference. We must then pick a resistance between 5.4k and 10.7k.

When the V_{CC} pin is connected to a low impedance supply, it is important that the supply voltage never exceed 6V, or the shunt regulator may begin to draw large currents. Some supplies may have nominal value sufficiently close to the shunt regulation voltage to prevent sizing of the resistor according to the above equation. For such supplies, a 470Ω series resistor may be used.

Polarity Selection

The external connection of the SEL pin selects the polarities of the LTC2909 adjustable inputs. SEL may be connected to GND, connected to V_{CC} or left unconnected during normal operation. When left unconnected, the maximum leakage allowable from the pin to either GND or V_{CC} is 10µA. Table 1 shows the three possible selections of polarity based on SEL connection.

Table 1. Voltage Threshold Selection

ADJ1 INPUT	ADJ2 INPUT	SEL
Positive Polarity (+) UV or (–) OV	Positive Polarity (+) UV or (–) OV	V_{CC}
Positive Polarity (+) UV or (–) OV	Negative Polarity (–) UV or (+) OV	Open
Negative Polarity (–) UV or (+) OV	Negative Polarity (–) UV or (+) OV	Ground

Note: Open = open circuit or driven by a three-state buffer in high impedance state with leakage current less than 10µA.

If the user's application requires, the SEL pin may be driven using a three-state buffer which satisfies the V_{IL}, V_{IH} and leakage of the three-state pin.

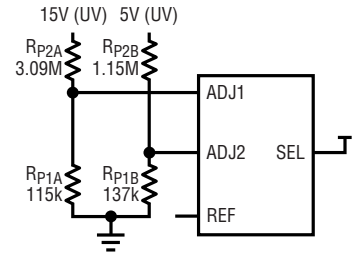
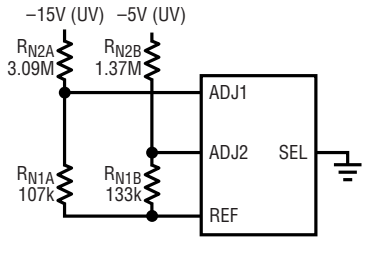
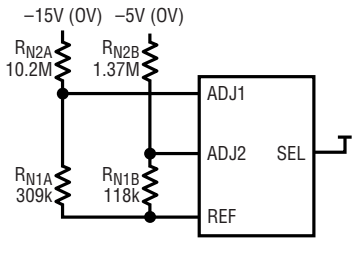
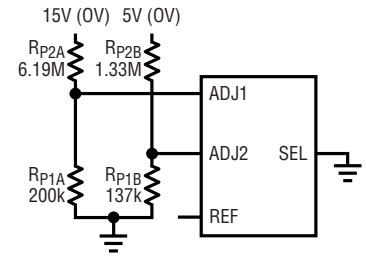
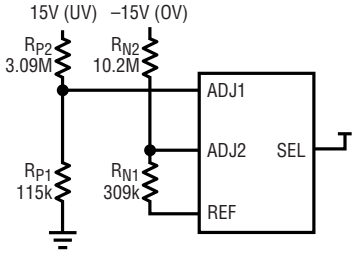
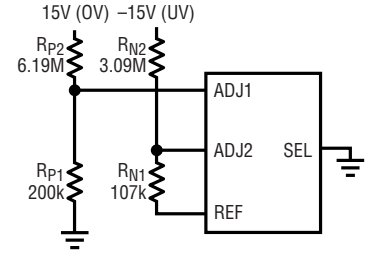
APPLICATIONS INFORMATION

If the state of the SEL pin configures a given input as "negative polarity," the voltage at the ADJx pin must be below the trip point (0.5V nominal), or the $\overline{RST}$ output will be pulled low. Conversely, if a given input is configured as "positive polarity," the pin voltage must be above the trip point or $\overline{RST}$ will assert low.

Thus, a "negative polarity" input may be used to determine whether a monitored negative voltage is smaller in absolute value than it should be (–UV), or a monitored positive voltage is larger than it should be (+OV). The opposite is true for a "positive polarity" input (–OV or +UV). These usages are also shown in Table 1. For purposes of this data sheet, a negative voltage is considered "undervoltage" if it is closer to ground than it should be (e.g., –4.3V for a –5V supply).

Proper configuration of the SEL pin and setting of the trip-points via external resistors allows for any two fault conditions to be detected. For example, the LTC2909 may monitor two supplies (positive, negative or one of each) for UV or for OV (or one UV and one OV). It may also monitor a single supply (positive or negative) for both UV and OV. Tables 2a and 2b show example configurations for monitoring possible combinations of fault condition and supply polarity.

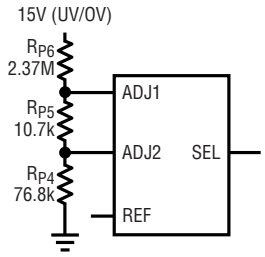
Table 2a. Possible Combinations of Supply Monitoring. For Example Purposes, All Supplies are Monitored at 5% Tolerance and Connections are Shown Only for ADJ1, ADJ2, REF, SEL

SEL = V_{CC}	SEL = GND
 **2 Positive UV**	 **2 Negative UV**
 **2 Negative OV**	 **2 Positive OV**
 **1 Positive UV, 1 Negative OV**	 **1 Positive OV, 1 Negative UV**

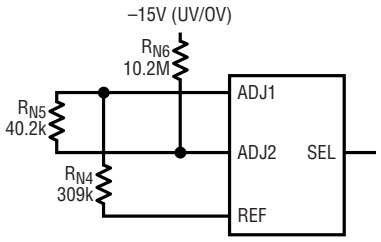
APPLICATIONS INFORMATION

Table 2b. Possible Combinations of Supply Monitoring. For Example Purposes, All Supplies are Monitored at 5% Tolerance and Connections are Shown Only for ADJ1, ADJ2, REF, SEL

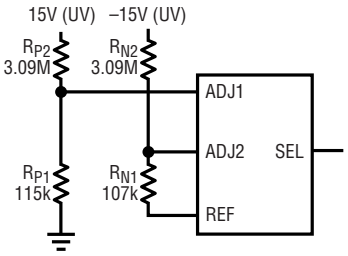
SEL OPEN



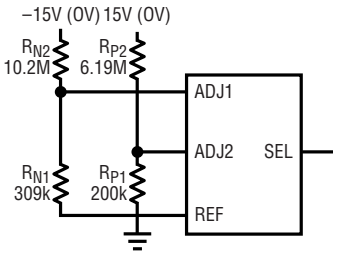
1 Positive UV and OV



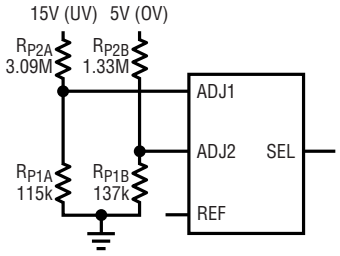
1 Negative UV and OV



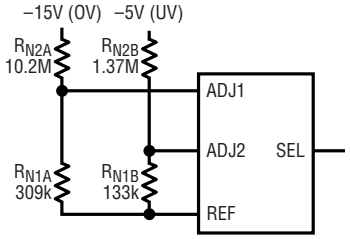
1 Positive UV, 1 Negative UV



1 Negative OV, 1 Positive OV



1 Positive UV, 1 Positive OV



1 Negative UV, 1 Negative OV

Adjust Input Trip Point

The trip threshold for the supplies monitored by the adjustable inputs is set with an external resistor divider, allowing the user complete control over the trip point. Selection of this trip voltage is crucial to the reliability of the system.

Any power supply has some tolerance band within which it is expected to operate (e.g., 5V ±10%). It is generally undesirable that a supervisor issue a reset when the power supply is inside this tolerance band. Such a "nuisance" reset reduces reliability by preventing the system from functioning under normal conditions.

To prevent nuisance resets, the supervisor threshold must be guaranteed to lie outside the power supply tolerance band. To ensure that the threshold lies outside the power supply tolerance range, the nominal threshold must lie outside that range by the monitor's accuracy specification.

All three of the LTC2909 inputs (ADJ1, ADJ2, V_{CC} UVLO) have the same relative threshold accuracy of ±1.5% of the programmed nominal input voltage (over the full operating temperature range). Therefore, using the LTC2909, the typical 10% UV threshold is at 11.5% below the nominal input voltage level. For a 5V input, the threshold is nominally 4.425V. With ±1.5% accuracy, the trip threshold range is 4.425V ±75mV over temperature (i.e., 10% to 13% below 5V). The monitored system must thus operate reliably down to 4.35V or 13% below 5V over temperature.

APPLICATIONS INFORMATION

The above discussion is concerned only with the DC value of the monitored supply. Real supplies also have relatively high frequency variation from sources such as load transients, noise and pickup. These variations should not be considered by the monitor in determining whether a supply voltage is valid or not. The variations may cause spurious outputs at $\overline{RST}$, particularly if the supply voltage is near its trip threshold.

A common solution to the problem of spurious reset is to introduce hysteresis around the nominal threshold. However, this hysteresis degrades the effective accuracy of the monitor and increases the range over which the system must operate. The LTC2909 therefore does not have hysteresis, except in comparator mode (see Setting the Reset Timeout). If hysteresis is desired in other modes, it may be added externally. See Typical Applications for an example.

The LTC2909 uses two techniques to combat spurious reset without sacrificing threshold accuracy. First, the timeout period helps prevent high frequency variation whose frequency is above 1/ t_{RST} from appearing at the $\overline{RST}$ output.

When either ADJ1 or ADJ2 becomes invalid, the $\overline{RST}$ pin asserts low. When the supply recovers past the threshold, the reset timer starts (assuming it is not disabled) and $\overline{RST}$ does not go high until it finishes. If the supply becomes invalid any time during the timeout period, the timer resets and starts fresh when the supply next becomes valid.

While the reset timeout is useful at preventing toggling of the reset output in most cases, it is not effective at preventing nuisance resets due to short glitches (from load transients or other effects) on a valid supply. To reduce sensitivity to these short glitches, the comparator outputs go through a lowpass filter before triggering the output logic. Any transient at the input of a comparator needs to be of sufficient magnitude and duration to pass the filter before it can change the monitor state.

The combination of the reset timeout and comparator filtering prevents spurious changes in the output state without sacrificing threshold accuracy. If further supply glitch immunity is needed, the user may place an external capacitor from the ADJ input to ground. The resultant RC lowpass filter with the resistor divider will further reject high frequency components of the supply, at the cost of slowing the monitor's response to fault conditions.

Selecting External Resistors

In a typical positive supply monitoring application, the ADJx pin connects to a tap point on an external resistive divider between a positive voltage being monitored and ground, as shown in Figure 1.

When monitoring a negative supply, the ADJx pin connects to a tap point on a resistive divider between the negative voltage being monitored and the buffered reference (REF), as shown in Figure 2.

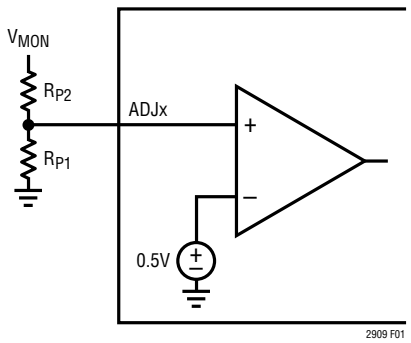


Figure 1. Setting Positive Supply Trip Point

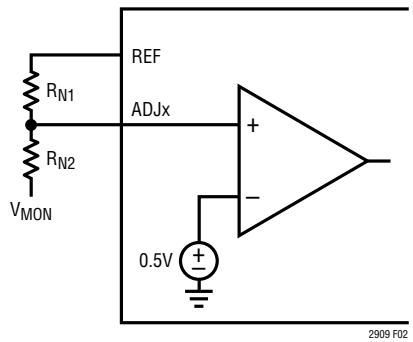


Figure 2. Setting Negative Supply Trip Point

Normally the user will select a desired trip voltage based on their supply and acceptable tolerances, and a value of R_{N1} or R_{P1} based on current draw. Current used by the resistor divider will be approximately:

$$I = \frac{0.5V}{R_{X1}}$$

Recommended range is 1k to 1M.

APPLICATIONS INFORMATION

For a positive-monitoring application, R_{P2} is then chosen by:

$$R_{P2} = R_{P1}(2V_{TRIP} - 1)$$

For a negative-monitoring application:

$$R_{N2} = R_{N1}(1 - 2V_{TRIP})$$

Note that the value V_{TRIP} should be negative for a negative application.

The LTC2909 can also be used to monitor a single supply for both UV and OV. This may be accomplished with three resistors, instead of the four required for two independent supplies. Configurations are shown in Figures 3 and 4. R_{P4} or R_{N4} may be chosen as is R_{P1} above.

For a given R_{P4}, monitoring a positive supply:

$$R_{P5} = R_{P4}\frac{V_{OV} - V_{UV}}{V_{UV}}$$

$$R_{P6} = R_{P4}\left(2V_{UV} - 1\right)\frac{V_{OV}}{V_{UV}}$$

For monitoring a negative supply with a given R_{N4}:

$$R_{N5} = R_{N4}\frac{V_{UV} - V_{OV}}{1 - V_{UV}}$$

$$R_{N6} = R_{N4}\left(1 - 2V_{UV}\right)\frac{1 - V_{OV}}{1 - V_{UV}}$$

For example, consider monitoring a –5V supply at ±10%. For this supply application: $V_{OV} = -5.575V$ and $V_{UV} = -4.425V$.

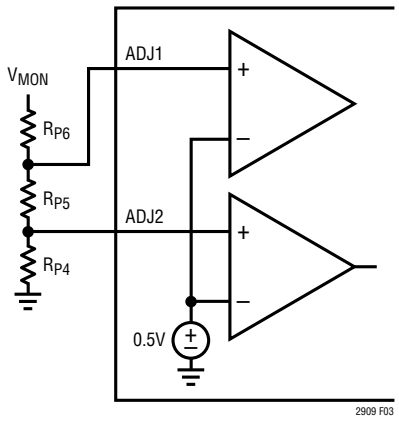


Figure 3. Setting UV and OV Trip Point for a Positive Supply

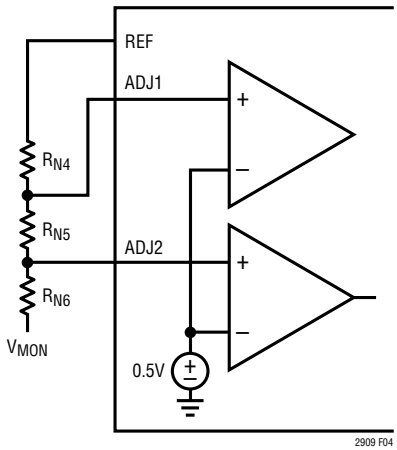


Figure 4. Setting UV and OV Trip Point for a Negative Supply

Suppose we wish to consume about 5µA in the divider, so $R_{N4} = 100k$. We then find $R_{N5} = 21.0k$, $R_{N6} = 1.18M$ (nearest 1% standard values have been chosen). Suggested values of resistors for 5% monitoring are shown in Table 3.

V_{CC} Monitoring/UVLO

The LTC2909 contains an accurate third 10% undervoltage monitor on the V_{CC} pin. This monitor is fixed at a nominal 11.5% below the V_{CC} specified in the part number. The standard part (LTC2909-2.5) is configured to monitor a 2.5V supply (UVLO threshold of 2.213V), but versions to monitor 3.3V and 5.0V (UVLO of 2.921V and 4.425V, respectively) are available.

For applications that do not need V_{CC} monitoring, the 2.5V version should be used, and the UVLO will simply guarantee that the V_{CC} is above the minimum required for proper threshold and timer accuracy before the timeout begins.

Setting the Reset Timeout

The reset timeout of the LTC2909 may be configured in one of three ways: internal 200ms, programmed by external capacitor and no timeout (comparator mode). The mode of the timer is determined by the connection of the TMR pin.

In externally-controlled mode, the TMR pin is connected by a capacitor to ground. The value of that capacitor allows for selection of a timeout ranging from about 400µs to 10 seconds. See the following section for details.

APPLICATIONS INFORMATION

Table 3. Suggested Resistor Values for 5% Monitoring

NOMINAL VOLTAGE	5% UV		5% OV		5% UV and OV		
	R_{X1}	R_{X2}	R_{X1}	R_{X2}	R_{X4}	R_{X5}	R_{X6}
24	232k	10.2M	102k	5.11M	82.5k	11.5k	4.12M
15	115k	3.09M	200k	6.19M	76.8k	10.7k	2.37M
12	49.9k	1.07M	102k	2.49M	76.8k	10.7k	1.87M
9	115k	1.82M	78.7k	1.43M	162k	22.6k	2.94M
5	137k	1.15M	137k	1.33M	76.8k	10.7k	732k
3.3	221k	1.15M	340k	2.05M	76.8k	10.7k	453k
2.5	115k	422k	51.1k	221k	137k	19.1k	576k
1.8	63.4k	150k	115k	324k	82.5k	11.5k	221k
1.5	59.0k	107k	137k	301k	76.8k	10.7k	158k
1.2	127k	158k	102k	158k	187k	26.1k	267k
1	200k	174k	100k	113k	107k	15.0k	105k
–5	133k	1.37M	118k	1.37M	174k	20.0k	2.00M
–9	97.6k	1.74M	115k	2.32M	182k	22.6k	3.65M
–12	107k	2.49M	40.2k	1.07M	40.2k	5.11k	1.07M
–15	107k	3.09M	309k	10.2M	309k	40.2k	10.2M

Trip points are nominal voltage ±6.5%.

If the user wishes to avoid having an external capacitor, the TMR pin should be tied to ground, switching the part to an internal 200ms timer.

If the user requires a shorter timeout than 400µs, or wishes to perform application-specific processing of the reset output, the part may be put in comparator mode by tying the TMR pin to V_{CC}. In comparator mode, the timer is bypassed and comparator outputs go straight to the reset output.

The current required to hold TMR at ground or V_{CC} is about 2µA. To force the pin from the floating state to ground or V_{CC} may require as much as 100µA during the transition.

When the part is in comparator mode, one of the two means of preventing false reset has been removed, so a small amount of one-sided hysteresis is added to the inputs to prevent oscillation as the monitored voltage passes through the threshold. This hysteresis is such that the valid-to-invalid transition threshold is unchanged, but the invalid-to-valid threshold is moved by about 0.7%. Thus, when the ADJ input polarity is positive, the threshold voltage is 500mV nominal when the input is above 500mV. As soon as the input drops below 500mV, the threshold moves up to 503.5mV nominal. Conversely, when configured as a negative-polarity input, the threshold is 500mV when the input is below 500mV, and switches to 496.5mV when the input goes above 500mV.

The comparator mode feature should be enabled by directly shorting the TMR pin to the V_{CC} pin. Connecting the pin to any other voltage may have unpredictable results.

Selecting the Reset Timing Capacitor

Connecting a capacitor, C_{TMR}, between the TMR pin and ground sets the reset timeout, t_{RST}. The following formula approximates the value of capacitor needed for a particular timeout:

$$C_{TMR} = t_{\overline{RST}} \bullet 110\ [pF/ms]$$

Leaving the TMR pin open with no external capacitor generates a reset timeout of approximately 400µs.

Maximum length of the reset timeout is limited by the ability of the part to charge a large capacitor on start-up. Initially, with a large (discharged) capacitor on the TMR pin, the part will assume it is in internal timer mode (since the pin voltage will be at ground). If the 2µA flowing out of the TMR pin does not charge the capacitor to the ground-sense threshold within the first 200ms after supplies become good, the internal timer cycle will complete and $\overline{RST}$ will go high too soon.

APPLICATIONS INFORMATION

This imposes a practical limit of 1µF (9 second timeout) if the length of timeout during power-up needs to be longer than 200ms. If the power-up timeout is not important, larger capacitors may be used, subject to the limitation that the capacitor leakage current must not exceed 500nA, or the function of the timer will be impaired.

$\overline{RST}$ Output Characteristics

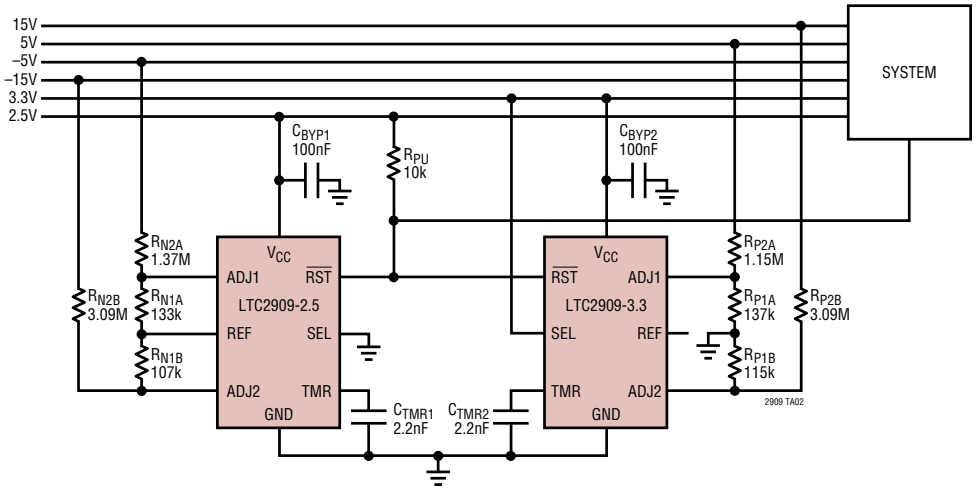
The DC characteristics of the $\overline{RST}$ pull-down strength are shown in the Typical Performance Characteristics section. $\overline{RST}$ is an open-drain pin and thus requires an external pull-up resistor to the logic supply. $\overline{RST}$ may be pulled above V_{CC}, providing the voltage limits of the pin are observed.

The open-drain nature of the $\overline{RST}$ pin allows for wired-OR connection of several LTC2909s to monitor more than two supplies (see Typical Applications). Other logic with open-drain outputs may also connect to the $\overline{RST}$ line, allowing other logic-determined conditions to issue a reset.

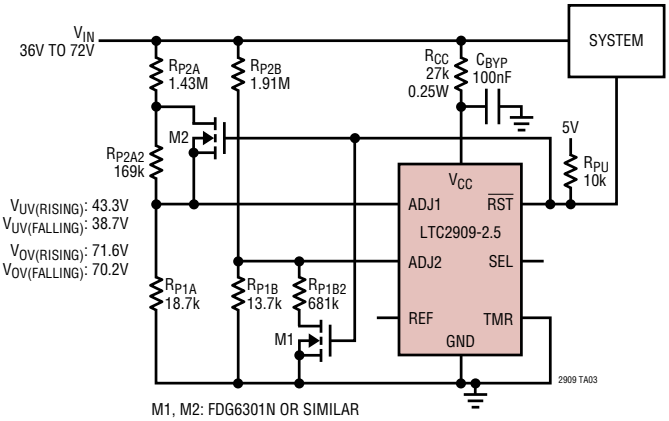
As noted in the discussion of power up and power down, the circuits that drive $\overline{RST}$ are powered by V_{CC}. During a fault condition, V_{CC} of at least 0.5V guarantees a V_{OL} of 0.15V at $\overline{RST}$.

TYPICAL APPLICATIONS

Six Supply Undervoltage Monitor with 2.5V Reset Output and 20ms Timeout



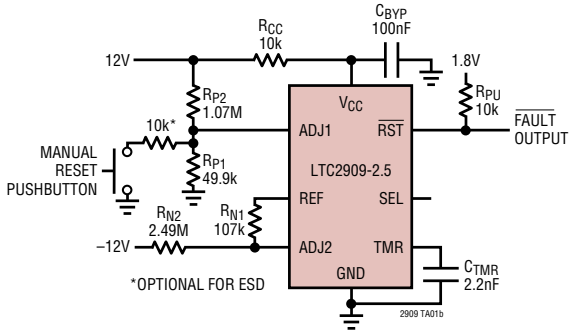
48V Telecom UV/OV Monitor with Hysteresis



M1, M2: FDG6301N OR SIMILAR

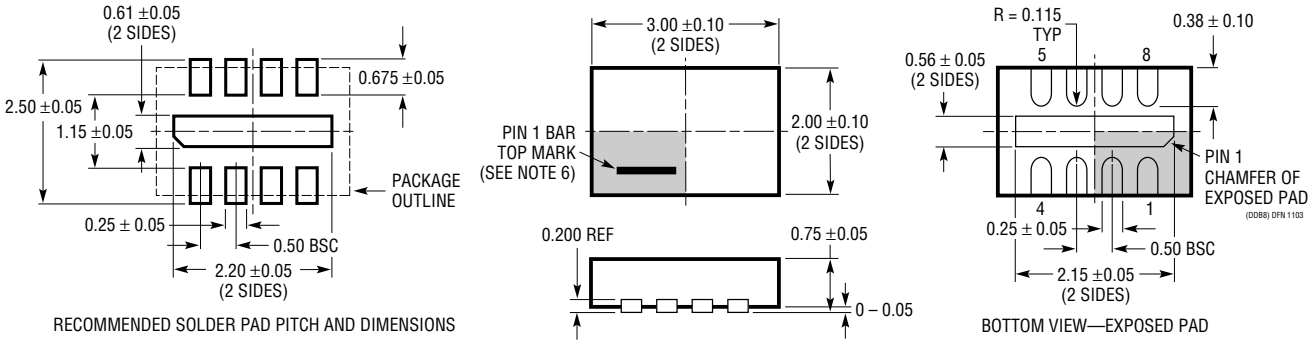
IF LOADING OF $\overline{RST}$ WILL EXCEED 1nF, A 1nF BYPASS CAPACITOR ON M1's DRAIN IS RECOMMENDED

±12V UV Monitor Powered from 12V, 20ms Timeout (1.8V Logic Out)



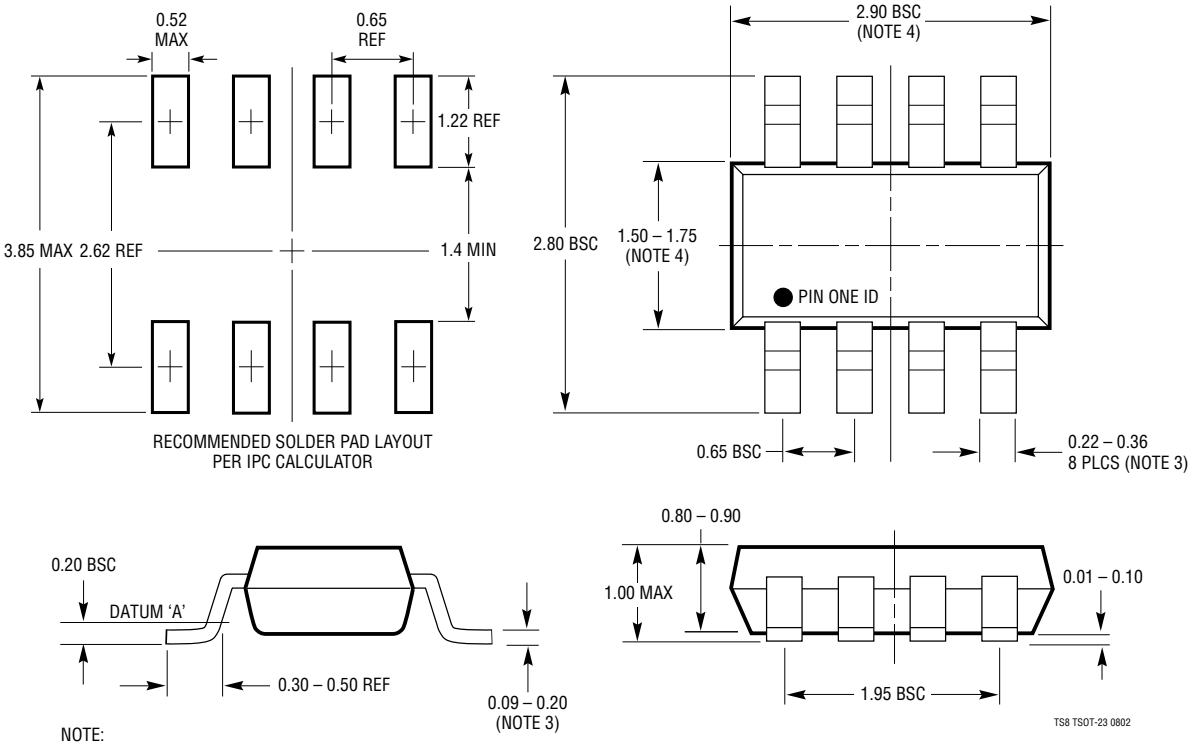
PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702)



NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

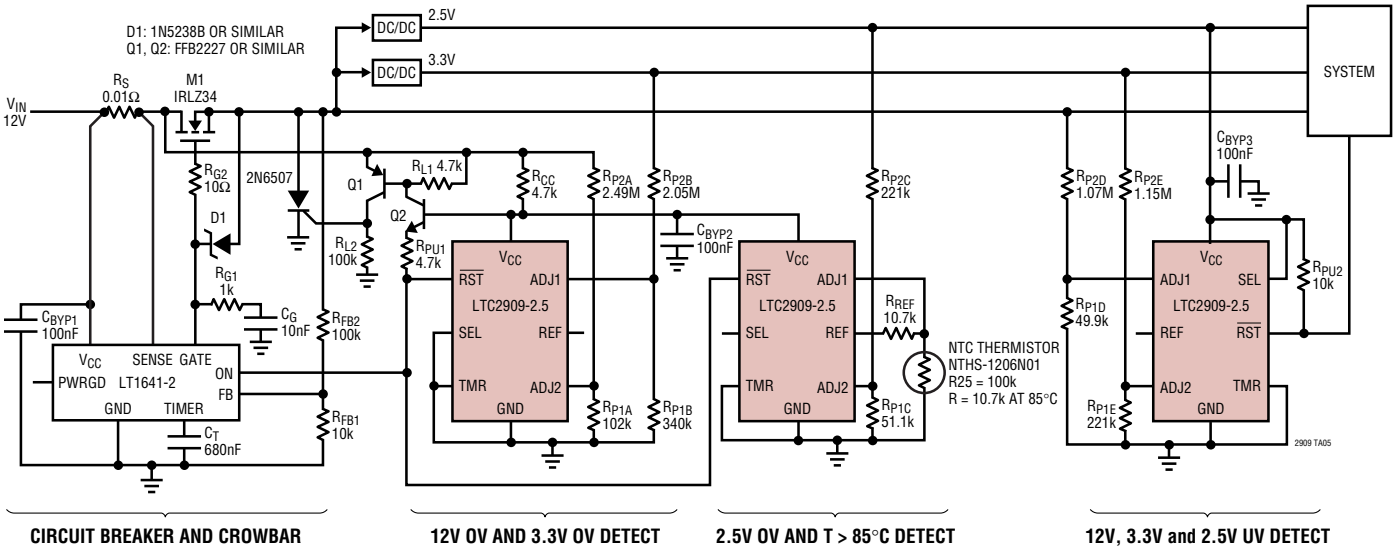
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

TYPICAL APPLICATION

Automotive Supply System with Overvoltage, Overcurrent and Overtemperature Protection and Undervoltage Reset



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326/LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1540	Nanopower Comparator with Reference	Adjustable Hysteresis
LTC1726-2.5/LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable Reset and Watchdog Time-Outs
LTC1727/LTC1728	Micropower Triple Supply Monitor with Open-Drain Reset	Individual Monitor Outputs in MSOP/5-Lead SOT-23
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2900	Programmable Quad Supply Monitor	Adjustable Reset, 10-Lead MSOP and 3mm × 3mm 10-Lead DFN Package
LTC2901	Programmable Quad Supply Monitor	Adjustable Reset and Watchdog Timer, 16-Lead SSOP Package
LTC2902	Programmable Quad Supply Monitor	Adjustable Reset and Tolerance, 16-Lead SSOP Package, Margining Functions
LTC2903	Precision Quad Supply Monitor	6-Lead SOT-23 Package, Ultralow Voltage Reset
LTC2904/LTC2905	3-State Programmable Precision Dual Supply Monitor	Adjustable Tolerance and Reset Timer, 8-Lead SOT-23 Package
LTC2906/LTC2907	Precision Dual Supply Monitor 1-Selectable and 1 Adjustable	Separate V_{CC} Pin, RST/$\overline{RST}$ Outputs/Adjustable Reset Timer
LTC2908	Precision Six Supply Monitor (Four Fixed and 2 Adjustable)	8-Lead SOT-23 and DDB Packages
LT6700	Micropower, Low Voltage, Dual Comparator with 400mV Reference	6-Lead SOT-23 Package

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