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Precision Triple Supply Monitor with Power-Fail Comparator

FEATURES

- **Ultralow Voltage Reset: V_{CC} = 0.5V Guaranteed**
- **Monitors Three Inputs Simultaneously:**
  3.3V, 5V, ADJ (LTC2911-1)
  3.3V, 2.5V, ADJ (LTC2911-2)
  3.3V, 1.8V, ADJ (LTC2911-3)
  3.3V, 1.2V, ADJ (LTC2911-4)
  3.3V, ADJ, ADJ (LTC2911-5)
- **±1.5% Threshold Accuracy**
- **Power-Fail Monitor**
- **$\overline{RST}$ State Can Be Held for Margining**
- Low Supply Current: 30µA Typical
- Input Glitch Immunity
- Adjustable Reset Timeout Period
- Selectable Internal Timeout Saves Components
- Space Saving 8-Lead TSOT-23 and 3mm × 2mm DFN Packages

APPLICATIONS

- Network Servers
- Desktop and Notebook Computers
- Automotive and Industrial Electronics

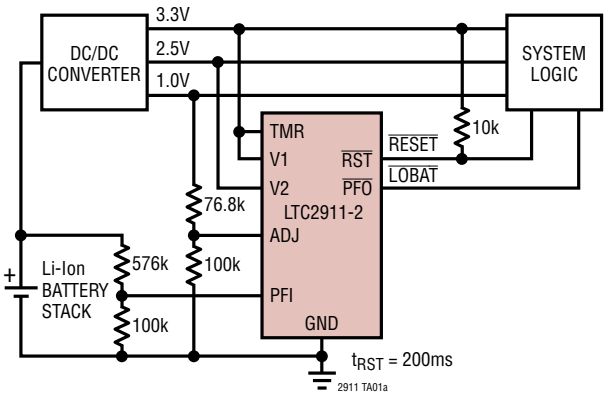
DESCRIPTION

The LTC®2911 is a low power, high accuracy triple supply monitor with a power-fail comparator. Reset timeout may be selected with an external capacitor or set to an internally generated 200ms.

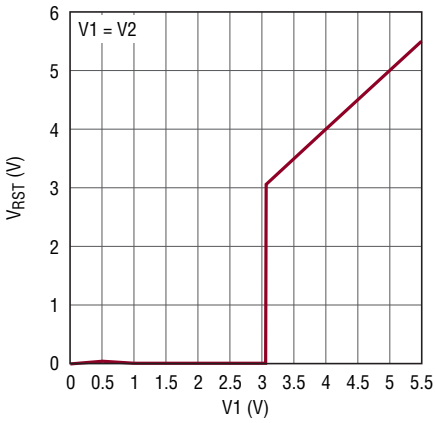
The V1 pin monitors a 3.3V supply. The V2 pin monitors a 5V, 2.5V, 1.8V, 1.2V or adjustable supply. A third adjustable input has a nominal 0.5V threshold allowing a resistive divider to configure its threshold. All three comparators feature a tight 1.5% threshold accuracy over the entire operating temperature range while a glitch filter ensures reliable reset operation.

A spare comparator can be configured to provide early warning of a low voltage condition. It causes the $\overline{PFO}$ output to pull low when the voltage of the PFI input falls below 0.5V, allowing the power-fail threshold to be configured with a resistive divider. A latch feature on the TMR pin allows the $\overline{RST}$ output to be latched to prevent system resets, simplifying margin testing.

TYPICAL APPLICATION



$\overline{RST}$ Output Voltage With 10k Pull-Up to V1



ABSOLUTE MAXIMUM RATINGS (Notes 1, 2, 3)

Supply Voltages
- V1, V2 ..... –0.3V to 6.5V

Input Voltages
- ADJ ..... –0.3V to 6.5V
- PFI ..... –0.3V to 2V
- TMR ..... –0.3V to (V1 + 0.3V)

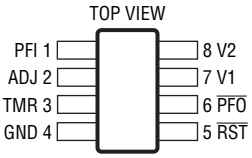
Output Voltages
- $\overline{RST}$, $\overline{PFO}$ ..... –0.3V to 6.5V

Operating Temperature Range
- LTC2911C ..... 0°C to 70°C
- LTC2911I ..... –40°C to 85°C
- LTC2911H ..... –40°C to 125°C

Storage Temperature Range ..... –65°C to 150°C

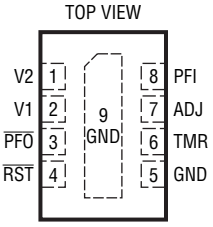
Lead Temperature (Soldering, 10 sec)
- TSOT-23 ..... 300°C

PIN CONFIGURATION



TS8 PACKAGE
8-LEAD PLASTIC TSOT-23

T_{JMAX} = 150°C, θ_{JA} = 195°C/W



DDB PACKAGE
8-LEAD (3mm × 2mm) PLASTIC DFN

T_{JMAX} = 150°C, θ_{JA} = 76°C/W
EXPOSED PAD (PIN 9) IS GND, PCB CONNECTION OPTIONAL

ORDER INFORMATION

LTC2911 C DDB –1 #TRM PBF

LEAD FREE DESIGNATOR
PBF = Lead Free Finish Parts
None = Lead Based Finish Parts

TAPE AND REEL
#TR = Tape and Reel
#TRM = 500-Piece Tape and Reel

PRODUCT SELECTION
–1, –2, –3, –4, –5
See Product Selection Guide for Details

PACKAGE TYPE
DDB = 8-Lead (3mm × 2mm) Plastic DFN
TS8 = 8-Lead Plastic TSOT-23

TEMPERATURE GRADE
C = Commercial Temperature Range (0°C to 70°C)
I = Industrial Temperature Range (–40°C to 85°C)
H = Automotive Temperature Range (–40°C to 125°C)

PRODUCT PART NUMBER

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

PRODUCT SELECTION GUIDE

PART NUMBER	PART MARKING	PACKAGE DESCRIPTION	V1	V2
LTC2911-1	LFHZ	8-Lead (3mm × 2mm) Plastic DFN	3.3V	5V
LTC2911-2	LFPG	8-Lead (3mm × 2mm) Plastic DFN	3.3V	2.5V
LTC2911-3	LFPJ	8-Lead (3mm × 2mm) Plastic DFN	3.3V	1.8V
LTC2911-4	LFPM	8-Lead (3mm × 2mm) Plastic DFN	3.3V	1.2V
LTC2911-5	LFPP	8-Lead (3mm × 2mm) Plastic DFN	3.3V	ADJ
LTC2911-1	LTFJB	8-Lead Plastic TSOT-23	3.3V	5V
LTC2911-2	LTFPH	8-Lead Plastic TSOT-23	3.3V	2.5V
LTC2911-3	LTFPK	8-Lead Plastic TSOT-23	3.3V	1.8V
LTC2911-4	LTFPN	8-Lead Plastic TSOT-23	3.3V	1.2V
LTC2911-5	LTFPQ	8-Lead Plastic TSOT-23	3.3V	ADJ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{ADJ} = 0.55V, V_{PFI} = 0.55V, V1 = 3.3V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{RT33}	3.3V, 5% Reset Threshold	V1 Input	●	3.036	3.086	3.135	V
V_{RT50}	5V, 5% Reset Threshold	V2 Input (LTC2911-1)	●	4.600	4.675	4.750	V
V_{RT25}	2.5V, 5% Reset Threshold	V2 Input (LTC2911-2)	●	2.300	2.338	2.375	V
V_{RT18}	1.8V, 5% Reset Threshold	V2 Input (LTC2911-3)	●	1.656	1.683	1.710	V
V_{RT12}	1.2V, 5% Reset Threshold	V2 Input (LTC2911-4)	●	1.104	1.122	1.140	V
V_{RTA}	ADJ Pin Threshold	ADJ Input and V2 Input of LTC2911-5	●	492.5	500	507.5	mV
V_{PFT}	PFI Pin Threshold	PFI Input Threshold (Falling)	●	492.5	500	507.5	mV
ΔV_{PFT}	PFI Hysteresis		●	10	15	19	mV
$V_{CC,OP}$	Minimum Operating Voltage to Guarantee $\overline{PFO}$ High (Note 3)	V_{PFI} = 0.55V	●			2.3	V
I_{V1}	V1 input Current (Note 4)	V1 = 3.3V, V1 > V2	●	10	30	80	µA
		V1 = 3.3V, V1 < V2	●	3	10	30	µA
I_{V2}	V2 Input Current (Note 4)	V2 = 5V (LTC2911-1)	●	10	35	80	µA
		V2 = 2.5V (LTC2911-2)	●	3	10	30	µA
		V2 = 1.8V (LTC2911-3)	●	2	10	30	µA
		V2 = 1.2V (LTC2911-4)	●	2	10	30	µA
		V2 = 0.55V (LTC2911-5)					
		C-Grade/I-Grade	●			±15	nA
		H-Grade	●			±40	nA
I_{ADJ}	ADJ Input Current	V_{ADJ} = 0.55V (C-Grade) (I-Grade)	●			±15	nA
		V_{ADJ} = 0.55V (H-Grade)	●			±40	nA
I_{PFI}	PFI Input Current	V_{PFI} = 0.55V (C-Grade) (I-Grade)	●			±15	nA
		V_{PFI} = 0.55V (H-Grade)	●			±40	nA
$I_{TMR(UP)}$	TMR Pull-Up Current	V_{TMR} = 1V	●	–1.5	–2.2	–2.9	µA
$I_{TMR(DOWN)}$	TMR Pull-Down Current	V_{TMR} = 1V	●	1.5	2.2	2.9	µA
I_{PU}	$\overline{RST}$, $\overline{PFO}$ Pull-Up Current	V_{PIN} = 0V	●	–20	–29	–40	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{ADJ} = 0.55V, V_{PFI} = 0.55V, V1 = 3.3V unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{P,PF}$	PFI Comparator Propagation Delay to $\overline{PFO}$	V_{PFI} Driven Beyond Threshold V_{PFT} by More Than 10%	●	8	30	80	µs
t_{UV}	V1, V2, ADJ Undervoltage Detect to $\overline{RST}$ Low	V_X Less Than Threshold V_{RTX} by More Than 10%	●	8	30	80	µs
V_{OH}	$\overline{RST}$, $\overline{PFO}$ Output Voltage High (Note 5)	I_{RST} = –1µA	●	V1 – 1		V1	V
V_{OL}	$\overline{RST}$, $\overline{PFO}$ Output Voltage Low (Note 6)	V_{CC} = 0.5V, I = 5µA V_{CC} = 1V, I = 100µA V_{CC} = 3V, I = 2.5mA	● ● ●		0.01 0.01 0.10	0.15 0.15 0.30	V V V
$t_{RST(EXT)}$	Reset Timeout Period, External	C_{TMR} = 2.2nF	●	15	20	27	ms
$t_{RST(INT)}$	Reset Timeout Period, Internal	V_{TMR} = V1	●	140	200	280	ms
$V_{TMR(INT)}$	Timer Internal Mode Threshold	V_{TMR} Rising	●	V1 – 0.40	V1 – 0.020	V1 – 0.10	V
$\Delta V_{TMR(INT)}$	Timer Internal Mode Hysteresis	V_{TMR} Falling	●	40	100	160	mV
$V_{TMR(LATCH)}$	Timer Latch Mode Threshold	V_{TMR} Falling	●	0.10	0.20	0.40	V
$\Delta V_{TMR(LATCH)}$	Timer Latch Mode Hysteresis	V_{TMR} Rising	●	40	75	160	mV
$t_{P,LR}$	Latch Release Propagation Delay to $\overline{RST}$ Low	V_{TMR} Rising, Step 0V to 0.6V	●		0.5	3	µs
$t_{SU,MON}$	Monitor Input Setup Time to Latch Enable (Note 7) Monitor Input Setup Time to Latch Release	V_{TMR} Falling, Step 0.6V to 0V V_{TMR} Rising, Step 0V to 0.6V	●	2			ms
$t_{HD, MON}$	Monitor Input Hold Time to Latch Enable Monitor Input Hold Time to Latch Release	V_{TMR} Falling, Step 0.6V to 0V V_{TMR} Rising, Step 0V to 0.6V	●	0			µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive; all voltages are referenced to GND unless otherwise noted.

Note 3: The internal supply voltage (V_{CC}) is generated from the greater of the voltages on the V1 and V2 inputs. V_{CC} = V1 for the LTC2911-5.

Note 4: Under typical operating conditions, quiescent current is drawn from the greater of the voltages on the V1 and V2 inputs. For the LTC2911-5 only V1 supplies the quiescent current.

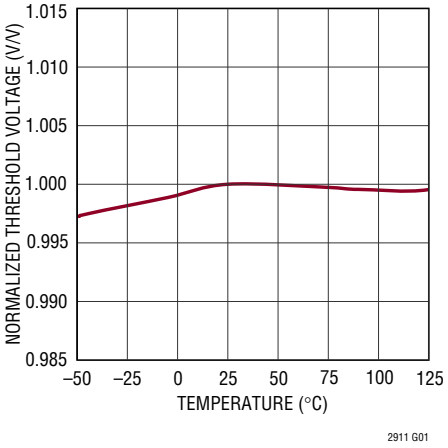
Note 5: The $\overline{RST}$ and $\overline{PFO}$ output pins on the LTC2911 have internal pull-ups to V1. However, for faster rise times or for V_{OH} voltages greater than V1, use an external pull-up resistor.

Note 6: The $\overline{RST}$ and $\overline{PFO}$ pull-down currents are derived from V1 and V2 except for the LTC2911-5 where the pull-down strength is derived only from V1.

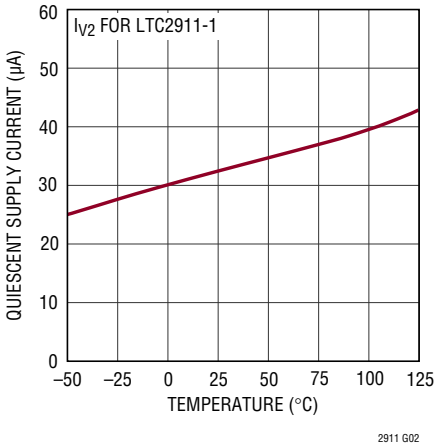
Note 7: $t_{SU,MON}$ is required to latch a low $\overline{RST}$ state and $t_{SU,MON}$ + t_{RST} is required to latch a high $\overline{RST}$ state.

TYPICAL PERFORMANCE CHARACTERISTICS

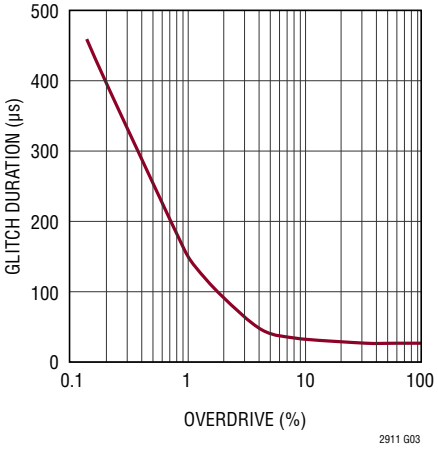
Normalized Reset and Power-Fail Threshold Voltages vs Temperature



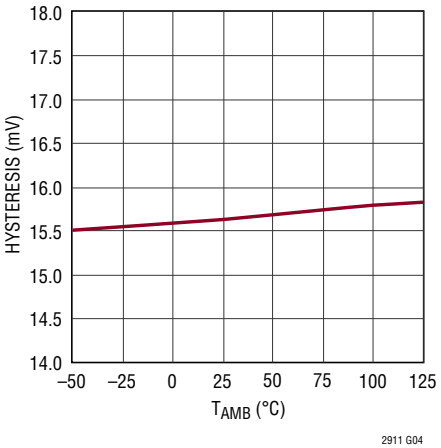
Quiescent Supply Current vs Temperature



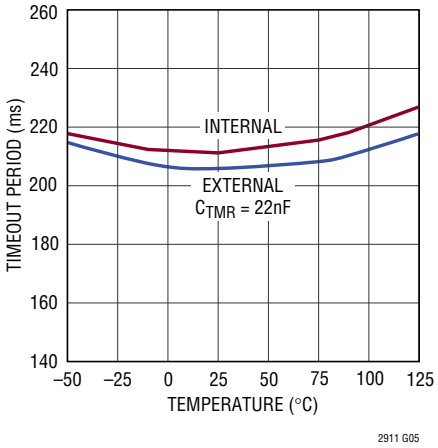
Allowable Glitch Duration vs Overdrive



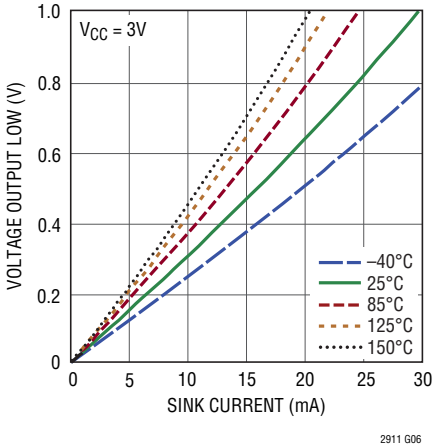
PFI Hysteresis vs Temperature



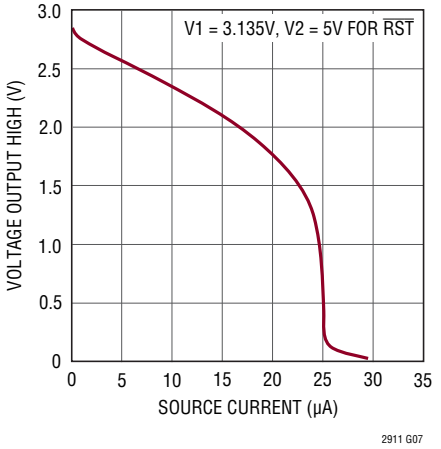
Reset Timeout Period vs Temperature



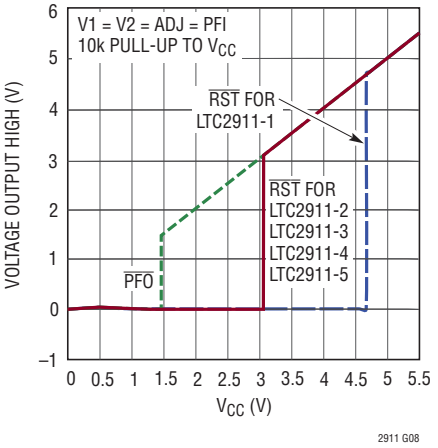
$\overline{RST}$, $\overline{PFO}$ Voltage Output Low vs Sink Current



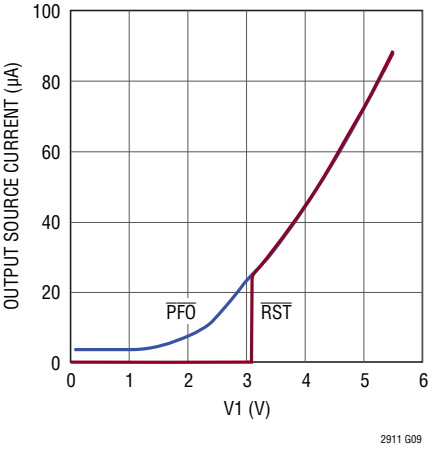
$\overline{RST}$, $\overline{PFO}$ Voltage Output High vs Source Current



$\overline{RST}$, $\overline{PFO}$ Voltage Output High vs V_{CC}



$\overline{RST}$, $\overline{PFO}$ Pin Source Current vs V1



PIN FUNCTIONS

ADJ: Adjustable Voltage Monitor Input. Input to a voltage monitor comparator with a 0.5V nominal threshold. Tie to V1 if unused.

Exposed Pad (DFN Only): Exposed pad may be left open or connected to device ground.

GND: Device Ground.

PFI: Power-Fail Voltage Monitor Input. Input to the power-fail comparator with a 500mV threshold at the falling edge and a 515mV threshold at the rising edge, giving a 3% hysteresis for noise rejection. Tie to V1 or GND if unused.

$\overline{\text{PFO}}$: Power-Fail Logic Output. This pin asserts low when the PFI input voltage is below its threshold and goes high when the PFI input voltage is above its threshold. This pin provides a weak pull-up current to V1. This current is typically 29µA at V1 = 3.3V. The pin can be pulled to voltages higher than V1 by external pull-up resistors. $\overline{\text{PFO}}$ provides an early warning signal of a system power failure.

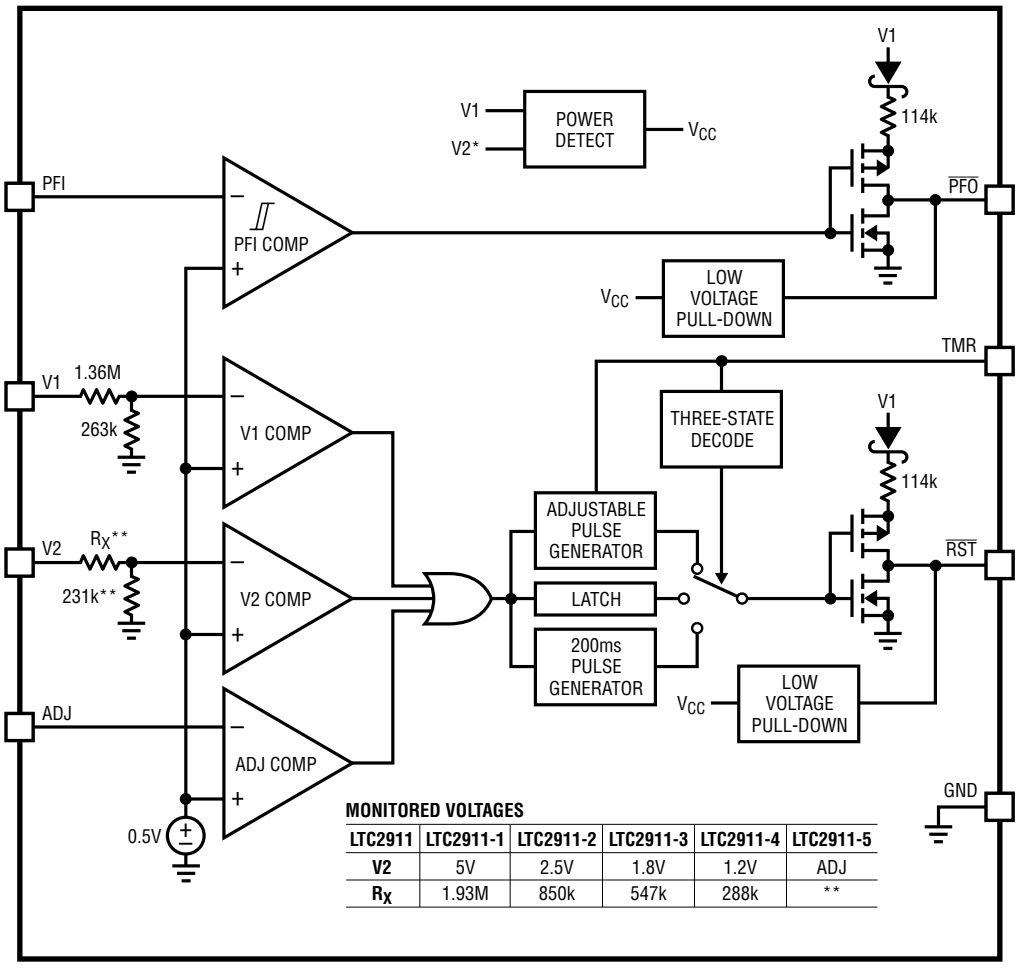
$\overline{\text{RST}}$: Reset Logic Output. This pin asserts low when any of the V1, V2, or ADJ inputs are below their reset thresholds. Pulls high when all the monitored inputs are above their thresholds for longer than a timeout period. This pin provides a weak pull-up current to V1. This current is typically 29µA at V1 = 3.3V. The pin can be pulled to voltages higher than V1 by external pull-up resistors. The status of $\overline{\text{RST}}$ can be latched by holding the TMR pin at GND.

TMR: Reset Timeout Control. Attach an external capacitor, C_{TMR}, to GND to set a reset timeout period of 9.4ms/nF. A low leakage ceramic capacitor is recommended for timer accuracy. A 2.2nF capacitor generates a 20ms timeout. Leaving the TMR pin open without a capacitor generates a minimum timeout of approximately 400µs which will vary depending on the parasitic capacitance on the pin. Tying this pin to V1 enables the internal 200ms timeout. Pulling this pin to GND latches the reset state.

V1: 3.3V Monitor and Power Supply Input. V1 is an accurate 3.3V, –5% undervoltage supply monitor. The internal V_{CC} is generated from the greater of the voltages at the V1 and V2 inputs for the LTC2911-1/LTC2911-2/LTC2911-3/LTC2911-4 options. The LTC2911-5 option always derives its power supply from the V1 pin. Bypass this pin to GND with a 0.1µF (or greater) capacitor for the LTC2911-2 through LTC2911-5.

V2: Voltage Monitor and Power Supply Input. V2 is a –5% undervoltage supply monitor for a 5V, 2.5V, 1.8V or 1.2V supply for the LTC2911-1/LTC2911-2/LTC2911-3/LTC2911-4 options, respectively. Because the internal V_{CC} is generated from the greater of the V1 and V2 inputs for these options, the V2 pin should be bypassed to GND with a 0.1µF (or greater) capacitor for the LTC2911-1. The V2 pin of the LTC2911-5 is a high impedance input with a 0.5V threshold, allowing the trip threshold of the monitored supply to be configured with a resistive divider.

BLOCK DIAGRAM



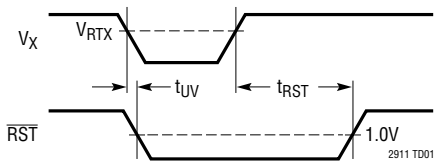
MONITORED VOLTAGES

LTC2911	LTC2911-1	LTC2911-2	LTC2911-3	LTC2911-4	LTC2911-5
V2	5V	2.5V	1.8V	1.2V	ADJ
R_X	1.93M	850k	547k	288k	**

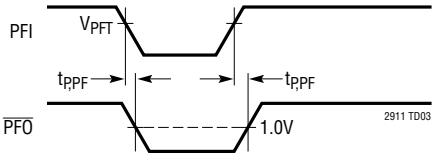
*FOR OPTIONS LTC2911-1 THROUGH LTC2911-4 ONLY. **OMIT THE RESISTIVE DIVIDER FOR THE LTC2911-5.

TIMING DIAGRAMS

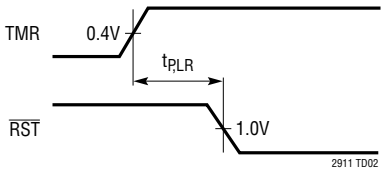
Undervoltage and Reset Timing



Power-Fail Timing



Latch Release to $\overline{RST}$ Low Timing

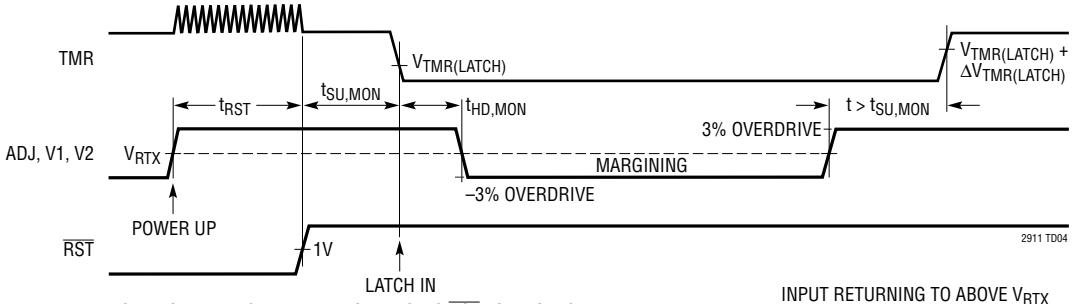


NOTE: ADJ FORCED LOW BEFORE TMR RELEASE

Latching $\overline{RST}$ High

Input Valid to Latch Enable Setup and Hold Timing

Input Valid to Latch Release Setup Timing



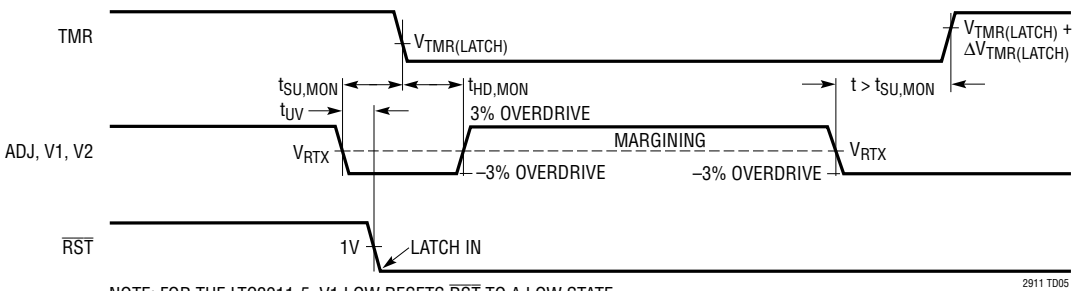
NOTE: FOR THE LTC2911-5, V1 LOW RESETS $\overline{RST}$ TO A LOW STATE

INPUT RETURNING TO ABOVE V_{RTX} FOR $t > t_{SU,MON}$, $\overline{RST}$ PIN STAYS HIGH

Latching $\overline{RST}$ Low

Input Invalid to Latch Enable Setup and Hold Timing

Input Invalid to Latch Release Setup Timing



NOTE: FOR THE LTC2911-5, V1 LOW RESETS $\overline{RST}$ TO A LOW STATE

INPUT RETURNING TO BELOW V_{RTX} FOR $t > t_{SU,MON}$, $\overline{RST}$ PIN STAYS LOW

APPLICATIONS INFORMATION

The LTC2911 is a low power, high accuracy triple supply monitor with power-fail comparator. For the LTC2911-1, LTC2911-2, LTC2911-3 and LTC2911-4 options, the V1 and V2 pins monitor two supplies. Their thresholds are preset internally based on the option chosen. A resistive divider connected to the ADJ pin configures the third threshold. For the LTC2911-5, the V2 pin is a high impedance adjustable input similar to the ADJ pin.

Reset timeout of the device may be selected with an external capacitor or set to an internally generated 200ms. The ADJ, V1 and V2 inputs must be valid (above their thresholds) for longer than the reset timeout period before the $\overline{RST}$ pin transitions high.

The power-fail comparator causes the $\overline{PFO}$ pin to pull low when the PFI pin falls below 0.5V. A resistive divider connected to the PFI pin configures the threshold of the monitored voltage. The $\overline{PFO}$ output typically provides an early warning of imminent power failure so that the system may begin shutdown procedures such as supply sequencing and/or storage of system state in nonvolatile memory.

Power-Up

The LTC2911-1, LTC2911-2, LTC2911-3 and LTC2911-4 supervisors are powered from the V1 and V2 pins, automatically selecting the pin with the higher potential. The exception in the device family, the LTC2911-5, derives its internal supply voltage (V_{CC}) only from V1. When all monitor inputs are above their thresholds, the quiescent supply current drawn from V_{CC} is typically 30µA (35µA for the LTC2911-1). When the three monitor inputs (V1, V2 and ADJ) rise above their thresholds, the appropriate timeout delay begins, after which $\overline{RST}$ pulls to V1. Once the PFI input rises above 515mV, the $\overline{PFO}$ output signals high indicating that the supply or voltage monitored by PFI is above threshold.

The LTC2911 uses proprietary low voltage drive circuitry for the $\overline{RST}$ and $\overline{PFO}$ pins which holds them low with V_{CC} (the higher of V1 and V2) as low as 0.5V. This helps prevent indeterminate voltages from appearing on the outputs during power-up. For additional details refer to the Output Pin Characteristics section.

When V1 and V2 are ramped simultaneously (for LTC2911-1/LTC2911-2/LTC2911-3/LTC2911-4), the pull-down current from the $\overline{RST}$ and $\overline{PFO}$ pins is about twice the current available when V1 or V2 is grounded.

Power Down

On power-down, when the voltage monitored by the power-fail comparator falls below the threshold configured by its resistive divider, the $\overline{PFO}$ pin pulls low to provide an early warning of imminent power failure. In a typically configured system, this occurs before the supplies monitored by V1, V2 or ADJ fall below their thresholds and cause the $\overline{RST}$ pin to pull low. The $\overline{RST}$ and $\overline{PFO}$ pins maintain a logic low output for V_{CC} as low as 0.5V. See the Output PIn Characteristics section for additional details.

Power-Fail Monitoring and $\overline{PFO}$ Signaling

The LTC2911's PFI input monitors a voltage through a resistive divider and compares it to the internal power-fail threshold. When PFI drops below 0.50V (the power-fail threshold) the $\overline{PFO}$ output pulls low to provide an early warning of a low voltage condition. When the PFI pin rises above 0.515V again, the $\overline{PFO}$ output signals high indicating a valid supply condition.

The PFI input typically monitors the primary power supply of a system. For example, the PFI pin may monitor the input supply of a DC/DC converter or a Li-Ion battery stack voltage. The $\overline{PFO}$ output typically provides a warning to the system that the power supply is on the verge of failing so that it can prepare for a controlled shutdown. For

APPLICATIONS INFORMATION

example, the $\overline{PFO}$ pin may connect to a processor nonmaskable interrupt. When the battery pack voltage drops below the shutdown threshold, as sensed at PFI, the PFO pin pulls low to issue an interrupt. Next, the processor begins shutdown procedures which may include supply sequencing and/or storage/erasure of system state in nonvolatile memory.

Threshold Accuracy

Specifying the minimum supply voltage for a system requires the designer to consider three factors: minimum supply voltage for proper operation, power supply tolerance, and supervisor reset threshold accuracy. Highly accurate supervisors ease the design challenge by decreasing the overall voltage margin required for reliable system operation.

The reset threshold band and the power supply tolerance bands should not overlap. This prevents false or nuisance resets when the power supply is actually within its specified tolerance band. The actual reset threshold of supervisors varies over a specified band. The LTC2911 supervisor varies ±1.5% around its nominal threshold voltage over temperature.

Figure 1 illustrates a typical 3.3V monitor. The LTC2911 has ±1.5% reset threshold accuracy. The nearest practical supervisor trip point is the sum of power supply tolerance and the LTC2911 tolerance. So a "5%" threshold is typically set to –6.5%, excluding resistor errors. Thus for a 3.3V "5%" threshold, the practical supervisor trip point is at 3.086V. The threshold is guaranteed to lie in the band between 3.036V and 3.135V over the operating temperature range. This 3.135V maximum threshold is at the lower limit of supply tolerance (3.3V – 5%) to prevent false tripping.

The system must operate reliably a little below 3.036V (or 3.3V, –8%), or risk malfunction before a reset signal is properly issued. A less accurate supervisor increases the supply voltage tolerance requirements and the risk of system malfunction. The LTC2911's ±1.5% threshold voltage specification minimizes these requirements.

V1 and V2 Supply Monitors

All the LTC2911 options have a V1 threshold equal to 3.086V (3.3V – 6.5%). The V2 thresholds are 4.675V (5V – 6.5%), 2.338V (2.5V – 6.5%), 1.683V (1.8V – 6.5%) and 1.122V (1.2V – 6.5%) for options LTC2911-1,

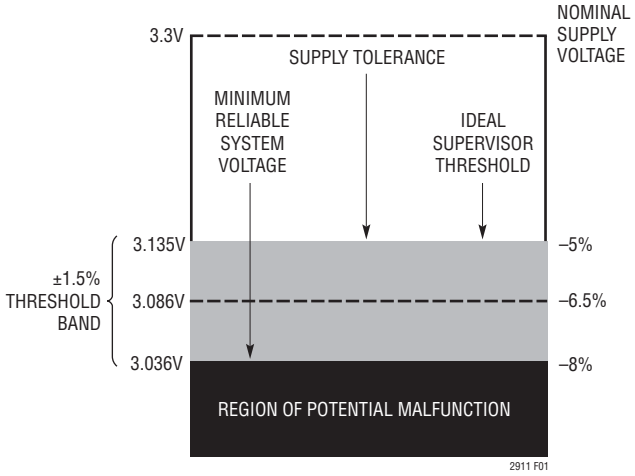


Figure 1. 1.5% Threshold Accuracy Improves System Reliability

APPLICATIONS INFORMATION

LTC2911-2, LTC2911-3 and LTC2911-4 respectively. V2 of the LTC2911-5 option is a high impedance input with a nominal 0.5V threshold.

Input Noise Filtering for $\overline{RST}$

The V1, V2 and ADJ comparators have a response time that is inversely proportional to overdrive. This characteristic is illustrated in the Typical Performance Characteristics as the graph Allowable Glitch Duration versus Overdrive. The ADJ and the LTC2911-5's V2 pin may be bypassed with a capacitor to increase the filtering in applications that demand it. The resultant RC lowpass filter at the inputs will further reject high frequency components, at the cost of slowing the monitor's response to fault conditions.

Resistor Selection for ADJ

The threshold of the supply monitored by the ADJ pin is configured with an external resistive divider (R2 and R1) connected between the supply and ground. The tap point for the divider is connected to the adjustable input (ADJ) which has a 0.5V threshold. (See Figure 2)

Normally, the user selects a trip voltage based on the supply and acceptable tolerances, and a value of R1 based on current drawn. For a given current, I, R1 is given by:

$$R1 = \frac{0.5V}{I}$$

To minimize errors arising from the ADJ input bias current, a value of less than 100k is recommended for R1.

R2 is then chosen by:

$$R2 = R1 \bullet \left(\frac{V_{TRIP\_ADJ}}{0.5V} - 1 \right)$$

where, V_{TRIP_ADJ} is the supply threshold when the ADJ pin falls below its 0.5V threshold.

For accurate monitoring, the resistor tolerance should be as small as possible. Resistor tolerance of 0.1% or some trimming of components should be considered for R2/R1 in applications that require an accurate trip point.

Resistor Selection for PFI

An external resistive divider (R3 and R4) connected between the supply and ground configures the threshold of the supply monitored by the power-fail comparator. The tap point for the divider is connected to the PFI input which has a 0.5V threshold. (See Figure 3a)

Resistor selection follows a process similar to that for the ADJ pin.

R3 is given by:

$$R3 = \frac{0.5V}{I}$$

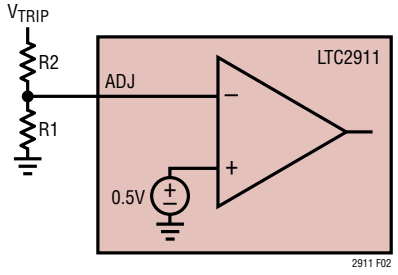


Figure 2. Setting the Adjustable (ADJ) Trip Point

APPLICATIONS INFORMATION

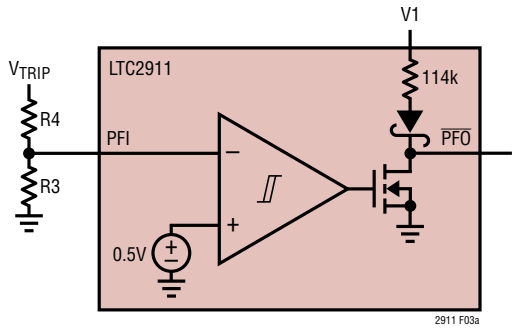


Figure 3a. Setting the Power-Fail (PFI) Trip Point

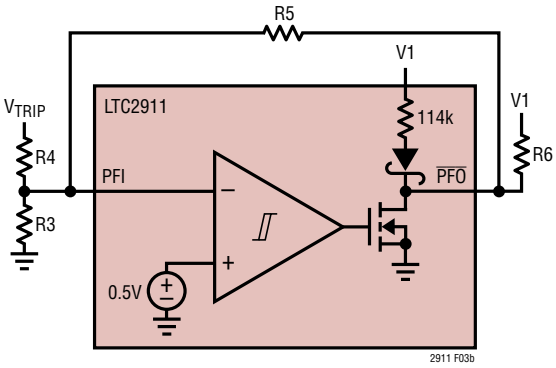


Figure 3b. Increasing Power-Fail Hysteresis

Again, to minimize errors arising from the PFI input bias current, a value of less than 100k is recommended for R3.

R4 can be chosen either using the PFI falling threshold or the PFI rising threshold.

For the falling edge threshold, use the equation:

$$R4 = R3 \bullet \left(\frac{V_{TRIP\_PFI\_FALL}}{0.5V} - 1 \right)$$

Alternatively, for the rising edge threshold, use the equation:

$$R4 = R3 \bullet \left(\frac{V_{TRIP\_PFI\_RISE}}{0.515V} - 1 \right)$$

where $V_{TRIP\_PFI\_FALL}$ is the supply threshold when the PFI pin falls below the 0.5V falling threshold, and $V_{TRIP\_PFI\_RISE}$ is the supply threshold when the PFI pin rises above the 0.515V rising threshold.

Note that $V_{TRIP\_PFI\_RISE}$ is typically 3% above the $V_{TRIP\_PFI\_FALL}$ due to the fact that the PFI 515mV rising threshold is 3% above its 500mV falling threshold.

In applications that require an accurate trip point, the R4 and R3 resistors should have small tolerances.

Hysteresis for Power-Fail Comparator

The power-fail comparator uses a positive 3% accurate hysteresis to combat spurious triggering while maintaining accurate thresholds for both the rising and falling edges. The nominal threshold is 500mV at the falling edge and 515mV at the rising edge. The hysteresis prevents oscillation when the monitored voltage passes through the thresholds. If the PFI pin is connected to an external resistive divider, it may be bypassed with a capacitor for additional noise filtering.

Increasing the Power-Fail Hysteresis

The power-fail comparator hysteresis can be increased by adding two resistors, R5 and R6, as shown in Figure 3b. When $\overline{PFO}$ is low, R5 sinks current from the center tap of the R3 and R4 resistive divider. The upper threshold is therefore given by:

$$V_H = 0.515V\left(1 + \frac{R4}{R3} + \frac{R4}{R5}\right)$$

When $\overline{PFO}$ is high, the series combination of R5 and R6 sources current into the center tap of the R3 and R4 resistive divider. This leads to a lower threshold of:

$$V_L = 0.5V\left(1 + \frac{R4}{R3}\right) - \frac{(3.3V - 0.5V)R4}{R5 + R6}$$

The addition of R5 and R6 increases the hysteresis to:

$$V_{HYST} = V_H - V_L$$

$$= 0.015\left(1 + \frac{R4}{R3}\right) + 0.515\left(\frac{R4}{R5}\right) + \frac{(3.3V - 0.5V)R4}{R5 + R6}$$

APPLICATIONS INFORMATION

Resistor Selection for Combined Reset and Power-Fail Divider

When the power-fail and reset signals are based on the same supply, the PFI and ADJ inputs may be connected to a single resistive divider formed from three resistors. The configuration is shown in Figure 4. For a given bias current I, R_A, R_B and R_C can be calculated from:

$$R_A = \frac{0.5V}{I}$$

$$R_B = R_A \bullet \left(\frac{V_{TRIP\_PFI\_FALL}}{V_{TRIP\_ADJ}} - 1 \right)$$

$$R_C = R_A \bullet \left(\frac{V_{TRIP\_ADJ}}{0.5V} - 1 \right) \bullet \left(\frac{V_{TRIP\_PFI\_FALL}}{V_{TRIP\_ADJ}} \right)$$

For example, consider monitoring a 5V, ±5% supply with $V_{TRIP\_PFI\_FALL}$ = 4.5V and V_{TRIP_ADJ} = 4V. The resulting $V_{TRIP\_PFI\_RISE}$ is equal to 4.63V or 3% above $V_{TRIP\_PFI\_FALL}$. The maximum $V_{TRIP\_PFI\_RISE}$ should not overlap the minimum power supply voltage level for $\overline{PFO}$ to deassert when the supply recovers. Mathematically, after factoring in the sum of the power supply tolerance and the LTC2911 tolerance, the $V_{TRIP\_PFI\_RISE}$ should be lower than 5V – 6.5%.

See Threshold Accuracy section for more details. In the design, if we wish to consume about 5µA in the divider, R_A = 100k. We then find R_B = 12.4k and R_C = 787k (nearest 1% standard values).

Setting the Reset Timeout

$\overline{RST}$ goes high after the V1, V2 and ADJ inputs are above their thresholds for a reset timeout period. Connecting the TMR pin to V1 enables the internal 200ms timer. To configure a different reset timeout period connect a capacitor between the TMR pin and ground.

The following formula approximates the value of capacitor needed for a particular timeout:

$$C_{TMR} = t_{RST} \bullet 106.5\ [pF/ms]$$

Leaving the TMR pin open with no external capacitor generates a reset timeout of approximately 400µs. Larger capacitors may be used to increase the timeout, but the capacitor leakage current must not exceed 500nA. Otherwise, the timer accuracy will be severely affected.

Suitable values of C_{TMR} for a given t_{RST} may be selected from Figure 5.

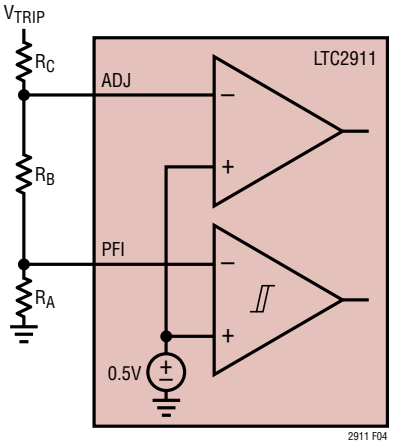


Figure 4. Combining PFI/ADJ Monitoring of One Supply with Three Resistors

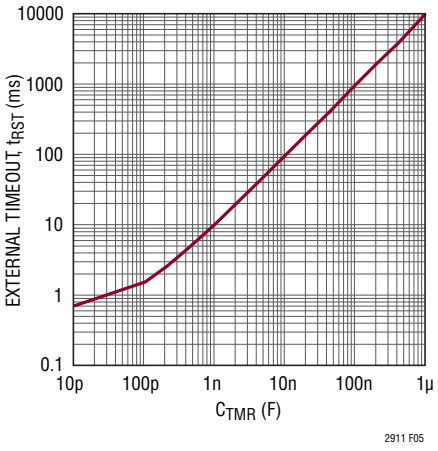


Figure 5. External Timeout vs C_{TMR}

APPLICATIONS INFORMATION

Reset Latch Mode

At any time, the TMR pin can be pulled low to latch the $\overline{RST}$ pin status, overriding the reset operation. This feature is useful when testing a system at supply voltages that might otherwise cause the $\overline{RST}$ pin to assert.

If the $\overline{RST}$ pin is unasserted (high) before the latch is enabled (by pulling the TMR pin low), $\overline{RST}$ will remain unasserted after the TMR pin is released. This is true provided that all reset monitor inputs are valid when TMR releases, regardless of their state while the TMR pin was low. However, if $\overline{RST}$ was unasserted before TMR was pulled low, and now one of the inputs is invalid when TMR is released, $\overline{RST}$ will assert after a t_{PL_LR} propagation delay (see Figure 6a). Conversely, if $\overline{RST}$ was asserted (low) before TMR was pulled low, and all inputs are valid when TMR is released, $\overline{RST}$ will deassert (go high) after a t_{RST} delay (see Figures 6b and 6c). The $\overline{RST}$ pin remains asserted for a full t_{RST} timeout after the TMR pin is released, regardless of the state of the t_{RST} timer before the latch was enabled. The reset latch mode is useful for performing supply margining tests without resetting the system (see Figure 6d).

At least 2.9µA of pull-up or pull-down current is required to hold the TMR pin high or low to configure the internal timer or reset latch mode. However, during the timer mode transition, 100µA will be required to switch the TMR floating state to ground or V1. Connecting the TMR pin to any voltage other than ground or V1 may have unpredictable results.

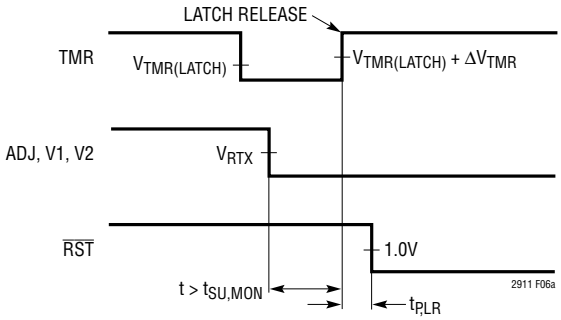


Figure 6a. Input Toggled Low While Timer Latched. $\overline{RST}$ Goes Low $t_{P,LR}$ After Latch Release

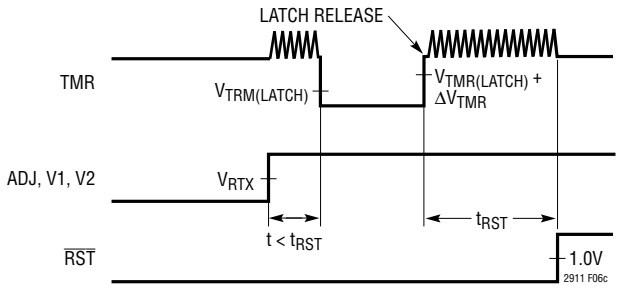


Figure 6c. Timer Latched Before Timeout. After Latch Release, $\overline{RST}$ Stays Low for a Full Timeout Before Going High

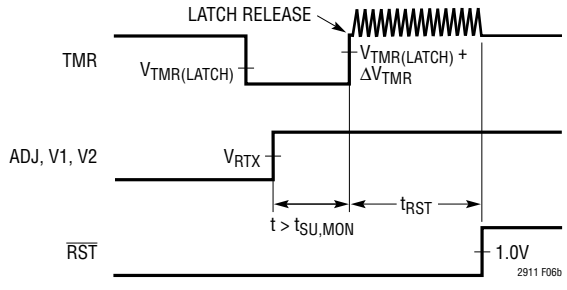


Figure 6b. Input Toggled High While Timer Latched. $\overline{RST}$ Goes High t_{RST} After Latch Release

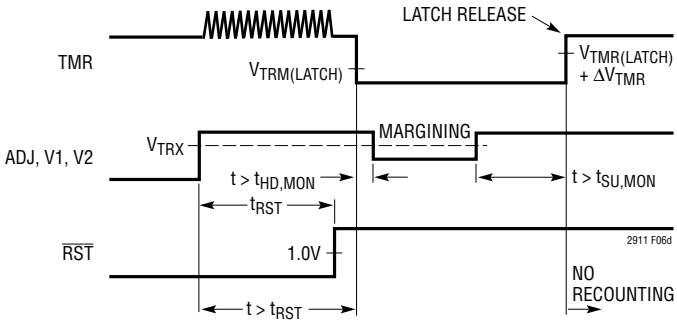


Figure 6d. Timer Latched After Timeout and $\overline{RST}$ High. $\overline{RST}$ Stays High After Margining if Inputs are Restored Before Release

APPLICATIONS INFORMATION

During power-up, with a capacitor connected to the TMR pin, the part remains in the reset latch mode described above until the 2.2µA flowing out of the TMR pin charges the capacitor beyond the $V_{TMR(LATCH)}$ threshold. For this reason, large capacitors will extend the $\overline{RST}$ timeout during power-up. For example, if C_{TMR} = 1µF, the LTC2911 leaves the reset latch mode 90ms after power-up and the $\overline{RST}$ pin goes high after a 9 second timeout.

Figures 7a and 7b show how the TMR pin can be driven low to latch the state of the $\overline{RST}$ pin or floated or driven high for external and internal reset timing, respectively.

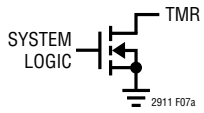


Figure 7a. Open-Drain (or Three-State Buffer) Output. Grounds TMR to Latch the State of $\overline{RST}$. Floats TMR for External Reset Timing

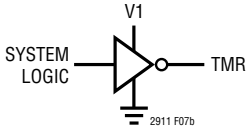


Figure 7b. V1 Powered Inverter. Grounds TMR to Latch the State of RST. Drives TMR High for Internal Reset Timing

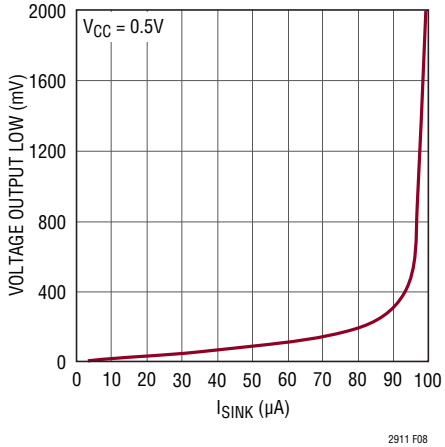


Figure 8. Voltage Output Low vs I_{SINK} at V_{CC} = 0.5V

Output Pin Characteristics

The DC characteristics of the $\overline{RST}$ and $\overline{PFO}$ pull-down strength are shown in the Typical Performance Characteristics. The circuits that drive the pull-down of the output pins are powered by the internal V_{CC} (the greater voltage of V1 or V2). During power-up, a V_{CC} of at least 0.5V ensures a low output state. The V_{OL} voltage depends on the current sunk by $\overline{RST}$ and $\overline{PFO}$ as shown in the Figure 8. The open-drain nature of the $\overline{RST}$ and $\overline{PFO}$ pins allows for wire-ORed connections. For example, multiple LTC2911s may be wire-ORed to monitor additional supplies, or open-drain logic can be connected to allow other conditions to issue the reset and/or power-fail signals.

Output Pin Rise and Fall Time

The open-drain output pins ($\overline{RST}$ and $\overline{PFO}$) contain weak pull-up circuitry to V1. Use an external pull-up resistor when the outputs need to pull beyond V1 and/or require a faster rise time. Use external pull-up resistor values of 100k or less.

When output pins are externally pulled up to voltages higher than V1, an internal network automatically protects the weak pull-up circuitry from reverse currents. For a given external load capacitance or C_{LOAD}, the rise and fall times can be estimated using Figure 9. The output pins have very strong pull-down capability. With a 150pF load capacitance the reset line can pull down in about 30ns.

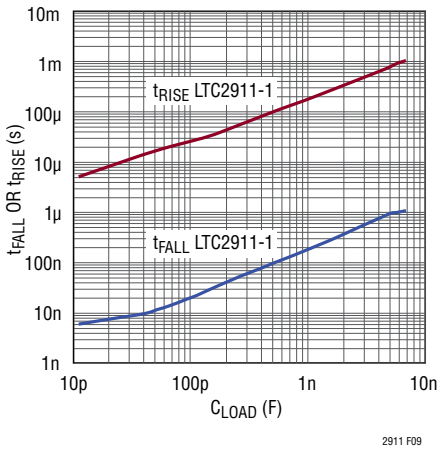
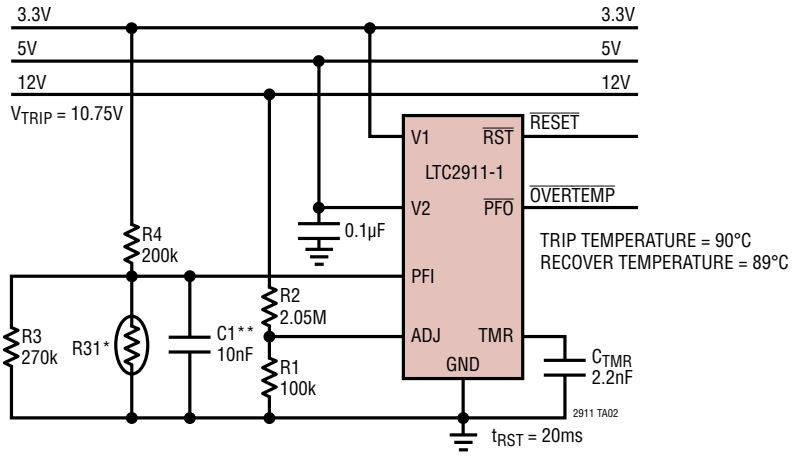


Figure 9. t_{RISE} and t_{FALL} vs C_{LOAD}

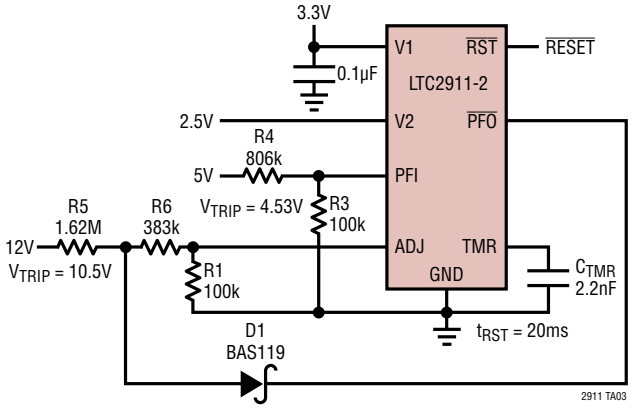
TYPICAL APPLICATIONS

Triple Supply Monitor and Overtemperature Signal



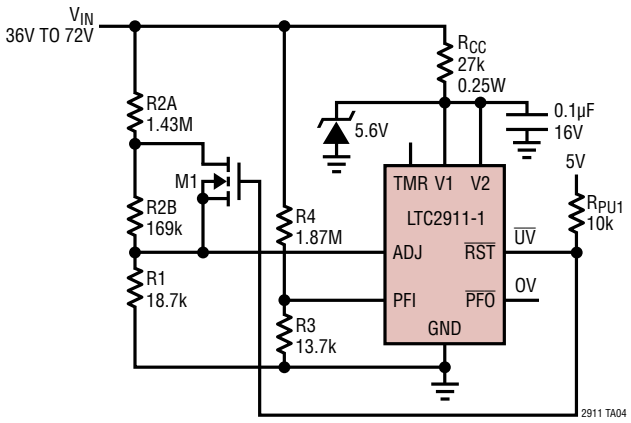
*THERMISTOR MURATA NTC NCP15WM474J03RC TOLERANCE 5%.
NTC RESISTANCE IS 474k AT ROOM, 35.8k AT 85°C
**OPTIONAL BYPASS CAPACITOR FOR SUPPLY TRANSIENT NOISE FILTERING

Quad Supply Monitor



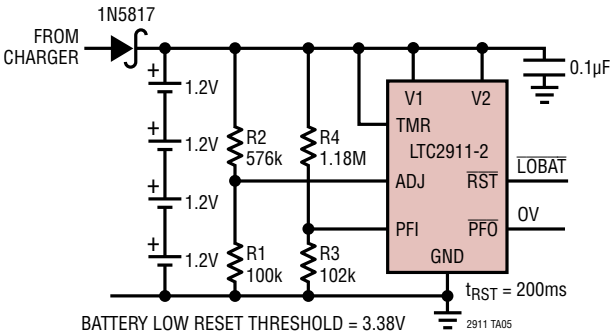
TYPICAL APPLICATIONS

48V Telecom UV/OV Monitor with Hysteresis



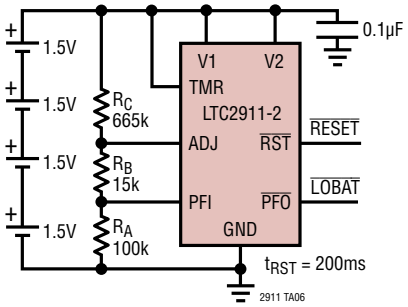
M1: FDG6301N OR SIMILAR
$V_{UV(RISING)}$ = 43.3V
$V_{UV(FALLING)}$ = 38.7V
$V_{OV(RISING)}$ = 70.8V
$V_{OV(FALLING)}$ = 68.8V

4-Cell NiMH Stack Voltage Monitor with Input Overvoltage Signaling



BATTERY LOW RESET THRESHOLD = 3.38V
OVERVOLTAGE TRIP THRESHOLD = 6.47V
OVERVOLTAGE RECOVER THRESHOLD = 6.28V

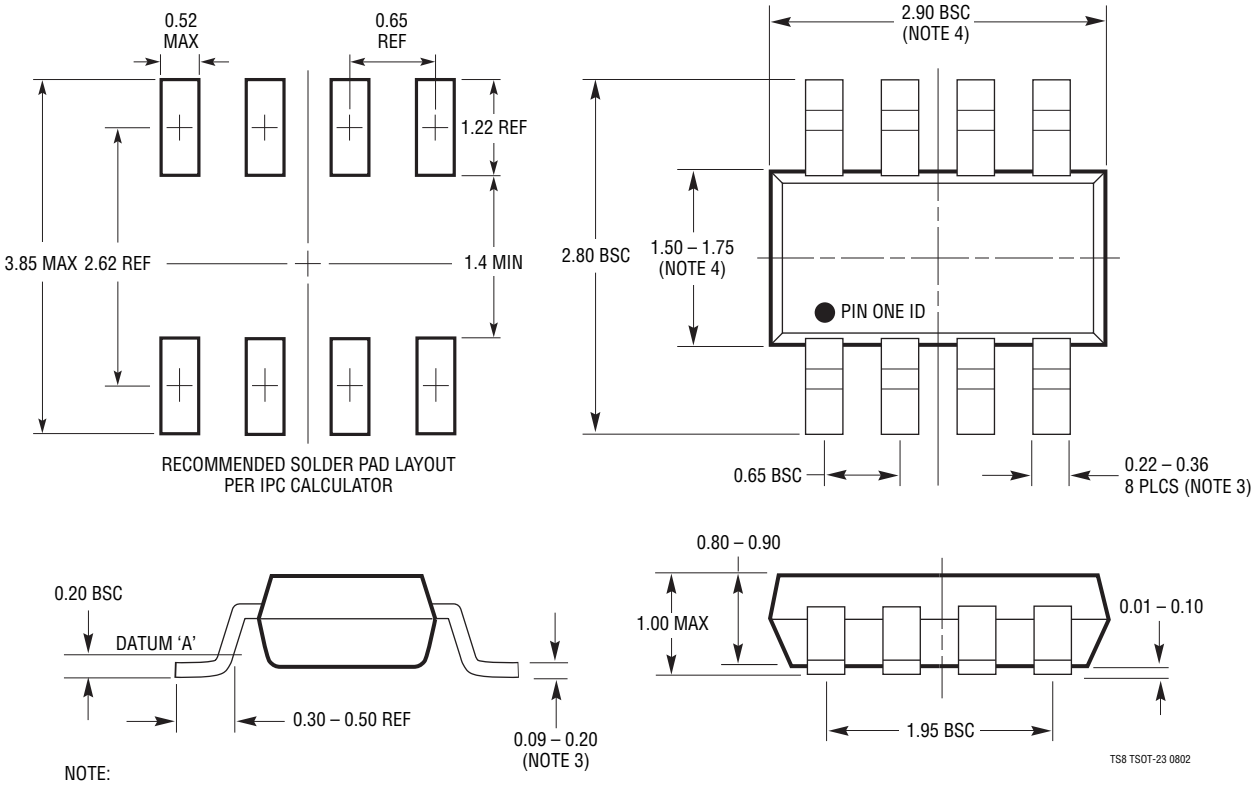
4-Cell Alkaline Stack Voltage Monitor with Early Power-Fail Warning



POWER-FAIL FALLING THRESHOLD = 3.90V
POWER-FAIL RISING THRESHOLD = 4.02V
RESET THRESHOLD = 3.39V

PACKAGE DESCRIPTION

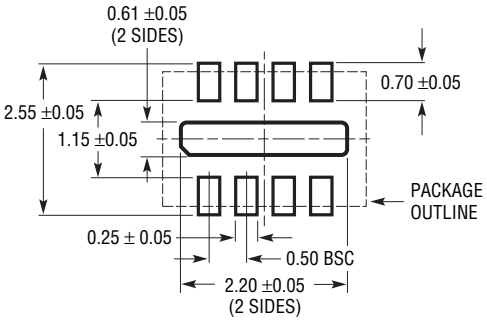
TS8 Package
8-Lead Plastic TSOT-23
(Reference LTC DWG # 05-08-1637)



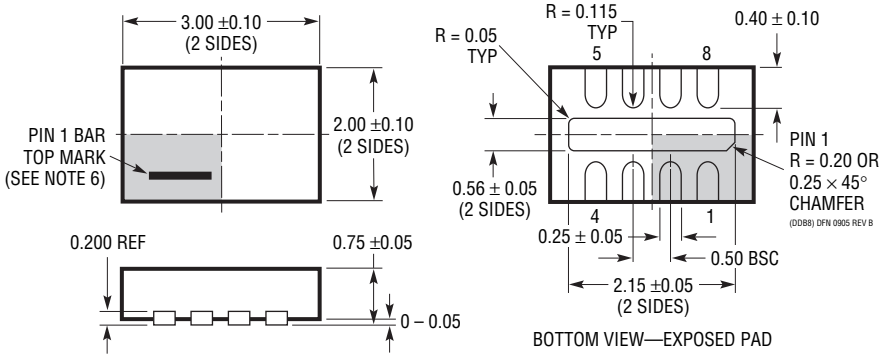
NOTE:
1. DIMENSIONS ARE IN MILLIMETERS
2. DRAWING NOT TO SCALE
3. DIMENSIONS ARE INCLUSIVE OF PLATING
4. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH AND METAL BURR
5. MOLD FLASH SHALL NOT EXCEED 0.254mm
6. JEDEC PACKAGE REFERENCE IS MO-193

PACKAGE DESCRIPTION

DDB Package
8-Lead Plastic DFN (3mm × 2mm)
(Reference LTC DWG # 05-08-1702 Rev B)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

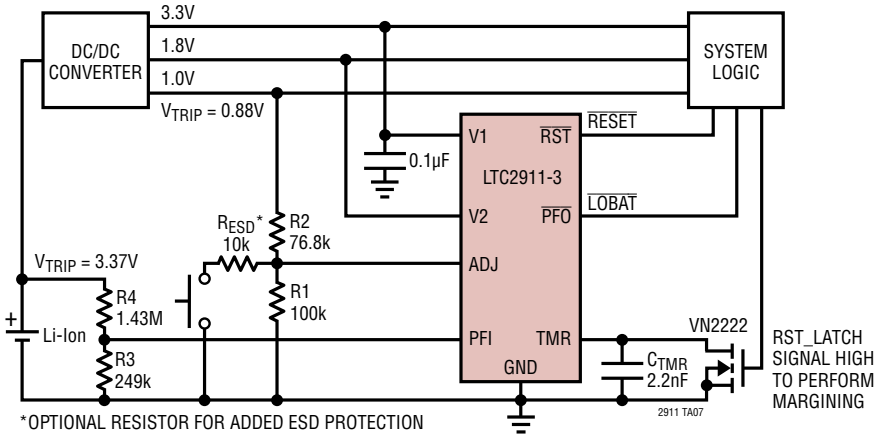


BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING CONFORMS TO VERSION (WECD-1) IN JEDEC PACKAGE OUTLINE M0-229
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

TYPICAL APPLICATION

Triple Supply Monitor with Early Power-Fail Warning (With Manual Reset and Latchable Reset for Margining)



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1326/LTC1326-2.5	Micropower Precision Triple Supply Monitor for 5V/2.5V, 3.3V and ADJ	4.725V, 3.118V, 1V Threshold (±0.75%)
LTC1536	Precision Triple Supply Monitor for PCI Applications	Meets PCI t_{FAIL} Timing Specifications
LTC1726-2.5/LTC1726-5	Micropower Triple Supply Monitor for 2.5V/5V, 3.3V and ADJ	Adjustable Reset and Watchdog Timeouts
LTC1727/LTC1728	Micropower Triple Supply Monitor With Open-Drain Reset	Individual Monitor Outputs in MSOP/5-Lead SOT-23
LTC1985-1.8	Micropower Triple Supply Monitor with Push-Pull Reset Output	5-Lead SOT-23 Package
LTC2909	Precision, Triple/Dual Input UV, OV and Negative Voltage Monitor	8-Lead SOT-23 and DFN Packages
LTC2912/LTC2913/ LTC2914	Single/Dual/Quad UV and OV Voltage Monitors	Separate V_{CC} Pin, Adjustable Reset Timer, H-Grade Temperature Range
LTC2915/LTC2916/ LTC2917/LTC2918	Single Voltage Monitor With 27 Unique Thresholds	Manual Reset, Watchdog, TSOT-8/MSOP-10 and 3mm × 2mm DFN Packages, H-Grade Temperature Range
LTC2919	Precision, Triple/Dual Input UV, OV and Negative Voltage Monitor	10-Lead 3mm × 2mm and MSOP Packages, H-Grade Temperature Range (Individual Outputs for ADJ Comparators and System $\overline{RST}$)

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