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Programmable Six Channel Sequencer and Voltage Supervisor with EEPROM

FEATURES

- **Time and Event Based Sequencing**
- **12 Programmable Undervoltage (UV) and Overvoltage (OV) Comparators: ±0.75% Accuracy**
- **I²C/SMBus Interface**
- **Stalled Power Supply Detection**
- **Single Wire Synchronization Allows Controller Expansion to 50 Devices (300 Power Supplies)**
- **Configuration and Fault Logging in EEPROM**
- EEPROM Specified Over Entire Temperature Range, Rated to 125°C, 10k Writes, 20yr Retention
- Supported by LTpowerPlay® GUI
- Fault and System Status Registers
- Reset Output with Programmable Delay
- Wide Input Supply Voltage Range: 2.9V to 16.5V
- 28-Lead QFN (5mm × 6mm) Package

APPLICATIONS

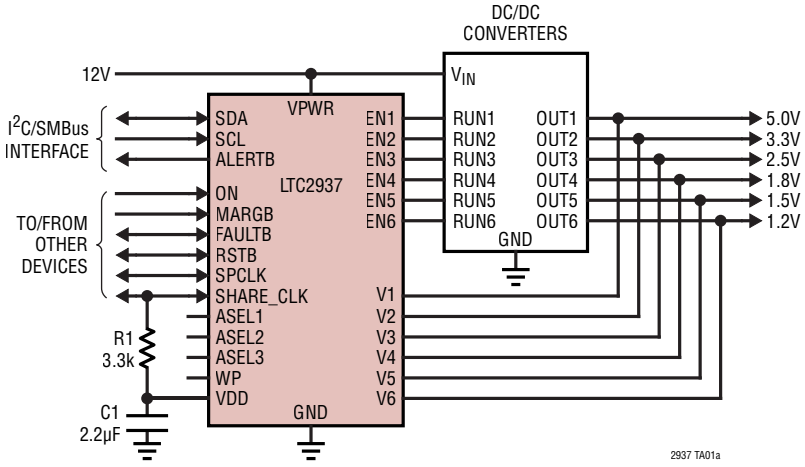
- Network Servers
- Data Storage Systems
- Telecom Equipment
- High Availability Computer Systems

DESCRIPTION

The LTC®2937 is a 6-channel power supply sequencer and voltage supervisor. Supplies are enabled or disabled with precise user controlled order and time spacing. To detect power supply output faults during sequencing and monitoring, the LTC2937 accurately monitors supply turn-on/-off delays and output voltage levels. In the event of a fault, response actions include complete power supply shutdown and optional restarts. Root cause of power faults are logged to EEPROM. For systems with high supply count, a simple single wire connection between multiple LTC2937 devices allows sequencing expansion to 300 supplies. After successful sequencing and supply voltage stabilization, the reset output pulls high to initiate microprocessor or other system activity. To accommodate supply margin testing, the reset output can be disabled. Upon supply turn-off, integrated current sources are available as needed to discharge slowly decaying supplies. Configuration EEPROM supports autonomous operation without software.

TYPICAL APPLICATION

Six Power Supply Sequencer and Supervisor



Sequenced Power Supply Waveforms

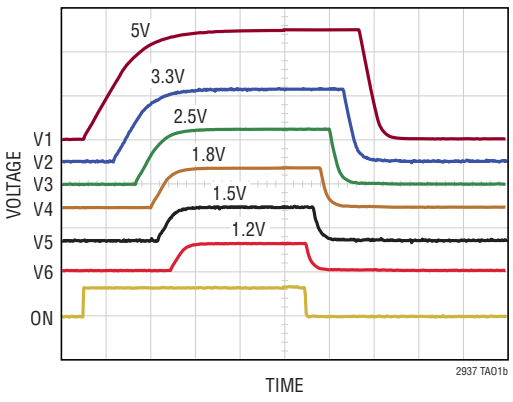


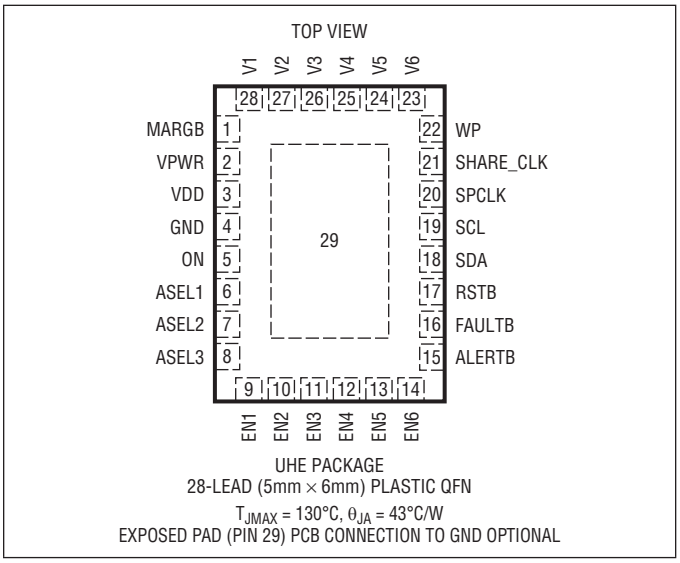
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

VPWR ..... –0.3V to 18V
EN1, EN2, EN3, EN4, EN5, EN6 ..... –0.3V to 16V
VDD, ALERTB, FAULTB, MARGB, RSTB,
ON, SCL, SDA, SHARE_CLK, SPCLK, WP,
V1, V2, V3, V4, V5, V6..... –0.3V to 6V
ASEL1, ASEL2, ASEL3..... –0.3V to VDD
Input Currents
V1, V2, V3, V4, V5, V6.....–1mA
Operating Junction Temperature Range
LTC2937C ..... 0°C to 70°C
LTC2937I .....–40°C to 85°C
LTC2937H..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 150°C
Maximum Junction Temperature ..... 130°C

PIN CONFIGURATION



UHE PACKAGE
28-LEAD (5mm × 6mm) PLASTIC QFN
T_{JMAX} = 130°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) PCB CONNECTION TO GND OPTIONAL

ORDER INFORMATION

http://www.linear.com/product/LTC2937#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2937CUHE#PBF	LTC2937CUHE#TRPBF	2937	28-Lead (5mm × 6mm) Plastic QFN	0°C to 70°C
LTC2937IUHE#PBF	LTC2937IUHE#TRPBF	2937	28-Lead (5mm × 6mm) Plastic QFN	–40°C to 85°C
LTC2937HUHE#PBF	LTC2937HUHE#TRPBF	2937	28-Lead (5mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VPWR = 12V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Device Power							
V_{VPWR}	VPWR Supply Input Operating Range		●	4.5		16.5	V
I_{VPWR}	VPWR Supply Current	Sequencing Complete, No VDD Load Writing to EEPROM	● ●			1 3	mA mA
VDD_{REG}	VDD Regulated Output	VPWR ≥ 4.5V, I_{VDD} = –1mA	●	3.234	3.3	3.366	V
V_{OP}	VDD Operating Range	VDD Connected to VPWR	●	2.9		5.5	V
V_{UVL}	VDD Undervoltage Lockout	VDD Rising	●	2.5	2.7	2.85	V
$V_{UVL(HYST)}$	VDD Undervoltage Lockout Hysteresis	VDD Falling			75		mV
V1, V2, V3, V4, V5, V6							
V_{MON}	V*n* Monitoring Thresholds (*n* = 1 through 6) (Note 3)	Adjustable Range Low Range High Range	● ● ●	0.2 0.5 1		1.2 3 6	V V V
V_{RES}	V*n* Threshold Programming LSB Resolution	Adjustable Range Low Range High Range			4 10 20		mV mV mV
$V_{MON(ACC)}$	V*n* Threshold Accuracy by Code (Note 4)	C-, I-Grades: Codes 155 to 255 Codes 55 to 154 Codes 5 to 54 H-Grade: Codes 155 to 255 Codes 55 to 154 Codes 5 to 54	 ● ● ● ● ● ●			 ±0.75 ±0.75 ±1.5 ±1 ±1 ±1.5	 % % % % % %
$V_{MON(HYST)}$	Temporary Sequence-Up Threshold Hysteresis (Note 5)	Sequence Up Threshold Achieved	●	–4	–5	–6	%
t_{PD}	V*n* Comparator Propagation Delay	2 LSB Overdrive of Configured Threshold 10 LSB Overdrive of Configured Threshold	 ●		35 10	 25	µs µs
R_{IN}	V*n* Input Resistance	Low Range and High Range	●	400	600	900	kΩ
I_{LKG}	V*n* Input Leakage Current	Adjustable Range, V = 1.2V	●			±15	nA
R_{ON}	V*n* Discharge On Resistance	V = 0.4V	●	25	40	50	Ω
$I_{AD(MAX)}$	V*n* Discharge Current	V = 1.8V	●	20	35	45	mA
V_{DTH}	V*n* Discharge Threshold	High and Low Range Adjustable Range (Positive Polarity) Adjustable Range (Negative Polarity)	● ● ●	300 50 1.12	400 120 1.2	500 190 1.28	mV mV V
EEPROM							
	Retention	(Notes 6, 7)	●	20			Years
	Endurance	1 Cycle = 1 STORE Command (Notes 6, 7)	●	10,000			Cycles
t_{PT}	Programming Time (Note 8)	STORE Command	●			130	ms
t_{RT}	Restore Time	RESTORE Command	●			2	ms
RSTB							
t_{RST}	Programmable Reset Delay (Register 0x22, RSTB_CONFIG)	b[15:13] = 000b b[15:13] = 001b b[15:13] = 010b b[15:13] = 011b b[15:13] = 100b b[15:13] = 101b b[15:13] = 110b b[15:13] = 111b	● ● ● ● ● ● ● ●	0 1.4 5.8 22 46 180 370 1480	0.05 1.6 6.4 26 51 200 410 1640	0.1 1.9 7.5 30 60 230 475 1900	ms ms ms ms ms ms ms ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VPWR = 12V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Sequence Timers							
t_{ON_MAX}	ton_max time (Registers 0x0A through 0x0F)	b[15:13] = 000b	●	∞	∞	∞	s
		b[15:13] = 001b	●	136	160	195	µs
		b[15:13] = 010b	●	540	640	780	µs
		b[15:13] = 011b	●	2.2	2.6	3.2	ms
		b[15:13] = 100b	●	8.7	10.2	12.4	ms
		b[15:13] = 101b	●	35	41	50	ms
		b[15:13] = 110b	●	140	164	200	ms
		b[15:13] = 111b	●	560	655	800	ms
t_{OND}	ton_delay Time (Registers 0x0A through 0x0F)	Timer Register Value N = b[12:0]	●	68 • N	80 • N	96 • N	µs
t_{OFF_MAX}	toff_max Time (Registers 0x10 through 0x15)	b[15:13] = 000b	●	∞	∞	∞	s
		b[15:13] = 001b	●	2.2	2.6	3.2	ms
		b[15:13] = 010b	●	8.7	10.2	12.4	ms
		b[15:13] = 011b	●	35	41	50	ms
		b[15:13] = 100b	●	140	164	200	ms
		b[15:13] = 101b	●	560	655	800	ms
		b[15:13] = 110b	●	2.3	2.6	3.2	s
		b[15:13] = 111b	●	9	10.5	13	s
t_{OFFD}	toff_delay Time (Registers 0x10 through 0x15)	Timer Register Value N = b[12:0]	●	68 • N	80 • N	96 • N	µs
SPCLK							
t_{ONSQ}	ON Input to Start of SPCLK	(Note 9)	●	40	80	120	µs
I_{PU}	SPCLK Pull-Up Current	V_{SPCLK} = GND	●	–30	–55	–80	µA
t_{LO}	Minimum SPCLK Low Time		●	16	20	26	µs
t_{HI}	Minimum SPCLK High Time		●	48	60	75	µs
t_{FLOAT}	SPCLK Float High Time	End of Sequencing	●	260	320	400	µs
SHARE_CLK							
f_{SHR}	Share Clock Frequency		●	85	100	110	kHz
Analog and Digital I/O							
V_{TH}	Input Threshold: ON, MARGB, WP, RSTB, FAULTB, SHARE_CLK, SPCLK		●	1	1.2	1.4	V
$V_{TH(HYST)}$	Input Threshold Hysteresis: ON, MARGB, WP, RSTB, FAULTB, SHARE_CLK, SPCLK				50		mV
V_{OL}	Voltage Output Low: ALERTB, RSTB, FAULTB, SHARE_CLK, SPCLK, EN1, EN2, EN3, EN4, EN5, EN6	I_{SINK} = 3mA	●		0.2	0.4	V
I_{PU}	Internal Pull-Up Current: ON, MARGB, WP, ALERTB, RSTB, FAULTB	V = GND	●	–4	–10	–16	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C and VPWR = 12V. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	Leakage Current: ALERTB, RSTB, FAULTB Leakage Current: EN1, EN2, EN3, EN4, EN5, EN6	V = 5.5V V = 15V	● ●			±1 ±1	µA µA
V_{OH}	Voltage Output High: ALERTB, RSTB, FAULTB	I_{SOURCE} = –1µA	●	VDD – 1			V
t_{PW}	Minimum Detectable Pulse Width: ON, FAULTB		●	25			µs
Serial Bus Interface and Address Inputs							
$V_{ASEL(H)}$	ASEL Input High Threshold		●	VDD – 0.4			V
$V_{ASEL(L)}$	ASEL Input Low Threshold		●			0.4	V
$V_{ASEL(OC)}$	ASEL Open Circuit Voltage				0.5 • VDD		V
$V_{ASEL(OCR)}$	ASEL Allowable Open Circuit Voltage Range		●	0.4 • VDD		0.6 • VDD	V
$I_{ASEL(HZ)}$	Allowable Leakage in Open State		●			±1	µA
	ASEL Input Resistance		●	120	180	280	kΩ
V_{STH}	SDA, SCL Input Threshold		●	1.5	1.8	2	V
I_{STH}	SDA, SCL Input Current	SDA or SCL = 5.5V	●		0	±2	µA
$V_{SDA(OL)}$	SDA Output Low Voltage	I_{SDA} = 3mA	●		0.3	0.4	V
Serial Bus Timing (Note 10)							
$f_{SCL(MIN)}$	Minimum Serial Clock Frequency		●			10	kHz
$f_{SCL(MAX)}$	Maximum Serial Clock Frequency		●	400			kHz
$t_{LOW(MIN)}$	Serial Clock Low Period		●			1.3	µs
$t_{HIGH(MIN)}$	Serial Clock High Period		●			0.6	µs
$t_{BUF(MIN)}$	Bus Free Time Between Stop and Start		●			1.3	µs
$t_{HD,STA(MIN)}$	Start Condition Hold Time		●			600	ns
$t_{SU,STA(MIN)}$	Start Condition Setup Time		●			600	ns
$t_{SU,STO(MIN)}$	Stop Condition Setup Time		●			600	ns
$t_{HD,DAT(MIN)}$	Data Hold Time	(LTC2937 Receiving Data)	●			0	ns
$t_{HD,DAT}$	Data Hold Time	(LTC2937 Transmitting Data)	●	300		900	ns
$t_{SU,DAT(MIN)}$	Data Setup Time		●			100	ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: Subscript (or placeholder) *n* denotes a channel number and is applied throughout this document.

Note 4: Threshold codes 0 through 4 are not used.

Note 5: During sequence-up operation, undervoltage comparators participating in sequencing receive a temporary 5% hysteresis after the respective monitored voltage exceeds its threshold for the first time. The hysteresis remains active until 50% of the programmed reset delay time has been completed. See the timing diagram and applications information for more details.

Note 6: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls.

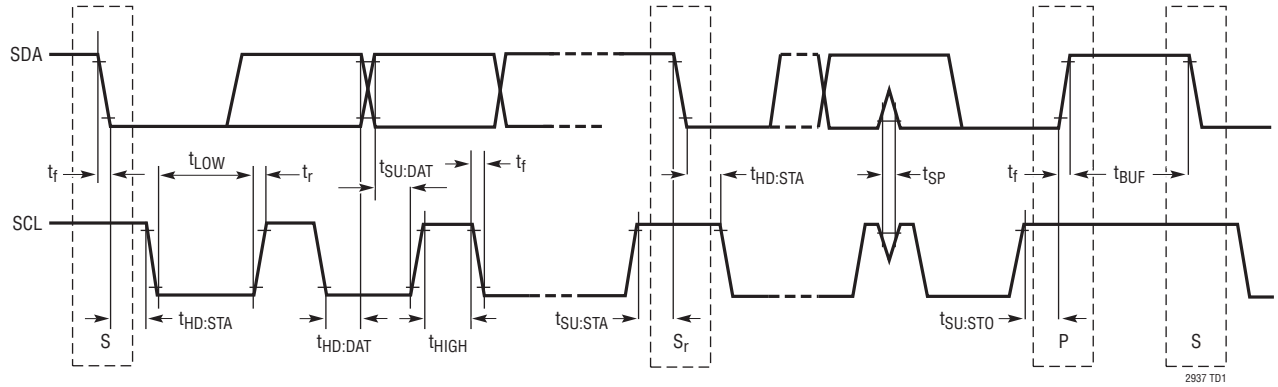
Note 7: EEPROM endurance and retention will be degraded when T_J > 85°C.

Note 8: The LTC2937 will not acknowledge any commands while a STORE command is being executed.

Note 9: If multiple LTC2937s are in use, t_{ONSQ} can stretch indefinitely until all devices are ready to sequence.

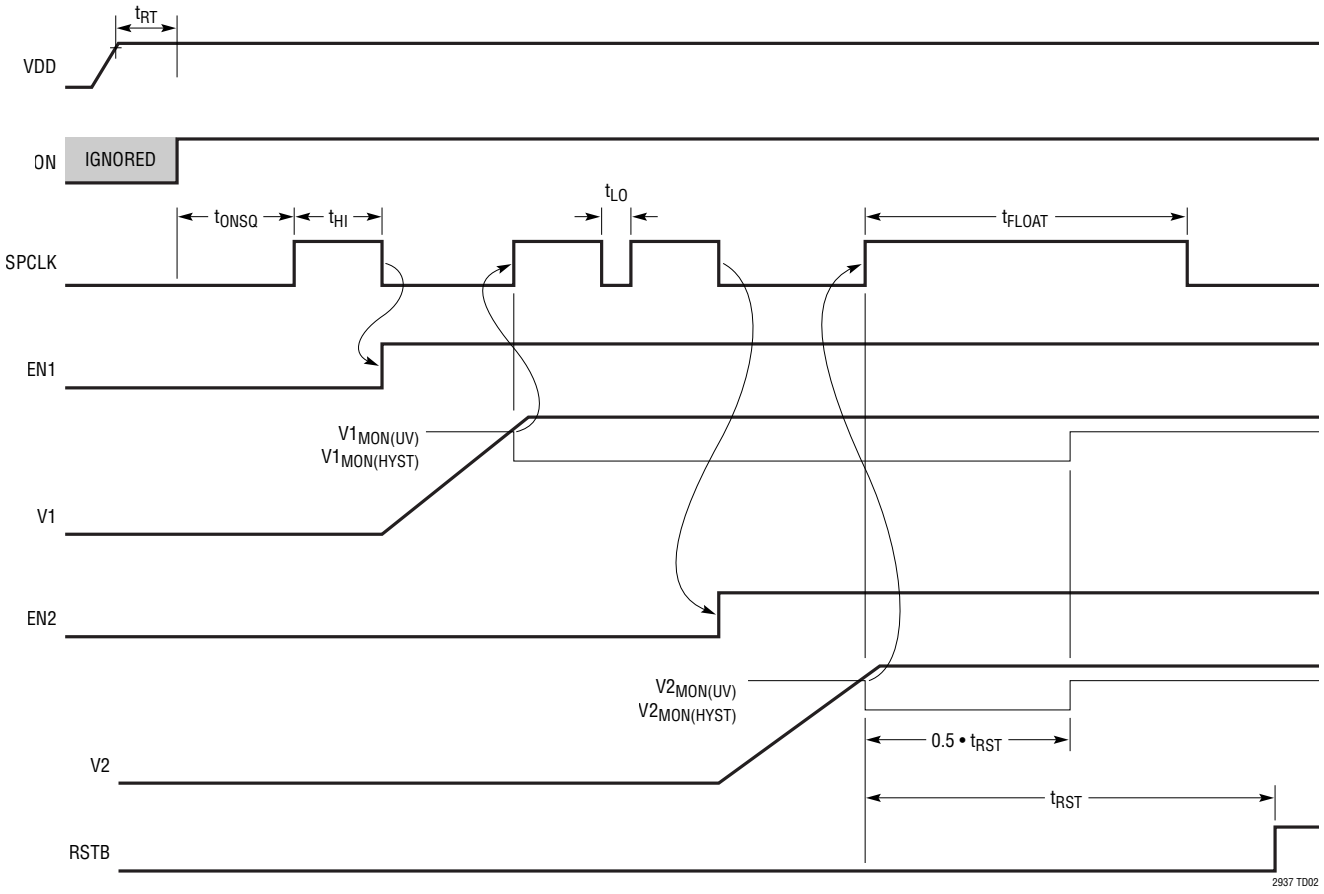
Note 10: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: (20 + 0.1 • C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 2.9V < V_{IO} < 5.5V.

SERIAL BUS TIMING DIAGRAM



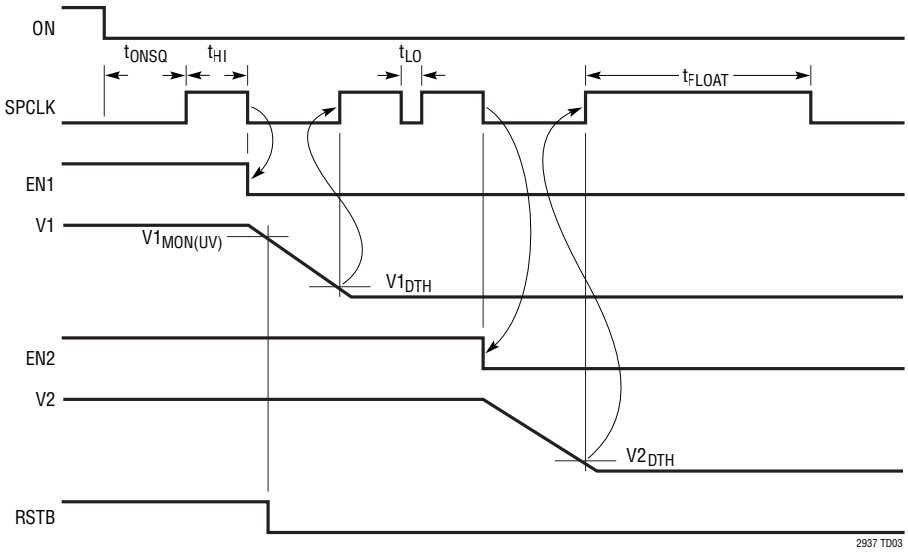
SEQUENCE-UP THRESHOLD TIMING DIAGRAM

Sequencing 2 Channels (V1, V2), Both Combined into RSTB Logic



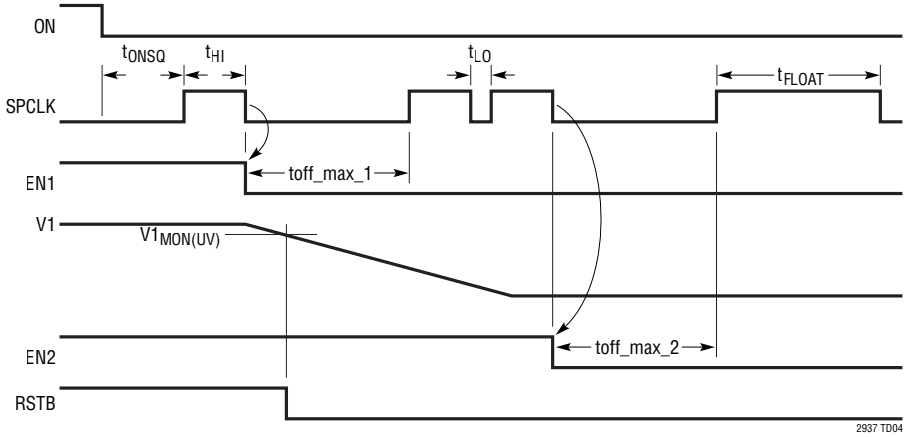
SEQUENCE-DOWN EVENT BASED TIMING DIAGRAM

Sequencing 2 Channels (V1, V2), Both Combined into RSTB Logic



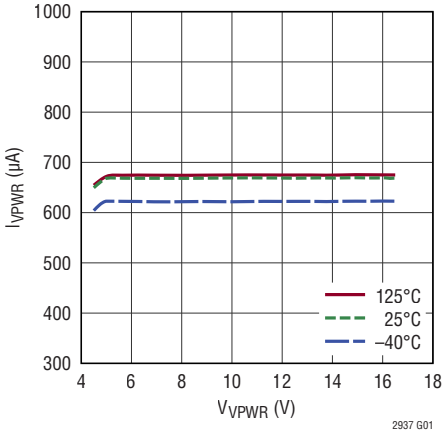
SEQUENCE-DOWN TIME BASED TIMING DIAGRAM

Sequencing 2 Channels (V1, V2), Both Combined into RSTB Logic. toff_max Timers Used for Post Disable Sequencing Delay; ON_OFF_CONTROL b[0] = 1

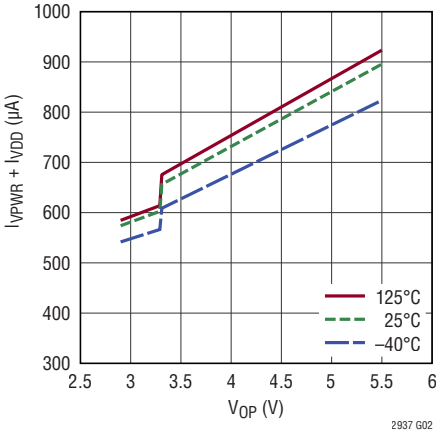


TYPICAL PERFORMANCE CHARACTERISTICS

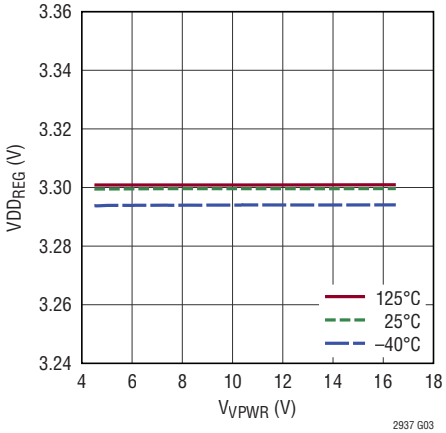
VPWR Input Current (Regulated VDD)



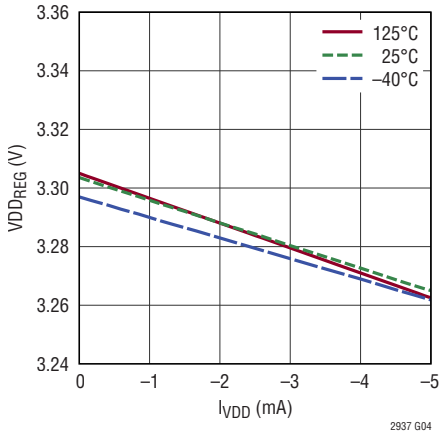
Input Current (VDD tied to VPWR)



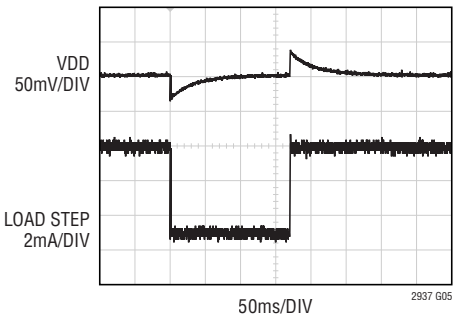
VDD Line Regulation



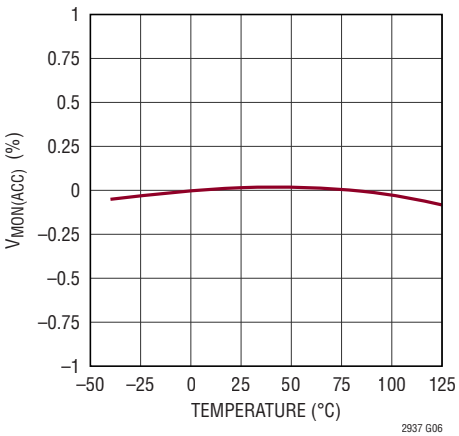
VDD Load Regulation



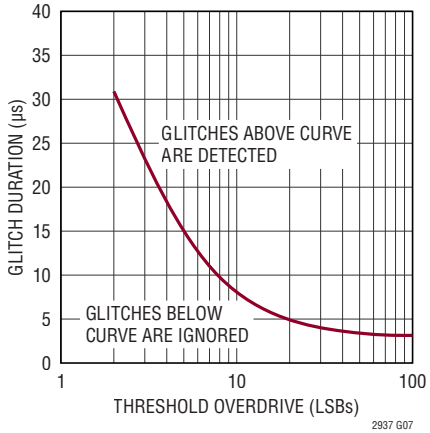
VDD Load Step Transient Response



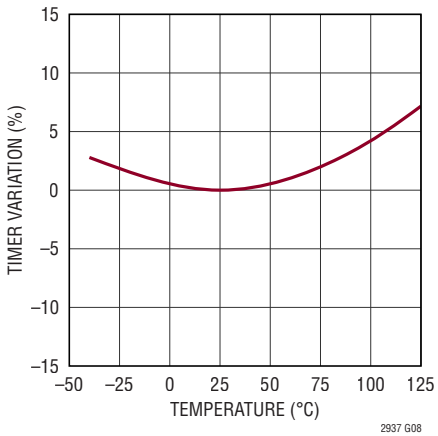
Comparator Threshold Accuracy vs Temperature



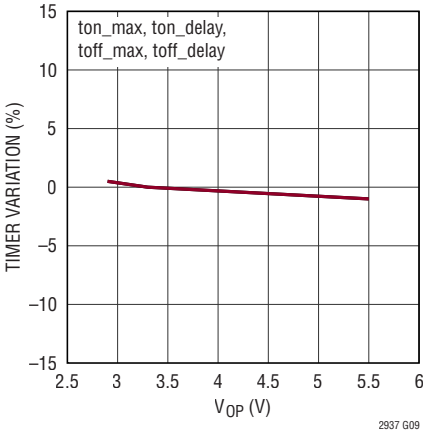
Comparator Glitch Immunity



Timer Variation vs Temperature

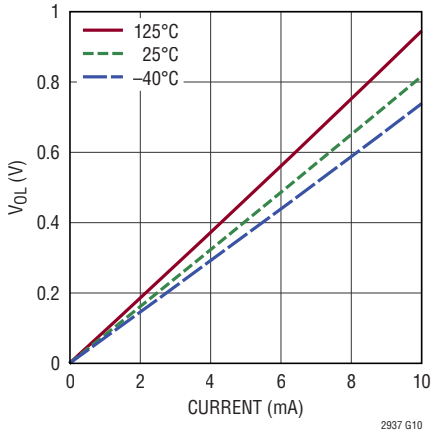


Timer Line Regulation

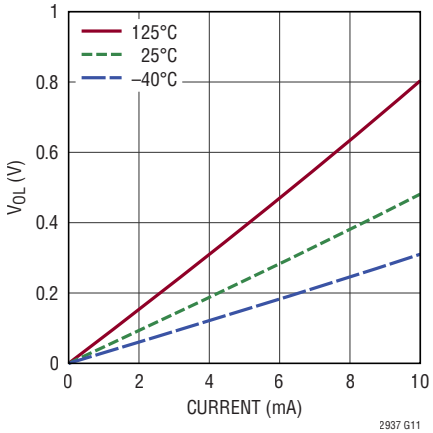


TYPICAL PERFORMANCE CHARACTERISTICS

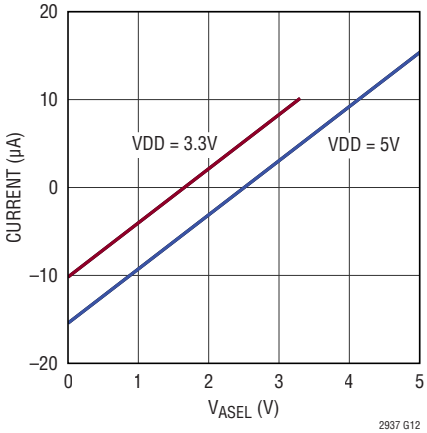
V_{OL} vs Output Sink Current RSTB, FAULTB, ALERTB



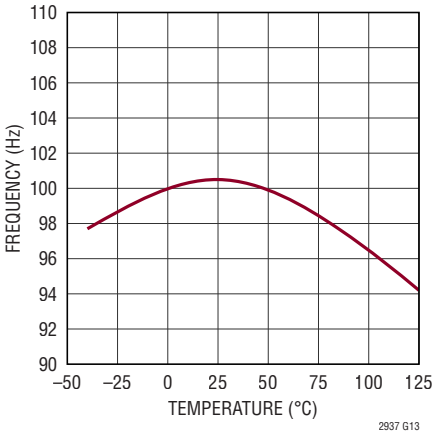
EN*n* V_{OL} vs Output Sink Current



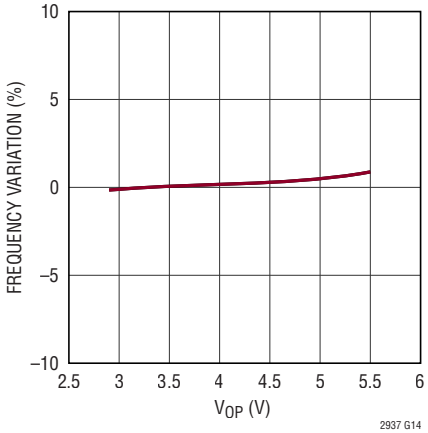
ASEL*n* Current vs Input Voltage



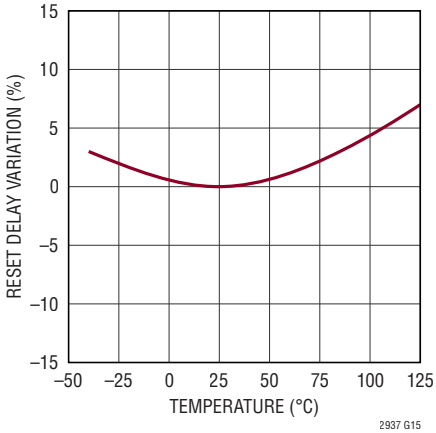
SHARE_CLK Frequency vs Temperature



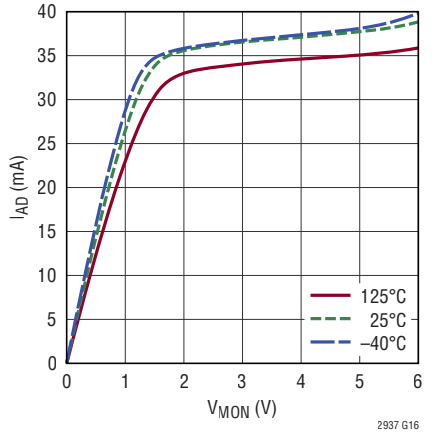
SHARE_CLK Frequency Line Regulation



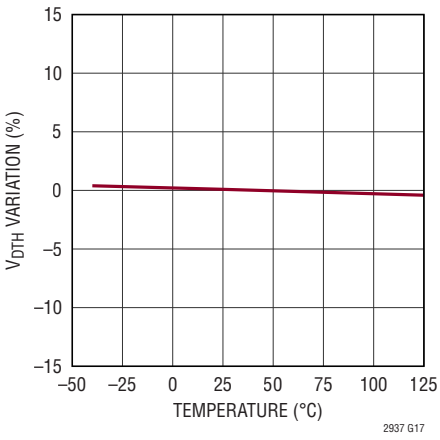
Reset Delay Variation vs Temperature



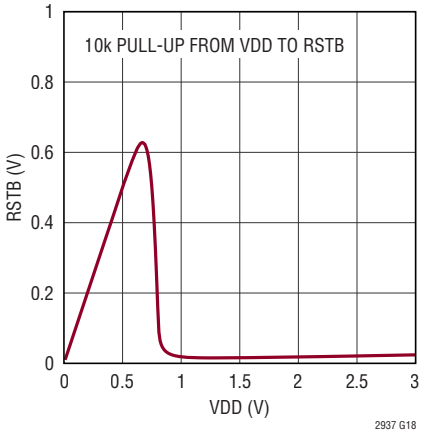
Active Discharge Current vs Monitor Input Voltage



Discharge Threshold Variation vs Temperature



RSTB (Low) vs VDD



PIN FUNCTIONS

ALERTB: Alert Open-Drain Output with 10µA Pull-Up to VDD. Asserts low in response to any designated fault. Conforms to SMBus standard. Apply the Alert Response Protocol to clear the ALERTB output and to identify the alerting device. Performing a read from the CLEAR_ALERTB register will also remove ALERTB pull-down.

ASEL1, ASEL2, ASEL3: Three-State Address-Select Inputs. Connect to GND, VDD or open to encode 1 of 27 device addresses. Consult the Operation section for the address look-up table.

EN1, EN2, EN3, EN4, EN5, EN6: Power Supply Enable Outputs. Connect these open-drain outputs to a respective power supply enable input or to a gate of an N-channel MOSFET (for pass applications). The enable outputs must be pulled up externally (to a maximum of 15V) if necessary. Some power supply enable inputs have internal pull-up sources, which eliminates the need for an external pull-up.

Exposed Pad: Leave open or connect to device GND.

FAULTB: Fault I/O with 10µA Pull-Up to VDD. Asserts low in response to any designated fault. Configure fault behavior in the FAULT_RESPONSE register. External devices may also pull down on FAULTB to initiate an optional fault response.

GND: Device Ground.

MARGB: Margin Input. Pull to ground to disable RSTB and prevent SUPERVISOR faults. Typically applied prior to margining supplies high or low during system test. Leave open or pull to VDD when not margining.

ON: Sequencing Up/Down Control Input. ON input response is gated by settings in the ON_OFF_CONTROL register. Internally pulled up to VDD with 10µA current source.

RSTB: Reset I/O with 10µA Pull-Up to VDD. Pulls low in response to designated voltage comparator violations. Pulls high when selected voltage sense thresholds are satisfied (ie not UV and/or not OV), and can be used as a system power-on-reset. The reset assertion delay after satisfying thresholds is programmable. May be pulled low by external devices and detected with b[12] of the MONITOR_STATUS command.

SCL: Serial Clock Input (400kHz Maximum). Requires external pull-up resistor.

SDA: Bidirectional Serial Data I/O. Requires external pull-up resistor.

SHARE_CLK: Clock Sharing Node. Connect multiple SHARE_CLK nodes together to establish a common time base between devices. Pull-up with a 3.3k to 10k resistor to VDD.

SPCLK: Sequence Position Clock I/O. Connect multiple LTC2937 SPCLK lines together for automatic sequence position control between devices. Pull-up devices are not recommended. Leave unconnected in a single device application. Minimize capacitance on this line to ensure reliable operation.

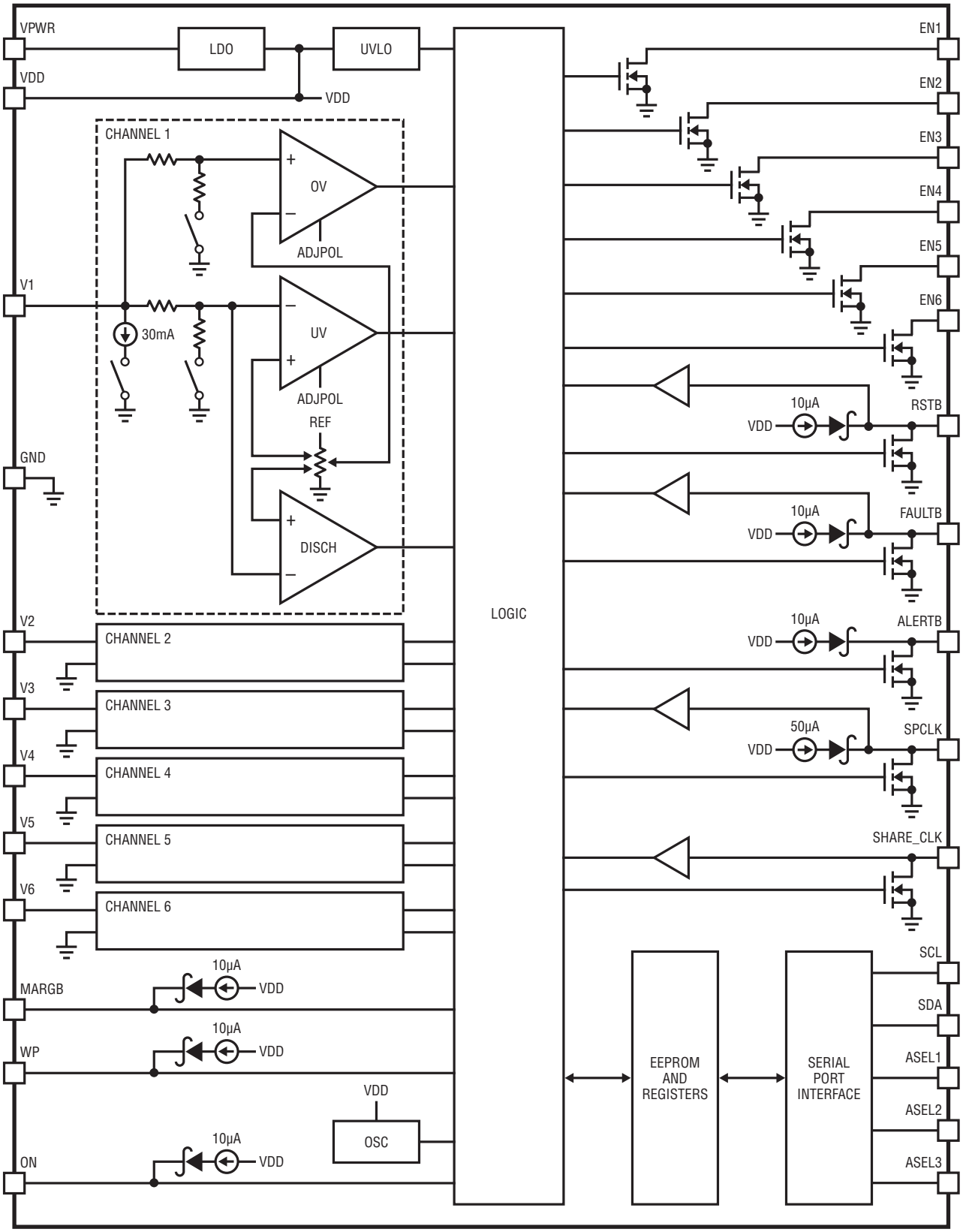
V1, V2, V3, V4, V5, V6: Undervoltage, Overvoltage and Discharge Comparator Inputs. There are three sense ranges. Adjustable: 0.2V to 1.2V in 4mV increments, Low: 0.5V to 3V in 10mV increments, and High: 1V to 6V in 20mV increments. When monitored supplies are shut off, internal pull-down current sources can be activated to accelerate the discharge of supply capacitance. Connect to device GND if unused.

VDD: 3.3V Internal Regulator Output. Bypass with a 2.2µF (or greater) capacitor to GND. Use this output to bias the address inputs or an external resistor network for sensing negative supply voltages. Do not load the regulated output with more than 5mA. Override the regulated output with an external supply (2.9V to 5.5V) connected to VPWR and VDD.

VPWR: Supply Voltage Input. Power supply operating range is 4.5V to 16.5V. Tie to VDD if unused. Bypass with 0.1µF (or greater) capacitor to GND.

WP: Write Protection Input. Pull to GND to enable write capability into the device. Leave open or tie to VDD to keep write protection active. The software controlled lock bit in the WRITE_PROTECTION register may also need deactivation to enable write capability.

BLOCK DIAGRAM



OPERATION

The LTC2937 is a six-channel programmable power supply sequencer and supervisor that can perform the following operations:

- Control the timing relationships and sequence order for six power supplies per device. Sequence supplies on the basis of time delays and/or qualifying events.
- Monitor power supplies for undervoltage (UV) and overvoltage (OV) conditions using two independent comparators on each of six inputs.
- Generate a system reset that is a function of user selected inputs with a programmable release delay.
- Synchronize sequencing across multiple controllers with a one wire connection (SPCLK).
- Synchronize timing across multiple controllers with a one wire connection (SHARE_CLK).
- Discharge slowly decaying supplies with built-in pull-down current sources.
- Monitor power supplies for discharge condition using the discharge comparators.
- Accept I^2C/SMBus programming commands.
- Initiate supply sequencing from an external source and/or programming command.
- Retrieve real-time system status.
- Generate a fault related interrupt on the ALERTB output and respond to an issued SMBus Alert Response.
- Respond to fault conditions by continuing operation indefinitely or disabling supplies immediately. Optionally, sequencing may be retried multiple times automatically (0 to 6 or unlimited) after a supply shutdown event.
- Report voltage and/or timing limit violations upon request.
- Pause sequencing operations to help identify system power problems.
- Store system configuration to EEPROM.
- Restore EEPROM contents to operating memory through programming or when VDD is applied on power-up.
- Recall first fault violations logged to EEPROM.
- EEPROM reads and writes over the entire specified supply voltage and temperature range.
- Provide two stage write protection to prevent inadvertent writes to memory.
- Disable system reset when performing voltage margining of supplies.
- Monitor negative power supplies.

OPERATION

Slave Addresses

The LTC2937 responds to one of 27 addresses. Connect the ASEL1, ASEL2 and ASEL3 inputs to VDD, GND, or leave open, as shown in Table 1. The LTC2937 always responds to the Global and Alert Response addresses regardless of the ASEL input states. The ASEL inputs are always active and operate in real time.

Table 1. LTC2937 Address Look-Up Table

DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS								ADDRESS INPUTS		
	7-Bit	8-Bit	6	5	4	3	2	1	0	R/W	ASEL3	ASEL2	ASEL1
Alert Response	0C	19	0	0	0	1	1	0	0	1	X	X	X
Global	36	6C	0	1	1	0	1	1	0	0	X	X	X
	37	6E	0	1	1	0	1	1	1	X	L	L	L
	38	70	0	1	1	1	0	0	0	X	L	L	NC
	39	72	0	1	1	1	0	0	1	X	L	L	H
	3A	74	0	1	1	1	0	1	0	X	L	NC	L
	3B	76	0	1	1	1	0	1	1	X	L	NC	NC
	3C	78	0	1	1	1	1	0	0	X	L	NC	H
	3D	7A	0	1	1	1	1	0	1	X	L	H	L
	3E	7C	0	1	1	1	1	1	0	X	L	H	NC
	3F	7E	0	1	1	1	1	1	1	X	L	H	H
	40	80	1	0	0	0	0	0	0	X	NC	L	L
	41	82	1	0	0	0	0	0	1	X	NC	L	NC
	42	84	1	0	0	0	0	1	0	X	NC	L	H
	43	86	1	0	0	0	0	1	1	X	NC	NC	L
	44	88	1	0	0	0	1	0	0	X	NC	NC	NC
	45	8A	1	0	0	0	1	0	1	X	NC	NC	H
	46	8C	1	0	0	0	1	1	0	X	NC	H	L
	47	8E	1	0	0	0	1	1	1	X	NC	H	NC
	48	90	1	0	0	1	0	0	0	X	NC	H	H
	49	92	1	0	0	1	0	0	1	X	H	L	L
	4A	94	1	0	0	1	0	1	0	X	H	L	NC
	4B	96	1	0	0	1	0	1	1	X	H	L	H
	4C	98	1	0	0	1	1	0	0	X	H	NC	L
	4D	9A	1	0	0	1	1	0	1	X	H	NC	NC
	4E	9C	1	0	0	1	1	1	0	X	H	NC	H
	4F	9E	1	0	0	1	1	1	1	X	H	H	L
	50	A0	1	0	1	0	0	0	0	X	H	H	NC
	51	A2	1	0	1	0	0	0	1	X	H	H	H

H = Tie to VDD, L = Tie to GND, NC = No Connect = Open, X = Don't Care

OPERATION

I²C Interface

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
x	SHOWN UNDER A FIELD INDICATES THAT THAT FIELD IS REQUIRED TO HAVE THE VALUE OF x
A	ACKNOWLEDGE
$\overline{A}$	NOT ACKNOWLEDGE
P	STOP CONDITION
☐	MASTER TO SLAVE
▒	SLAVE TO MASTER

2937 F01

Figure 1. Serial Bus Protocol Diagram Element Key

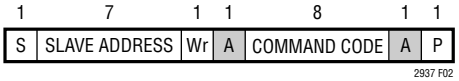


Figure 2. Send Byte Protocol

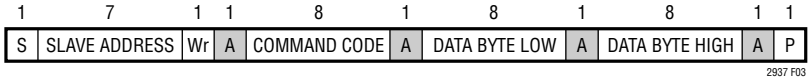


Figure 3. Write Word Protocol

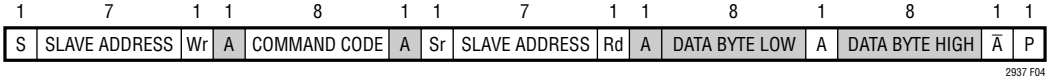


Figure 4. Read Word Protocol

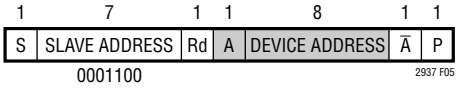


Figure 5. Alert Response Protocol

CONDENSED COMMAND SUMMARY

ON/OFF Commands

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE (Note 11)	WORD LENGTH (BITS)	EEPROM CAPACITY (BITS)	REF PAGE
ON_OFF_CONTROL	0x02	ON input and/or I^2C directed sequence up/down control settings.	R/W	16	16	19
Sequencing-Up Configuration Commands						
SEQ_UP_POSITION_*n*	0x16 – 0x1B	Sequence-up position for EN1 through EN6. Asynchronous enable controls.	R/W	16	16	24
TON_TIMERS_*n*	0x0A – 0x0F	Encode EN*n* delay time and maximum rise time for V*n*.	R/W	16	16	22
Voltage Supervisor Commands						
V_RANGE	0x03	Encode V*n* comparator ranges and Adjustable Range polarity.	R/W	16	16	20
V_THRESHOLD_*n*	0x04 – 0x09	Encode high and low thresholds for V*n*.	R/W	16	16	21
RSTB_CONFIG	0x22	Select comparator outputs for combination into RSTB response. Select RSTB assertion delay.	R/W	16	16	26
Sequencing-Down Configuration Commands						
SEQ_DOWN_POSITION_*n*	0x1C – 0x21	Sequence-down position for EN1 through EN6. Active discharge select for V1 through V6.	R/W	16	16	25
TOFF_TIMERS_*n*	0x10 – 0x15	Encode EN*n* delay time and maximum fall time for V*n*.	R/W	16	16	23
Fault, Status and Debugging Commands						
FAULT_RESPONSE	0x23	Configure fault response actions.	R/W	16	16	27
STATUS_INFORMATION	0x29	Summary of current device faults and status.	R	16	0	31
MONITOR_STATUS_ HISTORY	0x26	History of voltage monitor violations, SUPERVISOR faults and SEQUENCE faults.	R	16	0	29
MONITOR_BACKUP	0x2F	An EEPROM copy of the MONITOR_STATUS_HISTORY word after the first SUPERVISOR or SEQUENCE fault.	R	16	16	33
MONITOR_STATUS	0x30	Live voltage monitor and RSTB status.	R	16	0	34
SEQ_POSITION_COUNT	0x2B	Sequence position counter.	R	16	0	32
BREAK_POINT	0x2A	Enable and configure sequencing break points.	R/W	16	0	32
CLEAR	0x2E	Clear all status, fault and volatile history information.	S	0	0	30
CLEAR_ALERTB	0x28	Clear the ALERTB output by performing a read from this command address. The returned word contains no information.	R	16	0	30
Security and Device Information Commands						
WRITE_PROTECTION	0x00	Contains lock key code and software lock bit to prevent accidental overwrites of volatile and nonvolatile memory. Status of WP input.	R/W	16	16	18
STORE	0x2C	Store device configuration to EEPROM.	S	0	0	30
RESTORE	0x2D	Restore device configuration from EEPROM.	S	0	0	30
SPECIAL_LOT	0x01	Contains customer specific codes that identify the factory programmed configuration stored in EEPROM. Use as a scratchpad if customer codes are not applied.	R/W	16	16	18
DEVICE_ID	0x31	Read only. Contains 0x2937.	R	16	0	34

Note 11: R = read, W = write, S = send byte.

COMMAND DESCRIPTIONS

WRITE_PROTECTION
(Command Byte 0x00)

Prevent write operations into EEPROM or volatile memory with the software lock bit b[0] = 1 and/or hardware lock bit b[1] = 1. Deactivate the software lock bit by matching the device key string in b[15:2] while b[1:0] = 00b. Retrieve the state of the external hardware lock input (WP) in b[1]. Improve write security by having at least one bit in the device key set to logic 1. Change the device key if desired, when the device is unlocked.

The contents of any supported command may be read regardless of the lock bit settings. Commands are acknowledged under write protection. However, the device configuration will not change.

WRITE_PROTECTION Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:2]	device_key	Must match against programmed string in order to deactivate software write lock (default = 0x0EAA).
b[1]	hw_lock_bit	WP input status. 0: Unlocked. 1: Locked.
b[0]	sw_lock_bit	Software lock bit. 0: Unlocked. 1: Locked (default).

SPECIAL_LOT
(Command Byte 0x01)

Read the SPECIAL_LOT register to retrieve a customer specific code that identifies the factory programmed configuration stored in EEPROM. Use as a scratchpad if customer codes are not applied. Contact LTC Marketing to request a custom factory programmed configuration and special lot number. The default value is 0x0000.

COMMAND DESCRIPTIONS

ON_OFF_CONTROL
(Command Byte 0x02)

Configure the combination of ON input and/or I^2C inputs needed to control sequencing. Activate margin mode operation using b[6] or the external MARGB input. Specify time or event based sequence-down qualification. Prevent sequence-up initiation if supplies selected for sequencing are not discharged.

ON_OFF_CONTROL Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:8]	reserved	Ignore.
b[7]	on_state	Internal ON status. Representation of the ON input logically modified by the b[5:1] directives below and/or freeze mode bit b[8] from FAULT_RESPONSE (read only). 0: Internal ON is low. 1: Internal ON is high.
b[6]	i2c_margin	RSTB disable used during supply margining. 0: RSTB operates normally (default). 1: RSTB is allowed to pull high.
b[5]	discharge_start	Sequenced supply discharge threshold qualification. 0: Discharged supplies not required to start sequence-up (default). 1: Discharged supplies required to start sequence-up.
b[4]	i2c_on_off	Serial bus directed sequence on/off control. 0: Sequence down (default). 1: Sequence up.
b[3]	i2c_on_off_mask	Serial bus on/off control mask. 0: Ignore b[4]. If b[3] and b[2] are low, device is in sequence down state (default). 1: Listen to b[4]. If b[2] is high, the ON input is also required to initiate sequencing.
b[2]	on_input_mask	ON input mask. 0: Ignore the ON input. Sequencing control directed by b[4] if not masked (default). 1: Listen to ON input.
b[1]	on_polarity	Invert ON input logical state. Changing polarity should be performed with b[2] low because the response is immediate and could initiate a sequencing event. 0: Sequence up with ON input at logic high (default). 1: Sequence up with ON input at logic low.
b[0]	seq_down_qual	Select time or event based sequence down. 0: Event based. Sequence position clock (SPCLK) advances when supplies drop below their discharge threshold (default). 1: Time based. Sequence position clock (SPCLK) advances when respective toff_max time has elapsed, including any preceding toff_delay time (if timer set to infinity, operation defaults to voltage decay mode).

COMMAND DESCRIPTIONS

V_RANGE
(Command Byte 0x03)

Select the operating threshold range for each of the six voltage monitor inputs. The range selection applies to the OV and UV comparators connected to each input. The High Range covers thresholds between 1V and 6V in 20mV steps. The Low Range covers thresholds between 0.5V and 3V in 10mV steps. The Adjustable Range covers 0.2V to 1.2V in 4mV steps. Select the negative polarity option in the Adjustable Range when sensing negative voltages. Discharge comparator threshold and polarity adjusts automatically in response to the configured range selection.

V_RANGE Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:12]	reserved	Ignore.
b[11:10]	v6_range	Select V6 range. 00b: High Range (default). 01b: Low Range. 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).
b[9:8]	v5_range	Select V5 range. 00b: High Range (default). 01b: Low Range. 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).
b[7:6]	v4_range	Select V4 range. 00b: High Range. 01b: Low Range (default). 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).
b[5:4]	v3_range	Select V3 range. 00b: High Range. 01b: Low Range (default). 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).
b[3:2]	v2_range	Select V2 range. 00b: High Range. 01b: Low Range (default). 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).
b[1:0]	v1_range	Select V1 range. 00b: High Range. 01b: Low Range (default). 10b: Adjustable Range (positive polarity). 11b: Adjustable Range (negative polarity).

COMMAND DESCRIPTIONS (Note 3)

V_THRESHOLD_n

n	1	2	3	4	5	6
Command Byte	0x04	0x05	0x06	0x07	0x08	0x09

Program the OV and UV thresholds for each of the six voltage monitor inputs.

V_THRESHOLD_*n* Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:8]	ov_threshold_*n*	Encode one of 250 thresholds (0x05 through 0xFF). See below for voltage threshold encoding (TE) procedure.
b[7:0]	uv_threshold_*n*	Encode one of 250 thresholds (0x05 through 0xFF). See below for voltage threshold encoding (TE) procedure.

Voltage Threshold Encoding

Depending on the selected voltage range, threshold encoding (TE) is determined as follows:

For the high input range of 1V to 6V, the equation is:

$$TE = ROUND[50 \bullet (V_{MON} - 0.9)]$$

For the low input range of 0.5V to 3V, the equation is:

$$TE = ROUND[100 \bullet (V_{MON} - 0.45)]$$

For the high impedance adjustable input range of 0.2V to 1.2V, the equation is:

$$TE = ROUND[250 \bullet (V_{MON} - 0.18)]$$

As an example, consider the channel 1 Low Range defaults from the table below (ov_threshold_1 = 1.32V, uv_threshold_1 = 1.08V). The threshold encodings (TE) are therefore:

$$TE_{OV} = ROUND[100 \bullet (1.32 - 0.45)] = ROUND[100 \bullet (0.87)] = 87\ (0x57)$$

$$TE_{UV} = ROUND[100 \bullet (1.08 - 0.45)] = ROUND[100 \bullet (0.63)] = 63\ (0x3F)$$

The16-bit word contained in the V_THRESHOLD_1 register (0x573F) is formed from the simple concatenation of the OV and UV hexadecimal values.

Factory Defaults

n	RANGE	$V_{MON(OV)}$	$V_{MON(UV)}$	TE_{OV}	TE_{UV}
1	Low	1.32 V	1.08 V	0x57	0x3F
2	Low	1.65 V	1.35 V	0x78	0x5A
3	Low	1.98 V	1.62 V	0x99	0x75
4	Low	2.75 V	2.25 V	0xE6	0xB4
5	High	3.63 V	2.97 V	0x89	0x68
6	High	5.5 V	4.5V	0xE6	0xB4

COMMAND DESCRIPTIONS (Note 3)

TON_TIMERS_n

n	1	2	3	4	5	6
Command Byte	0x0A	0x0B	0x0C	0x0D	0x0E	0x0F

The TON_TIMER registers encode the enable delay time and the maximum allowable rise time per channel in one 16-bit word. The lowest thirteen bits (*ton_delay*) determine the amount time delay between the beginning of the programmed sequence position (determined by the SEQ_UP_POSITION_*n* command) and the release of the respective EN*n* output (in 80µs increments).

The upper three bits (*ton_max*) determine the amount of time that is allowed to elapse between the release of EN*n* and the voltage at the respective V*n* input reaching its UV threshold. Failing this test can cause a sequence-up fault depending on the FAULT_RESPONSE settings. A setting of ∞ defeats time checking during the sequence-up phase for the respective channel (sequencing will pause indefinitely until the UV threshold is crossed).

TON_TIMERS_*n* Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:13]	ton_max_*n*	Maximum rise time selection. Defined as the maximum time allowed between EN*n* release and successful crossing of UV threshold at the V*n* input.
b[12:0]	ton_delay_*n*	Time delay from start of selected sequence position to enable (EN*n*) release. ton_delay = 80 • N µs, where N is a 13-bit unsigned integer in b[12:0]. Delay range is from 0ms to 655ms. The default setting for b[12:0] = 0.

b[15:13]	ton_max
000b	∞ (default)
001b	160µs
010b	640µs
011b	2.6ms
100b	10.2ms
101b	41ms
110b	164ms
111b	655ms

COMMAND DESCRIPTIONS (Note 3)

TOFF_TIMERS_n

n	1	2	3	4	5	6
Command Byte	0x10	0x11	0x12	0x13	0x14	0x15

The TOFF_TIMER registers encode the disable delay time and the maximum allowable fall time per channel in one 16-bit word. The lowest thirteen bits (*toff_delay*) determine the amount time delay between the beginning of the programmed sequence position (determined by the SEQ_DOWN_POSITION_*n* command) and the pull-down of the respective EN*n* output (in 80µs increments).

The upper three bits (*toff_max*) determine the amount of time that is allowed to elapse between the pull-down of EN*n* and the voltage at the respective V*n* input falling below its discharge threshold. Failing this test can cause a sequence-down fault depending on the FAULT_RESPONSE settings. A setting of ∞ defeats time checking during the sequence-down phase for the respective channel (sequencing will pause indefinitely until the monitored voltage decays below its discharge threshold).

Sequence-down progress may also be gated by time instead of voltage decay. Choose the time based mode of operation with b[0] = 1 in the ON_OFF_CONTROL register. Use the *toff_max* settings below to set the time from EN*n* pulling low to the start of next sequence position. If multiple channels occupy the same sequence position, the longest combined time (*toff_delay_n* + *toff_max_n*) determines the sequence position hold time. In time delay mode, a *toff_max* setting of ∞ defaults operation to voltage decay mode.

TOFF_TIMERS_*n* Data Contents

<table>
<tr><th>BIT(S)</th><th>SYMBOL</th><th>OPERATION</th></tr>
<tr><td>b[15:13]</td><td>toff_max_n</td><td>Maximum fall time selection. Defined as the maximum time allowed between ENn pull-down and successful crossing of the discharge threshold at the Vn input.
<table>
<tr><th>b[15:13]</th><th>toff_max</th></tr>
<tr><td>000b</td><td>∞ (default)</td></tr>
<tr><td>001b</td><td>2.6ms</td></tr>
<tr><td>010b</td><td>10.2ms</td></tr>
<tr><td>011b</td><td>41ms</td></tr>
<tr><td>100b</td><td>164ms</td></tr>
<tr><td>101b</td><td>655ms</td></tr>
<tr><td>110b</td><td>2.6s</td></tr>
<tr><td>111b</td><td>10.5s</td></tr>
</table></td></tr>
<tr><td>b[12:0]</td><td>toff_delay_n</td><td>Time delay from start of selected sequence position to enable (ENn) pull-down.
toff_delay = 80 • N µs, where N is the 13-bit unsigned integer in b[12:0].
The default setting for b[12:0] = 0.</td></tr>
</table>

COMMAND DESCRIPTIONS (Note 3)

SEQ_UP_POSITION_n

n	1	2	3	4	5	6
Command Byte	0x16	0x17	0x18	0x19	0x1A	0x1B

Program the sequence position in which the respective enable output is allowed to pull high. Select from 1023 positions (1 through 1023) controlled by the sequence position clock (SPCLK) connected to all LTC2937s. Sequence-up positions may be different from the respective sequence-down positions. Any and all enable outputs may operate in any sequence position. If b[9:0] are set equal to 0, the respective channel is not participating and is ignored during sequencing up and down. A setting of zero enables the asynchronous on/off bit providing immediate enable output response. If the asynchronous on/off bit is in use, the respective channel does not participate in sequencing events but the respective UV/OV monitor conditions may be included in the RSTB response. Unused sequence positions add an 80µs space (t_{HI} + t_{LO}) between configured sequence positions. SPCLK self terminates after the last used sequence position.

SEQ_UP_POSITION_*n* Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:11]	reserved	Ignore.
b[10]	async_on_off_*n*	Asynchronous enable control. Release or pull-down the respective enable output immediately provided that b[9:0] = 0. 0: Pull down EN*n* immediately (default). 1: Release EN*n* immediately.
b[9:0]	seq_up_position_*n*	Specify a sequence-up position from 1 to 1023. If b[9:0] = 0, the channel does not participate in sequencing operations. Default b[9:0] = 0x001 (position 1).

COMMAND DESCRIPTIONS (Note 3)

SEQ_DOWN_POSITION_n

n	1	2	3	4	5	6
Command Byte	0x1C	0x1D	0x1E	0x1F	0x20	0x21

Program the sequence position in which the respective enable output is pulled down. Select from 1023 positions (1 through 1023) controlled by the sequence position clock (SPCLK) connected to all LTC2937s. Sequence-down positions may be different from the respective sequence-up positions. Any and all enable outputs may operate in any sequence position. If b[9:0] are set equal to 0, the respective channel is not participating and is ignored during sequencing down and up. Selectively configure V*n* inputs to receive current source pull-down when respective enable outputs are low. The active pull-down can be used to reduce power supply discharge time. Unused sequence positions add an 80µs space ($t_{HI} + t_{LO}$) between configured sequence positions. SPCLK self terminates after the last used sequence position.

SEQ_DOWN_POSITION_*n* Data Contents

BIT(S)	SYMBOL	OPERATION
b[15:11]	reserved	Ignore.
b[10]	active_pull_down_*n*	Apply pull-down current source to respective V*n* inputs to reduce power supply discharge time. If enabled, the source is active when the respective EN*n* output is low. 0: Active pull-down disabled (default). 1: Active pull-down enabled.
b[9:0]	seq_down_position_*n*	Specify a sequence-down position from 1 to 1023. If b[9:0] = 0, the channel does not participate in sequencing operations. Default b[9:0] = 0x001 (position 1).