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## FEATURES

- **Less Than ±0.5% Total Unadjusted Error 14-Bit  $\Delta\Sigma$  ADC with On-Chip Reference**
- **Dual, 8-Bit IDACs with 1x Voltage Buffers**
- **Linear, Voltage Servo Adjusts Supply Voltages by Ramping IDAC Outputs Up/Down**
- I<sup>2</sup>C Bus Interface (SMBus Compatible)
- Extensive, User Configurable Fault Monitoring
- On-Chip Temperature Sensor
- Available in 24-Pin 4mm × 5mm QFN Package

## APPLICATIONS

- Dual Power Supply Voltage Servo
- Monitoring Supply Voltage and Current
- Programmable Power Supplies
- Programmable Reference

## DESCRIPTION

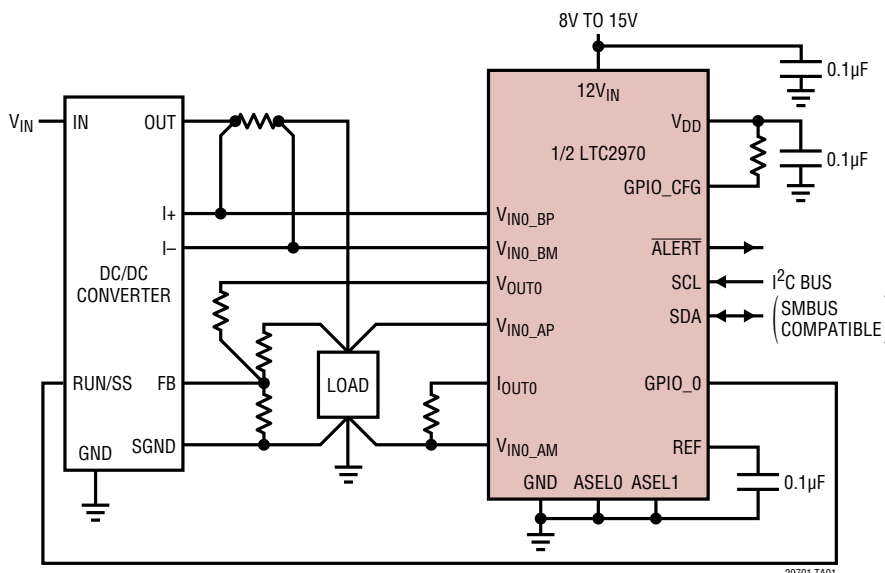
The **LTC<sup>®</sup>2970** is a dual power supply monitor and margining controller with an SMBus compatible I<sup>2</sup>C bus interface. A low-drift, on-chip reference and 14-bit  $\Delta\Sigma$  A/D converter allow precise measurements of supply voltages, load currents or internal die temperature. Fault management allows **ALERT** to be asserted for configurable overvoltage and undervoltage fault conditions. Two voltage buffered, 8-bit IDACs allow highly accurate programming of DC/DC converter output voltages. The IDACs can be configured to automatically servo the power supplies to the desired voltages using the ADC. The LTC2970-1 adds a tracking feature that can be used to turn multiple power supplies on or off in a controlled manner.

The bus address is set to 1 of 9 possible combinations by pin strapping the **ASEL0** and **ASEL1** pins. The LTC2970/LTC2970-1 are packaged in a 24-pin, 4mm × 5mm QFN package.

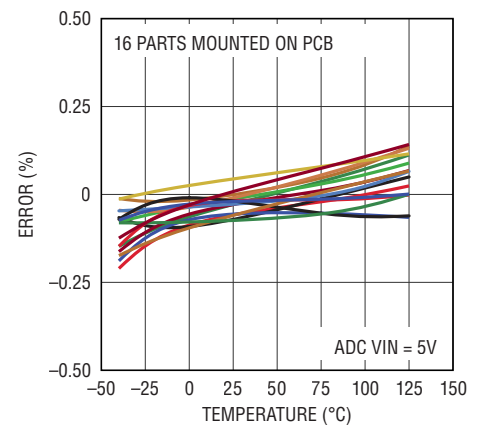
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## TYPICAL APPLICATION

**Dual Power Supply Monitor and Controller (One of Two Channels Shown)**



**ADC Total Unadjusted Error vs Temperature**



# LTC2970/LTC2970-1

## ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltages:

$V_{DD}$  ..... -0.3V to 6V  
 $12V_{IN}$  ..... -0.3V to 15V

Digital Input/Output Voltages:

ASELO, ASEL1 ..... -0.3V to  $V_{DD} + 0.3V$   
 SDA, SCL, GPIO\_CFG,  
 ALERT, GPIO\_0, GPIO\_1 ..... -0.3V to 6V

Analog Voltages:

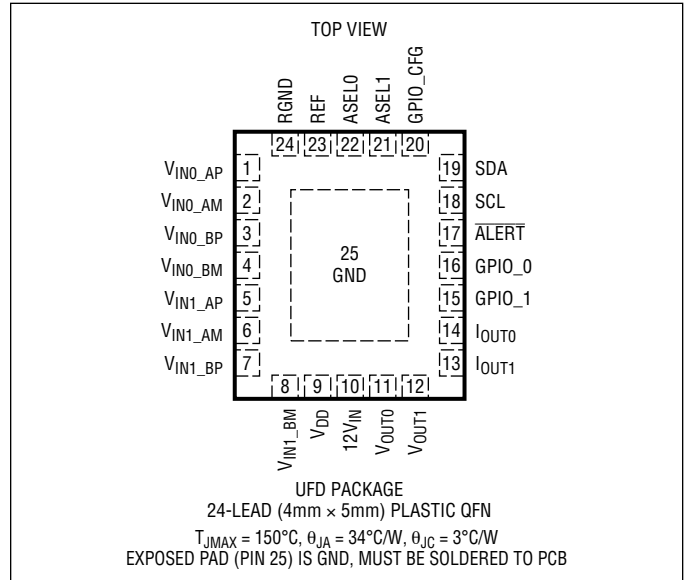
$V_{INO\_AP}$ ,  $V_{INO\_AM}$ ,  $V_{INO\_BP}$ ,  
 $V_{INO\_BM}$ ,  $V_{IN1\_AP}$ ,  $V_{IN1\_AM}$ ,  
 $V_{IN1\_BP}$ ,  $V_{IN1\_BM}$ ,  $V_{OUT0}$ ,  $V_{OUT1}$  ..... -0.3V to 6V  
 $I_{OUT0}$ ,  $I_{OUT1}$ , REF ..... -0.3V to  $V_{DD} + 0.3V$   
 RGND ..... -0.3V to 0.3V

Operating Ambient Temperature Range:

LTC2970C ..... 0°C to 70°C  
 LTC2970I ..... -40°C to 85°C  
 LTC2970H ..... -40°C to 125°C

Storage Temperature Range ..... -65°C to 150°C

## PIN CONFIGURATION



## ORDER INFORMATION <http://www.linear.com/product/LTC2970#orderinfo>

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2970CUFD#PBF	LTC2970CUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2970CUFD-1#PBF	LTC2970CUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	0°C to 70°C
LTC2970IUFD#PBF	LTC2970IUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	-40°C to 85°C
LTC2970IUFD-1#PBF	LTC2970IUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	-40°C to 85°C
LTC2970HUFD#PBF	LTC2970HUFD#TRPBF	2970	24-Pin (4mm × 5mm) Plastic QFN	-40°C to 125°C
LTC2970HUFD-1#PBF	LTC2970HUFD-1#TRPBF	29701	24-Pin (4mm × 5mm) Plastic QFN	-40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreeel/>. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{DD}$  and REF pins floating unless otherwise indicated,  $C_{VDD} = 100\text{nF}$  and  $C_{REF} = 100\text{nF}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Power-Supply Characteristics</b>							
$I_{V12}$	$12V_{IN}$ Supply Current	$V_{12VIN} = 12\text{V}$ , $V_{DD}$ Floating	●	4.24	7.5	mA	
$I_{DD}$	$V_{DD}$ Supply Current	$V_{DD} = 5\text{V}$ , $V_{12VIN} = V_{DD}$	●	3.7	5	mA	
$V_{LKO}$	$V_{DD}$ Undervoltage Lockout	$V_{DD}$ Ramping-Down, $V_{12VIN} = V_{DD}$	●	3.7	4.14	4.4	V
	$V_{DD}$ Undervoltage Lockout Hysteresis			118		mV	
$V_{DD}$	Supply Input Operating Range		●	4.5	5.75	V	
	Regulator Output Voltage	$8\text{V} \leq V_{12VIN} \leq 15\text{V}$ , $-1\text{mA} \leq I_{VDD} \leq 0$	●	4.75	4.95	5.25	V
	Regulator Output Voltage Temperature Coefficient			10		ppm/ $^\circ\text{C}$	
	Regulator Output Voltage Load Regulation	$-1\text{mA} \leq I_{VDD} \leq 0$			160	ppm/mA	
	Regulator Line Regulation	$8\text{V} \leq V_{12VIN} \leq 15\text{V}$ , $I_{VDD} = 0\text{mA}$			80	ppm/V	
	Regulator Output Short-Circuit Current	$V_{12VIN} = 12\text{V}$ , $V_{DD} = 0\text{V}$	●	-5	-34	-63	mA
$V_{12VIN}$	$12V_{IN}$ Supply Operating Range		●	8	15	V	
<b>Voltage Reference Characteristics</b>							
$V_{REF}$	Reference Output Voltage			1.229		V	
	Reference Voltage Temperature Coefficient			2		ppm/ $^\circ\text{C}$	
	Reference Overdrive Voltage Input Range		●	1	1.5	V	
<b>ADC Characteristics</b>							
$N_{ADC}$	Resolution	$N_{ADC} = 8.192\text{V}/16384$		500		$\mu\text{V}/\text{LSB}$	
$TUE_{ADC}$	Total Unadjusted Error	$V_{IN} = 3\text{V}$ , $V_{IN} = V_{INn\_XP} - V_{INn\_XM}$ (Note 3)	●		$\pm 0.5$	%	
$INL_{ADC}$	Integral Nonlinearity	(Note 4)	●	-4.5	2	4.5	LSB
$DNL_{ADC}$	Differential Nonlinearity	(Note 7)	●		$\pm 0.5$	LSB	
$V_{IN\_ADC}$	Input Voltage Range		●	0	6	V	
$V_{OS\_ADC}$	Offset Error		●	-1000	-316	1000	$\mu\text{V}$
	Offset Error Drift			0.19		$\mu\text{V}/^\circ\text{C}$	
$GAIN_{ADC}$	Gain Error	Full-Scale $V_{IN} = 6\text{V}$	●		$\pm 0.4$	%	
	Gain Error Drift			3		ppm/ $^\circ\text{C}$	
$T_{CONV\_ADC}$	Conversion Time			33.3		ms	
$C_{IN\_ADC}$	Input Sampling Capacitance			3		pF	
$F_{IN\_ADC}$	Input Sampling Frequency			61.4		kHz	
$I_{LEAK\_ADC}$	Input Leakage Current	$0\text{V} < V_{IN} < 6\text{V}$	●		$\pm 0.1$	$\mu\text{A}$	
<b>IDAC Output Current Characteristics</b>							
$N_{IOUT}$	Resolution (Guaranteed Monotonic)			8		Bits	
$INL_{IOUT}$	Integral Nonlinearity	$V_{IOUTn} < V_{DD} - 1.5\text{V}$	●		$\pm 1$	LSB	
$DNL_{IOUT}$	Differential Nonlinearity	$V_{IOUTn} < V_{DD} - 1.5\text{V}$	●		$\pm 1$	LSB	
$I_{FS-IOUT}$	Full-Scale Output Current	$V_{IOUTn} < V_{DD} - 1.5\text{V}$ , DAC Code = 'hff'	●	-236	-255	-276	$\mu\text{A}$
$I_{DRIFT-IOUT}$	Output Current Drift	DAC Code = 'hff'		32		ppm/ $^\circ\text{C}$	
$I_{OS-IOUT}$	Offset Current	DAC Code = 'h00'	●		$\pm 0.1$	$\mu\text{A}$	

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**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{DD}$  and REF pins floating unless otherwise indicated,  $C_{VDD} = 100\text{nF}$  and  $C_{REF} = 100\text{nF}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>Voltage Buffered IDAC Output Characteristics</b>							
INL_V <sub>OUT</sub>	Integral Nonlinearity	$R_{IOUTn} = 10\text{k}\Omega$ , No Load on $V_{OUTn}$ (Note 5)	●		±1	LSB	
DNL_V <sub>OUT</sub>	Differential Nonlinearity	$R_{IOUTn} = 10\text{k}\Omega$ , No Load on $V_{OUTn}$ (Note 5)	●		±1	LSB	
V <sub>OS</sub> -V <sub>OUT</sub>	Offset Voltage	$V_{OS} = V_{OUTn} - V_{IOUTn}$ , No Load on $V_{OUTn}$	●	1.6	±10	mV	
	Output Voltage Drift	No Load on $V_{OUTn}$		0.17		$\mu\text{V}/^\circ\text{C}$	
V <sub>OUT</sub>	Load Regulation	$0.1\text{V} < V_{OUTn} < V_{DD} - 1.5\text{V}$ , $I_{VOUTn}$ Source = 1mA		-57		ppm/mA	
		$0.1\text{V} < V_{OUTn} < V_{DD} - 1.5\text{V}$ , $I_{VOUTn}$ Sink = 1mA		100		ppm/mA	
	Leakage Current	$V_{OUTn}$ High-Z, $0\text{V} \leq V_{OUTn} \leq V_{DD}$	●	1	±100	nA	
	Short-Circuit Current Low	$V_{OUTn}$ Shorted to GND	●		-50	mA	
	Short-Circuit Current High	$V_{OUTn}$ Shorted to $V_{DD}$	●		50	mA	
<b>Soft Connect Comparator Characteristics (CMP0, CMP1)</b>							
V <sub>OS</sub>	Offset Voltage			±3		mV	
<b>Temperature Sensor Characteristics</b>							
TMP	Gain			0.25		$^\circ\text{C}/\text{LSB}$	
<b>12V<sub>IN</sub> Voltage Divider Characteristics</b>							
GAIN_12V <sub>IN</sub>	Gain		●	0.329	0.333	0.335	V/V
<b>Digital Inputs SCL, SDA, GPIO_CFG, GPIO_0, GPIO_1</b>							
V <sub>IH</sub>	High Level Input Voltage	SDA, SCL	●	2.1		V	
		GPIO_CFG, GPIO_0, GPIO_1	●	1.6		V	
V <sub>IL</sub>	Low Level Input Voltage	SDA, SCL	●		1.5	V	
		GPIO_CFG, GPIO_0, GPIO_1	●		1.0	V	
V <sub>HYST</sub>	Input Hysteresis			0.08		V	
I <sub>LEAK</sub>	Input Leakage Current	$0\text{V} \leq V_{IN} \leq 6\text{V}$	●		±1	$\mu\text{A}$	
C <sub>IN</sub>	Input Capacitance			10		pF	
<b>Three State Inputs ASEL[1:0]</b>							
V <sub>IH_ASEL</sub>	Input High Threshold Voltage		●		$V_{DD} - 0.5$	V	
V <sub>IL_ASEL</sub>	Input Low Threshold Voltage		●	0.5		V	
I <sub>IN,HL</sub>	High, Low Input Current	ASEL[1:0] = 0, $V_{DD}$	●		±20	$\mu\text{A}$	
I <sub>IN,Z</sub>	High Z Input Current		●	±2		$\mu\text{A}$	
<b>Open Drain Outputs SDA, GPIO_CFG, GPIO_0, GPIO_1, ALERT</b>							
V <sub>OL</sub>	Output Low Voltage	$I_{SINK} = 3\text{mA}$	●		0.4	V	
I <sub>OH</sub>	Input Leakage Current	$0\text{V} \leq V_{IN} \leq 6\text{V}$	●		±1	$\mu\text{A}$	

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS	
<b>I<sup>2</sup>C Interface Timing Characteristics</b>							
f <sub>SCL</sub>	Serial Clock Frequency	(Note 6)	●	10	400	kHz	
t <sub>LOW</sub>	Serial Clock Low Period	(Note 6)	●	1.3		μs	
t <sub>HIGH</sub>	Serial Clock High Period	(Note 6)	●	0.6		μs	
t <sub>BUF</sub>	Bus Free Time Between Stop and Start	(Note 6)	●	1.3		μs	
t <sub>HD,STA</sub>	Start Condition Hold Time	(Note 6)	●	600		ns	
t <sub>SU,STA</sub>	Start Condition Setup Time	(Note 6)	●	600		ns	
t <sub>SU,STO</sub>	Stop Condition Setup Time	(Note 6)	●	600		ns	
t <sub>HD,DAT</sub>	Data Hold Time (LTC2970 Receiving Data) Data Hold Time (LTC2970 Transmitting Data)	(Note 6)	●	0 300	900	ns ns	
t <sub>SU,DAT</sub>	Data Setup Time (LTC2970 Receiving Data)	(Note 6)	●	100		ns	
t <sub>SP</sub>	Pulse Width of Spike Suppressed	(Note 6)	●	98		ns	
t <sub>SETUP_GPIO</sub>	GPIO_0 and GPIO_1 Setup Time	GPIO_0 and GPIO_1 input setup time prior to the 26th rising SCL of an IO() I <sup>2</sup> C read. These inputs must be valid and stable by this time to be returned in the IO() read result. (Note 6)	●	2.5		μs	
t <sub>HOLD_GPIO</sub>	GPIO_0 and GPIO_1 Hold Time	GPIO_0 and GPIO_1 input hold time after the 26th rising SCL of an IO() I <sup>2</sup> C read. These inputs must be held until this amount of time has elapsed to be returned in the IO() read result. (Note 6)	●	2.5		μs	
t <sub>OUT_GPIO</sub>	GPIO_0 and GPIO_1 Output Time	GPIO_0 and GPIO_1 output delay after the 35th rising SCL of an I <sup>2</sup> C write. These outputs will become high impedance or begin driving low by this time. (Note 6)	●		2.5	μs	
<b>Internal Timers</b>							
t <sub>TIMEOUT_SMB</sub>	Stuck BUS Timer	The LTC2970 will release the I <sup>2</sup> C bus and terminate the current command if the command is not completed before this amount of time has elapsed.		24	32	39	ms
t <sub>SETUP_ADC</sub>	ADC Channel Setup Time	After selecting a new ADC channel, the LTC2970 will wait this amount of time to allow the analog input to settle before beginning an ADC conversion.			304		μs
t <sub>TIMEOUT_SYNC</sub>	Tracking SYNC Failure Timer	LTC2970-1 Only: The LTC2970-1 will abort a pending SYNC() command if a tracking command is not received before this amount of time has elapsed.			255		ms
t <sub>HOLD_TRACK</sub>	Tracking IDAC Disconnect Delay	LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG low, the LTC2970-1 will delay disconnecting the IDACs from the power supply feedback nodes by this amount of time. Used while tracking power supplies on.			32		ms

# LTC2970/LTC2970-1

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
$t_{\text{SETUP\_TRACK}}$	Tracking IDAC Disconnect Delay	LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG high, the LTC2970-1 will wait this amount of time before starting to decrement $\text{Chn\_a\_delay\_track}[9:0]$ . Used while tracking power supplies off.		32		ms
$t_{\text{DEC\_TRACK}}$	Tracking IDAC Decrement Rate	LTC2970-1 Only: The LTC2970-1 changes $\text{Chn\_a\_delay\_track}[9:0]$ at this rate.		88		$\mu\text{s}/\text{LSB}$

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

**Note 3:** TUE (%) is defined as:

$$\% \text{ Gain Error} + \frac{(\text{INL} \cdot 500\mu\text{V}/\text{LSB} + V_{\text{OS}})}{V_{\text{IN}}} \cdot 100$$

**Note 4:** Integral nonlinearity (INL) is defined as the deviation of a code from a straight line passing through the actual endpoints (0V and 6V) of the transfer curve. The deviation is measured from the center of the quantization band.

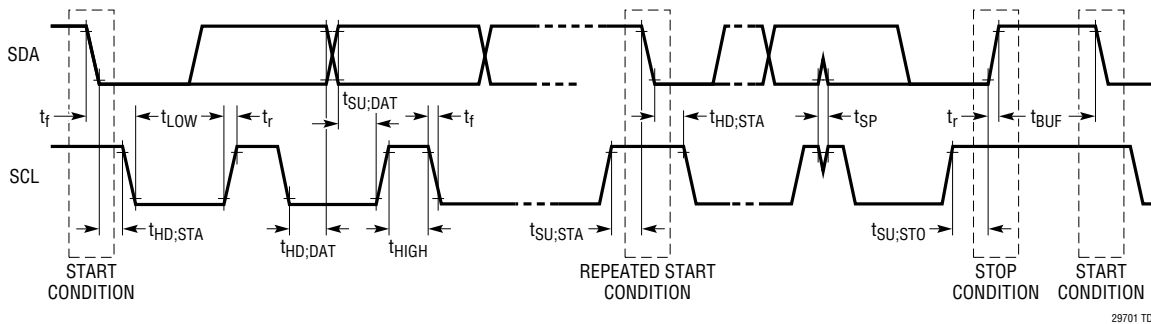
**Note 5:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 255 (full-scale).

**Note 6:** Maximum capacitive load,  $C_B$ , for SCL and SDA is 400pF. Data and clock rise time ( $t_r$ ) and fall time ( $t_f$ ) are:  $(20 + 0.1 \cdot C_B)(\text{ns}) < t_r < 300\text{ns}$  and  $(20 + 0.1 \cdot C_B)(\text{ns}) < t_f < 300\text{ns}$ .  $C_B$  = capacitance of one bus line in pF. SCL and SDA external pull-up voltage,  $V_{I0}$ , is  $3\text{V} < V_{I0} < 5.5\text{V}$ .

**Note 7:** This specification is guaranteed by design.

## TIMING DIAGRAM

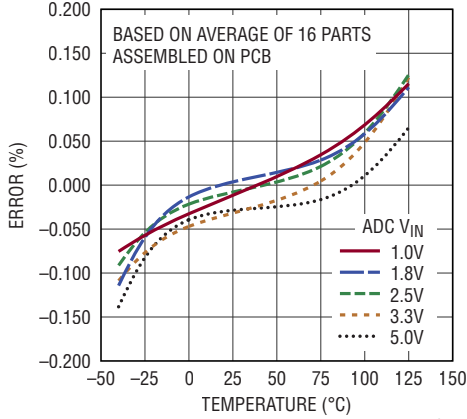
The I<sup>2</sup>C Bus Specification



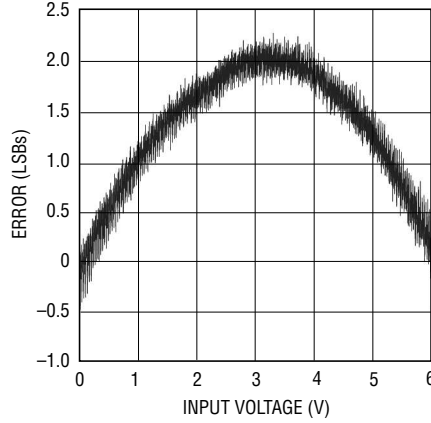
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# TYPICAL PERFORMANCE CHARACTERISTICS

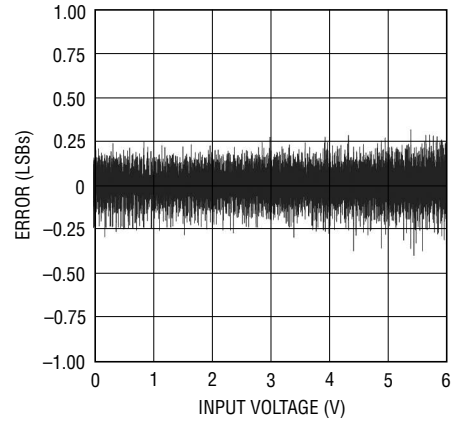
**ADC Total Unadjusted Error vs Temperature**



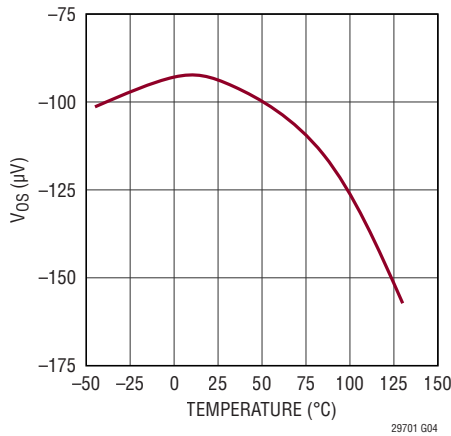
**ADC INL**



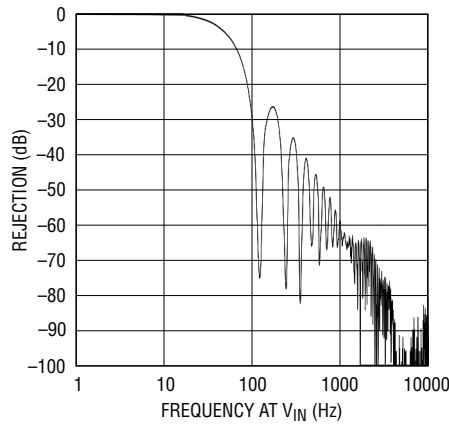
**ADC DNL**



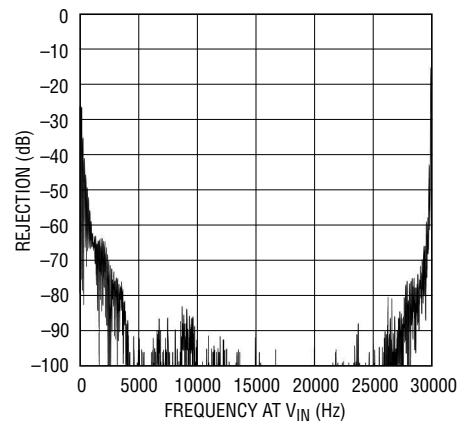
**ADC Zero Code Center Offset Voltage vs Temperature**



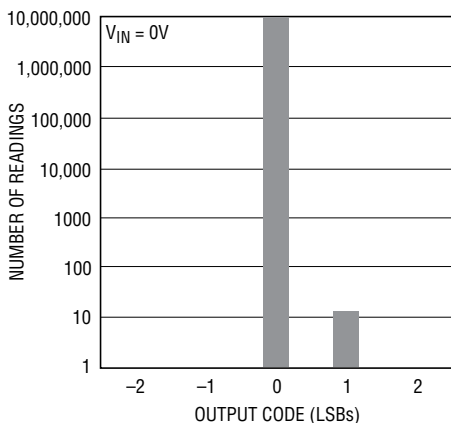
**ADC Rejection vs Frequency at  $V_{IN}$**



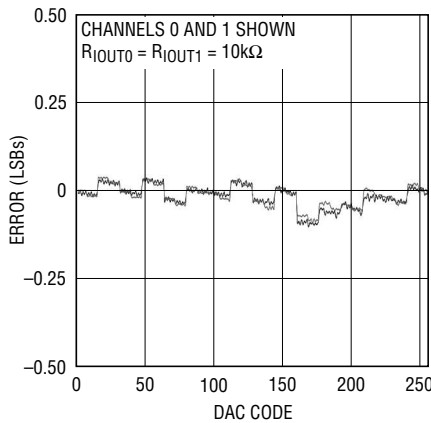
**ADC Rejection vs Frequency at  $V_{IN}$**



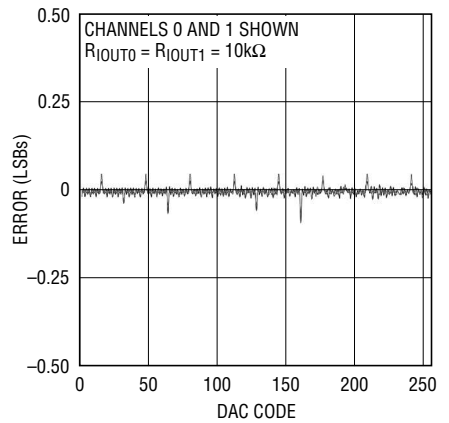
**ADC Noise Histogram**



**Voltage Buffered IDAC INL**



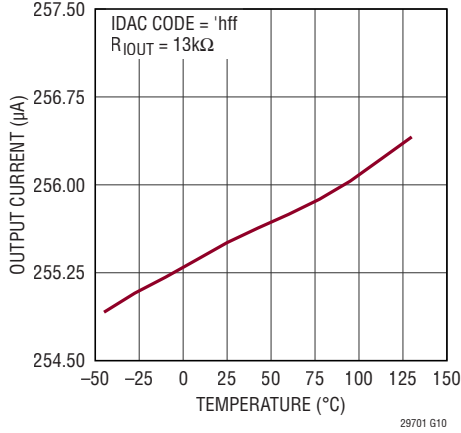
**Voltage Buffered IDAC DNL**



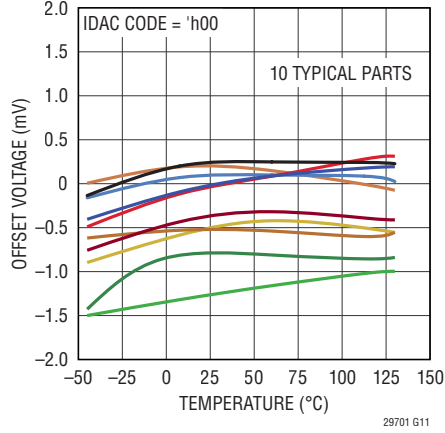


## TYPICAL PERFORMANCE CHARACTERISTICS

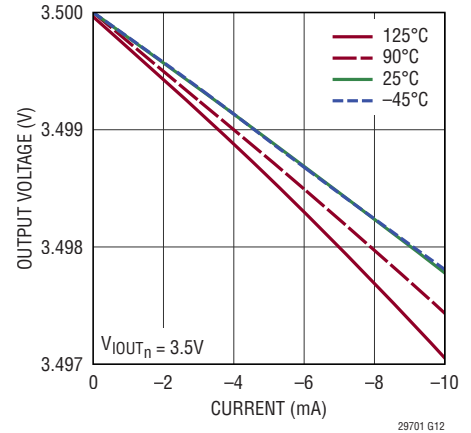
**IDAC Output Current vs Temperature**



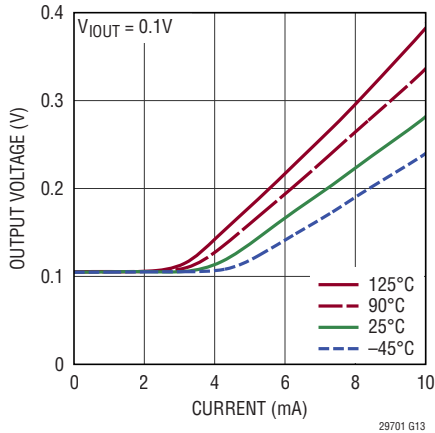
**V<sub>OUTn</sub> Offset Voltage vs Temperature**



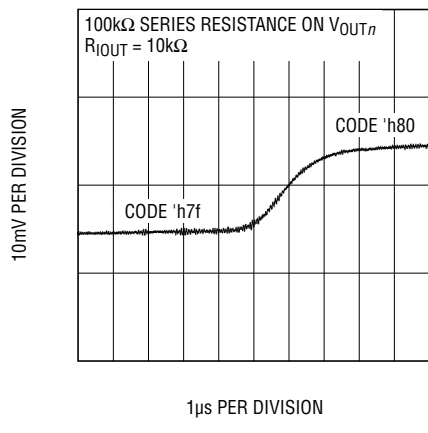
**Voltage Buffered IDAC Load Regulation Sourcing**



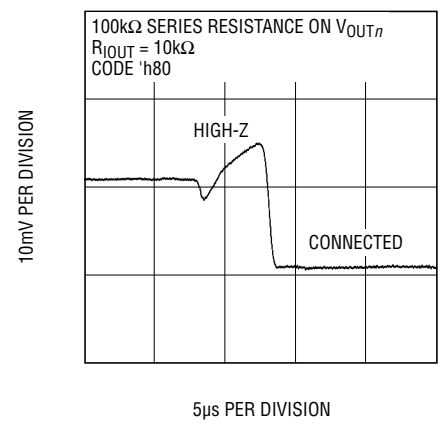
**Voltage Buffered IDAC Load Regulation Sinking**



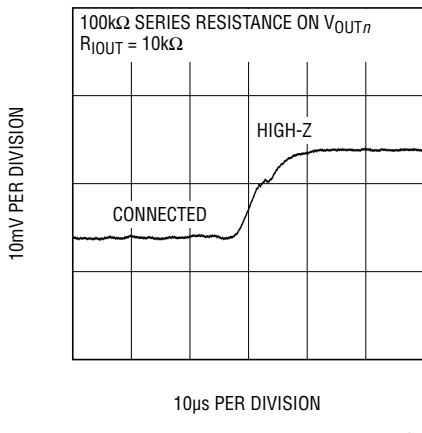
**Voltage Buffered IDAC Transient Response to 1LSB DAC Code Change**



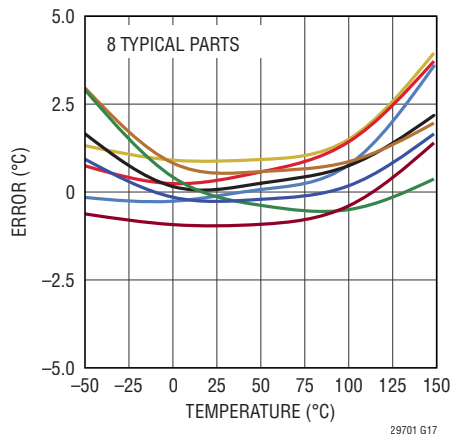
**Voltage Buffered IDAC Soft-Connect Transient Response**



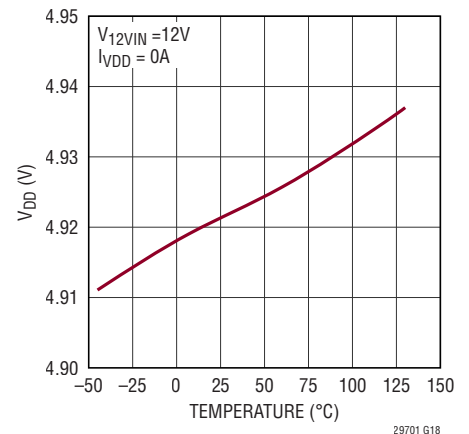
**Voltage Buffered IDAC Transient Response During Transition from On State to High-Z State**



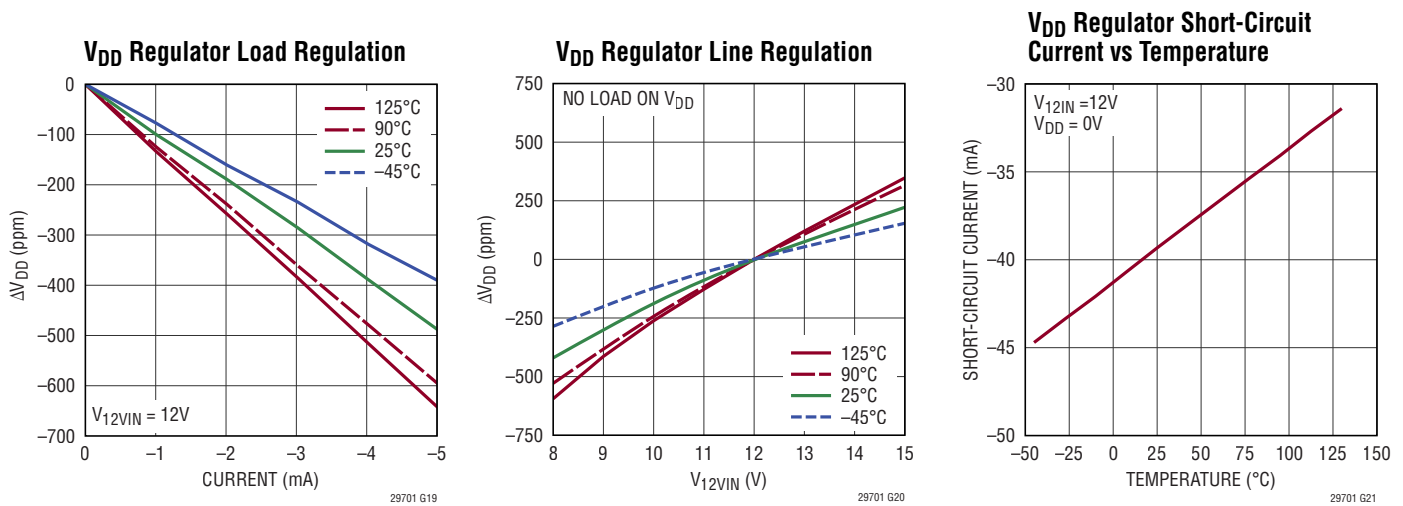
**Temperature Sensor Error vs Temperature**



**V<sub>DD</sub> Regulator Output Voltage vs Temperature**



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**V<sub>INO\_AP</sub> (Pin 1):** Positive CH0\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_A can be configured to servo IDACO.

**V<sub>INO\_AM</sub> (Pin 2):** Negative CH0\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_A can be configured to servo IDACO.

**V<sub>INO\_BP</sub> (Pin 3):** Positive CH0\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_B is a voltage monitor input only.

**V<sub>INO\_BM</sub> (Pin 4):** Negative CH0\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_B is a voltage monitor input only.

**V<sub>IN1\_AP</sub> (Pin 5):** Positive CH1\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_A can be configured to servo IDAC1.

**V<sub>IN1\_AM</sub> (Pin 6):** Negative CH1\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_A can be configured to servo IDAC1.

**V<sub>IN1\_BP</sub> (Pin 7):** Positive CH1\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_B is a voltage monitor input only.

**V<sub>IN1\_BM</sub> (Pin 8):** Negative CH1\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_B is a voltage monitor input only.

**V<sub>DD</sub> (Pin 9):** V<sub>DD</sub> Power Supply, Voltage Monitor Input, and Internal 5V Regulator Output. The supply input range is 4.5V to 5.75V. The V<sub>DD</sub> pin voltage can be connected to the ADC through an internal mux. Bypass the V<sub>DD</sub> pin to device ground with a 100nF capacitor (C<sub>VDD</sub>). If no 5V input voltage supply is available, float the V<sub>DD</sub> pin and power the LTC2970 from the 12V<sub>IN</sub> pin.

**12V<sub>IN</sub> (Pin 10):** 12V Power Supply and Voltage Monitor Input. An internal regulator generates 5V from 12V<sub>IN</sub>. The input range for 12V<sub>IN</sub> is 8V to 15V. Bypass this pin with a 100nF capacitor. The regulator's output is connected to the V<sub>DD</sub> pin. The 12V<sub>IN</sub> pin voltage can also be monitored by the ADC through a 3:1 attenuator and the internal mux. If no 12V supply input is available, tie the 12V<sub>IN</sub> to the V<sub>DD</sub> pin and operate from 4.5V to 5.75V.

**V<sub>OUTO</sub> (Pin 11):** CH0 Voltage Output. Buffered version of IDACO output voltage.

## PIN FUNCTIONS

**V<sub>OUT1</sub> (Pin 12): CH1 Voltage Output.** Buffered version of IDAC1 output voltage.

**I<sub>OUT1</sub> (Pin 13): IDAC1 Current Output.** Connect a resistor between this pin and the point-of-load ground for channel 1. The IDAC sources between 0 and 255 $\mu$ A.

**I<sub>OUT0</sub> (Pin 14): IDAC0 Current Output.** Connect a resistor between this pin and the point-of-load ground for channel 0. The IDAC sources between 0 and 255 $\mu$ A.

**GPIO\_1 (Pin 15): General Purpose Input or Open Drain Digital Output.** GPIO\_1 can be configured as the IDAC Fault or Faults output, a digital input, or an open-drain digital output.

**GPIO\_0 (Pin 16): General Purpose Input or Open Drain Digital Output.** GPIO\_0 can be configured as the voltage monitor power-good or power-good bar output, a digital input, or a programmable open-drain output. Power good is the NOR of all instantaneous OV and UV faults; it does not include IDAC faults.

**$\overline{\text{ALERT}}$  (Pin 17): Open Drain Digital Output.** Connect the SMBALERT signal to this pin.  $\overline{\text{ALERT}}$  is asserted low when either IDAC0 or IDAC1 rails out (optional), or when one of the monitored voltages ventures outside its UV and OV thresholds (also optional).

**SCL (Pin 18): Serial Bus Clock Input.**

**SDA (Pin 19): Serial Bus Data Input and Output.**

**GPIO\_CFG (Pin 20): GPIO Configuration Digital Input and Open Drain Output.** Pulling GPIO\_CFG high will cause the GPIO\_0 and GPIO\_1 open-drain outputs to automatically assert low after a power-on reset. If GPIO\_CFG is pulled low, then GPIO\_0 and GPIO\_1 do not assert low after power-up.

**ASEL1 (Pin 21): Slave Address Select Bit 1.** Tie this pin to the V<sub>DD</sub> pin, ground, or float in order to select the address location (see Table 2).

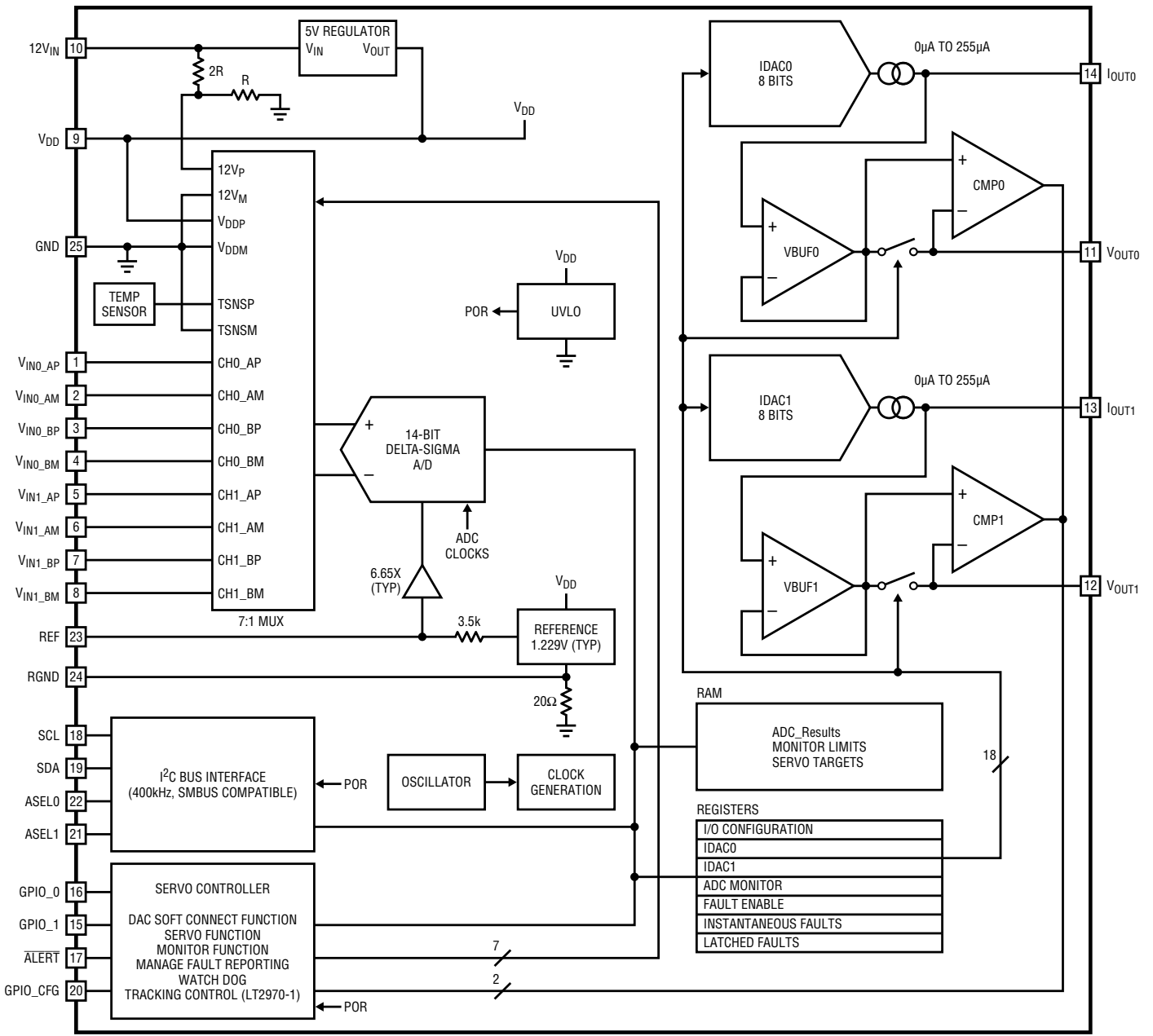
**ASEL0 (Pin 22): Slave Address Select Bit 0.** Tie this pin to the V<sub>DD</sub> pin, ground, or float in order to select the address location (see Table 2).

**REF (Pin 23): Internal Reference Output or ADC Reference Overdrive Input.** The voltage at this pin determines the full-scale input voltage of the delta-sigma ADC ( $V_{\text{FULL-SCALE}} = 6.65 \cdot V_{\text{REF}}$ , typically). An internal 3.5k resistor decouples the reference output from this pin. Bypass this pin to RGND with a 100nF capacitor (C<sub>REF</sub>).

**RGND (Pin 24): Reference Ground.** Connect to device ground.

**GND (Pin 25): Device Ground.** Must be soldered to ground.

# BLOCK DIAGRAM



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## OPERATION

### 1. LTC2970 Operation Overview

The LTC2970 is designed to control and monitor two power supplies. The LTC2970's superior accuracy allows it to precisely servo each supply's output voltage over a wide range of operating conditions; increasing accuracy, reducing power requirements and component costs. Margining may be performed with equal ease and precision. The monitoring functions allow for increased reliability by alerting a system host about incipient failures before they occur. The seven channel ADC may also be used to monitor current, temperature, and the 5V or optional 12V supply.

The LTC2970's unique architecture and control algorithm have been especially tailored for power supply management. The soft connect feature allows the LTC2970 to begin controlling a power supply without perturbing its initial value. The delta-sigma ADC architecture was specifically chosen to average out power-supply noise and allow the LTC2970 to ignore fast transients. Unlike discrete time DACs, the LTC2970's continuous time, voltage buffered IDAC is ideal for noise sensitive applications. The servo algorithm limits the IDAC step size to one LSB per iteration in order to minimize power supply transients. The point of load ground reference for the IDAC outputs minimize errors that would otherwise occur in a power system that experiences ground bounce. By selecting two resistor values, the user can choose the appropriate resolution while providing an important hardware range limit beyond which the supply may not be driven. The servo on fault option allows the LTC2970 to further reduce output voltage disturbances by only stepping the IDAC when the output voltage drifts outside of a user programmable window. The LTC2970 powers up in a high impedance state and will not interfere with default power supply operation. Similarly, powering down the LTC2970 will restore its high impedance state.

All communication with the LTC2970 is performed over an industry standard I<sup>2</sup>C bus. The LTC2970 I<sup>2</sup>C interface also meets all SMBus setup times, hold times, and timeout requirements. The ALERT pin may be used to signal that one or more of the fourteen configurable fault limits have been reached. Each fault may be individually masked. The I<sup>2</sup>C interface supports word reads, word writes and the SMBus Alert Response Address protocol. Two general purpose IO pins may be used to provide additional fault information or user defined system control. Powering down the LTC2970 will not interfere with I<sup>2</sup>C operation.

The LTC2970-1 enables power supply tracking and sequencing with the addition of a few external components. A special global address and synchronization command allow multiple LTC2970-1's to track and sequence multiple pairs of power supplies.

The LTC2970 can perform the following operations:

- Accept all programming commands and report status over the I<sup>2</sup>C or SMBus bus.
- Command each voltage buffered IDAC to connect to the corresponding power supply's feedback node through an external resistor using the IDAC code that most closely approximates the feedback node's regulation voltage (Soft Connect).
- Command each voltage buffered IDAC output to connect to the corresponding power supply's feedback node through an external resistor with a user-selected IDAC code (Hard Connect).
- Change the code of a previously connected IDAC.
- Disconnect each voltage buffered IDAC output from the power supply's feedback node.
- *LTC2970-1 Only:* Track two power supplies up or down. Multiple LTC2970-1's can be configured to track simultaneously or in a sequence.

## OPERATION

- Continuously servo one or both supplies to a programmed voltage.
- Perform a one-time servo of one or both supplies to a programmed voltage and hold the servo codes in the controlling IDAC.
- Perform a one time servo of one or both supplies to a programmed voltage and hold the code(s) in the controlling IDAC(s) until over/under voltage monitoring detects a fault, at which point a control bit may be used to allow the LTC2970 to servo back to the initial voltage target.
- Select any combination of seven possible ADC channels to be monitored by the ADC.
- Generate instantaneous faults based on user programmable overvoltage and undervoltage limits and fixed IDAC limits. The status of OR'd voltage limit faults and IDAC faults may be output over GPIO\_0 and GPIO\_1, respectively.
- Enable instantaneous faults to set associated latched faults using the FAULT\_EN register. The status of OR'd latched faults may be signalled using ALERT.
- Configure the GPIO\_0 and GPIO\_1 pins to act as inputs or outputs.

### 2. I<sup>2</sup>C Serial Digital Interface

The LTC2970 communicates with a host (master) using the 2-wire, I<sup>2</sup>C serial bus interface. The Timing Diagram shows the timing relationship of the signals on the bus.

The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2970 I<sup>2</sup>C interface is SMBus compatible; it meets all SMBus setup times, hold times and timeout requirements.

The LTC2970 is a receive-only (slave) device. The LTC2970 can signal the host through the SMBALERT protocol that it wants to talk by asserting  $\overline{\text{ALERT}}$  low. The LTC2970 supports the three I<sup>2</sup>C protocols summarized in Table 1.

#### Slave Address

The LTC2970 can respond to one of nine 7-bit addresses. The two slave address select pins (ASEL1 and ASEL0) are programmed by the user and determine the slave address, as shown in Table 2.

The LTC2970 also supports the ARA address and a global address that allows multiple LTC2970s to be programmed with the same data simultaneously, as shown in Table 3.

**Table 1. Supported I<sup>2</sup>C Command Types**

<b>READ DATA WORD:</b>
S:ADR:W:A:CMD:A:Sr:ADR:R:A:DATA:A:DATA:NACK:P
<b>WRITE DATA WORD:</b>
S:ADR:W:A:CMD:A:DATA:A:DATA:A:P
<b>ALERT RESPONSE</b>
S:ARA:R:A:ADR:NACK:P:

## OPERATION

**Table 2. LTC2970 Address Table**

ADDRESS[7:0] (R/W = 0)	ADDRESS[7:1]	ASEL1	ASEL0
8'hB8	7'h5C	L	L
8'hBA	7'h5D	L	F
8'hBC	7'h5E	L	H
8'hBE	7'h5F	F	L
8'hD6	7'h6B	F	F
8'hD8	7'h6C	F	H
8'hDA	7'h6D	H	L
8'hDC	7'h6E	H	F
8'hDE	7'h6F	H	H

L:  $V_{ASEL_n} < V_{IL\_ASEL}$  F: ASEL $_n$  Floating H:  $V_{ASEL_n} > V_{IH\_ASEL}$

**Table 3. Special LTC2970 Addresses**

	ADDRESS[7:0] (R/W = 0)	ADDRESS[7:1]	FUNCTION
ARA	8'h18	7'h0C	This is the standard Alert Response Address for all SMBus devices. This address is independent of the value of the ASEL1 and ASEL0 pins.
Global	8'hB6	7'h5B	This a global address to which all LTC2970s will respond. This address is independent of the value of the ASEL1 and ASEL0 pins.

### 3. Register Command Set

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH	COMMAND BYTE VALUE
FAULT()	Instantaneous Fault Status For All Channels	Read Only	16 Bits	'h00
FAULT_EN()	Enable For All Latched Faults and Servo On Fault	Read/Write	16 Bits	'h08
FAULT_LA_INDEX()	Index to All Latched Faults	Read Only	16 Bits	'h10
FAULT_LA()	Latched Fault Status For All Channels	Read Only	16 Bits	'h11
IO()	IO Control and Status Register	Read/Write	16 Bits	'h17
ADC_MON()	Control Register For Selecting ADC Channels to Monitor	Read/Write	16 Bits	'h18
*SYNC()	Control Register For Synchronizing Tracking Across Multiple Devices	Read/Write	16 Bits	'h1F
VDD_ADC()	$V_{DDIN}$ ADC Conversion Result Register	Read Only	16 Bits	'h28
VDD_OV()	$V_{DDIN}$ Overvoltage Monitor Control Register	Read/Write	16 Bits	'h29
VDD_UV()	$V_{DDIN}$ Undervoltage Monitor Control Register	Read/Write	16 Bits	'h2A
V12_ADC()	$12V_{IN}$ ADC Conversion Result Register	Read Only	16 Bits	'h38
V12_OV()	$12V_{IN}$ Overvoltage Monitor Control Register	Read/Write	16 Bits	'h39
V12_UV()	$12V_{IN}$ Undervoltage Monitor Control Register	Read/Write	16 Bits	'h3A
CH0_A_ADC()	CH0_A ADC Conversion Result Register	Read Only	16 Bits	'h40
CH0_A_OV()	CH0_A Overvoltage Monitor Control Register	Read/Write	16 Bits	'h41
CH0_A_UV()	CH0_A Undervoltage Monitor Control Register	Read/Write	16 Bits	'h42
CH0_A_SERVO()	CH0_A Voltage Servo Control Register	Read/Write	16 Bits	'h43
CH0_A_IDAC()	CH0_A IDAC Control Register	Read/Write	16 Bits	'h44
*CH0_A_IDAC_TRACK()	CH0_A IDAC Track Final Value Register	Read/Write	16 Bits	'h45
*CH0_A_DELAY_TRACK()	CH0_A IDAC Track Delay Register	Read/Write	16 Bits	'h46
CH0_B_ADC()	CH0_B ADC Conversion Result Register	Read Only	16 Bits	'h48
CH0_B_OV()	CH0_B Overvoltage Monitor Control Register	Read/Write	16 Bits	'h49
CH0_B_UV()	CH0_B Undervoltage Monitor Control Register	Read/Write	16 Bits	'h4A
CH1_A_ADC()	CH1_A ADC Conversion Result Register	Read Only	16 Bits	'h50
CH1_A_OV()	CH1_A Overvoltage Monitor Control Register	Read/Write	16 Bits	'h51
CH1_A_UV()	CH1_A Undervoltage Monitor Control Register	Read/Write	16 Bits	'h52

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## OPERATION

### 3. Register Command Set (Cont.)

COMMAND FUNCTION	DESCRIPTION	R/W	DATA LENGTH	COMMAND BYTE VALUE
CH1_A_SERVO()	CH1_A Voltage Servo Control Register	Read/Write	16 Bits	'h53
CH1_A_IDAC()	CH1_A IDAC Control Register	Read/Write	16 Bits	'h54
*CH1_A_IDAC_TRACK()	CH1_A IDAC Track Control Register	Read/Write	16 Bits	'h55
*CH1_A_DELAY_TRACK()	CH1_A IDAC Track Delay Register	Read/Write	16 Bits	'h56
CH1_B_ADC()	CH1_B ADC Conversion Result Register	Read Only	16 Bits	'h58
CH1_B_OV()	CH1_B Overvoltage Monitor Control Register	Read/Write	16 Bits	'h59
CH1_B_UV()	CH1_B Undervoltage Monitor Control Register	Read/Write	16 Bits	'h5A
TEMP_ADC()	Temperature ADC Conversion Result Register	Read/Write	16 Bits	'h68
RESERVED()	All other commands are reserved for future expansion and should not be written or read.	Read/Write	16 Bits	'hXX

\*LTC2970-1 Only. LTC2970 will not acknowledge these commands.

### 4. Detailed I<sup>2</sup>C Command Register Descriptions

#### FAULT: Instantaneous Fault Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_ch0_a_ov	0 = The associated channel is clear of instantaneous faults. 1 = The associated channel has an instantaneous fault. The reported faults are instantaneous and not latched. When used in conjunction with latched faults they may indicate faults that are transient in nature.
b[1]	Fault_ch0_a_uv	
b[2]	Fault_ch0_a_idac	
b[3]	Fault_ch0_b_ov	
b[4]	Fault_ch0_b_uv	
b[5]	Fault_ch1_a_ov	
b[6]	Fault_ch1_a_uv	
b[7]	Fault_ch1_a_idac	
b[8]	Fault_ch1_b_ov	
b[9]	Fault_ch1_b_uv	
b[10]	Fault_vdd_ov	
b[11]	Fault_vdd_uv	
b[12]	Fault_v12_ov	
b[13]	Fault_v12_uv	
b[15:14]	Reserved	Always Returns 0

#### FAULT\_EN: Fault Enabling Register – Read/Write

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_en_ch0_a_ov	0 = The associated bit in the FAULT_LA register will always be 0. (default) 1 = Instantaneous faults reported in the FAULT register will set associated bit in the FAULT_LA register.
b[1]	Fault_en_ch0_a_uv	
b[2]	Fault_en_ch0_a_idac	
b[3]	Fault_en_ch0_b_ov	
b[4]	Fault_en_ch0_b_uv	
b[5]	Fault_en_ch1_a_ov	
b[6]	Fault_en_ch1_a_uv	
b[7]	Fault_en_ch1_a_idac	
b[8]	Fault_en_ch1_b_ov	
b[9]	Fault_en_ch1_b_uv	
b[10]	Fault_en_vdd_ov	
b[11]	Fault_en_vdd_uv	
b[12]	Fault_en_v12_ov	
b[13]	Fault_en_v12_uv	
b[14]	Fault_en_ch0_a_servo	0 = Do not re-servo CH0_A in response to instantaneous OV or UV fault. 1 = Repeat a one time servo of CH0_A in response to instantaneous OV or UV fault. CH0_A must have servo operation enabled with Ch0_a_idac_servo_repeat set low, and Adc_mon_ch0_a set high.
b[15]	Fault_en_ch1_a_servo	0 = Do not re-servo CH1_A in response to instantaneous OV or UV fault. 1 = Repeat a one time servo of CH1_A in response to instantaneous OV or UV fault. CH1_A must have servo operation enabled with Idac_ch1_a_servo_repeat set low, and Adc_mon_ch1_a set high.

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## OPERATION

### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### FAULT\_INDEX: Latched Fault Index Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_la_index	0 = All faults indicated by FAULT_LA are clear. 1 = One or more faults indicated by FAULT_LA are set.  This register allows a summary of all latched faults to be viewed in a single read without resetting latched faults.
b[15:1]	Reserved	Always Returns 0

#### FAULT\_LA: Latched Fault Register – Read

BIT(s)	SYMBOL	OPERATION
b[0]	Fault_la_ch0_a_ov	0 = The associated channel is clear of faults. 1 = The associated channel has faulted and is enabled.
b[1]	Fault_la_ch0_a_uv	
b[2]	Fault_la_ch0_a_idac	The latched faults are set and held when the associated channel's instantaneous fault has occurred with faults enabled. Clearing the enable bit for the associated channel in FAULT_EN will immediately clear its corresponding latched fault bit.
b[3]	Fault_la_ch0_b_ov	
b[4]	Fault_la_ch0_b_uv	All latched channel faults are cleared when this register is read. They may be set again if the instantaneous fault condition and fault_en have not changed.
b[5]	Fault_la_ch1_a_ov	
b[6]	Fault_la_ch1_a_uv	Always Returns 0
b[7]	Fault_la_ch1_a_idac	
b[8]	Fault_la_ch1_b_ov	Always Returns 0
b[9]	Fault_la_ch1_b_uv	
b[10]	Fault_la_vdd_ov	Always Returns 0
b[11]	Fault_la_vdd_uv	
b[12]	Fault_la_v12_ov	Always Returns 0
b[13]	Fault_la_v12_uv	
b[15:14]	Reserved	Always Returns 0

#### IO: Input/Output Data and General Purpose Control Register – Read/Write unless specified otherwise.

BIT(s)	SYMBOL	OPERATION
b[1:0]	lo_cfg_0[1:0]	lo_cfg_0[1:0] is used to configure the function of the GPIO_0 pin and IO(lo_gpio_0). 00: lo_gpio_0 = GPIO_0 = Power_good. Power_good asserts high if there are no instantaneous overvoltage or undervoltage faults. 01: lo_gpio_0 = GPIO_0 = Power_good_bar. Power_good_bar is the complement of Power_good. 10: GPIO_0 is a general-purpose open-drain output and mirrors the value written to lo_gpio_0 (default). 11: GPIO_0 is a general-purpose digital input with lo_gpio_0 = GPIO_0
b[3:2]	lo_cfg_1[1:0]	lo_cfg_1[1:0] is used to configure the function of the GPIO_1 pin and IO(lo_gpio_1). 00: lo_gpio_1 = GPIO_1 = Idac_fault. Idac_fault asserts if either IDAC value is faulted (Chn_idac[7:0] = 8'h00 or 8'hff) 01: lo_gpio_1 = GPIO_1 = Idac_fault_bar. Idac_fault_bar is the complement of Idac_fault. 10 = GPIO_1 is a general-purpose open-drain output and mirrors the value written to lo_gpio_1 (default). 11 = GPIO_1 is a general-purpose digital input with lo_gpio_1 = GPIO_1
b[4]	lo_gpio_0	See lo_cfg_0. If the GPIO_CFG pin is pulled-high during a power on reset, lo_gpio_0 is cleared and the GPIO_0 open-drain output will assert low.
b[5]	lo_gpio_1	See lo_cfg_1. If the GPIO_CFG pin is pulled-high during a power on reset, lo_gpio_1 is cleared and the GPIO_1 open-drain output will assert low.
b[6]	lo_alertb	Mirrors the value of the $\overline{\text{ALERT}}$ pin. Read only.
b[7]	lo_alertb_enb	1 = $\overline{\text{ALERT}}$ pin never asserts (default). 0 = $\overline{\text{ALERT}}$ pin asserts low when one or more FAULT_LA bits are set.
b[8]	lo_i2c_adc_wen	1 = Special test mode that inhibits ADC from writing to ADC result register and allows user to update registers over the I <sup>2</sup> C serial interface. 0 = Normal operation (default).
b[9]	lo_gpio_cfg	Read only. GPIO_CFG digital input and open-drain output. Reading this bit returns the current state of the GPIO_CFG pin voltage.
b[10]	lo_track_start	Writing a 1 to this bit will start tracking all enabled channels. Returns a 1 when tracking is pending (LTC2970-1). Reserved on LTC2970 and always returns 0.
b[15:11]	Reserved	Always Returns 0

## OPERATION

### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### ADC\_MON: ADC Monitoring Mux Control Register – Read/Write

BIT(s)	SYMBOL	OPERATION
b[0]	Adc_mon_vdd	0 = ADC will not convert associated channel. (Default) 1 = ADC will continuously convert associated channel.
b[1]	Adc_mon_v12	
b[2]	Adc_mon_ch0_a	
b[3]	Adc_mon_ch0_b	
b[4]	Adc_mon_ch1_a	
b[5]	Adc_mon_ch1_b	
b[6]	Adc_mon_temp	
b[15:7]	Reserved	Always Returns 0

#### SYNC: Tracking Synchronization Control Register – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[0]	Sync_track	<p>Write</p> <p>0 = Do not synchronize. 1 = Synchronize all tracking enabled registers to the same starting point.</p> <p>Read</p> <p>0 = The LTC2970-1 is not synchronized for tracking (default). 1 = The LTC2970-1 is synchronized for tracking.</p> <p>Use of the global address will allow the synchronization status of multiple LTC2970-1s to be verified in a single read; since a one can only be returned if all LTC2970-1s are synchronized. The IO_track_start command may then be issued with the same global address to begin synchronized tracking across multiple ICs.</p>
b[15:1]	Reserved	Always Returns 0

#### VDD\_ADC, V12\_ADC, CH0\_A\_ADC, CH0\_B\_ADC, CH1\_A\_ADC, CH1\_B\_ADC, and TEMP\_ADC: ADC Conversion Result Registers – Read Only Unless Specified Otherwise

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_adc[14:0] V12_adc[14:0] Ch0_a_adc[14:0] Ch0_b_adc[14:0] Ch1_a_adc[14:0] Ch1_b_adc[14:0] Temp_adc[14:0]	<p>Measured data from ADC conversion.</p> <p>'h4000 corresponds to negative full-scale input voltage. 'h0000 corresponds to 0V. 'h3fff corresponds to full-scale input voltage.</p> <p>12V<sub>IN</sub> is divided by 3 before being measured by the ADC.</p> <p>2's complement format, b[14] = sign. Read/Write when lo_i2c_adc_wen = 1. Default value is undefined.</p>
b[15]	Vdd_adc_new V12_adc_new Ch0_a_adc_new Ch0_b_adc_new Ch1_a_adc_new Ch1_b_adc_new Temp_adc_new	<p>1 = The ADC has updated the associated result register since the last time the data was read. 0 = Previously read data. (Default)</p>

#### VDD\_OV, V12\_OV, CH0\_A\_OV, CH0\_B\_OV, CH1\_A\_OV, CH1\_B\_OV: Over Voltage Limit Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_ov[14:0] V12_ov[14:0] Ch0_a_ov[14:0] Ch0_b_ov[14:0] Ch1_a_ov[14:0] Ch1_b_ov[14:0]	<p>ADC overvoltage threshold limit.</p> <p>The associated instantaneous over voltage fault is asserted if the channel's ADC result is greater than this limit. Code 'h3fff disables OV threshold detect feature for that channel.</p> <p>12V<sub>IN</sub> is divided by 3 before being measured by the ADC.</p> <p>2's complement format, b[14] = sign. Default value is undefined.</p>
b[15]	Reserved	Always Returns 0

#### VDD\_UV, V12\_UV, CH0\_A\_UV, CH0\_B\_UV, CH1\_A\_UV, CH1\_B\_UV: Under Voltage Limit Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Vdd_uv[14:0] V12_uv[14:0] Ch0_a_uv[14:0] Ch0_b_uv[14:0] Ch1_a_uv[14:0] Ch1_b_uv[14:0]	<p>ADC undervoltage threshold limit.</p> <p>The associated instantaneous under voltage fault is asserted if the channel's ADC result is greater than this limit. Code 'h4000 disables UV threshold detect feature for that channel.</p> <p>12V<sub>IN</sub> is divided by 3 before being measured by the ADC.</p> <p>2's complement format, b[14] = sign. Default value is undefined.</p>
b[15]	Reserved	Always Returns 0

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### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### CH0\_A\_SERVO, CH1\_A\_SERVO: Voltage Servo Control Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[14:0]	Ch0_a_servo[14:0] Ch1_a_servo[14:0]	During servo operation Ch <sub>n</sub> _a_idac[7:0] output current is stepped to force Ch <sub>n</sub> _a_adc[14:0] code to equal target code stored in Ch <sub>n</sub> _a_servo[14:0]. 2's complement format, b[14] = sign Default value is undefined.
b[15]	Ch0_a_servo_en Ch1_a_servo_en	0 = Ch <sub>n</sub> _a servo disabled (default). 1 = Ch <sub>n</sub> _a servo enabled.

#### CH0\_A\_IDAC, CH1\_A\_IDAC: IDAC Control/Data Registers – Read/Write

BIT(s)	SYMBOL	OPERATION
b[7:0]	Ch0_a_idac[7:0] Ch1_a_idac[7:0]	Ch <sub>n</sub> _a IDAC data value.
b[8]	Ch0_a_idac_en Ch1_a_idac_en	0 = V <sub>OUT<sub>n</sub></sub> output tri-stated. 1 = V <sub>OUT<sub>n</sub></sub> output enabled. There are two ways to enable V <sub>OUT<sub>n</sub></sub> . 1) When Ch <sub>n</sub> _a_idac_en is set high with Ch <sub>n</sub> _a_idac_con low, the LTC2970 will perform a soft connect. During a soft connect, the V <sub>OUT<sub>n</sub></sub> voltage buffer output will not be connected to the V <sub>OUT<sub>n</sub></sub> pin until the internal algorithm has servo'd the voltage at the IDAC <sub>n</sub> pin to match the V <sub>OUT<sub>n</sub></sub> pin voltage. Resolution is one Ch <sub>n</sub> _a_idac LSB. 2) When Ch <sub>n</sub> _a_idac_en is enabled with Ch <sub>n</sub> _a_idac_con high, the LTC2970 will perform a hard connect. The V <sub>OUT<sub>n</sub></sub> voltage buffer will be immediately connected to the V <sub>OUT<sub>n</sub></sub> pin.
b[9]	Ch0_a_idac_con Ch1_a_idac_con	0 = V <sub>OUT<sub>n</sub></sub> is not enabled or has been enabled but is not yet connected to the output of the CH <sub>n</sub> voltage buffer. (Default) 1 = V <sub>OUT<sub>n</sub></sub> is enabled and has been connected to the output of the CH <sub>n</sub> voltage buffer. See Ch <sub>n</sub> _a_idac_en for additional information.

b[10]	Ch0_a_idac_pol Ch1_a_idac_pol	0 = Use this setting when increasing V <sub>OUT<sub>n</sub></sub> causes (VIN <sub>n</sub> _AP-VIN <sub>n</sub> _AM) to decrease. Inverting configuration common to DC/DC converters with external feedback networks. 1 = Use this setting when increasing V <sub>OUT<sub>n</sub></sub> causes (VIN <sub>n</sub> _AP-VIN <sub>n</sub> _AM) to increase. Non-inverting configuration common to DC/DC converters with trim pins.
b[11]	Ch0_a_idac_servo_repeat Ch1_a_idac_servo_repeat	0 = During servo operation, servo Ch <sub>n</sub> _a until the measured result is stable and matches the target code. 1 = During servo operation, continuously servo Ch <sub>n</sub> _a to the target code.
b[15:12]	Reserved	Always Returns 0

#### CH0\_A\_IDAC\_TRACK and CH1\_A\_IDAC\_TRACK: IDAC Tracking data and control registers – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[7:0]	Ch0_a_idac_track[7:0] Ch1_a_idac_track[7:0]	Final target value for of Ch <sub>n</sub> _a_idac[7:0]. During tracking, Ch <sub>n</sub> _a_idac[7:0] is incremented/decremented by 1 until it is equal to this value.
b[8]	Ch0_a_idac_track_en Ch1_a_idac_track_en	0 = inhibit tracking of Ch <sub>n</sub> _a_idac[7:0]. 1 = enable tracking of Ch <sub>n</sub> _a_idac[7:0]
b[15:9]	Reserved	Always Returns 0

#### CH0\_A\_DELAY\_TRACK and CH1\_A\_DELAY\_TRACK: IDAC Tracking delay register – Read/Write LTC2970-1 Only

BIT(s)	SYMBOL	OPERATION
b[9:0]	Ch0_a_delay_track[9:0] Ch1_a_delay_track[9:0]	Delay used to synchronize or offset tracking events.
b[15:10]	Reserved	Always Returns 0

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### 5. Soft Connecting the LTC2970 to the Power Supply Feedback Node

The soft connect feature allows the LTC2970 to connect to the power supply's feedback node with minimal disturbance to the supply's output voltage. This is accomplished by comparing the buffered voltage of  $I_{OUTn}$  to the voltage at  $V_{OUTn}$  and incrementing or decrementing  $Chn\_a\_idac[7:0]$  until the comparator output (COMP $n$ ) changes. The value of  $Chn\_a\_idac[7:0]$  when the comparator transitions is the appropriate value for a soft connect. The voltage buffer output is only connected to  $V_{OUTn}$  if the IDAC reaches this soft connect value without generating an instantaneous IDAC fault (Fault\_chn\_a\_idac).

#### Soft-Connect Procedure:

Determine the appropriate polarity for  $Chn\_a\_idac\_pol$ . Select  $Chn\_a\_idac\_pol = 1$  if incrementing  $V_{OUTn}$  causes differential voltage ( $VINn\_AP - VINn\_AM$ ) to increase. When properly programmed, lowering the value in  $Chn\_a\_idac[7:0]$  will always cause the output of the controlled power supply to decrease.

Ensure that the channel's IDAC is not currently enabled for connection, i.e., the  $Chn\_a\_idac\_en$  bit must be 0.

Update  $CHn\_A\_IDAC()$  with  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con = 0$ ,  $Chn\_a\_idac\_en = 1$ , and  $Chn\_a\_idac[7:0] = 0x80$ . The value programmed into  $Chn\_a\_idac[7:0]$  is ignored and  $Chn\_a\_idac[7:0]$  is initially set to 8'h80.

The LTC2970 will now ramp  $Chn\_a\_idac[7:0]$  while monitoring the output of the soft connect comparator. If the soft connect comparator trips, the LTC2970 will connect the output of  $V_{BUFn}$  to  $V_{OUTn}$  and set  $Chn\_a\_idac\_con$  high. If the soft connect comparator does not trip before the IDAC value reaches 'h00 or 'hFF, then the soft connection will fail, an IDAC fault will be indicated (Fault\_chn\_a\_idac), and  $Chn\_a\_idac\_con$  will remain low.

#### Soft-Connect Rules:

When both channels are requesting a soft connect, channel 0 has priority.

Soft connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$  or  $Chn\_a\_idac[7:0]$  if the LTC2970 is servicing a previously issued soft connect

on that channel or the previously issued soft connect failed with an IDAC fault (Fault\_chn\_a\_idac = 1). Recall that the  $Chn\_a\_idac\_en$  bit must initially have been set to 0.

*LTC2970-1 Only:* Soft connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$  or  $Chn\_a\_idac[7:0]$  if  $GPIO\_CFG$  is high and either  $GPIO\_0$  or  $GPIO\_1$  are high.

*LTC2970-1 Only:* Soft connect requests will be ignored and the user will not be able to change the  $Chn\_a\_idac\_pol$  bit if there is a pending tracking operation.

### 6. Hard Connecting the LTC2970 to the Power Supply Trim Pin

The hard connect feature allows the LTC2970 to bypass the soft connect algorithm and connect directly to the power supply's feedback node using the value programmed into  $Chn\_a\_idac[7:0]$ . This feature is useful for systems that have calculated or measured an acceptable voltage at which to connect the IDAC's buffered voltage  $V_{BUFn}$  to  $V_{OUTn}$ .

#### Hard Connect Procedure:

Determine the appropriate polarity for  $Chn\_a\_idac\_pol$ . Select  $Chn\_a\_idac\_pol = 1$  if incrementing  $V_{OUTn}$  causes ( $VINn\_AP - VINn\_AP$ ) to increase. When properly programmed, lowering the value in the IDAC will always cause the output of the controlled power supply to decrease.

Determine the value for  $Chn\_a\_idac[7:0]$ . The values 'h00 or 'hff are allowed, but they will trip the IDAC's fault bit (Fault\_chn\_a\_idac = 1).

When the IDAC is already connected, the value  $Chn\_a\_idac[7:0]$  and  $Chn\_a\_idac\_pol$  will be programmed into the IDAC provided all other conditions are met. See "Programming a Previously Connected Current DAC" for details

Update  $CHn\_A\_IDAC()$  with  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con = 1$ ,  $Chn\_a\_idac\_en = 1$ , and  $Chn\_a\_idac[7:0]$ .

#### Hard Connect Rules:

Hard connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con$  or  $Chn\_a\_idac[7:0]$  if the LTC2970 is servicing a previously issued soft connect on that channel or the previously issued

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soft connect failed with an IDAC fault (Fault\_chn\_a\_idac = 1). Recall that a new hard connection requires the previous value of Chn\_a\_idac\_en = 0.

*LTC2970-1 Only:* Hard connect requests will be ignored and the user will not be able to change Chn\_a\_idac\_pol, Chn\_a\_idac\_con or Chn\_a\_idac[7:0] if GPIO\_CFG is high and either GPIO\_0 or GPIO\_1 are high.

*LTC2970-1 Only:* Hard connect requests will be ignored and the user will not be able to change Chn\_a\_idac\_pol, Chn\_a\_idac\_con or Chn\_a\_idac[7:0] if there is a pending tracking operation.

### 7. Programming a Previously Connected IDAC

The LTC2970 IDAC's may be programmed after they have been connected with a soft connect or a hard connect provided a servo operation is not enabled on the associated channel.

#### *Procedure:*

Determine the value for Chn\_a\_idac[7:0]. The values 'h00 or 'hff are allowed, but will trip the IDAC's fault bit (Fault\_chn\_a\_idac = 1).

Verify that the IDAC is already connected, and that Chn\_a\_idac\_con is high.

Ensure that servo mode is not enabled for the channel being programmed. Chn\_a\_servo\_en must be low. This requirement prevents the user from interfering with a previously requested servo operation.

Update the CHn\_A\_IDAC() register with Chn\_a\_idac\_pol, Chn\_a\_idac\_con = 1, Chn\_a\_idac\_en = 1, and Chn\_a\_idac[7:0].

*Note:* Care should be taken to preserve the current value of the Chn\_a\_idac\_pol bit, since the LTC2970 does not prevent the user from changing this value when writing to the IDAC control registers.

#### *Rules:*

Setting Chn\_a\_idac\_con to zero will not disconnect the DAC unless Chn\_a\_idac\_en is also set low.

All Hard Connect rules apply.

### 8. Disconnecting the LTC2970 from the Power Supply Trim Pin

$V_{OUTn}$  can be placed in a high impedance state simply by clearing the Chn\_a\_idac\_en bit. In order to minimize the resulting disturbance to the power supply voltage, the IDAC code should not be changed from its current value when clearing the Chn\_a\_idac\_en bit. This is not an issue if the channel's associated servo\_en bit is high.

#### *Disconnect Procedure:*

Update CHn\_IDAC() with Chn\_a\_idac\_en set low.

The LTC2970 will immediately disconnect the buffered  $I_{OUTn}$  from  $V_{OUTn}$ .

#### *Disconnect Rules:*

Clearing Chn\_a\_idac\_con with Chn\_a\_idac\_en high will not disconnect the IDAC. Only setting Chn\_a\_idac\_en low will clear Chn\_a\_idac\_con.

*LTC2970-1 Only:* Chn\_a\_idac\_en may not be changed if the feedback node connection is configured for tracking. Tracking is enabled when GPIO\_CFG is high and either GPIO\_0 or GPIO\_1 are high.

### 9. Tracking Power Supplies Overview (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C interface to initiate a controlled power up or power down of two or more supplies (Figure 2 shows a typical LTC2970-1 application circuit). Multiple LTC2970-1's with different addresses may be simultaneously programmed using the LTC2970 group address and the SYNC() command. Tracking is enabled when GPIO\_CFG is pulled high and either GPIO\_0 or GPIO\_1 are high.

### 10. Tracking Power Supplies On (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C to initiate a controlled power up of two or more supplies.

*Procedure:* This procedure describes all the steps necessary to track up two or more power supplies. Steps that require I<sup>2</sup>C interaction are prefixed with the required I<sup>2</sup>C command function.

Power-up the LTC2970-1 with GPIO\_CFG pulled high.

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This causes open-drain outputs GPIO\_1 and GPIO\_0 to automatically pull the power supplies' run/soft-start pins to ground.

**CH<sub>n</sub>\_A\_IDAC():** Hard connect Ch<sub>n</sub>\_a\_idac[7:0] with a value that forces the power supplies off when GPIO\_CFG = 1. Verify that Ch<sub>n</sub>\_a\_idac\_pol is at the appropriate value.

**CH<sub>n</sub>\_A\_IDAC\_TRACK():** Set Ch<sub>n</sub>\_a\_idac\_track\_en = 1, and set the Ch<sub>n</sub>\_a\_idac\_track[7:0] target value to the code that causes V<sub>OUT<sub>n</sub></sub> to most closely approximate the corresponding power supply's feedback node voltage when it is in regulation.

**CH<sub>n</sub>\_A\_DELAY\_TRACK():** Set the value by which the incrementing of IDAC<sub>n</sub> should be delayed with respect to the start of tracking event. This controls whether the power supplies track up coincidentally or sequentially.

**IO():** Release the run/soft-start pins by programming io\_gpio\_n = 1. This will enable the power supplies without allowing their outputs to move since these are held low by Ch<sub>n</sub>\_a\_idac[7:0]. Wait until power supplies have had sufficient time to start running before starting tracking.

**SYNC():** Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync\_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io\_track\_start = 1. The LTC2970-1 will timeout this wait command after t<sub>TIMEOUT\_SYNC</sub>. Reading back Sync\_track = 1 using the global address will ensure all LTC2970-1's are synchronized before proceeding with the tracking operation.

**IO():** Set lo\_track\_start = 1 and keep the run/soft-start pins enabled. Use the global I<sup>2</sup>C address to simultaneously track up power supplies across multiple LTC2970-1's.

**LTC2970-1 response:** For each tracking enabled channel, the LTC2970-1 will decrement the CH<sub>n</sub>\_A\_delay\_track counter at a rate of t<sub>DEC\_TRACK</sub>. As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of Ch<sub>n</sub>\_a\_idac[7:0] by one count until the final value of Ch<sub>n</sub>\_a\_idac\_track[7:0] is reached, at which point Ch<sub>n</sub>\_a\_idac\_track\_en is de-asserted. When the final value is reached for all channels, GPIO\_CFG is asserted low. After a time delay of t<sub>HOLD\_TRACK</sub>, Ch<sub>n</sub>\_a\_idac\_en is de-asserted.

### Power-Up Tracking Rules:

Tracking cannot begin if Ch<sub>n</sub>\_a\_idac\_con is not connected. This condition is met when the previous procedure is followed.

Ch<sub>n</sub>\_a\_idac\_track\_pol, Ch<sub>n</sub>\_a\_idac\_track\_en, and ch0\_idac[7:0] updates will be ignored after IO(lo\_track\_start) is asserted until tracking is complete or whenever tracking is pending, i.e., GPIO\_CFG pulled high with either GPIO\_0 or GPIO\_1 asserted pulled high.

## 11. Tracking Power Supplies Off (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C to initiate a controlled power down of two or more supplies.

**Procedure:** This procedure describes all steps necessary to track down two or more power supplies. Steps that require I<sup>2</sup>C interaction are prefixed with the required I<sup>2</sup>C command function.

**CH<sub>n</sub>\_IDAC():** Disable the IDAC's for each tracking enabled channel (Ch<sub>n</sub>\_a\_idac\_en = 0). Ensure Ch<sub>n</sub>\_a\_idac\_pol is at the appropriate value.

**CH<sub>n</sub>\_IDAC\_TRACK():** Select the channels to be tracked by setting Ch<sub>n</sub>\_a\_idac\_track\_en = 1, and set the target value for each Ch<sub>n</sub>\_a\_idac\_track[7:0] to that which forces the supply off.

**CH<sub>n</sub>\_A\_DELAY\_TRACK():** Set the value by which the decrementing of that channel's DAC should be delayed with respect to the start of the tracking event. This controls whether the supplies track down coincidentally or sequentially.

**SYNC():** Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync\_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io\_track\_start = 1. The LTC2970-1 will timeout this wait command after t<sub>TIMEOUT\_SYNC</sub>. Reading back Sync\_track = 1 using the global address will ensure all LTC2970's are synchronized before proceeding with the tracking operation.

**IO():** Set lo\_track\_start = 1. Use the global I<sup>2</sup>C address to simultaneously track down power supplies across multiple LTC2970's.

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LTC2970-1 response: Each tracking enabled channel is soft connected. The GPIO\_CFG pin is released allowing it to be pulled high. The LTC2970-1 waits  $t_{\text{SETUP\_TRACK}}$  to allow GPIO\_CFG to settle. For each tracking enabled channel, the  $\text{Chn\_a\_delay\_track}$  counter is decremented at a rate of  $t_{\text{DEC\_TRACK}}$ . As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of  $\text{Chn\_a\_idac}[7:0]$  by one count until the final value of  $\text{Chn\_a\_idac\_track}[7:0]$  is reached. The tracking enable bit is then cleared for both channels ( $\text{Chn\_a\_idac\_track\_en} = 0$ ).

IO(): The I<sup>2</sup>C interface may then be used to set GPIO\_1 and GPIO\_0 low, disabling the power supplies.

### Power Down Tracking Rules:

Power down tracking requests will be ignored until the user has disabled the IDAC's by setting  $\text{Chn\_a\_idac\_en} = 0$  for each tracking enabled channel.

$\text{Chn\_a\_idac\_track\_pol}$ ,  $\text{Chn\_a\_idac\_track\_en}$ , and  $\text{ch0\_idac}[7:0]$  updates will be ignored after IO( $\text{IO\_track\_start}$ ) is asserted until tracking is complete and whenever tracking range is configured; (GPIO\_CFG high with either GPIO\_0 or GPIO\_1 asserted high).

## 12. Continuous Power Supply Voltage Servo

The continuous voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value. The voltage of the external supply is monitored over  $\text{Chn\_A\_ADC}$  and compared to a target value stored in  $\text{Chn\_a\_servo}$ . After each conversion,  $\text{Chn\_A\_IDAC}$  is incremented by 1, decremented by 1, or held; whichever brings or keeps the measured voltage closer to the targeted servo value.

### Procedure:

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating  $\text{CHN\_A\_IDAC}()$ ,  $\text{Chn\_a\_idac\_servo\_repeat}$  should be asserted high. The servo channel's IDAC must be enabled before  $\text{Chn\_A\_servo\_en}$  can be set high.

Determine the target servo voltage,  $\text{Chn\_a\_servo}[14:0]$ .

Update  $\text{CHN\_A\_SERVO}()$  with  $\text{Chn\_a\_servo\_en} = 1$ , and  $\text{Chn\_a\_servo}[14:0]$ .

Update  $\text{CHN\_A\_IDAC}()$  with  $\text{Chn\_a\_idac\_servo\_repeat} = 1$ . This step may be skipped if  $\text{Chn\_a\_idac\_servo\_repeat}$  was set high during the soft or hard connect procedure.

LTC2970 response: The LTC2970 will continuously increment, decrement or hold  $\text{Chn\_a\_idac}[7:0]$  in order to match the measured value of ( $\text{VIN}_n\text{-AP-VIN}_n\text{-AM}$ ) to  $\text{Chn\_a\_servo}[14:0]$ .

Whenever the  $\text{CHN\_A\_SERVO}()$  register is updated an internal flag is cleared indicating that a successful servo has not been completed. This internal flag,  $\text{Chn\_a\_servo\_done}$ , initially causes the ADC to operate in an accelerated 12-bit mode. Once the channel reaches the servo target, the ADC switches back to 14-bit mode for two conversions before asserting  $\text{Chn\_a\_servo\_done}$  high.

In continuous voltage servo mode the  $\text{Chn\_a\_servo\_done}$  flags allow the initial servo target to be reached quickly. During this time, ADC conversions for all non-servo channels are temporarily inhibited.

### Rules:

The IDAC associated with the servo channel must be enabled. If  $\text{Chn\_a\_idac\_en}$  is low the servo enable bit  $\text{Chn\_a\_servo\_en}$  is always forced low.

The IDAC associated with the servo channel must be connected ( $\text{Chn\_a\_idac\_con} = 1$ ).

An IDAC fault may be generated during a continuous servo operation. The LTC2970 will report the fault and continue trying to servo that channel.

*LTC2970-1 Only:* There must be no pending tracking commands. A pending tracking command will clear  $\text{Chn\_a\_servo\_en}$ .

*LTC2970-1 Only:* The tracking range must not be enabled; (GPIO\_CFG high with either GPIO\_0 or GPIO\_1 asserted high). An enabled tracking range will clear  $\text{Chn\_a\_servo\_en}$  low.



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### 13. One Time Power Supply Voltage Servo

The one time voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value and then stop updating the IDAC once the target value has been reached.

#### *Procedure:*

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating `CHn_A_IDAC()`, `Chn_a_idac_servo_repeat` should be de-asserted low. The servo channel's IDAC must be enabled before `Chn_a_servo_en` may be set high.

Update `CHn_A_IDAC()` with `Chn_a_idac_servo_repeat = 0`. This step may be skipped if `Chn_a_idac_servo_repeat` was cleared low during the soft or hard connect procedure.

Update `FAULT_EN()` with `Fault_en_chn_a_servo = 0`. This prevents the LTC2970 from reinitiating a servo after an overvoltage or undervoltage fault.

Determine the target servo voltage, `Chn_a_servo[14:0]`.

Update `CHn_A_SERVO()` register with `Chn_a_servo_en = 1`, and `Chn_a_servo[14:0]`.

**LTC2970 response:** The LTC2970 will increment, decrement or hold `Chn_a_idac[7:0]` in order to match the measured value of (`VINn_AP-VINn_AM`) to `Chn_a_servo[14:0]`. The servo procedure will end when the internal `Chn_a_servo_done` flag is set (see "Continuous Power Supply Voltage Servo"). At this point the IDAC is either programmed to the appropriate servo value or faulted.

#### *Rules:*

All "Continuous Power Supply Voltage Servo" rules apply.

### 14. One Time Power Supply Voltage Servo with Repeat On Fault

The LTC2970 one time voltage servo feature may be modified to allow the LTC2970 to perform an additional power supply servo operation after an undervoltage or overvoltage fault is detected on the servo channel.

#### *Procedure:*

Follow procedure outlined for "One Time Power Supply Voltage Servo".

Update `FAULT_EN()` with `Fault_en_chn_a_servo = 1`.

Enable detection of the appropriate instantaneous faults for all servo channels; see "Generating and Monitoring Instantaneous Faults".

**LTC2970 response:** Any time an instantaneous undervoltage or overvoltage fault is detected on the servo channel (`Fault_ov_a_chn` or `Fault_uv_a_chn`), the internal `Chn_a_servo_done` flag for that channel is cleared, and the LTC2970 will perform a complete one time servo. This allows the LTC2970 to precisely restore the power supply to the target servo value, after it has drifted beyond a user defined operating window.

#### *Rules:*

All "Continuous Power Supply Voltage Servo" rules apply.

During a permanent undervoltage or overvoltage fault the LTC2970 will continuously try to correct the faulted channel, after each failed attempt all other channels that need monitoring by the ADC will be serviced.

### 15. Configuring ADC to Monitor Input Channels and Internal Temperature Sensor

The LTC2970 is able to perform ADC conversions on any combination of seven different input channels. A channel is converted if its associated `ADC_MON()` bit is set high. Refer to Table 7 for details.

#### *Procedure:*

Update `ADC_MON()` with the control bit of each channel that is to be monitored set high.

**LTC2970 response:** All enabled channels will be sequentially converted. The result of the most recent conversion may be read from the ADC result register. Each time a conversion is completed the new data bit associated with the result register is asserted high. The new data bit is reset each

## OPERATION

**Table 7. LTC2970 ADC Conversion and Fault Limit Registers**

INPUT CHANNEL	ADC_MON() CONTROL BIT	ADC RESULT REGISTER (2s COMPLEMENT)	OV FAULT REGISTER (2s COMPLEMENT)	UV FAULT REGISTER (2s COMPLEMENT)
TEMPERATURE	Adc_mon_temp	Temp_adc[14:0]	-	-
VIN1_BP-VIN1_BM	Adc_mon_b_ch1	Ch1_b_adc[14:0]	Ch1_b_ov[14:0]	Ch1_b_uv[14:0]
VIN1_AP-VIN1_AM	Adc_mon_a_ch1	Ch1_a_adc[14:0]	Ch1_a_ov[14:0]	Ch1_a_uv[14:0]
VINO_BP-VINO_BM	Adc_mon_b_ch0	Ch0_b_adc[14:0]	Ch0_b_ov[14:0]	Ch0_b_uv[14:0]
VINO_AP-VINO_AM	Adc_mon_a_ch0	Ch0_a_adc[14:0]	Ch0_a_ov[14:0]	Ch0_a_uv[14:0]
12VIN	Adc_mon_v12	V12_adc[14:0]	V12_ov[14:0]	V12_uv[14:0]
VDD	Adc_mon_vdd	Vdd_adc[14:0]	Vdd_ov[14:0]	Vdd_uv[14:0]

time the result register is read. This provides a simple mechanism for supervisory software to determine if a new conversion has been completed since data was last read.

### Rules:

The LTC2970 assigns priority to ADC conversions of CH1\_A\_ADC and CH0\_A\_ADC when these channels are in their initial fast servo mode.

The IO() register control bit lo\_i2c\_adc\_wen must be low in order for ADC conversions to be performed.

*LTC2970-1 Only:* ADC conversions are suspended during any pending tracking requests.

## 16. Generating and Monitoring Instantaneous Faults

The LTC2970 supports fourteen different types of instantaneous faults. These faults together with the conditions that trigger them are defined in Table 8. There are six undervoltage faults, six overvoltage faults and two IDAC limit faults. The FAULT() command may be used to read the status of all instantaneous fault bits. The IO() command may be used to configure GPIO\_0 and GPIO\_1 to view voltage limit and IDAC faults respectively. The state of GPIO\_0 and GPIO\_1 may be read using IO().

**Table 8. LTC2970 Fault Reporting Bits and Conditions**

CONDITION THAT GENERATES AN INSTANTANEOUS FAULT	FAULT() INSTANTANEOUS FAULT REPORTING	FAULT_EN() ENABLE FOR LATCHED FAULT REPORTING	FAULT_LA() LATCHED FAULT REPORTING
V12_adc[14:0] < V12_uv[14:0]	Fault_v12_uv	Fault_en_v12_uv	Fault_la_v12_uv
V12_adc[14:0] > V12_ov[14:0]	Fault_v12_ov	Fault_en_v12_ov	Fault_la_v12_ov
Vdd_adc[14:0] < Vdd_uv[14:0]	Fault_vdd_uv	Fault_en_vdd_uv	Fault_la_vdd_uv
Vdd_adc[14:0] > Vdd_ov[14:0]	Fault_vdd_ov	Fault_en_vdd_ov	Fault_la_vdd_ov
Ch1_b_adc[14:0] < Ch1_b_uv[14:0]	Fault_ch1_b_uv	Fault_en_ch1_b_uv	Fault_la_ch1_b_uv
Ch1_b_adc[14:0] > Ch1_b_ov[14:0]	Fault_ch1_b_ov	Fault_en_ch1_b_ov	Fault_la_ch1_b_ov
Idac_a_ch1[7:0] = 8'ff or 8'h00	Fault_ch1_a_idac	Fault_en_ch1_a_idac	Fault_la_ch1_a_idac
Ch1_a_adc[14:0] < Ch1_a_uv[14:0]	Fault_ch1_a_uv	Fault_en_ch1_a_uv	Fault_la_ch1_a_uv
Ch1_a_adc[14:0] > Ch1_a_ov[14:0]	Fault_ch1_a_ov	Fault_en_ch1_a_ov	Fault_la_ch1_a_ov
Ch0_b_adc[14:0] < Ch0_b_uv[14:0]	Fault_ch0_b_uv	Fault_en_ch0_b_uv	Fault_la_ch0_b_uv
Ch0_b_adc[14:0] > Ch0_b_ov[14:0]	Fault_ch0_b_ov	Fault_en_ch0_b_ov	Fault_la_ch0_b_ov
Idac_a_ch0[7:0] = 8'ff or 8'h00	Fault_ch0_a_idac	Fault_en_ch0_a_idac	Fault_la_ch0_a_idac
Ch0_a_adc[14:0] < Ch0_a_uv[14:0]	Fault_ch0_a_uv	Fault_en_ch0_a_uv	Fault_la_ch0_a_uv
Ch0_a_adc[14:0] > Ch0_a_ov[14:0]	Fault_ch0_a_ov	Fault_en_ch0_a_ov	Fault_la_ch0_a_ov