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Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
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2-Channel PMBus Power System Manager Featuring Programmable Power Good Outputs

FEATURES

- **Sequence, Trim, Margin and Supervise Two Power Supplies**
- **Manage Faults, Monitor Telemetry**
- **PMBus Compliant Command Set**
- **Supported by LTpowerPlay® GUI**
- **Margin or Trim Supplies to Within 0.25% of Target**
- **Monitor Input Current (±1%) and Accumulate Energy**
- **Fast OV/UV Supervisors per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple ADI PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously Without Additional Software**
- **Configurable Power Good Output Pins**
- Accurate Monitoring of Output Voltage, Output Current, Temperature, and Input Voltage and Current
- 1.8V to 3.3V I^2C/SMBus Serial Interface
- Connect Directly to Regulator IMON Pins
- Can Be Powered from 3.3V, or 4.5V to 15V
- Available in 44-Pin 6mm × 7mm QFN Package

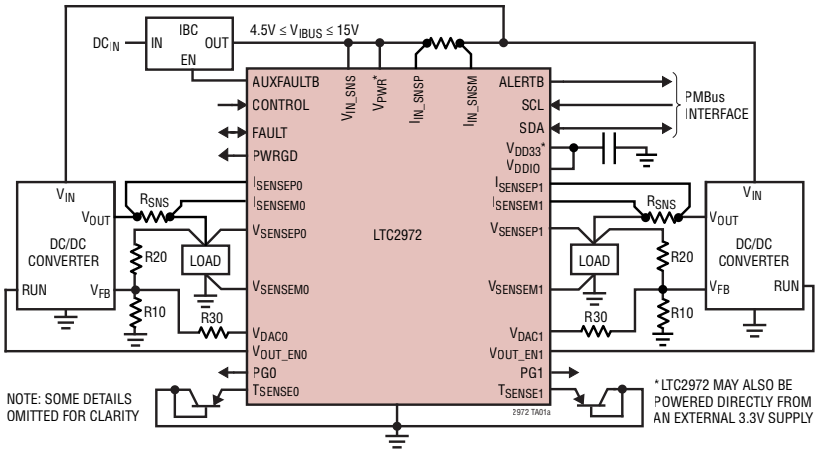
APPLICATIONS

- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Video and Medical Imaging

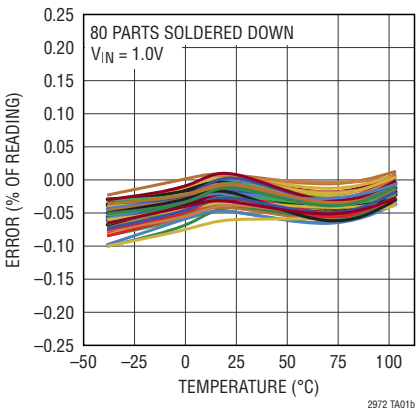
DESCRIPTION

The LTC®2972 is a 2-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under voltage and temperature threshold limits for two power supply output channels as well as over and under voltage threshold limits for a single power supply input channel. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors two output voltages, two output currents, two external temperatures, input voltage and current, and die temperature. Input power, energy, and output power are also calculated. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple ADI Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

TYPICAL APPLICATION



Closed-Loop Servo Error vs Temperature



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages:
- V_{PWR} ..... –0.3V to 15V
- V_{DD33} ..... –0.3V to 3.6V
- V_{DD25} ..... –0.3V to 2.75V

Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1, PG[1:0], V_{DDIO} ..... –0.3V to 3.6V
- PWRGD, SHARE_CLK, WDI/RESETB, WP, FAULTB0, FAULTB1 ..... –0.3V to 3.6V
- ASEL0, ASEL1 ..... –0.3V to 3.6V

Analog Voltages:
- REFP ..... –0.3V to 1.35V
- REFM ..... –0.3V to 0.3V
- V_{IN_SNS}, $V_{IN\_SNS\_CAP}$ ..... –0.3V to 15V
- I_{IN_SNSP}, I_{IN_SNSM} to V_{IN_SNS} ..... –0.3V to 0.3V
- $V_{SENSEP[1:0]}$ ..... –0.3V to 6V
- $V_{SENSEM[1:0]}$ ..... –0.3V to 6V
- $I_{SENSEP[1:0]}$ ..... –0.3V to 6V
- $I_{SENSEM[1:0]}$ ..... –0.3V to 6V
- $V_{OUT\_EN[1:0]}$, AUXFAULTB ..... –0.3V to 15V
- $V_{DAC[1:0]}$ ..... –0.3V to 6V
- $T_{SENSE[1:0]}$ ..... –0.3V to 3.6V
- I_{IN_SNSP}, I_{IN_SNSM} ..... –0.3V to 15V

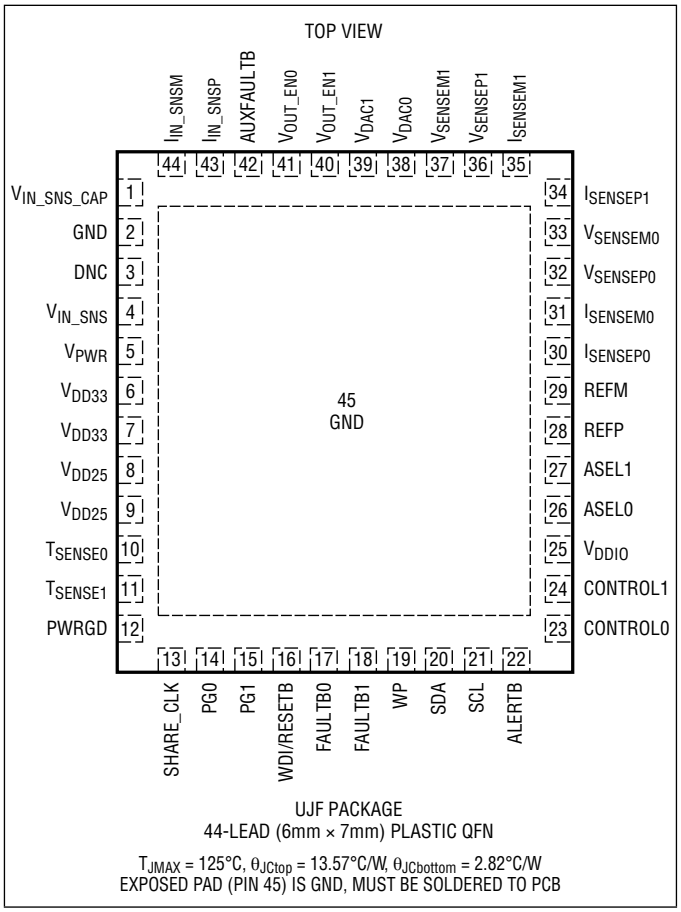
Operating Junction Temperature Range:
- LTC2972C ..... 0°C to 70°C
- LTC2972I ..... –40°C to 105°C

Storage Temperature Range ..... –65°C to 150°C*

Maximum Junction Temperature ..... 125°C*

*See OPERATION section for detailed EEPROM derating information for junction temperatures in excess of 105°C.

PIN CONFIGURATION



UJF PACKAGE
44-LEAD (6mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JCtop} = 13.57°C/W, $\theta_{JCbottom}$ = 2.82°C/W
EXPOSED PAD (PIN 45) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC2972#orderinfo

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC2972CUJF#PBF	LTC2972CUJF#TRPBF	LTC2972UJF	44-Lead (6mm × 7mm) Plastic QFN	0°C to 70°C
LTC2972IUJF#PBF	LTC2972IUJF#TRPBF	LTC2972UJF	44-Lead (6mm × 7mm) Plastic QFN	–40°C to 105°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range	V_{DD33} Floating	●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		6.7	9	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		6.7	9	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.25	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	75	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} applied until the TON_DELAY Timer Starts			30		ms
V_{DDIO}	V_{DDIO} Input Operating Range		●	1.62		3.6	V
R_{IN}	V_{DDIO} Input Resistance	0 ≤ V_{VDDIO} ≤ 3.6V	●	53	68.8	86	kΩ
Voltage Reference Characteristics							
V_{REF}	Output Voltage (Note 3)	V_{REF} = V_{REFP} – V_{REFM}, 0 < I_{REFP} < 100µA	●	1.216	1.228	1.240	V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 4)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = (V_{SENSEP}*n* – V_{SENSEM}*n*)	●	0		6	V
		Single-Ended Voltage: V_{SENSEM}*n*	●	–0.1		0.1	V
	Current Sense Input Range	Single-Ended Voltage: I_{SENSEP}*n*, I_{SENSEM}*n*	●	–0.1		6	V
		Differential Current Sense Voltage: V_{IN_ADC} = (I_{SENSEP}*n* – I_{SENSEM}*n*) Mfr_config_imon_sel = 0 Mfr_config_imon_sel = 1	 ● ●	 –170 –0.1		 170 6	 mV V
N_ADC	Voltage Sense Resolution	0V ≤ V_{IN_ADC} ≤ 6V, READ_VOUT			122		µV/LSB
	Current Sense Resolution with IOUT_CAL_GAIN = 1Ω	0mV ≤ |V_{IN_ADC}| < 16mV (Note 5) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}|			15.625 31.25 62.5 125 250		µA/LSB µA/LSB µA/LSB µA/LSB µA/LSB
TUE_ADC_VOLT_SNS	Total Unadjusted Error (Note 3)	Voltage Sense Inputs V_{IN_ADC} ≥ 1V	●			±0.25	% of Reading
		Voltage Sense Inputs 0 ≤ V_{IN_ADC} ≤ 1V	●			±2.5	mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TUE_ADC_ CURR_SNS	Total Unadjusted Error (Note 3)	Current Sense Inputs 20mV ≤ $\|V_{IN\_ADC}\|$ ≤ 170mV Mfr_config_imon_sel = 0	●			±0.3	% of Reading
		Current Sense Inputs $\|V_{IN\_ADC}\|$ ≤ 20mV Mfr_config_imon_sel = 0	●			±60	µV
		Current Sense Inputs V_{IN_ADC} ≥ 1V Mfr_config_imon_sel = 1	●			±0.25	% of Reading
		Current Sense Inputs 0 ≤ V_{IN_ADC} ≤ 1V Mfr_config_imon_sel = 1	●			±2.5	mV
V_{OS_ADC}	Offset Error	$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs, V_{OS} • IOUT_CAL_ GAIN, IOUT_CAL_GAIN = 1000mΩ Mfr_config_imon_sel = 0	●			±35	µV
t_{CONV_ADC}	Conversion Time	$V_{SENSEP}n$, $V_{SENSEM}n$, V_{IN_SNS} Inputs (Note 6)			6.15		ms
		$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs (Note 6) Mfr_config_imon_sel = 0			24.6		ms
		$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs (Note 6) Mfr_config_imon_sel = 1			6.15		ms
		Internal Temperature (READ_TEMPERATURE_2) (Note 6)			24.6		ms
t_{UPDATE_ADC}	Update Time	Mfr_ein_config_hd = 0 (Note 6)			135		ms
		Mfr_ein_config_hd = 1 (Note 6)			305		ms
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz
Sense Input Current Characteristics (Note 7)							
I_{IN_VSENSE}	Input Current	$V_{SENSEP}n$ and $V_{SENSEM}n$ Inputs	●			±15	µA
	Differential Input Current	$V_{SENSEP}n$ and $V_{SENSEM}n$ Inputs, V_{IN_DIFF} = 6V	●			±30	µA
I_{IN_ISENSE}	Input Current	$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs Mfr_config_imon_sel = 0	●			±1	µA
		$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs Mfr_config_imon_sel = 1	●			±4	µA
	Differential Input Current	$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs, $\|V_{IN\_DIFF}\|$ = 170mV Mfr_config_imon_sel = 0	●			±1	µA
		$I_{SENSEP}n$ and $I_{SENSEM}n$ Inputs, $\|V_{IN\_DIFF}\|$ = 6.0V Mfr_config_imon_sel = 1	●			±8	µA
DAC Output Characteristics							
N_V_{DAC}	Resolution				10		Bits
V_{FS_VDAC}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_0	●	1.3	1.38	1.44	V
		DAC Code = 0x3FF, DAC Polarity = 1, Buffer Gain Setting_1	●	2.5	2.65	2.77	V
INL_V_{DAC}	Integral Nonlinearity	(Note 8)	●			±2	LSB
DNL_V_{DAC}	Differential Nonlinearity	(Note 8)	●			±2.4	LSB
V_{OS_VDAC}	Offset Voltage	(Note 8)	●			±10	mV
V_{DAC}	Load Regulation	$V_{DAC}n$ = 2.65V, $I_{VDAC}n$ Sourcing = 2mA			100		ppm/mA
		$V_{DAC}n$ = 0.1V, $I_{VDAC}n$ Sinking = 2mA			100		ppm/mA
	PSRR	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}			60		dB
	Leakage Current	$V_{DAC}n$ Hi-Z, 0V ≤ $V_{DAC}n$ ≤ 6V	●			±100	nA
	Short-Circuit Current Low	$V_{DAC}n$ Shorted to GND	●	–12		–4	mA
	Short-Circuit Current High	$V_{DAC}n$ Shorted to V_{DD33}	●	4		12	mA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
C_{OUT}	Output Capacitance	V_{DACn} Hi-Z				10		pF
t_{S_VDAC}	DAC Output Update Rate	Fast Servo Mode				500		µs
Voltage Supervisor Characteristics								
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	Low Resolution Mode	●	0		6	V
			High Resolution Mode	●	0		3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$		●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode				4		mV/LSB
		0V to 6V Range: Low Resolution Mode				8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode		●			±1.25	% of Reading
		V_{IN_VS} ≤ 2V, Low Resolution Mode					±25	mV
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode		●			±1.0	% of Reading
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode		●			±1.5	% of Reading
		V_{IN_VS} ≤ 0.8V, High Resolution Mode					±12	mV
t_{S_VS}	Update Rate					12.21		µs
V_{IN_SNS} Input Characteristics								
V_{IN_SNS}	V_{IN_SNS} Input Voltage Range	(Note 9)		●	0		15	V
I_{VIN_SNS}	V_{IN_SNS} Input Current	V_{VIN_SNS} = 4.5V		●	80	140	200	µA
		V_{VIN_SNS} = 12V		●	150	250	350	µA
		V_{VIN_SNS} = 15V		●	180	300	420	µA
TUE_{VIN_SNS}	V_{IN_ON}, V_{IN_OFF} Threshold Total Unadjusted Error	4.5V ≤ V_{VIN_SNS} ≤ 8V		●			±2.0	% of Reading
		V_{VIN_SNS} > 8V		●			±1.0	% of Reading
TUE_VIN	READ_VIN Total Unadjusted Error	4.5V ≤ V_{VIN_SNS} ≤ 15V (Note 9)		●			±0.5	% of Reading
DAC Soft-Connect Comparator Characteristics								
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V		●		±1	±18	mV
		V_{DACPn} = 1.3V		●		±2	±26	mV
		V_{DACPn} = 2.65V		●		±3	±52	mV
Input Current Sense Characteristics								
V_{IIN}	Common Mode Input Range	V_{IIN_SNSP} = V_{IIN_SNSM} (Note 9)		●	4.5		15	V
I_{IIN}	I_{IIN_SNSP}, I_{IIN_SNSM} Input Current	V_{IIN_SNSP} = V_{IIN_SNSM} = V_{IIN_SNS} (Note 2)		●		0.5	2	µA
FS_IIN	Full-Scale Input Current Sense Voltage Range	Referred to (V_{IIN_SNSP} – V_{IIN_SNSM})	High Range	●	–100		100	mV
			Medium Range	●	–50		50	mV
			Low Range	●	–20		20	mV
TUE_IIN	Total Unadjusted Error	|V_{IIN_SNSP} – V_{IIN_SNSM}| = 100mV, High Range		●			±0.6	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 50mV, Medium Range		●			±0.65	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 20mV, Low Range		●			±0.75	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 20mV, High Range		●			±1	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 15mV, Medium Range		●			±1	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 10mV, Low Range		●			±1	% of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 0mV, High Range		●			±100	µV
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 0mV, Medium Range		●			±75	µV
		|V_{IIN_SNSP} – V_{IIN_SNSM}| = 0mV, Low Range		●			±50	µV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
CMRR_IIN	DC CMRR	4.5V ≤ V_{IIN_SNSP} = V_{IIN_SNS} ≤ 15V $\lvert V_{IIN\_SNSP} - V_{IIN\_SNSM} \rvert$ = 100mV High Range	●	85			dB
	AC CMRR	V_{IIN_SNSP} = V_{IIN_SNS}= 12V ± 100mV f = 62.5kHz			85		dB
t_{CONV_IIN}	Conversion Time				25		ms
t_{UPDATE}	Update Rate				5.4		Hz
External Temperature Sensor Characteristics (READ_TEMPERATURE_1)							
t_{CONV_TSENSE}	Conversion Time	For One Channel, (Total Latency for Both Channels Is 2 • 66ms)			66		ms
I_{TSENSE_HI}	T_{SENSE} High Level Current		●	–90	–64	–40	µA
I_{TSENSE_LOW}	T_{SENSE} Low Level Current		●	–5.5	–4	–2.5	µA
TUE_TS	Total Unadjusted Error	Ideal Diode Assumed			±3		°C
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP_1_GAIN = 1/N_TS				1.10	
Internal Temperature Sensor Characteristics (READ_TEMPERATURE_2)							
TUE_TS2	Total Unadjusted Error				±1		°C
V_{OUT} Enable Output ($V_{OUT\_EN\ [1:0]}$) Characteristics							
I_{VOUT_ENn}	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	3	5	8	mA
		V_{VOUT_ENn} = 0.4V	●	33	50	65	µA
	Output Leakage Current	0V ≤ V_{VOUT_ENn} ≤ 15V	●			±20	µA
V_{VOUT_VALID}	Minimum V_{DD33} when V_{OUT_ENn} Valid	V_{VOUT_ENn} ≤ 0.4V	●			1.1	V
General Purpose Output (AUXFAULTB) Characteristics							
$I_{AUXFAULTB}$	Output Sinking Current	Strong Pull-Down Enabled, $V_{AUXFAULTB}$ = 0.4V	●	3	5	8	mA
	Output Leakage Current	0V ≤ $V_{AUXFAULTB}$ ≤ 15V	●			±20	µA
Energy Meter Characteristics							
TUE_ETB	Energy Meter Time-Base Error		●			±1	% of Reading
TUE_PIN	READ_PIN Total Unadjusted Error	V_{IIN_SNSP} – V_{IIN_SNSM} = 50mV, Medium Range	●			±1	% of Reading
TUE_EIN	Energy Meter Total Unadjusted Error	V_{IIN_SNSP} – V_{IIN_SNSM} = 50mV, Medium Range	●			±2	% of Reading
EEPROM Characteristics							
Endurance	(Notes 10, 11)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 10, 11)	T_J < 105°C	●	20			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 12)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		200	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, PG0, PG1, WDI/RESETB, FAULTB0, FAULTB1, WP							
V_{IH}	Input High Threshold Voltage	1.62V ≤ V_{VDDIO} ≤ 3.6V	●	0.7 • V_{VDDIO}			V
V_{IL}	Input Low Threshold Voltage	1.62V ≤ V_{VDDIO} ≤ 3.6V	●			0.3 • V_{VDDIO}	V
V_{HYST}	Input Hysteresis	FAULTB*n*, CONTROL*n*, PG*n*, WDI/RESETB, WP			20		mV
		SDA, SCL			80		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SP}	Pulse Width of Spike Suppressed	FAULTB0, FAULTB1, CONTROL*n*			10		µs
		SDA, SCL			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			180			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB} \leq 1.5V$	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB} \leq 1.5V$	●	0.3		200	µs
f_{WDI}	Watchdog Timer Interrupt Input Frequency		●			1	MHz
C_{IN}	Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	$V_{SHARE\_CLK} < 0.8V$	●	0.825		1.11	µs
t_{RISE}	Rise Time	$V_{SHARE\_CLK} < 0.8V$ to $V_{SHARE\_CLK} > 1.6V$	●			450	ns
I_{LEAK}	Input Leakage Current	$0V \leq V_{SHARE\_CLK} \leq V_{DD33} + 0.3V$	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Digital Outputs SDA, ALERTB, SHARE_CLK, FAULTB0, FAULTB1, PWRGD, PG0, PG1							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
I_{HIZ}	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 13)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 13)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 13)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 13)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 13)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 13)		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 13)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2972 Receiving Data) (Note 13)		●	0			ns
	Data Hold Time (LTC2972 Transmitting Data) (Note 13)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 13)		●	100			ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33} = V_{DDIO}, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SP}	Pulse Width of Spike Suppressed (Note 13)				98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0 Mfr_config_all_longer_pmbus_timeout = 1	● ●		25 200	35 280	ms ms
Additional Digital Timing Characteristics							
t_{OFF_MIN}	Minimum Off-Time for Any Channel				100		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage (V_{REF}) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

Note 4: Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 5: The current sense resolution is determined by the L11 format, the value of IOUT_CAL_GAIN, and the magnitude of the current being measured. See Table 3 on page 77 for details.

Note 6: The nominal time between successive ADC conversions (latency of the ADC) for any given channel is t_{UPDATE_ADC}.

Note 7: V_{SENSE} and I_{SENSE} input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as ($I^+ – I^–$) where I^+ is the current into the positive device pin and $I^–$ is the current into the negative device pin.

Note 8: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 9: While READ_VIN operates with 0V ≤ V_{IN_SNS} ≤ 15V, the valid READ_IIN, READ_PIN, and MFR_EIN operating range is 4.5V ≤ V_{IN_SNS} ≤ 15V.

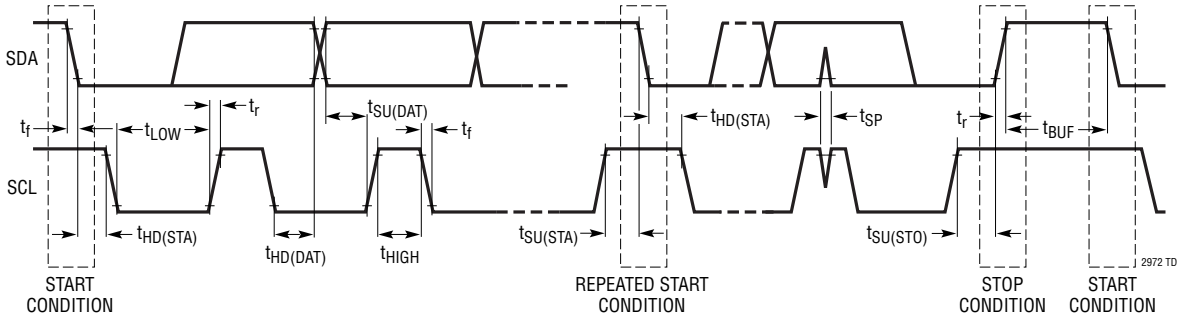
Note 10: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 11: EEPROM endurance and retention will be degraded when T_J > 105°C.

Note 12: The LTC2972 will not acknowledge any PMBus commands, except for MFR_COMMON, when a STORE_USER_ALL command is being executed. See also OPERATION section.

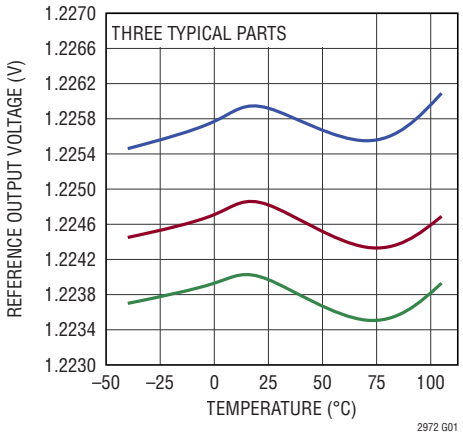
Note 13: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: (20 + 0.1• C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{DDIO}, is 1.35V < V_{DDIO} < 3.6V.

PMBUS TIMING DIAGRAM

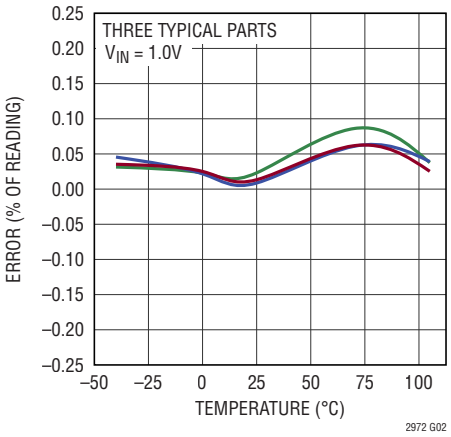


TYPICAL PERFORMANCE CHARACTERISTICS

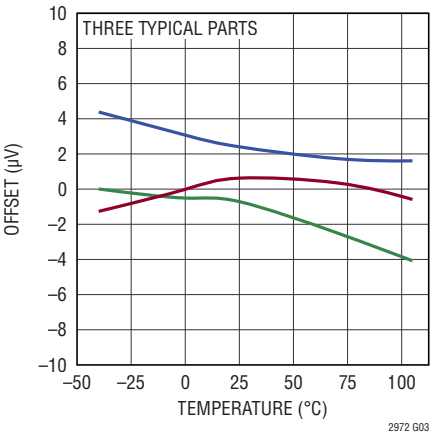
Reference Voltage vs Temperature



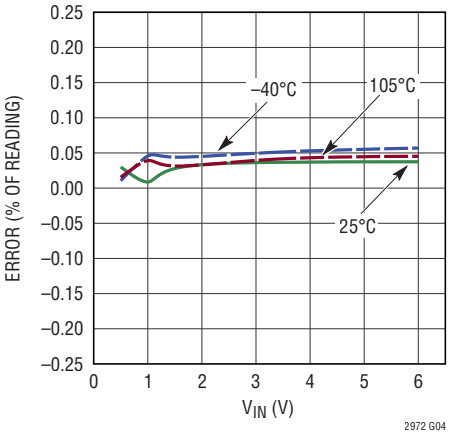
ADC READ_VOUT ADC Total Unadjusted Error vs Temperature



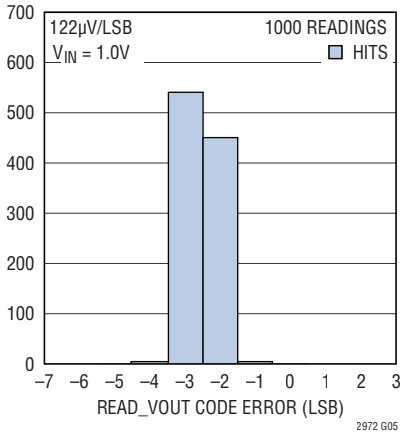
ADC READ_IOUT Input Referred Offset Voltage vs Temperature



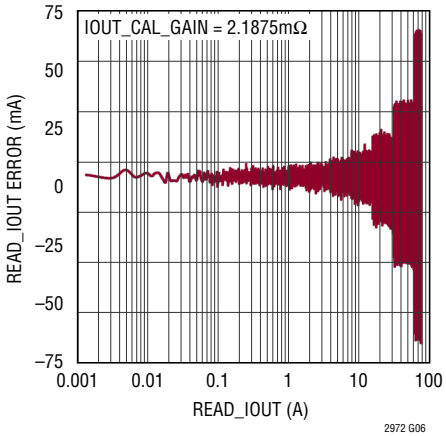
ADC READ_VOUT ADC Total Unadjusted Error vs Input Voltage



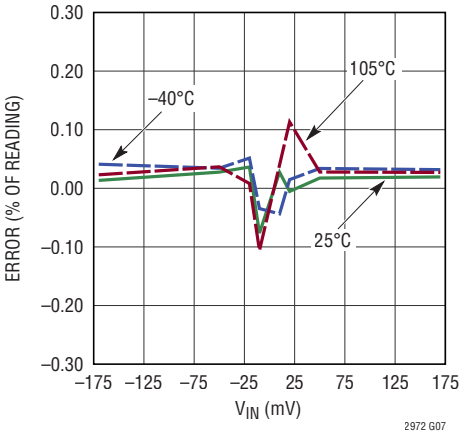
ADC READ_VOUT Noise Histogram



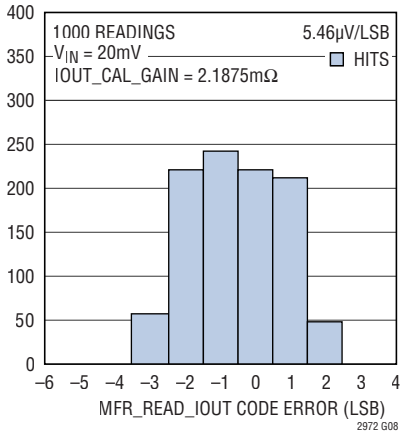
ADC READ_IOUT Error vs READ_IOUT



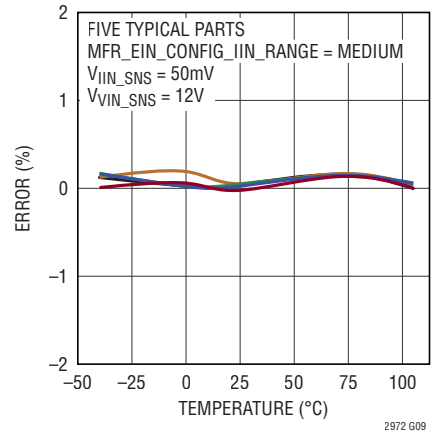
ADC MFR_READ_IOUT ADC Total Unadjusted Error vs Input Voltage



ADC MFR_READ_IOUT Noise Histogram

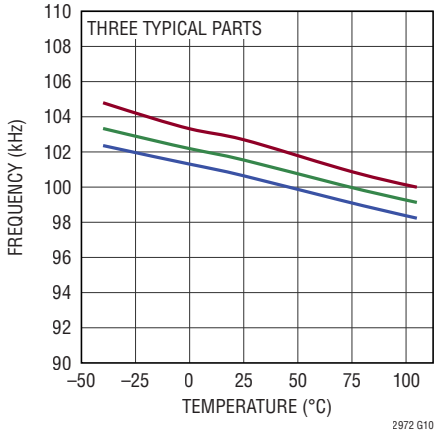


Power Measurement Error

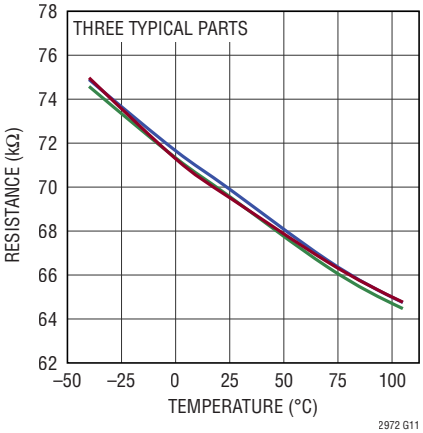


TYPICAL PERFORMANCE CHARACTERISTICS

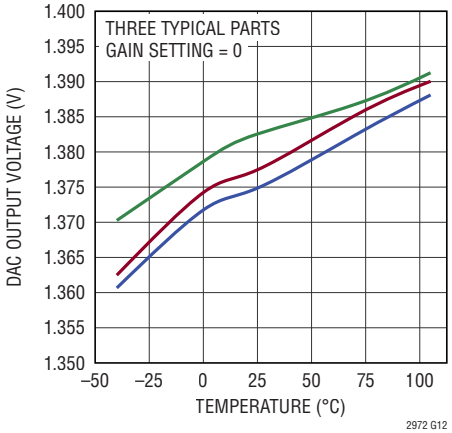
SHARE_CLK Output Frequency vs Temperature



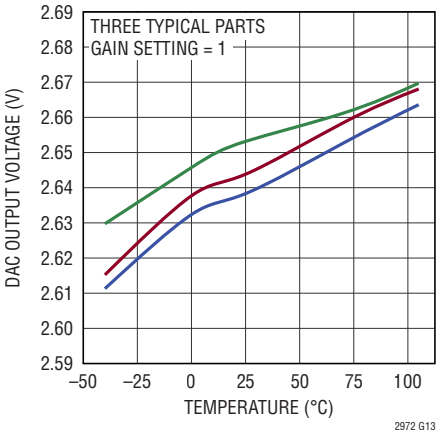
V_{DDIO} Input Resistance vs Temperature



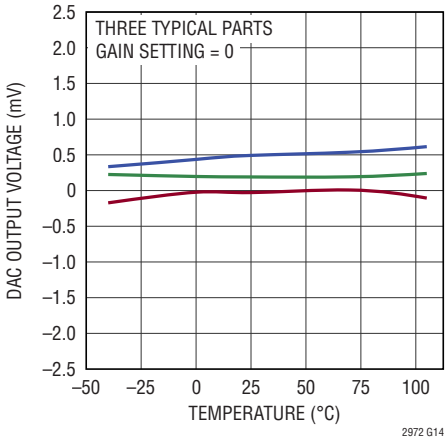
DAC Full-Scale Voltage vs Temperature, Gain Setting = 0



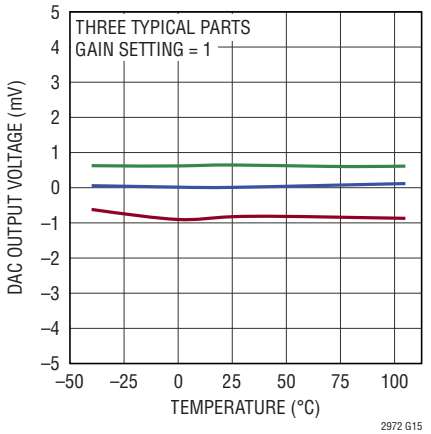
DAC Full-Scale Voltage vs Temperature, Gain Setting = 1



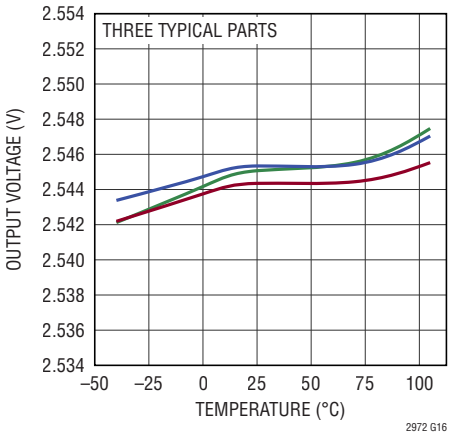
DAC Offset Voltage vs Temperature, Gain Setting = 0



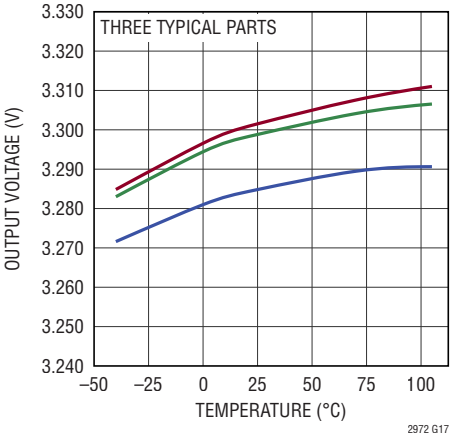
DAC Offset Voltage vs Temperature, Gain Setting = 1



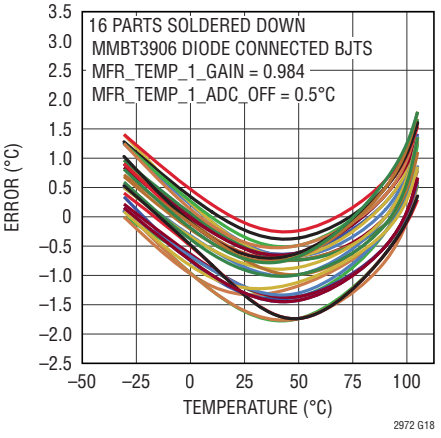
V_{DD25} Regulator Output Voltage vs Temperature



V_{DD33} Regulator Output Voltage vs Temperature

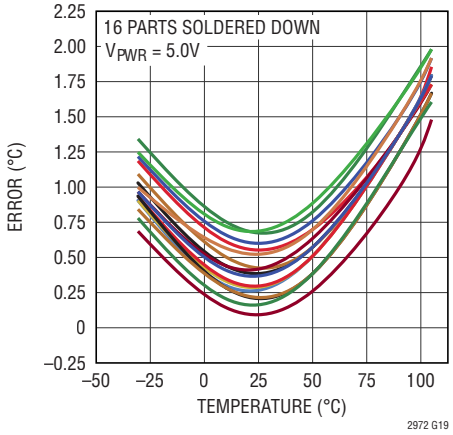


External Temperature READ_TEMPERATURE_1 Error vs Temperature

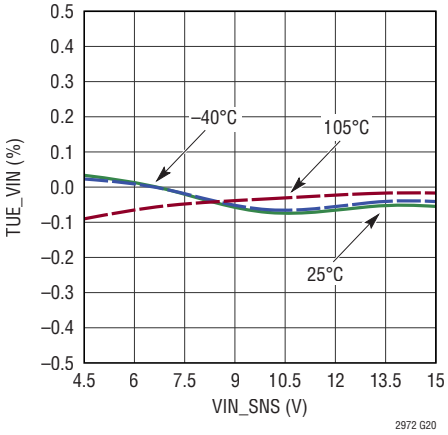


TYPICAL PERFORMANCE CHARACTERISTICS

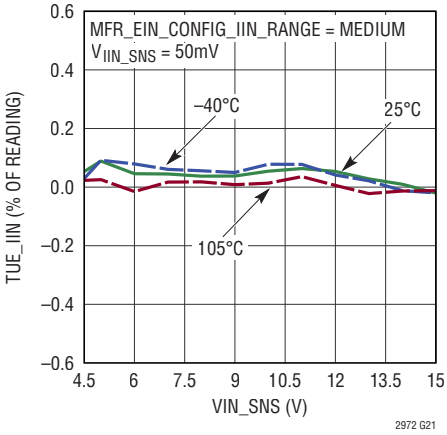
READ_TEMPERATURE_2 Error vs Temperature



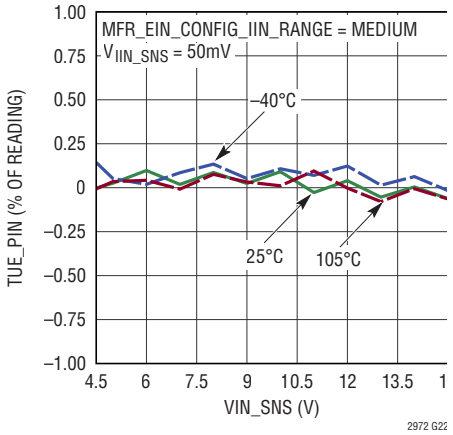
TUE_VIN vs VIN_SNS



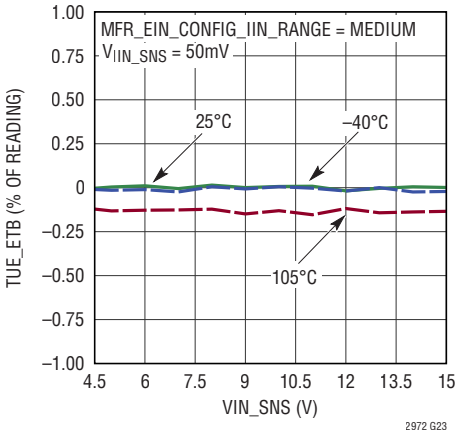
TUE_IIN vs VIN_SNS



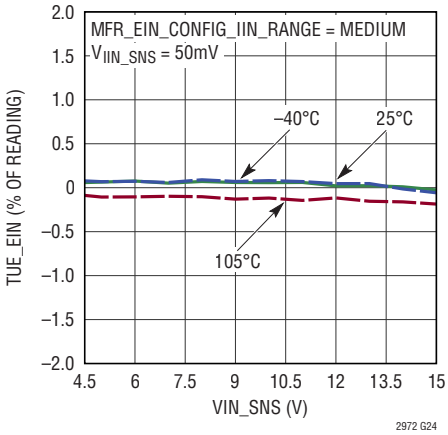
TUE_PIN vs VIN_SNS



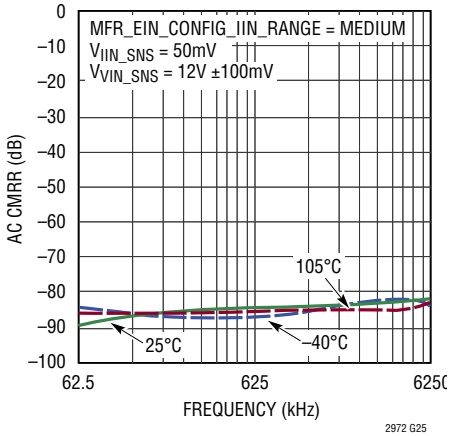
TUE_ETB vs VIN_SNS



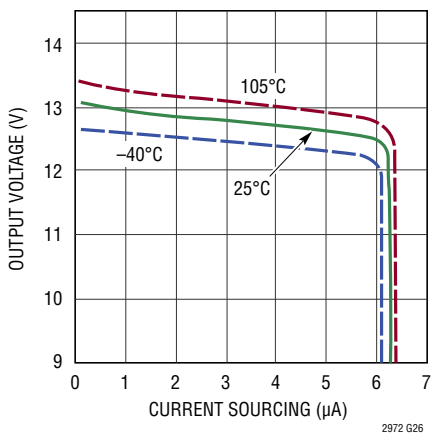
TUE_EIN vs VIN_SNS



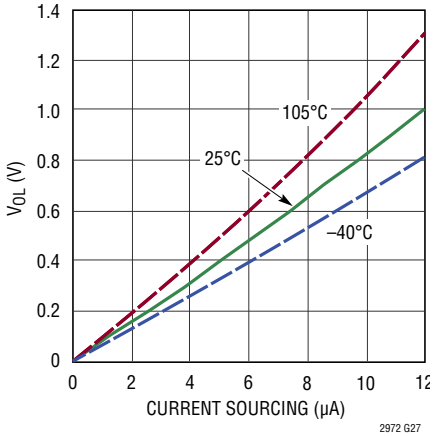
READ_IIN Common Mode Gain vs Frequency



$V_{OUT\_EN[0:1]}$ and AUXFAULTB Output High Voltage vs Load Current

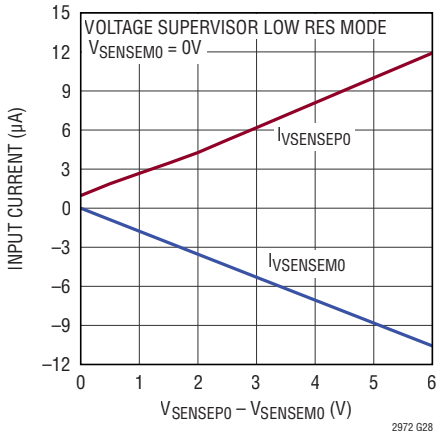


$V_{OUT\_EN[0:1]}$ and AUXFAULTB VOL vs Load Current

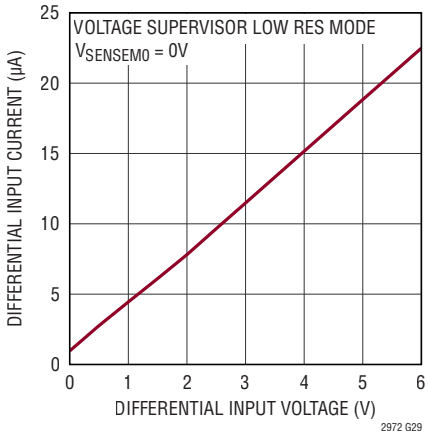


TYPICAL PERFORMANCE CHARACTERISTICS

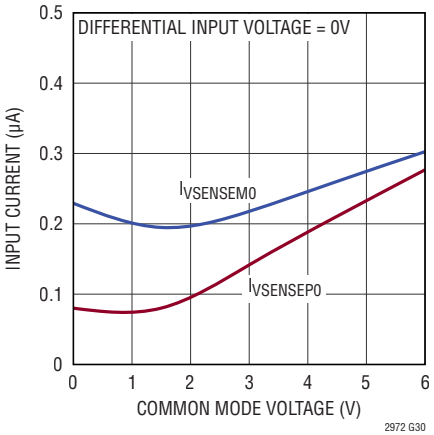
Voltage Sense Input Currents vs Differential Input Voltage



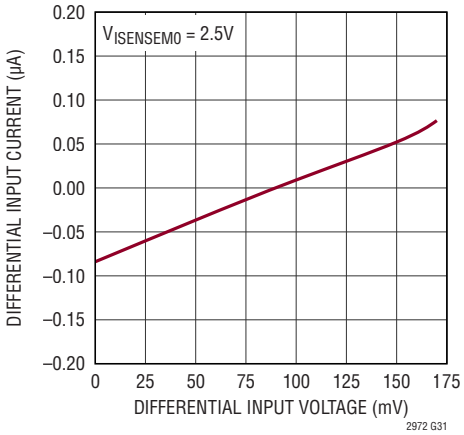
Voltage Sense Differential Input Current vs Differential Input Voltage



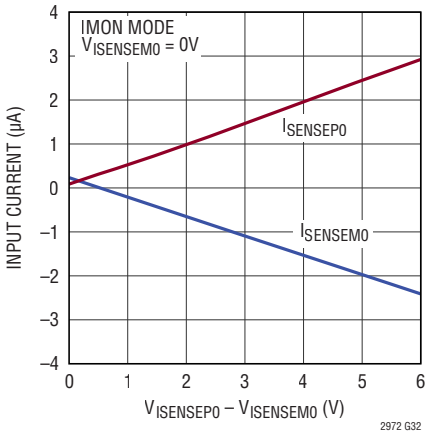
Current Sense Input Currents vs Common Mode Voltage



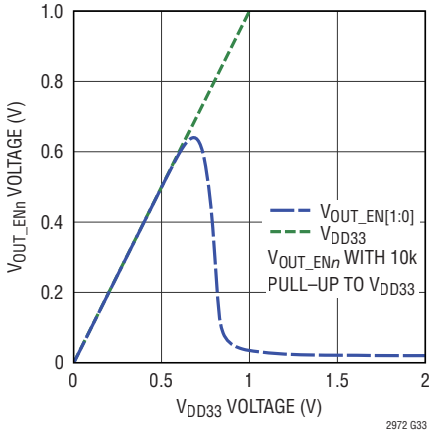
Current Sense Differential Input Current vs Differential Input Voltage



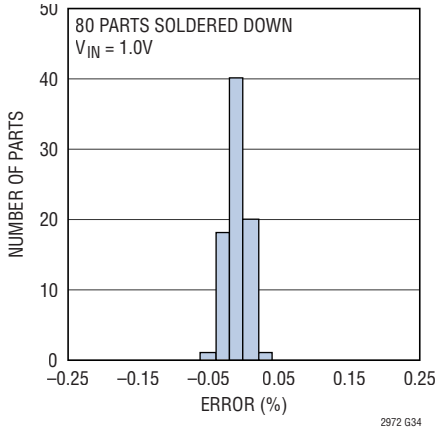
IMON Sense Input Currents vs Differential Input Voltage



$V_{OUT\_EN[1:0]}$ Output Voltage vs V_{DD33}



Closed-Loop Servo Error



PIN FUNCTIONS

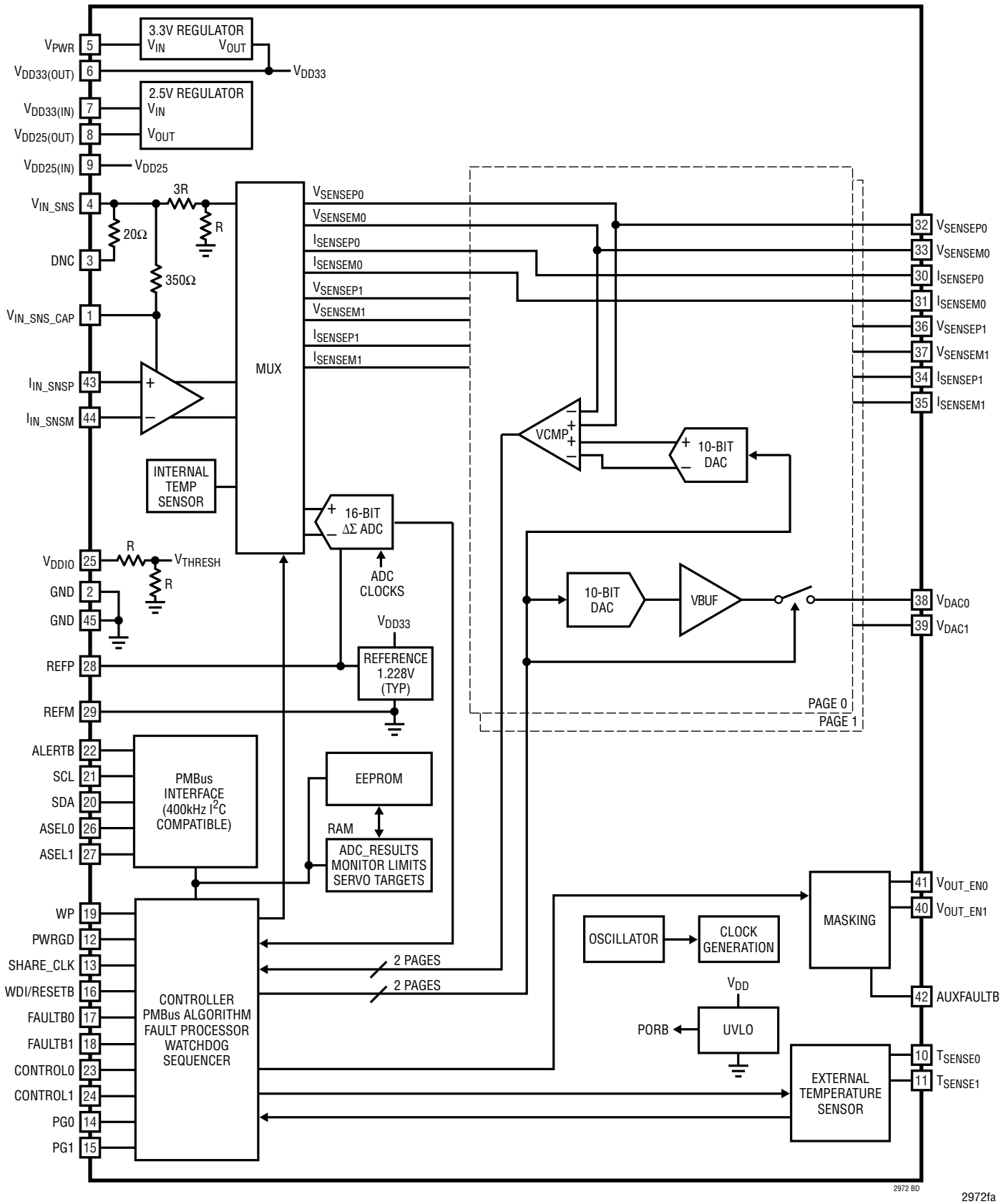
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$V_{SENSEP0}$	32*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	33*	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
V_{OUT_EN0}	41	Out	DC/DC Converter Enable-0 Pin.
V_{OUT_EN1}	40	Out	DC/DC Converter Enable-1 Pin.
AUXFAULTB	42	Out	Auxiliary Fault Output Pin. Can Be Configured to Pull Low When OV/UV Detected
DNC	3	Do Not Connect	Do Not Connect to this Pin
V_{IN_SNS}	4	In	V_{IN} SENSE Input. This Voltage is Compared Against the V_{IN} On and Off Voltage Thresholds In Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V_{PWR}	5	In	V_{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5 to 15V). If a 4.5V to 15V Supply Voltage Is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1µF Capacitor
V_{DD33}	6	In/Out	If Shorted to V_{PWR}, It Serves as 3.13 to 3.47V Supply Input Pin. Otherwise It Is a 3.3V Internally Regulated Voltage Output (Use 0.1µF Decoupling Capacitor to GND). If using the internal regulator to provide V_{DD33}, do not connect to V_{DD33} pins of any other devices
V_{DD33}	7	In	Input for Internal 2.5V Sub-Regulator. Short this Pin to Pin 6. If using the internal regulator to provide VDD33, do not connect to V_{DD33} pins of any other devices
V_{DD25}	8	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor. Do not connect to V_{DD25} pins of any other devices
V_{DD25}	9	In	2.5V Supply Voltage Input. Short this Pin to Pin 8. Do not connect to V_{DD25} pins of any other devices
T_{SENSE0}	10*	In/Out	External Temperature Current Output and Voltage Input for Channel 0. Maximum allowed capacitance is 1µF
T_{SENSE1}	11*	In/Out	External Temperature Current Output and Voltage Input for Channel 1. Maximum allowed capacitance is 1µF
PWRGD	12	Out	Power-Good Open Drain Output. Indicates When Selected Outputs Are Power Good. Can be Used as System Power-On Reset
SHARE_CLK	13	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49kΩ Pull-Up Resistor to V_{DD33}. Connect to all other SHARE_CLK pins in the system
PG0	14	In/Out	Configurable Open-Drain Output and Digital Input for Channel 0. Connect a 10kΩ Pull-Up Resistor to V_{DDIO}.
PG1	15	In/Out	Configurable Open-Drain Output and Digital Input for Channel 1. Connect a 10kΩ Pull-Up Resistor to V_{DDIO}
WDI/RESETB	16	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10kΩ Pull-Up Resistor to V_{DD33}. Rising Edge Resets Watchdog Counter. Holding this Pin Low for More than t_{RESETB} Resets the Chip
FAULTB0	17	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-0. Connect a 10kΩ Pull-Up Resistor to V_{DDIO}
FAULTB1	18	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-1. Connect a 10kΩ Pull-Up Resistor to V_{DDIO}
WP	19	In	Digital Input. Write-Protect Input Pin, Active High
SDA	20	In/Out	PMBus Bidirectional Serial Data Pin
SCL	21	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	22	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	23	In	Control Pin 0 Input
CONTROL1	24	In	Control Pin 1 Input
V_{DDIO}	25	In	Sets the Input Threshold of all Digital inputs, except SHARE_CLK, ASEL[1:0], VOUT_EN[1:0] and AUX_FAULTB, to approximately 45% of V_{DDIO}. Connect to a supply voltage between 1.5V and 3.6V. Connect all of the LTC2972 pins pull-up resistors to this pin except WDI/RESETB, SHARE_CLK and VOUT_EN[1:0]. Connect these pins pull-up resistors to V_{DD33}

PIN FUNCTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
ASEL0	26	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
ASEL1	27	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
REFP	28	Out	Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM
REFM	29	Out	Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP
$I_{SENSEP0}$	30*	In	DC/DC Converter Differential (+) Output Current-0 Sensing Pin
$I_{SENSEM0}$	31*	In	DC/DC Converter Differential (–) Output Current-0 Sensing Pin
$I_{SENSEP1}$	34*	In	DC/DC Converter Differential (+) Output Current-1 Sensing Pin
$I_{SENSEM1}$	35*	In	DC/DC Converter Differential (–) Output Current-1 Sensing Pin
$V_{IN\_SNS\_CAP}$	1	Out	V_{IN_SNS} Filter Capacitor Pin. Bypass to Ground with a 10nF Ceramic Capacitor
GND	2	Ground	
V_{DAC0}	38	Out	DAC0 Output
V_{DAC1}	39	Out	DAC1 Output
I_{IN_SNSP}	43	In	DC/DC Converter Differential (+) Input Current Sensing Pin. If Unused, Connect to V_{IN_SNS}
I_{IN_SNSM}	44	In	DC/DC Converter Differential (–) Input Current Sensing Pin. If Unused, Connect to V_{IN_SNS}
$V_{SENSEP1}$	36*	In	DC/DC Converter Differential (+) Output Voltage-1 Sensing Pin
$V_{SENSEM1}$	37*	In	DC/DC Converter Differential (–) Output Voltage-1 Sensing Pin
GND	45	Ground	Exposed Pad. Must Be Soldered to PCB

* Tie any unused $V_{SENSEPn}/I_{SENSEPn}$, $V_{SENSEMn}/I_{SENSEMn}$ or T_{SENSEn} pins to GND. Refer to Unused ADC Sense Inputs in the Applications Information section.

BLOCK DIAGRAM



OPERATION

LTC2972 OPERATION OVERVIEW

The LTC2972 is a PMBus programmable power supply controller, monitor, sequencer and voltage supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and LTC2972 internal temperature readback through the PMBus interface.
- Connect directly to a DC/DC converters IMON pin or the DCR sense network for output current telemetry readback.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC2972 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of ADC current measurements.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR_RETRY_COUNT programs the number of retries (0 to 6 or infinite) for both pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow trimming restart if target drifts outside of V_{OUT} warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when V_{DD33} is applied on power-up.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2972 FAULTB0 and FAULTB1 pins.
- Propagate per-channel POWER GOOD status via the PG0 and PG1 pins, or configure these pins as general-purpose IOs.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV and UV faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Read high side input current, input voltage, input power, and accumulated input energy.

OPERATION

- Record minimum and maximum input voltage, input current, input power, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr_ee_unlock, Mfr_ee_erase, and Mfr_ee_data). Facilitates in-house bulk programming.
- Accommodate multiple hosts with Command Plus.

EEPROM

The LTC2972 contains internal EEPROM (Nonvolatile Memory) with error-correcting-code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non-destructive operation above T_J = 105°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 105°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 105°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when T_J > 85°C.

The degradation in EEPROM retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

k = 8.617 • 10^{-5} eV/°K

T_{USE} = 105°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 125°C for 10 hours.

T_{STRESS} = 125°C

T_{USE} = 105°C

AF = 8.65

Equivalent operating time at 105°C = 86.5 hours.

So the overall retention of the EEPROM was degraded by an additional 76.5 hours as a result of operation at a junction temperature of 125°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a junction temperature of 105°C.

AUXFAULTB

The MFR_CONFIG2_LTC2972 and MFR_CONFIG3_LTC2972 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUXFAULTB pin to be driven low. The only fault types which can be propagated to the AUXFAULTB pin are over/under voltage faults.

RESETB

Holding the WDI/RESETB pin low for more than t_{RESETB} will cause the LTC2972 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I^2C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2972 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to V_{DD33} with a 10k resistor. WDI/RESETB includes an internal 256µs deglitch filter so additional filter capacitance on this pin is not recommended.

V_{DDIO}

The V_{DDIO} pin defines the input threshold of the SDA, SCL, ALERTB, PWRGD, FAULTB[1:0], CONTROL[1:0], PG[1:0], WDI/RESETB, and WP pins to allow for lower voltage digital communication. An internal resistive divider at the V_{DDIO} pin sets the internal threshold voltage to approximately 45% of the V_{DDIO} pin voltage. The VOUT_EN[1:0], AUX_FAULTB, and SHARE_CLK pins are not affected by the voltage at the V_{DDIO} pin and should always be pulled up to V_{DD33}.

OPERATION

PMBus SERIAL DIGITAL INTERFACE

The LTC2972 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2972 is a slave device. The master can communicate with the LTC2972 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1 to 13 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I^2C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a master device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at:

www.pmbus.org

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I^2C. This can be found at:

www.smbus.org

When using an I^2C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I^2C read.

Device Address

The I^2C/SMBus address of the LTC2972 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V_{DD33}, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTC2972s can be connected together to control eighteen outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I^2C/SMBus device or global addresses, including I^2C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2972 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

Processing Commands

The LTC2972 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2972 is busy.

OPERATION

EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	t_{MASS_WRITE}	See Electrical Characterization table. The LTC2972 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read.
RESTORE_USER_ALL	30ms	The LTC2972 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_CLEAR	175ms	The LTC2972 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_STORE	20ms	The LTC2972 will not accept any commands while it is transferring fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
Internal Fault log	20ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_ RESTORE	2ms	The LTC2972 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read.

*The typical delay is measured from the command's stop to the next command's start.

Other Commands

COMMAND	TYPICAL DELAY*	COMMENT
MFR_CONFIG	<50µs	The LTC2972 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.
IOUT_CAL_GAIN and IOUT_CAL_OFFSET	<500µs	The LTC2972 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.

*The delay is measured from the command's stop to the next command's start.

Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2972 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs.

OPERATION

Table 1. LTC2972 Address Look-Up Table with MFR_I2C_BASE_ADDRESS Set to 7-bit 0x5C

ADDRESS PINS		DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							
ASEL1	ASEL0		7-Bit	8-Bit	6	5	4	3	2	1	0	R/W
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V_{DD33}, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7-bit 0x5C (Factory Default)

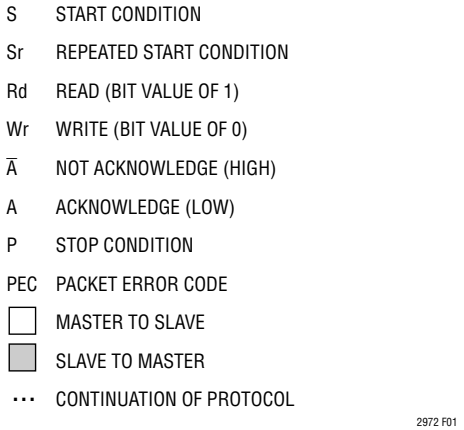


Figure 1. PMBus Packet Protocol Diagram Element Key

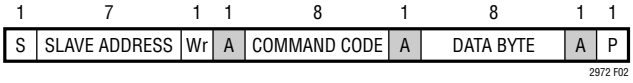


Figure 2. Write Byte Protocol

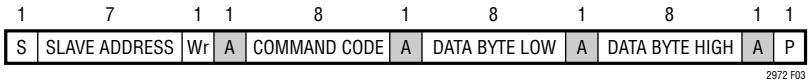


Figure3. Write Word Protocol

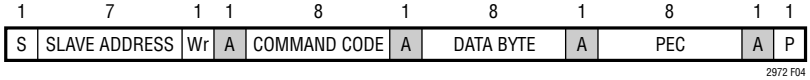


Figure 4. Write Byte Protocol with PEC

OPERATION

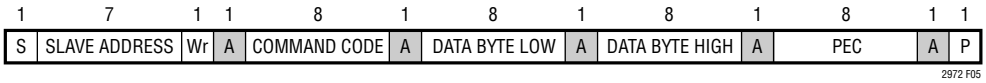


Figure 5. Write Word Protocol with PEC

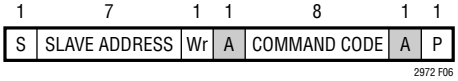


Figure 6. Send Byte Protocol

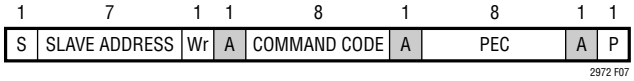


Figure 7. Send Byte Protocol with PEC

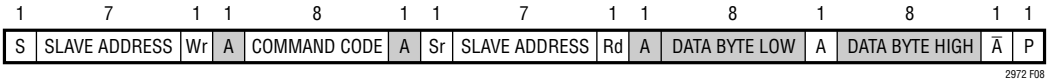


Figure 8. Read Word Protocol

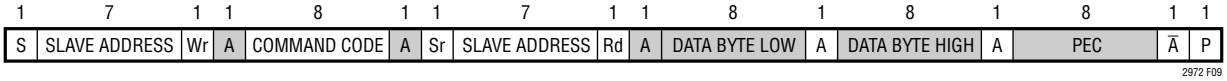


Figure 9. Read Word Protocol with PEC

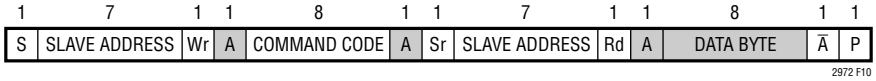


Figure 10. Read Byte Protocol

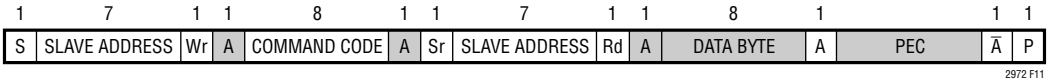


Figure 11. Read Byte Protocol with PEC

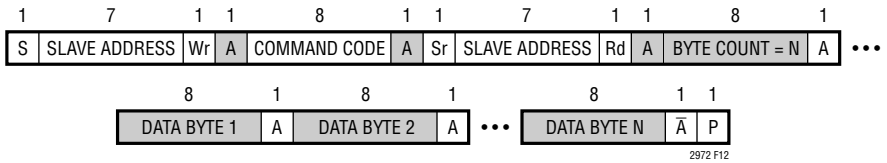


Figure 12. Block Read

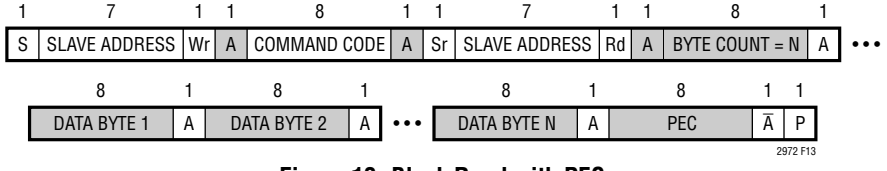


Figure 13. Block Read with PEC

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	31
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	37
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	38
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	68
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	32
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	46
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	46
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	88
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	52
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	53
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	53
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	53
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	53
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	49
VIN_OFF	0x36	Input voltage below which power conversion is disabled. Both V_{OUT_EN} pins go off immediately or sequence off after TOFF_DELAY (See Mfr_config_track_en*n*).	R/W Word	N	L11	V	Y	9.0 0xD240	49
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	54
IOUT_CAL_OFFSET	0x39	Offset applied to the current sense measurement in Amps.	R/W Word	Y	L11	A	Y	0 0x8000	54
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	53
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	64
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	49
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	49

Note: The data format abbreviations are detailed at the end of this table