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4-Channel PMBus Power System Manager Featuring Accurate Input Current and Energy Measurement

FEATURES

- **Sequence, Trim, Margin and Supervise Four Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus™ Compliant Command Set**
- **Supported by LTpowerPlay™ GUI**
- **Margin or Trim Supplies to Within 0.25% of Target**
- **Monitor Input Current (±1%) and Accumulate Energy**
- **Fast OV/UV and OC Supervisors Per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously Without Additional Software**
- External Temperature and Input Voltage Supervisors
- Accurate Monitoring of Four Output Voltages, Four Output Currents, Four External Temperatures, Input Voltage and Current, and Internal Die Temperature
- I^2C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Pin-Compatible to the LTC2974
- Available in 64-Lead 9mm × 9mm QFN Package

APPLICATIONS

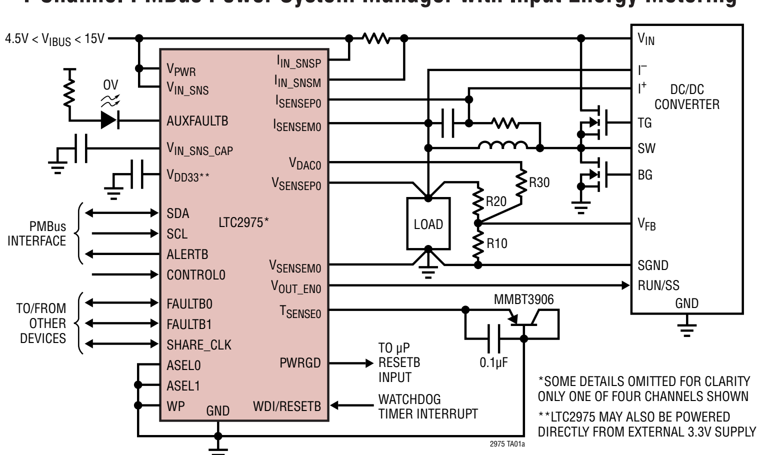
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Video and Medical Imaging

DESCRIPTION

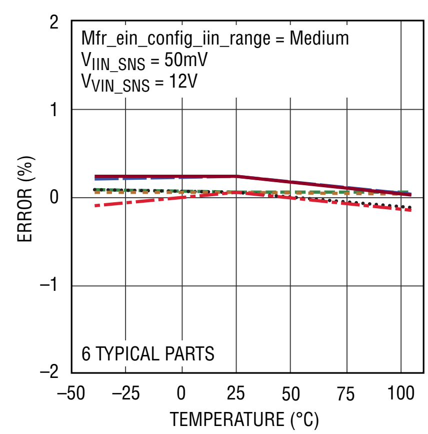
The LTC®2975 is a 4-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include over and under current, voltage and temperature threshold limits for four power supply output channels as well as over and under voltage threshold limits for a single power supply input channel. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors four output voltages, four output currents, four external temperatures, input voltage and current, and die temperature. Input power, energy, and output power is also calculated. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM supports autonomous operation without additional software.

TYPICAL APPLICATION

4-Channel PMBus Power System Manager with Input Energy Metering



Power Measurement Error



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages:
- V_{PWR} .... –0.3V to 15V
- V_{DD33} .... –0.3V to 3.6V
- V_{DD25} .... –0.3V to 2.75V

Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1, CONTROL2, CONTROL3 .... –0.3V to 3.6V
- PWRGD, SHARE_CLK, WDI/RESETB, WP, FAULTB0, FAULTB1 .... –0.3V to 3.6V
- ASEL0, ASEL1 .... –0.3V to 3.6V

Analog Voltages:
- REFP .... –0.3V to 1.35V
- REFM .... –0.3V to 0.3V
- V_{IN_SNS}, $V_{IN\_SNS\_CAP}$ .... –0.3V to 15V
- I_{IN_SNSP}, I_{IN_SNSM} to V_{IN_SNS} .... –0.3V to 0.3V
- $V_{SENSEP[3:0]}$ .... –0.3V to 6V
- $V_{SENSEM[3:0]}$ .... –0.3V to 6V
- $I_{SENSEP[3:0]}$ .... –0.3V to 6V
- $I_{SENSEM[3:0]}$ .... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, AUXFAULTB .... –0.3V to 15V
- $V_{DAC[3:0]}$ .... –0.3V to 6V
- $T_{SENSE[3:0]}$ .... –0.3V to 3.6V
- I_{IN_SNSP}, I_{IN_SNSM} .... –0.3V to 15V

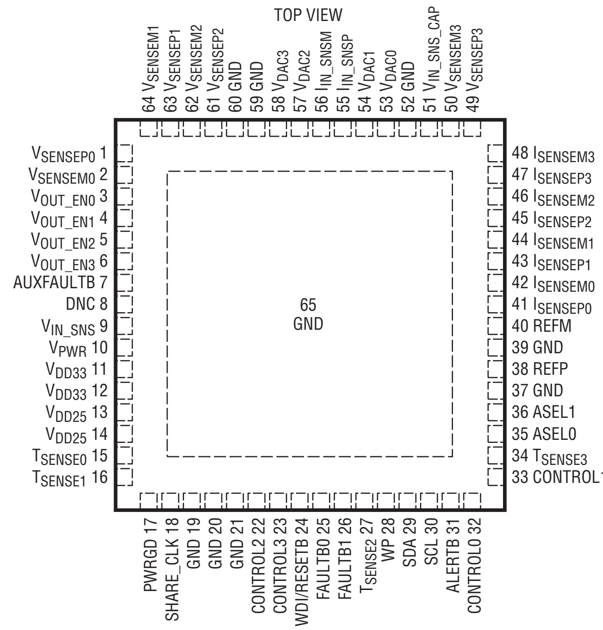
Operating Junction Temperature Range:
- LTC2975C .... 0°C to 70°C
- LTC2975I .... –40°C to 105°C

Storage Temperature Range .... –65°C to 150°C*

Maximum Junction Temperature .... 125°C*

*See OPERATION section for detailed EEPROM derating information for junction temperatures in excess of 105°C.

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JCtop} = 7°C/W, $\theta_{JCbottom}$ = 1°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC2975CUP#PBF	LTC2975CUP#TRPBF	LTC2975UP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2975IUP#PBF	LTC2975IUP#TRPBF	LTC2975UP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 105°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range	V_{DD33} Floating (Note 2)	●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating (Note 2)	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.25	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	50	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} applied until the TON_DELAY timer starts			30		ms
Voltage Reference Characteristics							
V_{REF}	Output Voltage	V_{REF} = V_{REFP} – V_{REFM}, 0 < I_{REFP} < 100µA	●	1.220	1.232	1.244	V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 3)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPn}$, $I_{SENSEMn}$	●	–0.1		6	V
		Differential Current Sense Voltage: V_{IN_ADC} = ($I_{SENSEPn}$ – $I_{SENSEMn}$)	●	–170		170	mV
N_ADC	Voltage Sense Resolution	0V ≤ V_{IN_ADC} ≤ 6V, READ_VOUT			122		µV/LSB
	Current Sense Resolution with IOUT_CAL_GAIN = 1Ω	0mV ≤ |V_{IN_ADC}| < 16mV (Note 4) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}|			15.625 31.25 62.5 125 250		µA/LSB µA/LSB µA/LSB µA/LSB µA/LSB
TUE_ADC_VOLT_SNS	Total Unadjusted Error	Voltage Sense Inputs V_{IN_ADC} ≥ 1V	●			±0.25	% of Reading
		Voltage Sense Inputs 0 ≤ V_{IN_ADC} ≤ 1V	●			±2.5	mV
TUE_ADC_CURR_SNS	Total Unadjusted Error	Current Sense Inputs 20mV ≤ |V_{IN_ADC}| ≤ 170mV	●			±0.3	% of Reading
		Current Sense Inputs |V_{IN_ADC}| ≤ 20mV	●			±60	µV
V_{OS_ADC}	Offset Error	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs, V_{OS} • IOUT_CAL_GAIN, IOUT_CAL_GAIN = 1000mΩ	●			±35	µV
t_{CONV_ADC}	Conversion Time	$V_{SENSEPn}$, $V_{SENSEMn}$, V_{IN_SNS} Inputs (Note 5)			6.15		ms
		$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs (Note 5)			24.6		ms
		Internal Temperature (READ_TEMPERATURE_2) (Note 5)			24.6		ms
t_{UPDATE_ADC}	Update Time	Note 5, Mfr_ein_config_hd = 0			190		ms
		Note 5, Mfr_ein_config_hd = 1			500		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz
Sense Input Current Characteristics (Note 12)							
I_{IN_VSENSE}	Input Current	$V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs	●			±15	µA
	Differential Input Current	$V_{SENSEPn}$ and $V_{SENSEMn}$ Inputs, V_{IN_DIFF} = 6V	●			±30	µA
I_{IN_ISENSE}	Input Current	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs	●			±3	µA
	Differential Input Current	$I_{SENSEPn}$ and $I_{SENSEMn}$ Inputs, $\lvert V_{IN\_DIFF}\rvert$ = 0.17V	●			±5	µA
DAC Output Characteristics							
N_V_{DAC}	Resolution				10		Bits
V_{FS_VDAC}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1; Buffer Gain Setting_0 Buffer Gain Setting_1	● ●	1.3 2.5	1.38 2.65	1.44 2.77	V V
INL_V_{DAC}	Integral Nonlinearity	(Note 6)	●			±2	LSB
DNL_V_{DAC}	Differential Nonlinearity	(Note 6)	●			±2.4	LSB
V_{OS_VDAC}	Offset Voltage	(Note 6)	●			±15	mV
V_{DAC}	Load Regulation	V_{DACn} = 2.65V, I_{VDACn} Sourcing = 2mA			100		ppm/mA
		V_{DACn} = 0.1V, I_{VDACn} Sinking = 2mA			100		ppm/mA
	PSRR	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}			60		dB
	Leakage Current	V_{DACn} Hi-Z, 0V ≤ V_{DACn} ≤ 6V	●			±100	nA
	Short-Circuit Current Low	V_{DACn} Shorted to GND	●	–12		–4	mA
	Short-Circuit Current High	V_{DACn} Shorted to V_{DD33}	●	4		12	mA
C_{OUT}	Output Capacitance	V_{DACn} Hi-Z			10		pF
t_{S_VDAC}	DAC Output Update Rate	Fast Servo Mode			250		µs
Voltage Supervisor Characteristics							
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$); Low Resolution Mode High Resolution Mode	● ●	0 0		6 3.8	V V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode	●			±1.25	% of Reading
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode	●			±1.0	% of Reading
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode	●			±1.5	% of Reading
t_{S_VS}	Update Period				12.21		µs
Current Supervisor Characteristics							
V_{IN_CS}	Current Sense Input Range	Single-Ended Voltage: $I_{SENSEPn}$, $I_{SENSEMn}$	●	–0.1		6	V
		Differential Voltage: V_{IN_CS} = ($I_{SENSEPn}$ – $I_{SENSEMn}$)	●	–170		170	mV
N_CS	Current Sense Resolution	IOUT_OC_FAULT_LIMIT • IOUT_CAL_GAIN IOUT_UC_FAULT_LIMIT • IOUT_CAL_GAIN			400		µV/LSB
TUE_CS	Total Unadjusted Error	50mV ≤ $\lvert V_{IN\_CS}\rvert$ ≤ 170mV	●			±3	% of Reading
		$\lvert V_{IN\_CS}\rvert$ < 50mV	●			±1.5	mV
V_{OS_CS}	Offset Error	V_{IN_CS} = 0	●			±600	µV
t_{S_CS}	Update Period				12.21		µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN_SNS} Input Characteristics							
V_{IN_SNS}	V_{IN_SNS} Input Voltage Range	(Note 11)	●	0		15	V
I_{VIN_SNS}	VIN_SNS Input Current	V_{VIN_SNS} = 4.5V	●	80	140	200	µA
		V_{VIN_SNS} = 12V	●	150	250	350	µA
		V_{VIN_SNS} = 15V	●	180	300	420	µA
$TUE_{VIN\_SNS\_T}$	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	4.5V ≤ V_{VIN_SNS} ≤ 8V	●			±2.0	% of Reading
		V_{VIN_SNS} > 8V	●			±1.0	% of Reading
TUE_VIN	READ_VIN Total Unadjusted Error	4.5V ≤ V_{VIN_SNS} ≤ 15V (Note 11)	●			±0.5	% of Reading
DAC Soft-Connect Comparator Characteristics							
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V	●		±1	±18	mV
		V_{DACPn} = 1.3V	●		±2	±26	mV
		V_{DACPn} = 2.65V	●		±3	±52	mV
Input Current Sense Characteristics							
V_{IIN}	Common Mode Input Range	V_{IIN_SNSP} = V_{IIN_SNSM} (Note 11)	●	4.5		15	V
I_{IIN}	I_{IIN_SNSP}, I_{IIN_SNSM} Input Current	V_{IIN_SNSP} = V_{IIN_SNSM} = V_{IIN_SNS} (Note 2)	●		0.5	2	µA
FS_IIN	Full-Scale Input Current Sense Voltage Range	Referred to (V_{IIN_SNSP} – V_{IIN_SNSM}) High Range Medium Range Low Range	● ● ●	–100 –50 –20		100 50 20	mV mV mV
TUE_IIN	Total Unadjusted Error	|V_{IIN_SNSP} – V_{IIN_SNSM} | = 100mV, High Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 50mV, Medium Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 20mV, Low Range	● ● ●			±0.6 ±0.65 ±0.75	% of Reading % of Reading % of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM} | = 20mV, High Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 15mV, Medium Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 10mV, Low Range	● ● ●			±1 ±1 ±1	% of Reading % of Reading % of Reading
		|V_{IIN_SNSP} – V_{IIN_SNSM} | = 0mV, High Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 0mV, Medium Range |V_{IIN_SNSP} – V_{IIN_SNSM} | = 0mV, Low Range	● ● ●			±100 ±75 ±50	µV µV µV
CMRR_IIN	DC CMRR	4.5V ≤ V_{IIN_SNSP} = V_{IIN_SNS} ≤ 15V |V_{IIN_SNSP} – V_{IIN_SNSM}| = 100mV High Range	●	85			dB
	AC CMRR	V_{IIN_SNSP} = V_{IIN_SNS}= 12V ± 100mV f = 62.5kHz			85		dB
t_{CONV_IIN}	Conversion Time				25		ms
t_{UPDATE}	Update Rate				5.4		Hz
External Temperature Sensor Characteristics (READ_TEMPERATURE_1)							
t_{CONV_TSENSE}	Conversion Time	For One Channel, (Total Latency For All Channels Is 4 • 66ms)			66		ms
I_{TSENSE_HI}	T_{SENSE} High Level Current		●	–90	–64	–40	µA
I_{TSENSE_LOW}	T_{SENSE} Low Level Current		●	–5.5	–4	–2.5	µA
TUE_TS	Total Unadjusted Error	Ideal Diode Assumed	●		±3		°C
N_TS	Maximum Ideality Factor	READ_TEMPERATURE_1 = 175°C MFR_TEMP_1_GAIN = 1/N_TS				1.10	
Internal Temperature Sensor Characteristics (READ_TEMPERATURE_2)							
TUE_TS2	Total Unadjusted Error				±1		°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF, $C_{VIN\_SNS\_CAP}$ = 10nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT} Enable Output ($V_{OUT\_EN\,[3:0]}$) Characteristics							
V_{VOUT_ENn}	Output High Voltage	I_{VOUT_ENn} = –5µA, V_{DD33} = 3.13V	●	10	13	14.7	V
I_{VOUT_ENn}	Output Sourcing Current	V_{VOUT_ENn} Pull-Up Enabled, V_{VOUT_ENn} = 1V	●	–5	–7	–9	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	2.5	5	8	mA
		Weak Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	33	50	65	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
General Purpose Output (AUXFAULTB) Characteristics							
$V_{AUXFAULTB}$	Output High Voltage	$I_{AUXFAULTB}$ = –5µA, V_{DD33} = 3.13V	●	10	13	14.7	V
$I_{AUXFAULTB}$	Output Sourcing Current	AUXFAULTB Pull-Up Enabled, $V_{AUXFAULTB}$ = 1V	●	–5	–7	–9	µA
	Output Sinking Current	Strong Pull-Down Enabled, $V_{AUXFAULTB}$ = 0.4V	●	2.5	5	8	mA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ $V_{AUXFAULTB}$ ≤ 15V	●			±1	µA
Energy Meter Characteristics							
TUE_ETB	Energy Meter Time-Base Error		●			±1.5	% of Reading
TUE_PIN	READ_PIN Total Unadjusted Error	V_{IIN_SNSP} – V_{IIN_SNSM} = 50mV, Medium Range	●			±1	% of Reading
TUE_EIN	Energy Meter Total Unadjusted Error	V_{IIN_SNSP} – V_{IIN_SNSM} = 50mV, Medium Range	●			±2.5	% of Reading
EEPROM Characteristics							
Endurance	(Notes 7, 10)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 7, 10)	T_J < 105°C	●	20			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 8)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, CONTROL2, CONTROL3, WDI/RESETB, FAULTB0, FAULTB1, WP							
V_{IH}	High Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●	2.1			V
		CONTROL*n* Only	●	1.85			V
V_{IL}	Low Level Input Voltage	FAULTB0, FAULTB1, SDA, SCL, WDI/RESETB, WP	●			1.5	V
		CONTROL*n* Only	●			1.6	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 3.6V	●			±2	µA
t_{SP}	Pulse Width of Spike Suppressed	FAULTB0, FAULTB1, CONTROL*n*			10		µs
		SDA, SCL			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			180			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB}$ ≤ 1.5V	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB}$ ≤ 1.5V	●	0.3		200	µs
f_{WDI}	Watchdog Timer Interrupt Input Frequency		●			1	MHz
C_{IN}	Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	V_{SHARE_CLK} < 0.8V	●	0.825		1.11	µs

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{RISE}	Rise Time	V_{SHARE_CLK} < 0.8V to V_{SHARE_CLK} > 1.6V	●			450	ns
I_{LEAK}	Input Leakage Current	0V ≤ V_{SHARE_CLK} ≤ V_{DD33} + 0.3V	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Digital Outputs SDA, ALERTB, SHARE_CLK, FAULTB0, FAULTB1, PWRGD							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
I_{HIZ}	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 9)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 9)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 9)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 10)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 9)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 9)		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 9)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2975 Receiving Data) (Note 9)		●	0			ns
	Data Hold Time (LTC2975 Transmitting Data) (Note 9)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 9)		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 9)				98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated	Mfr_config_all_longer_pmbus_timeout = 0 Mfr_config_all_longer_pmbus_timeout = 1	● ●		25 200	35 280	ms ms
Additional Digital Timing Characteristics							
t_{OFF_MIN}	Minimum Off-Time for Any Channel				100		ms

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: Hysteresis in the output voltage is created by package stress that differs depending on whether IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 4: The current sense resolution is determined by the L11 format and the mV units of the returned value. For example, a full-scale value of 170mV returns a L11 value of 0xF2A8 = 680 • 2^{-2} = 170. This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is 2^{-2}mA = 250µA. Each successively lower range improves resolution by cutting the LSB size in half.

Note 5: The nominal time between successive ADC conversions (latency of the ADC) for any given channel is t_{UPDATE_ADC}.

ELECTRICAL CHARACTERISTICS

Note 6: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 7: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 8: The LTC2975 will not acknowledge any PMBus commands, except for MFR_COMMON, when a STORE_USER_ALL command is being executed. See also OPERATION section.

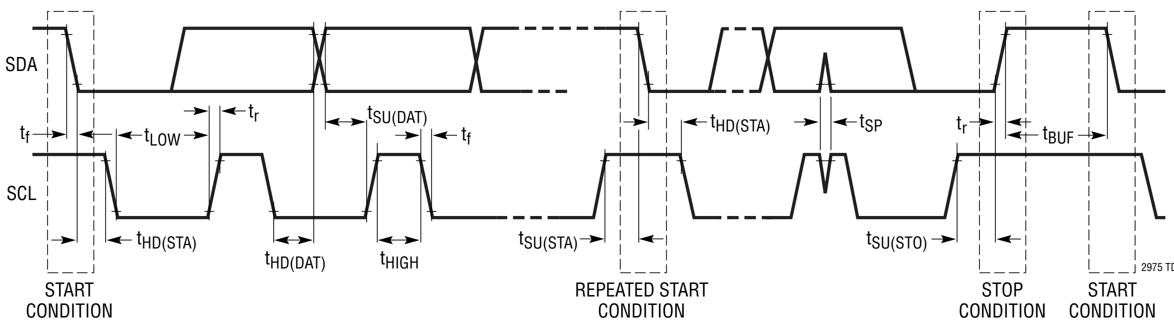
Note 9: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: (20 + 0.1• C_B) (ns) < t_r < 300ns and (20 + 0.1 • C_B) (ns) < t_f < 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is 3.13V < V_{IO} < 3.6V.

Note 10: EEPROM endurance and retention will be degraded when T_J > 105°C.

Note 11: While READ_VIN operates with 0V ≤ V_{IN_SNS} ≤ 15V, the valid READ_IIN, READ_PIN, and MFR_EIN operating range is 4.5V ≤ V_{IN_SNS} ≤ 15V.

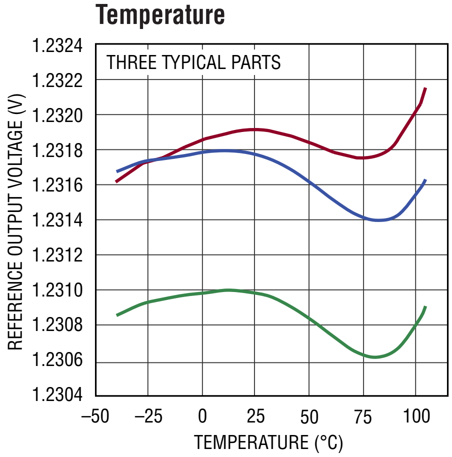
Note 12: V_{SENSE} and I_{SENSE} input currents are characterized by input current and input differential current. Input current is defined as current into a single device pin (see Note 2). Input differential current is defined as ($I^+ – I^–$) where I^+ is the current into the positive device pin and $I^–$ is the current into the negative device pin.

PMBUS TIMING DIAGRAM

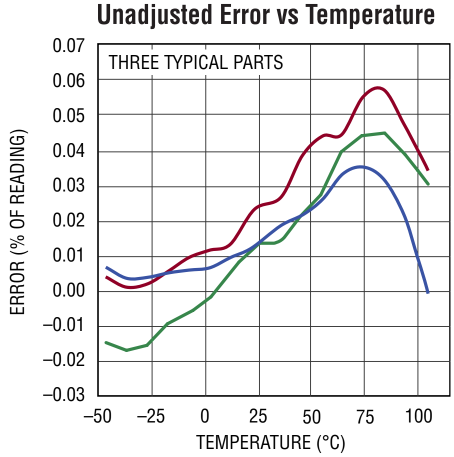


TYPICAL PERFORMANCE CHARACTERISTICS

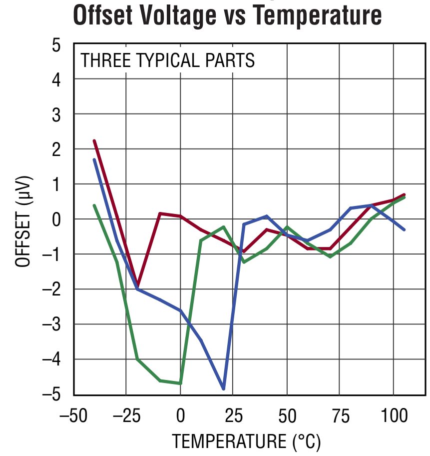
Reference Voltage vs Temperature



ADC READ_VOUT ADC Total Unadjusted Error vs Temperature

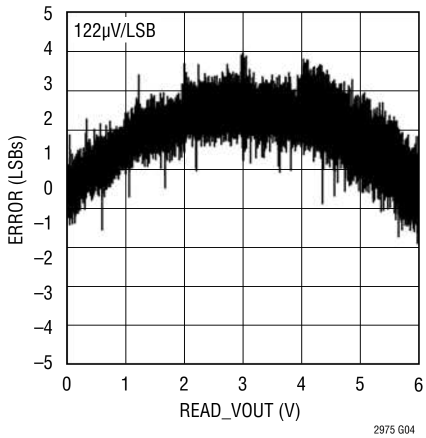


ADC READ_IOUT Input Referred Offset Voltage vs Temperature

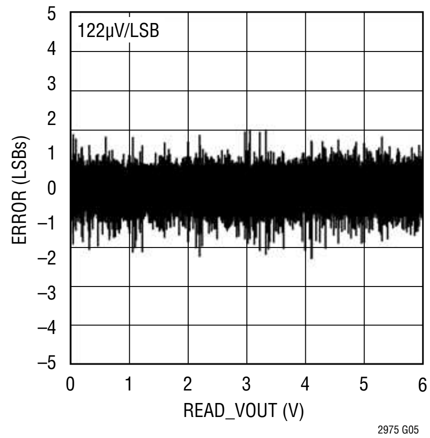


TYPICAL PERFORMANCE CHARACTERISTICS

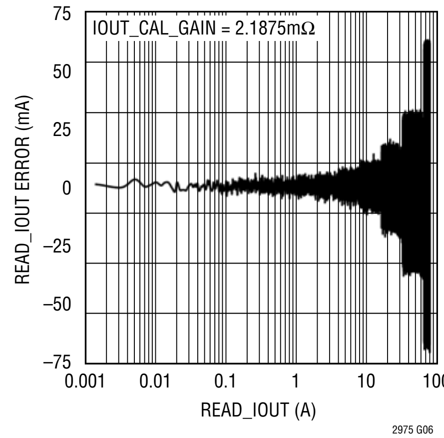
ADC READ_VOUT-INL



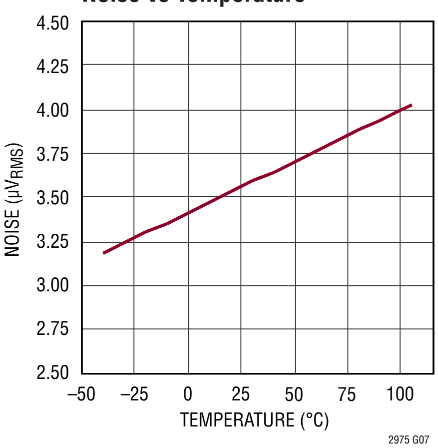
ADC READ_VOUT-DNL



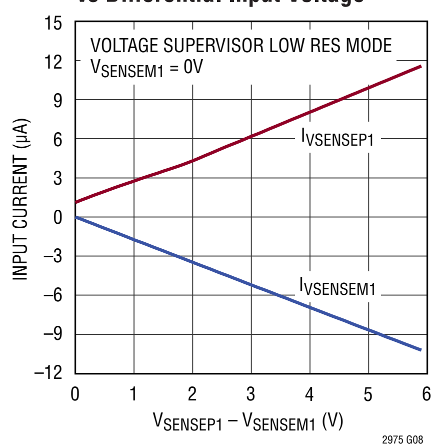
ADC READ_IOUT Error vs READ_IOUT



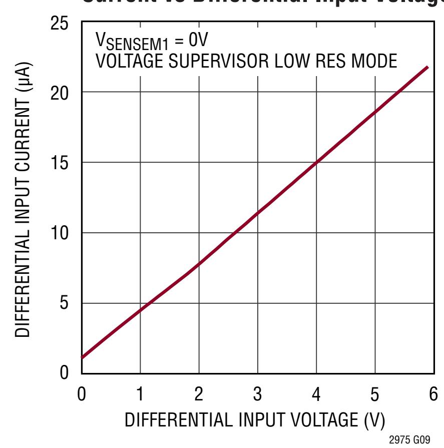
ADC READ_IOUT Input Referred Noise vs Temperature



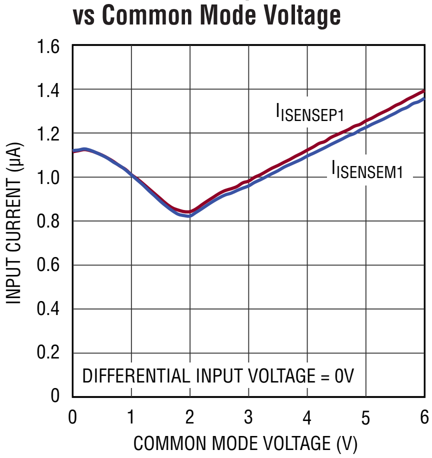
Voltage Sense Input Currents vs Differential Input Voltage



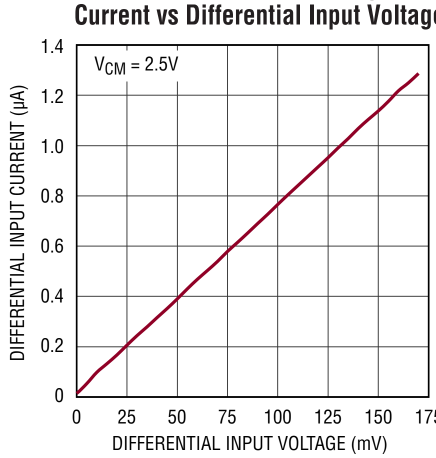
Voltage Sense Differential Input Current vs Differential Input Voltage



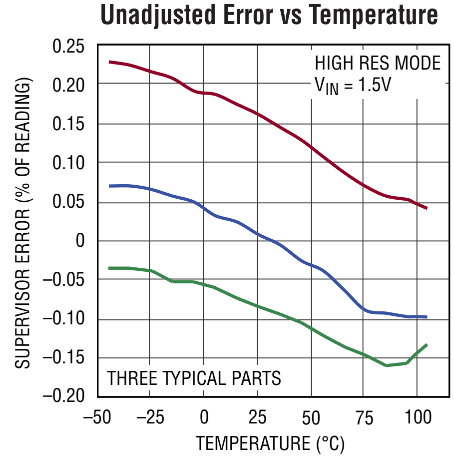
Current Sense Input Current vs Common Mode Voltage



Current Sense Differential Input Current vs Differential Input Voltage

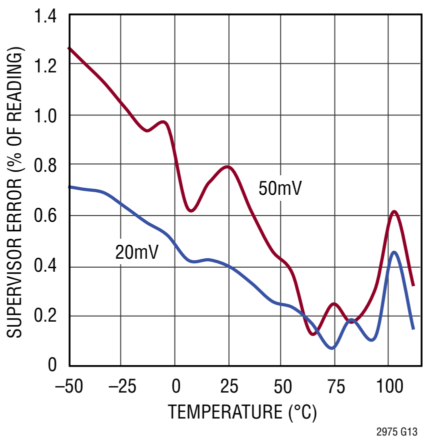


Voltage Supervisor Total Unadjusted Error vs Temperature

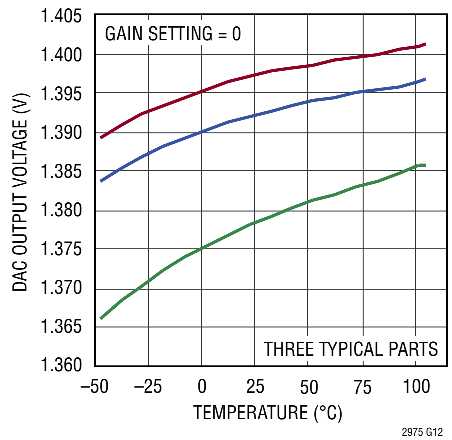


TYPICAL PERFORMANCE CHARACTERISTICS

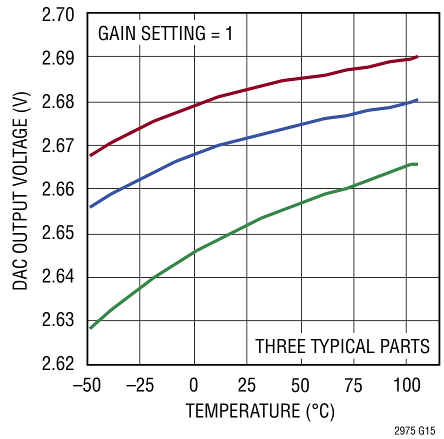
Current Supervisor Total Unadjusted Error vs Temperature



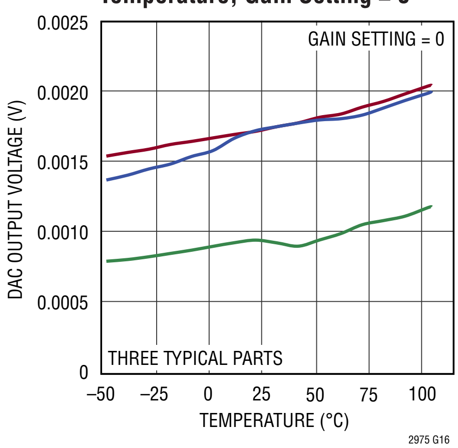
DAC Full-Scale Voltage vs Temperature, Gain Setting = 0



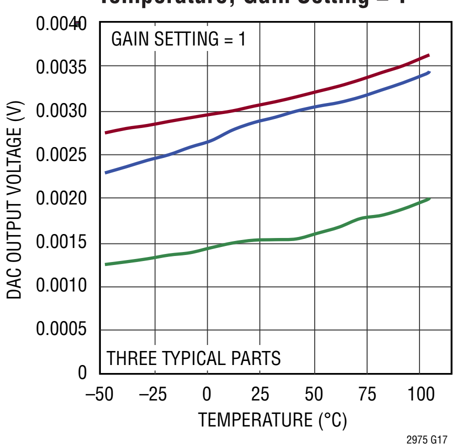
DAC Full-Scale Voltage vs Temperature, Gain Setting = 1



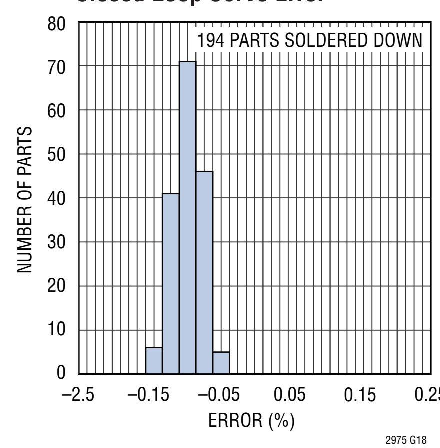
DAC Offset Voltage vs Temperature, Gain Setting = 0



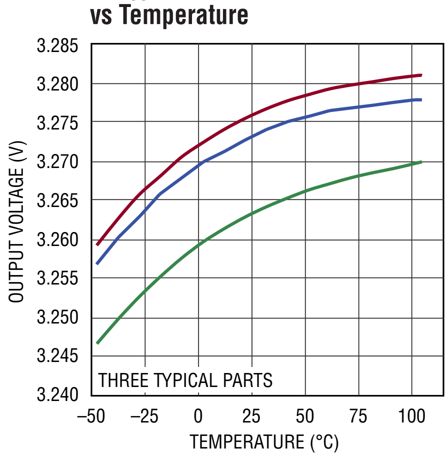
DAC Offset Voltage vs Temperature, Gain Setting = 1



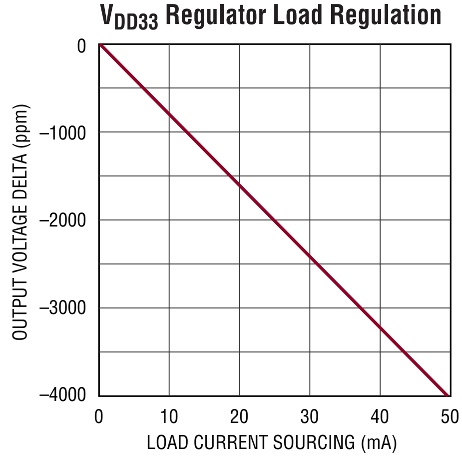
Closed Loop Servo Error



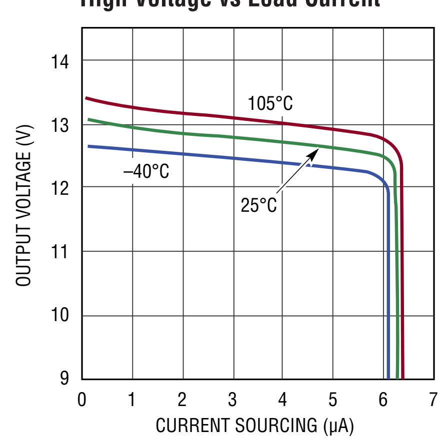
V_{DD33} Regulator Output Voltage vs Temperature



V_{DD33} Regulator Load Regulation

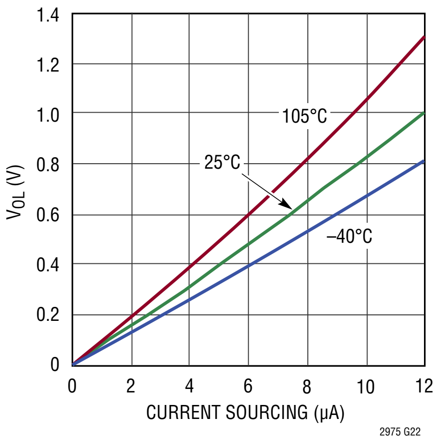


$V_{OUT\_EN[0:3]}$ and AUXFAULTB Output High Voltage vs Load Current

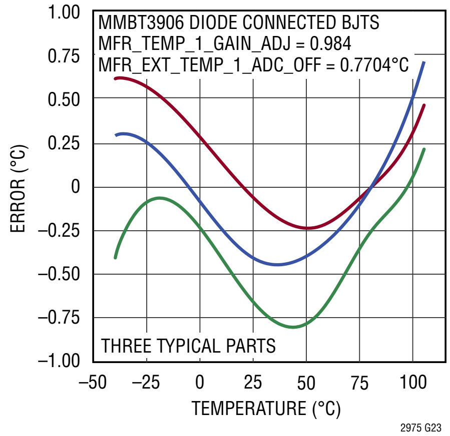


TYPICAL PERFORMANCE CHARACTERISTICS

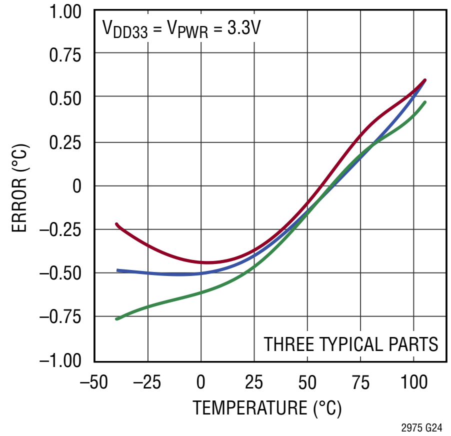
$V_{OUT\_EN[0:3]}$ and AUXFAULTB VOL vs Load Current



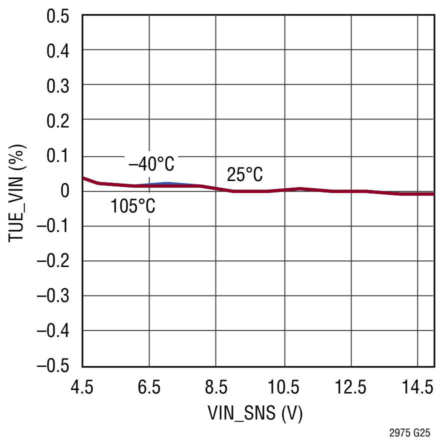
External Temperature READ_TEMPERATURE_1 Error vs Temperature



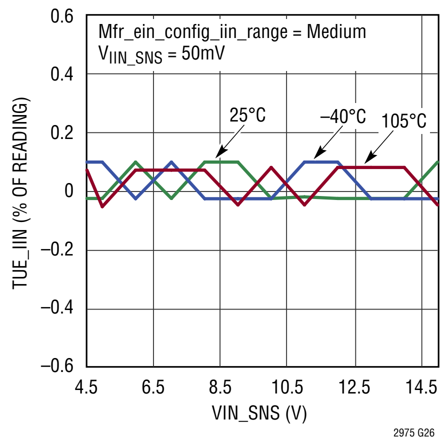
READ_TEMPERATURE_2 Error vs Temperature



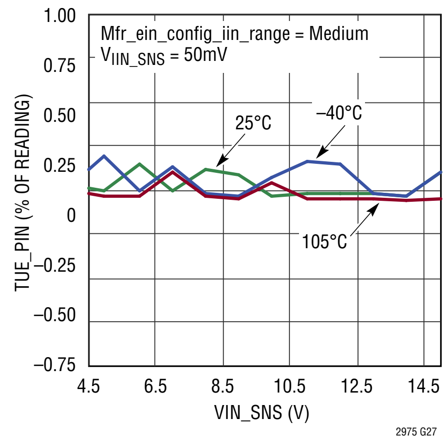
TUE_VIN vs VIN_SNS



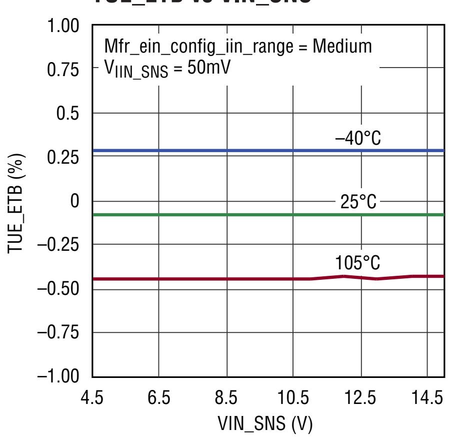
TUE_IIN vs VIN_SNS



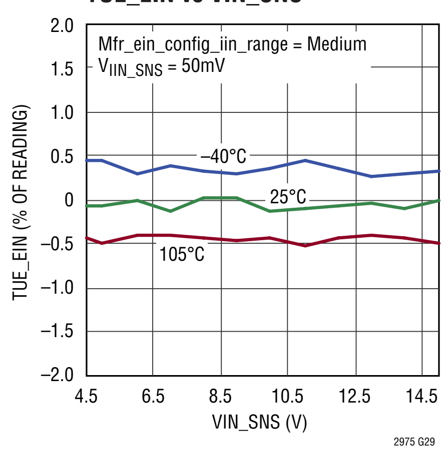
TUE_PIN vs VIN_SNS



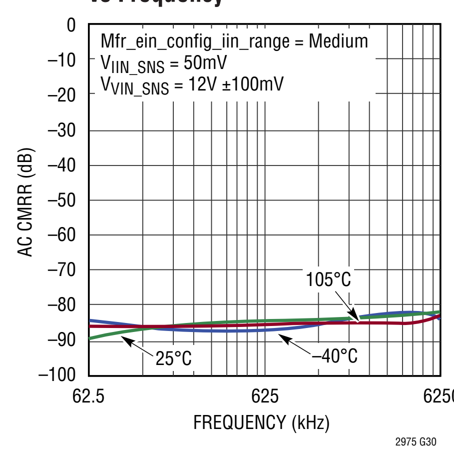
TUE_ETB vs VIN_SNS



TUE_EIN vs VIN_SNS



READ_IIN Common Mode Gain vs Frequency



PIN FUNCTIONS

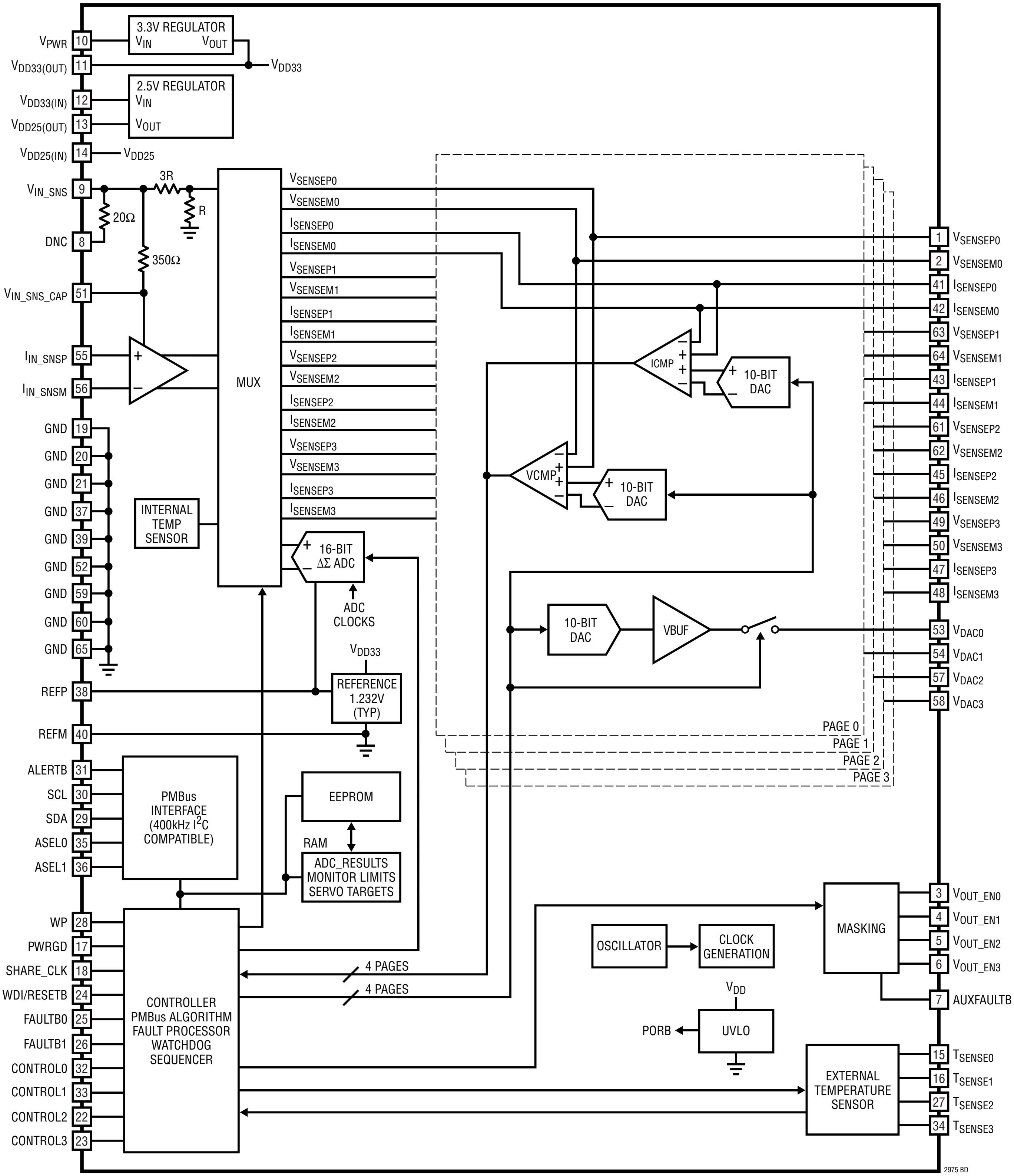
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$V_{SENSEP0}$	1*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	2*	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
V_{OUT_EN0}	3	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN1}	4	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN2}	5	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
V_{OUT_EN3}	6	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA
AUXFAULTB	7	Out	Auxiliary Fault Output Pin. Output High Voltage Optionally Pulled-Up to 12V by 5µA. Can Be Configured to Pull Low When OV/OC/UC Detected
DNC	8	Do Not Connect	Do Not Connect to this Pin
V_{IN_SNS}	9	In	V_{IN} SENSE Input. This Voltage is Compared Against the V_{IN} On and Off Voltage Thresholds In Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V_{PWR}	10	In	V_{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5 to 15V). If a 4.5V to 15V Supply Voltage Is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1µF Capacitor.
V_{DD33}	11	In/Out	If Shorted to V_{PWR}, It Serves as 3.13 to 3.47V Supply Input Pin. Otherwise It Is a 3.3V Internally Regulated Voltage Output (Use 0.1µF Decoupling Capacitor to GND). If using the internal regulator to provide VDD33, do not connect to VDD33 pins of any other devices.
V_{DD33}	12	In	Input for Internal 2.5V Sub-Regulator. Short this Pin to Pin 11
V_{DD25}	13	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor. Do not connect to VDD25 pins of any other devices.
V_{DD25}	14	In	2.5V Supply Voltage Input. Short this Pin to Pin 13
T_{SENSE0}	15*	In/Out	External Temperature Current Output and Voltage Input for Channel 0. Maximum allowed capacitance is 1µF
T_{SENSE1}	16*	In/Out	External Temperature Current Output and Voltage Input for Channel 1. Maximum allowed capacitance is 1µF
PWRGD	17	Out	Power-Good Open Drain Output. Indicates When Selected Outputs Are Power Good. Can be Used as System Power-on Reset
SHARE_CLK	18	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49kΩ Pull-Up Resistor to V_{DD33}. Connect to all other SHARE_CLK pins in the system.
GND	19	Ground	Chip Ground. Must Be Soldered to PCB
GND	20	Ground	Chip Ground. Must Be Soldered to PCB
GND	21	Ground	Chip Ground. Must Be Soldered to PCB
CONTROL2	22	In	Control Pin 2 Input
CONTROL3	23	In	Control Pin 3 Input
WDI/RESETB	24	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10kΩ Pull-Up Resistor to V_{DD33}. Rising Edge Resets Watchdog Counter. Holding this Pin Low for More than t_{RESETB} Resets the Chip
FAULTB0	25	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-0. Connect a 10kΩ Pull-Up Resistor to V_{DD33}
FAULTB1	26	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-1. Connect a 10kΩ Pull-Up Resistor to V_{DD33}
T_{SENSE2}	27*	In/Out	External Temperature Current Output and Voltage Input for Channel 2. Maximum allowed capacitance is 1µF
WP	28	In	Digital Input. Write-Protect Input Pin, Active High
SDA	29	In/Out	PMBus Bidirectional Serial Data Pin
SCL	30	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	31	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation

PIN FUNCTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
CONTROL0	32	In	Control Pin 0 Input
CONTROL1	33	In	Control Pin 1 Input
T_{SENSE3}	34*	In/Out	External Temperature Current Output and Voltage Input for Channel 3. Maximum allowed capacitance is 1µF
ASEL0	35	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
ASEL1	36	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
GND	37	Ground	Chip Ground. Must Be Soldered to PCB
REFP	38	Out	Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM
GND	39	Ground	Chip Ground. Must Be Soldered to PCB
REFM	40	Out	Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP
$I_{SENSEP0}$	41*	In	DC/DC Converter Differential (+) Output Current-0 Sensing Pin
$I_{SENSEM0}$	42*	In	DC/DC Converter Differential (–) Output Current-0 Sensing Pin
$I_{SENSEP1}$	43*	In	DC/DC Converter Differential (+) Output Current-1 Sensing Pin
$I_{SENSEM1}$	44*	In	DC/DC Converter Differential (–) Output Current-1 Sensing Pin
$I_{SENSEP2}$	45*	In	DC/DC Converter Differential (+) Output Current-2 Sensing Pin
$I_{SENSEM2}$	46*	In	DC/DC Converter Differential (–) Output Current-2 Sensing Pin
$I_{SENSEP3}$	47*	In	DC/DC Converter Differential (+) Output Current-3 Sensing Pin
$I_{SENSEM3}$	48*	In	DC/DC Converter Differential (–) Output Current-3 Sensing Pin
$V_{SENSEP3}$	49*	In	DC/DC Converter Differential (+) Output Voltage-3 Sensing Pin
$V_{SENSEM3}$	50*	In	DC/DC Converter Differential (–) Output Voltage-3 Sensing Pin
$V_{IN\_SNS\_CAP}$	51	Out	V_{IN_SNS} Filter Capacitor Pin. Bypass to Ground with a 10nF Ceramic Capacitor
GND	52	Ground	Chip Ground. Must be Soldered to PCB.
V_{DAC0}	53	Out	DAC0 Output
V_{DAC1}	54	Out	DAC1 Output
I_{IN_SNSP}	55	In	DC/DC Converter Differential (+) Input Current Sensing Pin. If Unused, Connect to V_{IN_SNS}
I_{IN_SNSM}	56	In	DC/DC Converter Differential (–) Input Current Sensing Pin. If Unused, Connect to V_{IN_SNS}
V_{DAC2}	57	Out	DAC2 Output
V_{DAC3}	58	Out	DAC3 Output
GND	59	Ground	Chip Ground. Must Be Soldered to PCB
GND	60	Ground	Chip Ground. Must Be Soldered to PCB
$V_{SENSEP2}$	61*	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
$V_{SENSEM2}$	62*	In	DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin
$V_{SENSEP1}$	63*	In	DC/DC Converter Differential (+) Output Voltage-1 Sensing Pin
$V_{SENSEM1}$	64*	In	DC/DC Converter Differential (–) Output Voltage-1 Sensing Pin
GND	65	Ground	Exposed Pad. Must Be Soldered to PCB

* Tie any unused $V_{SENSEPn}$/$I_{SENSEPn}$, $V_{SENSEMn}$/$I_{SENSEMn}$ or T_{SENSEn} pins to GND. Refer to Unused ADC Sense Inputs in the Applications Information section.

BLOCK DIAGRAM



OPERATION

LTC2975 OPERATION OVERVIEW

The LTC2975 is a PMBus programmable power supply controller, monitor, sequencer and voltage and current supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage, output voltage, output current, output temperature, and LTC2975 internal temperature readback through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the startup of DC/DC converters via PMBus programming and the CONTROL input pins. The LTC2975 supports time-based sequencing and tracking sequencing. Cascade sequence on with time based sequence off is also supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, autonomously or through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Trim or margin the DC/DC converter output voltage with direct access to the margin DAC.
- Supervise the DC/DC converter input voltage, output voltage, load current and the inductor temperatures for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Accurately handle inductor self-heating transients using a proprietary algorithm. These self-heating effects are combined with external temperature sensor readings to improve accuracy of current supervisors and ADC current measurement.
- Respond to a fault condition by continuing operation indefinitely, latching-off after a programmable deglitch period, latching-off immediately or sequencing off after TOFF_DELAY. Use retry mode to automatically recover from a latched-off condition. With retry enabled, MFR_RETRY_COUNT programs the number of retries (0 to 6 or infinite) for all pages.
- Optionally stop trimming the DC/DC converter output voltage after it reaches the initial margin or nominal target. Optionally allow trimming restart if target drifts outside of V_{OUT} warning limits.
- Store command register contents with CRC to EEPROM through PMBus programming.
- Restore EEPROM contents through PMBus programming or when V_{DD33} is applied on power-up.
- Report the DC/DC converter output voltage status through the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the LTC2975 FAULTB0 and FAULTB1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output OV, UV, OC and UC faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition.
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the on state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Read high side input current, input voltage, input power, and accumulated input energy.
- Record minimum and maximum input voltage, input current, input power, output voltages, output currents and output temperatures.
- Access user EEPROM data directly, without altering RAM space (Mfr_ee_unlock, Mfr_ee_erase, and Mfr_ee_data). Facilitates in-house bulk programming.
- Accommodate multiple hosts with Command Plus.

OPERATION

EEPROM

The LTC2975 contains internal EEPROM (Non-Volatile Memory) to store configuration settings and fault log information. EEPROM endurance, retention and mass write operation time are specified over the operating temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Non destructive operation above T_J = 105°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 105°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 105°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when T_J > 105°C.

The degradation in EEPROM retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\cdot\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4eV

k = 8.617 • 10^{-5} eV/°K

T_{USE} = 105°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 125°C for 10 hours.

T_{STRESS} = 125°C

T_{USE} = 105°C

AF = 8.65

Equivalent operating time at 105°C = 86.5 hours.

So the overall retention of the EEPROM was degraded by 86.5 hours as a result of operation at a junction temperature of 125°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a junction temperature of 105°C.

AUXFAULTB

The AUXFAULTB pin can be configured to indicate when some fault conditions have been detected, using a third output level. See Figure 1 for a conceptual view of this multiplexing.

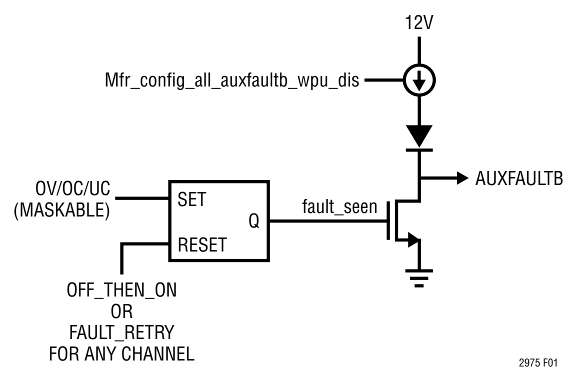


Figure 1. AUXFAULTB MUX

The MFR_CONFIG2_LTC2975 and MFR_CONFIG3_LTC2975 commands can be used on a per channel basis to select which, if any, fault conditions will cause the AUXFAULTB pin to be driven to its third output level (fast pull-down to GND). The only fault types which can be propagated to the AUXFAULTB pin are overvoltage faults and overcurrent/undercurrent faults.

Mfr_config_all_auxfaultb_wpu selects whether the AUXFAULTB pin is in the hi-Z state, or weakly pulled-up to approximately 12V, using a 5μA current. As shown in Figure 1, the pull-down to GND overrides if any enabled faults are detected.

OPERATION

RESETB

Holding the WDI/RESETB pin low for more than t_{RESETB} will cause the LTC2975 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I^2C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2975 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to V_{DD33} with a 10k resistor. WDI/RESETB includes an internal 256µs deglitch filter so additional filter capacitance on this pin is not recommended.

PMBus SERIAL DIGITAL INTERFACE

The LTC2975 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2975 is a slave device. The master can communicate with the LTC2975 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus commands are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 2 to 14 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the SMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I^2C byte commands because they provide timeouts to prevent bus hangs and optional Packet Error Checking (PEC) to ensure data integrity. In general, a master device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: Section 5: Transport. This can be found at:

www.pmbus.org

For a description of the differences between SMBus and I^2C, refer to System Management Bus (SMBus) Specification Version 2.0: Appendix B – Differences between SMBus and I^2C. This can be found at:

www.smbus.org

When using an I^2C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of a PMBus read command by concatenating a start command byte write with an I^2C read.

Device Address

The I^2C/SMBus address of the LTC2975 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V_{DD33}, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTC2975s can be connected together to control thirty six outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I^2C/SMBus device or global addresses, including I^2C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2975 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

OPERATION

Processing Commands

The LTC2975 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2975 is busy.

EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	t_{MASS_WRITE}	See Electrical Characterization table. The LTC2975 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read.
RESTORE_USER_ALL	30ms	The LTC2975 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_CLEAR	175ms	The LTC2975 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_STORE	20ms	The LTC2975 will not accept any commands while it is transferring fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read.
Internal Fault log	20ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read.
MFR_FAULT_LOG_ RESTORE	2ms	The LTC2975 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read.

*The typical delay is measured from the command's stop to the next command's start.

Other Commands

COMMAND	TYPICAL DELAY*	COMMENT
MFR_CONFIG	<50µs	The LTC2975 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.
IOUT_CAL_GAIN	<500µs	The LTC2975 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read.

*The delay is measured from the command's stop to the next command's start.

Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2975 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs.

OPERATION

Table 1. LTC2975 Address Look-Up Table with MFR_I2C_BASE_ADDRESS Set to 7bit 0x5C

ADDRESS PINS		DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS							
ASEL1	ASEL0		7-Bit	8-Bit	6	5	4	3	2	1	0	R/W
X	X	Alert Response	0C	19	0	0	0	1	1	0	0	1
X	X	Global	5B	B6	1	0	1	1	0	1	1	0
L	L	N = 0	5C*	B8	1	0	1	1	1	0	0	0
L	NC	N = 1	5D	BA	1	0	1	1	1	0	1	0
L	H	N = 2	5E	BC	1	0	1	1	1	1	0	0
NC	L	N = 3	5F	BE	1	0	1	1	1	1	1	0
NC	NC	N = 4	60	C0	1	1	0	0	0	0	0	0
NC	H	N = 5	61	C2	1	1	0	0	0	0	1	0
H	L	N = 6	62	C4	1	1	0	0	0	1	0	0
H	NC	N = 7	63	C6	1	1	0	0	0	1	1	0
H	H	N = 8	64	C8	1	1	0	0	1	0	0	0

H = Tie to V_{DD33}, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7bit 0x5C (Factory Default)

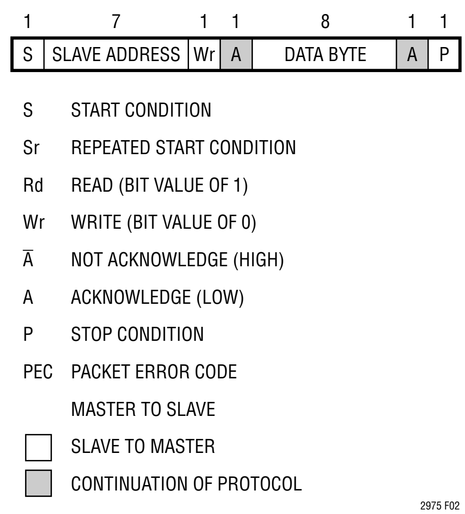


Figure 2. PMBus Packet Protocol Diagram Element Key

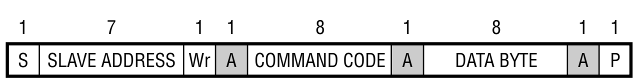


Figure 3. Write Byte Protocol

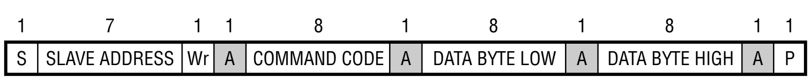


Figure 4. Write Word Protocol

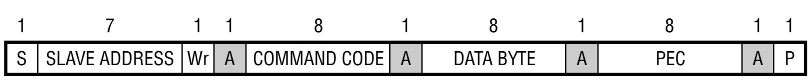


Figure 5. Write Byte Protocol with PEC

OPERATION

1	7	1	1	8	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC	A	P

2975 F06

Figure 6. Write Word Protocol with PEC

1	7	1	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	P

2975 F07

Figure 7. Send Byte Protocol

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	PEC	A	P

2975 F08

Figure 8. Send Byte Protocol with PEC

1	7	1	1	8	1	1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	$\overline{A}$	P

2975 F09

Figure 9. Read Word Protocol

1	7	1	1	8	1	1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC	$\overline{A}$	P

2975 F10

Figure 10. Read Word Protocol with PEC

1	7	1	1	8	1	1	7	1	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE	$\overline{A}$	P

2975 F11

Figure 11. Read Byte Protocol

1	7	1	1	8	1	1	7	1	1	8	1		1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE	A	PEC	$\overline{A}$	P

2975 F12

Figure 12. Read Byte Protocol with PEC

1	7	1	1	8	1	1	7	1	1	8	1	
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	BYTE COUNT = N	A	•••

8	1	8	1		8	1	1
DATA BYTE 1	A	DATA BYTE 2	A	•••	DATA BYTE N	$\overline{A}$	P

2975 F13

Figure 13. Block Read

1	7	1	1	8	1	1	7	1	1	8	1	
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	BYTE COUNT = N	A	•••

8	1	8	1		8	1	8	1	1
DATA BYTE 1	A	DATA BYTE 2	A	•••	DATA BYTE N	A	PEC	$\overline{A}$	P

2975 F14

Figure 14. Block Read with PEC

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	29
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	34
ON_OFF_CONFIG	0x02	CONTROL pin and PMBus on/off command setting.	R/W Byte	Y	Reg		Y	0x1E	35
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	64
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	30
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	45
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	45
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xB0	83
VOUT_MODE	0x20	Output voltage data format and mantissa exponent (2^{-13}).	R Byte	Y	Reg			0x13	51
VOUT_COMMAND	0x21	Servo target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	51
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	51
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	51
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	51
VIN_ON	0x35	Input voltage above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	47
VIN_OFF	0x36	Input voltage below which power conversion is disabled. All V_{OUT_EN} pins go off immediately or sequence off after TOFF_DELAY (See Mfr_config_track_en*n*).	R/W Word	N	L11	V	Y	9.0 0xD240	47
IOUT_CAL_GAIN	0x38	The nominal resistance of the current sense element in mΩ.	R/W Word	Y	L11	mΩ	Y	1.0 0xBA00	52
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	51
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	59
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	51
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	51
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Used for Ton_max_fault and power good de-assertion.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	51

Note: The data format abbreviations are detailed at the end of this table

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	59
IOUT_OC_FAULT_LIMIT	0x46	Output overcurrent fault limit.	R/W Word	Y	L11	A	Y	10.0 0xD280	60
IOUT_OC_FAULT_RESPONSE	0x47	Action to be taken by the device when an output overcurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	60
IOUT_OC_WARN_LIMIT	0x4A	Output overcurrent warning limit.	R/W Word	Y	L11	A	Y	5.0 0xCA80	52
IOUT_UC_FAULT_LIMIT	0x4B	Output undercurrent fault limit. Used to detect a reverse current and must be a negative value.	R/W Word	Y	L11	A	Y	–1.0 0xB400	52
IOUT_UC_FAULT_RESPONSE	0x4C	Action to be taken by the device when an output undercurrent fault is detected.	R/W Byte	Y	Reg		Y	0x00	60
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	65.0 0xEA08	54
OT_FAULT_RESPONSE	0x50	Action to be taken by the device when an overtemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	61
OT_WARN_LIMIT	0x51	Overtemperature warning limit for the external temperature sensor	R/W Word	Y	L11	°C	Y	60.0 0xE3C0	54
UT_WARN_LIMIT	0x52	Undertemperature warning limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	0 0x8000	54
UT_FAULT_LIMIT	0x53	Undertemperature fault limit for the external temperature sensor.	R/W Word	Y	L11	°C	Y	–5.0 0xCD80	54
UT_FAULT_RESPONSE	0x54	Action to be taken by the device when an undertemperature fault is detected on the external temperature sensor.	R/W Byte	Y	Reg		Y	0xB8	61
VIN_OV_FAULT_LIMIT	0x55	Input overvoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	15.0 0xD3C0	47
VIN_OV_FAULT_RESPONSE	0x56	Action to be taken by the device when an input overvoltage fault is detected.	R/W Byte	N	Reg		Y	0x80	61
VIN_OV_WARN_LIMIT	0x57	Input overvoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	14.0 0xD380	47
VIN_UV_WARN_LIMIT	0x58	Input undervoltage warning limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	47
VIN_UV_FAULT_LIMIT	0x59	Input undervoltage fault limit measured at VIN_SNS pin.	R/W Word	N	L11	V	Y	0 0x8000	47
VIN_UV_FAULT_RESPONSE	0x5A	Action to be taken by the device when an input undervoltage fault is detected.	R/W Byte	N	Reg		Y	0x00	61
POWER_GOOD_ON	0x5E	Output voltage at or above which a power good should be asserted.	R/W Word	Y	L16	V	Y	0.96 0x1EB8	51
POWER_GOOD_OFF	0x5F	Output voltage at or below which a power good should be de-asserted when Mfr_ config_all_pwrgd_off_uses_uv is clear.	R/W Word	Y	L16	V	Y	0.94 0x1E14	51
TON_DELAY	0x60	Time from CONTROL pin and/or OPERATION command = ON to V_{OUT_EN} pin = ON.	R/W Word	Y	L11	mS	Y	1.0 0xBA00	56

PMBUS COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE: FLOAT HEX	REF PAGE
TON_RISE	0x61	Time from when the V_{OUT_ENn} pin goes high until the LTC2975 optionally soft-connects its DAC and begins to servo the output voltage to the desired value.	R/W Word	Y	L11	mS	Y	10.0 0xD280	56
TON_MAX_FAULT_LIMIT	0x62	Maximum time from V_{OUT_EN} pin on assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results.	R/W Word	Y	L11	mS	Y	15.0 0xD3C0	56
TON_MAX_FAULT_RESPONSE	0x63	Action to be taken by the device when a TON_MAX_FAULT event is detected.	R/W Byte	Y	Reg		Y	0xB8	62
TOFF_DELAY	0x64	Time from CONTROL pin and/or OPERATION command = OFF to V_{OUT_EN} pin = OFF.	R/W Word	Y	L11	mS	Y	1.0 0xBA00	56
STATUS_BYTE	0x78	One byte summary of the unit's fault condition.	R Byte	Y	Reg			NA	65
STATUS_WORD	0x79	Two byte summary of the unit's fault condition.	R Word	Y	Reg			NA	65
STATUS_VOUT	0x7A	Output voltage fault and warning status.	R Byte	Y	Reg			NA	66
STATUS_IOUT	0x7B	Output current fault and warning status.	R Byte	Y	Reg			NA	66
STATUS_INPUT	0x7C	Input supply fault and warning status.	R Byte	N	Reg			NA	66
STATUS_TEMPERATURE	0x7D	External temperature fault and warning status for READ_TEMPERATURE_1.	R Byte	Y	Reg			NA	67
STATUS_CML	0x7E	Communication and memory fault and warning status.	R Byte	N	Reg			NA	67
STATUS_MFR_SPECIFIC	0x80	Manufacturer specific fault and state information.	R Byte	Y	Reg			NA	68
READ_VIN	0x88	Input supply voltage.	R Word	N	L11	V		NA	70
READ_IIN	0x89	DC/DC converter input current.	R Word	Y	L11	A		NA	70
READ_VOUT	0x8B	DC/DC converter output voltage.	R Word	Y	L16	V		NA	70
READ_IOUT	0x8C	DC/DC converter output current.	R Word	Y	L11	A		NA	71
READ_TEMPERATURE_1	0x8D	External diode junction temperature. This is the value used for all temperature related processing, including IOUT_CAL_GAIN.	R Word	Y	L11	°C		NA	71
READ_TEMPERATURE_2	0x8E	Internal junction temperature.	R Word	N	L11	°C		NA	71
READ_POUT	0x96	DC/DC converter output power.	R Word	Y	L11	W		NA	71
READ_PIN	0x97	DC/DC converter input power.	R Word	Y	L11	W		NA	70
PMBUS_REVISION	0x98	PMBus revision supported by this device. Current revision is 1.1.	R Byte	N	Reg			0x11	83
USER_DATA_00	0xB0	Manufacturer reserved for LTpowerPlay.	R/W Word	N	Reg		Y	NA	83
USER_DATA_01	0xB1	Manufacturer reserved for LTpowerPlay.	R/W Word	Y	Reg		Y	NA	83
USER_DATA_02	0xB2	OEM Reserved.	R/W Word	N	Reg		Y	NA	83
USER_DATA_03	0xB3	Scratchpad location.	R/W Word	Y	Reg		Y	0x0000	83
USER_DATA_04	0xB4	Scratchpad location.	R/W Word	N	Reg		Y	0x0000	83
MFR_LTC_RESERVED_1	0xB5	Manufacturer reserved.	R/W Word	Y	Reg		Y	NA	83