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# 8-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement

## FEATURES

- **Sequence, Trim, Margin and Supervise Eight Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus™ Compliant Command Set**
- **Supported by LTpowerPlay® GUI**
- **Margin or Trim Supplies to Within 0.25% of Target**
- **Fast OV/UV Supervisors Per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple LTC PSM Devices**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously without Additional Software**
- Internal Temperature and Input Voltage Supervisors
- Accurate Monitoring of Eight Output Voltages, Input Voltage and Internal Die Temperature
- $I^2C$/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Programmable Watchdog Timer
- 100% Pin-Compatible Upgrade to the LTC2978/LTC2978A
- Available in 64-Pin 9mm × 9mm QFN Package

## APPLICATIONS

- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

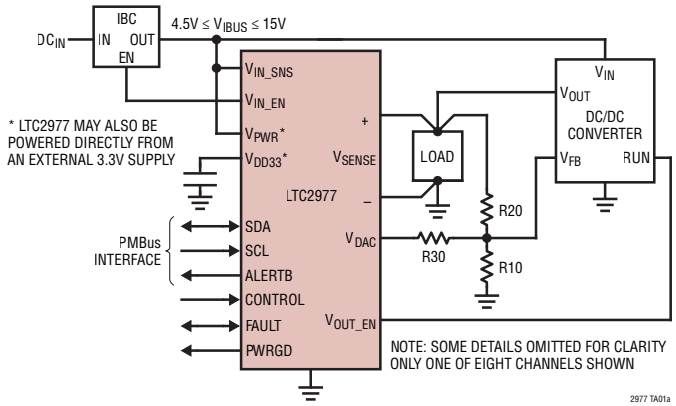
## DESCRIPTION

The LTC®2977 is an 8-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for eight power supply output channels and one power supply input channel, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors eight output voltages, one input voltage, and die temperature. In addition, odd numbered channels can be configured to measure the voltage across a current sense resistor. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC Power System Management (PSM) devices. Configuration EEPROM with ECC supports autonomous operation without additional software.

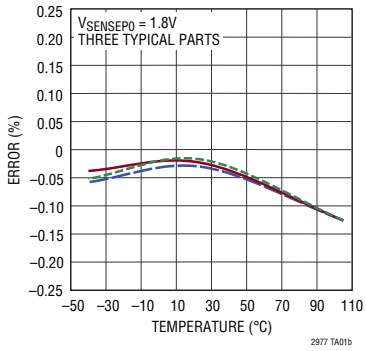


## TYPICAL APPLICATION

**8-Channel PMBus Power System Manager**




**Typical ADC Total Unadjusted Error vs Temperature**



# TABLE OF CONTENTS

# TABLE OF CONTENTS

## ABSOLUTE MAXIMUM RATINGS

**(Notes 1, 2)**

Supply Voltages:

- $V_{PWR}$ ..... –0.3V to 15V
- $V_{DD33}$ ..... –0.3V to 3.6V
- $V_{DD25}$ ..... –0.3V to 2.75V

Digital Input/Output Voltages:

- ALERTB, SDA, SCL, CONTROL0, CONTROL1 ..... –0.3V to 5.5V
- PWRGD, SHARE_CLK, WDI/RESETB, WP ..... –0.3V to $V_{DD33}$ + 0.3V
- FAULTB00, FAULTB01, FAULTB10, FAULTB11 ..... –0.3V to $V_{DD33}$ + 0.3V
- ASEL0, ASEL1 ..... –0.3V to $V_{DD33}$ + 0.3V

Analog Voltages:

- REFP ..... –0.3V to 1.35V
- REFM ..... –0.3V to 0.3V
- $V_{IN\_SNS}$ ..... –0.3V to 15V
- $V_{SENSEP[7:0]}$ ..... –0.3V to 6V
- $V_{SENSEM[7:0]}$ ..... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, $V_{IN\_EN}$ ..... –0.3V to 15V
- $V_{OUT\_EN[7:4]}$ ..... –0.3V to 6V
- $V_{DACP[7:0]}$ ..... –0.3V to 6V
- $V_{DACM[7:0]}$ ..... –0.3V to 0.3V

Operating Junction Temperature Range:

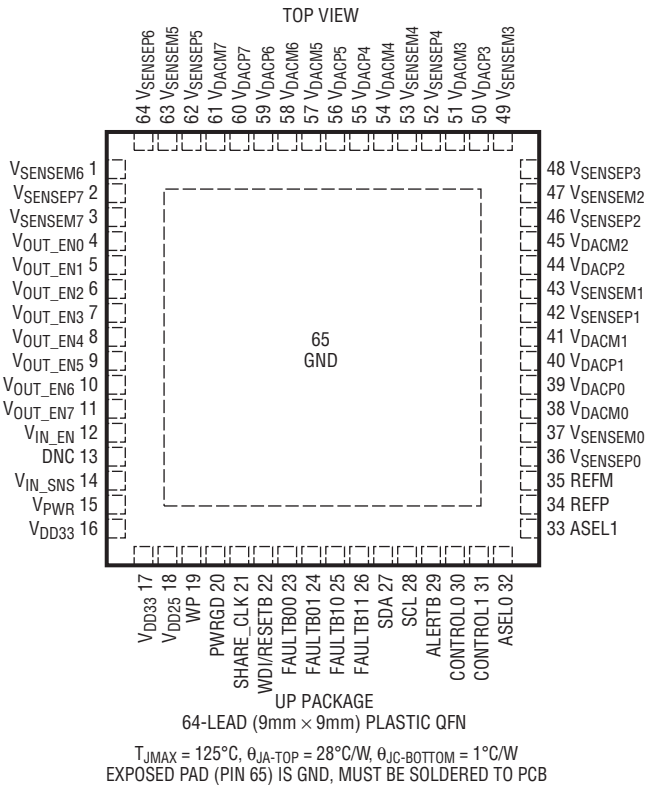
- LTC2977C ..... 0°C to 70°C
- LTC2977I ..... –40°C to 105°C

Storage Temperature Range ..... –65°C to 150°C*

Maximum Junction Temperature ..... 125°C*

*See OPERATION section for detailed EEPROM de-rating information for junction temperatures in excess of 105°C.

## PIN CONFIGURATION




UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

$T_{JMAX}$ = 125°C, $\theta_{JA-TOP}$ = 28°C/W, $\theta_{JC-BOTTOM}$ = 1°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

## ORDER INFORMATION

http://www.linear.com/product/LTC2977#orderinfo

| LEAD FREE FINISH | TAPE AND REEL | PART MARKING* | PACKAGE DESCRIPTION | JUNCTION TEMPERATURE RANGE |
|---|---|---|---|---|
| LTC2977CUP#PBF | LTC2977CUP#TRPBF | LTC2977UP | 64-Pin (9mm × 9mm) Plastic QFN | 0°C to 70°C |
| LTC2977IUP#PBF | LTC2977IUP#TRPBF | LTC2977UP | 64-Pin (9mm × 9mm) Plastic QFN | –40°C to 105°C |

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V, $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Power Supply Characteristics** | | | | | | | |
| $V_{PWR}$ | $V_{PWR}$ Supply Input Operating Range | | ● | 4.5 | | 15 | V |
| $I_{PWR}$ | $V_{PWR}$ Supply Current | 4.5V ≤ $V_{PWR}$ ≤ 15V, $V_{DD33}$ Floating | ● | | 10 | 13 | mA |
| $I_{VDD33}$ | $V_{DD33}$ Supply Current | 3.13V ≤ $V_{DD33}$ ≤ 3.47V, $V_{PWR}$ = $V_{DD33}$ | ● | | 10 | 13 | mA |
| $V_{UVLO\_VDD33}$ | $V_{DD33}$ Undervoltage Lockout | $V_{DD33}$ Ramping Up, $V_{PWR}$ = $V_{DD33}$ | ● | 2.35 | 2.55 | 2.8 | V |
| | $V_{DD33}$ Undervoltage Lockout Hysteresis | | | | 120 | | mV |
| $V_{DD33}$ | Supply Input Operating Range | $V_{PWR}$ = $V_{DD33}$ | ● | 3.13 | | 3.47 | V |
| | Regulator Output Voltage | 4.5V ≤ $V_{PWR}$ ≤ 15V | ● | 3.13 | 3.26 | 3.47 | V |
| | Regulator Output Short-Circuit Current | $V_{PWR}$ = 4.5V, $V_{DD33}$ = 0V | ● | 75 | 90 | 140 | mA |
| $V_{DD25}$ | Regulator Output Voltage | 3.13V ≤ $V_{DD33}$ ≤ 3.47V | ● | 2.35 | 2.5 | 2.6 | V |
| | Regulator Output Short-Circuit Current | $V_{PWR}$ = $V_{DD33}$ = 3.47V, $V_{DD25}$ = 0V | ● | 30 | 55 | 80 | mA |
| $t_{INIT}$ | Initialization Time | Time from $V_{IN}$ Applied Until the TON_DELAY Timer Starts | | | 30 | | ms |
| **Voltage Reference Characteristics** | | | | | | | |
| $V_{REF}$ | Output Voltage (Note 3) | $V_{REF}$ = $V_{REFP}$ – $V_{REFM}$, 0 < $I_{REFP}$ < 100µA | | | 1.232 | | V |
| | Temperature Coefficient | | | | 3 | | ppm/°C |
| | Hysteresis | (Note 4) | | | 100 | | ppm |
| **ADC Characteristics** | | | | | | | |
| $V_{IN\_ADC}$ | Voltage Sense Input Range | Differential Voltage: $V_{IN\_ADC}$ = ($V_{SENSEPn}$ – $V_{SENSEMn}$) | ● | 0 | | 6 | V |
| | | Single-Ended Voltage: $V_{SENSEMn}$ | ● | –0.1 | | 0.1 | V |
| | Current Sense Input Range (Odd Numbered Channels Only) | Single-Ended Voltage: $V_{SENSEPn}$, $V_{SENSEMn}$ | ● | –0.1 | | 6 | V |
| | | Differential Voltage: $V_{IN\_ADC}$ | ● | –170 | | 170 | mV |
| N_ADC | Voltage Sense Resolution Uses L16 Format | 0V ≤ $V_{IN\_ADC}$ ≤ 6V<br>Mfr_config_adc_hires = 0 | | | 122 | | µV/LSB |
| | Current Sense Resolution (Odd Numbered Channels Only) | 0mV ≤ \|$V_{IN\_ADC}$\| < 16mV (Note 12)<br>16mV ≤ \|$V_{IN\_ADC}$\| < 32mV<br>32mV ≤ \|$V_{IN\_ADC}$\| < 63.9mV<br>63.9mV ≤ \|$V_{IN\_ADC}$\| < 127.9mV<br>127.9mV ≤ \|$V_{IN\_ADC}$\|<br>Mfr_config_adc_hires = 1 | | | 15.625<br>31.25<br>62.5<br>125<br>250 | | µV/LSB<br>µV/LSB<br>µV/LSB<br>µV/LSB<br>µV/LSB |
| TUE_ADC_VOLT_SNS | Total Unadjusted Error (Note 3) | Voltage Sense Mode $V_{IN\_ADC}$ ≥ 1V | ● | | | ±0.25 | % of Reading |
| | | Voltage Sense Mode 0 ≤ $V_{IN\_ADC}$ ≤ 1V | ● | | | ±2.5 | mV |
| TUE_ADC_CURR_SNS | Total Unadjusted Error (Note 3) | Current Sense Mode, Odd Numbered Channels Only, 20mV ≤ $V_{IN\_ADC}$ ≤ 170mV | ● | | | ±0.7 | % of Reading |
| | | Current Sense Mode, Odd Numbered Channels Only, $V_{IN\_ADC}$ ≤ 20mV | ● | | | ±140 | µV |
| $V_{OS\_ADC}$ | Offset Error | Current Sense Mode, Odd Numbered Channels Only | ● | | | ±35 | µV |
| $t_{CONV\_ADC}$ | Conversion Time | Voltage Sense Mode (Note 5) | | | 6.15 | | ms |
| | | Current Sense Mode (Note 5) | | | 24.6 | | ms |
| | | Temperature Input (Note 5) | | | 24.6 | | ms |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V; $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| $t_{UPDATE\_ADC}$ | Update Time | Odd Numbered Channels in Current Sense Mode (Note 5) | | | | 160 | | ms |
| $C_{IN\_ADC}$ | Input Sampling Capacitance | | | | | 1 | | pF |
| $f_{IN\_ADC}$ | Input Sampling Frequency | | | | | 62.5 | | kHz |
| $I_{IN\_ADC}$ | Input Leakage Current | $V_{IN\_ADC}$ = 0V, 0V ≤ $V_{COMMONMODE}$ ≤ 6V, Current Sense Mode | | ● | | | ±0.5 | µA |
| | Differential Input Current | $V_{IN\_ADC}$ = 0.17V, Current Sense Mode | | ● | | 80 | 250 | nA |
| | | $V_{IN\_ADC}$ = 6V, Voltage Sense Mode | | ● | | 10 | 15 | µA |
| **DAC Output Characteristics** | | | | | | | | |
| $N\_V_{DACP}$ | Resolution | | | | | 10 | | Bits |
| $V_{FS\_VDACP}$ | Full-Scale Output Voltage (Programmable) | DAC Code = 0x3FF<br>DAC Polarity = 1 | Buffer Gain Setting_0<br>Buffer Gain Setting_1 | ●<br>● | 1.32<br>2.53 | 1.38<br>2.65 | 1.44<br>2.77 | V<br>V |
| $INL\_V_{DACP}$ | Integral Nonlinearity | (Note 6) | | ● | | | ±2 | LSB |
| $DNL\_V_{DACP}$ | Differential Nonlinearity | (Note 6) | | ● | | | ±2.4 | LSB |
| $V_{OS\_VDACP}$ | Offset Voltage | (Note 6) | | ● | | | ±10 | mV |
| $V_{DACP}$ | Load Regulation ($V_{DACPn}$ – $V_{DACMn}$) | $V_{DACPn}$ = 2.65V, $I_{VDACPn}$ Sourcing = 2mA | | | | 100 | | ppm/mA |
| | | $V_{DACPn}$ = 0.1V, $I_{VDACPn}$ Sinking = 2mA | | | | 100 | | ppm/mA |
| | PSRR ($V_{DACPn}$ – $V_{DACMn}$) | DC: 3.13V ≤ $V_{DD33}$ ≤ 3.47V, $V_{PWR}$ = $V_{DD33}$ | | | | 60 | | dB |
| | | 100mV Step in 20ns with 50pF Load | | | | 40 | | dB |
| | DC CMRR ($V_{DACPn}$ – $V_{DACMn}$) | –0.1V ≤ $V_{DACMn}$ ≤ 0.1V | | | | 60 | | dB |
| | Leakage Current | $V_{DACPn}$ Hi-Z, 0V ≤ $V_{DACPn}$ ≤ 6V | | ● | | | ±100 | nA |
| | Short-Circuit Current Low | $V_{DACPn}$ Shorted to GND | | ● | –10 | | –4 | mA |
| | Short-Circuit Current High | $V_{DACPn}$ Shorted to $V_{DD33}$ | | ● | 4 | | 10 | mA |
| $C_{OUT}$ | Output Capacitance | $V_{DACPn}$ Hi-Z | | | | 10 | | pF |
| $t_{S\_VDACP}$ | DAC Output Update Rate | Fast Servo Mode | | | | 500 | | µs |
| **Voltage Supervisor Characteristics** | | | | | | | | |
| $V_{IN\_VS}$ | Input Voltage Range (Programmable) | $V_{IN\_VS}$ = ($V_{SENSEPn}$ – $V_{SENSEMn}$) | Low Resolution Mode<br>High Resolution Mode | ●<br>● | 0<br>0 | | 6<br>3.8 | V<br>V |
| | | Single-Ended Voltage: $V_{SENSEMn}$ | | ● | –0.1 | | 0.1 | V |
| N_VS | Voltage Sensing Resolution | 0V to 3.8V Range: High Resolution Mode | | | | 4 | | mV/LSB |
| | | 0V to 6V Range: Low Resolution Mode | | | | 8 | | mV/LSB |
| TUE_VS | Total Unadjusted Error | 2V ≤ $V_{IN\_VS}$ ≤ 6V, Low Resolution Mode | | ● | | | ±1.25 | % of Reading |
| | | 1.5V < $V_{IN\_VS}$ ≤ 3.8V, High Resolution Mode | | ● | | | ±1.0 | % of Reading |
| | | 0.8V ≤ $V_{IN\_VS}$ ≤ 1.5V, High Resolution Mode | | ● | | | ±1.5 | % of Reading |
| $t_{S\_VS}$ | Update Period | | | | | 12.21 | | µs |
| **$V_{IN\_SNS}$ Input Characteristics** | | | | | | | | |
| $V_{VIN\_SNS}$ | $V_{IN\_SNS}$ Input Voltage Range | | | ● | 0 | | 15 | V |
| $R_{VIN\_SNS}$ | $V_{IN\_SNS}$ Input Resistance | | | ● | 70 | 90 | 110 | kΩ |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V; $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $TUE_{VIN\_SNS}$ | VIN_ON, VIN_OFF Threshold Total Unadjusted Error | 3V ≤ $V_{VIN\_SNS}$ ≤ 8V | ● | | | ±2.0 | % of Reading |
| | | $V_{VIN\_SNS}$ > 8V | ● | | | ±1.0 | |
| | READ_VIN Total Unadjusted Error | 3V ≤ $V_{VIN\_SNS}$ ≤ 8V | ● | | | ±1.5 | % of Reading |
| | | $V_{VIN\_SNS}$ > 8V | ● | | | ±1.0 | |
| **DAC Soft-Connect Comparator Characteristics** | | | | | | | |
| $V_{OS\_CMP}$ | Offset Voltage | $V_{DACP}$*n* = 0.2V | ● | | ±1 | ±18 | mV |
| | | $V_{DACP}$*n* = 1.3V | ● | | ±2 | ±26 | mV |
| | | $V_{DACP}$*n* = 2.65V | ● | | ±3 | ±52 | mV |
| **Temperature Sensor Characteristics** | | | | | | | |
| TUE_TS | Total Unadjusted Error | | | | ±1 | | °C |
| **$V_{OUT}$ Enable Output ($V_{OUT\_EN}$ [3:0]) Characteristics** | | | | | | | |
| $V_{VOUT\_EN}$*n* | Output High Voltage (Note 11) | $I_{VOUT\_EN}$*n* = –5µA, $V_{DD33}$ = 3.3V | ● | 10 | 12.5 | 14.7 | V |
| $I_{VOUT\_EN}$*n* | Output Sourcing Current | $V_{VOUT\_EN}$*n* Pull-Up Enabled, $V_{VOUT\_EN}$*n* = 1V | ● | –5 | –6 | –8 | µA |
| | Output Sinking Current | Strong Pull-Down Enabled, $V_{VOUT\_EN}$*n* = 0.4V | ● | 3 | 5 | 8 | mA |
| | | Weak Pull-Down Enabled, $V_{VOUT\_EN}$*n* = 0.4V | ● | 33 | 50 | 60 | µA |
| | Output Leakage Current | Internal Pull-Up Disabled, 0V ≤ $V_{VOUT\_ENn}$ ≤ 15V | ● | | | ±1 | µA |
| $V_{VOUT\_VALID}$ | Minimum $V_{DD33}$ when $V_{VOUT\_EN}$*n* Valid | $V_{VOUT\_EN}$*n* ≤ 0.4V | ● | | | 1.1 | V |
| **$V_{OUT}$ Enable Output ($V_{OUT\_EN}$ [7:4]) Characteristics** | | | | | | | |
| $I_{VOUT\_EN}$*n* | Output Sinking Current | Strong Pull-Down Enabled, $V_{OUT\_EN}$*n* = 0.1V | ● | 3 | 6 | 9 | mA |
| | Output Leakage Current | 0V ≤ $V_{VOUT\_ENn}$ ≤ 6V | ● | | | ±1 | µA |
| $V_{VOUT\_VALID}$ | Minimum $V_{DD33}$ when $V_{VOUT\_EN}$*n* Valid | $V_{VOUT\_EN}$*n* ≤ 0.4V | ● | | | 1.1 | V |
| **$V_{IN}$ Enable Output ($V_{IN\_EN}$) Characteristics** | | | | | | | |
| $V_{VIN\_EN}$ | Output High Voltage | $I_{VIN\_EN}$ = –5µA, $V_{DD33}$ = 3.3V | ● | 10 | 12.5 | 14.7 | V |
| $I_{VIN\_EN}$ | Output Sourcing Current | $V_{IN\_EN}$ Pull-Up Enabled, $V_{VIN\_EN}$ = 1V | ● | –5 | –6 | –8 | µA |
| | Output Sinking Current | $V_{VIN\_EN}$ = 0.4V | ● | 3 | 5 | 8 | mA |
| | Leakage Current | Internal Pull-Up Disabled, 0V ≤ $V_{VIN\_EN}$ ≤ 15V | ● | | | ±1 | µA |
| **EEPROM Characteristics** | | | | | | | |
| Endurance | (Notes 7, 10) | 0°C < $T_J$ < 85°C During EEPROM Write Operations | ● | 10,000 | | | Cycles |
| Retention | (Notes 7, 10) | $T_J$ < 105°C | ● | 20 | | | Years |
| $t_{MASS\_WRITE}$ | Mass Write Operation Time (Note 8) | STORE_USER_ALL, 0°C < $T_J$ < 85°C During EEPROM Write Operations | ● | | 440 | 4100 | ms |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V; $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | ● | 2.1 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | ● | | | 1.5 | V |
| $V_{HYST}$ | Input Hysteresis | | | | 20 | | mV |
| $I_{LEAK}$ | Input Leakage Current | 0V ≤ $V_{PIN}$ ≤ 5.5V, SDA, SCL, CONTROL*n* Pins Only | ● | | | ±2 | µA |
| | | 0V ≤ $V_{PIN}$ ≤ $V_{DD33}$ + 0.3V, FAULTB*zn*, WDI/RESETB, WP Pins Only | ● | | | ±2 | µA |
| $t_{SP}$ | Pulse Width of Spike Suppressed | FAULTB*zn*, CONTROL*n* Pins Only | | | 10 | | µs |
| | | SDA, SCL Pins Only | | | 98 | | ns |
| $t_{FAULT\_MIN}$ | Minimum Low Pulse Width for Externally Generated Faults | | | 110 | | | ms |
| $t_{RESETB}$ | Pulse Width to Assert Reset | $V_{WDI/RESETB}$ ≤ 1.5V | ● | 300 | | | µs |
| $t_{WDI}$ | Pulse Width to Reset Watchdog Timer | $V_{WDI/RESETB}$ ≤ 1.5V | ● | 0.3 | | 200 | µs |
| $f_{WDI}$ | Watchdog Interrupt Input Frequency | | ● | | | 1 | MHz |
| $C_{IN}$ | Digital Input Capacitance | | | | 10 | | pF |
| **Digital Input SHARE_CLK** | | | | | | | |
| $V_{IH}$ | High Level Input Voltage | | ● | 1.6 | | | V |
| $V_{IL}$ | Low Level Input Voltage | | ● | | | 0.8 | V |
| $f_{SHARE\_CLK\_IN}$ | Input Frequency Operating Range | | ● | 90 | | 110 | kHz |
| $t_{LOW}$ | Assertion Low Time | $V_{SHARE\_CLK}$ < 0.8V | ● | 0.825 | | 1.1 | µs |
| $t_{RISE}$ | Rise Time | $V_{SHARE\_CLK}$ < 0.8V to $V_{SHARE\_CLK}$ > 1.6V | ● | | | 450 | ns |
| $I_{LEAK}$ | Input Leakage Current | 0V ≤ $V_{SHARE\_CLK}$ ≤ $V_{DD33}$ + 0.3V | ● | | | ±1 | µA |
| $C_{IN}$ | Input Capacitance | | | | 10 | | pF |
| **Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11** | | | | | | | |
| $V_{OL}$ | Digital Output Low Voltage | $I_{SINK}$ = 3mA | ● | | | 0.4 | V |
| $f_{SHARE\_CLK\_OUT}$ | Output Frequency Operating Range | 5.49kΩ Pull-Up to $V_{DD33}$ | ● | 90 | 100 | 110 | kHz |
| **Digital Inputs ASEL0,ASEL1** | | | | | | | |
| $V_{IH}$ | Input High Threshold Voltage | | ● | $V_{DD33}$ – 0.5 | | | V |
| $V_{IL}$ | Input Low Threshold Voltage | | ● | | | 0.5 | V |
| $I_{IH,IL}$ | High, Low Input Current | ASEL[1:0] = 0, $V_{DD33}$ | ● | | | ±95 | µA |
| $I_{HIZ}$ | Hi-Z Input Current | | ● | | | ±24 | µA |
| $C_{IN}$ | Input Capacitance | | | | 10 | | pF |
| **Serial Bus Timing Characteristics** | | | | | | | |
| $f_{SCL}$ | Serial Clock Frequency (Note 9) | | ● | 10 | | 400 | kHz |
| $t_{LOW}$ | Serial Clock Low Period (Note 9) | | ● | 1.3 | | | µs |
| $t_{HIGH}$ | Serial Clock High Period (Note 9) | | ● | 0.6 | | | µs |
| $t_{BUF}$ | Bus Free Time Between Stop and Start (Note 9) | | ● | 1.3 | | | µs |
| $t_{HD,STA}$ | Start Condition Hold Time (Note 9) | | ● | 600 | | | ns |
| $t_{SU,STA}$ | Start Condition Setup Time (Note 9) | | ● | 600 | | | ns |
| $t_{SU,STO}$ | Stop Condition Setup Time (Note 9) | | ● | 600 | | | ns |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at $T_J$ = 25°C. $V_{PWR}$ = $V_{IN\_SNS}$ = 12V; $V_{DD33}$, $V_{DD25}$, REFP and REFM pins floating, unless otherwise indicated. $C_{VDD33}$ = 100nF, $C_{VDD25}$ = 100nF and $C_{REF}$ = 100nF. (Note 2)**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $t_{HD,DAT}$ | Data Hold Time (LTC2977 Receiving Data) (Note 9) | | ● | 0 | | | ns |
| | Data Hold Time (LTC2977 Transmitting Data) (Note 9) | | ● | 300 | | 900 | ns |
| $t_{SU,DAT}$ | Data Setup Time (Note 9) | | ● | 100 | | | ns |
| $t_{SP}$ | Pulse Width of Spike Suppressed (Note 9) | | | | 98 | | ns |
| $t_{TIMEOUT\_BUS}$ | Time Allowed to Complete any PMBus Command After Which Time SDA Will Be Released and Command Terminated | Mfr_config_all_longer_pmbus_timeout = 0<br>Mfr_config_all_longer_pmbus_timeout = 1 | ●<br>● | | 25<br>200 | 35<br>280 | ms<br>ms |
| **Additional Digital Timing Characteristics** | | | | | | | |
| $t_{OFF\_MIN}$ | Minimum Off Time for Any Channel | | | | 100 | | ms |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified. If power is supplied to the chip via the $V_{DD33}$ pin only, connect $V_{PWR}$ and $V_{DD33}$ pins together.

**Note 3:** The ADC total unadjusted error includes all error sources. First, a two-point analog trim is performed to achieve a flat reference voltage ($V_{REF}$) over temperature. This results in minimal temperature coefficient, but the absolute voltage can still vary. To compensate for this, a high-resolution, drift-free, and noiseless digital trim is applied at the output of the ADC, resulting in a very high accuracy measurement.

**Note 4:** Hysteresis in the output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 105°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

**Note 5:** The time between successive ADC conversions (latency of the ADC) for any given channel is given as: 36.9ms + (6.15ms • number of ADC channels configured in Low Resolution mode) + (24.6ms • number of ADC channels configured in High Resolution mode).

**Note 6:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

**Note 7:** EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

**Note 8:** The LTC2977 will not acknowledge any PMBus commands except for MFR_COMMON, while a mass write operation is being executed. This includes the STORE_USER_ALL and MFR_FAULT_LOG_STORE commands or a fault log store initiated by a channel faulting off.

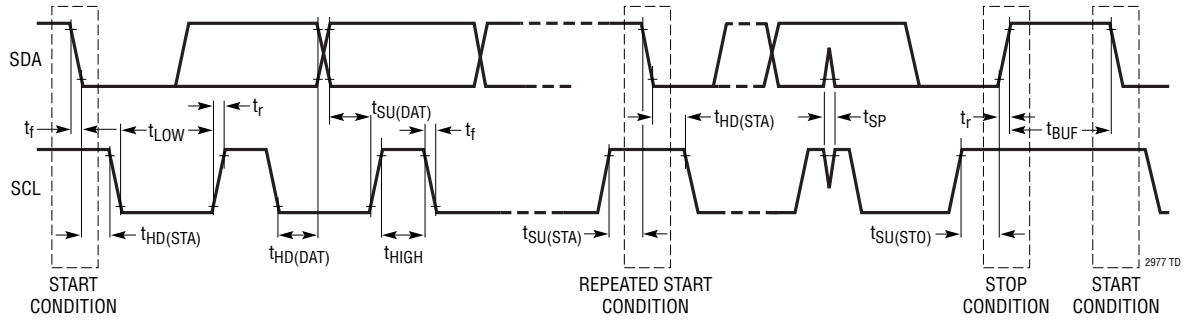
**Note 9:** Maximum capacitive load, $C_B$, for SCL and SDA is 400pF. Data and clock rise time ($t_r$) and fall time ($t_f$) are: (20 + 0.1 • $C_B$) (ns) < $t_r$ < 300ns and (20 + 0.1 • $C_B$) (ns) < $t_f$ < 300ns. $C_B$ = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, $V_{IO}$, is 3.13V < $V_{IO}$ < 5.5V.

**Note 10:** EEPROM endurance and retention will be degraded when $T_J$ > 105°C.

**Note 11:** Output enable pins are charge-pumped from $V_{DD33}$.

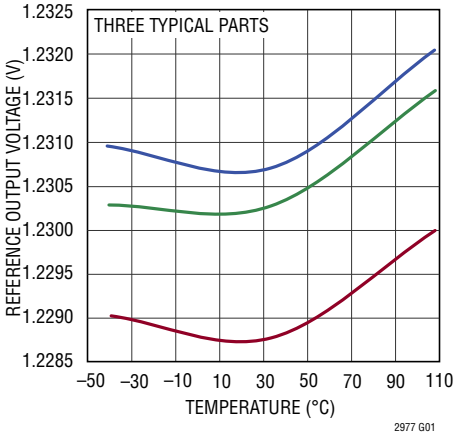
**Note 12:** The current sense resolution is determined by the L11 format and the mV units of the returned value. For example, a full-scale value of 170mV returns an L11 value of 0xF2A8 = 680 • $2^{-2}$ = 170. This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is $2^{-2}$ mV = 250µV. Each successively lower range improves resolution by cutting the LSB size in half.

## PMBUS TIMING DIAGRAM

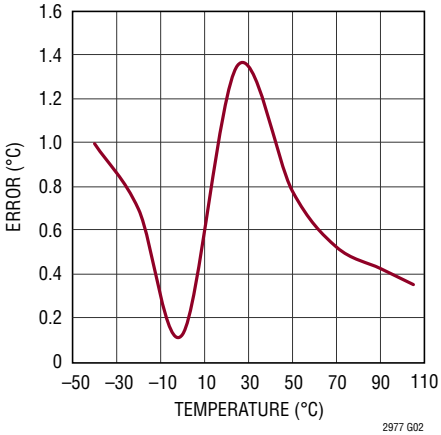


# TYPICAL PERFORMANCE CHARACTERISTICS

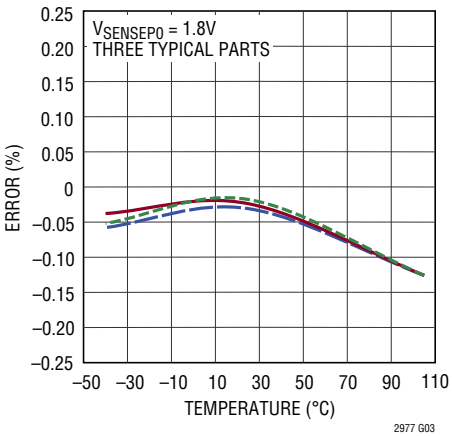
### Reference Voltage vs Temperature



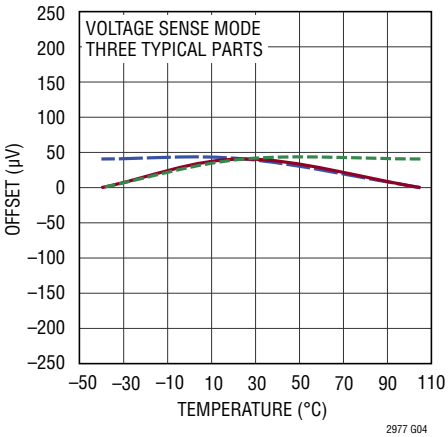

### Temperature Sensor Error vs Temperature



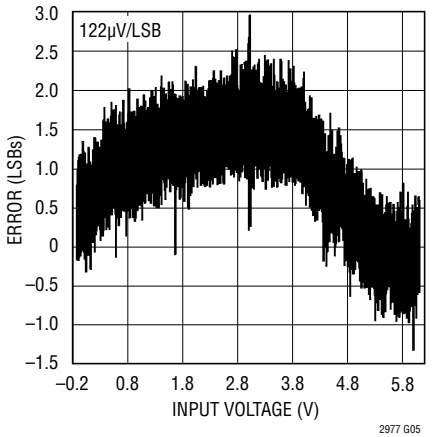

### ADC Total Unadjusted Error vs Temperature



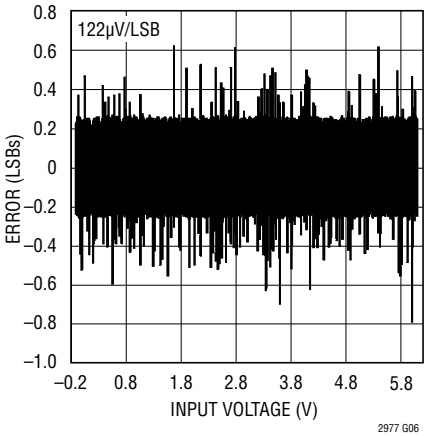

### ADC Zero Code Center Offset Voltage vs Temperature



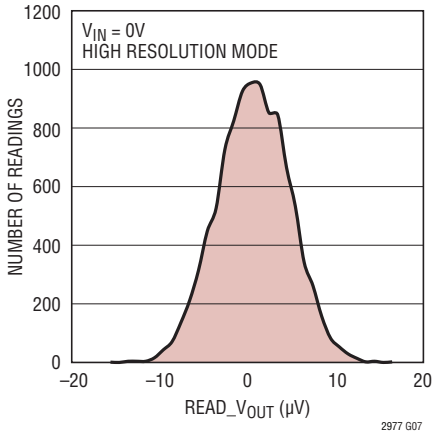

### ADC-INL



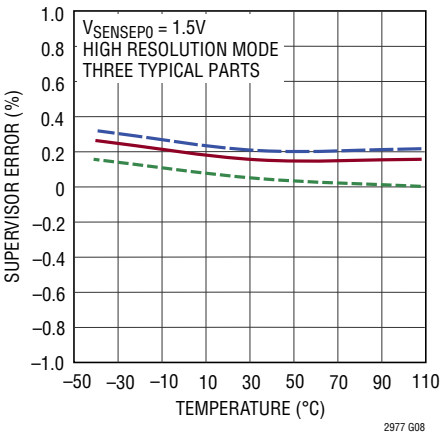

### ADC-DNL



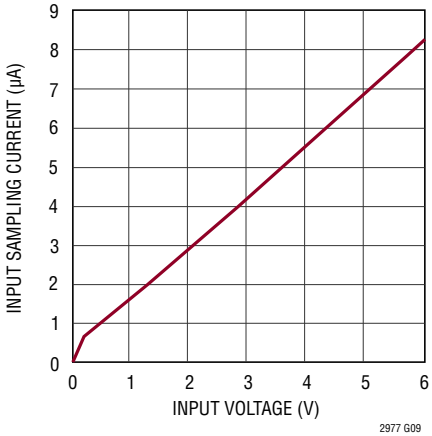

### ADC Noise Histogram




### Voltage Supervisor Total Unadjusted Error vs Temperature

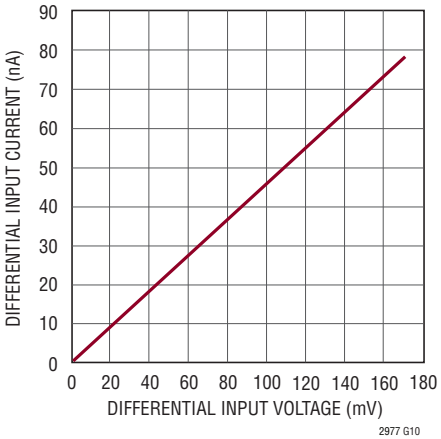



### Input Sampling Current vs Differential Input Voltage

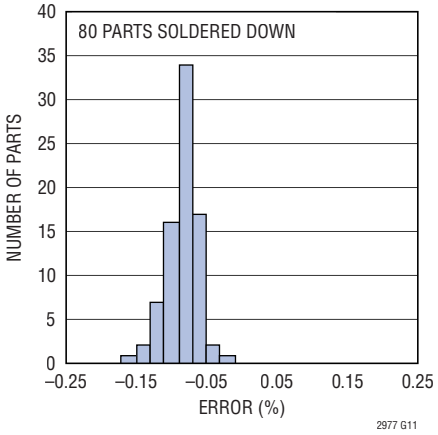


# TYPICAL PERFORMANCE CHARACTERISTICS

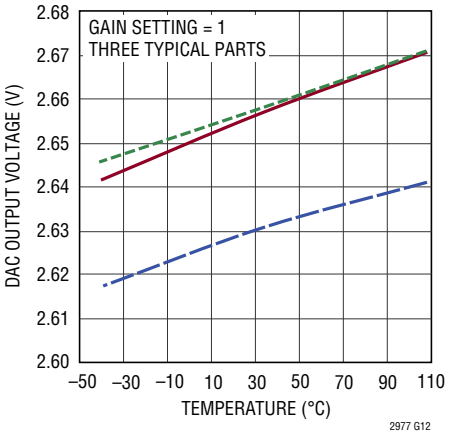
### ADC High Resolution Mode Differential Input Current



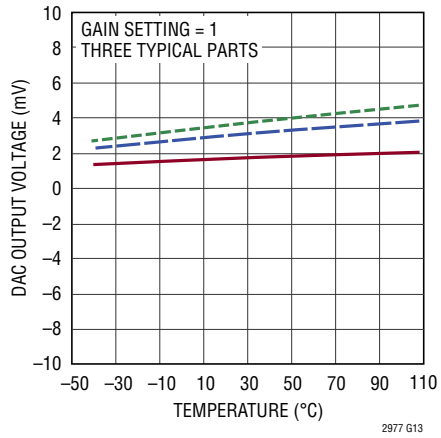

### Closed-Loop Servo Error



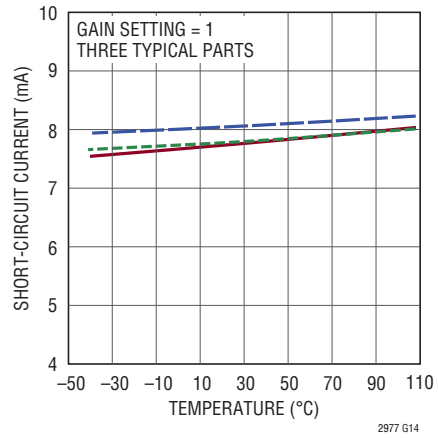

### DAC Full-Scale Output Voltage vs Temperature



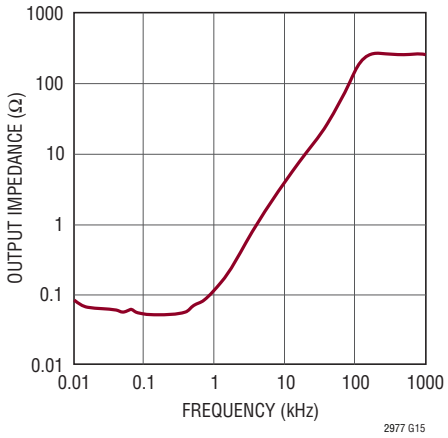

### DAC Offset Voltage vs Temperature



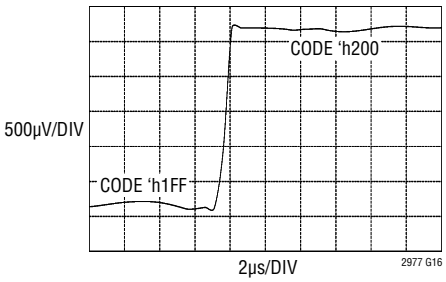

### DAC Short-Circuit Current vs Temperature



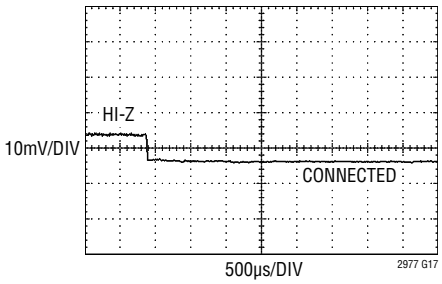

### DAC Output Impedance vs Frequency




### DAC Transient Response to 1LSB DAC Code Change

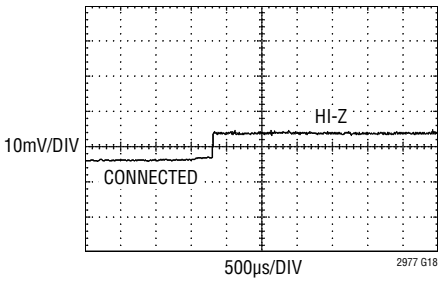



### DAC Soft-Connect Transient Response when Transitioning from Hi-Z State to ON State




100k SERIES RESISTANCE ON
CODE: 'h1FF

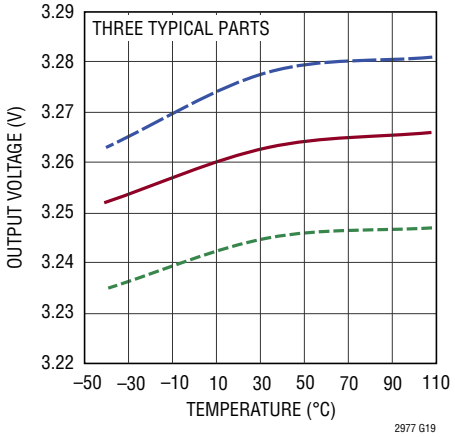
### DAC Soft-Connect Transient Response when Transitioning from ON State to Hi-Z State



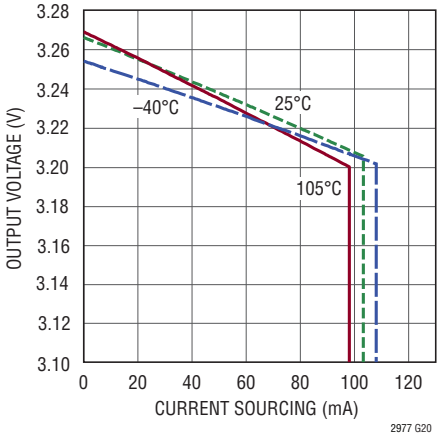

100k SERIES RESISTANCE ON
CODE: 'h1FF

# TYPICAL PERFORMANCE CHARACTERISTICS

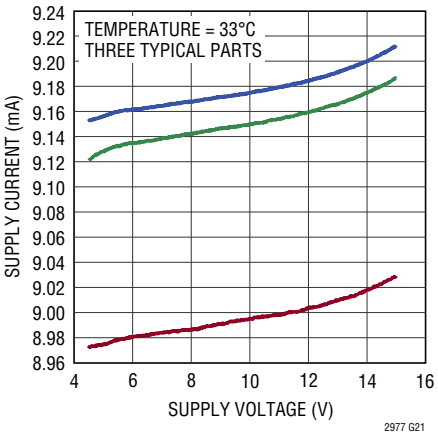
**$V_{DD33}$ Regulator Output Voltage vs Temperature**



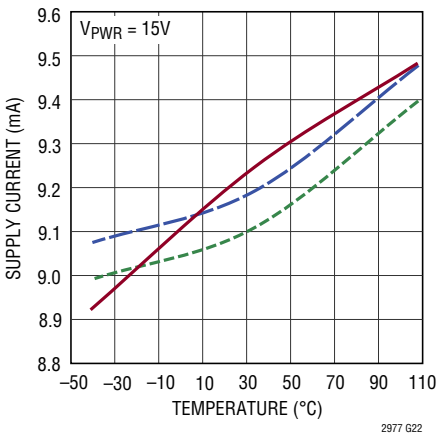

**$V_{DD33}$ Regulator Load Regulation**



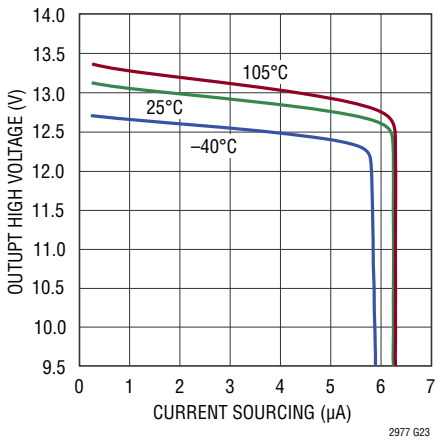

**Supply Current vs Supply Voltage**



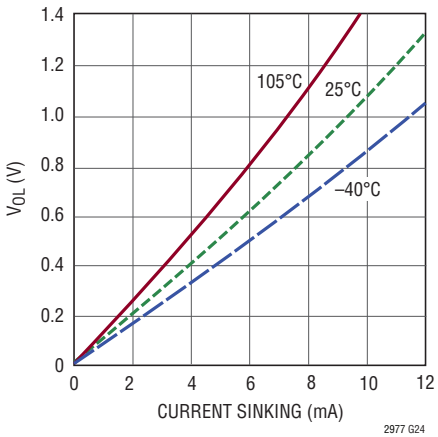

**Supply Current vs Temperature**



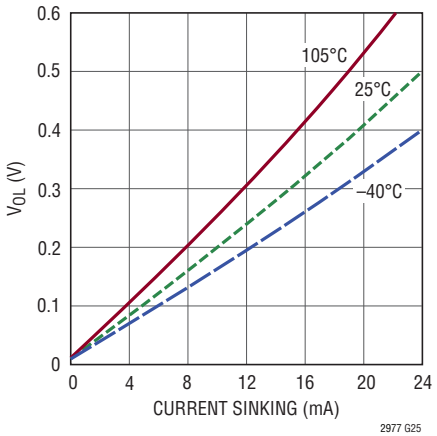

**$V_{OUT\_EN[3:0]}$ and $V_{IN\_EN}$ Output High Voltage vs Current**



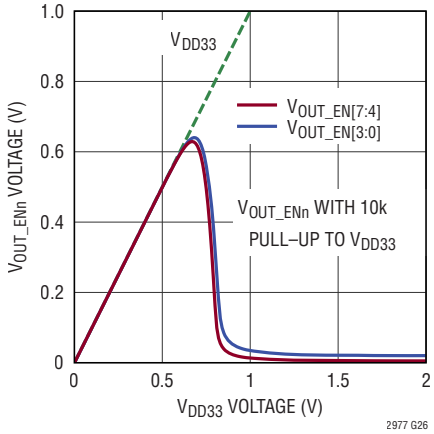

**$V_{OUT\_EN[3:0]}$ and $V_{IN\_EN}$ Output $V_{OL}$ vs Current**




**$V_{OUT\_EN[7:4]}$ $V_{OL}$ vs Current**




**$V_{OUT\_EN[7:0]}$ Output Voltage vs $V_{DD33}$**



## PIN FUNCTIONS

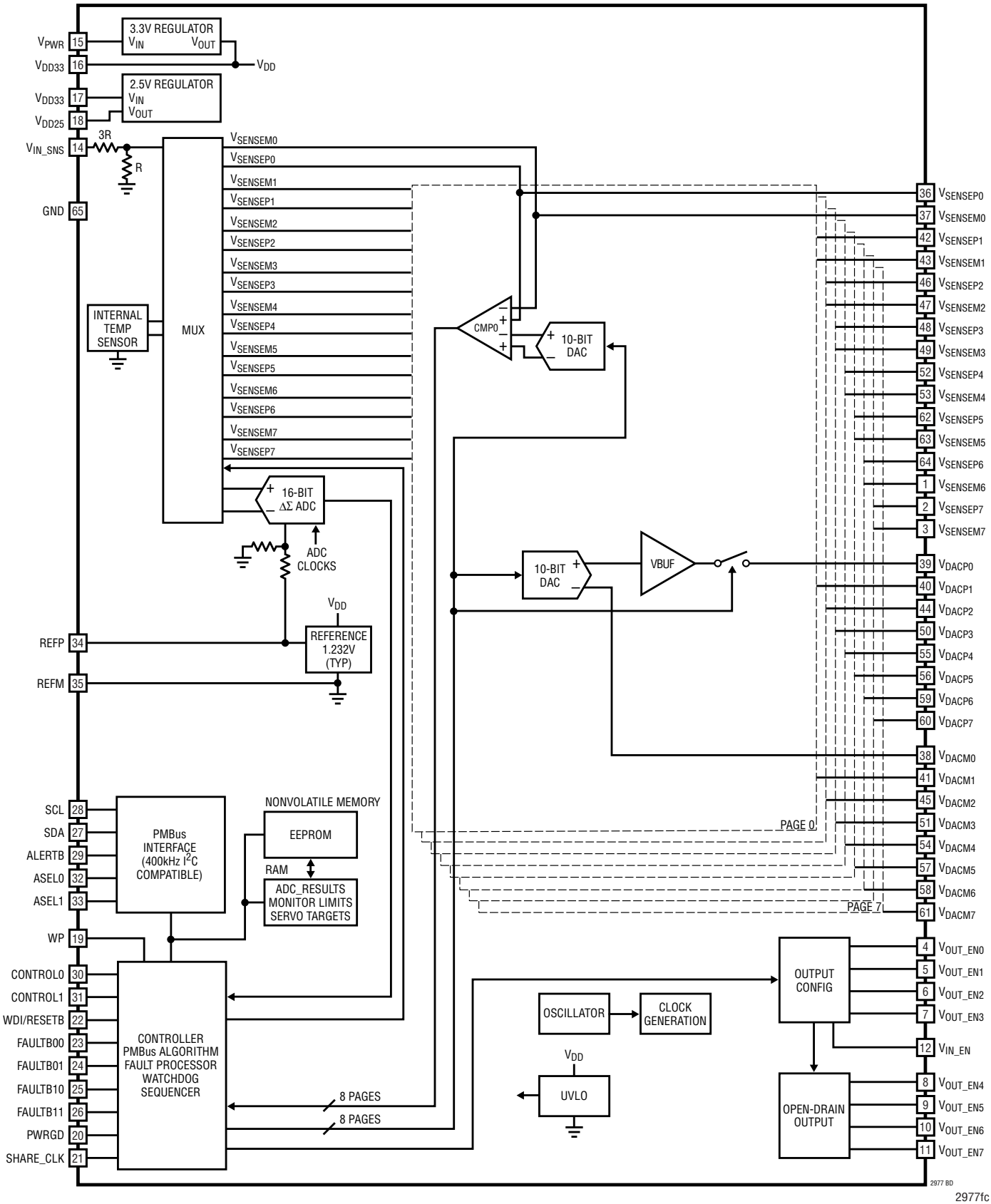
| PIN NAME | PIN NUMBER | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| $V_{SENSEM6}$ | 1* | In | DC/DC Converter Differential (–) Output Voltage-6 Sensing Pin |
| $V_{SENSEP7}$ | 2* | In | DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin |
| $V_{SENSEM7}$ | 3* | In | DC/DC Converter Differential (–) Output Voltage or Current-7 Sensing Pin |
| $V_{OUT\_EN0}$ | 4 | Out | DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA |
| $V_{OUT\_EN1}$ | 5 | Out | DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA |
| $V_{OUT\_EN2}$ | 6 | Out | DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA |
| $V_{OUT\_EN3}$ | 7 | Out | DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA |
| $V_{OUT\_EN4}$ | 8 | Out | DC/DC Converter Enable-4 Pin. Open-Drain Pull-Down Output. |
| $V_{OUT\_EN5}$ | 9 | Out | DC/DC Converter Enable-5 Pin. Open-Drain Pull-Down Output. |
| $V_{OUT\_EN6}$ | 10 | Out | DC/DC Converter Enable-6 Pin. Open-Drain Pull-Down Output. |
| $V_{OUT\_EN7}$ | 11 | Out | DC/DC Converter Enable-7 Pin. Open-Drain Pull-Down Output. |
| $V_{IN\_EN}$ | 12 | Out | DC/DC Converter $V_{IN}$ ENABLE Pin. Output High Voltage Optionally Pulled Up to 12V by 5µA |
| DNC | 13 | Do Not Connect | Do Not Connect to This Pin |
| $V_{IN\_SNS}$ | 14 | In | $V_{IN}$ SENSE Input. This Voltage is Compared Against the $V_{IN}$ On and Off Voltage Thresholds in Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters. |
| $V_{PWR}$ | 15 | In | $V_{PWR}$ Serves as the Unregulated Power Supply Input to the Chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short $V_{PWR}$ to $V_{DD33}$ and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1µF Capacitor. |
| $V_{DD33}$ | 16 | In/Out | If Shorted to $V_{PWR}$, it Serves as 3.13V to 3.47V Supply Input Pin. Otherwise, it is a 3.3V Internally Regulated Voltage Output (Use 0.1µF Decoupling Capacitor to GND). If using the internal regulator to provide $V_{DD33}$, do not connect to $V_{DD33}$ pins of any other devices. |
| $V_{DD33}$ | 17 | In | Input for Internal 2.5V Sub-Regulator. Short This Pin to Pin 16. If using the internal regulator to provide $V_{DD33}$, do not connect to $V_{DD33}$ pins of any other devices. |
| $V_{DD25}$ | 18 | In/Out | 2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor. Do not connect to $V_{DD25}$ pins of any other devices. |
| WP | 19 | In | Digital Input. Write-Protect Input Pin, Active High. |
| PWRGD | 20 | Out | Power Good Open-Drain Output. Indicates When Outputs are Power Good. Can be Used as System Power-On Reset. |
| SHARE_CLK | 21 | In/Out | Bidirectional Clock Sharing Pin. Connect a 5.49k Pull-Up Resistor to $V_{DD33}$. Connect to all other SHARE_CLK pins in the system. |
| WDI/RESETB | 22 | In | Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k Pull-Up Resistor to $V_{DD33}$. Rising Edge Resets Watchdog Counter. Holding This Pin Low for More Than $t_{RESETB}$ Resets the Chip. |
| FAULTB00 | 23 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-00. Connect a 10k Pull-Up Resistor to $V_{DD33}$. |
| FAULTB01 | 24 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-01. Connect a 10k Pull-Up Resistor to $V_{DD33}$. |
| FAULTB10 | 25 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-10. Connect a 10k Pull-Up Resistor to $V_{DD33}$. |
| FAULTB11 | 26 | In/Out | Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-11. Connect a 10k Pull-Up Resistor to $V_{DD33}$. |
| SDA | 27 | In/Out | PMBus Bidirectional Serial Data Pin |
| SCL | 28 | In | PMBus Serial Clock Input Pin (400kHz Maximum) |
| ALERTB | 29 | Out | Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation. |
| CONTROL0 | 30 | In | Control Pin 0 Input |
| CONTROL1 | 31 | In | Control Pin 1 Input |
| ASEL0 | 32 | In | Ternary Address Select Pin 0 Input. Connect to $V_{DD33}$, GND or Float to Encode 1 of 3 Logic States. |
| ASEL1 | 33 | In | Ternary Address Select Pin 1 Input. Connect to $V_{DD33}$, GND or Float to Encode 1 of 3 Logic States. |
| REFP | 34 | Out | Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM. |
| REFM | 35 | Out | Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP. |
| $V_{SENSEP0}$ | 36* | In | DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin |
| $V_{SENSEM0}$ | 37* | In | DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin |

## PIN FUNCTIONS

| PIN NAME | PIN NUMBER | PIN TYPE | DESCRIPTION |
|---|---|---|---|
| $V_{DACM0}$ | 38 | Out | DAC0 Return. Connect to Channel 0 DC/DC Converter's GND Sense or Return to GND. |
| $V_{DACP0}$ | 39 | Out | DAC0 Output |
| $V_{DACP1}$ | 40 | Out | DAC1 Output |
| $V_{DACM1}$ | 41 | Out | DAC1 Return. Connect to Channel 1 DC/DC Converter's GND Sense or Return to GND. |
| $V_{SENSEP1}$ | 42* | In | DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins |
| $V_{SENSEM1}$ | 43* | In | DC/DC Converter Differential (–) Output Voltage or Current-1 Sensing Pins |
| $V_{DACP2}$ | 44 | Out | DAC2 Output |
| $V_{DACM2}$ | 45 | Out | DAC2 Return. Connect to Channel 2 DC/DC Converter's GND Sense or Return to GND. |
| $V_{SENSEP2}$ | 46* | In | DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin |
| $V_{SENSEM2}$ | 47* | In | DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin |
| $V_{SENSEP3}$ | 48* | In | DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins |
| $V_{SENSEM3}$ | 49* | In | DC/DC Converter Differential (–) Output Voltage or Current-3 Sensing Pins |
| $V_{DACP3}$ | 50 | Out | DAC3 Output |
| $V_{DACM3}$ | 51 | Out | DAC3 Return. Connect to Channel 3 DC/DC Converter's GND Sense or Return to GND. |
| $V_{SENSEP4}$ | 52* | In | DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin |
| $V_{SENSEM4}$ | 53* | In | DC/DC Converter Differential (–) Output Voltage-4 Sensing Pin |
| $V_{DACM4}$ | 54 | Out | DAC4 Return. Connect to Channel 4 DC/DC Converter's GND Sense or Return to GND. |
| $V_{DACP4}$ | 55 | Out | DAC4 Output |
| $V_{DACP5}$ | 56 | Out | DAC5 Output |
| $V_{DACM5}$ | 57 | Out | DAC5 Return. Connect to Channel 5 DC/DC Converter's GND Sense or Return to GND. |
| $V_{DACM6}$ | 58 | Out | DAC6 Return. Connect to Channel 6 DC/DC Converter's GND Sense or Return to GND. |
| $V_{DACP6}$ | 59 | Out | DAC6 Output |
| $V_{DACP7}$ | 60 | Out | DAC7 Output |
| $V_{DACM7}$ | 61 | Out | DAC7 Return. Connect to Channel 7 DC/DC Converter's GND Sense or Return to GND. |
| $V_{SENSEP5}$ | 62* | In | DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins |
| $V_{SENSEM5}$ | 63* | In | DC/DC Converter Differential (–) Output Voltage or Current-5 Sensing Pins |
| $V_{SENSEP6}$ | 64* | In | DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin |
| GND | 65 | Ground | Exposed Pad, Must be Soldered to PCB |

*Any unused $V_{SENSEPn}$ or $V_{SENSEMn}$ or $V_{DACMn}$ pins must be tied to GND.

# BLOCK DIAGRAM



# OPERATION

## OPERATION OVERVIEW

The LTC2977 is a PMBus programmable power system controller, monitor, sequencer and voltage supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage and output voltage/current readback through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the start-up of DC/DC converters via PMBus programming and their control input pins. Time-based sequencing and tracking sequencing are both supported.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Allow the user to trim or margin the DC/DC converter output voltage in a manual operating mode by providing direct access to the margin DAC.
- Supervise the DC/DC converter output voltage, input voltage, and the LTC2977 die temperature for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Respond to a fault condition by either continuing operation indefinitely, latching off after a programmable deglitch period, latching off immediately or sequencing off after TOFF_DELAY. A retry mode may be used to automatically recover from a latched-off condition. When enabled, the number of retries (0 to 6 or infinite) is the same for all pages and is programmed in MFR_RETRY_COUNT.
- Optionally stop trimming the DC/DC converter output voltage after reaching the initial margin or nominal target. Optionally allow servo to resume if target drifts outside of $V_{OUT}$ warning limits.
- Store command register contents to EEPROM with CRC and ECC through PMBus programming.
- Restore EEPROM contents through PMBus programming or when $V_{DD33}$ is applied on power-up.
- Report the DC/DC converter output voltage status through the PMBus interface and the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the FAULTBz0 and FAULTBz1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output voltage OV and UV faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the ON state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Record minimum and maximum observed values of input voltage, output voltages and temperature.
- Access user EEPROM data directly, without altering RAM space (MFR_EE_UNLOCK, MFR_EE_ERASE, and MFR_EE_DATA). Facilitates in-house bulk programming.

## OPERATION

### EEPROM

The LTC2977 contains internal EEPROM (nonvolatile memory) with error-correcting code (ECC) to store configuration settings and fault log information. EEPROM endurance, retention, and mass write operation time are specified over the operating junction temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

Nondestructive operation above $T_J$ = 105°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 105°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 105°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when $T_J > 85°C$.

The degradation in EEPROM retention for temperatures >105°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

where:

AF = acceleration factor

Ea = activation energy = 1.4 eV

$k = 8.617 \times 10^{-5}$ eV/°K

$T_{USE}$ = 105°C specified junction temperature

$T_{STRESS}$ = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 125°C for 10 hours.

$T_{STRESS}$ = 125°C

$T_{USE}$ = 105°C

AF = 8.65

Equivalent operating time at 105°C = 86.5 hours.

So the overall retention of the EEPROM was degraded by 76.5 hours as a result of operation at a junction temperature of 125°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 175,200 hours at a maximum junction temperature of 105°C.

### RESET

Holding the WDI/RESETB pin low for more than $t_{RESETB}$ will cause the LTC2977 to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the $I^2C$ bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2977 will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to $V_{DD33}$ with a 10k resistor. WDI/RESETB includes an internal 256µs deglitch filter so additional filter capacitance on this pin is not recommended.

### OTHER OPERATIONS

#### Clock Sharing

Multiple LTC PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARE_CLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all LTC2977s.

SHARE_CLK can optionally be used to synchronize ON/OFF dependency on $V_{IN}$ across multiple chips by setting the Mfr_config_all_vin_share_enable bit of the MFR_CONFIG_ALL_LTC2977 register. When configured this way the chip will hold SHARE_CLK low when the unit is off for insufficient input voltage and upon detecting that SHARE_CLK is held low the chip will disable all channels after a brief deglitch period. When the SHARE_CLK pin is allowed to rise, the chip will respond by beginning a soft-start sequence. In this case the slowest VIN_ON detection will take over and synchronize other chips to its soft-start sequence.

# OPERATION

## PMBus SERIAL DIGITAL INTERFACE

The LTC2977 communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2977 is a slave device. The master can communicate with the LTC2977 using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1-12 illustrate the aforementioned SMBus protocols. All transactions support PEC (packet error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

The LTC2977 will not acknowledge any PMBus command other than MFR_COMMON if it is still busy with a STORE_USER_ALL, RESTORE_USER_ALL, MFR_CONFIG_LTC2977 or if fault log data is being written to the EEPROM. Status_word_busy will be set when this happens.

## PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon $I^2C$ with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple $I^2C$ byte commands because they provide timeouts to prevent bus hangs and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for $I^2C$ communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: paragraph 5: Transport. This can be found at:

www.pmbus.org.

For a description of the differences between SMBus and $I^2C$, refer to system management bus (SMBus) specification version 2.0: Appendix B – Differences Between SMBus and $I^2C$. This can be found at:

www.smbus.org.

When using an $I^2C$ controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of the PMBus read command by concatenating a start command byte write with an $I^2C$ read.

## OPERATION

| | |
|---|---|
| S | START CONDITION |
| Sr | REPEATED START CONDITION |
| Rd | READ (BIT VALUE OF 1) |
| Wr | WRITE (BIT VALUE OF 0) |
| $\overline{A}$ | NOT ACKNOWLEDGE (HIGH) |
| A | ACKNOWLEDGE (LOW) |
| P | STOP CONDITION |
| PEC | PACKET ERROR CODE |
| ☐ | MASTER TO SLAVE |
| ▒ | SLAVE TO MASTER |
| ··· | CONTINUATION OF PROTOCOL |

2977 F01a

**Figure 1a. PMBus Packet Protocol Diagram Element Key**

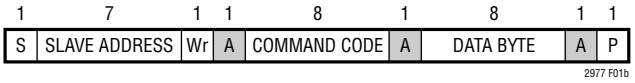



**Figure 1b. Write Byte Protocol**

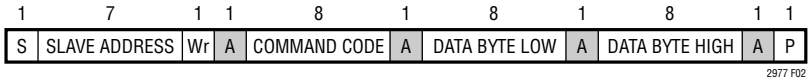



**Figure 2. Write Word Protocol**

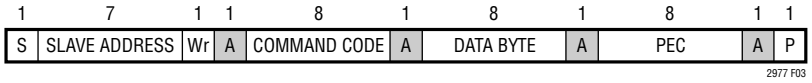



**Figure 3. Write Byte Protocol with PEC**

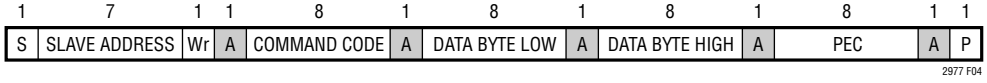



**Figure 4. Write Word Protocol with PEC**

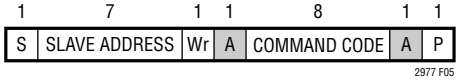



**Figure 5. Send Byte Protocol**

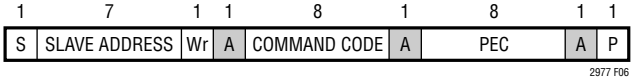



**Figure 6. Send Byte Protocol with PEC**

## OPERATION

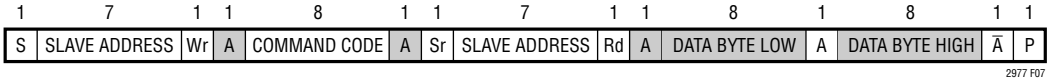



**Figure 7. Read Word Protocol**

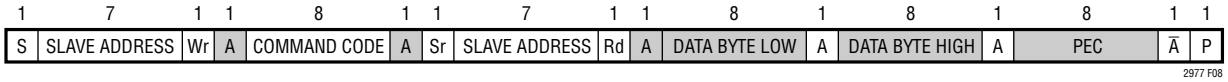



**Figure 8. Read Word Protocol with PEC**

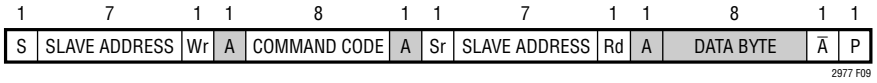



**Figure 9. Read Byte Protocol**

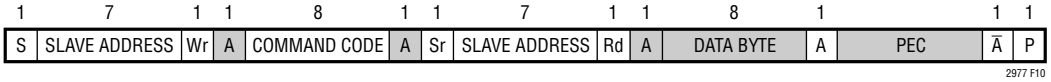



**Figure 10. Read Byte Protocol with PEC**

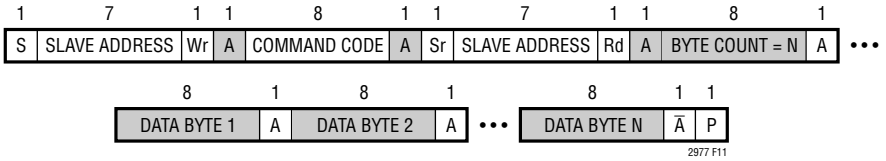



**Figure 11. Block Read**

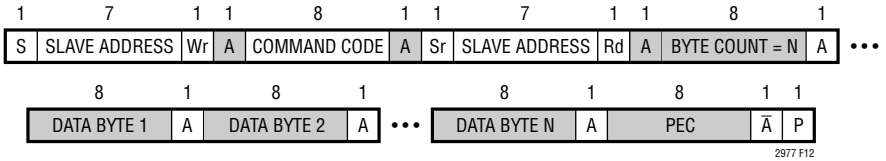



**Figure 12. Block Read with PEC**

## OPERATION

### Device Address

The I²C/SMBus address of the LTC2977 equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to $V_{DD33}$, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTC2977s can be connected together to control 72 outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I²C/SMBus device or global addresses, including I²C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2977 always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

**Table 1. LTC2977 Address Look-Up Table with MFR_I2C_BASE_ADDRESS Set to 7-Bit 0x5C**

| ADDRESS PINS | | DESCRIPTION | HEX DEVICE ADDRESS | | BINARY DEVICE ADDRESS BITS | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| ASEL1 | ASEL0 | | 7-Bit | 8-Bit | 6 | 5 | 4 | 3 | 2 | 1 | 0 | R/W |
| X | X | Alert Response | 0C | 19 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 |
| X | X | Global | 5B | B6 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| L | L | N = 0 | 5C* | B8 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| L | NC | N = 1 | 5D | BA | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| L | H | N = 2 | 5E | BC | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| NC | L | N = 3 | 5F | BE | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| NC | NC | N = 4 | 60 | C0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| NC | H | N = 5 | 61 | C2 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| H | L | N = 6 | 62 | C4 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| H | NC | N = 7 | 63 | C6 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| H | H | N = 8 | 64 | C8 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |

H = Tie to $V_{DD33}$, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7bit 0x5C (Factory Default)

# OPERATION

## Processing Commands

The LTC2977 uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables. MFR_COMMON is a special command that may always be read even when the part is busy. This provides an alternate method for a host to determine if the LTC2977 is busy.

**EEPROM Related Commands**

| COMMAND | TYPICAL DELAY* | COMMENT |
|---|---|---|
| STORE_USER_ALL | $t_{MASS\_WRITE}$ | See Electrical Characteristics table. The LTC2977 will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed. MFR_COMMON may always be read. |
| RESTORE_USER_ALL | 30ms | The LTC2977 will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed. MFR_COMMON may always be read. |
| MFR_FAULT_LOG_CLEAR | 175ms | The LTC2977 will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read. |
| MFR_FAULT_LOG_STORE | 20ms | The LTC2977 will not accept any commands while it is transferring the fault log RAM buffer to EEPROM space. The command byte will be NACKed. MFR_COMMON may always be read. |
| Internal Fault log | 20ms | An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed. MFR_COMMON may always be read. |
| MFR_FAULT_LOG_ RESTORE | 2ms | The LTC2977 will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed. MFR_COMMON may always be read. |

*The typical delay is measured from the command's stop to the next command's start.

| COMMAND | TYPICAL DELAY* | COMMENT |
|---|---|---|
| MFR_CONFIG_LTC2977 | <50µs | The LTC2977 will not accept any commands while it is completing this command. The command byte will be NACKed. MFR_COMMON may always be read. |

*The typical delay is measured from the command's stop to the next command's start.

**Other PMBus Timing Notes**

| COMMAND | COMMENT |
|---|---|
| CLEAR_FAULTS | The LTC2977 will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs. |

# PMBus COMMAND SUMMARY

### Summary Table

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | EEPROM | DEFAULT VALUE | REF PAGE |
|---|---|---|---|---|---|---|---|---|---|
| PAGE | 0x00 | Channel or page currently selected for any command that supports paging. | R/W Byte | N | Reg | | | 0x00 | 28 |
| OPERATION | 0x01 | Operating mode control. On/Off, Margin High and Margin Low. | R/W Byte | Y | Reg | | Y | 0x00 | 33 |
| ON_OFF_CONFIG | 0x02 | CONTROL pin & PMBus bus on/off command setting. | R/W Byte | Y | Reg | | Y | 0x1E | 34 |
| CLEAR_FAULTS | 0x03 | Clear any fault bits that have been set. | Send Byte | Y | | | | NA | 34 |
| WRITE_PROTECT | 0x10 | Level of protection provided by the device against accidental changes. | R/W Byte | N | Reg | | Y | 0x00 | 28 |
| STORE_USER_ALL | 0x15 | Store entire operating memory to EEPROM. | Send Byte | N | | | | NA | 35 |
| RESTORE_USER_ALL | 0x16 | Restore entire operating memory from EEPROM. | Send Byte | N | | | | NA | 35 |
| CAPABILITY | 0x19 | Summary of PMBus optional communication protocols supported by this device. | R Byte | N | Reg | | | 0xB0 | 35 |
| VOUT_MODE | 0x20 | Output voltage data format and mantissa exponent. ($2^{-13}$) | R Byte | Y | Reg | | | 0x13 | 35 |
| VOUT_COMMAND | 0x21 | Servo Target. Nominal DC/DC converter output voltage setpoint. | R/W Word | Y | L16 | V | Y | 1.0 0x2000 | 36 |
| VOUT_MAX | 0x24 | Upper limit on the output voltage the unit can command regardless of any other commands. | R/W Word | Y | L16 | V | Y | 4.0 0x8000 | 36 |
| VOUT_MARGIN_HIGH | 0x25 | Margin high DC/DC converter output voltage setting. | R/W Word | Y | L16 | V | Y | 1.05 0x219A | 36 |
| VOUT_MARGIN_LOW | 0x26 | Margin low DC/DC converter output voltage setting. | R/W Word | Y | L16 | V | Y | 0.95 0x1E66 | 36 |
| VIN_ON | 0x35 | Input voltage ($V_{IN\_SNS}$) above which power conversion can be enabled. | R/W Word | N | L11 | V | Y | 10.0 0xD280 | 36 |
| VIN_OFF | 0x36 | Input voltage ($V_{IN\_SNS}$) below which power conversion is disabled. All $V_{OUT\_EN}n$ pins go off immediately. | R/W Word | N | L11 | V | Y | 9.0 0xD240 | 36 |
| VOUT_OV_FAULT_LIMIT | 0x40 | Output overvoltage fault limit | R/W Word | Y | L16 | V | Y | 1.1 0x2333 | 36 |
| VOUT_OV_FAULT_RESPONSE | 0x41 | Action to be taken by the device when an output overvoltage fault is detected. | R/W Byte | Y | Reg | | Y | 0x80 | 38 |
| VOUT_OV_WARN_LIMIT | 0x42 | Output overvoltage warning limit . | R/W Word | Y | L16 | V | Y | 1.075 0x2266 | 36 |
| VOUT_UV_WARN_LIMIT | 0x43 | Output undervoltage warning limit | R/W Word | Y | L16 | V | Y | 0.925 0x1D9A | 36 |
| VOUT_UV_FAULT_LIMIT | 0x44 | Output undervoltage fault limit. Limit used to determine if TON_MAX_FAULT has been met and the unit is on. | R/W Word | Y | L16 | V | Y | 0.9 0x1CCD | 36 |
| VOUT_UV_FAULT_RESPONSE | 0x45 | Action to be taken by the device when an output undervoltage fault is detected. | R/W Byte | Y | Reg | | Y | 0x7F | 38 |
| OT_FAULT_LIMIT | 0x4F | Overtemperature fault limit. | R/W Word | N | L11 | °C | Y | 105.0 0xEB48 | 37 |
| OT_FAULT_RESPONSE | 0x50 | Action to be taken by the device when an overtemperature fault is detected. | R/W Byte | N | Reg | | Y | 0xB8 | 39 |

# PMBus COMMAND SUMMARY

### Summary Table

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | EEPROM | DEFAULT VALUE | REF PAGE |
|---|---|---|---|---|---|---|---|---|---|
| OT_WARN_LIMIT | 0x51 | Overtemperature warning limit. | R/W Word | N | L11 | °C | Y | 70.0 0xEA30 | 37 |
| UT_WARN_LIMIT | 0x52 | Undertemperature warning limit. | R/W Word | N | L11 | °C | Y | 0 0x8000 | 37 |
| UT_FAULT_LIMIT | 0x53 | Undertemperature fault limit. | R/W Word | N | L11 | °C | Y | –40.0 0xE580 | 37 |
| UT_FAULT_RESPONSE | 0x54 | Action to be taken by the device when an undertemperature fault is detected. | R/W Byte | N | Reg | | Y | 0xB8 | 39 |
| VIN_OV_FAULT_LIMIT | 0x55 | Input overvoltage fault limit measured at $V_{IN\_SNS}$ pin | R/W Word | N | L11 | V | Y | 15.0 0xD3C0 | 36 |
| VIN_OV_FAULT_ RESPONSE | 0x56 | Action to be taken by the device when an input overvoltage fault is detected. | R/W Byte | N | Reg | | Y | 0x80 | 39 |
| VIN_OV_WARN_LIMIT | 0x57 | Input overvoltage warning limit measured at $V_{IN\_SNS}$ pin | R/W Word | N | L11 | V | Y | 14.0 0xD380 | 36 |
| VIN_UV_WARN_LIMIT | 0x58 | Input undervoltage warning limit measured at $V_{IN\_SNS}$ pin. | R/W Word | N | L11 | V | Y | 0 0x8000 | 36 |
| VIN_UV_FAULT_LIMIT | 0x59 | Input undervoltage fault limit measured at $V_{IN\_SNS}$ pin | R/W Word | N | L11 | V | Y | 0 0x8000 | 36 |
| VIN_UV_FAULT_ RESPONSE | 0x5A | Action to be taken by the device when an input undervoltage fault is detected. | R/W Byte | N | Reg | | Y | 0x00 | 39 |
| POWER_GOOD_ON | 0x5E | Output voltage at or above which a power good should be asserted. | R/W Word | Y | L16 | V | Y | 0.96 0x1EB8 | 36 |
| POWER_GOOD_OFF | 0x5F | Output voltage at or below which a power good should be deasserted. | R/W Word | Y | L16 | V | Y | 0.94 0x1E14 | 36 |
| TON_DELAY | 0x60 | Time from CONTROL pin and/or OPERATION command = ON to $V_{OUT\_ENn}$ pin = ON. | R/W Word | Y | L11 | ms | Y | 1.0 0xBA00 | 37 |
| TON_RISE | 0x61 | Time from when the $V_{OUT\_ENn}$ pin goes high until the LTC2977 optionally soft-connects its DAC and begins to servo the output voltage to the desired value. | R/W Word | Y | L11 | ms | Y | 10.0 0xD280 | 37 |
| TON_MAX_FAULT_LIMIT | 0x62 | Maximum time from $V_{OUT\_ENn}$ = ON assertion that an UV condition will be tolerated before a TON_MAX_FAULT condition results. | R/W Word | Y | L11 | ms | Y | 15.0 0xD3C0 | 37 |
| TON_MAX_FAULT_ RESPONSE | 0x63 | Action to be taken by the device when a TON_MAX_FAULT event is detected. | R/W Byte | Y | Reg | | Y | 0xB8 | 40 |
| TOFF_DELAY | 0x64 | Time from CONTROL pin and/or OPERATION command = OFF to $V_{OUT\_ENn}$ pin = OFF. | R/W Word | Y | L11 | ms | Y | 1.0 0xBA00 | 37 |
| STATUS_BYTE | 0x78 | One byte summary of the unit's fault condition. | R Byte | Y | Reg | | | NA | 41 |
| STATUS_WORD | 0x79 | Two byte summary of the unit's fault condition. | R Word | Y | Reg | | | NA | 41 |
| STATUS_VOUT | 0x7A | Output voltage fault and warning status. | R Byte | Y | Reg | | | NA | 42 |
| STATUS_INPUT | 0x7C | Input voltage fault and warning status measured at VIN_SNS pin. | R Byte | N | Reg | | | NA | 42 |
| STATUS_TEMPERATURE | 0x7D | Temperature fault and warning status for READ_TEMPERATURE_1. | R Byte | N | Reg | | | NA | 42 |

# PMBus COMMAND SUMMARY

### Summary Table

| COMMAND NAME | CMD CODE | DESCRIPTION | TYPE | PAGED | DATA FORMAT | UNITS | EEPROM | DEFAULT VALUE | REF PAGE |
|---|---|---|---|---|---|---|---|---|---|
| STATUS_CML | 0x7E | Communication and memory fault and warning status. | R Byte | N | Reg | | | NA | 43 |
| STATUS_MFR_SPECIFIC | 0x80 | Manufacturer specific fault and state information. | R Byte | Y | Reg | | | NA | 43 |
| READ_VIN | 0x88 | Input voltage measured at VIN_SNS pin. | R Word | N | L11 | V | | NA | 44 |
| READ_VOUT | 0x8B | DC/DC converter output voltage. | R Word | Y | L16 | V | | NA | 44 |
| READ_TEMPERATURE_1 | 0x8D | Internal junction temperature. | R Word | N | L11 | °C | | NA | 44 |
| PMBUS_REVISION | 0x98 | PMBus revision supported by this device. Current revision is 1.1. | R Byte | N | Reg | | | 0x11 | 44 |
| USER_DATA_00 | 0xB0 | Manufacturer reserved for LTpowerPlay™. | R/W Word | N | Reg | | Y | NA | 60 |
| USER_DATA_01 | 0xB1 | Manufacturer reserved for LTpowerPlay. | R/W Word | Y | Reg | | Y | NA | 60 |
| USER_DATA_02 | 0xB2 | OEM reserved. | R/W Word | N | Reg | | Y | NA | 60 |
| USER_DATA_03 | 0xB3 | Scratchpad location. | R/W Word | Y | Reg | | Y | 0x00 | 60 |
| USER_DATA_04 | 0xB4 | Scratchpad location. | R/W Word | N | Reg | | Y | 0x00 | 60 |
| MFR_LTC_RESERVED_1 | 0xB5 | Manufacturer reserved. | R/W Word | Y | Reg | | Y | NA | 60 |
| MFR_INFO | 0xB6 | Manufacturer specific information. | R Word | N | Reg | | | NA | 58 |
| MFR_STATUS_2 | 0xB7 | Additional manufacturer specific fault and state information. | R Word | Y | Reg | | | NA | 61 |
| MFR_LTC_RESERVED_2 | 0xBC | Manufacturer reserved. | R/W Word | Y | Reg | | | NA | 60 |
| MFR_EE_UNLOCK | 0xBD | Unlock user EEPROM for access by MFR_EE_ERASE and MFR_EE_DATA commands. | R/W Byte | N | Reg | | | NA | 64 |
| MFR_EE_ERASE | 0xBE | Initialize user EEPROM for bulk programming by MFR_EE_DATA. | R/W Byte | N | Reg | | | NA | 64 |
| MFR_EE_DATA | 0xBF | Data transferred to and from EEPROM using sequential PMBus word reads or writes. Supports bulk programming. | R/W Word | N | Reg | | | NA | 64 |
| MFR_COMMAND_PLUS | 0xC0 | Alternate access to block read and other data: commands for all hosts. | R/W Word | N | Reg | | | NA | 30 |
| MFR_DATA_PLUS0 | 0xC1 | Alternate access to block read and other data: data for alternate host 0. | R/W Word | N | Reg | | | NA | 30 |
| MFR_DATA_PLUS1 | 0xC2 | Alternate access to block read an other data: data for alternate host 1. | R/W Word | N | Reg | | | NA | 30 |
| MFR_TELEMETRY | 0xCF | Telemetry data for all output channels. | R Block | N | Reg | | | NA | 62 |
| MFR_CONFIG_LTC2977 | 0xD0 | Configuration bits that are channel specific. | R/W Word | Y | Reg | | Y | 0x0080 | 45 |
| MFR_CONFIG_ALL_LTC2977 | 0xD1 | Configuration bits that are common to all pages. | R/W Word | N | Reg | | Y | 0x1C7B | 49 |
| MFR_FAULTBz0_PROPAGATE | 0xD2 | Configuration that determines if a channel's faulted off state is propagated to the FAULTB00 and FAULTB10 pins. | R/W Byte | Y | Reg | | Y | 0x00 | 50 |
| MFR_FAULTBz1_PROPAGATE | 0xD3 | Manufacturer configuration that Configuration that determines if a channel's faulted off state is propagated to the FAULTB01 and FAULTB11 pins. | R/W Byte | Y | Reg | | Y | 0x00 | 50 |
| MFR_PWRGD_EN | 0xD4 | Configuration for mapping PWRGD and WDI/RESETB status to the PWRGD pin. | R/W Word | N | Reg | | Y | 0x0000 | 51 |