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8-Channel PMBus Power System Manager Featuring Accurate Output Voltage Measurement

FEATURES

- **Sequence, Trim, Margin and Supervise Eight Power Supplies**
- **Manage Faults, Monitor Telemetry and Create Fault Logs**
- **PMBus Compliant Command Set**
- **Supported by LTpowerPlay™ GUI**
- **Margin or Trim Supplies to 0.25% Accuracy**
- **Fast OV/UV Supervisors per Channel**
- **Coordinate Sequencing and Fault Management Across Multiple Chips**
- **Automatic Fault Logging to Internal EEPROM**
- **Operate Autonomously without Additional Software**
- Internal Temperature and Input Voltage Supervisors
- Accurate Monitoring of Eight Output Voltages, Input Voltage and Internal Die Temperature
- I^2C/SMBus Serial Interface
- Can Be Powered from 3.3V, or 4.5V to 15V
- Programmable Watchdog Timer
- 100% Compatible with the LTC2978
- Available in 64-pin 9mm × 9mm QFN Package

APPLICATIONS

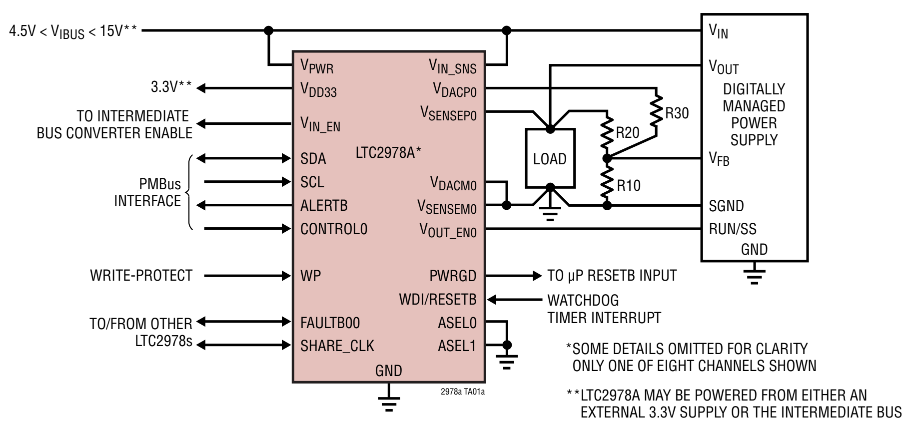
- Computers and Network Servers
- Industrial Test and Measurement
- High Reliability Systems
- Medical Imaging
- Video

DESCRIPTION

The LTC®2978A is an 8-channel Power System Manager used to sequence, trim (servo), margin, supervise, manage faults, provide telemetry and create fault logs. PMBus commands support power supply sequencing, precision point-of-load voltage adjustment and margining. DACs use a proprietary soft-connect algorithm to minimize supply disturbances. Supervisory functions include overvoltage and undervoltage threshold limits for eight power supply output channels and one power supply input channel, as well as over and under temperature limits. Programmable fault responses can disable the power supplies with optional retry after a fault is detected. Faults that disable a power supply can automatically trigger black box EEPROM storage of fault status and associated telemetry. An internal 16-bit ADC monitors eight output voltages, one input voltage, and die temperature. In addition, odd numbered channels can be configured to measure the voltage across a current sense resistor. A programmable watchdog timer monitors microprocessor activity for a stalled condition and resets the microprocessor if necessary. A single wire bus synchronizes power supplies across multiple LTC power system management devices. Configuration EEPROM supports autonomous operation without additional software.

TYPICAL APPLICATION

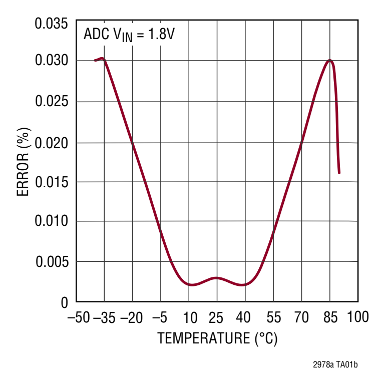
8-Channel PMBus Power System Manager



*SOME DETAILS OMITTED FOR CLARITY ONLY ONE OF EIGHT CHANNELS SHOWN

**LTC2978A MAY BE POWERED FROM EITHER AN EXTERNAL 3.3V SUPPLY OR THE INTERMEDIATE BUS

Typical ADC Total Unadjusted Error vs Temperature



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ABSOLUTE MAXIMUM RATINGS

(Notes 1, 2)

Supply Voltages:
- V_{PWR} to GND .... –0.3V to 15V
- V_{DD33} to GND .... –0.3V to 3.6V
- V_{DD25} to GND .... –0.3V to 2.75V

Digital Input/Output Voltages:
- ALERTB, SDA, SCL, CONTROL0, CONTROL1... –0.3V to 5.5V
- PWRGD, SHARE_CLK, WDI/RESETB, WP....................–0.3V to V_{DD33} + 0.3V
- FAULTB00, FAULTB01, FAULTB10, FAULTB11 ....–0.3V to V_{DD33} + 0.3V
- ASEL0, ASEL1..........................–0.3V to V_{DD33} + 0.3V

Analog Voltages:
- REFP... –0.3V to 1.35V
- REFM to GND....................................... –0.3V to 0.3V
- V_{IN_SNS} to GND..................................... –0.3V to 15V
- $V_{SENSEP[7:0]}$ to GND .... –0.3V to 6V
- $V_{SENSEM[7:0]}$ to GND .... –0.3V to 6V
- $V_{OUT\_EN[3:0]}$, V_{IN_EN} to GND .... –0.3V to 15V
- $V_{OUT\_EN[7:4]}$ to GND .... –0.3V to 6V
- $V_{DACP[7:0]}$ to GND .... –0.3V to 6V
- $V_{DACM[7:0]}$ to GND .... –0.3V to 0.3V

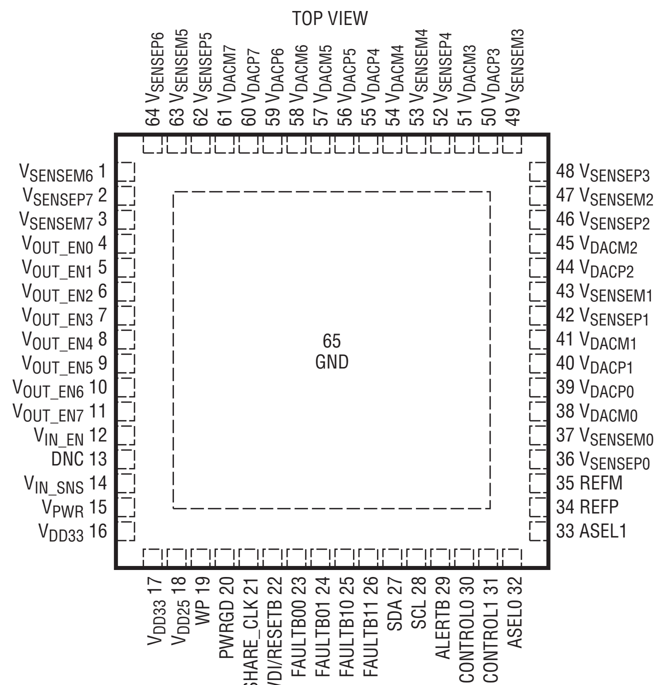
Operating Junction Temperature Range:
- LTC2978AC... 0°C to 70°C
- LTC2978AI..–40°C to 85°C

Storage Temperature Range ....–65°C to 125°C

Maximum Junction Temperature .... 125°C*

*See OPERATION section for detailed EEPROM derating information for junction temperatures in excess of 85°C.

PIN CONFIGURATION



UP PACKAGE
64-LEAD (9mm × 9mm) PLASTIC QFN

T_{JMAX} = 125°C, $\theta_{JA\text{-}TOP}$ = 28°C/W, $\theta_{JC\text{-}BOTTOM}$ = 1°C/W
EXPOSED PAD (PIN 65) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	JUNCTION TEMPERATURE RANGE
LTC2978ACUP#PBF	LTC2978ACUP#TRPBF	LTC2978AUP	64-Lead (9mm × 9mm) Plastic QFN	0°C to 70°C
LTC2978AIUP#PBF	LTC2978AIUP#TRPBF	LTC2978AUP	64-Lead (9mm × 9mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container. Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V, V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Power-Supply Characteristics							
V_{PWR}	V_{PWR} Supply Input Operating Range		●	4.5		15	V
I_{PWR}	V_{PWR} Supply Current	4.5V ≤ V_{PWR} ≤ 15V, V_{DD33} Floating	●		10	13	mA
I_{VDD33}	V_{DD33} Supply Current	3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}	●		10	13	mA
V_{UVLO_VDD33}	V_{DD33} Undervoltage Lockout	V_{DD33} Ramping Up, V_{PWR} = V_{DD33}	●	2.35	2.55	2.8	V
	V_{DD33} Undervoltage Lockout Hysteresis				120		mV
V_{DD33}	Supply Input Operating Range	V_{PWR} = V_{DD33}	●	3.13		3.47	V
	Regulator Output Voltage	4.5V ≤ V_{PWR} ≤ 15V	●	3.13	3.26	3.47	V
	Regulator Output Short-Circuit Current	V_{PWR} = 4.5V, V_{DD33} = 0V	●	75	90	140	mA
V_{DD25}	Regulator Output Voltage	3.13V ≤ V_{DD33} ≤ 3.47V	●	2.35	2.5	2.6	V
	Regulator Output Short-Circuit Current	V_{PWR} = V_{DD33} = 3.47V, V_{DD25} = 0V	●	30	55	80	mA
t_{INIT}	Initialization Time	Time from V_{IN} Applied Until the TON_DELAY Timer Starts			135		ms
Voltage Reference Characteristics							
V_{REF}	Output Voltage	V_{REF} = V_{REFP} – V_{REFM}, 0 < I_{REFP} < 100μA			1.232		V
	Temperature Coefficient				3		ppm/°C
	Hysteresis	(Note 3)			100		ppm
ADC Characteristics							
V_{IN_ADC}	Voltage Sense Input Range	Differential Voltage: V_{IN_ADC} = ($V_{SENSEPn}$ – $V_{SENSEMn}$)	●	0		6	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
	Current Sense Input Range (Odd Numbered Channels Only)	Single-Ended Voltage: $V_{SENSEPn}$, $V_{SENSEMn}$	●	–0.1		6	V
		Differential Voltage: V_{IN_ADC}	●	–170		170	mV
N_ADC	Voltage Sense Resolution (Uses L16 Format)	0V ≤ V_{IN_ADC} ≤ 6V			122		μV/LSB
	Current Sense Resolution (Odd Numbered Channels Only)	0mV ≤ |V_{IN_ADC}| < 16mV (Note11) 16mV ≤ |V_{IN_ADC}| < 32mV 32mV ≤ |V_{IN_ADC}| < 63.9mV 63.9mV ≤ |V_{IN_ADC}| < 127.9mV 127.9mV ≤ |V_{IN_ADC}|			15.625 31.25 62.5 125 250		μV/LSB μV/LSB μV/LSB μV/LSB μV/LSB
TUE_ADC_ VOLT_SNS	Total Unadjusted Error	Voltage Sense Mode V_{IN_ADC} ≥ 1V	●			±0.25	% of Reading
		Voltage Sense Mode 0 ≤ V_{IN_ADC} ≥ 1V	●			±2.5	mV
TUE_ADC_ CURR_SNS	Total Unadjusted Error	Current Sense Mode, Odd Numbered Channels Only, 20mV ≤ V_{IN_ADC} ≤ 170mV	●			±0.7	% of Reading
		Current Sense Mode, Odd Numbered Channels Only, V_{IN_ADC} ≤ 20mV	●			140	μV
V_{OS_ADC}	Offset Error	Current Sense Mode, Odd Numbered Channels Only	●			±35	μV
t_{CONV_ADC}	Conversion Time	Voltage Sense Mode (Note 4)			6.15		ms
		Current Sense Mode (Note 4)			24.6		ms
		Temperature Input (Note 4)			24.6		ms
t_{UPDATE_ADC}	Maximum Update Time	Odd Numbered Channels in Current Sense Mode (Note 4)			160		ms

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V; V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN_ADC}	Input Sampling Capacitance				1		pF
f_{IN_ADC}	Input Sampling Frequency				62.5		kHz
I_{IN_ADC}	Input Leakage Current	V_{IN_ADC} = 0V, 0V ≤ $V_{COMMONMODE}$ ≤ 6V, Current Sense Mode	●			±0.5	µA
	Differential Input Current	V_{IN_ADC} = 0.17V, Current Sense Mode	●		80	250	nA
		V_{IN_ADC} = 6V, Voltage Sense Mode	●		10	15	µA
DAC Output Characteristics							
N_V_{DACP}	Resolution				10		Bits
V_{FS_VDACP}	Full-Scale Output Voltage (Programmable)	DAC Code = 0x3FF, DAC Polarity = 1; Buffer Gain Setting_0	●	1.32	1.38	1.44	V
		DAC Code = 0x3FF, DAC Polarity = 1; Buffer Gain Setting_1	●	2.53	2.65	2.77	V
INL_V_{DACP}	Integral Nonlinearity	(Note 5)	●			±2	LSB
DNL_V_{DACP}	Differential Nonlinearity	(Note 5)	●			±2.4	LSB
V_{OS_VDACP}	Offset Voltage	(Note 5)	●			±10	mV
V_{DACP}	Load Regulation (V_{DACPn} – V_{DACMn})	V_{DACPn} = 2.65V, I_{VDACPn} Sourcing = 2mA			100		ppm/mA
		V_{DACPn} = 0.1V, I_{VDACPn} Sinking = 2mA			100		ppm/mA
	PSRR (V_{DACPn} – V_{DACMn})	DC: 3.13V ≤ V_{DD33} ≤ 3.47V, V_{PWR} = V_{DD33}			60		dB
		100mV Step in 20ns with 50pF Load			40		dB
	DC CMRR (V_{DACPn} – V_{DACMn})	–0.1V ≤ V_{DACMn} ≤ 0.1V			60		dB
	Leakage Current	V_{DACPn} Hi-Z, 0V ≤ V_{DACPn} ≤ 6V	●			±100	nA
	Short-Circuit Current Low	V_{DACPn} Shorted to GND	●	–10		–4	mA
	Short-Circuit Current High	V_{DACPn} Shorted to V_{DD33}	●	4		10	mA
C_{OUT}	Output Capacitance	V_{DACPn} Hi-Z			10		pF
t_{S_VDACP}	DAC Output Update Rate	Fast Servo Mode			250		µs
Voltage Supervisor Characteristics							
V_{IN_VS}	Input Voltage Range (Programmable)	V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$); Low Resolution Mode	●	0		6	V
		V_{IN_VS} = ($V_{SENSEPn}$ – $V_{SENSEMn}$); High Resolution Mode	●	0		3.8	V
		Single-Ended Voltage: $V_{SENSEMn}$	●	–0.1		0.1	V
N_VS	Voltage Sensing Resolution	0V to 3.8V Range: High Resolution Mode			4		mV/LSB
		0V to 6V Range: Low Resolution Mode			8		mV/LSB
TUE_VS	Total Unadjusted Error	2V ≤ V_{IN_VS} ≤ 6V, Low Resolution Mode	●			±1.25	%
		1.5V < V_{IN_VS} ≤ 3.8V, High Resolution Mode	●			±1.0	%
		0.8V ≤ V_{IN_VS} ≤ 1.5V, High Resolution Mode	●			±1.5	%
t_{S_VS}	Update Rate				12.21		µs
V_{IN_SNS} Input Characteristics							
V_{VIN_SNS}	V_{IN_SNS} Input Voltage Range		●	0		15	V
R_{VIN_SNS}	V_{IN_SNS} Input Resistance		●	70	90	110	kΩ
TUE_{VIN_SNS}	VIN_ON, VIN_OFF Threshold Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V	●			±2.0	%
		V_{VIN_SNS} > 8V	●			±1.0	%
	READ_VIN Total Unadjusted Error	3V ≤ V_{VIN_SNS} ≤ 8V	●			±1.5	%
		V_{VIN_SNS} > 8V	●			±1.0	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V; V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Soft-Connect Comparator Characteristics							
V_{OS_CMP}	Offset Voltage	V_{DACPn} = 0.2V	●		±1	±18	mV
		V_{DACPn} = 1.3V	●		±2	±26	mV
		V_{DACPn} = 2.65V	●		±3	±52	mV
Temperature Sensor Characteristics							
TUE_TS	Total Unadjusted Error				±1		°C
V_{OUT} Enable Output (V_{OUT_EN} [3:0]) Characteristics							
V_{VOUT_ENn}	Output High Voltage (Note 10)	I_{VOUT_ENn} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VOUT_ENn}	Output Sourcing Current	V_{VOUT_ENn} Pull-Up Enabled, V_{VOUT_ENn} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	Strong Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	3	5	8	mA
		Weak Pull-Down Enabled, V_{VOUT_ENn} = 0.4V	●	33	50	60	µA
	Output Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VOUT_ENn} ≤ 15V	●			±1	µA
V_{OUT} Enable Output (V_{OUT_EN} [7:4]) Characteristics							
I_{VOUT_ENn}	Output Sinking Current	Strong Pull-Down Enabled, V_{OUT_ENn} = 0.1V	●	3	6	9	mA
	Output Leakage Current	0V ≤ V_{VOUT_ENn} ≤ 6V	●			±1	µA
V_{IN} Enable Output (V_{IN_EN}) Characteristics							
V_{VIN_EN}	Output High Voltage	I_{VIN_EN} = –5µA, V_{DD33} = 3.3V	●	10	12.5	14.7	V
I_{VIN_EN}	Output Sourcing Current	V_{IN_EN} Pull-Up Enabled, V_{VIN_EN} = 1V	●	–5	–6	–8	µA
	Output Sinking Current	V_{VIN_EN} = 0.4V	●	3	5	8	mA
	Leakage Current	Internal Pull-Up Disabled, 0V ≤ V_{VIN_EN} ≤ 15V	●			±1	µA
EEPROM Characteristics							
Endurance	(Notes 6, 9)	0°C < T_J < 85°C During EEPROM Write Operations	●	10,000			Cycles
Retention	(Notes 6, 9)	T_J < 85°C	●	10			Years
t_{MASS_WRITE}	Mass Write Operation Time (Note 7)	STORE_USER_ALL, 0°C < T_J < 85°C During EEPROM Write Operations	●		440	4100	ms
Digital Inputs SCL, SDA, CONTROL0, CONTROL1, WDI/RESETB, FAULTB00, FAULTB01, FAULTB10, FAULTB11, WP							
V_{IH}	High Level Input Voltage		●	2.1			V
V_{IL}	Low Level Input Voltage		●			1.5	V
V_{HYST}	Input Hysteresis				20		mV
I_{LEAK}	Input Leakage Current	0V ≤ V_{PIN} ≤ 5.5V, SDA, SCL, CONTROL*n* Pins Only	●			±2	µA
		0V ≤ V_{PIN} ≤ V_{DD33} + 0.3V, FAULTB*zn*, WDI/RESETB, WP Pins Only	●			±2	µA
t_{SP}	Pulse Width of Spike Suppressed	FAULTB*zn*, CONTROL*n* Pins Only			10		µs
		SDA, SCL Pins Only			98		ns
t_{FAULT_MIN}	Minimum Low Pulse Width for Externally Generated Faults			110			ms
t_{RESETB}	Pulse Width to Assert Reset	$V_{WDI/RESETB}$ ≤ 1.5V	●	300			µs
t_{WDI}	Pulse Width to Reset Watchdog Timer	$V_{WDI/RESETB}$ ≤ 1.5V	●	0.3		200	µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_J = 25°C. V_{PWR} = V_{IN_SNS} = 12V; V_{DD33}, V_{DD25}, REFP and REFM pins floating, unless otherwise indicated. C_{VDD33} = 100nF, C_{VDD25} = 100nF and C_{REF} = 100nF.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
f_{WDI}	Watchdog Interrupt Input Frequency		●			1	MHz
C_{IN}	Digital Input Capacitance				10		pF
Digital Input SHARE_CLK							
V_{IH}	High Level Input Voltage		●	1.6			V
V_{IL}	Low Level Input Voltage		●			0.8	V
$f_{SHARE\_CLK\_IN}$	Input Frequency Operating Range		●	90		110	kHz
t_{LOW}	Assertion Low Time	V_{SHARE_CLK} < 0.8V	●	0.825		1.1	µs
t_{RISE}	Rise Time	V_{SHARE_CLK} < 0.8V to V_{SHARE_CLK} > 1.6V	●			450	ns
I_{LEAK}	Input Leakage Current	0V ≤ V_{SHARE_CLK} ≤ V_{DD33} + 0.3V	●			±1	µA
C_{IN}	Input Capacitance				10		pF
Digital Outputs SDA, ALERTB, PWRGD, SHARE_CLK, FAULTB00, FAULTB01, FAULTB10, FAULTB11							
V_{OL}	Digital Output Low Voltage	I_{SINK} = 3mA	●			0.4	V
$f_{SHARE\_CLK\_OUT}$	Output Frequency Operating Range	5.49kΩ Pull-Up to V_{DD33}	●	90	100	110	kHz
Digital Inputs ASEL0,ASEL1							
V_{IH}	Input High Threshold Voltage		●	V_{DD33} – 0.5			V
V_{IL}	Input Low Threshold Voltage		●			0.5	V
$I_{IH,IL}$	High, Low Input Current	ASEL[1:0] = 0, V_{DD33}	●			±95	µA
$I_{IH,\ Z}$	Hi-Z Input Current		●			±24	µA
C_{IN}	Input Capacitance				10		pF
Serial Bus Timing Characteristics							
f_{SCL}	Serial Clock Frequency (Note 8)		●	10		400	kHz
t_{LOW}	Serial Clock Low Period (Note 8)		●	1.3			µs
t_{HIGH}	Serial Clock High Period (Note 8)		●	0.6			µs
t_{BUF}	Bus Free Time Between Stop and Start (Note 8)		●	1.3			µs
$t_{HD,STA}$	Start Condition Hold Time (Note 8)		●	600			ns
$t_{SU,STA}$	Start Condition Setup Time (Note 8)		●	600			ns
$t_{SU,STO}$	Stop Condition Setup Time (Note 8)		●	600			ns
$t_{HD,DAT}$	Data Hold Time (LTC2978A Receiving Data) (Note 8)		●	0			ns
	Data Hold Time (LTC2978A Transmitting Data) (Note 8)		●	300		900	ns
$t_{SU,DAT}$	Data Setup Time (Note 8)		●	100			ns
t_{SP}	Pulse Width of Spike Suppressed (Note 8)				98		ns
$t_{TIMEOUT\_BUS}$	Time Allowed to Complete any PMBus Command after Which Time SDA Will Be Released and Command Terminated	Longer Timeout = 0 Longer Timeout = 1	● ●		25 200	35 280	ms ms
Additional Digital Timing Characteristics							
t_{OFF_MIN}	Minimum Off-Time for Any Channel				100		ms

ELECTRICAL CHARACTERISTICS

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive. All currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified. If power is supplied to the chip via the V_{DD33} pin only, connect V_{PWR} and V_{DD33} pins together.

Note 3: Hysteresis in the output voltage is created by package stress that differs depending on whether the IC was previously at a higher or lower temperature. Output voltage is always measured at 25°C, but the IC is cycled to 85°C or –40°C before successive measurements. Hysteresis is roughly proportional to the square of the temperature change.

Note 4: The time between successive ADC conversions (latency of the ADC) for any given channel is given as: 36.9ms + (6.15ms • number of ADC channels configured in Low Resolution mode) + (24.6ms • number of ADC channels configured in High Resolution mode).

Note 5: Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to full-scale code, 1023.

Note 6: EEPROM endurance and retention are guaranteed by design, characterization and correlation with statistical process controls. The minimum retention specification applies for devices whose EEPROM has been cycled less than the minimum endurance specification.

Note 7: The LTC2978A will not acknowledge any PMBus commands while a mass write operation is being executed. This includes the STORE_USER_ALL and MFR_FAULT_LOG_STORE commands or a fault log store initiated by a channel faulting off.

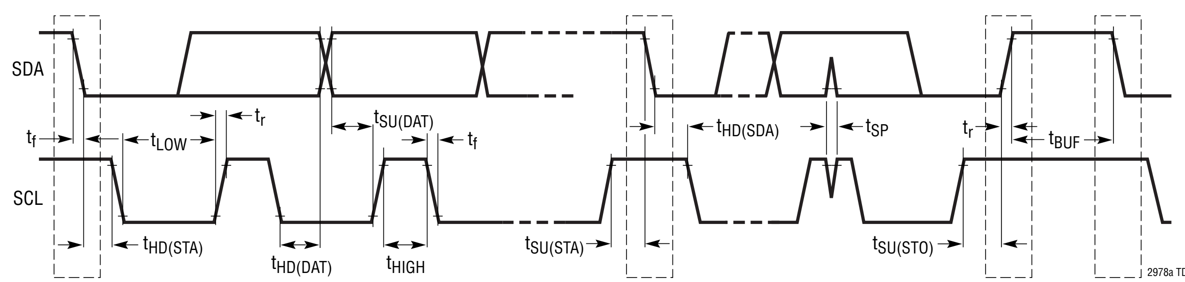
Note 8: Maximum capacitive load, C_B, for SCL and SDA is 400pF. Data and clock rise time (t_r) and fall time (t_f) are: $(20 + 0.1 \cdot C_B)$ (ns) $< t_r <$ 300ns and $(20 + 0.1 \cdot C_B)$ (ns) $< t_f <$ 300ns. C_B = capacitance of one bus line in pF. SCL and SDA external pull-up voltage, V_{IO}, is $3.13V < V_{IO} < 5.5V$.

Note 9: EEPROM endurance and retention will be degraded when $T_J > 85°C$.

Note 10: Output enable pins are charge-pumped from V_{DD33}.

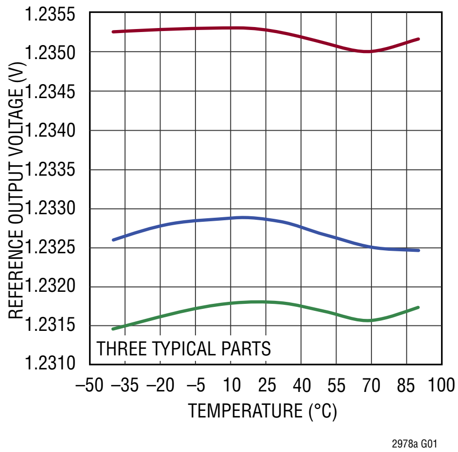
Note 11: The current sense resolution is determined by the L11 format and the mV units of the returned value. For example a full scale value of 170mV returns an L11 value of 0xF2A8 = $680 \cdot 2^{-2}$ = 170. This is the lowest range that can represent this value without overflowing the L11 mantissa and the resolution for 1LSB in this range is 2^{-2} mV = 250µV. Each successively lower range improves resolution by cutting the LSB size in half.

PMBUS TIMING DIAGRAM

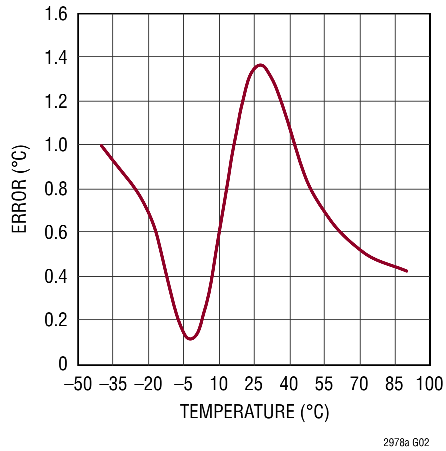


TYPICAL PERFORMANCE CHARACTERISTICS

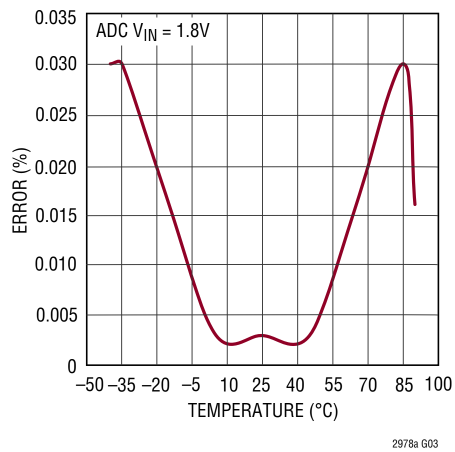
Reference Voltage vs Temperature



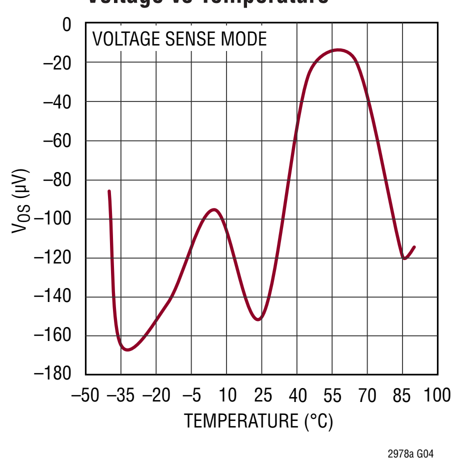
Temperature Sensor Error vs Temperature



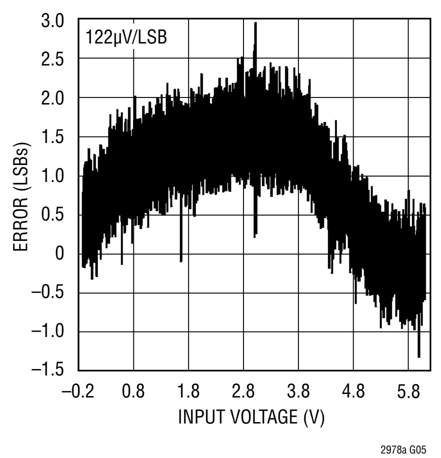
ADC Total Unadjusted Error vs Temperature



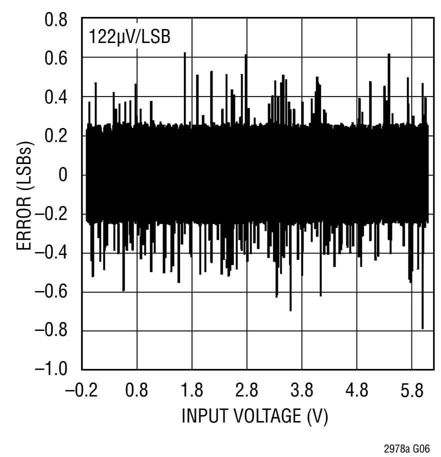
ADC Zero Code Center Offset Voltage vs Temperature



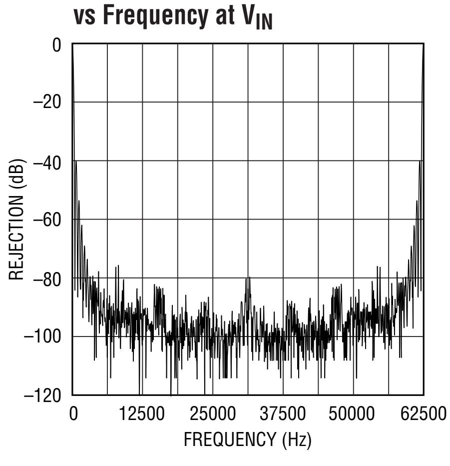
ADC-INL



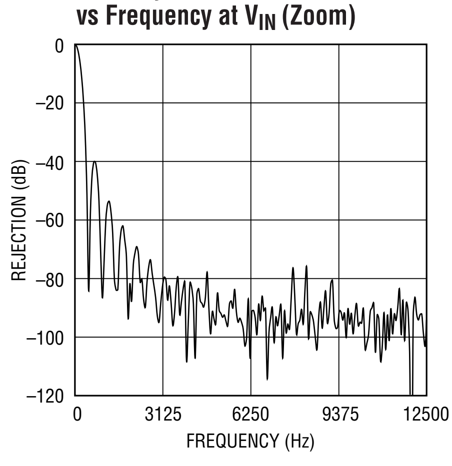
ADC-DNL



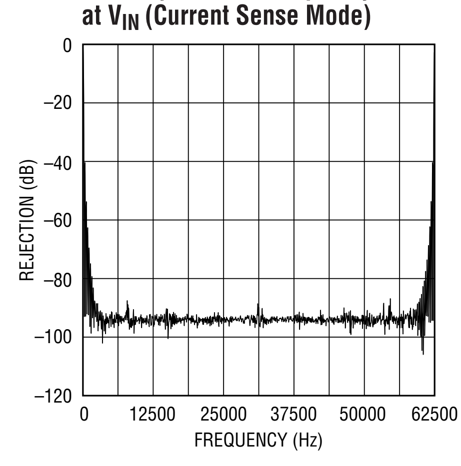
ADC Rejection vs Frequency at V_{IN}



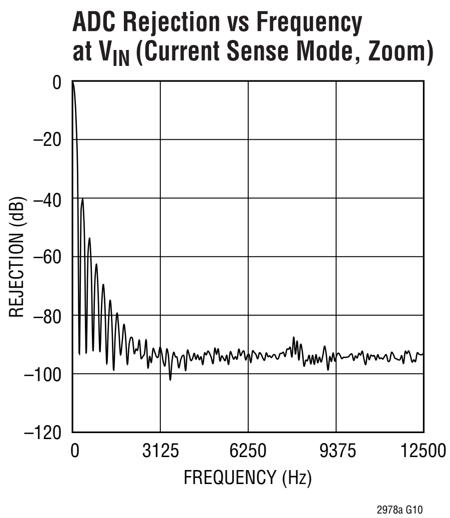
ADC Rejection vs Frequency at V_{IN} (Zoom)

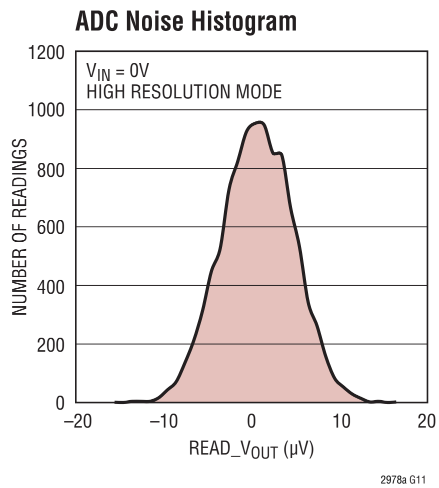


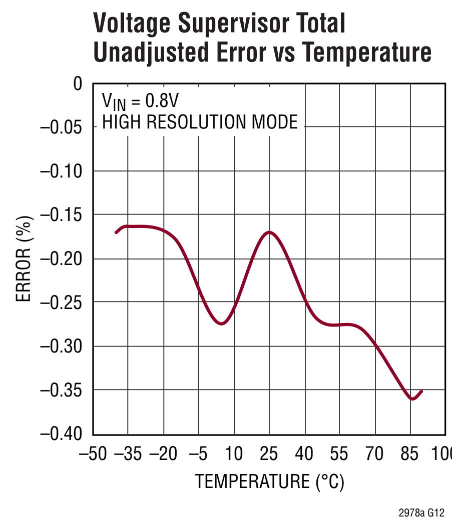
ADC Rejection vs Frequency at V_{IN} (Current Sense Mode)

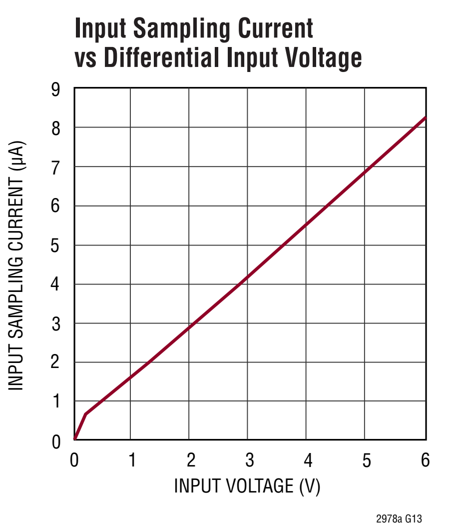


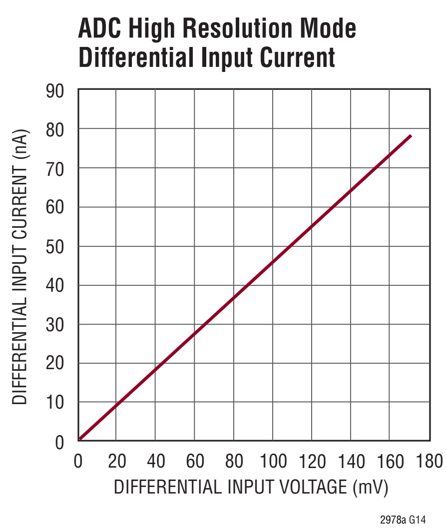
TYPICAL PERFORMANCE CHARACTERISTICS

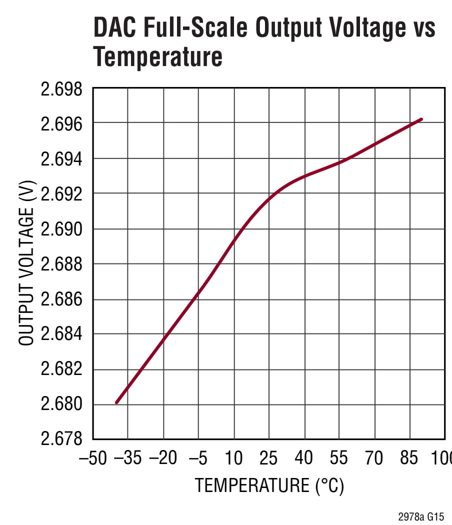


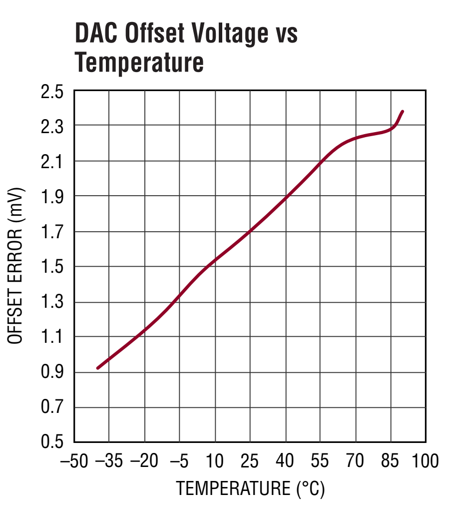


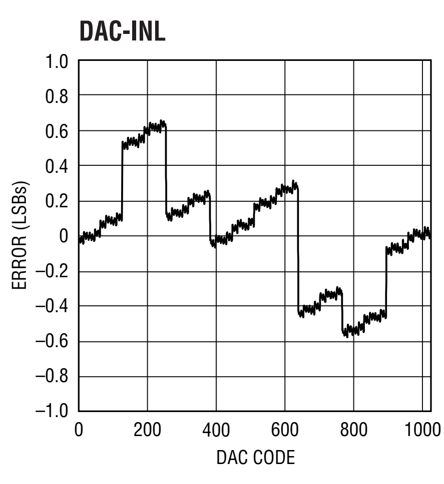


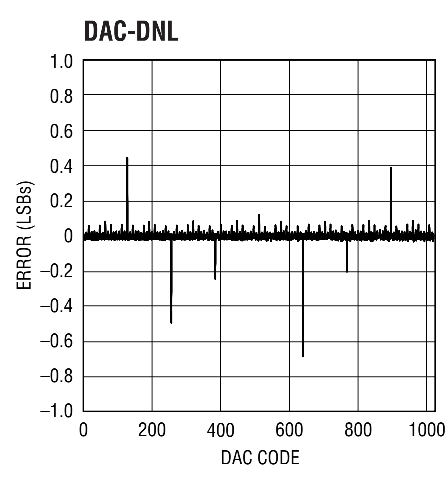




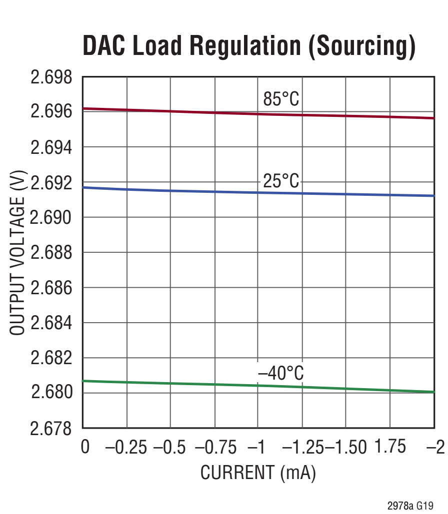


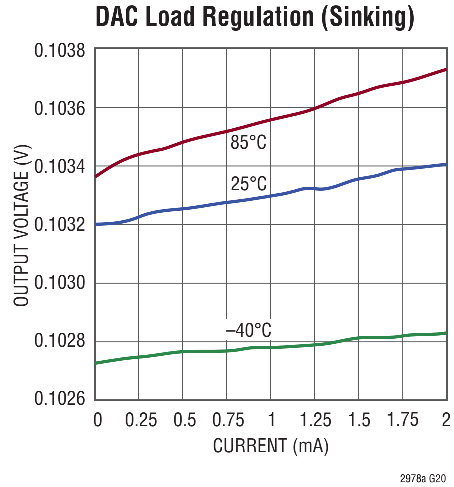


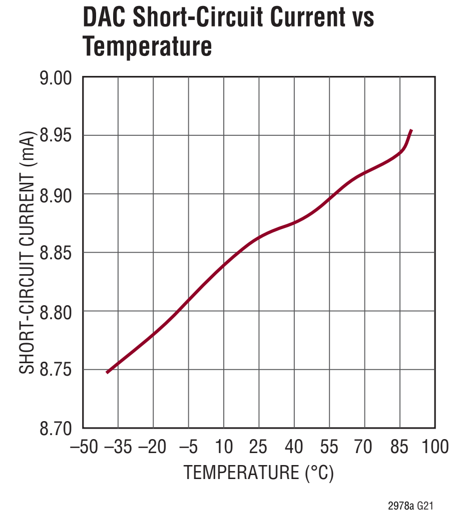


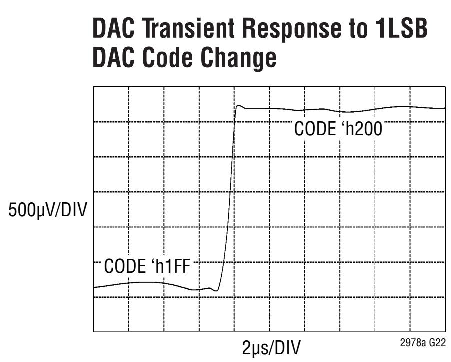


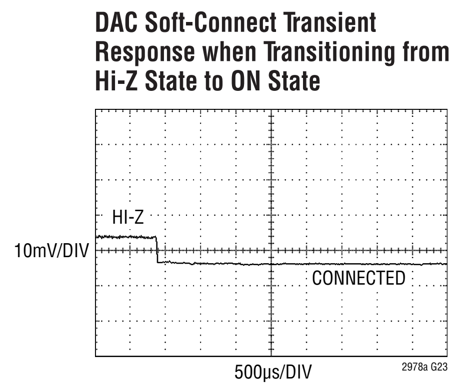
TYPICAL PERFORMANCE CHARACTERISTICS



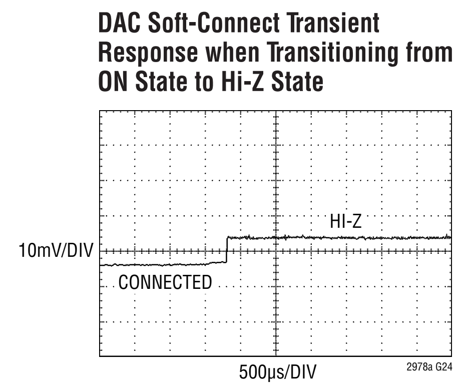








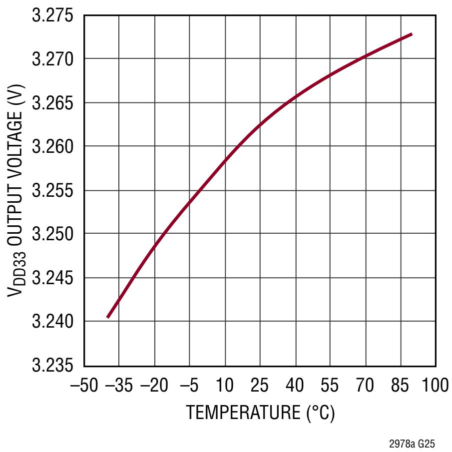
100k SERIES RESISTANCE ON
CODE: ‘h1FF



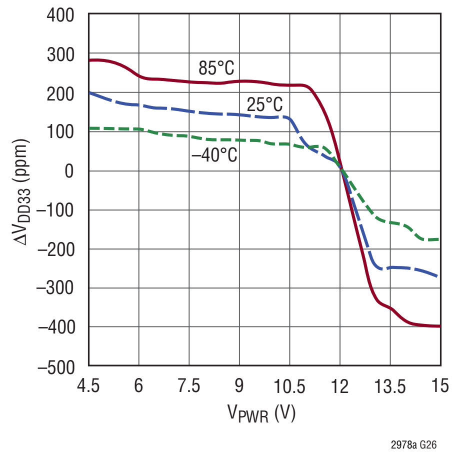
100k SERIES RESISTANCE ON
CODE: ‘h1FF

TYPICAL PERFORMANCE CHARACTERISTICS

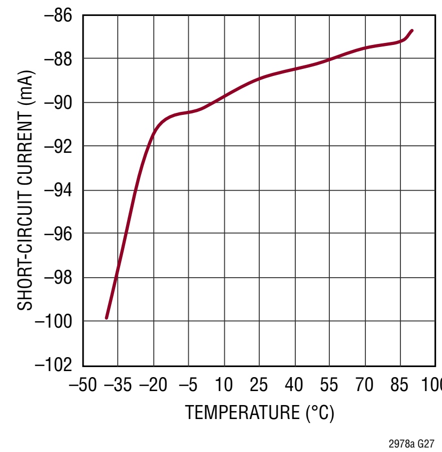
V_{DD33} Regulator Output Voltage vs Temperature



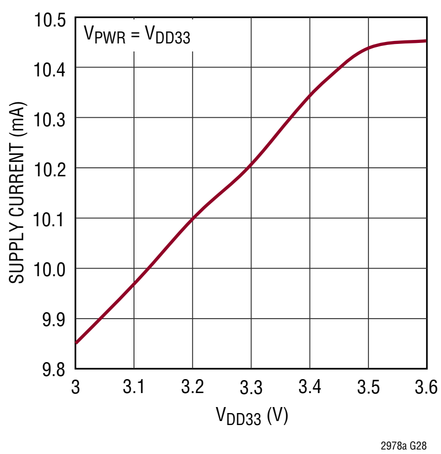
V_{DD33} Regulator Line Regulation



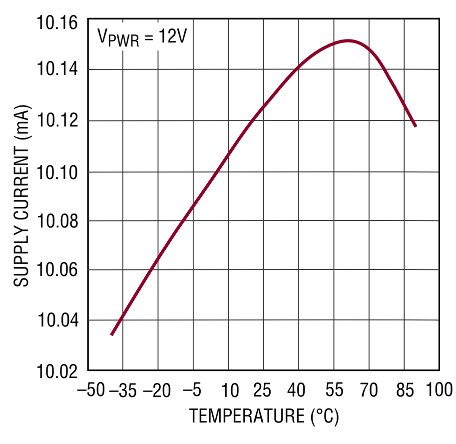
V_{DD33} Regulator Short-Circuit Current vs Temperature



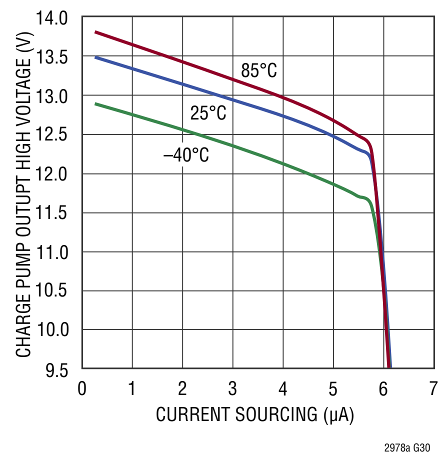
Supply Current vs Supply Voltage



Supply Current vs Temperature

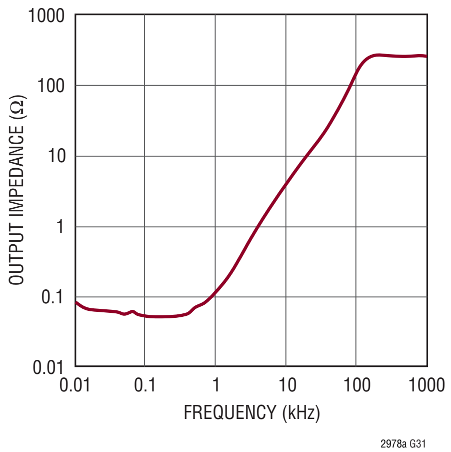


$V_{OUT\_EN[3:0]}$ and V_{IN_EN} Output High Voltage vs Load Current

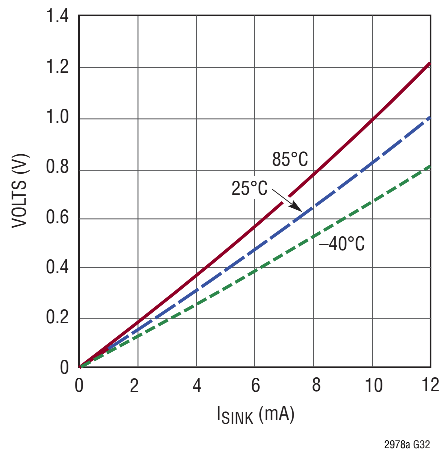


TYPICAL PERFORMANCE CHARACTERISTICS

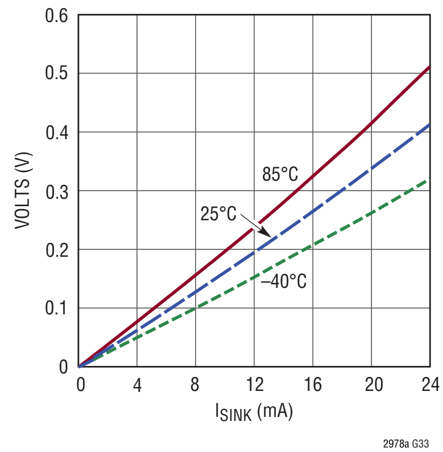
DAC Output Impedance vs Frequency



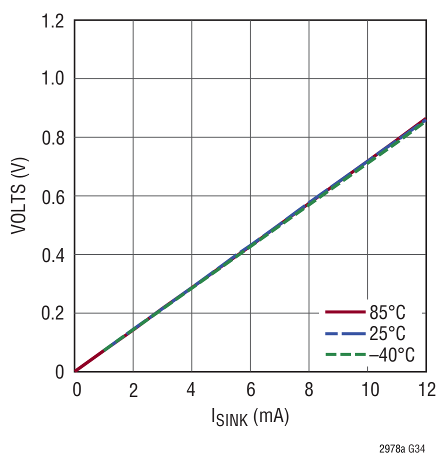
$V_{OUT\_EN[3:0]}$ and V_{IN_EN} V_{OL} vs Current



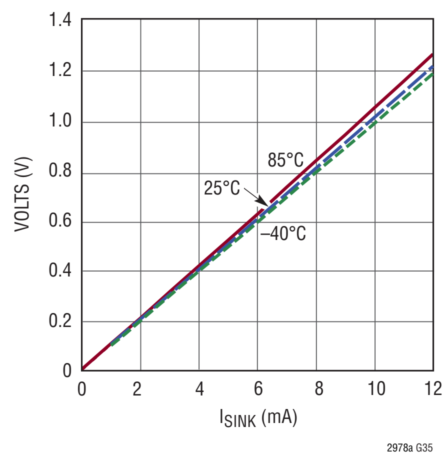
$V_{OUT\_EN[7:4]}$ V_{OL} vs Current



PWRGD and FAULTBz*n* V_{OL} vs Current



ALERTB V_{OL} vs Current



PIN FUNCTIONS

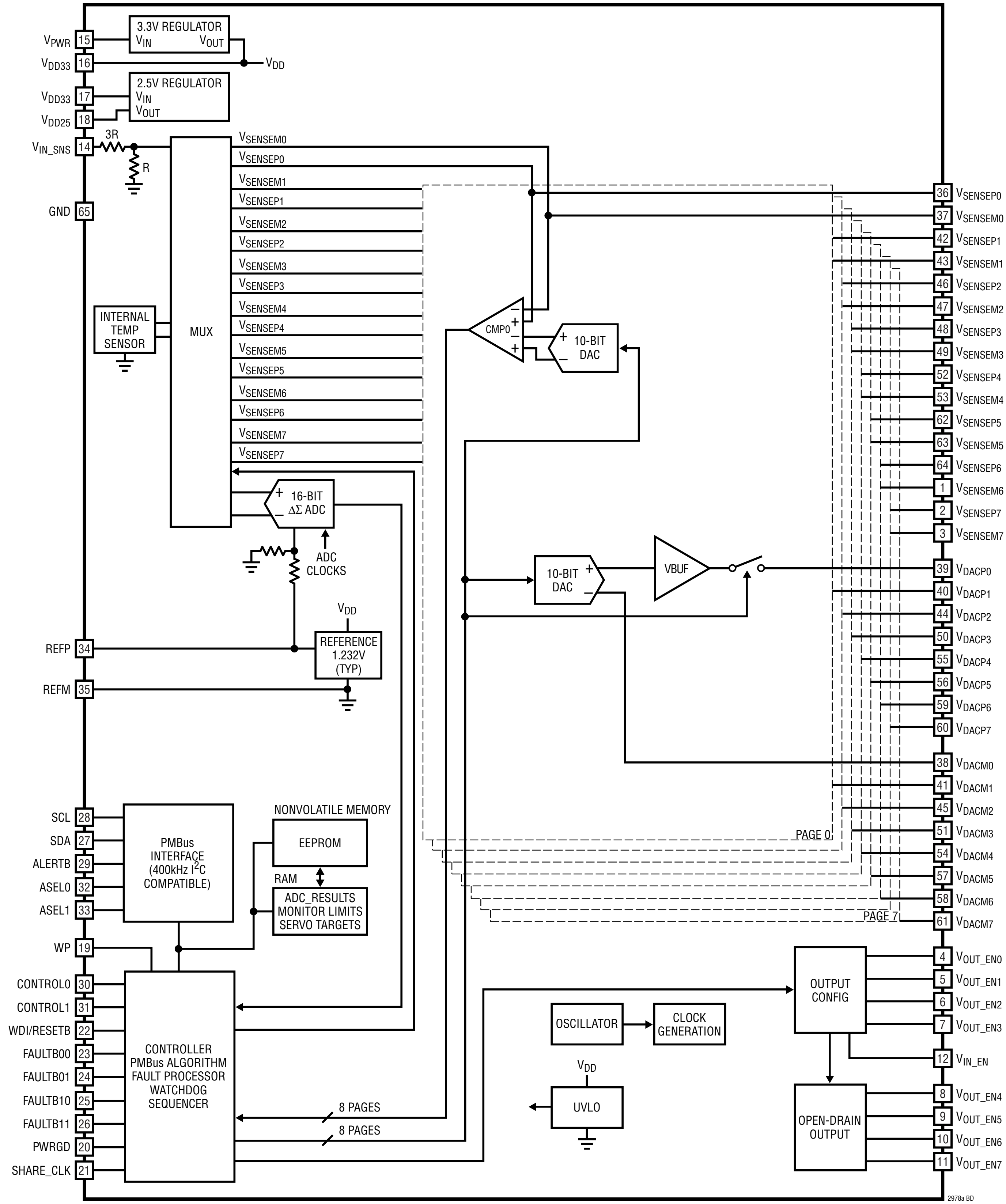
PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
$V_{SENSEM6}$	1*	In	DC/DC Converter Differential (–) Output Voltage-6 Sensing Pin
$V_{SENSEP7}$	2*	In	DC/DC Converter Differential (+) Output Voltage or Current-7 Sensing Pin
$V_{SENSEM7}$	3*	In	DC/DC Converter Differential (–) Output Voltage or Current-7 Sensing Pin
V_{OUT_EN0}	4	Out	DC/DC Converter Enable-0 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V_{OUT_EN1}	5	Out	DC/DC Converter Enable-1 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V_{OUT_EN2}	6	Out	DC/DC Converter Enable-2 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V_{OUT_EN3}	7	Out	DC/DC Converter Enable-3 Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
V_{OUT_EN4}	8	Out	DC/DC Converter Open-Drain Pull-Down Output-4
V_{OUT_EN5}	9	Out	DC/DC Converter Open-Drain Pull-Down Output-5
V_{OUT_EN6}	10	Out	DC/DC Converter Open-Drain Pull-Down Output-6
V_{OUT_EN7}	11	Out	DC/DC Converter Open-Drain Pull-Down Output-7
V_{IN_EN}	12	Out	DC/DC Converter V_{IN} ENABLE Pin. Output High Voltage Optionally Pulled Up to 12V by 5μA
DNC	13	Do Not Connect	Do Not Connect to This Pin
V_{IN_SNS}	14	In	V_{IN} SENSE Input. This Voltage is Compared Against the V_{IN} On and Off Voltage Thresholds in Order to Determine When to Enable and Disable, Respectively, the Downstream DC/DC Converters
V_{PWR}	15	In	V_{PWR} Serves as the Unregulated Power Supply Input to the Chip (4.5V to 15V). If a 4.5V to 15V Supply Voltage is Unavailable, Short V_{PWR} to V_{DD33} and Power the Chip Directly from a 3.3V Supply. Bypass to GND with 0.1µF Capacitor.
V_{DD33}	16	In/Out	If Shorted to V_{PWR}, it Serves as 3.13V to 3.47V Supply Input Pin. Otherwise it is a 3.3V Internally Regulated Voltage Output (Use 0.1µF Decoupling Capacitor to GND)
V_{DD33}	17	In	Input for Internal 2.5V Sub-Regulator. Short This Pin to Pin 16
V_{DD25}	18	In/Out	2.5V Internally Regulated Voltage Output. Bypass to GND with a 0.1µF Capacitor
WP	19	In	Digital Input. Write-Protect Input Pin, Active High
PWRGD	20	Out	Power Good Open-Drain Output. Indicates When Outputs are Power Good. Can be Used as System Power-On Reset. The Latency of This Signal May Be as Long as the ADC Latency. See Note 4.
SHARE_CLK	21	In/Out	Bidirectional Clock Sharing Pin. Connect a 5.49k Pull-Up Resistor to V_{DD33}
WDI/RESETB	22	In	Watchdog Timer Interrupt and Chip Reset Input. Connect a 10k Pull-Up Resistor to V_{DD33}. Rising Edge Resets Watchdog Counter. Holding This Pin Low for More Than t_{RESETB} Resets the Chip
FAULTB00	23	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-00. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB01	24	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-01. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB10	25	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-10. Connect a 10k Pull-Up Resistor to V_{DD33}
FAULTB11	26	In/Out	Open-Drain Output and Digital Input. Active Low Bidirectional Fault Indicator-11. Connect a 10k Pull-Up Resistor to V_{DD33}
SDA	27	In/Out	PMBus Bidirectional Serial Data Pin
SCL	28	In	PMBus Serial Clock Input Pin (400kHz Maximum)
ALERTB	29	Out	Open-Drain Output. Generates an Interrupt Request in a Fault/Warning Situation
CONTROL0	30	In	Control Pin 0 Input
CONTROL1	31	In	Control Pin 1 Input
ASEL0	32	In	Ternary Address Select Pin 0 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
ASEL1	33	In	Ternary Address Select Pin 1 Input. Connect to V_{DD33}, GND or Float to Encode 1 of 3 Logic States
REFP	34	Out	Reference Voltage Output. Needs 0.1µF Decoupling Capacitor to REFM
REFM	35	Out	Reference Return Pin. Needs 0.1µF Decoupling Capacitor to REFP.
$V_{SENSEP0}$	36*	In	DC/DC Converter Differential (+) Output Voltage-0 Sensing Pin
$V_{SENSEM0}$	37*	In	DC/DC Converter Differential (–) Output Voltage-0 Sensing Pin
V_{DACM0}	38*	Out	DAC0 Return. Connect to Channel 0 DC/DC Converter's GND Sense or Return to GND
V_{DACP0}	39	Out	DAC0 Output
V_{DACP1}	40	Out	DAC1 Output

PIN FUNCTIONS

PIN NAME	PIN NUMBER	PIN TYPE	DESCRIPTION
V_{DACM1}	41*	Out	DAC1 Return. Connect to Channel 1 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP1}$	42*	In	DC/DC Converter Differential (+) Output Voltage or Current-1 Sensing Pins
$V_{SENSEM1}$	43*	In	DC/DC Converter Differential (–) Output Voltage or Current-1 Sensing Pins
V_{DACP2}	44	Out	DAC2 Output
V_{DACM2}	45*	Out	DAC2 Return. Connect to Channel 2 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP2}$	46*	In	DC/DC Converter Differential (+) Output Voltage-2 Sensing Pin
$V_{SENSEM2}$	47*	In	DC/DC Converter Differential (–) Output Voltage-2 Sensing Pin
$V_{SENSEP3}$	48*	In	DC/DC Converter Differential (+) Output Voltage or Current-3 Sensing Pins
$V_{SENSEM3}$	49*	In	DC/DC Converter Differential (–) Output Voltage or Current-3 Sensing Pins
V_{DACP3}	50	Out	DAC3 Output
V_{DACM3}	51*	Out	DAC3 Return. Connect to Channel 3 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP4}$	52*	In	DC/DC Converter Differential (+) Output Voltage-4 Sensing Pin
$V_{SENSEM4}$	53*	In	DC/DC Converter Differential (–) Output Voltage-4 Sensing Pin
V_{DACM4}	54*	Out	DAC4 Return. Connect to Channel 4 DC/DC Converter's GND Sense or Return to GND
V_{DACP4}	55	Out	DAC4 Output
V_{DACP5}	56	Out	DAC5 Output
V_{DACM5}	57*	Out	DAC5 Return. Connect to Channel 5 DC/DC Converter's GND Sense or Return to GND
V_{DACM6}	58*	Out	DAC6 Return. Connect to Channel 6 DC/DC Converter's GND Sense or Return to GND
V_{DACP6}	59	Out	DAC6 Output
V_{DACP7}	60	Out	DAC7 Output
V_{DACM7}	61*	Out	DAC7 Return. Connect to Channel 7 DC/DC Converter's GND Sense or Return to GND
$V_{SENSEP5}$	62*	In	DC/DC Converter Differential (+) Output Voltage or Current-5 Sensing Pins
$V_{SENSEM5}$	63*	In	DC/DC Converter Differential (–) Output Voltage or Current-5 Sensing Pins
$V_{SENSEP6}$	64*	In	DC/DC Converter Differential (+) Output Voltage-6 Sensing Pin
GND	65	Ground	Exposed Pad, Must be Soldered to PCB

*Any unused $V_{SENSEPn}$ or $V_{SENSEMn}$ or V_{DACMn} pins must be tied to GND.

BLOCK DIAGRAM



OPERATION

OPERATION OVERVIEW

The LTC2978A is a PMBus programmable power system controller, monitor, sequencer and voltage supervisor that can perform the following operations:

- Accept PMBus compatible programming commands.
- Provide DC/DC converter input voltage and output voltage/current read back through the PMBus interface.
- Control the output of DC/DC converters that set the output voltage with a trim pin or DC/DC converters that set the output voltage using an external resistor feedback network.
- Sequence the start-up of DC/DC converters via PMBus programming and their control input pins.
- Trim the DC/DC converter output voltage (typically in 0.02% steps), in closed-loop servo operating mode, through PMBus programming.
- Margin the DC/DC converter output voltage to PMBus programmed limits.
- Allow the user to trim or margin the DC/DC converter output voltage in a manual operating mode by providing direct access to the margin DAC.
- Supervise the DC/DC converter output voltage, input voltage, and the LTC2978A die temperature for overvalue/undervalue conditions with respect to PMBus programmed limits and generate appropriate faults and warnings.
- Respond to a fault condition by either continuing operation indefinitely, latching off after a programmable deglitch period or latching off immediately. A retry mode may be used to automatically recover from a latched-off condition.
- Optionally stop trimming the DC/DC converter output voltage after it reached the initial margin or nominal target. Optionally allow servo to resume if target drifts outside of V_{OUT} warning limits.
- Store command register contents with CRC to EEPROM through PMBus programming.
- Restore EEPROM contents through PMBus programming or when V_{DD33} is applied on power-up.
- Report the DC/DC converter output voltage status through the PMBus interface and the power good output.
- Generate interrupt requests by asserting the ALERTB pin in response to supported PMBus faults and warnings.
- Coordinate system wide fault responses for all DC/DC converters connected to the FAULTBz0 and FAULTBz1 pins.
- Synchronize sequencing delays or shutdown for multiple devices using the SHARE_CLK pin.
- Software and hardware write protect the command registers.
- Disable the input voltage to the supervised DC/DC converters in response to output voltage OV and UV faults.
- Log telemetry and status data to EEPROM in response to a faulted-off condition
- Supervise an external microcontroller's activity for a stalled condition with a programmable watchdog timer and reset it if necessary.
- Prevent a DC/DC converter from re-entering the ON state after a power cycle until a programmable interval (MFR_RESTART_DELAY) has elapsed and its output has decayed below a programmable threshold voltage (MFR_VOUT_DISCHARGE_THRESHOLD).
- Record minimum and maximum observed values of input voltage, output voltages and temperature.

EEPROM

The LTC2978A contains internal EEPROM (nonvolatile memory) to store configuration settings and fault log information. EEPROM endurance, retention, and mass write operation time are specified over the operating junction temperature range. See Electrical Characteristics and Absolute Maximum Ratings sections.

OPERATION

Nondestructive operation above T_J = 85°C is possible although the Electrical Characteristics are not guaranteed and the EEPROM will be degraded.

Operating the EEPROM above 85°C may result in a degradation of retention characteristics. The fault logging function, which is useful in debugging system problems that may occur at high temperatures, only writes to fault log EEPROM locations. If occasional writes to these registers occur above 85°C, a slight degradation in the data retention characteristics of the fault log may occur.

It is recommended that the EEPROM not be written using STORE_USER_ALL or bulk programming when T_J > 85°C.

The degradation in EEPROM retention for temperatures >85°C can be approximated by calculating the dimensionless acceleration factor using the following equation.

$$AF = e^{\left[\left(\frac{Ea}{k}\right)\bullet\left(\frac{1}{T_{USE}+273}-\frac{1}{T_{STRESS}+273}\right)\right]}$$

Where:

AF = acceleration factor

Ea = activation energy = 1.4 eV

$k = 8.625 \times 10^{-5}$ eV/°K

T_{USE} = 85°C specified junction temperature

T_{STRESS} = actual junction temperature °C

Example: Calculate the effect on retention when operating at a junction temperature of 95°C for 10 hours.

T_{STRESS} = 95°C

T_{USE} = 85°C

AF = 3.4

Equivalent operating time at 85°C = 34 hours.

So the overall retention of the EEPROM was degraded by 34 hours as a result of operation at a junction temperature of 95°C for 10 hours. Note that the effect of this overstress is negligible when compared to the overall EEPROM retention rating of 87,600 hours at a maximum junction temperature of 85°C.

RESET

Holding the WDI/RESETB pin low for more than t_{RESETB} will cause the LTC2978A to enter the power-on reset state. While in the power-on reset state, the device will not communicate on the I^2C bus. Following the subsequent rising-edge of the WDI/RESETB pin, the LTC2978A will execute its power-on sequence per the user configuration stored in EEPROM. Connect WDI/RESETB to VDD33 with a 10k resistor. WDI/RESETB includes an internal 256μs deglitch filter so additional filter capacitance on this pin is not recommended.

WRITE-PROTECT PIN

The WP pin allows the user to write-protect the LTC2978A's configuration registers. The WP pin is active high, and when asserted it provides Level 2 protection: all writes are disabled except to the WRITE_PROTECT, PAGE, STORE_USER_ALL, OPERATION, MFR_PAGE_FF_MASK and CLEAR_FAULTS commands. The most restrictive setting between the WP pin and WRITE_PROTECT command will override. For example if WP = 1 and WRITE_PROTECT = 0x80, then the WRITE_PROTECT command overrides, since it is the most restrictive.

OTHER OPERATIONS

Clock Sharing

Multiple LTC PMBus devices can synchronize their clocks in an application by connecting together the open-drain SHARE_CLK input/outputs to a pull-up resistor as a wired OR. In this case the fastest clock will take over and synchronize all LTC2978As.

SHARE_CLK can optionally be used to synchronize ON/OFF dependency on V_{IN} across multiple chips by setting the Mfr_config_all_vin_share_enable bit of the MFR_CONFIG_ALL_LTC2978 register. When configured this way the chip will hold SHARE_CLK low when the unit is off for insufficient input voltage, and upon detecting that SHARE_CLK is held low the chip will disable all channels after a brief deglitch period. When the SHARE_CLK pin is allowed to rise, the

OPERATION

chip will respond by beginning a soft-start sequence. In this case the slowest VIN_ON detection will take over and synchronize other chips to its soft-start sequence.

PMBus SERIAL DIGITAL INTERFACE

The LTC2978A communicates with a host (master) using the standard PMBus serial bus interface. The PMBus Timing Diagram shows the timing relationship of the signals on the bus. The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2978A is a slave device. The master can communicate with the LTC2978A using the following formats:

- Master transmitter, slave receiver
- Master receiver, slave transmitter

The following SMBus protocols are supported:

- Write Byte, Write Word, Send Byte
- Read Byte, Read Word, Block Read
- Alert Response Address

Figures 1-12 illustrate the aforementioned SMBus protocols. All transactions support PEC (parity error check) and GCP (group command protocol). The Block Read supports 255 bytes of returned data. For this reason, the PMBus timeout may be extended using the Mfr_config_all_longer_pmbus_timeout setting.

The LTC2978A will not acknowledge any PMBus command if it is still busy with a STORE_USER_ALL, RESTORE_USER_ALL, MFR_CONFIG_LTC2978 or if fault log data is being written to the EEPROM. Status_word_busy will also be set, but ALERTB will not be asserted low.

PMBus

PMBus is an industry standard that defines a means of communication with power conversion devices. It is comprised of an industry standard SMBus serial interface and the PMBus command language.

The PMBus two wire interface is an incremental extension of the SMBus. SMBus is built upon I^2C with some minor differences in timing, DC parameters and protocol. The SMBus protocols are more robust than simple I^2C byte commands because they provide timeouts to prevent bus hangs and optional packet error checking (PEC) to ensure data integrity. In general, a master device that can be configured for I^2C communication can be used for PMBus communication with little or no change to hardware or firmware.

For a description of the minor extensions and exceptions PMBus makes to SMBus, refer to PMBus Specification Part 1 Revision 1.1: paragraph 5: Transport. This can be found at:

www.pmbus.org.

For a description of the differences between SMBus and I^2C, refer to system management bus (SMBus) specification version 2.0: Appendix B – Differences Between SMBus and I^2C. This can be found at:

www.smbus.org.

When using an I^2C controller to communicate with a PMBus part it is important that the controller be able to write a byte of data without generating a stop. This will allow the controller to properly form the repeated start of the PMBus read command by concatenating a start command byte write with an I^2C read.

OPERATION

1	7	1	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	P
			x		x	

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
x	SHOWN UNDER A FIELD INDICATES THAT THE FIELD IS REQUIRED TO HAVE THE VALUE OF x
A	ACKNOWLEDGE (THIS BIT POSITION MAY BE 0 FOR AN ACK OR 1 FOR A NACK)
P	STOP CONDITION
PEC	PACKET ERROR CODE
☐ (white)	MASTER TO SLAVE
■ (shaded)	SLAVE TO MASTER
...	CONTINUATION OF PROTOCOL

2978a F01a

Figure 1a. PMBus Packet Protocol Diagram Element Key

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE	A	P

2978a F01b

Figure 1b. Write Byte Protocol

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

2978a F02

Figure 2. Write Word Protocol

1	7	1	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE	A	PEC	A	P

2978a F03

Figure 3. Write Byte Protocol with PEC

1	7	1	1	8	1	8	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC	A	P

2978a F04

Figure 4. Write Word Protocol with PEC

1	7	1	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	P

2978a F05

Figure 5. Send Byte Protocol

1	7	1	1	8	1	8	1	1
S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	PEC	A	P

2978a F06

Figure 6. Send Byte Protocol with PEC

OPERATION

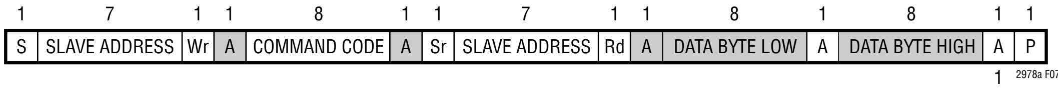


Figure 7. Read Word Protocol

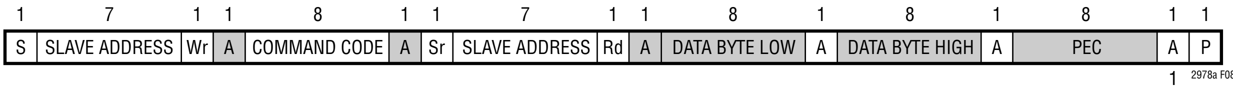


Figure 8. Read Word Protocol with PEC

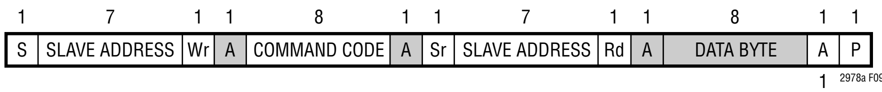


Figure 9. Read Byte Protocol

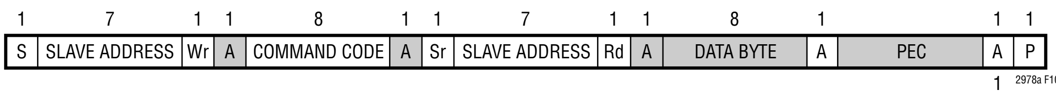


Figure 10. Read Byte Protocol with PEC

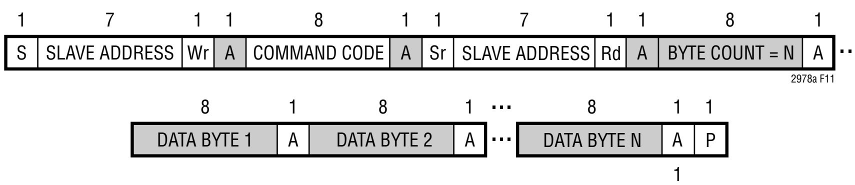


Figure 11. Block Read

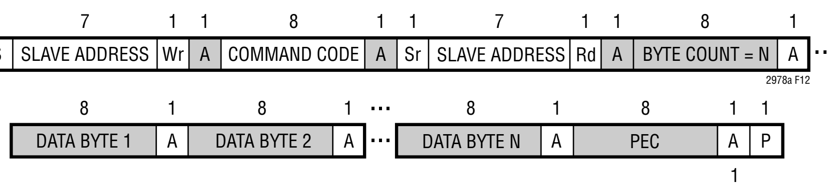


Figure 12. Block Read with PEC

OPERATION

Device Address

The I²C/SMBus address of the LTC2978A equals the base address + N where N is a number from 0 to 8. N can be configured by setting the ASEL0 and ASEL1 pins to V_{DD33}, GND or FLOAT. See Table 1. Using one base address and the nine values of N, nine LTC2978As can be connected together to control 72 outputs. The base address is stored in the MFR_I2C_BASE_ADDRESS register. The base address can be written to any value, but generally should not be changed unless the desired range of addresses overlap existing addresses. Watch that the address range does not overlap with other I²C/SMBus device or global addresses, including I²C/SMBus multiplexers and bus buffers. This will bring you great happiness.

The LTC2978A always responds to its global address and the SMBus Alert Response address regardless of the state of its ASEL pins and the MFR_I2C_BASE_ADDRESS register.

Table 1. LTC2978A Device Address Look-Up Table

ADDRESS DESCRIPTION	HEX DEVICE ADDRESS		BINARY DEVICE ADDRESS BITS								ADDRESS PINS	
	7-Bit	8-Bit	6	5	4	3	2	1	0	R/W	ASEL1	ASEL0
Alert Response	0C	19	0	0	0	1	1	0	0	1	X	X
Global	5B	B6	1	0	1	1	0	1	1	0	X	X
N = 0	5C*	B8	1	0	1	1	1	0	0	0	L	L
N = 1	5D	BA	1	0	1	1	1	0	1	0	L	NC
N = 2	5E	BC	1	0	1	1	1	1	0	0	L	H
N = 3	5F	BE	1	0	1	1	1	1	1	0	NC	L
N = 4	60	C0	1	1	0	0	0	0	0	0	NC	NC
N = 5	61	C2	1	1	0	0	0	0	1	0	NC	H
N = 6	62	C4	1	1	0	0	0	1	0	0	H	L
N = 7	63	C6	1	1	0	0	0	1	1	0	H	NC
N = 8	64	C8	1	1	0	0	1	0	0	0	H	H

H = Tie to V_{DD33}, NC = No Connect = Open or Float, L = Tie to GND, X = Don't Care
*MFR_I2C_BASE_ADDRESS = 7bit 5C (Factory Default)

OPERATION

Processing Commands

The LTC2978A uses a dedicated processing block to ensure quick response to all of its commands. There are a few exceptions where the part will NACK a subsequent command because it is still processing the previous command. These are summarized in the following tables.

EEPROM Related Commands

COMMAND	TYPICAL DELAY*	COMMENT
STORE_USER_ALL	t_{MASS_WRITE}	See Electrical Characteristics table. The LTC2978A will not accept any commands while it is transferring register contents to the EEPROM. The command byte will be NACKed.
RESTORE_USER_ALL	30ms	The LTC2978A will not accept any commands while it is transferring EEPROM data to command registers. The command byte will be NACKed.
MFR_FAULT_LOG_CLEAR	175ms	The LTC2978A will not accept any commands while it is initializing the fault log EEPROM space. The command byte will be NACKed.
MFR_FAULT_LOG_STORE	20ms	The LTC2978A will not accept any commands while it is transferring the fault log RAM buffer to EEPROM space. The command byte will be NACKed.
Internal Fault log	10ms	An internal fault log event is a one time event that uploads the contents of the fault log to EEPROM in response to a fault. Internal fault logging may be disabled. Commands received during this EEPROM write are NACKed.
MFR_FAULT_LOG_RESTORE	2ms	The LTC2978A will not accept any commands while it is transferring EEPROM data to the fault log RAM buffer. The command byte will be NACKed.

*The typical delay is measured from the command's stop to the next command's start.

COMMAND	TYPICAL DELAY*	COMMENT
MFR_CONFIG_LTC2978	<50µs	The LTC2978A will not accept any commands while it is completing this command. The command byte will be NACKed.

*The typical delay is measured from the command's stop to the next command's start.

Other PMBus Timing Notes

COMMAND	COMMENT
CLEAR_FAULTS	The LTC2978A will accept commands while it is completing this command but the affected status flags will not be cleared for up to 500µs.

PMBus COMMAND SUMMARY

Summary Table

COMMAND NAME	CMD CODE	DESCRIPTION	TYPE	PAGED	DATA FORMAT	UNITS	EEPROM	DEFAULT VALUE FLOAT HEX	REF PAGE
PAGE	0x00	Channel or page currently selected for any command that supports paging.	R/W Byte	N	Reg			0x00	30
OPERATION	0x01	Operating mode control. On/Off, Margin High and Margin Low.	R/W Byte	Y	Reg		Y	0x00	31
ON_OFF_CONFIG	0x02	CONTROL pin & PMBus bus on/off command setting.	R/W Byte	Y	Reg		Y	0x12	32
CLEAR_FAULTS	0x03	Clear any fault bits that have been set.	Send Byte	Y				NA	32
WRITE_PROTECT	0x10	Level of protection provided by the device against accidental changes.	R/W Byte	N	Reg		Y	0x00	33
STORE_USER_ALL	0x15	Store entire operating memory to EEPROM.	Send Byte	N				NA	33
RESTORE_USER_ALL	0x16	Restore entire operating memory from EEPROM.	Send Byte	N				NA	33
CAPABILITY	0x19	Summary of PMBus optional communication protocols supported by this device.	R Byte	N	Reg			0xE0	33
VOUT_MODE	0x20	Output voltage data format and mantissa exponent. (2^{-13})	R Byte	Y	Reg			0x13	34
VOUT_COMMAND	0x21	Servo Target. Nominal DC/DC converter output voltage setpoint.	R/W Word	Y	L16	V	Y	1.0 0x2000	34
VOUT_MAX	0x24	Upper limit on the output voltage the unit can command regardless of any other commands.	R/W Word	Y	L16	V	Y	4.0 0x8000	34
VOUT_MARGIN_HIGH	0x25	Margin high DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	1.05 0x219A	34
VOUT_MARGIN_LOW	0x26	Margin low DC/DC converter output voltage setting.	R/W Word	Y	L16	V	Y	0.95 0x1E66	34
VIN_ON	0x35	Input voltage (V_{IN_SNS}) above which power conversion can be enabled.	R/W Word	N	L11	V	Y	10.0 0xD280	34
VIN_OFF	0x36	Input voltage (V_{IN_SNS}) below which power conversion is disabled. All V_{OUT_EN} pins go off immediately.	R/W Word	N	L11	V	Y	9.0 0xD240	34
VOUT_OV_FAULT_LIMIT	0x40	Output overvoltage fault limit.	R/W Word	Y	L16	V	Y	1.1 0x2333	34
VOUT_OV_FAULT_RESPONSE	0x41	Action to be taken by the device when an output overvoltage fault is detected.	R/W Byte	Y	Reg		Y	0x80	36
VOUT_OV_WARN_LIMIT	0x42	Output overvoltage warning limit.	R/W Word	Y	L16	V	Y	1.075 0x2266	34
VOUT_UV_WARN_LIMIT	0x43	Output undervoltage warning limit.	R/W Word	Y	L16	V	Y	0.925 0x1D9A	34
VOUT_UV_FAULT_LIMIT	0x44	Output undervoltage fault limit. Limit used to determine if TON_MAX_FAULT has been met and the unit is on.	R/W Word	Y	L16	V	Y	0.9 0x1CCD	34
VOUT_UV_FAULT_RESPONSE	0x45	Action to be taken by the device when an output undervoltage fault is detected.	R/W Byte	Y	Reg		Y	0x7F	36
OT_FAULT_LIMIT	0x4F	Overtemperature fault limit.	R/W Word	N	L11	°C	Y	85.0 0xEAA8	35