
Chipsmall
深圳市津利帝科技有限公司
Geelead Technology Limited
Chipsmall
采购部
情暖大凉山
公益助学行动

LTC2992

Dual Wide Range Power Monitor

FEATURES

- **Rail-to-Rail Input Range: 0V to 100V**
- **Wide Input Supply Range: 2.7V to 100V**
- **Measures Current, Voltage, and Power**
- **Shunt Regulator for Supplies >100V**
- **8-/12-Bit ADCs with Less Than ±0.3% Total Unadjusted Error**
- Four General Purpose Inputs/Outputs Configurable as ADC Inputs
- Continuous Scan and Snapshot Modes
- Stores Minimum and Maximum Measurements
- Alerts When Alarm Thresholds Exceeded
- Shutdown Mode with $I_Q < 50\mu A$
- Split SDA Pin Eases Opto-Isolation
- Available in 16-Lead 4mm × 3mm DFN and MSOP Packages

APPLICATIONS

- Telecom Infrastructure
- Industrial Equipment
- Automotive
- Computer Systems and Servers

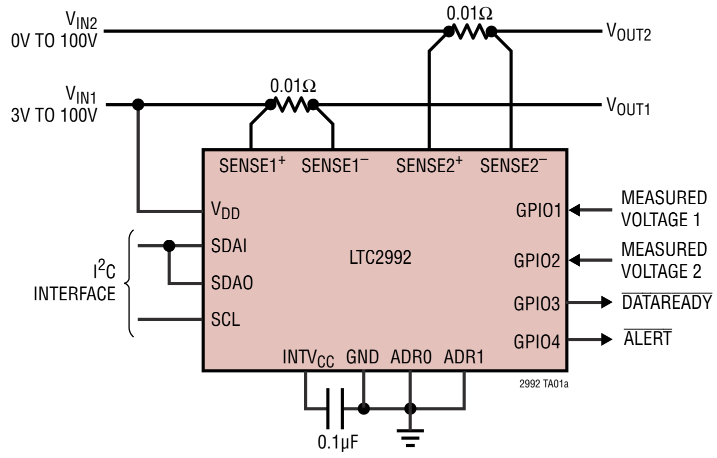
DESCRIPTION

The LTC®2992 is a rail-to-rail system monitor that measures current, voltage, and power of two supplies. It features an operating range of 2.7V to 100V and includes a shunt regulator for supplies above 100V. The voltage measurement range of 0V to 100V is independent of the input supply. Two ADCs simultaneously measure each supply's current. A third ADC monitors the input voltages and four auxiliary external voltages. Each supply's current and power is added for total system consumption. Minimum and maximum values are stored and an overrange alert with programmable thresholds minimizes the need for software polling. Data is reported via a standard I^2C interface. Shutdown mode reduces current consumption to 25µA typically.

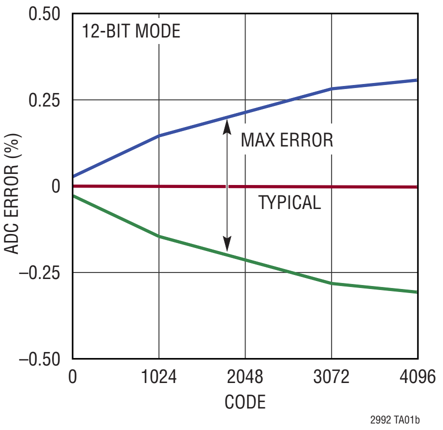
The LTC2992 I^2C interface includes separate data input and output pins for use with standard or opto-isolated I^2C connections. The LTC2992-1 has an inverted data output for use with inverting opto-isolator configurations.

TYPICAL APPLICATION

Dual Wide Range Power Monitor



ADC Error (GPIO)



ABSOLUTE MAXIMUM RATINGS

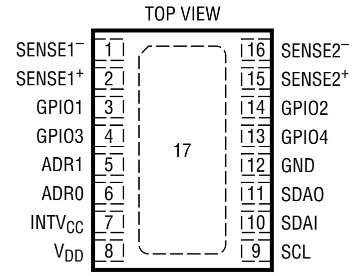
(Notes 1, 2)

Supply Voltages	
V_{DD}	–0.3V to 100V
$INTV_{CC}$ (Note 3)	–0.3V to Lesser of 5.8V, V_{DD} + 0.3V
Analog Input Voltages	
SENSEn⁺, SENSEn⁻	–1V to 100V
SENSEn⁺ to SENSEn⁻	–1V to 1V
ADR0, ADR1	–0.3V to 7V
GPIO1-4	–0.3V to 7V
Digital Input/Output Voltages	
SCL, SDAI (Note 4)	–0.3V to 5.9V
SDAO, $\overline{\text{SDAO}}$, GPIO1-4	–0.3V to 7V

Average Pin Currents	
$INTV_{CC}$	–10mA to 35mA
SCL, SDAI	5mA
SDAO, $\overline{\text{SDAO}}$, GPIO1-4	20mA
Operating Junction Temperature Range	
LTC2992C	0°C to 70°C
LTC2992I	–40°C to 85°C
LTC2992H	–40°C to 125°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10sec)	
MS Package Only	300°C

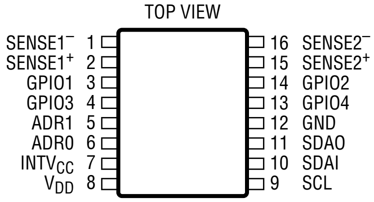
PIN CONFIGURATION

LTC2992



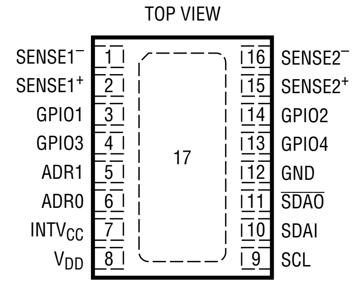
DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 17) PCB GND CONNECTION IS OPTIONAL

LTC2992



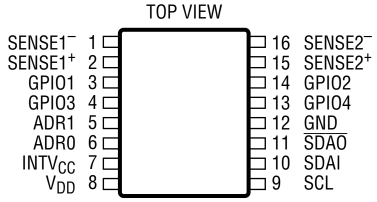
MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W, θ_{JC} = 21°C/W

LTC2992-1



DE PACKAGE
16-LEAD (4mm × 3mm) PLASTIC DFN
T_{JMAX} = 150°C, θ_{JA} = 43°C/W, θ_{JC} = 5.5°C/W
EXPOSED PAD (PIN 17) PCB GND CONNECTION IS OPTIONAL

LTC2992-1



MS PACKAGE
16-LEAD PLASTIC MSOP
T_{JMAX} = 150°C, θ_{JA} = 120°C/W, θ_{JC} = 21°C/W

ORDER INFORMATION http://www.linear.com/product/LTC2992#orderinfo

TUBE	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC2992CDE#PBF	LTC2992CDE#TRPBF	2992	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2992IDE#PBF	LTC2992IDE#TRPBF	2992	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2992HDE#PBF	LTC2992HDE#TRPBF	2992	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2992CDE-1#PBF	LTC2992CDE-1#TRPBF	29921	16-Lead (4mm × 3mm) Plastic DFN	0°C to 70°C
LTC2992IDE-1#PBF	LTC2992IDE-1#TRPBF	29921	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 85°C
LTC2992HDE-1#PBF	LTC2992HDE-1#TRPBF	29921	16-Lead (4mm × 3mm) Plastic DFN	–40°C to 125°C
LTC2992CMS#PBF	LTC2992CMS#TRPBF	2992	16-Lead Plastic MSOP	0°C to 70°C
LTC2992IMS#PBF	LTC2992IMS#TRPBF	2992	16-Lead Plastic MSOP	–40°C to 85°C
LTC2992HMS#PBF	LTC2992HMS#TRPBF	2992	16-Lead Plastic MSOP	–40°C to 125°C
LTC2992CMS-1#PBF	LTC2992CMS-1#TRPBF	29921	16-Lead Plastic MSOP	0°C to 70°C
LTC2992IMS-1#PBF	LTC2992IMS-1#TRPBF	29921	16-Lead Plastic MSOP	–40°C to 85°C
LTC2992HMS-1#PBF	LTC2992HMS-1#TRPBF	29921	16-Lead Plastic MSOP	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 3V to 100V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{DD}	V_{DD} Input Supply Voltage		●	3		100	V
V_{CC}	$INTV_{CC}$ Input Supply Voltage		●	2.7		5.8	V
I_{DD}	V_{DD} Supply Current	V_{DD} = 48V, $INTV_{CC}$ Open Shutdown	● ●		1.2 25	1.6 50	mA µA
I_{CC}	$INTV_{CC}$ Supply Current	$INTV_{CC}$ = V_{DD} = 5V Shutdown	● ●		1.0 25	1.4 50	mA µA
$V_{CC(LDO)}$	$INTV_{CC}$ Linear Regulator Voltage	8V < V_{DD} < 100V I_{LOAD} = 0mA	●	4.6	5	5.4	V
$\Delta V_{CC(LDO)}$	$INTV_{CC}$ Linear Regulator Load Regulation	8V < V_{DD} < 100V I_{LOAD} = 0mA to 10mA	●		100	250	mV
V_{CCZ}	Shunt Regulator Voltage at $INTV_{CC}$	V_{DD} = 48V, I_{CC} = 1.5mA	●	5.8	6.2	6.7	V
ΔV_{CCZ}	Shunt Regulator Load Regulation	V_{DD} = 48V, I_{CC} = 1.5mA to 35mA	●			250	mV
$V_{CC(UVL)}$	$INTV_{CC}$ Supply Undervoltage Lockout	$INTV_{CC}$ Rising, V_{DD} = $INTV_{CC}$	●	2.2	2.5	2.69	V
$V_{DD(UVL)}$	V_{DD} Supply Undervoltage Lockout	V_{DD} Rising, $INTV_{CC}$ Open	●	2.4	2.7	3	V
$V_{CCI2C(RST)}$	$INTV_{CC}$ I^2C Logic Reset	$INTV_{CC}$ Falling, V_{DD} = $INTV_{CC}$	●	1.7	2.1		V
$V_{DDI2C(RST)}$	V_{DD} I^2C Logic Reset	V_{DD} Falling, $INTV_{CC}$ Open	●	1.7	2.1		V
SENSE Inputs							
$I_{SENSE^+(HI)}$	48V SENSE$^+$ Input Current	SENSE$^+$, SENSE$^-$, V_{DD} = 48V Shutdown	● ●		120	170 2	µA µA
$I_{SENSE^-(HI)}$	48V SENSE$^-$ Input Current	SENSE$^+$, SENSE$^-$, V_{DD} = 48V Shutdown	● ●			20 1	µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 3V to 100V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SENSE^+(LO)}$	0V SENSE$^+$ Source Current	SENSE$^+$, SENSE$^-$ = 0V, V_{DD} = 48V	●			–10	µA
		Shutdown	●			–1	µA
$I_{SENSE^-(LO)}$	0V SENSE$^-$ Source Current	SENSE$^+$, SENSE$^-$ = 0V, V_{DD} = 48V	●			–5	µA
		Shutdown	●			–1	µA
ADC							
RES	Resolution (No Missing Codes)	NADC[7] = 1	●	8			Bits
	(Note 5)	NADC[7] = 0	●	12			Bits
V_{FS}	Full-Scale Voltage	ΔSENSE (Note 6)	●	50.9	51.2	51.5	mV
		SENSE$^+$	●	102	102.4	102.8	V
		GPIO	●	2.042	2.048	2.054	V
LSB	LSB Step Size	ΔSENSE			200		µV
	8-Bit Mode	SENSE$^+$			400		mV
		GPIO			8		mV
	LSB Step Size	ΔSENSE			12.5		µV
	12-Bit Mode	SENSE$^+$			25		mV
		GPIO			0.5		mV
TUE	Total Unadjusted Error (Note 7)	ΔSENSE	●			±0.8	%
	8-Bit Mode	SENSE$^+$	●			±0.8	%
		GPIO	●			±0.8	%
	Total Unadjusted Error	ΔSENSE	●			±0.6	%
	12-Bit Mode	SENSE$^+$	●			±0.4	%
		GPIO	●			±0.3	%
V_{OS}	Offset Error 8-Bit Mode	ΔSENSE, SENSE$^+$, GPIO	●			±1	LSB
	Offset Error	ΔSENSE (C-, I-Grade)	●			±2.1	LSB
	12-Bit Mode	ΔSENSE (H-Grade)	●			±3.1	LSB
		SENSE$^+$	●			±1.5	LSB
		GPIO	●			±1.1	LSB
INL	Integral Nonlinearity 8-Bit Mode	ΔSENSE, SENSE$^+$, GPIO	●			±1	LSB
	Integral Nonlinearity	ΔSENSE	●			±3.5	LSB
	12-Bit Mode	SENSE$^+$, GPIO	●			±2	LSB
σ_T	Transition Noise	ΔSENSE			0.5		μV_{RMS}
		SENSE$^+$			0.3		mV_{RMS}
		GPIO			5		μV_{RMS}
t_{CONV}	Conversion Time (Snapshot Mode)	ΔSENSE	●	3.9	4.1	4.3	ms
	8-Bit Mode	SENSE$^+$, GPIO	●	0.97	1.02	1.08	ms
	Conversion Time (Snapshot Mode)	ΔSENSE	●	62.4	65.6	68.8	ms
	12-Bit Mode	SENSE$^+$, GPIO	●	15.6	16.4	17.2	ms
GPIO							
$V_{GPIO(TH)}$	GPIO Pin Input Threshold	V_{GPIO} Rising	●	1.13	1.23	1.33	V
$V_{GPIO(OL)}$	GPIO Pin Output Low Voltage	I_{GPIO} = 8mA	●		0.15	0.4	V
I_{GPIO}	GPIO Pin Input Current	V_{DD} = 48V, GPIO = 3V	●		0	±1	µA
I^2C Interface (V_{DD} = 48V)							
$V_{ADR(H)}$	ADR0, ADR1 Input High Threshold		●	1.8	2.4	2.7	V
$V_{ADR(L)}$	ADR0, ADR1 Input Low Threshold		●	0.3	0.6	0.9	V
$I_{ADR(IN)}$	ADR0, ADR1 Input Current	ADR0, ADR1 = 0V, 3V	●			±13	µA
$I_{ADR(IN,Z)}$	Allowable Leakage When Open		●			±7	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{DD} is from 3V to 100V unless otherwise noted. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{OD(OL)}$	SDAO, $\overline{\text{SDAO}}$, Output Low Voltage	I_{SDAO}, $I_{\overline{SDAO}}$ = 8mA	●		0.15	0.4	V
$I_{SDA,SCL(IN)}$	SDAI, SDAO, $\overline{\text{SDAO}}$, SCL Leakage Current	SDAI, SDAO, $\overline{\text{SDAO}}$, SCL = 5V	●		0	±1	µA
$V_{SDA,SCL(TH)}$	SDAI, SCL Input Threshold		●	1.5	1.8	2.1	V
$V_{SDA,SCL(CL)}$	SDAI, SCL Clamp Voltage	I_{SDAI}, I_{SCL} = 0.5mA, 5mA	●	5.9		6.9	V
I^2C Interface Timing							
$f_{SCL(MAX)}$	Maximum SCL Clock Frequency		●	400			kHz
t_{LOW}	SCL Low Period		●		0.65	1.3	µs
t_{HIGH}	SCL High Period		●		50	600	ns
$t_{BUF(MIN)}$	Bus Free Time Between STOP/START Condition		●		0.12	1.3	µs
$t_{HD,\ STA(MIN)}$	Hold Time after (Repeated) START Condition		●		140	600	ns
$t_{SU,\ STA(MIN)}$	Repeated START Condition Setup Time		●		30	600	ns
$t_{SU,\ STO(MIN)}$	STOP Condition Setup Time		●		30	600	ns
$t_{HD,\ DATI(MIN)}$	Data Hold Time Input		●		–100	0	ns
$t_{HD,\ DATO(MIN)}$	Data Hold Time Output		●	300	600	900	ns
$t_{SU,\ DAT(MIN)}$	Data Setup Time		●		30	100	ns
$t_{SP(MAX)}$	Maximum Suppressed Spike Pulse Width		●	50	110	250	ns
t_{RST}	Stuck Bus Reset Time	SCL or SDAI Held Low	●	25	33		ms
C_X	SCL, SDAI Input Capacitance (Note 5)				5	10	pF

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into pins are positive. All voltages are referenced to ground, unless otherwise noted.

Note 3: An internal shunt regulator limits the $INTV_{CC}$ pin to a minimum of 5.8V. Driving this pin to voltages beyond 5.8V may damage the part. This pin can be safely tied to higher voltages through a resistor that limits the current below 35mA.

Note 4: Internal clamps limit the SCL and SDAI pins to a minimum of 5.9V. Driving these pins to voltages beyond the clamp may damage the part. The pins can be safely tied to higher voltages through resistors that limit the current below 5mA.

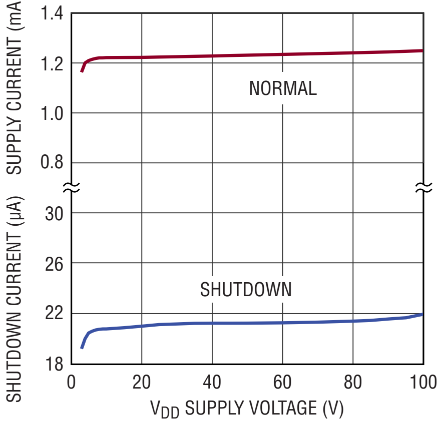
Note 5: Guaranteed by design and not subjected to test.

Note 6: ∆SENSE is defined as $V_{SENSE}^+ - V_{SENSE}^-$

Note 7: TUE is the maximum ADC error for any code expressed as a percentage of full-scale.

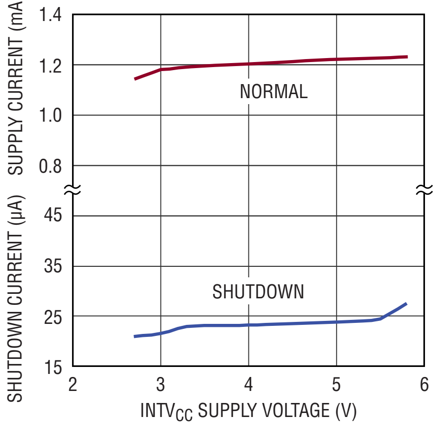
TYPICAL PERFORMANCE CHARACTERISTICS

V_{DD} Supply Current



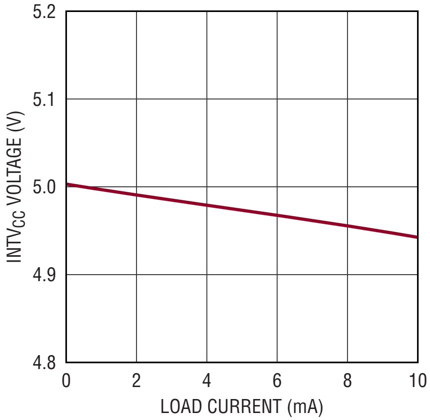
2992 G01

INTV$_{CC}$ Supply Current



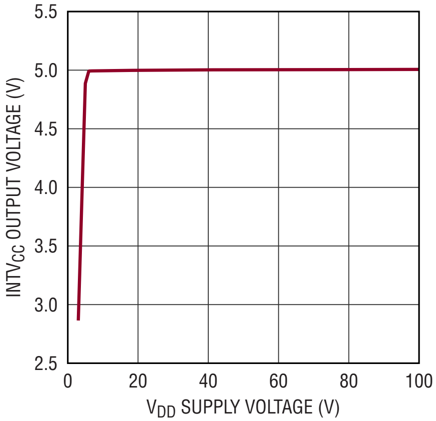
2992 G02

INTV$_{CC}$ Load Regulation



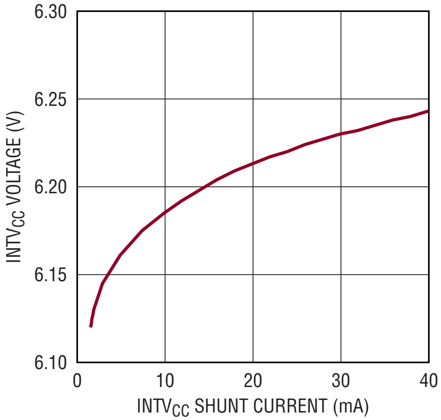
2992 G03

INTV$_{CC}$ Line Regulation



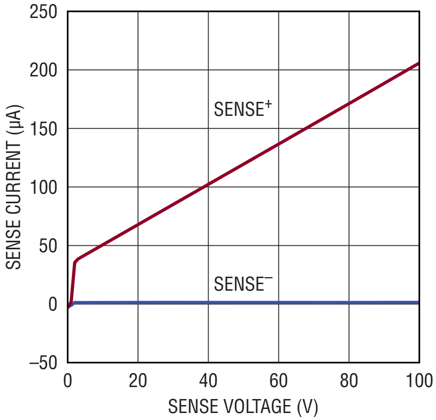
2992 G04

INTV$_{CC}$ Shunt Regulator Load Regulation



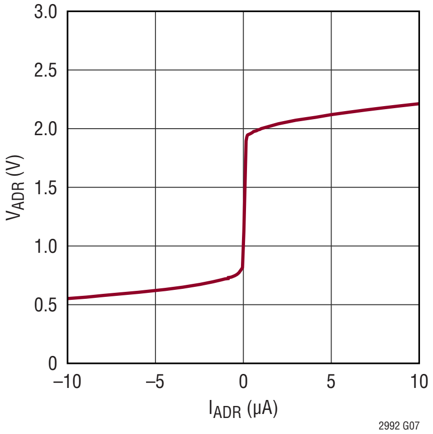
2992 G05

SENSE Input Current



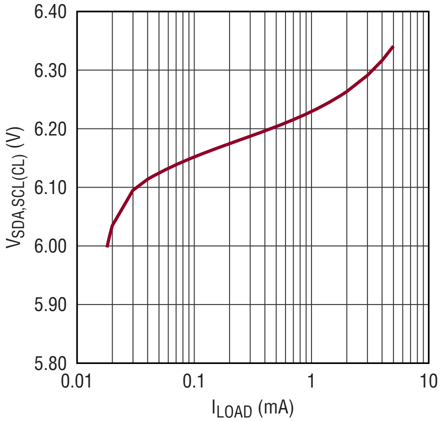
2992 G06

ADR Voltage with Current Source or Sink



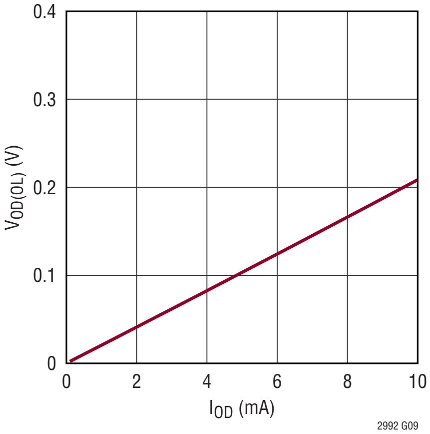
2992 G07

SCL/SDAI Loaded Clamp Voltage vs Load Current



2992 G08

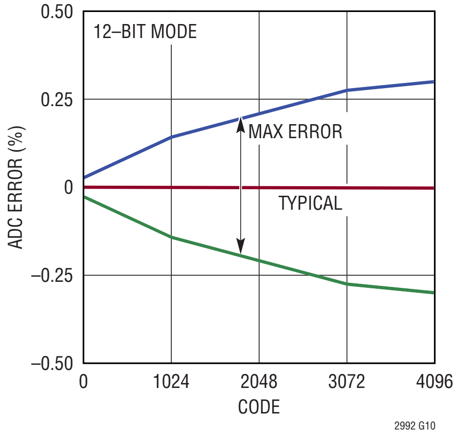
GPIO, SDAO, $\overline{\text{SDAO}}$ Loaded Output Low Voltage vs Load Current



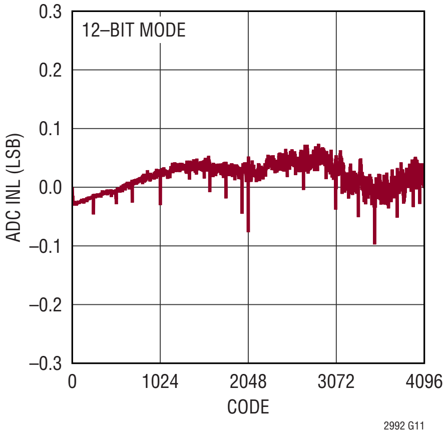
2992 G09

TYPICAL PERFORMANCE CHARACTERISTICS

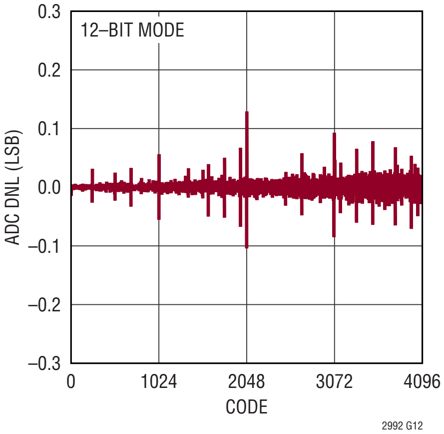
ADC Error (GPIO)



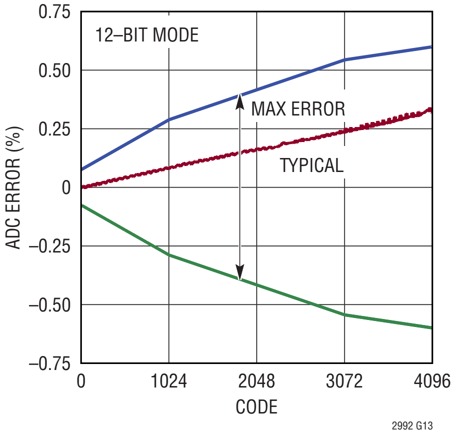
ADC Integral Nonlinearity (GPIO)



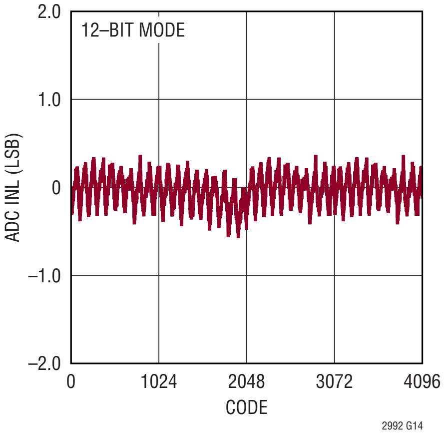
ADC Differential Nonlinearity (GPIO)



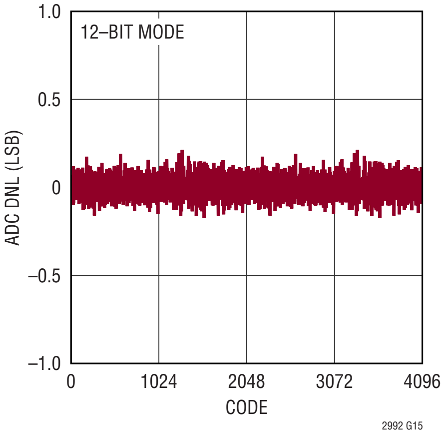
ADC Error (ΔSENSE)



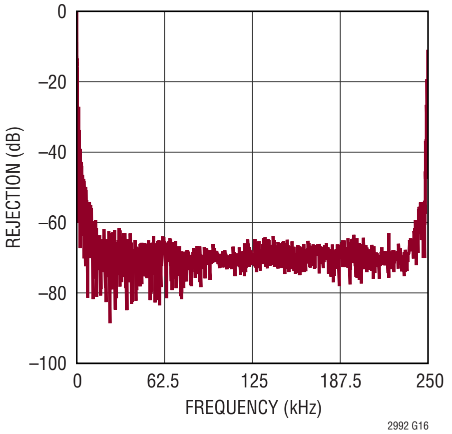
ADC Integral Nonlinearity (ΔSENSE)



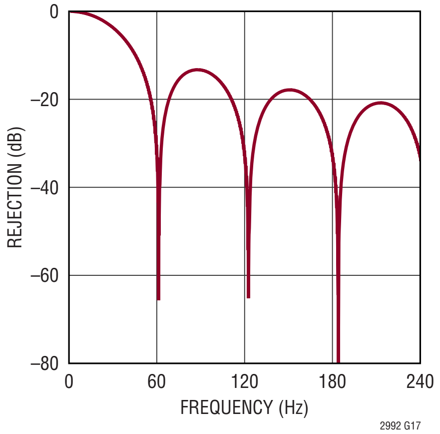
ADC Differential Nonlinearity (ΔSENSE)



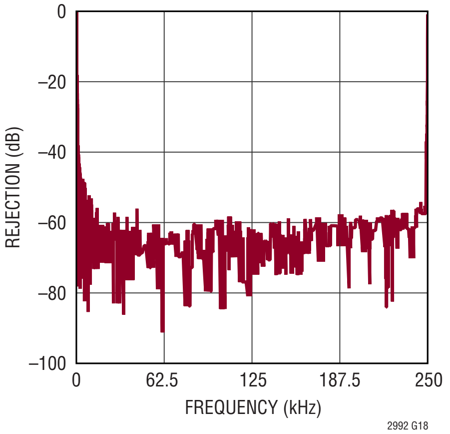
ADC Input Signal Attenuation (GPIO)



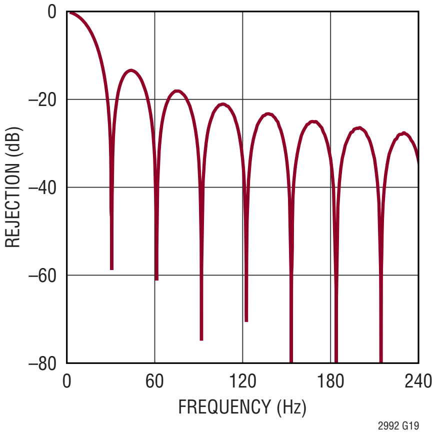
ADC Input Signal Attenuation (GPIO, Low Frequencies)

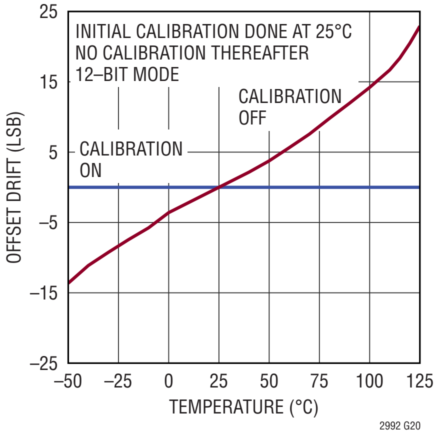


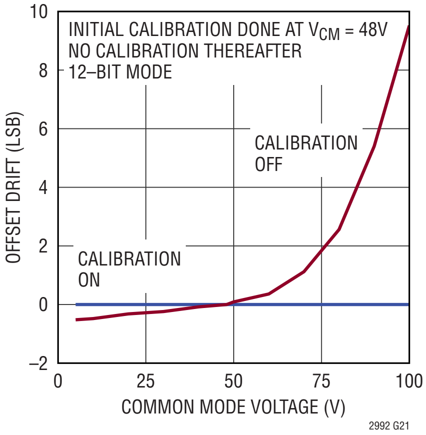
ADC Input Signal Attenuation (ΔSENSE)



TYPICAL PERFORMANCE CHARACTERISTICS


ADC Input Signal Attenuation (ΔSENSE, Low Frequencies)


Current Sense Amplifier Offset Drift Over Temperature


Current Sense Amplifier Offset Drift Over Input Common Mode

PIN FUNCTIONS

ADR1, ADR0: I^2C Device Address Inputs. Connecting these pins to $INTV_{CC}$, GND or leaving the pins open configures one of nine possible addresses. See Table 3 in Applications Information section for details.

EXPOSED PAD: Exposed Pad may be left open or connected to device ground. For best thermal performance, connect to a copper plane with an array of vias.

GND: Device Ground.

GPIO1, GPIO2: General Purpose Input/Output (Open Drain). Configurable to general purpose output, logic input, or data converter input. Tie to ground if unused. See Table 18 in Applications Information section for details.

GPIO3: General Purpose Input/Output (Open Drain). Configurable to general purpose output, logic input, data converter input or data ready signal ($\overline{\text{DATAREADY}}$). As $\overline{\text{DATAREADY}}$, it is latched low or pulses low for 16μs or 128μs when any of the ADC's data becomes available. Tie to ground if unused. See Table 18 in Applications Information section for details.

GPIO4: General Purpose Input/Output (Open Drain). Configurable to general purpose output, logic input, data converter input or SMBus alert ($\overline{\text{ALERT}}$). As $\overline{\text{ALERT}}$, it is pulled to ground when a fault occurs to alert the host controller. A fault alert is enabled by setting the corresponding bit in the ALERT registers as shown in Tables 7, 11, 13 and 15. Tie to ground if unused. See Tables 18 and 19 in Applications Information section for details.

$INTV_{CC}$: Internal Low Voltage Supply Input/Output. This pin is used to power internal circuitry. It can be configured as a direct input for a low voltage supply, as linear regulator from a higher voltage supply connected to V_{DD}, or as a shunt regulator. Connect this pin directly to a 2.7V to 5.8V supply if available. When $INTV_{CC}$ is powered from an external supply, connect the V_{DD} pin to $INTV_{CC}$. If V_{DD} is connected to a 8V to 100V supply, $INTV_{CC}$ becomes the 5V output of an internal series regulator that can supply up to 10mA to external circuitry. For even higher supply voltages or if a floating topology is desired, $INTV_{CC}$ can be used as a 6.2V shunt regulator. Connect the supply to

PIN FUNCTIONS

INTV_{CC} through a resistor or current source that limits the current to less than 35mA. An undervoltage lockout circuit disables the ADC when the voltage at this pin drops below 2.5V. Connect a bypass capacitor of 0.1µF or greater from this pin to ground. If an external load is present, for loop stability, use a bypass capacitor of 1µF or greater. See Flexible Power Supply section.

SCL: I^2C Bus Clock Input. Data at the SDAI pin is shifted in or out on rising edges of SCL. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SCL and V_{DD} or INTV_{CC}. The voltage at SCL is internally clamped to 6.3V typically.

SDAI: I^2C Bus Data Input. Used for shifting in address, command or data bits. This pin is driven by an open-collector output from a master controller. An external pull-up resistor or current source is required and can be placed between SDAI and V_{DD} or INTV_{CC}. The voltage at SDAI is internally clamped to 6.3V typically. Tie to SDAO for normal I^2C operation.

SDAO (LTC2992 only): I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. An external pull-up resistor or current source is required. Tie to SDAI for normal I^2C operation.

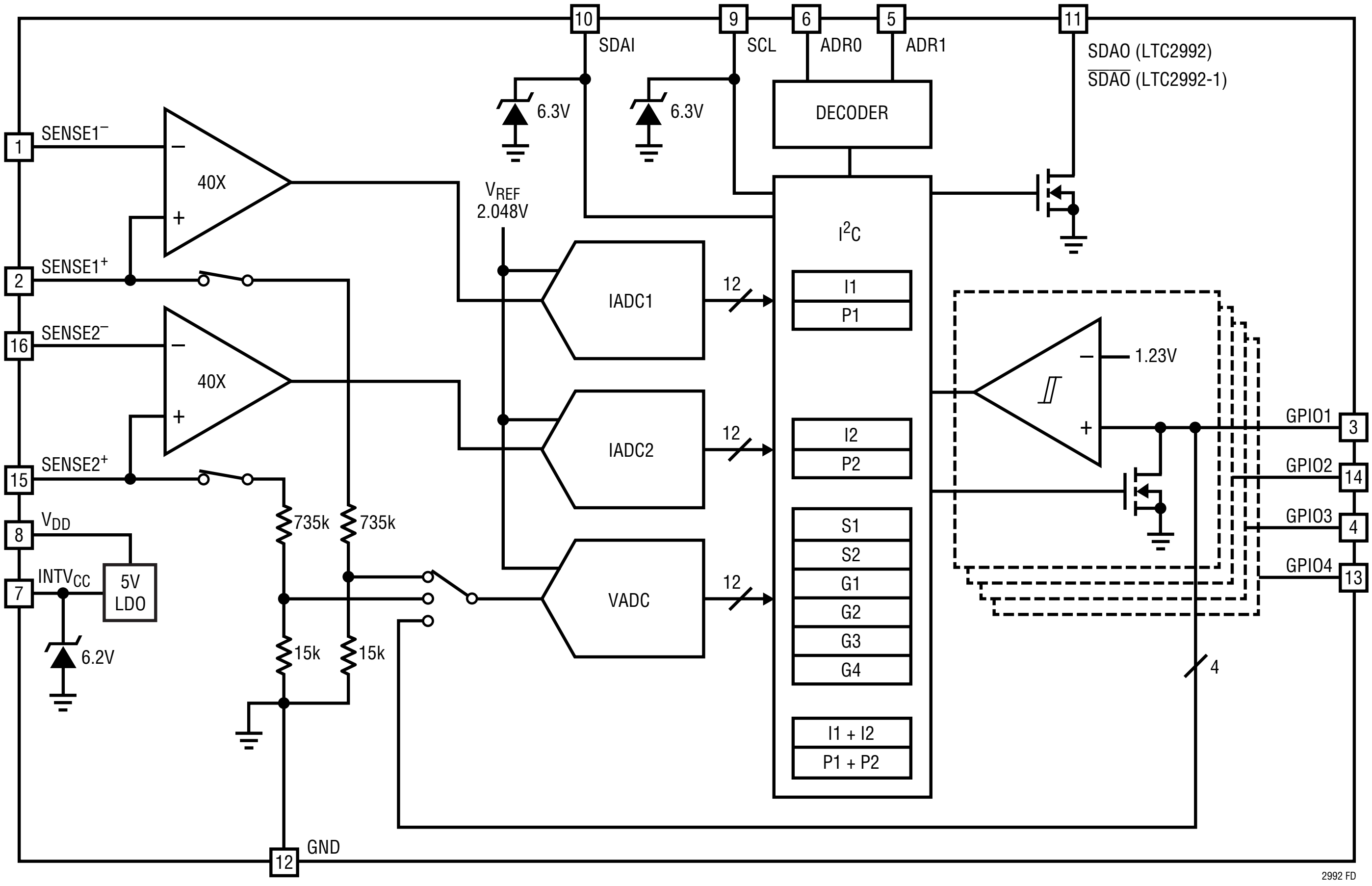
$\overline{\text{SDAO}}$ (LTC2992-1 only): Inverted I^2C Bus Data Output. Open-drain output used for sending data back to the master controller or acknowledging a write operation. Data is inverted for convenience of opto-isolation. An external pull-up resistor or current source is required. The LTC2992-1 cannot be used in nonisolated I^2C applications without additional components.

SENSE1^+, SENSE2^+: Supply Voltage and Current Sense Input. Used as a voltage supply and current sense input for internal current sense amplifier. The voltage at this pin is monitored by the onboard ADC with a full-scale input range of 102.4V. See Figure 19 for recommended Kelvin connection.

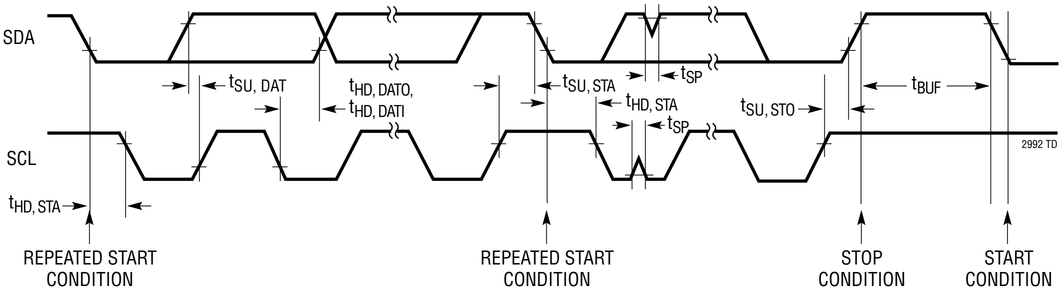
SENSE1^-, SENSE2^-: Current Sense Input. Connect an external sense resistor between SENSE^+ and SENSE^-. The differential voltage between SENSE^+ and SENSE^- is monitored by the onboard ADC with a full-scale sense voltage of 51.2mV. Tie both SENSE^- and SENSE^+ together to a voltage between 0V and 100V if current measurement is unused.

V_{DD}: High Voltage Supply Input. This pin powers an internal series regulator with input voltages ranging from 3V to 100V and produces 5V at INTV_{CC} when V_{DD} is above 8V. Connect a bypass capacitor of 0.1µF or greater from this pin to ground if external load is present on the INTV_{CC} pin. See Flexible Power Supply section.

FUNCTIONAL DIAGRAM



TIMING DIAGRAM



OPERATION

The LTC2992 accurately monitors current, voltage and power of two 0V to 100V supplies. An internal linear regulator allows the LTC2992 to operate directly from a 3V to 100V rail, or from an external supply voltage between 2.7V and 5.8V. Quiescent current is less than 1.6mA in normal operation. Enabling shutdown mode via the I^{2}C interface reduces the quiescent current to below 50µA.

There are three onboard 8-/12-bit ADCs as shown in the Functional Diagram. Each supply's load current is measured with an external current sense resistor connected between SENSE$^+$ and SENSE$^-$. Internal amplifiers gain up the voltage drop across the sense resistor for monitoring by the IADCs (full-scale 51.2mV). VADC is used for voltage measurements and its input is selectively connected to SENSE1$^+$, SENSE2$^+$ (full-scale 102.4V) or any of the four GPIO pins (full-scale 2.048V). Each conversion takes 33ms for the IADCs and 16ms for the VADC in 12-bit mode. The conversion time can be shortened by a factor of 16 when 8-bit mode is selected.

The ADCs can be configured to run continuously (continuous scan) or on demand (snapshot mode). In continuous scan mode, the VADC measures selected voltages of the six inputs in round robin fashion. See the Applications Information section for more details. Status bits in the ADC STATUS register signal new conversion results from the ADCs have been written into onboard registers.

The GPIO1 to GPIO4 pins are also general purpose inputs or general purpose open-drain outputs. In addition, GPIO3 may be configured as $\overline{\text{DATAREADY}}$ output while GPIO4 is also an SMBus alert ($\overline{\text{ALERT}}$) output. $\overline{\text{DATAREADY}}$ indicates availability of the most recent conversion results from any of the ADCs while $\overline{\text{ALERT}}$ indicates one or more faults have occurred.

Onboard memory stores the minimum and maximum values for each ADC measurement and calculates power data by digitally multiplying the stored current and voltage data. When the ADC measured value falls outside its programmed window thresholds, a fault event is logged and the $\overline{\text{ALERT}}$ (GPIO4) may optionally pull low. The LTC2992 also calculates the total current and power consumption of the two monitored supplies.

The LTC2992 includes an I^{2}C interface to access the onboard data registers and to program the alert threshold, configuration and control registers. Two three-state pins, ADR1 and ADR0, are decoded to allow nine device addresses (see Table 3). The SDA pin is split into SDAI (input) and SDAO (output, LTC2992) or $\overline{\text{SDAO}}$ (output, LTC2992-1) to facilitate opto-isolation. Tie SDAI and SDAO together for normal, nonisolated I^{2}C operation.

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The LTC2992 offers a compact and complete solution to monitor power from two supply rails in high side and/or low side current sensing applications. With an input common mode range of 0V to 100V and a wide input supply operating voltage range from 2.7V to 100V, this device is ideal for a wide variety of power management applications including automotive, industrial and telecom infrastructure. The basic application circuit shown in Figure 1 provides monitoring of high side currents (5.12A/10.24A full-scale), input voltages (102.4V full-scale) and two external voltages (2.048V full-scale), all using internal 12-bit ADCs.

Data Converters

The LTC2992 features three ΔΣ A/D converters (ADC) that can be configured to 8- or 12-bit. The ΔΣ architecture inherently averages input signals and noise during the measurement period. Two ADCs (IADC1 and IADC2) monitor the differential voltages between $SENSE^+$ and $SENSE^-$ (ΔSENSE) with 51.2mV full-scale to allow accurate measurement of load currents across low value shunt resistors. The third ADC (VADC) monitors two $SENSE^+$ and four GPIO pins with full-scale of 102.4V for $SENSE^+$ and 2.048V for GPIO.

The supply voltage data are derived from $SENSE1^+$ and $SENSE2^+$ or GPIO1 and GPIO2 depending on the external application circuit. $SENSE1^+$ and $SENSE2^+$ are selected by default as these are normally connected to the supply voltages. In negative supply voltage systems, the supply voltages can be measured through external resistive dividers connected to the GPIO1 and GPIO2 pins. See Flexible Power Supply section for details.

The operation and conversion sequence of the ADCs, multiplier operand and VADC input selections are controlled by the settings in the CTRLA register as shown in Table 1.

The timing sequence for some of these configurations are shown in Figure 2 (2a to 2f). The timing diagram shown in Figure 2a illustrates the conversion sequence in the default configuration (CTRLA[7:0]=0x00). Upon power-up (t_1), the IADCs will always measure their corresponding current sense amplifier's offset (calibration) and then the load current (ΔSENSE1/2). Meanwhile, VADC begins measurement of $SENSE1^+$, $SENSE2^+$, GPIO1, GPIO2, GPIO3 and GPIO4 successively.

At t_3 a new IADC conversion begins. To generate power, the most recent voltage data (S1 at t_2, S2 at t_3) from VADC is stored in a latch as an operand to the adder as shown in Figure 3. IMOD1 represents IADC1's modulator which converts the load current into a 1-bit data stream. Each 1 in the bitstream adds to the accumulators the voltage data such that they contain the power values $I1 \times S1$ and $I2 \times S2$ at the end of the IADC conversions at t_5. Voltage latch content is then updated to the corresponding data registers. I1 is added to I2 to generate total current and P1 is added to P2 to generate total power. In the summing process, the least significant bit of the results are truncated. Consequently, the summing results need to be shifted one bit to the left to restore the correct quantity. Note that the

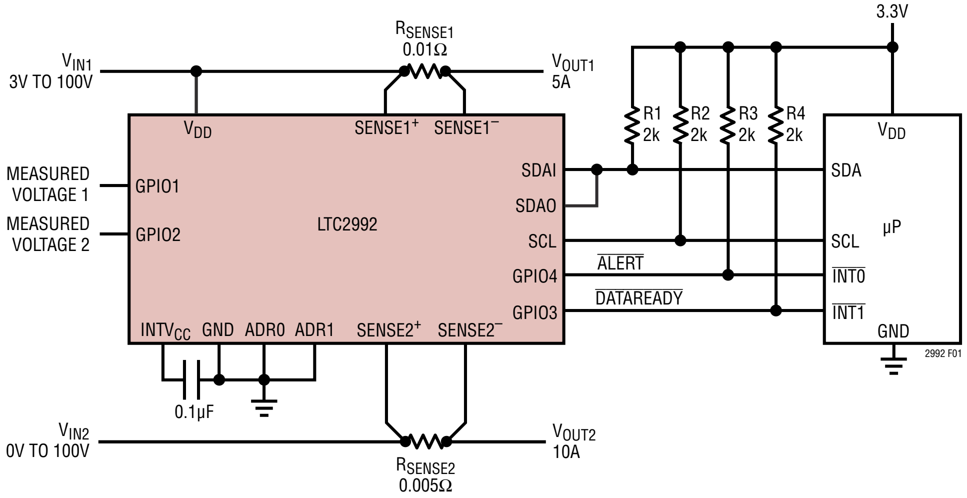

Figure 1. Dual High Side Power Monitor

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calculated LSB (see Design Example section) for current and power of both supplies have to match. Otherwise, external µP can be used to first compute physical amount of current and power for each supply and then perform the summing.

The LTC2992 measures the current sense amplifier's input offset to calibrate subsequent IADC measurements. During offset measurement, IADC cannot capture load current information. By default, such calibration is done for every IADC conversion as shown in Figure 2a. In most applications, the calibration frequency can be reduced by writing to CTRLA register with its CTRLA[7] bit set to 1. A one-off calibration is then performed immediately after the I^{2}C write operation as shown in Figure 2b.

VADC by default monitors six input voltages sequentially as shown in Figure 2a with an update rate of 10Hz for each input. Therefore, input signals such as supply rail voltages with average value that varies at less than 5Hz can be accurately monitored. Otherwise, the input update rate can be increased by reducing the number of inputs monitored via CTRLA[4:3]. Figure 2c shows only the SENSE$^+$ pins being monitored in continuous scan mode with an effective update rate of 30Hz. The remaining inputs may be monitored by switching to snapshot mode when needed.

A snapshot mode is available to make on-demand measurement of a single selected voltage without power data update (SENSE1$^+$, SENSE2$^+$, GPIO1, GPIO2, GPIO3 or GPIO4) or two selected voltages (either SENSE1$^+$ and SENSE2$^+$, or GPIO1 and GPIO2). To make a snapshot measurement, write the 3-bit code of the desired voltage input to CTRLA[2:0] and 01 to CTRLA[6:5]. After completion of the conversion, the ADCs will halt and the corresponding

Table 1. ADC Configuration Via CTRLA Register

BIT	NAME	OPERATION			
CTRLA[7]	Offset Calibration	Offset Calibration for Current Measurements [1] = Calibrate on Demand [0] = Every Conversion (Default)			
CTRLA[6:5]	Measurement Mode	[11] = Shutdown [10] = Single Cycle mode The VADC converts SENSE1$^+$, SENSE2$^+$, GPIO1, GPIO2, GPIO3, GPIO4 once and stops. The IADCs stop after one conversion. P1 = SENSE1$^+$ × ΔSENSE1; P2 = SENSE2$^+$ × ΔSENSE2 [01] = Snapshot Mode Snapshot Initializes Conversion on All 3 ADCs Simultaneously. VADC Converts the Channel(s) per CTRLA[2:0] [00] = Continuous Scan Mode (Default) The Selected Channels for VADC are Defined by CTRLA[4:3]			
CTRLA[4:3]	Voltage Selection for Continuous Scan Mode	CTRLA[4:3]	VADC	P1	P2
		11	GPIO1, GPIO2, GPIO3, GPIO4	GPIO1 × ΔSENSE1	GPIO2 × ΔSENSE2
		10	GPIO1, GPIO2	GPIO1 × ΔSENSE1	GPIO2 × ΔSENSE2
		01	SENSE1$^+$, SENSE2$^+$	SENSE1$^+$ × ΔSENSE1	SENSE2$^+$ × ΔSENSE2
		00 (Default)	SENSE1$^+$, SENSE2$^+$, GPIO1, GPIO2, GPIO3, GPIO4	SENSE1$^+$ × ΔSENSE1	SENSE2$^+$ × ΔSENSE2
CTRLA[2:0]	Voltage Selection for Snapshot Mode	CTRLA[2:0]	VADC	P1	P2
		111	GPIO1, GPIO2	GPIO1 × ΔSENSE1	GPIO2 × ΔSENSE2
		110	SENSE1$^+$, SENSE2$^+$	SENSE1$^+$ × ΔSENSE1	SENSE2$^+$ × ΔSENSE2
		101	GPIO4	ΔSENSE1/2 without P1/P2 updates	
		100	GPIO3		
		011	GPIO2		
		010	GPIO1		
		001	SENSE2$^+$		
		000 (Default)	SENSE1$^+$		

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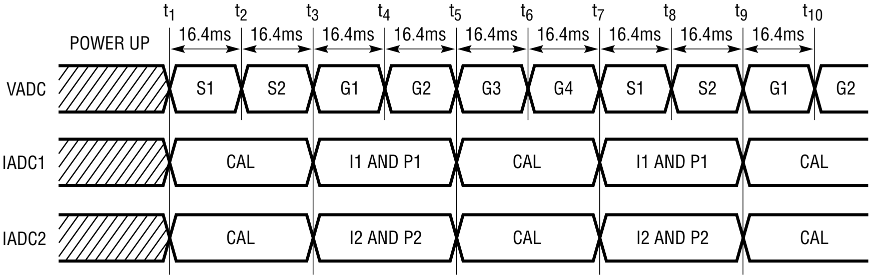
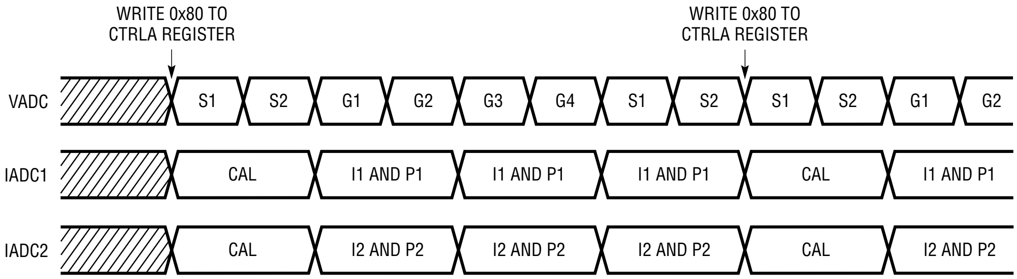
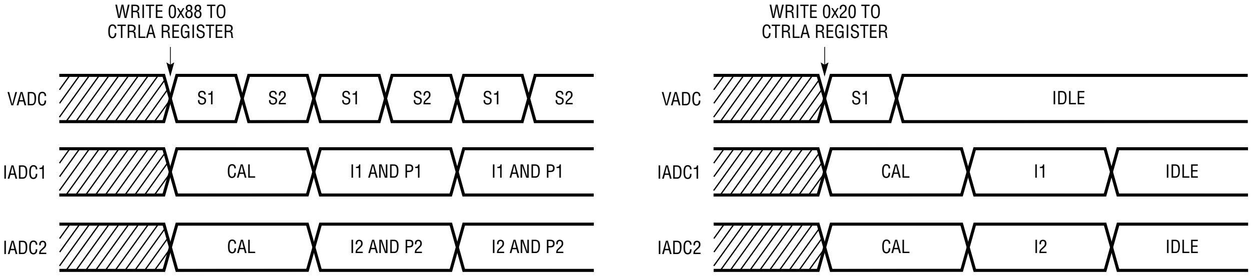


(2a) Continuous Scan Mode with Calibration Every Cycle (Default)
S1, S2, G1, G2, G3, G4: SENSE1$^+$, SENSE2$^+$, GPIO1, GPIO2, GPIO3, and GPIO4
CAL: Calibration of Current Sense Amplifier
I1, I2: ΔSENSE1, ΔSENSE2
P1, P2: POWER1, POWER2

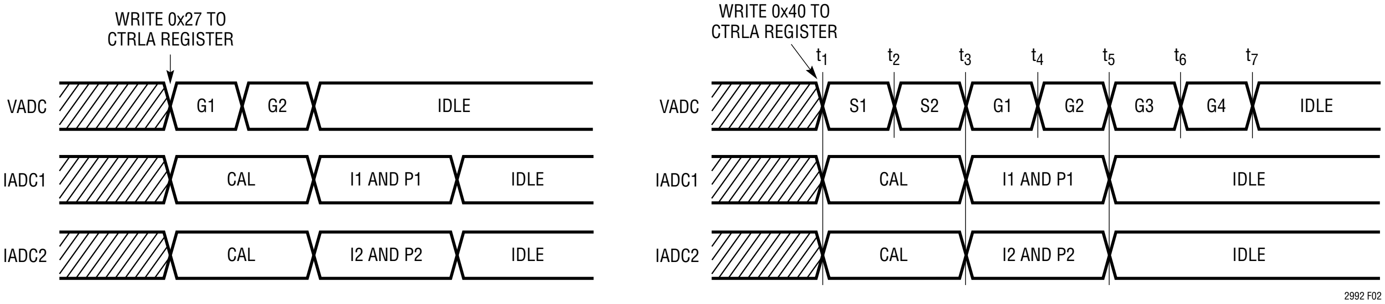


(2b) Continuous Scan Mode with On-Demand Calibration. CTRLA[7:0] = 0x80



(2c) Continuous Scan Mode with On-Demand Calibration. CTRLA[7:0] = 0x88

(2d) Snapshot Mode for Single Voltage. CTRLA[7:0] = 0x20



(2e) Snapshot Mode for Two Voltages. CTRLA[7:0] = 0x27

(2f) Single Cycle Mode. CTRLA[7:0] = 0x40

Figure 2

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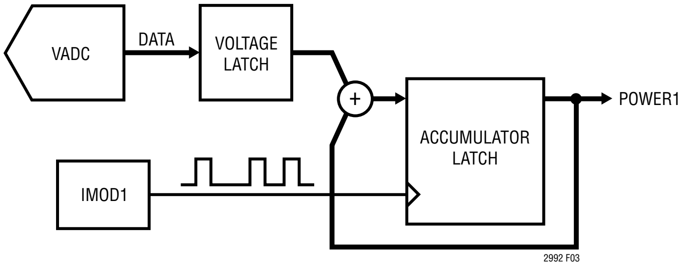


Figure 3. POWER1 Generator Blocks

bits in ADC STATUS register (Table 10) are set to indicate the availability of new data. An alert may be generated at the end of a snapshot conversion by setting bit AL4[7:6] in the ALERT4 register (Table 15). To make another snapshot measurement, rewrite the CTRLA register. Figure 2d shows a snapshot operation of SENSE1$^+$ with no updates to power data since only single voltage is selected while Figure 2e shows combo snapshot operation of GPIO1 and GPIO2 with new power data.

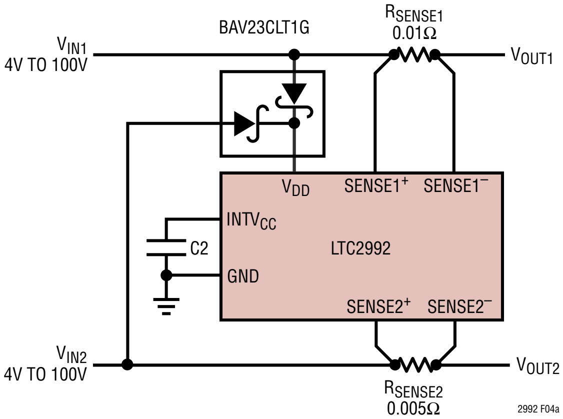
A single cycle mode allows all six voltages to be measured once with a single I^2C command. To initiate such mode, write 10 to CTRLA[6:5] as shown in Figure 2f. SENSE1$^+$, SENSE2$^+$ are updated together with current and power values at t_5. At t_7 the conversions are done and the ADCs are halted.

If there is an extended period of I^2C communication between the LTC2992 and the controller, some of the ADC result may be lost. This is because during the I^2C communication, the ADCs are prevented from updating the internal registers to avoid corrupting the data. This problem can be overcome by breaking the I^2C communication into blocks of less than one conversion period (16.4ms for 12-bit mode and 1ms for 8-bit mode).

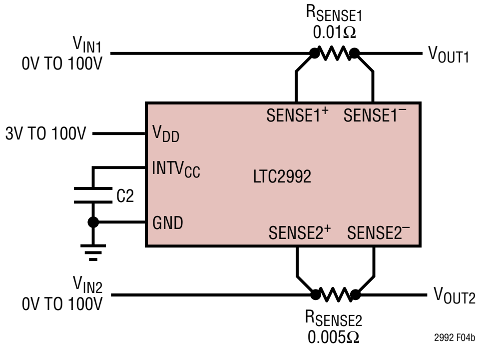
Flexible Power Supply

The LTC2992 can be externally configured to derive power from a wide range of supplies. The LTC2992 includes an onboard linear regulator to power the low voltage internal circuitry connected to the $INTV_{CC}$ pin from high V_{DD} voltages. The linear regulator operates with V_{DD} voltages from 3V to 100V, and a shunt regulator is available for voltages above 100V. The linear regulator produces a 5V output capable of supplying 10mA at the $INTV_{CC}$ pin when V_{DD} is greater than 8V. The regulator is disabled when the junction temperature rises above 150°C, and the output is protected against accidental shorts. Bypass capacitors of 0.1µF, or greater, at both the V_{DD} and $INTV_{CC}$ pins are recommended for optimal transient performance. Note that operation with high V_{DD} voltages can result in significant power dissipation, and care is required to ensure that the maximum operating junction temperature stays below 125°C. For improved thermal resistance, use the DFN package and solder the exposed pad to a large copper region on the PCB.

Figure 4a shows the LTC2992 being used to monitor input supplies that range from 4V to 100V. No separate supply is needed since V_{DD} can be connected to either of the input supplies. To prevent loss of operation from either supply's failure, V_{DD} is connected to V_{IN1} and V_{IN2} via diodes. If the LTC2992 is used to monitor input supplies of 0V to 100V, it can derive power from a wide range separate supply connected to the V_{DD} pin as shown in Figure 4b. The

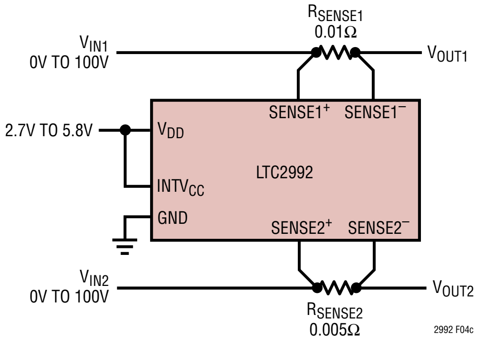


(4a) Derives Power from the Supplies Being Monitored



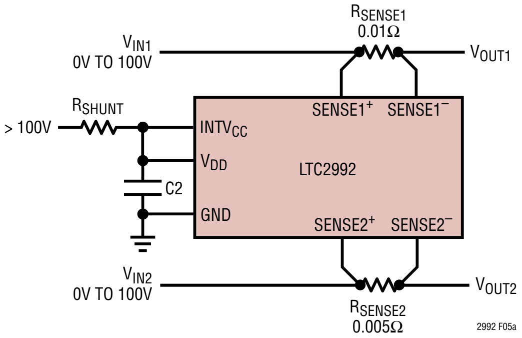
(4b) Derives Power from a Separate Wide Range Supply

APPLICATIONS INFORMATION



(4c) Derives Power from a Separate Low Voltage Supply

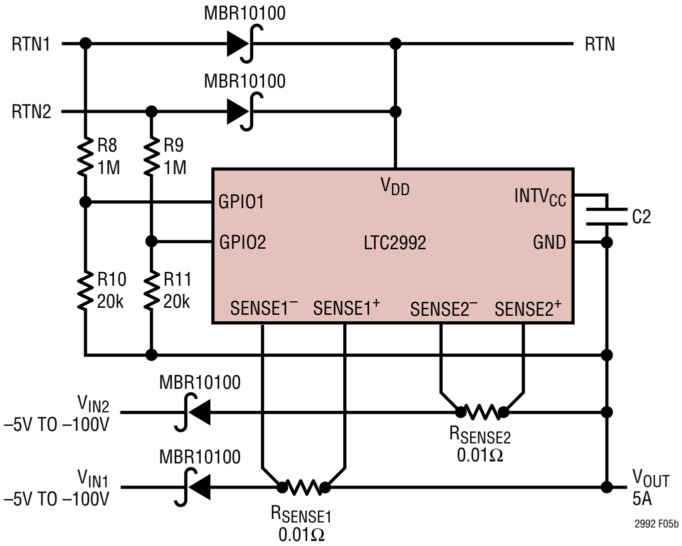
SENSE$^{+/–}$ pins can be biased independently of the part's supply voltage. Alternatively, if a low voltage supply is present it can be connected to the $INTV_{CC}$ pin, as shown in Figure 4c, to minimize on-chip power dissipation. When $INTV_{CC}$ is powered from a separate supply, connect V_{DD} to $INTV_{CC}$.



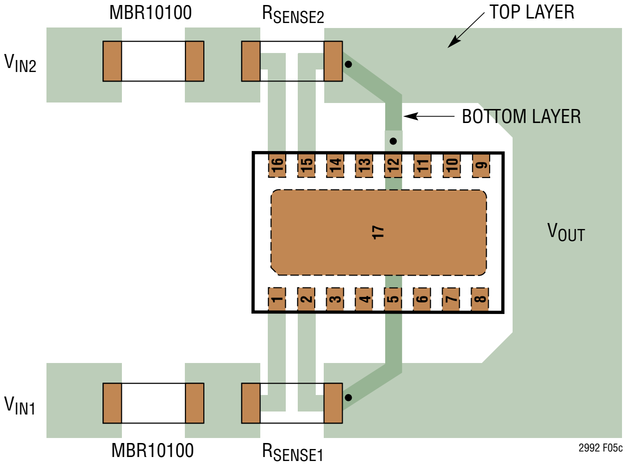
(5a) Derives Power Through a Low Side Shunt Regulator in a High Side Current Sense Topology

Figure 5a shows a high side rail-to-rail power monitor which derives power from a separate supply greater than 100V. The voltage at $INTV_{CC}$ is clamped at 6.3V above ground in a low side shunt regulator configuration to power the part.

In dual feed, low side power monitor applications, the device ground and the current sense inputs are connected to the diode-ORed output of the input supplies' negative terminal as shown in Figure 5b. Note that the SENSE$^–$ pins operate at a voltage more negative than the device ground. It is highly recommended that the SENSE$^+$ pins be operating at as close to device ground potential as possible so that at full-scale the SENSE$^–$ pins are limited to 80mV below device ground for accurate measurements. A recommended layout for Figure 5b's SENSE pins connection is shown in Figure 5c. Layout the common connection



(5b) Derives Power from the Supply Monitored in a Low Side Current Sense Topology



(5c) Recommended Layout for Figure 5b's SENSE Pins Connection

(V_{OUT}) close to the SENSE$^+$ terminal of the sense resistors with a wide track to prevent excessive potential difference between the SENSE$^+$ pins when load current is supplied entirely by V_{IN1} or V_{IN2}.

Supply Undervoltage Lockout

During power-up, the internal I^{2}C logic and the ADCs are enabled when either V_{DD} or $INTV_{CC}$ rises above its under-voltage lockout threshold (2.7V for V_{DD} and 2.5V for $INTV_{CC}$ typically). During power-down, the ADCs are disabled when V_{DD} and $INTV_{CC}$ fall below their respective

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undervoltage lockout thresholds. If V_{DD} or $INTV_{CC}$ remains above their typical 2.1V I^2C reset threshold, the internal I^2C logic retains the state before power-down. If V_{DD} or $INTV_{CC}$ is then increased as in a normal power-up, the ADCs will run according to CTRLA register's setting at that point in time. The internal I^2C logic is reset when V_{DD} and $INTV_{CC}$ fall below their respective I^2C reset thresholds.

Shutdown Mode

The LTC2992 includes a low quiescent current shutdown mode, controlled by bits CTRLA[6:5] in the CTRLA register (Table 1). Setting CTRLA[6:5]=11 puts the part in shutdown mode, powering down the ADC, internal reference and on-board linear regulator. The internal I^2C bus remains active, and although the ADR1 and ADR0 pins are disabled, the device will retain the most recently programmed I^2C bus address. All onboard registers retain their contents and can be accessed through the I^2C interface. To re-enable ADC conversions, reset bit CTRLA[6:5] in the CTRLA register. The analog circuitry will power up and all registers will retain their contents.

The onboard linear regulator is disabled in shutdown mode to conserve power. If the onboard linear regulator is used to power external I^2C bus related circuitry such as opto-couplers or pull-ups, I^2C communication will be lost when the part is shut down. The LTC2992 would then have to be reset by cycling its power to come out of shutdown. If low I_Q mode is not required, ensure 11 cannot be written to CTRLA[6:5] in the CTRLA register during software development. It is recommended that external regulators be used in such applications if powering down the LTC2992 is desirable. As an added layer of protection against this scenario, bit CTRLB[4] in the CTRLB register can be set during system configuration to enable the LTC2992 to automatically exit shutdown mode when the I^2C lines are low for more than 33ms (which can be a result of accidental shutdown of the LTC2992's linear regulator powering the I^2C). The user can elect to be alerted of this event by setting bit AL4[4] in the ALERT4 register (Table 15). Quiescent current drops below 50µA in shutdown mode with the internal regulator disabled.

Configuring the GPIO Pins

The LTC2992 has four GPIO pins configurable through the GPIO IO CONTROL register (Table 18) to be used as general purpose input/output pins. By configuring the CTRLA register, the voltage at the four GPIO pins can be measured by the VADC. GPIO1 through GPIO4 have comparators monitoring the voltage on these pins with a threshold of 1.23V typically, the results of which may be read from bits GS[3:0] in the GPIO STATUS register, as shown in Table 17. An alert may be generated, when GPIO1, GPIO2 or GPIO3 cross the comparator threshold voltage (1.23V typical), by setting bits AL4[3:1], respectively, in the ALERT4 register.

GPIO1, GPIO2, GPIO3 and GPIO4 can be pulled low as general purpose outputs, which are otherwise high impedance. GPIO3 can also be used as a data ready output ($\overline{\text{DATAREADY}}$) to indicate new data from any of the three ADCs by configuring GIO[5:4] in the GPIO IO CONTROL register. The output can be in the form of a low pulse with duration of 16µs or 128µs or a latched low state. The ADC STATUS register (Table 10) indicates which of the monitored voltages has been recently updated. This register is cleared-on-read, which will also release the GPIO3 from its latched low state.

GPIO4 is by default an SMBus alert ($\overline{\text{ALERT}}$) output that pulls low when an alert event is present. To pull GPIO4 ($\overline{\text{ALERT}}$) low in the absence of an alert event, set GC[7] of the GPIO4 CONTROL register (Table 19). Clearing this bit will release the GPIO4 ($\overline{\text{ALERT}}$). GC[7] is set whenever an alert event occurs. Setting GC[6] will similarly pull GPIO4 low.

I^2C Reset

To avoid the need of power-cycling the part for a reset, LTC2992 features a software reset which is enabled by setting CTRLB[0] of CTRLB register (Table 6). This bit is self-cleared. All internal registers except the present value data registers are reset to their default states. The ADCs will sample continuously after reset without any reconfiguration since this is the default behavior.

Storing Minimum and Maximum Values

The LTC2992 compares each measurement including the calculated power with the stored values in the respective MIN and MAX registers for each parameter (Table 4). If the new conversion is beyond the stored minimum or maximum values, the MIN or MAX registers are updated with the new values. The MIN and MAX registers are refreshed only when ADCs update the internal registers. Writing via I^2C to the ADC registers does not affect the MIN and MAX registers. To initiate a new peak hold cycle for all measurements, set CTRLB[3] of CTRLB register (Table 6). This bit is self-cleared. For new peak hold cycle of selective measurement, write all 1's to its MIN register and all 0's to its MAX register via the I^2C bus. These registers will be updated when the next respective ADC conversion is done.

The LTC2992 also includes MIN and MAX threshold registers (Table 4) for the measured parameters including the calculated power. At power-up or reset by I^2C command, the MAX threshold registers are set to all 1's, and MIN threshold registers are set to all 0's, effectively disabling them. The MIN and MAX threshold registers can be reprogrammed to any desired value via the I^2C bus.

Fault Alert and Resetting Faults

As soon as a measured quantity falls below the minimum threshold or exceeds the maximum threshold, the LTC2992 sets the corresponding flag in the FAULT1 (Table 8), FAULT2 (Table 12) and FAULT3 registers (Table 14). Other events such as GPIO state change have their present status in the GPIO STATUS (Table 17) register and any fault is latched in the FAULT4 (Table 16) register. The GPIO4 pin is pulled low if the appropriate bit in the ALERT1 (Table 7), ALERT2 (Table 11), ALERT3 (Table 13) and ALERT4 (Table 15) registers is set when the fault occurs. More details on the alert behavior can be found in the Alert Response Protocol section.

An active fault indication can be reset by writing zeros to the corresponding FAULT register bits or setting bit CTRLB[5] in the CTRLB register. If bit CTRLB[5] is set, reading the fault register will cause the corresponding register to reset. All FAULT register bits are also cleared if the V_{DD} and $INTV_{CC}$ fall below their respective I^2C logic reset threshold.

ADC Resolution and Conversion Rate

The resolution of the ADCs can be configured to 8-bit by setting bit NADC[7] of NADC register (Table 9) through an I^2C write command to speed up ADC conversions.

Table 2. ADC Resolution and Conversion Rate

RESOLUTION		12-BIT	8-BIT
NADC[7]		0	1
Conversion Time	SENSE⁺, GPIO	16.4ms	1.02ms
	ΔSENSE*	65.6ms	4.1ms
LSB Step Size	SENSE⁺	25mV	400mV
	GPIO	0.5mV	8mV
	ΔSENSE	12.5µV	200µV

*Snapshot mode

If the resolution is changed while an ADC conversion is in progress, that conversion will be aborted. In continuous scan mode, a new conversion of the same quantity will be started with the new resolution and continues in the original sequence. Otherwise, a new snapshot of one, two or multiple quantities (single cycle) will take place. Resetting the peak hold registers by setting CTRLB[3] in the CTRLB register via I^2C bus prior to changing the ADC resolution is recommended to ensure integrity of the peak hold values.

The data format in 8-bit mode for voltage/current is left justified by four bits and power is left justified by eight bits with respect to the 12-bit's format as shown in Figure 6.

POWER REGISTER VALUE						
MODE	BIT					
	23:20	19:16	15:12	11:8	7:4	3:0
12-bit	Data	Data	Data	Data	Data	Data
8-bit	Data	Data	Data	Data	0x0	0x0

VOLTAGE/CURRENT REGISTER VALUE				
MODE	BIT			
	15:12	11:8	7:4	3:0
12-bit	Data	Data	Data	0x0
8-bit	Data	Data	0x0	0x0

Figure 6. Data Format in 12-Bit and 8-Bit Mode

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ADC Status and Data Ready Signal

ADC STATUS register (Table 10) indicates availability of new measurement results in the internal registers and is reset after it is read via I^2C bus. Details on configuring GPIO3 as $\overline{\text{DATAREADY}}$ can be found in Configuring the GPIO Pins section. To illustrate the behavior of $\overline{\text{DATAREADY}}$ as new data becomes available, an example in which the ADCs are continuously converting is shown in Figure 7. GPIO3 is initially configured to output a 16µs low pulse with new data as is seen at t_4 and t_5. As S1 and S2 data are updated together with I1 and I2 at t_5, no GPIO3 pulse is seen at t_2 and t_3. GPIO3 is then reconfigured to latch low with new data—this happens at t_6. GPIO3 is released from its latched state when an I^2C read command to ADC STATUS register is done.

Crosstalk Mitigation

The GPIO pins are general purpose pins that can be used to monitor digital or analog signals. Even with an averaging architecture of the ΔΣ ADCs, crosstalk may still be problematic if an application requires monitoring of precision analog signals and noisy digital signals with the GPIO pins.

To preserve measurement accuracy of the analog signals, a few measures can be taken:

1. Physically separate the clean and noisy signals. For example, the clean signal may be monitored with GPIO1/3 while the noisy signal is monitored with GPIO2/4 on the other side of the part.
2. If adjacent GPIO pins have to be used, then decouple the analog signal to device ground near the GPIO pin with an external capacitor. Typically, a capacitance of 0.1µF should suffice.
3. Shield the sensitive signal with ground.
4. In a multi-layer PCB, the sensitive signal should be routed mostly sandwiched between two ground layers and exit next to the part for connection to the pin.

A layout example is given in Layout Considerations section for two-layered board design.

I^2C Interface

The LTC2992 includes an I^2C/SMBus-compatible interface to provide access to the onboard registers. Figure 8 shows a general data transfer format using the I^2C bus.

The LTC2992 is a read/write slave device and supports the SMBus read byte, write byte, read word and write word protocols. The LTC2992 also supports extended read and write commands that allow reading or writing more than two bytes of data. When using the read/write word or extended read and write commands, the bus master issues an initial register address and the internal register address pointer automatically increments by 1 after each byte of data is read or written. After the register address reaches 0x97, it will roll over to 0x00 and continue incrementing. A STOP condition resets the register address pointer to 0x00. The data formats for the above commands are shown in Figure 8 through Figure 14. Note that only

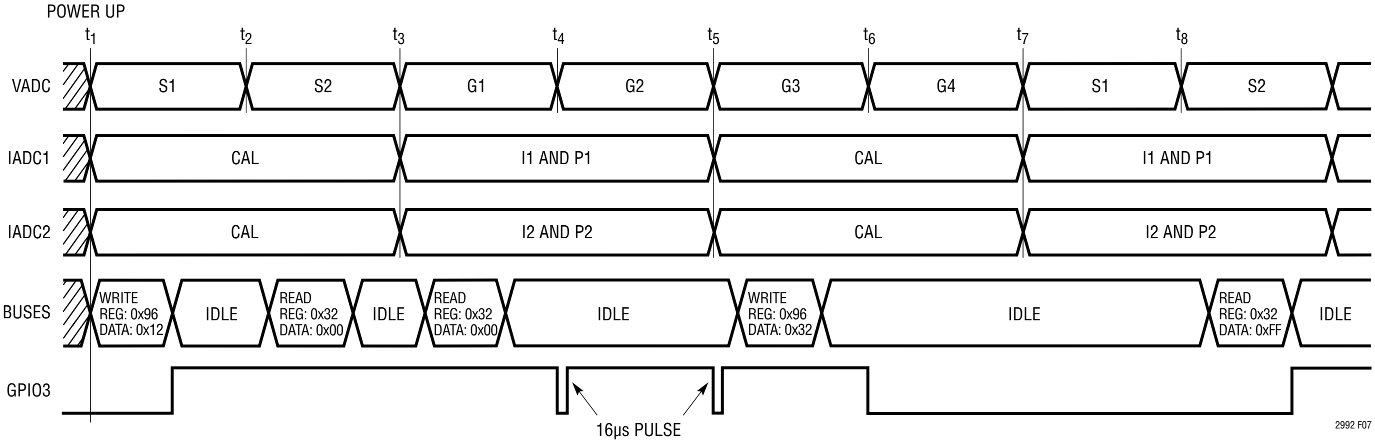

Figure 7. Configuring GPIO3 as $\overline{\text{DATAREADY}}$

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the read byte command is available to the 0xE7 and 0xE8 (MFR_SPECIAL_ID) registers (Table 4).

I^{2}C Device Addressing

Nine distinct I^{2}C bus addresses are configurable using the three-state pins ADR0 and ADR1, as shown in Table 3. ADR0 and ADR1 should be tied to INTV$_{CC}$, to GND, or left floating (NC) to configure the lower four address bits. During low power shutdown, the address select state is latched into memory powered from standby supply. Address bits a6, a5 and a4 are permanently set to 110 and the least significant bit is the R/$\overline{W}$ bit. In addition, all LTC2992 devices will respond to a common mass write address (1100110)b; this allows the bus master to write to several LTC2992s simultaneously, regardless of their individual address settings. The LTC2992 will also respond to the standard SMBus ARA address (0001100)b if the GPIO4 ($\overline{ALERT}$) pin is asserted. See the Alert Response Protocol section for more details. The LTC2992 will not respond to the ARA address if no alerts are pending.

Start and Stop Conditions

When the I^{2}C bus is idle, both SCL and SDA are in the high state. A bus master signals the beginning of a transmission with a START condition by transitioning SDA from high to low while SCL stays high. When the master has finished communicating with the slave, it issues a STOP

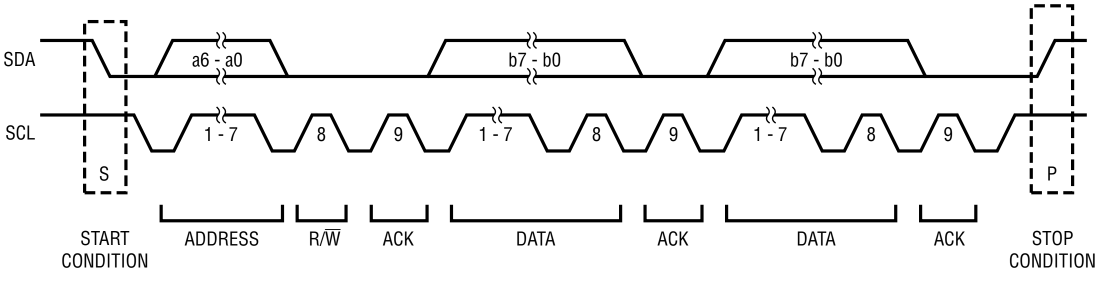

Figure 8. General Data Transfer Over I^{2}C

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	P
	1 1 0 a3:a0	0	0	b7:b0	0	b7:b0	0	

2992 F09

☐ FROM MASTER TO SLAVE
▨ FROM SLAVE TO MASTER

A: ACKNOWLEDGE (LOW)
$\overline{A}$: NOT ACKNOWLEDGE (HIGH)
R: READ BIT (HIGH)

$\overline{W}$: WRITE BIT (LOW)
S: START CONDITION
P: STOP CONDITION

Figure 9. Serial Bus SDA Write Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	DATA	A	P
	1 1 0 a3:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0	

2992 F10

Figure 10. Serial Bus SDA Write Word Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	DATA	A	DATA	A	...	DATA	A	P
	1 1 0 a3:a0	0	0	b7:b0	0	b7:b0	0	b7:b0	0	...	b7:b0	0	

2992 F11

Figure 11. Serial Bus SDA Write Page Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	$\overline{A}$	P
	1 1 0 a3:a0	0	0	b7:b0	0		1 1 0 a3:a0	1	0	b7:b0	1	

2992 F12

Figure 12. Serial Bus SDA Read Byte Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	$\overline{A}$	P
	1 1 0 a3:a0	0	0	b7:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	1	

2992 F13

Figure 13. Serial Bus SDA Read Word Protocol

S	ADDRESS	$\overline{W}$	A	COMMAND	A	S	ADDRESS	R	A	DATA	A	DATA	...	DATA	$\overline{A}$	P
	1 1 0 a3:a0	0	0	b7:b0	0		1 1 0 a3:a0	1	0	b7:b0	0	b7:b0	...	b7:b0	1	

2992 F14

Figure 14. Serial Bus SDA Read Page Protocol

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condition by transitioning SDA from low to high while SCL stays high. The bus is then free for another transmission.

Stuck-Bus Reset

The LTC2992 I^2C interface features a stuck-bus reset timer to prevent it from holding the bus lines low indefinitely if the SCL signal is interrupted during a transfer. The timer starts when either SCL or SDAI is low, and resets when both SCL and SDAI are pulled high. If either SCL or SDAI are low for over 33ms, the stuck-bus timer will expire, and the internal I^2C interface and the SDAO pin pull-down logic will be reset to release the bus. Normal communication will resume at the next START command.

Acknowledge

The acknowledge signal is used for handshaking between the master and the slave to indicate that the last byte of data was received. The master always releases the SDA line during the acknowledge clock pulse. The LTC2992 will pull the SDA line low on the 9th clock cycle to acknowledge receipt of the data. If the slave fails to acknowledge by leaving SDA high, then the master can abort the transmission by generating a STOP condition. When the master is receiving data from the slave, the master must acknowledge the slave by pulling down the SDA line during the 9th clock pulse to indicate receipt of a data byte. After the last byte has been received by the master, it will leave the SDA line high (not acknowledge) and issue a STOP condition to terminate the transmission.

Write Protocol

The master begins a write operation with a START condition followed by the 7-bit slave address and the $R/\overline{W}$ bit set to zero. After the addressed LTC2992 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to write. The LTC2992 acknowledges this and then latches the command byte into its internal register address pointer. The master then delivers the data byte and the LTC2992 acknowledges once more and writes the data into the internal register pointed to by the register address pointer. If the master continues sending additional data bytes with a write word or extended write command, the additional data bytes will be acknowledged by the LTC2992, the register address pointer will automatically increment by one, and data will be written as previously stated. The write operation terminates and the register address pointer resets to 0x00 when the master sends a STOP condition.

Read Protocol

The master begins a read operation with a START condition followed by the 7-bit slave address and the $R/\overline{W}$ bit set to zero. After the addressed LTC2992 acknowledges the address byte, the master then sends a command byte that indicates which internal register the master wishes to read. The LTC2992 acknowledges this and then latches the command byte into its internal register address pointer. The master then sends a repeated START condition followed by the same 7-bit address with the $R/\overline{W}$ bit now set to 1. The LTC2992 acknowledges and sends the contents of the requested register. The transmission terminates when the master sends a STOP condition. If the master acknowledges the transmitted data byte, as in a read word command, the LTC2992 will send the contents of the next register. If the master keeps acknowledging, the LTC2992 will keep incrementing the register address pointer and sending out data bytes. The read operation terminates and the register address pointer resets to 0x00 when the master sends a STOP condition.

Alert Response Protocol

When any of the fault bits in the fault registers (FAULT1, FAULT2, FAULT3 and FAULT4) are set, a bus alert is generated if the appropriate bit in the ALERT1, ALERT2, ALERT3 or ALERT4 registers has been set. This allows the bus master to select which faults will generate alerts. At power-up, all ALERT registers are cleared (no alerts enabled) and the GPIO4 ($\overline{\text{ALERT}}$) pin is high. If an alert is enabled, the corresponding fault causes the GPIO4 ($\overline{\text{ALERT}}$) pin to pull low. The bus master responds to the alert in accordance with the SMBus alert response protocol by broadcasting the alert response address (0001100)b, and the LTC2992 replies with its own address and releases its GPIO4 ($\overline{\text{ALERT}}$) pin, as shown in Figure 15. The GPIO4 ($\overline{\text{ALERT}}$) line is also released if CTRLB[7] is set and the LTC2992 is addressed (see Table 6) by any message. The GPIO4 ($\overline{\text{ALERT}}$) signal

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is not pulled low again until the fault registers indicate a different fault has occurred or the original fault is cleared and it occurs again. Note that this means repeated or continuing faults will not generate additional alerts until the associated fault register bits have been cleared.

S	ALERT RESPONSE ADDRESS	R	A	DEVICE ADDRESS	$\overline{A}$	P
	0 0 0 1 1 0 0	1	0	a7:a0	1	

2992 F15

Figure 15. Serial Bus SDA Alert Response Protocol

If two or more LTC2992s on the same bus are generating alerts when the ARA is broadcast, the bus master will repeat the alert response protocol until the GPIO4 ($\overline{\text{ALERT}}$) line is released. Standard I^2C arbitration causes the device with the highest priority (lowest address) to reply first and the device with the lowest priority (highest address) to reply last.

Opto-Isolating the I^2C Bus

Opto-isolating a standard I^2C device is complicated by the bidirectional SDA pin. The LTC2992/LTC2992-1 minimize this problem by splitting the standard I^2C SDA line into SDAI (input) and SDAO (output, LTC2992) or $\overline{\text{SDAO}}$ (inverted output, LTC2992-1). The SCL is an input-only pin and does not require special circuitry to isolate. For conventional nonisolated I^2C applications, use the LTC2992 and tie the SDAI and SDAO pins together to form a standard I^2C SDA pin. Low speed isolated interfaces that use standard open-drain opto-isolators can use the LTC2992 with the SDAI and SDAO pins separated, as shown in Figure 16. Connect SDAI to the output of the incoming opto-isolator with a pull-up resistor to $INTV_{CC}$ or a local 5V supply; connect SDAO to the cathode of the outgoing opto-isolator with a current-limiting resistor in series with the anode. The input and output must be connected together on the isolated side of the bus to allow the LTC2992 to participate in I^2C arbitration. Note that maximum I^2C bus speed will generally be limited by the speed of the opto-couplers used in this application.

Figure 17 shows an alternate connection for use with low speed opto-couplers and the LTC2992-1. This circuit uses a limited-current pull-up on the internally clamped SDAI pin and clamps the $\overline{\text{SDAO}}$ pin with the input diode of the outgoing opto-isolator, removing the need to use $INTV_{CC}$ for biasing in the absence of a separate low voltage supply. For proper clamping:

$$\frac{V_{IN(MAX)} - V_{SDA,SCL(MIN)}}{I_{SDA,SCL(MAX)}} \le R4 \le \frac{V_{IN(MIN)} - V_{SDA,SCL(MAX)}}{I_{SDA,SCL(MIN)}} \qquad (1)$$

$$\frac{V_{IN(MAX)} - 5.9V}{5mA} \le R4 \le \frac{V_{IN(MIN)} - 6.9V}{0.5mA}$$

As an example, a supply that operates from 36V to 72V would require the value of R4 to be between 13k and 58k. The LTC2992-1 must be used in this application to ensure that $\overline{\text{SDAO}}$ signal polarity is correct. R4 may

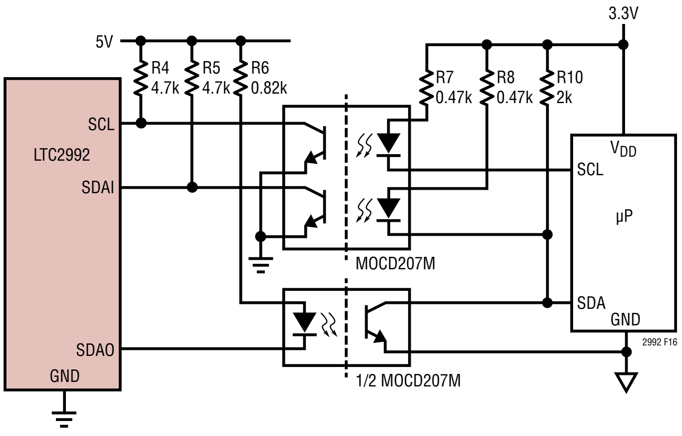

Figure 16. Opto-Isolation of a 10kHz I^2C Interface Between LTC2992 and Microcontroller

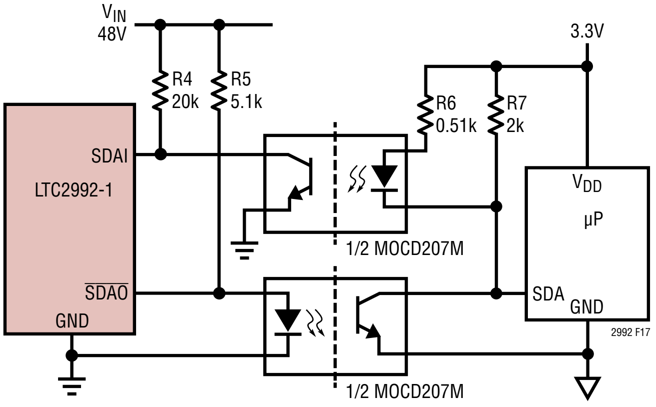

Figure 17. Opto-Isolation of a 1.5kHz I^2C Interface Between LTC2992-1 and Microcontroller (SCL Omitted for Clarity)

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be split into two or more series connected units to meet thermal requirements.

The LTC2992 can also be used with high speed optocouplers with push-pull outputs and inverted logic as shown in Figure 18. The incoming opto-isolator draws power from INTV$_{CC}$, and the data output is connected directly to the SDAI pin with no pull-up required. Ensure current drawn does not exceed the 10mA maximum capability of the INTV$_{CC}$ pin. The SDAO pin is connected to the cathode of the outgoing opto-coupler with a current limiting resistor connected back to INTV$_{CC}$. An additional discrete diode is required at the output of the outgoing opto-coupler to provide the open-drain pull-down that the I^{2}C requires. Finally, the input of the incoming opto-isolator is connected back to the output as in the low speed case.

Layout Considerations

A Kelvin connection between the sense resistor R$_{SNS}$ and the LTC2992 is recommended to achieve accurate current sensing (Figure 19). The recommended minimum trace width for 1oz copper foil is 0.02″ per amp to ensure the trace stays at a reasonable temperature. Using 0.03″ per amp or wider is preferred. Note that 1oz copper exhibits a sheet resistance of about 530µΩ per square. In very high current applications where the sense resistor can dissipate significant power, the PCB layout should include good thermal management techniques such as extra vias and wide metal area. 2oz or thicker copper should be considered for such applications. The trace from sense resistors to SENSE$^+$ pins should be as short as possible to minimize IR drop due to pin current.

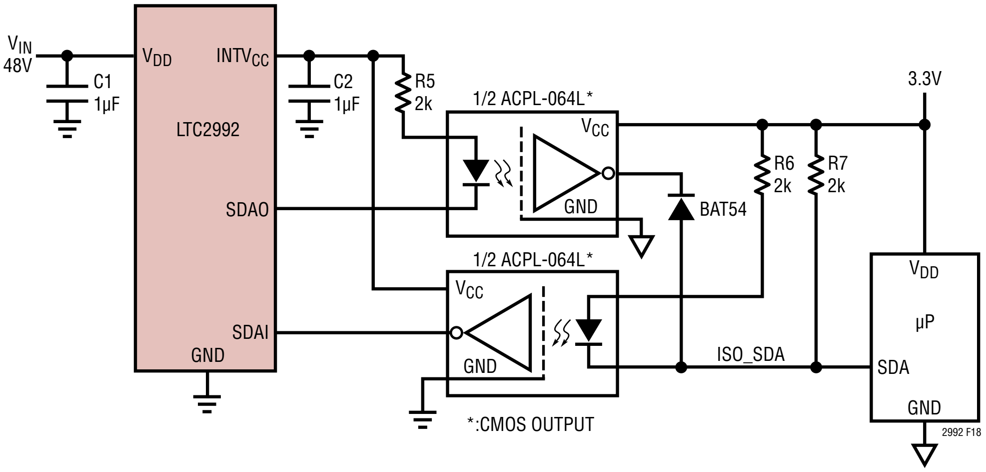

Figure 18. Opto-Isolation of a I^{2}C Interface with Low Power, High Speed Opto-Couplers (SCL Omitted for Clarity)

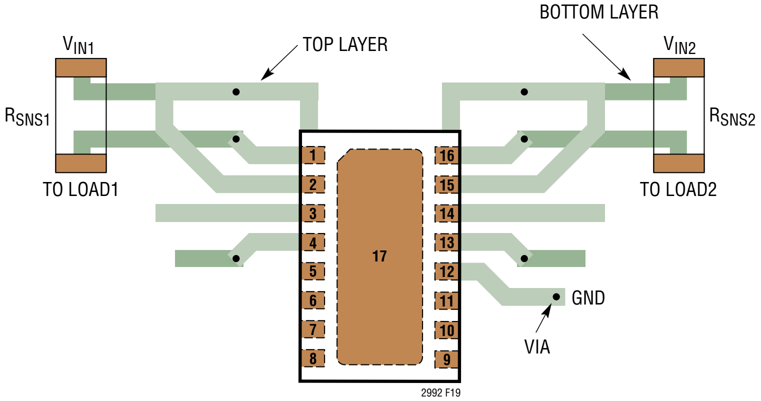

Figure 19. Recommended PCB Layout

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Design Example

As a design example, consider a –36V to –72V Advanced TCA system with I^2C current, voltage and power monitors (See Figure 20).

The load current is either supplied by V_{IN1} or V_{IN2} or both depending on their voltages. Choose similar values for R_{SENSE1} and R_{SENSE2} in accordance to the following equation:

$$R_{SENSE1,2} < \frac{V_{FS(\Delta SENSE1,2)}}{I_{LOAD(MAX)}}$$

$$R_{SENSE1,2} < \frac{51.2\text{mV}}{5\text{A}} = 10.24\text{m}\Omega$$

R_{SENSE1} and R_{SENSE2} are chosen to be 10mΩ.

$$\text{Current of } V_{IN1} \text{ or } V_{IN2} = \frac{12.5\mu\text{V}}{R_{SENSE}} = 1.25\text{mA/LSB}$$

$$\text{Total Current} = 2.5\text{mA/LSB}$$

We also have to consider the power dissipated in the sense resistors which can be calculated with the following equation:

$$P = (I_{LOAD})^2 \bullet R_{SENSE}$$

$$P = (5\text{A})^2 \bullet 10\text{m}\Omega = 0.25\text{W}$$

Use at least 0.5W rated sense resistors to ensure thermal compliance.

Next, select the resistive dividers that measure the supply voltages V_{IN1} and V_{IN2}. Note that the voltage drop across the N-channel MOSFET and sense resistor is not included in the derivation for the following equations.

$$\frac{R12}{R10+R12} < \frac{V_{FS(GPIO2)}}{V_{IN2}}, \frac{R13}{R11+R13} < \frac{V_{FS(GPIO1)}}{V_{IN1}}$$

$$\frac{R12}{R10+R12} < \frac{2.048\text{V}}{72\text{V}} = 0.028$$

$$\frac{R13}{R11+R13} < \frac{2.048\text{V}}{72\text{V}} = 0.028$$

Choose R10,11 = 1MΩ, and R12,13 = 20kΩ to allow a input voltage measurement range from 0V to 104.4V.

$$\text{Voltage of } V_{IN1} = \frac{R11+R13}{R13} \bullet V_{GPIO1} = \frac{25.5\text{mV}}{\text{LSB}}$$

$$\text{Voltage of } V_{IN2} = \frac{R10+R12}{R12} \bullet V_{GPIO2} = \frac{25.5\text{mV}}{\text{LSB}}$$

An error term can be added to the voltage results above to account for the voltage drop across the N-channel MOSFET and sense resistor:

$$V_{ERROR} = \Delta V_{DS} \text{ of FDS3672} + \Delta SENSE$$

The maximum error occurs when the load current is at its maximum of 5A. Using the above equation, this works out to be 160mV with 110mV contribution (see below for calculation) from the FDS3672. Without compensation, this would cause measurement error of 0.45% for V_{IN} = 36V.

LTC4354 and LTC4355 low side and high side ideal diode-OR controllers drive N-channel MOSFETs to minimize the diode power consumption. The 100V, N-channel MOSFET FDS3672 in the SO-8 package with $R_{DS(ON)}$ = 22mΩ (max) is chosen as switches. The maximum voltage drop across it is:

$$\Delta V_{DS} = 5\text{A} \times 22\text{m}\Omega = 110\text{mV}$$

Since external resistive dividers are used for supply voltage measurement, CTRLA register 0x00 is set to 0x10 to continuously monitor GPIO1 and GPIO2.

$$\text{POWER1} = V_{IN1} \bullet \text{Current of } V_{IN1}$$

$$\text{POWER1} = 25.5\text{mV} \bullet 1.25\text{mA/LSB} = 31.875\mu\text{W/LSB}$$

$$\text{POWER2} = 31.875\mu\text{W/LSB}$$

$$\text{Total Power} = 63.75\mu\text{W/LSB}$$

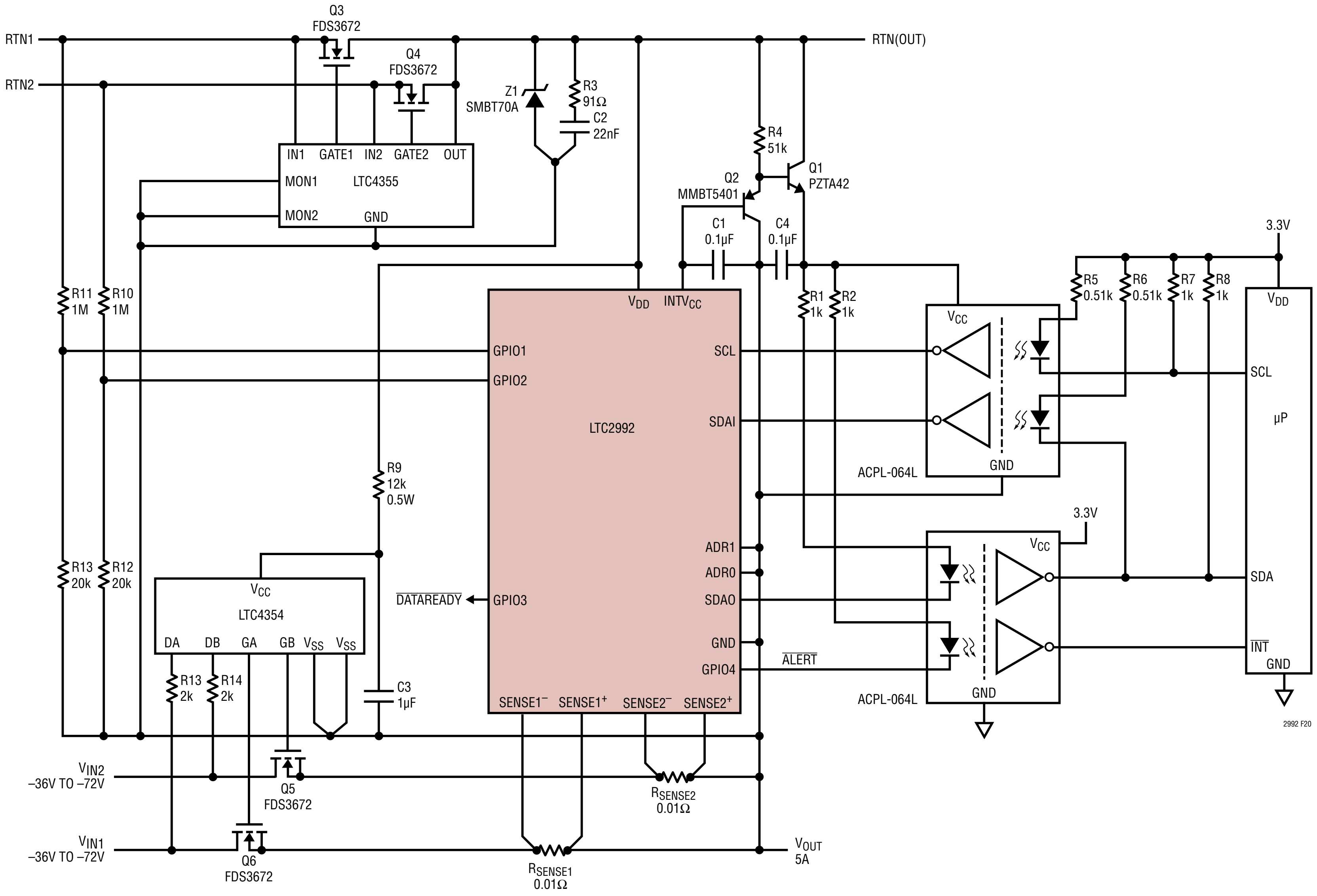

Figure 20. Design Example: Advanced TCA System with I^2C Current, Voltage and Power Monitors