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Nanopower Buck-Boost DC/DC with Energy Harvesting Battery Life Extender

FEATURES

- **Dual Input, Single Output DC/DCs with Input Prioritizer**
  - **Energy Harvesting Input: 3.0V to 19V Buck DC/DC**
  - **Primary Cell Input: 1.8V to 5.5V Buck-Boost DC/DC**
- **Zero Battery I_Q When Energy Harvesting Source is Available**
- **Ultralow Quiescent Current: 750nA at No-Load**
- **Low Noise LDO Post Regulator**
- Integrated Supercapacitor Balancer
- Up to 50mA of Output Current
- Programmable DC/DC and LDO Output Voltages, Buck UVLO, and Buck-Boost Peak Input Current
- Integrated Low Loss Full-Wave Bridge Rectifier
- Input Protective Shunt: Up to 25mA at $V_{IN} \geq 20V$
- 5mm × 5mm QFN-32 Package

APPLICATIONS

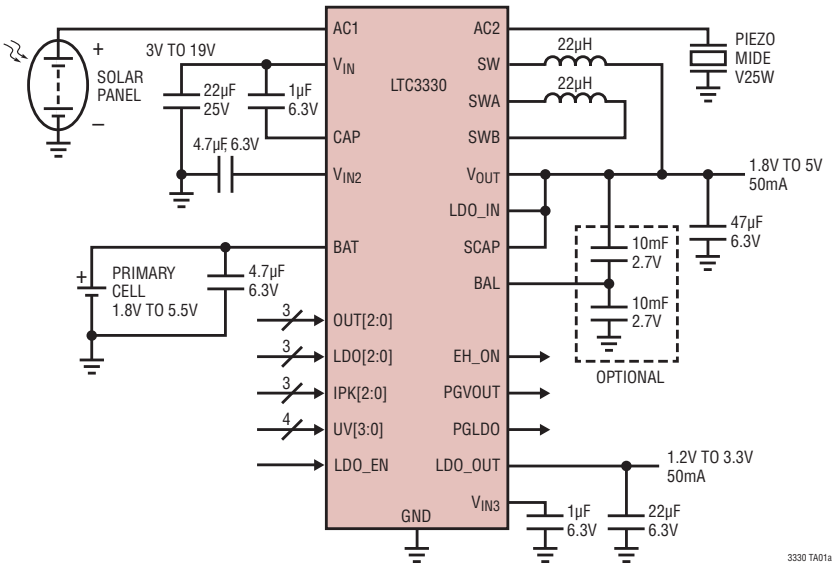
- Energy Harvesting
- Solar Powered Systems with Primary Cell Backup
- Wireless HVAC Sensors and Security Devices
- Mobile Asset Tracking

DESCRIPTION

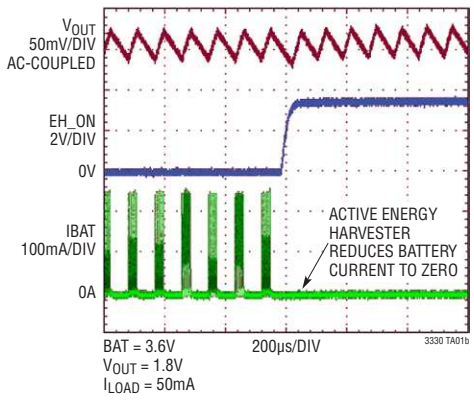
The LTC®3330 integrates a high voltage energy harvesting power supply plus a DC/DC converter powered by a primary cell battery to create a single output supply for alternative energy applications. The energy harvesting power supply, consisting of an integrated full-wave bridge rectifier and a high voltage buck converter, harvests energy from piezoelectric, solar, or magnetic sources. The primary cell input powers a buck-boost converter capable of operation down to 1.8V at its input. Either DC/DC converter can deliver energy to a single output. The buck operates when harvested energy is available, reducing the quiescent current draw on the battery to essentially zero, thereby extending the life of the battery. The buck-boost powers V_{OUT} only when harvested energy goes away.

A low noise LDO post regulator and a supercapacitor balancer are also integrated, accommodating a wide range of output storage configurations. Voltage and current settings for both inputs and outputs are programmable via pin-strapped logic inputs. The LTC3330 is available in a 5mm × 5mm QFN-32 package.

TYPICAL APPLICATION



Extended Battery Life with Energy Harvesting



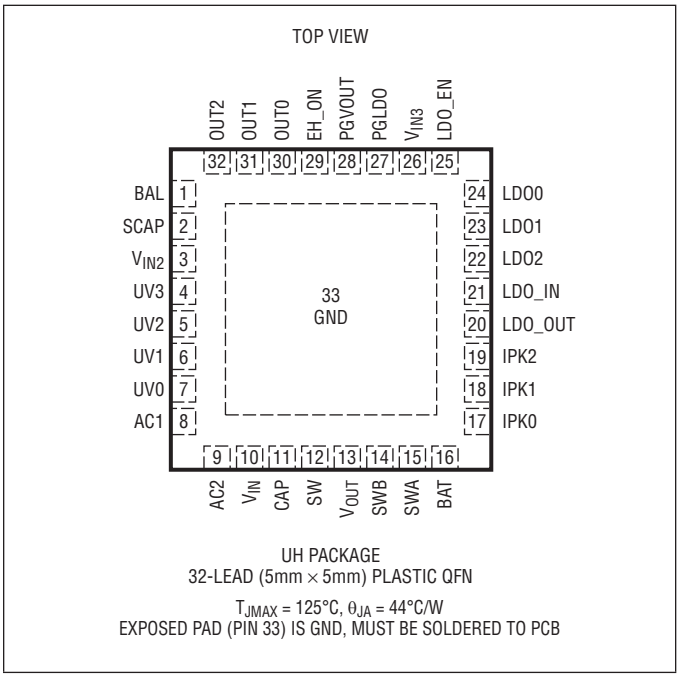
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}
Low Impedance Source .....–0.3 to 19V*
Current-Fed, I_{SW} = 0A.....25mA
AC1, AC2.....0 to V_{IN}
BAT, V_{OUT}, V_{IN3}, LDO_IN, SCAP, PGVOUT, PGLDO, LDO_EN.....–0.3 to 6V
V_{IN2}.....–0.3V to [Lesser of (V_{IN} + 0.3V) or 6V]
CAP..... [Higher of –0.3V or (V_{IN} – 6V)] to V_{IN}
LDO_OUT, LDO[2:0] .....–0.3V to LDO_IN + 0.3V
BAL .....–0.3V to SCAP + 0.3V
OUT[2:0], IPK[2:0], EH_ON .....–0.3V to [Lesser of (V_{IN3} + 0.3V) or 6V]
UV[3:0] ..... –0.3V to [Lesser of (V_{IN2} + 0.3V) or 6V]
I_{AC1}, I_{AC2} .....±50mA
I_{SW}, I_{SWA}, I_{SWB}, I_{VOUT} 350mA
I_{LDO_OUT}.....50mA
Operating Junction Temperature Range (Notes 2, 3).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

*V_{IN} has an internal 20V clamp

PIN CONFIGURATION



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 44°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3330EUH#PBF	LTC3330EUH#TRPBF	3330	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C
LTC3330IUH#PBF	LTC3330IUH#TRPBF	3330	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 5V, BAT = 3.6V, SCAP = 0V, LDO_IN = 0V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Buck Input Voltage Range		●			19	V
V_{BAT}	Buck-Boost Input Voltage Range		●	1.8		5.5	V
I_{VIN}	V_{IN} Quiescent Current						
	V_{IN} Input in UVLO	V_{IN} = 2.5V, BAT = 0V			450	700	nA
	V_{IN} Input in UVLO	V_{IN} = 16V, BAT = 0V			840	1400	nA
	Buck Enabled, Sleeping	V_{IN} = 4V, BAT = 0V			1200	1800	nA
	Buck Enabled, Sleeping	V_{IN} = 18V, BAT = 0V			1800	2500	nA
	Buck Enabled, Not Sleeping	V_{IN} = 5V, BAT = 0V, I_{SW1} = 0A (Note 4)			150	225	µA
I_{BAT}	BAT Quiescent Current						
	BAT Input with V_{IN} Active	BAT = 1.8V, V_{IN} = 5V		–10	0	10	nA
	Buck-Boost Enabled, Sleeping	BAT = 5V, V_{IN} = 0V			750	1200	nA
	Buck-Boost Enabled, Not Sleeping	BAT = 5V, V_{IN} = 0V, I_{SWA} = I_{SWB} = 0A (Note 4)			200	300	µA
I_{VOUT}	V_{OUT} Leakage Current	V_{OUT} = 5.0V, OUT[2:0] = 111, Sleeping			100	150	nA
V_{INUVLO}	V_{IN} Undervoltage Lockout Thresholds (Rising or Falling)	3V Level	●	2.91	3.00	3.09	V
		4V Level	●	3.88	4.00	4.12	V
		5V Level	●	4.85	5.00	5.15	V
		6V Level	●	5.82	6.00	6.18	V
		7V Level	●	6.79	7.00	7.21	V
		8V Level	●	7.76	8.00	8.24	V
		9V Level	●	8.73	9.00	9.27	V
		10V Level	●	9.70	10.0	10.30	V
		11V Level	●	10.67	11.0	11.33	V
		12V Level	●	11.64	12.0	12.36	V
		13V Level	●	12.61	13.0	13.39	V
		14V Level	●	13.58	14.0	14.42	V
		15V Level	●	14.55	15.0	15.45	V
		16V Level	●	15.52	16.0	16.48	V
		17V Level	●	16.49	17.0	17.51	V
		18V Level	●	17.46	18.0	18.54	V
V_{SHUNT}	V_{IN} Shunt Regulator Voltage	I_{VIN} = 1mA	●	19.0	20.0	21.0	V
I_{SHUNT}	Maximum Protective Shunt Current			25			mA
	Internal Bridge Rectifier Loss ($\lvert V_{AC1} - V_{AC2} \rvert - V_{IN}$)	I_{BRIDGE} = 10µA		700	800	900	mV
		I_{BRIDGE} = 50mA		1350	1550	1750	mV
	Internal Bridge Rectifier Reverse Leakage Current	$V_{REVERSE}$ = 18V				20	nA
	Internal Bridge Rectifier Reverse Breakdown Voltage	$I_{REVERSE}$ = 1µA		V_{SHUNT}	30		V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 5V, BAT = 3.6V, SCAP = 0V, LDO_IN = 0V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{OUT}	Regulated Buck/Buck-Boost Output Voltage	1.8V Output Selected					
		Sleep Threshold	●		1.806	1.872	V
		Wake-Up Threshold	●	1.728	1.794		V
		2.5V Output Selected					
		Sleep Threshold	●		2.508	2.575	V
		Wake-Up Threshold	●	2.425	2.492		V
		2.8V Output Selected					
		Sleep Threshold	●		2.809	2.884	V
		Wake-Up Threshold	●	2.716	2.791		V
		3.0V Output Selected					
		Sleep Threshold	●		3.010	3.090	V
		Wake-Up Threshold	●	2.910	2.990		V
		3.3V Output Selected					
		Sleep Threshold	●		3.311	3.400	V
		Wake-Up Threshold	●	3.200	3.289		V
		3.6V Output Selected					
		Sleep Threshold	●		3.612	3.708	V
		Wake-Up Threshold	●	3.492	3.588		V
		4.5V Output Selected					
		Sleep Threshold	●		4.515	4.635	V
		Wake-Up Threshold	●	4.365	4.485		V
		5.0V Output Selected					
		Sleep Threshold	●		5.017	5.150	V
		Wake-Up Threshold	●	4.850	4.983		V
	PGVOUT Falling Threshold	As a Percentage of V_{OUT} Target (Note 5)	●	88	92	96	%
I_{PEAK_BUCK}	Buck Peak Switch Current			200	250	350	mA
I_{BUCK}	Available Buck Output Current			100			mA
I_{PEAK_BB}	Buck-Boost Peak Switch Current	250mA Target Selected		200	250	350	mA
		150mA Target Selected		120	150	210	mA
		100mA Target Selected		80	100	140	mA
		50mA Target Selected		40	50	70	mA
		25mA Target Selected		20	25	35	mA
		15mA Target Selected		12	15	21	mA
		10mA Target Selected		8	10	14	mA
		5mA Target Selected		4	5	7	mA
I_{BB}	Available Buck-Boost Current	I_{PEAK_BB} = 250mA, BAT = 1.8V, V_{OUT} = 3.3V		50			mA
R_{P_BUCK}	Buck PMOS Switch On-Resistance				1.4		Ω
R_{N_BUCK}	Buck NMOS Switch On-Resistance				1.2		Ω
R_{P_BB}	Buck-Boost PMOS Input and Output Switch On-Resistance	IPK[2:0] = 111			0.7		Ω
		IPK[2:0] = 110			0.9		Ω
		IPK[2:0] = 101			1.2		Ω
		IPK[2:0] = 100			2.1		Ω
		IPK[2:0] = 011			3.9		Ω
		IPK[2:0] = 010			6.3		Ω
		IPK[2:0] = 001			9.2		Ω
		IPK[2:0] = 000			17.7		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 5V, BAT = 3.6V, SCAP = 0V, LDO_IN = 0V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
R_{N_BB}	Buck-Boost NMOS Input and Output Switch On-Resistance	IPK2 = 1 IPK2 = 0			0.6 3.8		Ω Ω
$I_{LEAK(P)}$	PMOS Switch Leakage	Buck/Buck-Boost Regulators		–20		20	nA
$I_{LEAK(N)}$	NMOS Switch Leakage	Buck/Buck-Boost Regulators		–20		20	nA
	Maximum Buck Duty Cycle	Buck/Buck-Boost Regulators	●	100			%
V_{LDO_IN}	LDO_IN Input Range		●	1.8V		5.5V	V
I_{LDO_IN}	LDO_IN Quiescent Current	LDO_IN = 5.0V, I_{LDO_OUT} = 0mA			400	600	nA
I_{LDO_OUT}	LDO_OUT Leakage Current	LDO_OUT = 3.3V, LDO[2:0] = 110			100	150	nA
LDO_OUT	Regulated LDO Output Voltage	Error as a Percentage of Target, 100µA Load	 ●	–2.0 –3.0		2.0 3.0	% %
	LDO Line Regulation (1.8V to 5.5V)	LDO_OUT = 1.2V, 10mA Load			2		mV/V
	LDO Load Regulation (10µA to 10mA)	LDO_IN = 5.0V, LDO_OUT = 3.3V			0.5		mV/mA
	LDO Dropout Voltage	LDO_OUT = 3.3V, 10mA LOAD			50		mV
R_{P_LDO}	LDO PMOS Switch On-Resistance	LDO_IN = 3.3V, I_{LDO_OUT} = 10mA			5		Ω
	LDO Current Limit	LDO_IN = 5.0V		50			mA
	PGLDO Rising Threshold	As a Percentage of the 3.3V LDO_OUT Target	●	88	92	96	%
	PGLDO Falling Threshold	As a Percentage of the 3.3V LDO_OUT Target	●	86	90	94	%
V_{SCAP}	Supercapacitor Balancer Input Range		●	2.5		5.5	V
I_{SCAP}	Supercapacitor Balancer Quiescent Current	SCAP = 5.0V			150	225	nA
I_{SOURCE}	Supercapacitor Balancer Source Current	SCAP = 5.0V, BAL = 2.4V		10			mA
I_{SINK}	Supercapacitor Balancer Sink Current	SCAP = 5.0V, BAL = 2.6V		10			mA
V_{BAL}	Supercapacitor Balance Point	Percentage of SCAP Voltage	●	49	50	51	%
V_{IH}	Digital Input High Voltage	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]	●	1.2			V
V_{IL}	Digital Input Low Voltage	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]	●			0.4	V
I_{IH}	Digital Input High Current	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]			0	10	nA
I_{IL}	Digital Input Low Current	Pins LDO_EN, OUT[2:0], LDO[2:0], IPK[2:0], UV[3:0]			0	10	nA
V_{OH}	PGVOUT, PGLDO Output High Voltage EH_ON Output High Voltage	BAT = 5V, 1µA Out of Pin V_{IN} = 6V, 1µA Out of Pin	● ●	4.0 3.8			V V
V_{OL}	PGVOUT, PGLDO, EH_ON Output Low Voltage	BAT = 5V, 1µA into Pin	●			0.4	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3330E is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3330E is guaranteed to meet specifications from 0°C to 85°C. The LTC3330I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

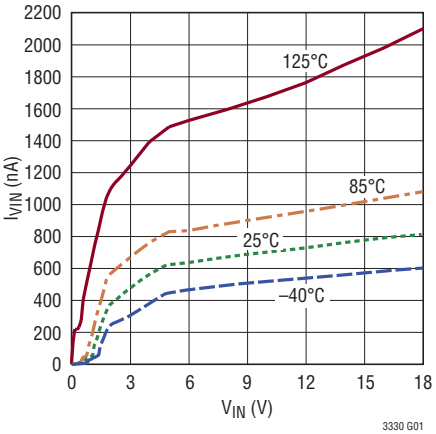
Note 3: T_J is calculated from the ambient T_A and power dissipation PD according to the following formula: $T_J = T_A + (P_D \bullet \theta_{JA})$.

Note 4: Dynamic supply current is higher due to gate charge being delivered at the switching frequency.

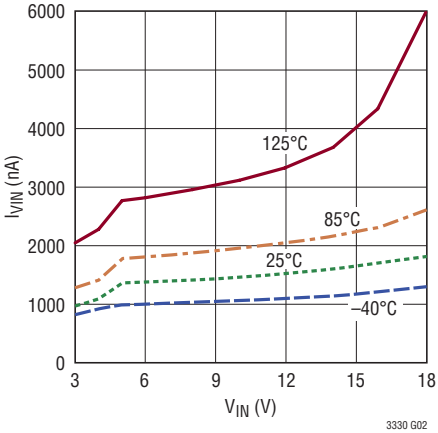
Note 5: The PGVOUT Rising threshold is equal to the sleep threshold. See V_{OUT} specification.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

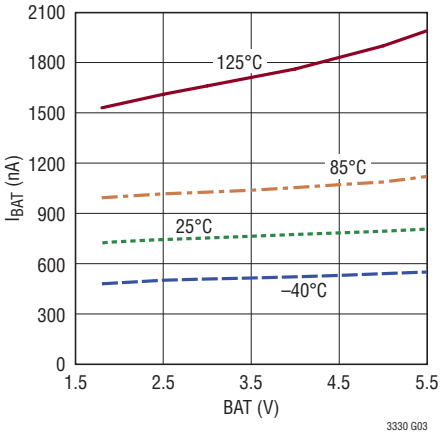
I_{VIN} in UVLO vs V_{IN}



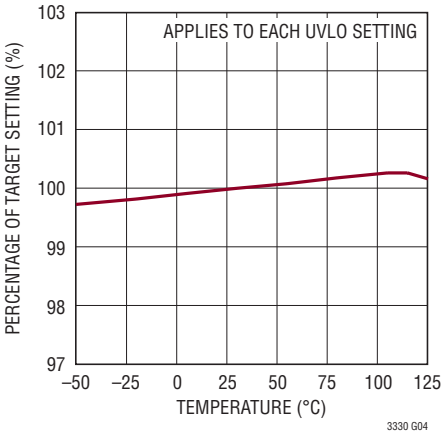
I_{VIN} in Sleep vs V_{IN}



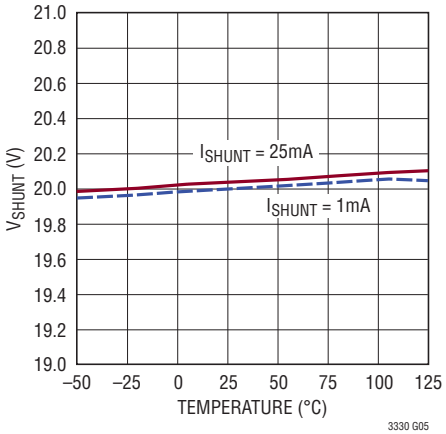
I_{BAT} in Sleep vs BAT



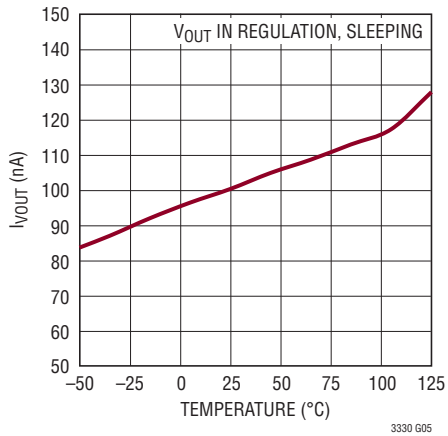
UVLO Threshold vs Temperature



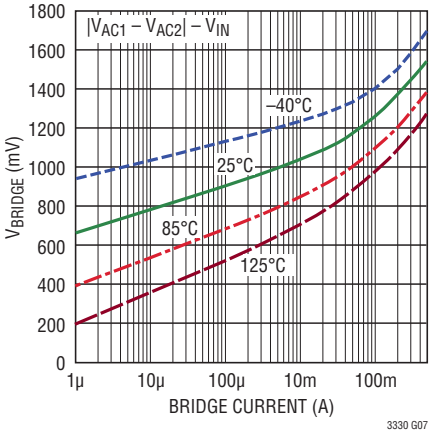
V_{SHUNT} vs Temperature



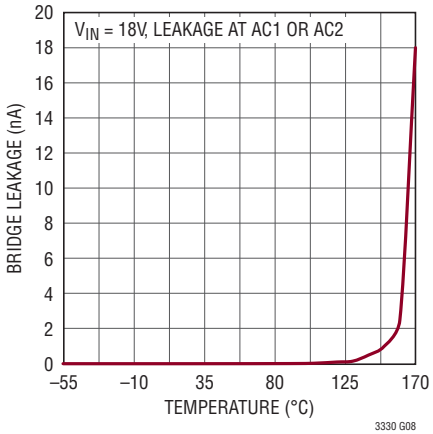
I_{VOUT} vs Temperature



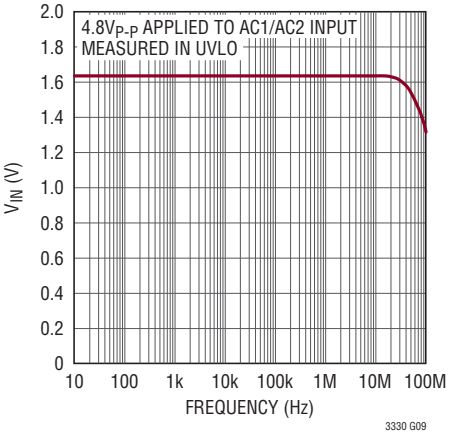
Total Bridge Rectifier Drop vs Bridge Current



Bridge Leakage vs Temperature

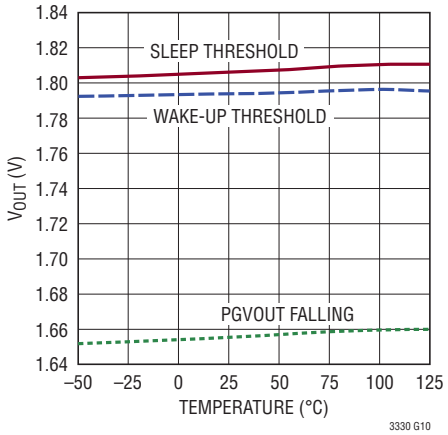


Bridge Frequency Response

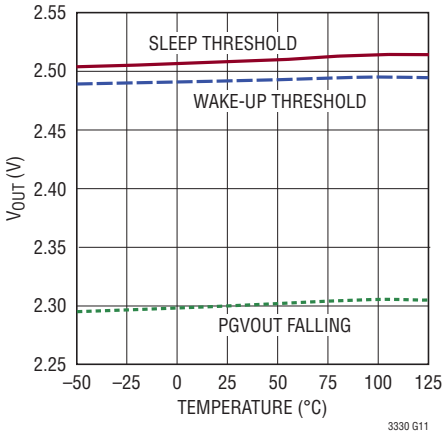


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

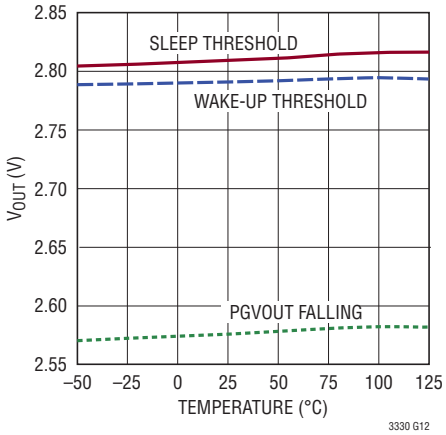
1.8V Output vs Temperature



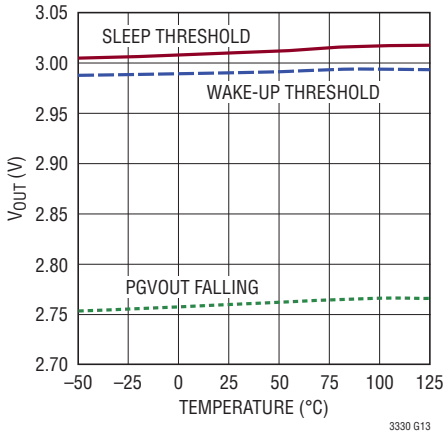
2.5V Output vs Temperature



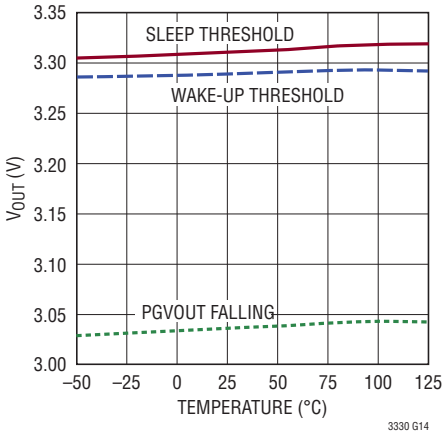
2.8V Output vs Temperature



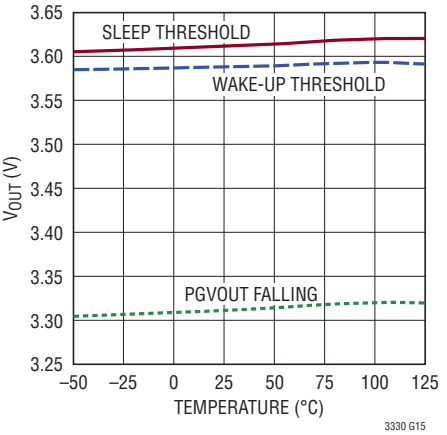
3V Output vs Temperature



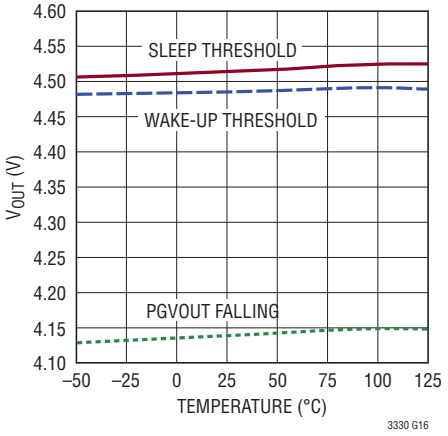
3.3V Output vs Temperature



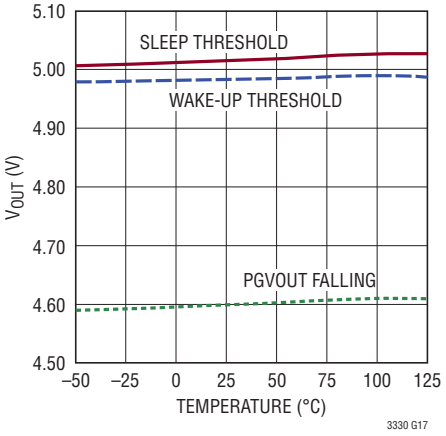
3.6V Output vs Temperature



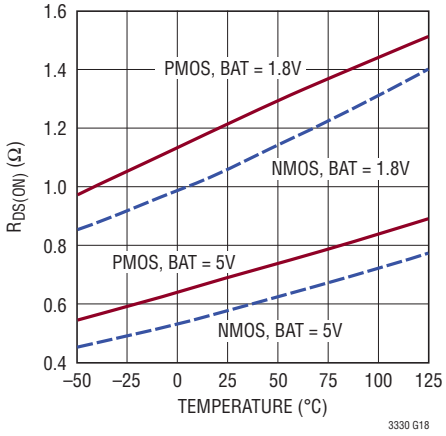
4.5V Output vs Temperature



5V Output vs Temperature

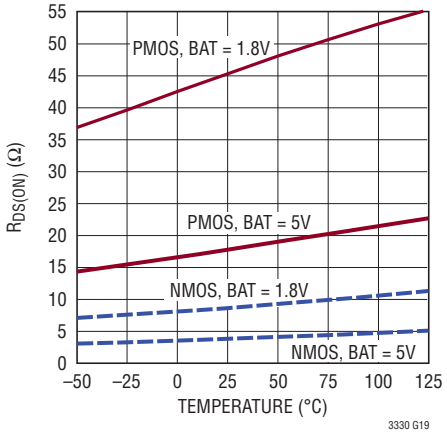


$R_{DS(ON)}$ of Buck-Boost PMOS/NMOS vs Temperature, 250mA I_{PEAK} Setting

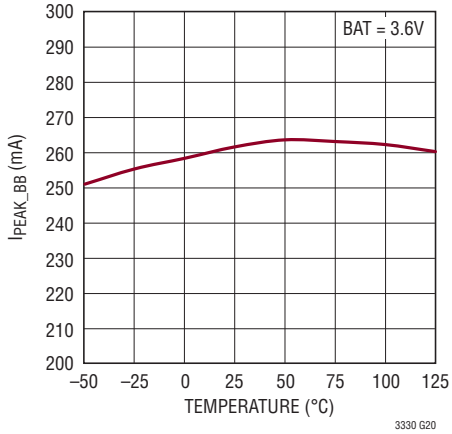


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

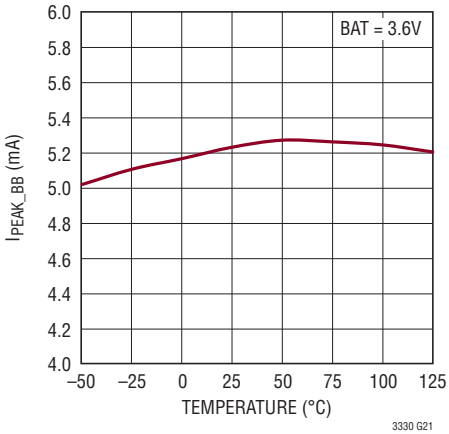
$R_{DS(ON)}$ of Buck-Boost PMOS/NMOS vs Temperature, 5mA I_{PEAK} Setting



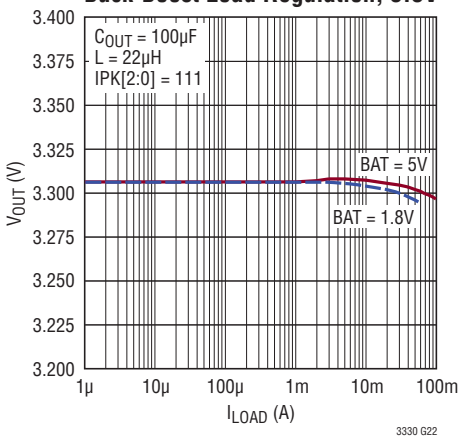
I_{PEAK_BB} vs Temperature, 250mA I_{PEAK} Setting



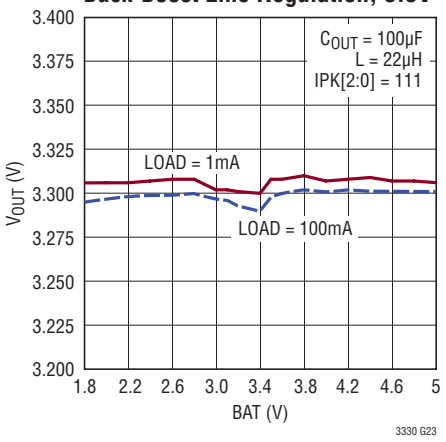
I_{PEAK_BB} vs Temperature, 5mA I_{PEAK} Setting



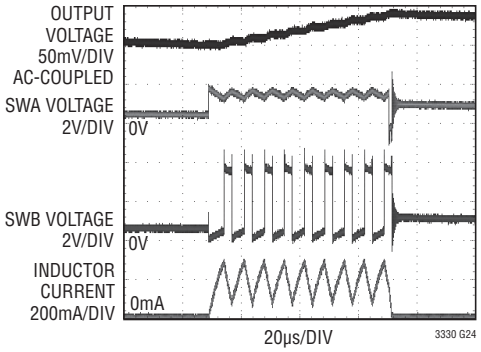
Buck-Boost Load Regulation, 3.3V



Buck-Boost Line Regulation, 3.3V

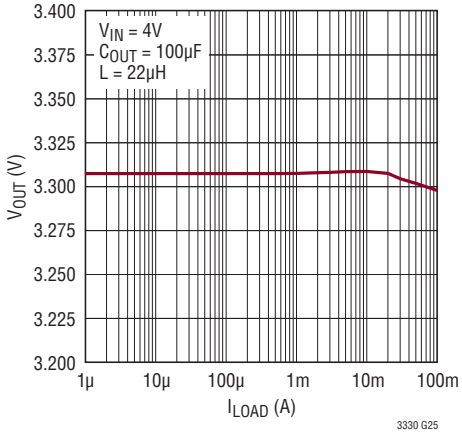


Buck-Boost Switching Waveforms

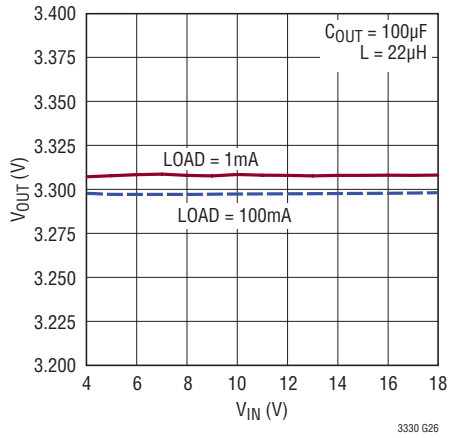


BAT = 1.8V, V_{OUT} = 3.3V
I_{LOAD} = 10mA
L = 22µH, C_{OUT} = 100µF

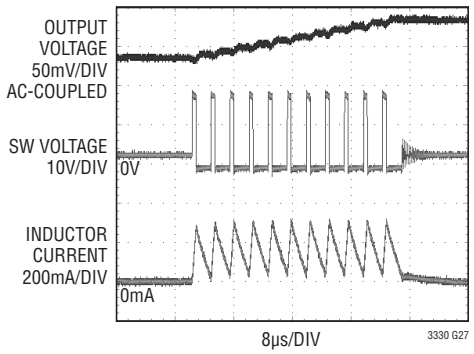
Buck Load Regulation, 3.3V



Buck Line Regulation, 3.3V



Buck Switching Waveforms

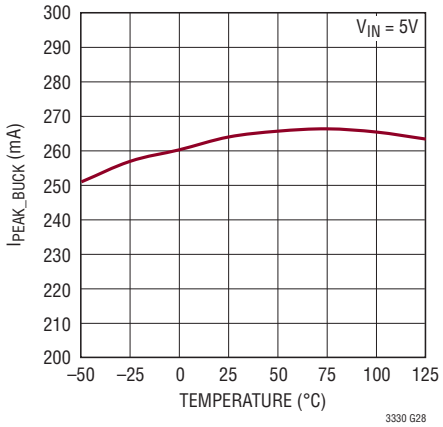


VIN = 18V, V_{OUT} = 3.3V
I_{LOAD} = 10mA
L = 22µH, C_{OUT} = 100µF

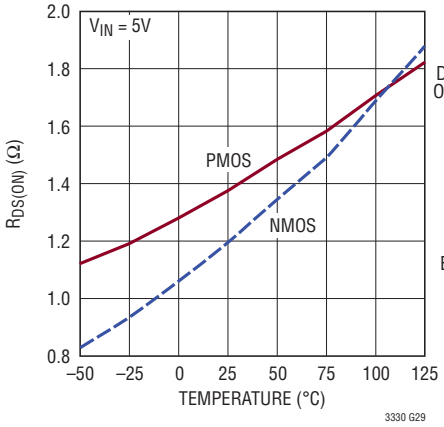
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

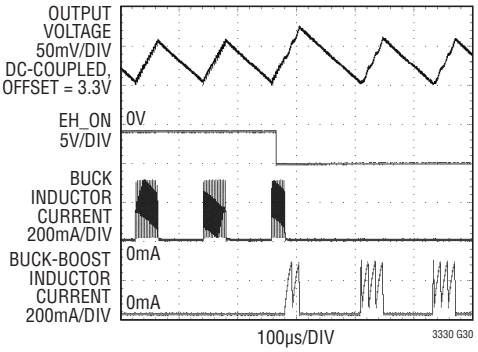
I_{PEAK_BUCK} vs Temperature



$R_{DS(ON)}$ of Buck PMOS/NMOS vs Temperature

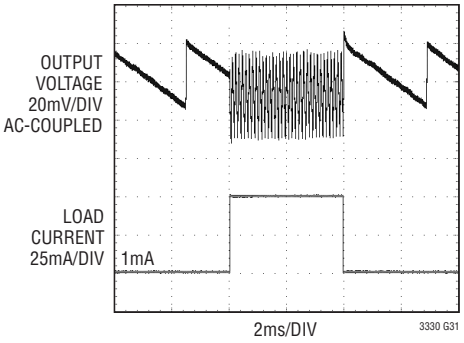


Prioritizer Buck to Buck-Boost Transition



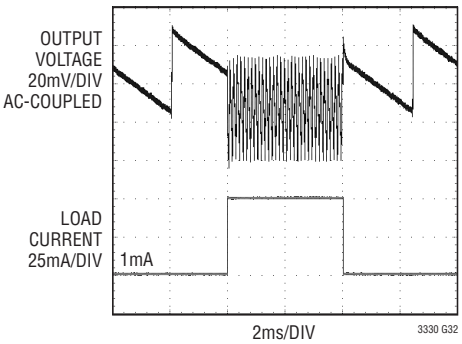
V_{IN} TRANSITIONS 18V TO 17V, UV[3:0] = 1110
BAT = 4.1V, V_{OUT} = 3.3V
I_{LOAD} = 50mA, C_{OUT} = 100µF, L_{BUCK} = 22µH, $L_{BUCK-BOOST}$ = 22µH

Buck-Boost Load Step Response



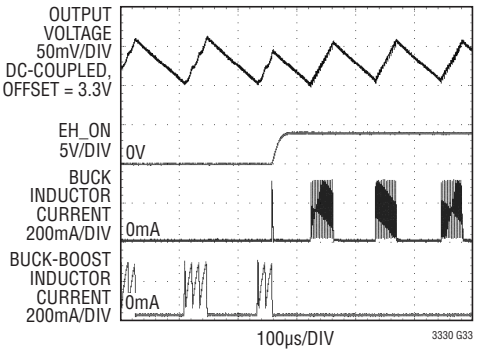
BAT = 3V, V_{OUT} = 3.3V
C_{OUT} = 100µF, L = 22µF
LOAD STEP FROM 1mA TO 50mA

Buck Load Step Response



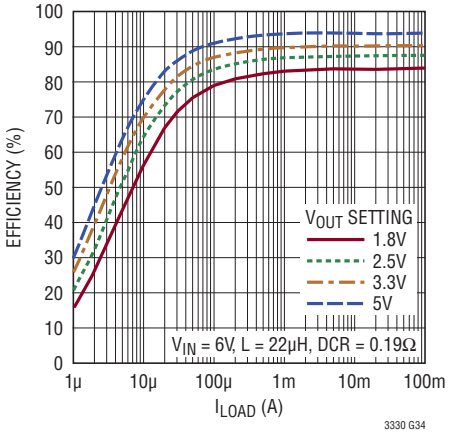
V_{IN} = 18V, V_{OUT} = 3.3V
C_{OUT} = 100µF, L = 22µF
LOAD STEP FROM 1mA TO 50mA

Prioritizer Buck-Boost to Buck Transition

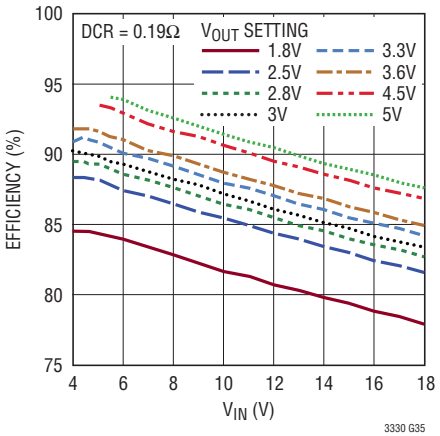


V_{IN} TRANSITIONS 17V TO 18V, UV[3:0] = 1110
BAT = 4.1V, V_{OUT} = 3.3V
I_{LOAD} = 50mA, C_{OUT} = 100µF, L_{BUCK} = 22µH, $L_{BUCK-BOOST}$ = 22µH

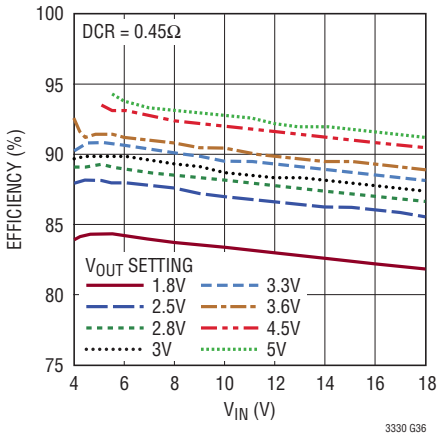
Buck Efficiency vs I_{LOAD}



Buck Efficiency vs V_{IN} for I_{LOAD} = 100mA, L = 22µH



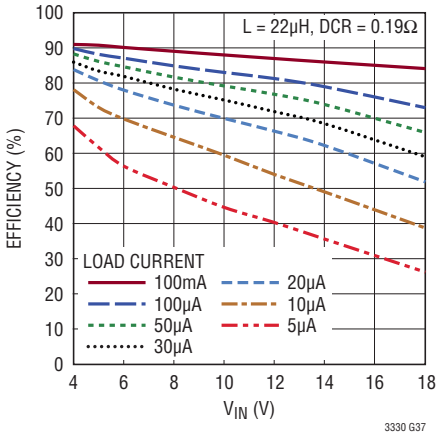
Buck Efficiency vs V_{IN} for I_{LOAD} = 100mA, L = 100µH



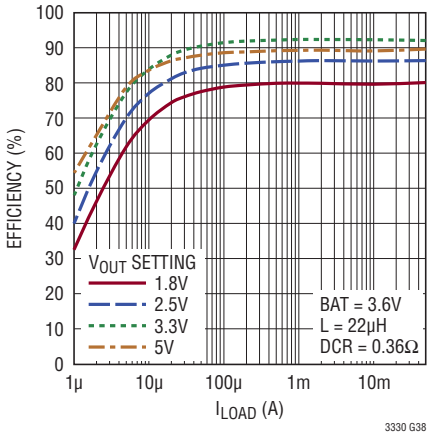
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

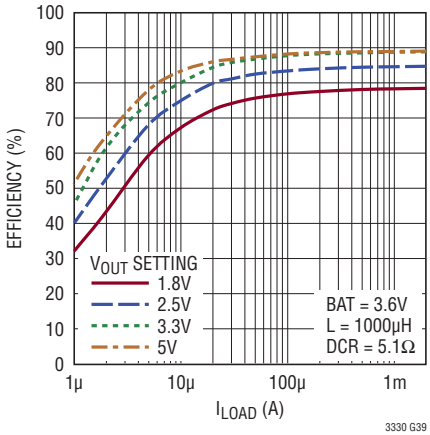
Buck Efficiency vs V_{IN}, for V_{OUT} = 3.3V



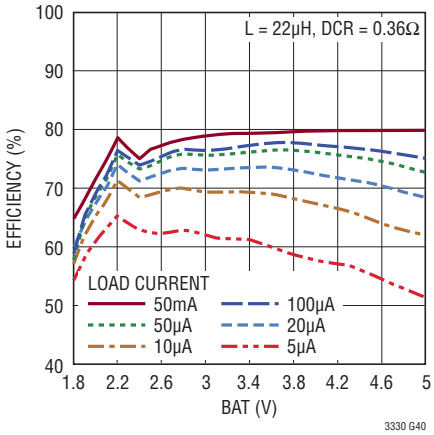
Buck-Boost Efficiency vs I_{LOAD}, 250mA I_{PEAK} Setting



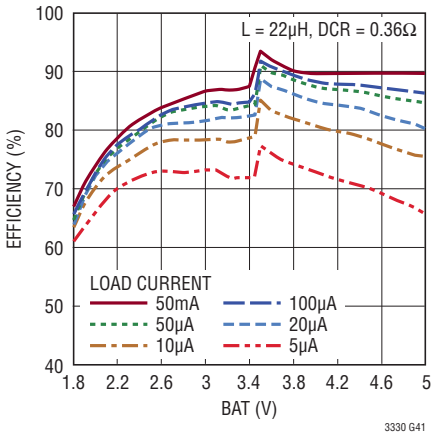
Buck-Boost Efficiency vs I_{LOAD}, 5mA I_{PEAK} Setting



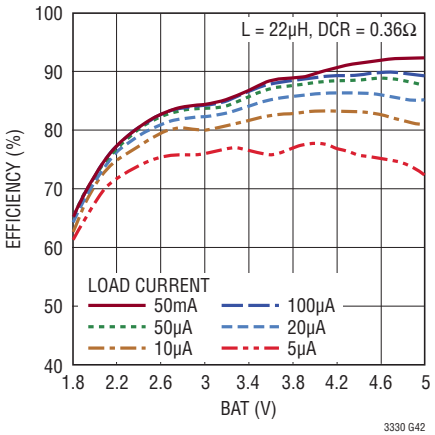
Buck-Boost Efficiency vs BAT for V_{OUT} = 1.8V, 250mA I_{PEAK} Setting



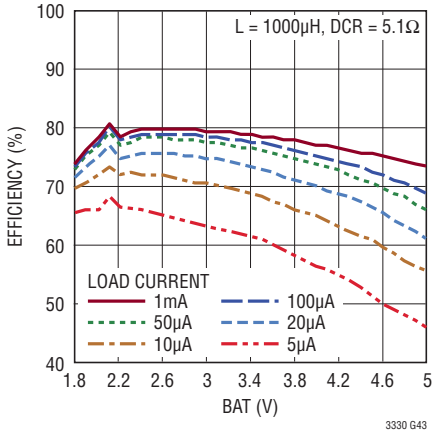
Buck-Boost Efficiency vs BAT for V_{OUT} = 3.3V, 250mA I_{PEAK} Setting



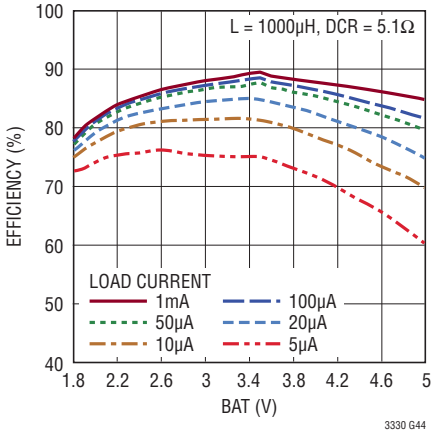
Buck-Boost Efficiency vs BAT for V_{OUT} = 5V, 250mA I_{PEAK} Setting



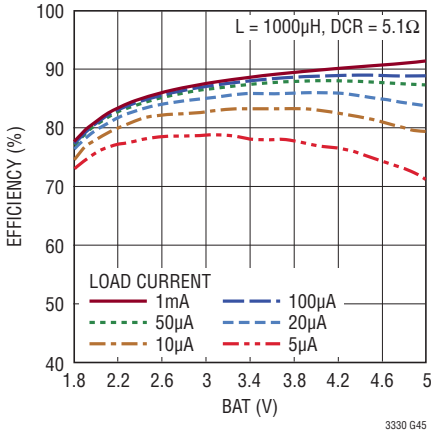
Buck-Boost Efficiency vs BAT for V_{OUT} = 1.8V, 5mA I_{PEAK} Setting



Buck-Boost Efficiency vs BAT for V_{OUT} = 3.3V, 5mA I_{PEAK} Setting



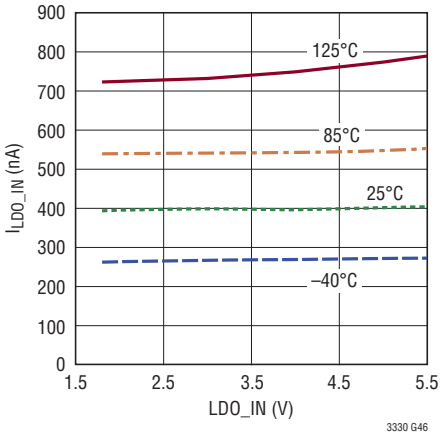
Buck-Boost Efficiency vs BAT for V_{OUT} = 5V, 5mA I_{PEAK} Setting



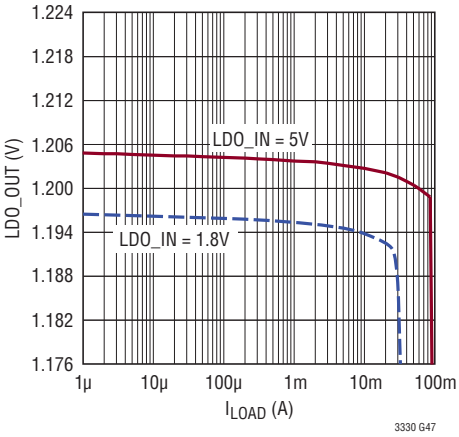
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

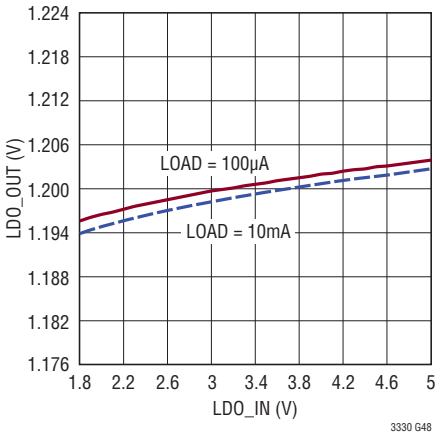
I_{LDO_IN} vs LDO_IN



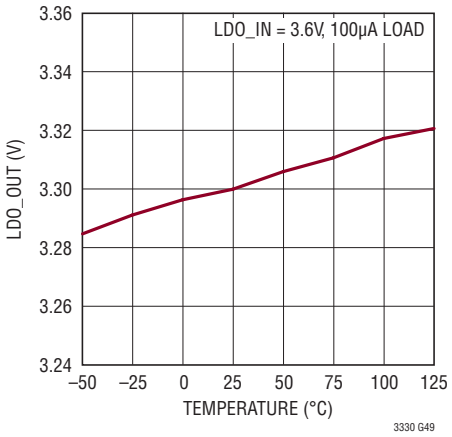
LDO Load Regulation, 1.2V



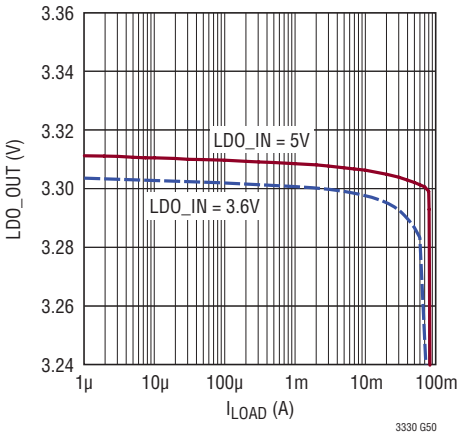
LDO Line Regulation, 1.2V



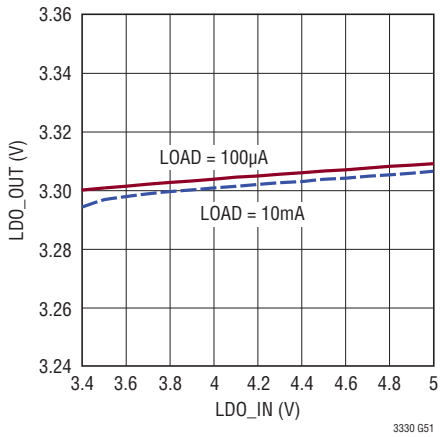
LDO_OUT vs Temperature, LDO_OUT = 3.3V



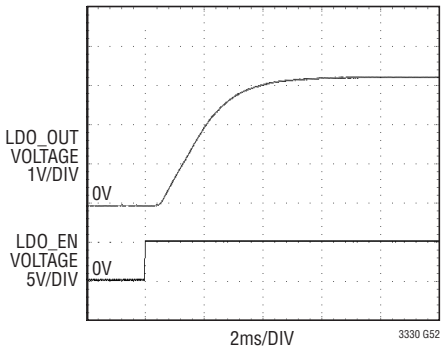
LDO Load Regulation, 3.3V



LDO Line Regulation, 3.3V

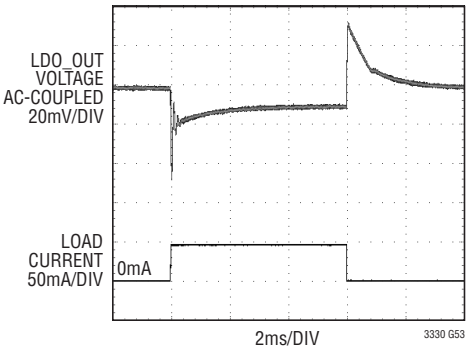


LDO Start-Up



LDO_IN = 5V, LDO[2:0] = 110
C_{LDO_OUT} = 22µF

LDO Load Step

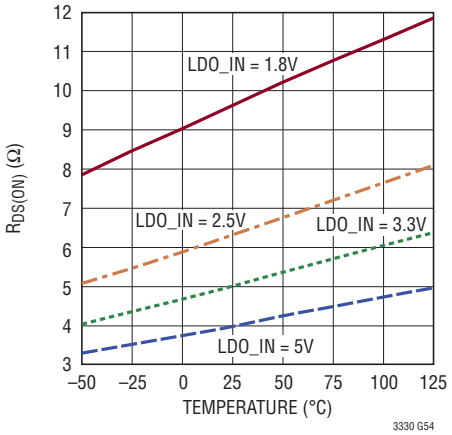


LDO_IN = 5V, LDO_OUT = 3.3V
C_{LDO_OUT} = 33µF
LOAD STEP BETWEEN 1mA AND 50mA

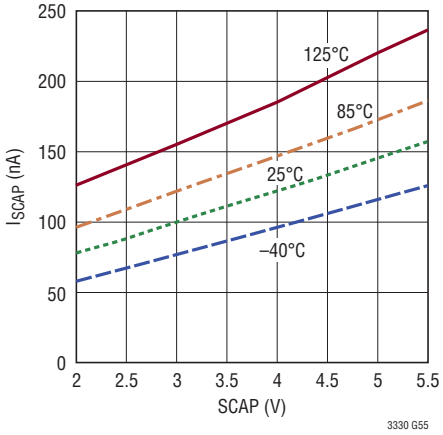
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

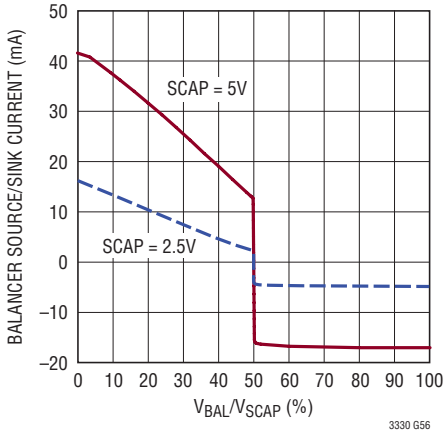
$R_{DS(ON)}$ of LDO PMOS vs Temperature



I_{SCAP} vs SCAP



Supercapacitor Balancer Source/ Sink Current



PIN FUNCTIONS

BAL (Pin 1): Supercapacitor Balance Point. The common node of a stack of two supercapacitors is connected to BAL. A source/sink balancing current of up to 10mA is available. Tie BAL along with SCAP to GND to disable the balancer and its associated quiescent current.

SCAP (Pin 2): Supply and Input for Supercapacitor Balancer. Tie the top of a 2-capacitor stack to SCAP and the middle of the stack to BAL to activate balancing. Tie SCAP along with BAL to GND to disable the balancer and its associated quiescent current.

V_{IN2} (Pin 3): Internal Low Voltage Rail to Serve as Gate Drive for Buck NMOS Switch. Connect a 4.7µF (or larger) capacitor from V_{IN2} to GND. This pin is not intended for use as an external system rail.

UV3, UV2, UV1, UV0 (Pins 4, 5, 6, 7): UVLO Select Bits for the Buck Switching Regulator. Tie high to V_{IN2} or low to GND to select the desired UVLO rising and falling thresholds (see Table 4). The UVLO falling threshold must be greater than the selected V_{OUT} regulation level. Do not float.

AC1 (Pin 8): Input Connection for Piezoelectric Element, Other AC Source, or current limited DC source (used in conjunction with AC2 for differential AC inputs).

AC2 (Pin 9): Input Connection for Piezoelectric Element, Other AC Source, or current limited DC source (used in conjunction with AC1 for differential AC inputs).

V_{IN} (Pin 10): Rectified Input Voltage. A capacitor on this pin serves as an energy reservoir and input supply for the buck regulator. The V_{IN} voltage is internally clamped to a maximum of 20V (typical).

CAP (Pin 11): Internal Rail Referenced to V_{IN} to Serve as Gate Drive for Buck PMOS Switch. Connect a 1µF (or larger) capacitor between CAP and V_{IN}. This pin is not intended for use as an external system rail.

SW (Pin 12): Switch Node for the Buck Switching Regulator. Connect a 22µH or greater external inductor between this node and V_{OUT}.

V_{OUT} (Pin 13): Regulated Output Voltage Derived from the Buck or Buck-Boost Switching Regulator.

SWB (Pin 14): Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor (value in Table 3) between this node and SWA.

SWA (Pin 15): Switch Node for the Buck-Boost Switching Regulator. Connect an external inductor (value in Table 3) between this node and SWB.

BAT (Pin 16): Battery Input. BAT serves as the input to the buck-boost switching regulator.

PIN FUNCTIONS

IPK0, IPK1, IPK2 (Pins 17, 18, 19): I_{PEAK_BB} Select Bits for the Buck-Boost Switching Regulator. Tie high to V_{IN3} or low to GND to select the desired I_{PEAK_BB} (see Table 3). Do not float.

LDO_OUT (Pin 20): Regulated LDO Output. This output can be used as a quiet supply. One of the eight settings provides for a current limited switched output where LDO_OUT = LDO_IN.

LDO_IN (Pin 21): Input Voltage for the LDO regulator.

LDO2, LDO1, LDO0 (Pins 22, 23, 24): LDO Voltage Select Bits. Tie high to LDO_IN or low to GND to select the desired LDO_OUT voltage (see Table 2). Do not float.

LDO_EN (Pin 25): LDO Enable Input. Active high input with logic levels referenced to LDO_IN. Do not float.

V_{IN3} (Pin 26): Internal Low Voltage Rail Used by the Prioritizer. Logic high reference for IPK[2:0] and OUT[2:0]. Connect a 1µF (or larger) capacitor from V_{IN3} to GND. This pin is not intended for use as an external system rail.

PGLDO (Pin 27): Power Good Output for LDO_OUT. Logic level output referenced to an internal maximum rail (see Operation). PGLDO transitioning high indicates 92% (typical) regulation has been reached on LDO_OUT. PGLDO remains high until LDO_OUT falls to 90% (typical) of the programmed regulation point.

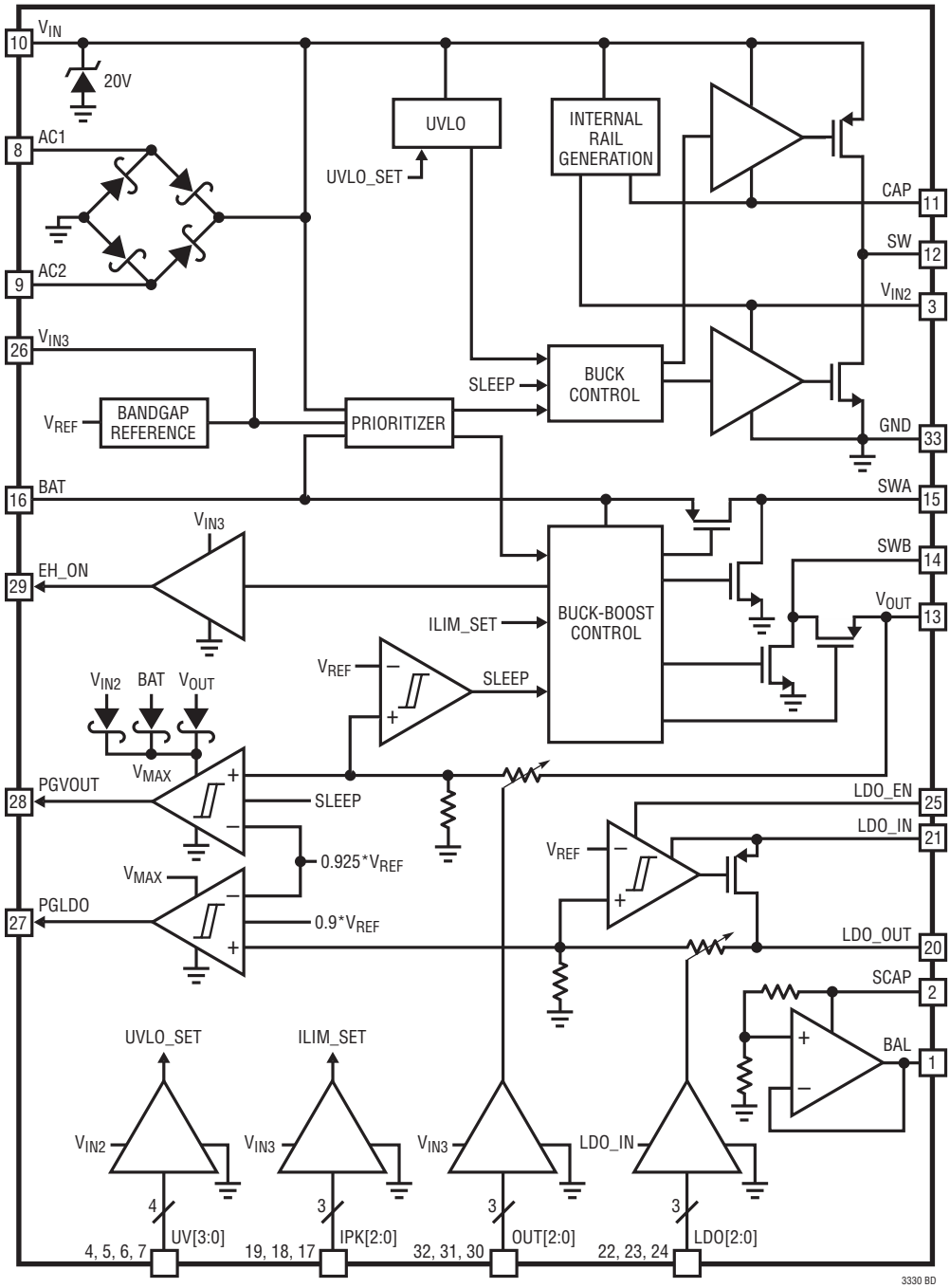
PGVOUT (Pin 28): Power Good Output for V_{OUT}. Logic level output referenced to an internal maximum rail (see Operation). PGVOUT transitioning high indicates regulation has been reached on V_{OUT} (V_{OUT} = Sleep Rising). PGVOUT remains high until V_{OUT} falls to 92% (typical) of the programmed regulation point.

EH_ON (Pin 29): Switcher Status. Logic level output referenced to V_{IN3}. EH_ON is high when the buck switching regulator is in use. It is pulled low when the buck-boost switching regulator is in use.

OUT0, OUT1, OUT2 (Pins 30, 31, 32): V_{OUT} Voltage Select Bits. Tie high to V_{IN3} or low to GND to select the desired V_{OUT} (see Table 1). Do not float.

GND (Exposed Pad Pin 33): Ground. The exposed pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3330.

BLOCK DIAGRAM



OPERATION

Modes of Operation

The following four tables detail all programmable settings on the LTC3330.

Table 1. Output Voltage Selection

OUT2	OUT1	OUT0	V_{OUT}
0	0	0	1.8V
0	0	1	2.5V
0	1	0	2.8V
0	1	1	3.0V
1	0	0	3.3V
1	0	1	3.6V
1	1	0	4.5V
1	1	1	5.0V

Table 2. LDO Voltage Selection

LDO2	LDO1	LDO0	LDO_OUT
0	0	0	1.2V
0	0	1	1.5V
0	1	0	1.8V
0	1	1	2.0V
1	0	0	2.5V
1	0	1	3.0V
1	1	0	3.3V
1	1	1	= LDO_IN

Table 3. I_{PEAK_BB} Selection

IPK2	IPK1	IPK0	I_{LIM}	L_{MIN}
0	0	0	5mA	1000µH
0	0	1	10mA	470µH
0	1	0	15mA	330µH
0	1	1	25mA	220µH
1	0	0	50mA	100µH
1	0	1	100mA	47µH
1	1	0	150mA	33µH
1	1	1	250mA	22µH

Table 4. V_{IN} UVLO Threshold Selection

UV3	UV2	UV1	UV0	UVLO RISING	UVLO FALLING
0	0	0	0	4V	3V
0	0	0	1	5V	4V
0	0	1	0	6V	5V
0	0	1	1	7V	6V
0	1	0	0	8V	7V
0	1	0	1	8V	5V
0	1	1	0	10V	9V
0	1	1	1	10V	5V
1	0	0	0	12V	11V
1	0	0	1	12V	5V
1	0	1	0	14V	13V
1	0	1	1	14V	5V
1	1	0	0	16V	15V
1	1	0	1	16V	5V
1	1	1	0	18V	17V
1	1	1	1	18V	5V

OPERATION

OVERVIEW

The LTC3330 combines a buck switching regulator and a buck-boost switching regulator to produce an energy harvesting solution with battery backup. The converters are controlled by a prioritizer that selects which converter to use based on the availability of a battery and/or harvestable energy. If harvested energy is available the buck regulator is active and the buck-boost is OFF. With an optional LDO and supercapacitor balancer and an array of different configurations the LTC3330 suits many applications.

BUCK CONVERTER

The synchronous buck converter is an ultralow quiescent current power supply tailored to energy harvesting applications. It is designed to interface directly to a piezoelectric or alternative A/C power source, rectify the input voltage, and store harvested energy on an external capacitor while maintaining a regulated output voltage. It can also bleed off any excess input power via an internal protective shunt regulator.

INTERNAL BRIDGE RECTIFIER

An internal full-wave bridge rectifier accessible via the differential AC1 and AC2 inputs rectifies AC sources such as those from a piezoelectric element. The rectified output is stored on a capacitor at the V_{IN} pin and can be used as an energy reservoir for the buck converter. The bridge rectifier has a total drop of about 800mV at typical piezo-generated currents (~10µA), but is capable of carrying up to 50mA. Either side of the bridge can be operated independently as a single-ended AC or DC input.

BUCK UNDERVOLTAGE LOCKOUT (UVLO)

When the voltage on V_{IN} rises above the UVLO rising threshold the buck converter is enabled and charge is transferred from the input capacitor to the output capacitor. When the input capacitor voltage is depleted below the UVLO falling threshold the buck converter is disabled. These thresholds can be set according to Table 4 which offers UVLO rising thresholds from 4V to 18V with large or small hysteresis windows. This allows for programming of the UVLO window near the peak power point of the input source. Extremely low quiescent current (450nA typical) in UVLO allows energy to accumulate on the input capacitor in situations where energy must be harvested from low power sources.

INTERNAL RAIL GENERATION (CAP, V_{IN2}, V_{IN3})

Two internal rails, CAP and V_{IN2}, are generated from V_{IN} and are used to drive the high side PMOS and low side NMOS of the buck converter, respectively. Additionally the V_{IN2} rail serves as logic high for the UVLO threshold select bits UV[3:0]. The V_{IN2} rail is regulated at 4.8V above GND while the CAP rail is regulated at 4.8V below V_{IN}. These are not intended to be used as external rails. Bypass capacitors are connected to the CAP and V_{IN2} pins to serve as energy reservoirs for driving the buck switches. When V_{IN} is below 4.8V, V_{IN2} is equal to V_{IN} and CAP is held at GND. Figure 1 shows the ideal V_{IN}, V_{IN2} and CAP relationship.

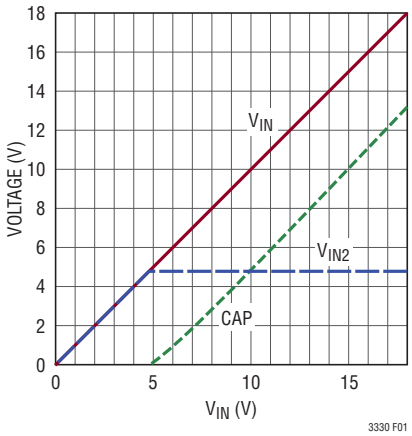


Figure 1. Ideal V_{IN}, V_{IN2} and CAP Relationship

V_{IN3} is an internal rail used by the buck and the buck-boost. When the LTC3330 runs the buck V_{IN3} will be a Schottky diode drop below V_{IN2}. When it runs the buck-boost V_{IN3} is equal to BAT.

BUCK OPERATION

The buck regulator uses a hysteretic voltage algorithm to control the output through internal feedback from the V_{OUT} sense pin. The buck converter charges an output capacitor through an inductor to a value slightly higher than the regulation point. It does this by ramping the inductor current up to I_{PEAK_BUCK} through an internal

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PMOS switch and then ramping it down to 0mA through an internal NMOS switch. This efficiently delivers energy to the output capacitor. The ramp rate is determined by V_{IN}, V_{OUT}, and the inductor value. When the buck brings the output voltage into regulation the converter enters a low quiescent current sleep state that monitors the output voltage with a sleep comparator. During this operating mode load current is provided by the output capacitor. When the output voltage falls below the regulation point the buck regulator wakes up and the cycle repeats. This hysteretic method of providing a regulated output reduces losses associated with FET switching and maintains an output at light loads. The buck delivers a minimum of 100mA of average load current when it is switching. V_{OUT} can be set from 1.8V to 5V via the output voltage select bits, OUT[2:0] (see Table 1).

When the sleep comparator senses that the output has reached the sleep threshold the buck converter may be in the middle of a cycle with current still flowing through the inductor. Normally both synchronous switches would turn off and the current in the inductor would freewheel to zero through the NMOS body diode, but the NMOS switch is kept on to prevent the conduction loss that would occur in the diode if the NMOS were off. If the PMOS is on when the sleep comparator trips the NMOS will turn on immediately in order to ramp down the current. If the NMOS is on it will be kept on until the current reaches zero.

Though the quiescent current when the buck is switching is much greater than the sleep quiescent current, it is still a small percentage of the average inductor current which results in high efficiency over most load conditions. The buck operates only when sufficient energy has been accumulated in the input capacitor and the length of time the converter needs to transfer energy to the output is much less than the time it takes to accumulate energy. Thus, the buck operating quiescent current is averaged over a long period of time so that the total average quiescent current is low. This feature accommodates sources that harvest small amounts of ambient energy.

BUCK-BOOST CONVERTER

The buck-boost uses the same hysteretic voltage algorithm as the buck to control the output, V_{OUT}, with the same sleep comparator. The buck-boost has three modes of operation: buck, buck-boost, and boost. An internal mode comparator determines the mode of operation based on BAT and V_{OUT}. Figure 2 shows the four internal switches of the buck-boost converter. In each mode the inductor current is ramped up to I_{PEAK_BB}, which is programmable via the IPK[2:0] bits and ranges from 5mA to 250mA (see Table 3).

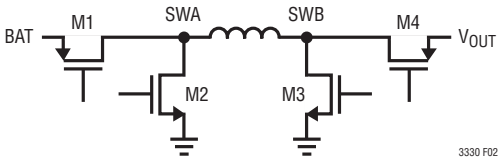

Figure 2: Buck-Boost Power Switches

In BUCK mode M4 is always on and M3 is always off. The inductor current is ramped up through M1 to I_{PEAK_BB} and down to 0mA through M2. In boost mode M1 is always on and M2 is always off. The inductor current is ramped up to I_{PEAK_BB} when M3 is on and is ramped down to 0mA when M4 is on as V_{OUT} is greater than BAT in boost mode. Buck-boost mode is very similar to boost mode in that M1 is always on and M2 is always off. If BAT is less than V_{OUT} the inductor current is ramped up to I_{PEAK_BB} through M3. When M4 turns on the current in the inductor will start to ramp down. However, because BAT is close to V_{OUT} and M1 and M4 have finite on-resistance the current ramp will exhibit a slow exponential decay, lowering the average current delivered to V_{OUT}. For this reason the lower current threshold is set to $I_{PEAK\_BB}/2$ in buck-boost mode to maintain high average current to the load. If BAT is greater than V_{OUT} in buck-boost mode the inductor current still ramps up to I_{PEAK_BB} and down to $I_{PEAK\_BB}/2$. It can still ramp down if BAT is greater than V_{OUT} because the final value of the current in the inductor would be $(V_{IN} – V_{OUT})/ (R_{ON1} + R_{ON4})$. If BAT is exactly $I_{PEAK\_BB}/2•(R_{ON1} + R_{ON4})$ above V_{OUT} the inductor current will

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not reach the I_{PEAK_BB}/2 threshold and switches M1 and M4 will stay on all the time. For higher BAT voltages the mode comparator will switch the converter to buck mode. M1 and M4 will remain on for BAT voltages up to V_{OUT} + I_{PEAK_BB}•(R_{ON1} + R_{ON4}). At this point the current in the inductor is equal to I_{PEAK_BB} and the I_{PEAK_BB} comparator will trip turning off M1 and turning on M2 causing the inductor current to ramp down to IZERO, completing the transition from buck-boost mode to buck mode.

V_{OUT} Power Good

A power good comparator is provided for the V_{OUT} output. It transitions high the first time the LTC3330 goes to sleep, indicating that V_{OUT} has reached regulation. It transitions low when V_{OUT} falls to 92% (typical) of its value at regulation. The PGVOUT output is referenced to an internal rail that is generated to be the highest of V_{IN2}, BAT, and V_{OUT} less a Schottky diode drop.

Prioritizer

The input prioritizer on the LTC3330 decides whether to use the energy harvesting input or the battery input to power V_{OUT}. If a battery is powering the buck-boost converter and harvested energy causes a UVLO rising transition on V_{IN}, the prioritizer will shut off the buck-boost and turn on the buck, orchestrating a smooth transition that maintains regulation of V_{OUT}. When harvestable energy disappears, the prioritizer will first poll the battery voltage. If the battery voltage is above 1.8V the prioritizer will switch back to the buck-boost while maintaining regulation. If the battery voltage is below 1.8V the buck-boost is not enabled and V_{OUT} cannot be supported until harvestable energy is again available. If either BAT or V_{IN} is grounded, the prioritizer allows the other input to run if its input is high enough for operation. The specified quiescent current in UVLO is valid upon start-up of the V_{IN} input and when the battery has taken over regulation of the output. If the battery is less than 1.8V when UVLO is entered and the prioritizer does not enable the buck-boost several hundred nanoamperes of additional quiescent current will appear on V_{IN}.

When the prioritizer selects the V_{IN} input the current on the BAT input drops to zero. However, if the voltage on BAT is higher than V_{IN2}, a fraction of the V_{IN} quiescent current will appear on BAT due to internal level shifting. This only affects a small range of battery voltages and UVLO settings.

A digital output, EH_ON, is low when the prioritizer has selected the BAT input and is high when the prioritizer has selected the V_{IN} input. The EH_ON output is referenced to V_{IN3}.

Low Drop Out Regulator

An integrated low drop out regulator (LDO) is available with its own input, LDO_IN. It will regulate LDO_OUT to seven different output voltages based on the LDO[2:0] pins. An eighth mode is provided to turn the LDO into a current-limited switch in which the PMOS is always on. LDO_EN enables the LDO when high and when low eliminates all quiescent current on LDO_IN. The LDO is designed to provide 50mA over a range of LDO_IN and LDO_OUT combinations. A current limit set above 50mA is available to dial back the current if the output is grounded or the load demands more than 50mA. The LDO also features a 1ms soft-start for smooth output start-up.

A power good signal on the PGLDO pin indicates when the voltage at LDO_OUT rises above 92% (typical) of its final value, or after tripped, when the LDO_OUT falls below 90% of that value. The PGLDO output is referenced to an internal rail that is generated to be the highest of V_{IN2}, BAT, and V_{OUT} less a Schottky diode drop.

Supercapacitor Balancer

An integrated supercapacitor balancer with 150nA of quiescent current is available to balance a stack of two supercapacitors. Typically the input, SCAP, will tie to V_{OUT} to allow for increased energy storage at V_{OUT} with supercapacitors. The BAL pin is tied to the middle of the stack and can source and sink 10mA to regulate the BAL pin's voltage to half that of the SCAP pin's voltage. To disable the balancer and its associated quiescent current the SCAP and BAL pins can be tied to ground.

APPLICATIONS

The LTC3330 allows for energy harvesting from a variety of alternative energy sources in order to extend the life of a battery powered wireless sensor system. The extremely low quiescent current of the LTC3330 facilitates harvesting from sources generating only microamps of current. The onboard bridge rectifier is suitable for AC piezoelectric or electromagnetic sources as well as providing reverse protection for DC sources such as solar and thermoelectric generators. The LTC3330 powers the V_{OUT} output continuously by seamlessly switching between the energy harvesting and battery inputs.

When harvestable energy is available, it is transferred through the bridge rectifier where it accumulates on the V_{IN} capacitor. A low quiescent current UVLO mode allows the voltage on the capacitor to increase towards a programmed UVLO rising threshold. When the voltage rises to this level, the buck converter turns on and transfers energy to V_{OUT}. As energy is transferred the voltage at V_{IN} may decrease to the UVLO falling threshold. If this happens, the buck converter turns off and the buck-boost then turns on to service the load from the battery input while more energy is harvested. When the buck is running the quiescent current on the BAT pin is essentially zero.

The LTC3330 is well suited to wireless systems which consume low average power but occasionally need a higher concentrated burst of power to accomplish a task. If these bursts occur with a low duty cycle such that the total energy needed for a burst can be accumulated between bursts then the output can be maintained entirely by the harvester. If the bursts need to happen more frequently or if harvestable energy goes away the battery will be used.

Piezo Energy Harvesting

Ambient vibrational energy can be harvested with a piezoelectric transducer which produces a voltage and current in response to strain. Common piezoelectric elements are PZT (lead zirconate titanate) ceramics, PVDF (polyvinylidene fluoride) polymers, or other composites. Ceramic piezoelectric elements exhibit a piezoelectric effect when the crystal structure of the ceramic is compressed and internal dipole movement produces a voltage. Polymer elements comprised of long-chain molecules produce a voltage when flexed as molecules repel each other. Ceramics are often used under direct pressure while a polymer is commonly used as a cantilevered beam.

A wide range of piezoelectric elements are available and produce a variety of open-circuit voltages and short-circuit currents. Typically the open-circuit voltage and short-circuit currents increase with available vibrational energy as shown in Figure 3. Piezoelectric elements can be placed in series or in parallel to achieve desired open-circuit voltages.

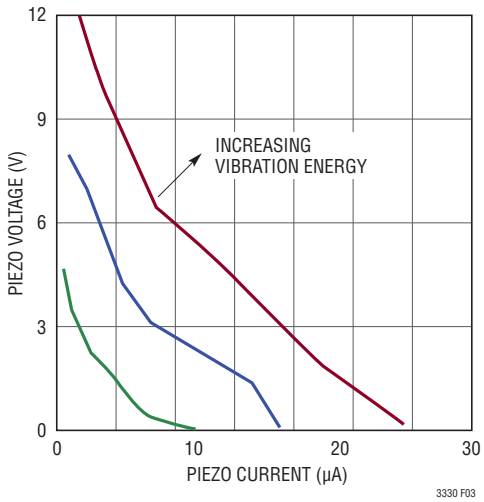

Figure 3. Typical Piezoelectric Load Lines for Piezo Systems T220-A4-503X

Piezos produce the most power when they operate at approximately half the open circuit voltage for a given vibration level. The UVLO window can be programmed to straddle this voltage so that the piezo operates near the peak power point. In addition to the normal configuration of connecting the piezo across the AC1 and AC2 inputs, a piezo can be connected from either AC1 or AC2 to ground. The resulting configuration is a voltage doubler as seen in Figure 4 where the intrinsic capacitance of the piezo is used as the doubling capacitor.

APPLICATIONS

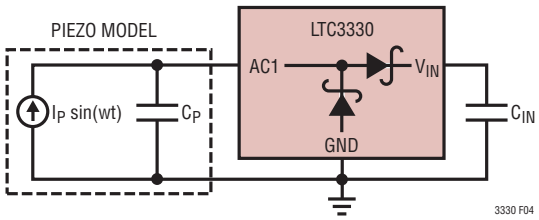

Figure 4. LTC3330 Voltage Doubler Configuration

A second piezo may be connected from AC2 to ground. This may be of use if the second piezo is mechanically tuned to a different resonant frequency present in the system than the first piezo. Of the two piezos the one operating at the higher open circuit voltage will win over the other piezo and its doubled voltage will appear on the V_{IN} capacitor. To achieve maximum power transfer from the piezo with the doubler the UVLO window should be set to the open circuit voltage of the piezo.

Piezoelectric elements are available from the manufacturers listed in Table 5.

Table 5. Piezoelectric Element Manufacturers

Advanced Cerametrics	www.advancedcerametrics.com
Piezo Systems	www.piezo.com
Measurement Specialties	www.meas-spec.com
PI (Physik Instrumente)	www.pi-usa.us
MIDE Technology Corporation	www.mide.com
Morgan Technical Ceramics	www.morganelectroceramics.com

Electromagnetic Energy Harvesting

Another alternative AC source is an electromagnetic vibration harvester in which a magnet vibrating inside a coil induces an AC voltage and current in the coil that can then be rectified and harvested by the LTC3330. The vibration could be ambient to the system or it could be caused by an impulse as in a spring loaded switch.

Solar Energy Harvesting

The LTC3330 can harvest solar energy as the bridge rectifier can be used to provide reverse protection for a solar panel. A solar cell produces current in proportion to the amount of light falling on it. Figure 5 shows the relationship between current and voltage for a solar panel illuminated with several levels of light. The maximum power output occurs near the knee of each curve where the cell transitions from a constant current device to a constant voltage device. Fortunately, the peak power point doesn't change much with illumination and an appropriate UVLO window can be selected so that the panel operates near the peak power point for a majority of light conditions.

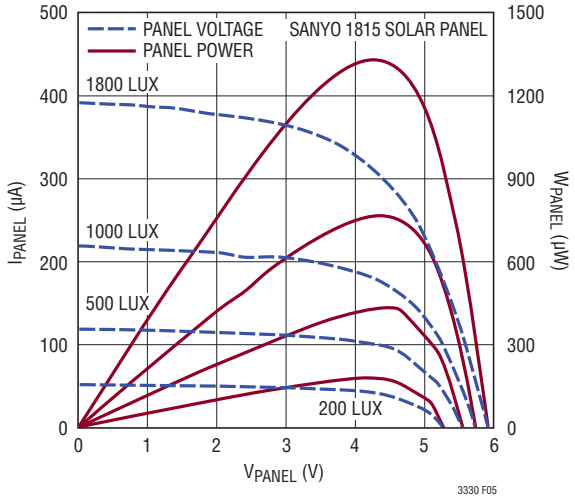

Figure 5. Typical Solar Panel Characteristics

Two solar panels can be connected to the LTC3330, one from AC1 to ground and another from AC2 to ground. Each panel could be aimed in a different direction to capture light from different angles or at different times of the day as the sun moves. The panels should be similar or the same so that the selected UVLO window is optimal for both panels.

BAT, V_{IN}, and V_{OUT} Capacitors

The input capacitor for the buck-boost on the BAT pin should be bypassed with at least 4.7µF to GND. In cases where the series resistance of the battery is high, a larger capacitor may be desired to handle transients. A larger capacitor may also be necessary when operating close to 1.8V with the higher I_{PEAK_BB} selections to prevent the battery voltage from falling below 1.8V when the buck-boost is switching.

The input capacitor to the buck on V_{IN} and the V_{OUT} capacitor can vary widely and should be selected to optimize the use of an energy harvesting source depending

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on whether storage of the harvested energy is needed at the input or the output. Storing energy at the input takes advantage of the high input voltage as the energy stored in a capacitor increases with the square of its voltage. Storage at the output may be necessary to handle load transients greater than the 100mA the buck can provide.

The input or output capacitor should be sized to store enough energy to provide output power for the length of time required. If enough energy is stored so that the buck does not reach the UVLO falling threshold during a load transient then the battery current will always be zero. Spacing load transients so that the average power required to service the application is less than or equal to the power available from the energy harvesting source will then greatly extend the life of the battery. The V_{IN} capacitor should be rated to withstand the highest voltage ever present at V_{IN}.

The following equation can be used to size the input capacitor to meet the power requirements of the output for the desired duration:

$$P_{LOAD}\, t_{LOAD} = \frac{1}{2}\eta C_{IN}(V_{IN}^2 - V_{UVLOFALLING}^2)$$

$$V_{UVLOFALLING} \le V_{IN} \le V_{SHUNT}$$

Here η is the average efficiency of the buck converter over the input voltage range and V_{IN} is the input voltage when the buck begins to switch. Typically V_{IN} will be the UVLO rising threshold. This equation may overestimate the input capacitor necessary as it may be acceptable to allow the load current to deplete the output capacitor all the way to the lower PGVOUT threshold. It also assumes that the input source charging has a negligible effect during this time.

The duration for which the buck or buck-boost regulator sleeps depends on the load current and the size of the V_{OUT} capacitor. The sleep time decreases as the load current increases and/or as the output capacitor decreases. The DC sleep hysteresis window is ±6mV for the 1.8V output and scales linearly with the output voltage setting (±12mV for the 3.6V setting, etc.). Ideally this means that the sleep time is determined by the following equation:

$$t_{SLEEP} = C_{OUT}\frac{V_{DC\_HYS}}{I_{LOAD}}$$

This is true for output capacitors on the order of 100µF or larger, but as the output capacitor decreases towards 10µF, delays in the internal sleep comparator along with the load current itself may result in the V_{OUT} voltage slewing past the DC thresholds. This will lengthen the sleep time and increase V_{OUT} ripple. A capacitor less than 10µF is not recommended as V_{OUT} ripple could increase to an undesirable level. If transient load currents above 100mA are required then a larger capacitor should be used at the output. This capacitor will be continuously discharged during a load condition and the capacitor can be sized for an acceptable drop in V_{OUT}:

$$C_{OUT} = (I_{LOAD} - I_{DC/DC})\frac{t_{LOAD}}{V_{OUT}^{+} - V_{OUT}^{-}}$$

Here V_{OUT}^{+} is the value of V_{OUT} when PGVOUT goes high and V_{OUT}^{-} is the desired lower limit of V_{OUT}. $I_{DC/DC}$ is the average current being delivered from either the buck converter or the buck-boost converter. The buck converter typically delivers 125mA on average to the output as the inductor current is ramped up to 250mA and down to zero. The current the buck-boost delivers depends on the mode of operation and the I_{PEAK_BB} setting. In buck mode the deliverable current is $I_{PEAK\_BB}/2$. In buck-boost and boost modes the deliverable current also depends on the V_{IN} to V_{OUT} ratio:

Buck-boost mode: $$I_{DC/DC} = \frac{3}{4} I_{PEAK\_BB}\frac{V_{IN}}{V_{OUT}}$$

Boost mode: $$I_{DC/DC} = \frac{1}{2} I_{PEAK\_BB}\frac{V_{IN}}{V_{OUT}}$$

A standard surface mount ceramic capacitor can be used for C_{OUT}, though some applications may be better suited to a low leakage aluminum electrolytic capacitor or a supercapacitor. These capacitors can be obtained from manufacturers such as Vishay, Illinois Capacitor, AVX, or CAP-XX.

APPLICATIONS

Supercapacitor Balancer

If supercapacitors are used at V_{OUT} the onboard supercapacitor balancer can be used to balance them with ±10mA of balance current. A list of supercapacitor suppliers is provided in Table 6.

Table 6. Supercapacitor Suppliers

CAP-XX	www.cap-xx.com
NESS CAP	www.nesscap.com
Maxwell	www.maxwell.com
Bussman	www.cooperbussman.com
AVX	www.avx.com
Illinios Capacitor	www.illcap.com
Tecate Group	www.tecategroup.com

By seamlessly combining a battery source and an energy harvesting source, the LTC3330 enables the use of supercapacitors in energy harvesting applications. The battery provides the initial current required to overcome the effects of the diffusion current when voltage is first applied to the supercapacitors. The energy harvesting source can then support the lower steady state leakage current and average load current.

LDO Capacitors

The input to the low dropout regulator, LDO_IN, should be bypassed with at least 4.7µF to GND. If LDO_IN is connected to V_{OUT} the V_{OUT} capacitor may adequately bypass the LDO input. If the board connection between LDO_IN and V_{OUT} is long then an additional 1µF bypass capacitor to GND near the LDO_IN pin may be required.

The LDO_OUT capacitor should be at least 22µF to keep load step responses within 2% of regulation. A smaller capacitor may lead to worse transient response and/or instability whereas a higher capacitor will improve transient response.

CAP, V_{IN2}, and V_{IN3} Capacitors

A 1µF or larger capacitor must be connected between V_{IN} and CAP and a 4.7µF capacitor must be connected between V_{IN2} and GND. These capacitors hold up the internal rails during buck switching and compensate the internal rail generation circuits. In applications where the voltage at V_{IN} is limited to less than 6V, the CAP pin can be tied to GND and the V_{IN2} pin can be tied to V_{IN} as shown in Figure 6. An optional 5.6V Zener diode can be connected to V_{IN} to clamp V_{IN} in this scenario. The leakage of the Zener diode below its clamping voltage should be considered as it could be comparable to the quiescent current of the LTC3330. This circuit does not require the capacitors on V_{IN2} and CAP, saving two components and allowing for a lower voltage rating for the single V_{IN} capacitor.

A 1µF or larger bypass capacitor must be connected from V_{IN3} to ground. V_{IN3} is an internal rail that is shared by both the buck and buck-boost. It is not intended for use as a system rail. It is used as a the logic high reference level for the IPK[2:0] and OUT[2:0] digital inputs. In the event that these pins are dynamically driven in the application, external inverters may be needed and they must use V_{IN3} as a rail. However, care must be taken not to overload V_{IN3} and the quiescent current of such logic should be kept minimal. The output resistance of the V_{IN3} pin is typically 15kΩ.

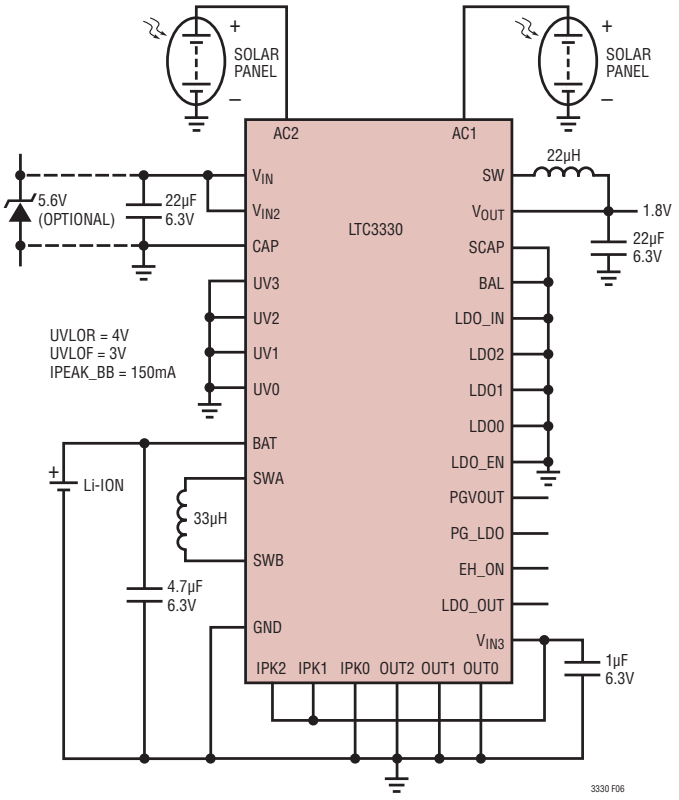


Figure 6. Low Voltage Solar Harvester with Reduced Component Count (V_{IN} < 6V)

APPLICATIONS

Inductor Selection

The buck is optimized to work with a 22µH inductor in typical applications. A larger inductor will benefit high voltage applications by increasing the on-time of the PMOS switch and improving efficiency by reducing gate charge loss. Choose an inductor with a DC current rating greater than 350mA. The DCR of the inductor can have an impact on efficiency as it is a source of loss. Tradeoffs between price, size, and DCR should be evaluated.

The buck-boost is optimized to work with a minimum inductor of 22µH for the 250mA I_{PEAK_BB} setting. For the other seven I_{PEAK_BB} settings the inductor value should increase as the I_{PEAK_BB} selection decreases to maintain the same $I_{PEAK\_BB} \bullet L$ product. The minimum inductor values for the buck-boost for each I_{PEAK_BB} setting are listed in Table 3. Larger inductors may increase efficiency. Choose an inductor with an I_{SAT} rating at least 50% greater than the selected I_{PEAK} value. Table 7 lists several inductors that work well with both the buck and the buck-boost.

Table 7. Recommended Inductors for the LTC3330

PART NUMBER	L(µH)	MANUFACTURER	SIZE (mm) (L × W × H)	MAX IDC (mA)	MAX DCR (Ω)
744043102	1000	Würth Electronic	4.8 × 4.8 × 2.8	80	7
LPS5030-105ML		Coilcraft	5.51 × 5.51 × 2.9	110	5.1
LPS4018-105ML		Coilcraft	3.9 × 3.9 × 1.7	98	18
LPS3314-105ML		Coilcraft	3.3 × 3.3 × 1.3	99	31
B82442T1105K050		EPCOS	5.6 × 5 × 5	150	9.5
744043471	470	Würth Electronic	4.8 × 4.8 × 2.8	125	2.6
LPS4018-474ML		Coilcraft	3.9 × 3.9 × 1.7	160	7.8
LPS3314-474ML		Coilcraft	3.3 × 3.3 × 1.3	110	12
B82442T147K050		EPCOS	5.6 × 5 × 5	240	4.73
744042331	330	Würth Electronic	4.8 × 4.8 × 1.8	130	4.5
LPS4018-334ML		Coilcraft	3.9 × 3.9 × 1.7	190	5.9
LPS3314-334ML		Coilcraft	3.3 × 3.3 × 1.3	110	9.3
B82442T1334K050		EPCOS	5.6 × 5 × 5	280	3.29
744042221	220	Würth Electronic	4.8 × 4.8 × 1.8	160	3.2
LPS4018-224ML		Coilcraft	3.9 × 3.9 × 1.7	260	3.7
LPS3314-224ML		Coilcraft	3.3 × 3.3 × 1.3	160	6
B82442T1224K050		EPCOS	5.6 × 5 × 5	330	2.2
744031101	100	Würth Electronic	3.8 × 3.8 × 1.65	180	2.4
LPS4018-104ML		Coilcraft	3.9 × 3.9 × 1.7	360	1.4
LPS3314-104ML		Coilcraft	3.3 × 3.3 × 1.3	230	2.75
B82442T1104K050		EPCOS	5.6 × 5 × 5	510	0.99
744031470	47	Würth Electronic	3.8 × 3.8 × 1.65	250	1
LPS4018-473ML		Coilcraft	3.9 × 3.9 × 1.7	550	0.65
LPS3314-473ML		Coilcraft	3.3 × 3.3 × 1.3	330	1.4
B82442T1473K050		EPCOS	5.6 × 5 × 5	700	0.519
744031330	33	Würth Electronic	3.8 × 3.8 × 1.65	320	0.66
LPS4018-333ML		Coilcraft	3.9 × 3.9 × 1.7	640	0.42
LPS3314-333ML		Coilcraft	3.3 × 3.3 × 1.3	380	0.92
1070BS-330ML		Toko	3.2 × 3.2 × 2	230	0.61
B82442T1333K050		EPCOS	5.6 × 5 × 5	840	0.36
744031220	22	Würth Electronic	3.8 × 3.8 × 1.65	360	0.45
LPS5030-223ML		Coilcraft	5.51 × 5.51 × 2.9	750	0.19
LPS4018-223ML		Coilcraft	3.9 × 3.9 × 1.7	800	0.36
LPS3314-223ML		Coilcraft	3.3 × 3.3 × 1.3	450	0.72
1070AS-220M		Toko	3.2 × 3.2 × 2	410	0.64
B82442T1223K050		EPCOS	5.6 × 5 × 5	1040	0.238
744029220	22	Würth Electronic	2.8 × 2.8 × 1.35	300	0.97
1069BS-220M		Toko	3.2 × 3.2 × 1.8	290	0.495

APPLICATIONS

Summary of Digital Inputs and Outputs

There are 14 digital pin-strapped logic inputs to the LTC3330 and three digital logic outputs. These and the rails they are referenced to are summarized in Table 8.

Table 8. Digital Pin Summary

INPUT PIN	LOGIC HIGH LEVEL
UV[3:0]	V_{IN2}
IPK[2:0]	V_{IN3}
OUT[2:0]	V_{IN3}
LDO[2:0]	LDO_IN
LDO_EN	LDO_IN up to 6V

OUTPUT PIN	LOGIC HIGH LEVEL
PGVOUT	MAX (BAT, V_{IN2}, V_{OUT})
PGLDO	MAX (BAT, V_{IN2}, V_{OUT})
EH_ON	V_{IN3}

LTC3330 System Solutions

The LTC3330 can be paired with other Linear Technology low quiescent current integrated circuits to form a multirail system. Figure 7 shows an LTC3330 powering an LTC3388-3 from its 5V output. The LTC3388-3, an 800nA Buck converter, is configured here to produce a negative 5V rail by tying the V_{OUT} pin to ground and tying its GND pin to the regulated –5V output. The result is a ±5V energy harvesting power supply with battery backup.

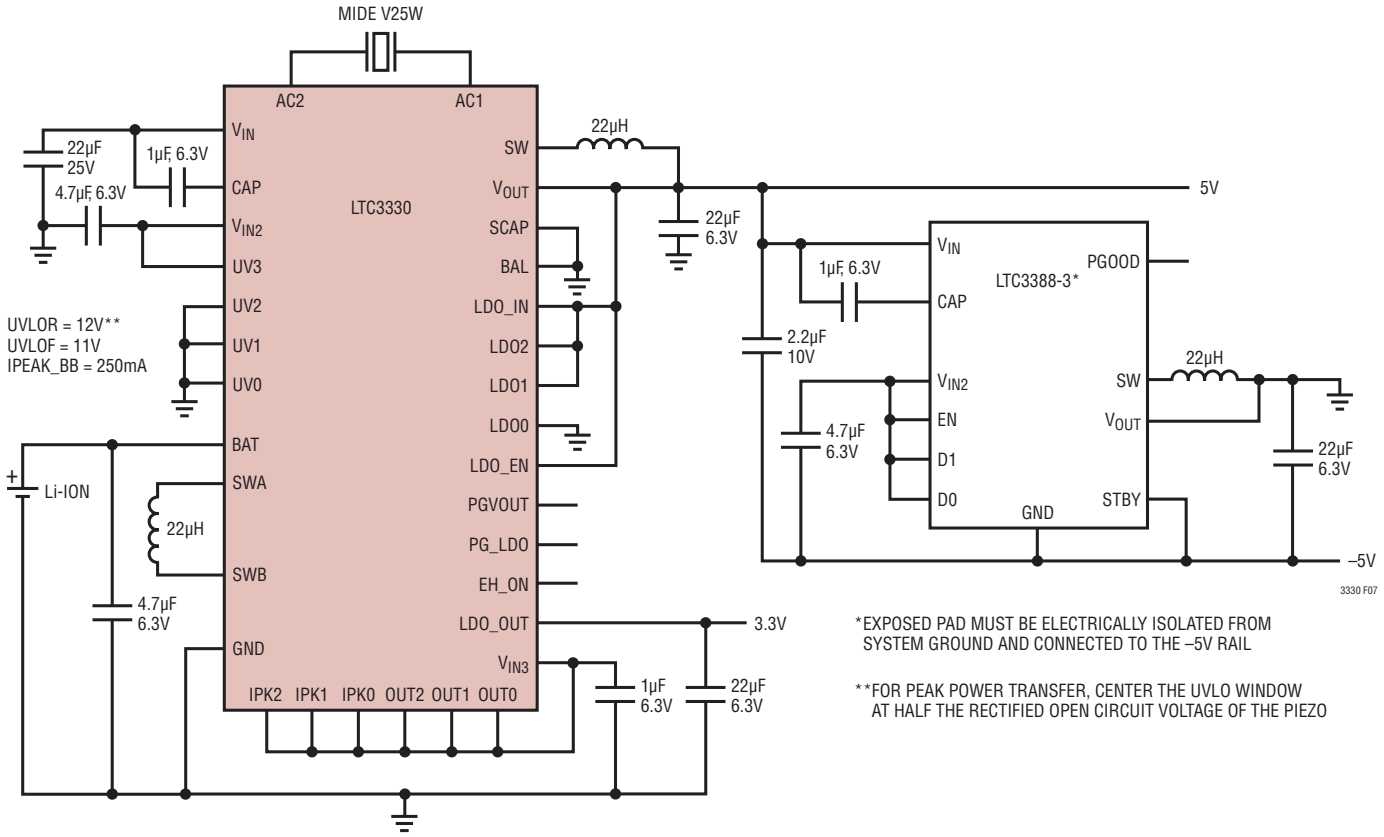


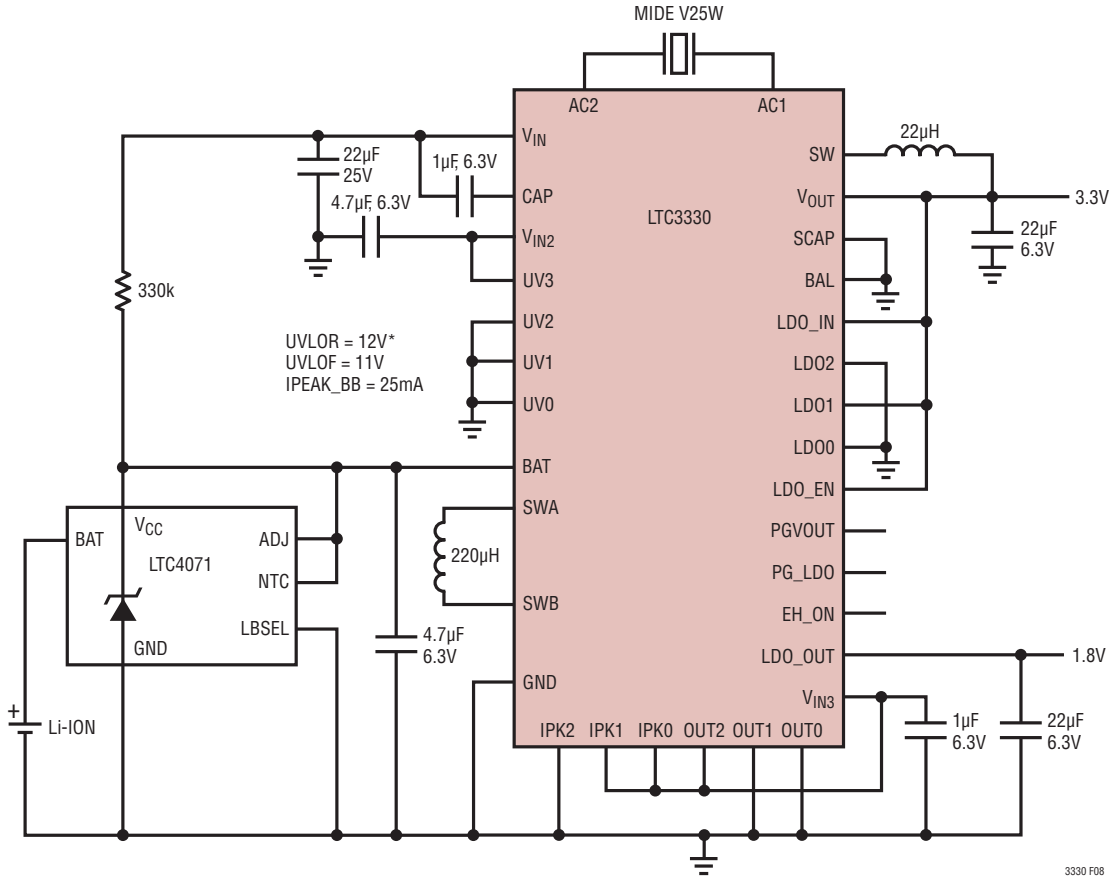
Figure 7. Dual ±5V Power Supply with a 3.3V LDO Output

APPLICATIONS

When paired with the 550nA LTC4071 shunt battery charger with low battery disconnect the LTC3330 can charge a battery from an energy harvesting source as shown in Figure 8. A battery is connected to the BAT pin of the LTC4071. If the battery voltage drops below a selected level the battery will be disconnected and protected from further discharge. A charging resistor is connected from V_{IN} of the LTC3330 to V_{CC} of the LTC4071 to create a charging path. V_{CC} is then the input to the LTC3330 buck-boost at the BAT pin. The charging resistor should be sized in accordance with the available energy from the energy harvesting source to allow the V_{IN} pin voltage of the LTC3330 to reach the UVLO rising threshold and prioritize powering the output at V_{OUT}.

Higher Efficiency Battery Powered Buck

If the battery voltage will always be higher than the regulated output of the LTC3330 then the battery powered buck-boost will always run in buck mode. In this case the inductor that is usually placed between SWA and SWB can go directly to V_{OUT} from SWA, bypassing internal switch M4 of the buck-boost (Figure 9). This will reduce conduction losses in the converter and improve the efficiency at higher loads.



*FOR PEAK POWER TRANSFER, CENTER THE UVLO WINDOW AT HALF THE RECTIFIED OPEN CIRCUIT VOLTAGE OF THE PIEZO

Figure 8. Energy Harvesting Battery Charger with Low Battery Disconnect