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High Current Supercapacitor Backup Controller and System Monitor

FEATURES

- **High Efficiency Synchronous Step-Down CC/CV Charging of One to Four Series Supercapacitors**
- **Step-Up Mode in Backup Provides Greater Utilization of Stored Energy in Supercapacitors**
- **14-Bit ADC for Monitoring System Voltages/Currents, Capacitance and ESR**
- **Active Overvoltage Protection Shunts**
- **Internal Active Balancers—No Balance Resistors**
- V_{IN}: 4.5V to 35V, $V_{CAP(n)}$: Up to 5V per Capacitor, Charge/Backup Current: 10+A
- Programmable Input Current Limit Prioritizes System Load Over Capacitor Charge Current
- Dual Ideal Diode PowerPath™ Controller
- All N-FET Charger Controller and PowerPath Controller
- Compact 38-Lead 5mm × 7mm QFN Package

APPLICATIONS

- High Current 12V Ride-Through UPS
- Servers/Mass Storage/High Availability Systems

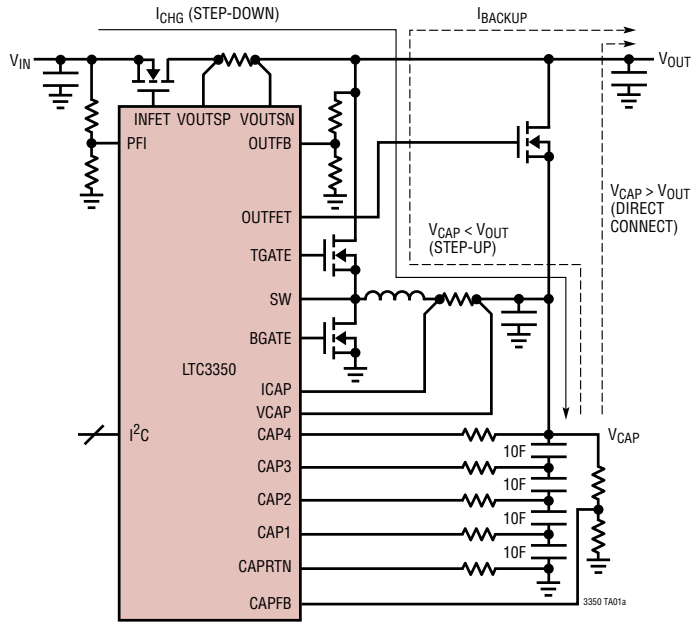
DESCRIPTION

The LTC®3350 is a backup power controller that can charge and monitor a series stack of one to four supercapacitors. The LTC3350's synchronous step-down controller drives N-channel MOSFETs for constant current/constant voltage charging with programmable input current limit. In addition, the step-down converter can run in reverse as a step-up converter to deliver power from the supercapacitor stack to the backup supply rail. Internal balancers eliminate the need for external balance resistors and each capacitor has a shunt regulator for overvoltage protection.

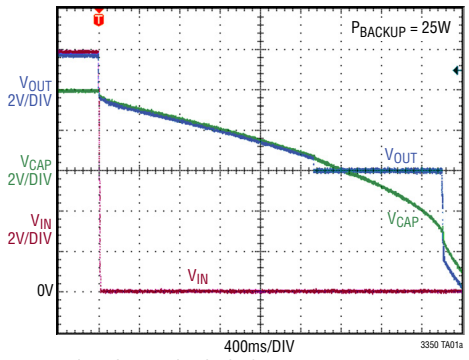
The LTC3350 monitors system voltages, currents, stack capacitance and stack ESR which can all be read over the I²C/SMBus. The dual ideal diode controller uses N-channel MOSFETs for low loss power paths from the input and supercapacitors to the backup system supply. The LTC3350 is available in a low profile 38-lead 5mm × 7mm × 0.75mm QFN surface mount package.

TYPICAL APPLICATION

High Current Supercapacitor Charger and Backup Supply



Backup Operation



BACK PAGE APPLICATION CIRCUIT

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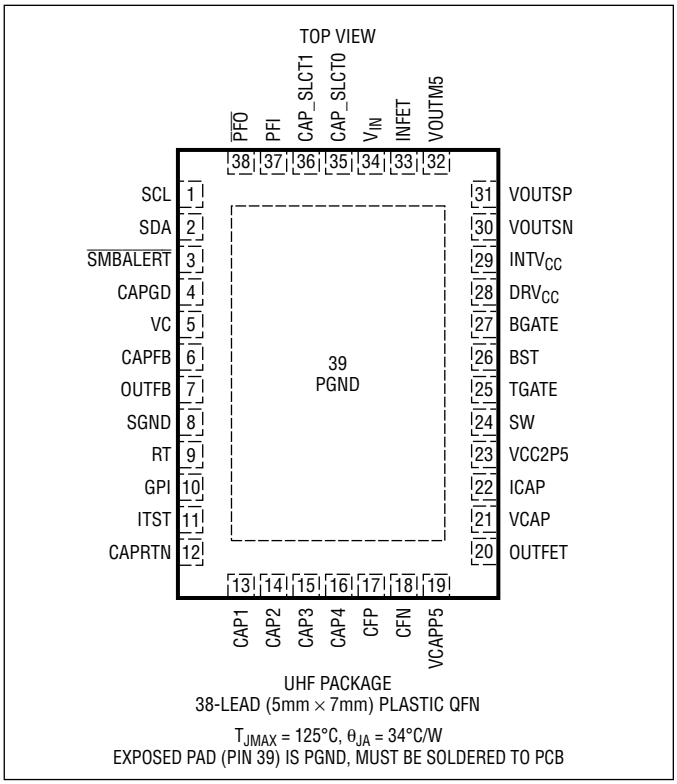
ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, VOUTSP, VOUTSN ..... –0.3V to 40V
VCAP ..... –0.3V to 22V
CAP4-CAP3, CAP3-CAP2, CAP2-CAP1,
CAP1-CAPRTN ..... –0.3V to 5.5V
DRV_{CC}, OUTFB, CAPFB, $\overline{SMBALERT}$, CAPGD,
$\overline{PFO}$, GPI, SDA, SCL ..... –0.3V to 5.5V
BST ..... –0.3V to 45.5V
PFI ..... –0.3V to 20V
CAP_SLCT0, CAP_SLCT1 .....–0.3 to 3V
BST to SW ..... –0.3V to 5.5V
VOUTSP to VOUTSN, ICAP to VCAP ..... –0.3V to 0.3V
I_{INTVCC} 100mA
$I_{CAP(1,2,3,4)}$, I_{CAPRTN} 600mA
I_{CAPGD}, $I_{\overline{PFO}}$, $I_{\overline{SMBALERT}}$ 10mA
Operating Junction Temperature Range
(Notes 2, 3).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3350EUHF#PBF	LTC3350EUHF#TRPBF	3350	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3350IUHF#PBF	LTC3350IUHF#TRPBF	3350	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator							
V_{IN}	Input Supply Voltage		●	4.5		35	V
I_Q	Input Quiescent Current (Note 4)				4		mA
$V_{CAPFBHI}$	Maximum Regulated V_{CAP} Feedback Voltage	V_{CAPDAC} Full Scale (1111b)	 ●	1.188 1.176	1.200 1.200	1.212 1.224	V V
$V_{CAPFBLO}$	Minimum Regulated V_{CAP} Feedback Voltage	V_{CAPDAC} Zero Scale (0000b)		0.628	0.638	0.647	V
I_{CAPFB}	CAPFB Input Leakage Current	V_{CAPFB} = 1.2V	●	–50		50	nA
V_{OUTFB}	Regulated V_{OUT} Feedback Voltage		 ●	1.188 1.176	1.200 1.200	1.212 1.224	V V
$V_{OUTFB(TH)}$	OUTFET Turn-Off Threshold	Falling Threshold		1.27	1.3	1.33	V
I_{OUTFB}	OUTFB Input Leakage Current	V_{OUTFB} = 1.2V	●	–50		50	nA
V_{OUTBST}	V_{OUT} Voltage in Step-Up Mode	V_{IN} = 0V	●	4.5		35	V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.85	4.3 4	4.45	V V
$V_{DRVUVLO}$	DRV_{CC} Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.75	4.2 3.9	4.35	V V
V_{DUVLO}	V_{IN} – V_{CAP} Differential Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	145 55	185 90	225 125	mV mV
V_{OVLO}	V_{IN} Overvoltage Lockout	Rising Threshold Falling Threshold	● ●	37.7 36.3	38.6 37.2	39.5 38.1	V V
V_{VCAPP5}	Charge Pump Output Voltage	Relative to V_{CAP}, 0V ≤ V_{CAP} ≤ 20V			5		V
Input Current Sense Amplifier							
V_{SNSI}	Regulated Input Current Sense Voltage (VOUTSP – VOUTSN)		 ●	31.36 31.04	32.00 32.00	32.64 32.96	mV mV
Charge Current Sense Amplifier							
V_{SNSC}	Regulated Charge Current Sense Voltage (ICAP – VCAP)	V_{CAP} = 10V	 ●	31.36 31.04	32.00 32.00	32.64 32.96	mV mV
V_{CMC}	Common Mode Range (ICAP, VCAP)			0		20	V
V_{PEAK}	Peak Inductor Current Sense Voltage		●	51	58	65	mV
V_{REV}	Reverse Inductor Current Sense Voltage	Step-Down Mode	●	3.867	7	10	mV
I_{ICAP}	ICAP Pin Current	Step-Down Mode, V_{SNSC} = 32mV Step-Up Mode, V_{SNSC} = 32mV			30 135		µA µA
Error Amplifier							
g_{MV}	V_{CAP} Voltage Loop Transconductance				1		mmho
g_{MC}	Charge Current Loop Transconductance				64		µmho
g_{MI}	Input Current Loop Transconductance				64		µmho
g_{MO}	V_{OUT} Voltage Loop Transconductance				400		µmho
Oscillator							
f_{SW}	Switching Frequency	R_T = 107k	 ●	495 490	500 500	505 510	kHz kHz
	Maximum Programmable Frequency	R_T = 53.6k			1		MHz
	Minimum Programmable Frequency	R_T = 267k			200		kHz

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DC_{MAX}	Maximum Duty Cycle	Step-Down Mode Step-Up Mode		97 87	98 93	99.5	% %
Gate Drivers							
R_{UP-TG}	TGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-TG}$	TGATE Pull-Down On-Resistance				0.6		Ω
R_{UP-BG}	BGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-BG}$	BGATE Pull-Down On-Resistance				0.6		Ω
t_{r-TG}	TGATE 10% to 90% Rise Time	C_{LOAD} = 3.3nF			18	25	ns
t_{f-TG}	TGATE 10% to 90% Fall Time	C_{LOAD} = 3.3nF			8	15	ns
t_{r-BG}	BGATE 10% to 90% Rise Time	C_{LOAD} = 3.3nF			18	25	ns
t_{f-BG}	BGATE 10% to 90% Fall Time	C_{LOAD} = 3.3nF			8	15	ns
t_{NO}	Non-Overlap Time				50		ns
$t_{ON(MIN)}$					85		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	5.2V ≤ V_{IN} ≤ 35V			5		V
ΔV_{INTVCC}	Load Regulation	I_{INTVCC} = 50mA			–1.5	–2.5	%
PowerPath/Ideal Diodes							
V_{FTO}	Forward Turn-On Voltage				65		mV
V_{FR}	Forward Regulation				30		mV
V_{RTO}	Reverse Turn Off				–30		mV
$t_{IF(ON)}$	INFET Rise Time	INFET – V_{IN} > 3V, C_{INFET} = 3.3nF			560		µs
$t_{IF(OFF)}$	INFET Fall Time	INFET – V_{IN} < 1V, C_{INFET} = 3.3nF			1.5		µs
$t_{OF(ON)}$	OUTFET Rise Time	OUTFET – V_{CAP} > 3V, C_{OUTFET} = 3.3nF			0.13		µs
$t_{OF(OFF)}$	OUTFET Fall Time	OUTFET – V_{CAP} < 1V, C_{OUTFET} = 3.3nF			0.26		µs
Power-Fail Comparator							
$V_{PFI(TH)}$	PFI Input Threshold (Falling Edge)		●	1.147	1.17	1.193	V
$V_{PFI(HYS)}$	PFI Hysteresis				30		mV
I_{PFI}	PFI Input Leakage Current	V_{PFI} = 0.5V	●	–50		50	nA
$V_{\overline{PFO}}$	$\overline{PFO}$ Output Low Voltage	I_{SINK} = 5mA			200		mV
$I_{\overline{PFO}}$	$\overline{PFO}$ High-Z Leakage Current	$V_{\overline{PFO}}$ = 5V	●			1	µA
	PFI Falling to $\overline{PFO}$ Low Delay				85		ns
	PFI Rising to $\overline{PFO}$ High Delay				0.4		µs
CAPGD							
$V_{CAPFB(TH)}$	CAPGD Rising Threshold as % of Regulated V_{CAP} Feedback Voltage	V_{capfb_dac} = Full Scale (1111b)	●	90	92	94	%
$V_{CAPFB(HYS)}$	CAPGD Hysteresis at CAPFB as a % of Regulated V_{CAP} Feedback Voltage	V_{capfb_dac} = Full Scale (1111b)			1.25		%
V_{CAPGD}	CAPGD Output Low Voltage	I_{SINK} = 5mA			200		mV
I_{CAPGD}	CAPGD High-Z Leakage Current	V_{CAPGD} = 5V	●			1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog-to-Digital Converter							
V_{RES}	Measurement Resolution				16		Bits
V_{GPI}	General Purpose Input Voltage Range	Unbuffered Buffered		0 0		5 3.5	V V
I_{GPI}	General Purpose Input Pin Leakage Current	Buffered Input				1	µA
R_{GPI}	GPI Pin Resistance	Buffer Disabled			2.5		MΩ
Measurement System Error							
V_{ERR}	Measurement Error (Note 5)	V_{IN} = 0V V_{IN} = 30V				100 1.5	mV %
		V_{OUTSP} = 5V V_{OUTSP} = 30V				100 1.5	mV %
		V_{CAP} = 0V V_{CAP} = 10V				100 1.5	mV %
		V_{GPI} = 0V, Unbuffered V_{GPI} = 3.5V, Unbuffered				2 1	mV %
		V_{CAP1} = 0V V_{CAP1} = 2V				2 1	mV %
		V_{CAP2} = 0V V_{CAP2} = 2V				2 1	mV %
		V_{CAP3} = 0V V_{CAP3} = 2V				2 1	mV %
		V_{CAP4} = 0V V_{CAP4} = 2V				2 1	mV %
		V_{SNSI} = 0mV V_{SNSI} = 32mV				200 2	µV %
		V_{SNSC} = 0mV V_{SNSC} = 32mV				200 2	µV %
CAP1 to CAP4							
R_{SHNT}	Shunt Resistance				0.5		Ω
DV_{CAPMAX}	Maximum Capacitor Voltage with Shunts Enabled	2 or More Capacitors in Stack				3.6	V
Programming Pins							
V_{ITST}	ITST Voltage	R_{TST} = 121Ω		1.185	1.197	1.209	V
I^2C/SMBus – SDA, SCL, $\overline{SMBALERT}$							
$I_{IL,SDA,SCL}$	Input Leakage Low			–1		1	µA
$I_{IH,SDA,SCL}$	Input Leakage High			–1		1	µA
V_{IH}	Input High Threshold			1.5			V
V_{IL}	Input Low Threshold					0.8	V
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	Low Period of SCL Clock			1.3			µs
t_{HIGH}	High Period of SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD,STA}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time After a Repeated Start Condition			0.6			µs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, V_{DRVCC} = V_{INTVCC} unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
$V_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ Output Low Voltage	I_{SINK} = 1mA			200		mV
$I_{\overline{SMBALERT}}$	$\overline{SMBALERT}$ High-Z Leakage Current	$V_{\overline{SMBALERT}}$ = 5V	●			1	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3350 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3350E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3350I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 34°C/W for the UHF package.

Note 3: The LTC3350 includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

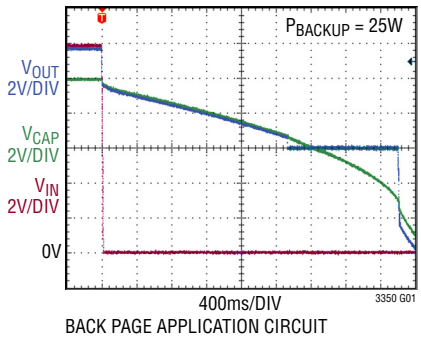
Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

Note 5: Measurement error is the magnitude of the difference between the actual measured value and the ideal value. V_{SNSI} is the voltage between VOUTSP and VOUTSN, representing input current. V_{SNSC} is the voltage between ICAP and VCAP, representing charge current. Error for V_{SNSI} and V_{SNSC} is expressed in µV, a conversion to an equivalent current may be made by dividing by the sense resistors, R_{SNSI} and R_{SNSC}, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS

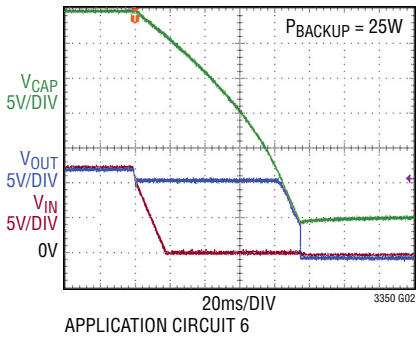
T_A = 25°C, Application Circuit 4 unless otherwise noted.

Supercapacitor Backup Operation



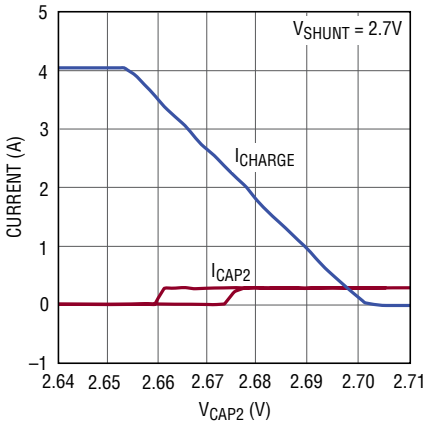
BACK PAGE APPLICATION CIRCUIT

HV Electrolytic Backup Operation



APPLICATION CIRCUIT 6

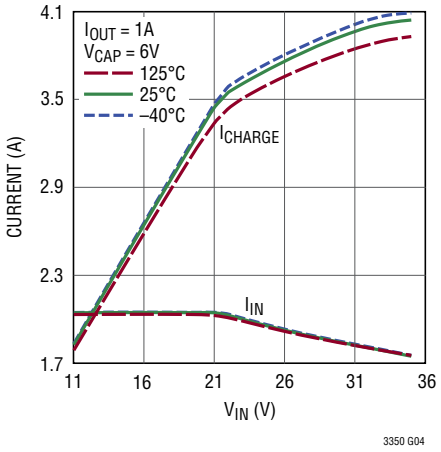
Shunt Operation Using V_{CAP2}



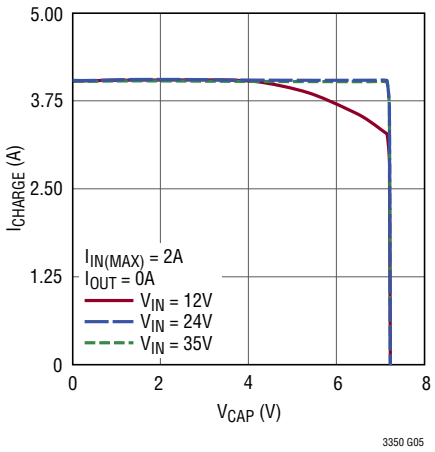
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, Application Circuit 4 unless otherwise noted.

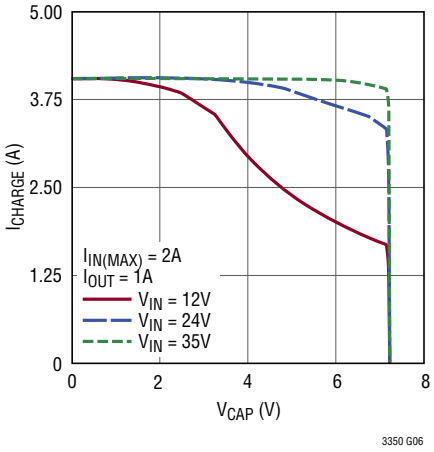
I_{IN} and I_{CHARGE} vs V_{IN}



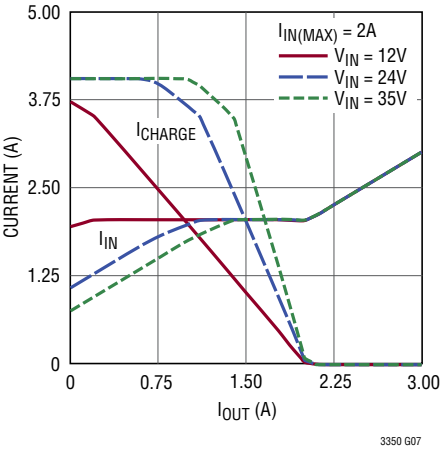
I_{CHARGE} vs V_{CAP}



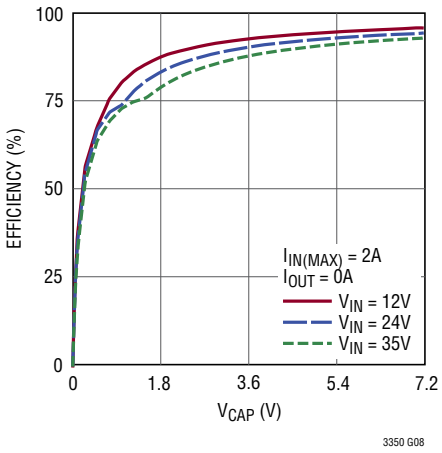
I_{CHARGE} vs V_{CAP}



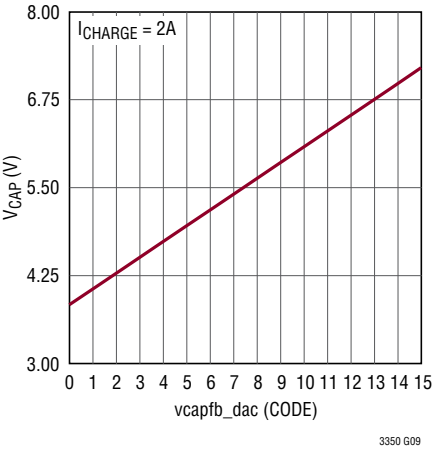
I_{IN} and I_{CHARGE} vs I_{OUT}



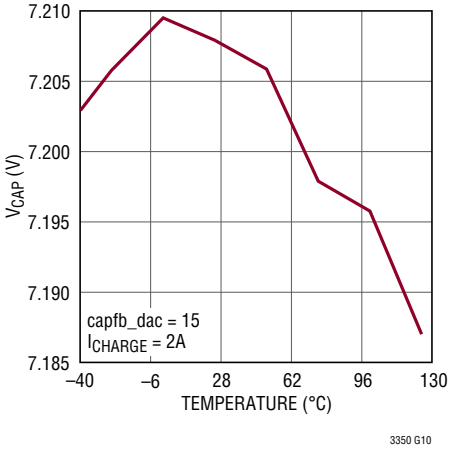
Charger Efficiency vs V_{CAP}



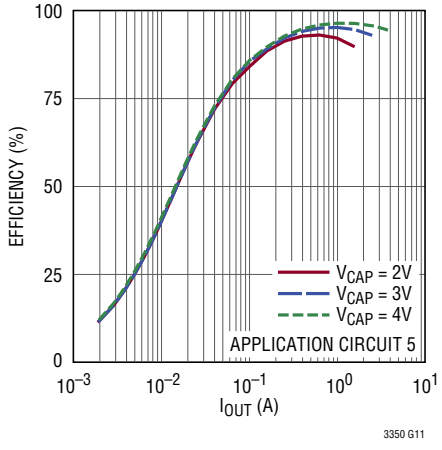
V_{CAP} vs vcapfb_dac



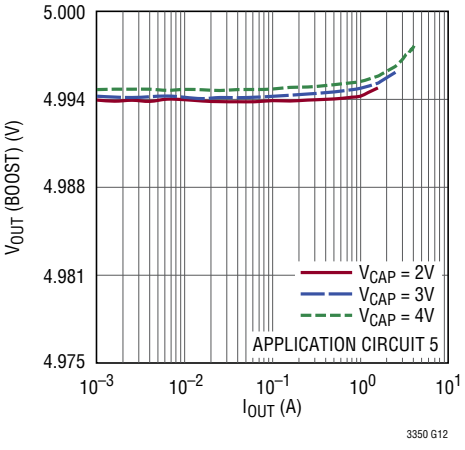
V_{CAP} vs Temperature



Efficiency in Boost Mode



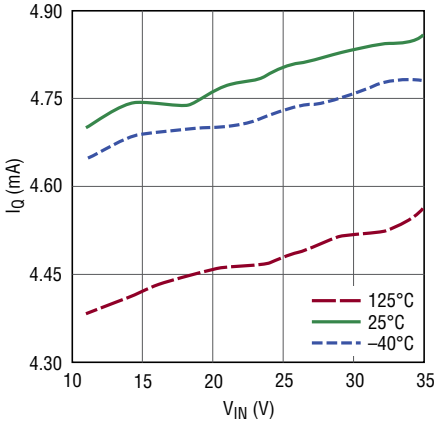
Load Regulation in Boost Mode



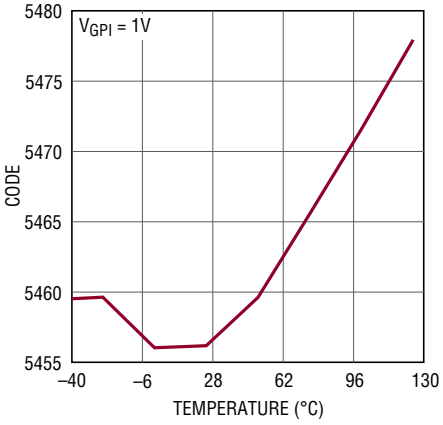
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, Application Circuit 4 unless otherwise noted.

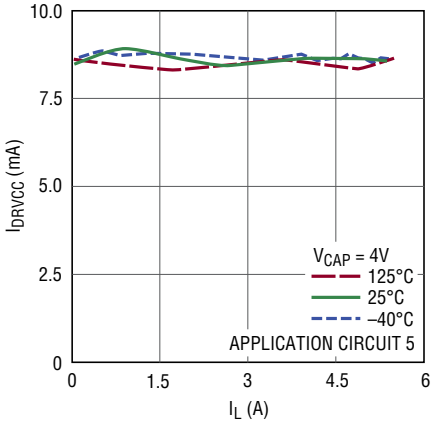
I_Q vs V_{IN}, Pulse Skipping



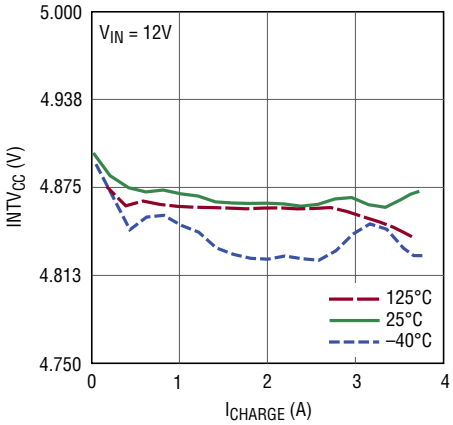
GPI Code vs Temperature



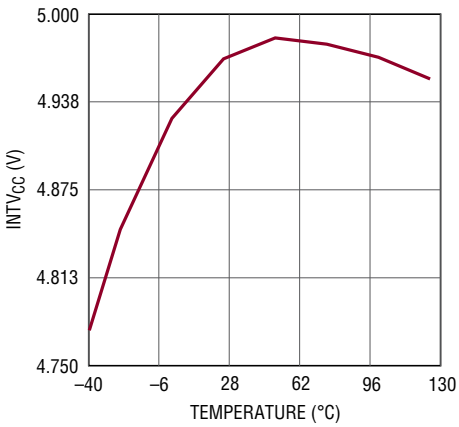
DRV_{CC} Current vs Boost Inductor Current



$INTV_{CC}$ vs Charge Current



$INTV_{CC}$ vs Temperature



PIN FUNCTIONS

SCL (Pin 1): Clock Pin for the I^2C/SMBus Serial Port.

SDA (Pin 2): Bidirectional Data Pin for the I^2C/SMBus Serial Port.

$\overline{\text{SMBALERT}}$ (Pin 3): Interrupt Output. This open-drain output is pulled low when an alarm threshold is exceeded, and will remain low until the acknowledgement of the part's response to an SMBus ARA.

CAPGD (Pin 4): Capacitor Power Good. This open-drain output is pulled low when CAPFB is below 92% of its regulation point.

VC (PIN 5): Control Voltage Pin. This is the compensation node for the charge current, input current, supercapacitor stack voltage and output voltage control loops. An RC network is connected between VC and SGND. Nominal voltage range for this pin is 1V to 3V.

CAPFB (Pin 6): Capacitor Stack Feedback Pin. This pin closes the feedback loop for constant voltage regulation. An external resistor divider between VCAP and SGND with the center tap connected to CAPFB programs the final supercapacitor stack voltage. This pin is nominally equal to the output of the V_{CAP} DAC when the synchronous controller is in constant voltage mode while charging.

OUTFB (Pin 7): Step-Up Mode Feedback Pin. This pin closes the feedback loop for voltage regulation of V_{OUT} during input power failure using the synchronous controller in step-up mode. An external resistor divider between V_{OUT} and SGND with the center tap connected to OUTFB programs the minimum backup supply rail voltage when input power is unavailable. This pin is nominally 1.2V when in backup and the synchronous controller is not in current limit. To disable step-up mode tie OUTFB to $INTV_{CC}$.

SGND (Pin 8): Signal Ground. All small-signal and compensation components should be connected to this pin, which in turn connects to PGND at one point. This pin should also Kelvin to the bottom plate of the capacitor stack.

RT (Pin 9): Timing Resistor. The switching frequency of the synchronous controller is set by placing a resistor, R_T, from this pin to SGND. This resistor is always required. If not present the synchronous controller will not start.

GPI (Pin 10): General Purpose Input. The voltage on this pin is digitized directly by the ADC. For high impedance inputs an internal buffer can be selected and used to drive the ADC. The GPI pin can be connected to a negative temperature coefficient (NTC) thermistor to monitor the temperature of the supercapacitor stack. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used. The digitized voltage on this pin can be read in the meas_gpi register.

ITST (Pin 11): Programming Pin for Capacitance Test Current. This current is used to partially discharge the capacitor stack at a precise rate for capacitance measurement. This pin servos to 1.2V during a capacitor measurement. A resistor, R_{TST}, from this pin to SGND programs the test current. R_{TST} must be at least 121Ω.

CAPRTN (Pin 12): Capacitor Stack Shunt Return Pin. This pin is connected to the grounded bottom plate of the first super capacitor in the stack through a shunt resistor.

CAP1 (Pin 13): First Supercapacitor Pin. The top plate of the first supercapacitor and the bottom plate of the second supercapacitor are connected to this pin through a shunt resistor. CAP1 and CAPRTN are used to measure the voltage across the first super capacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. The voltage between this pin and CAPRTN is digitized and can be read in the meas_vcap1 register.

CAP2 (Pin 14): Second Supercapacitor Pin. The top plate of the second supercapacitor and the bottom plate of the third supercapacitor are connected to this pin through a shunt resistor. CAP2 and CAP1 are used to measure the voltage across the second supercapacitor and to shunt

PIN FUNCTIONS

current around the capacitor to provide balancing and prevent overvoltage. If not used this pin should be shorted to CAP1. The voltage between this pin and CAP1 is digitized and can be read in the meas_vcap2 register.

CAP3 (Pin 15): Third Supercapacitor Pin. The top plate of the third supercapacitor and the bottom plate of the fourth supercapacitor are connected to this pin through a shunt resistor. CAP3 and CAP2 are used to measure the voltage across the third supercapacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. If not used this pin should be shorted to CAP2. The voltage between this pin and CAP2 is digitized and can be read in the meas_vcap3 register.

CAP4 (Pin 16): Fourth Supercapacitor Pin. The top plate of the fourth supercapacitor is connected to this pin through a shunt resistor. CAP4 and CAP3 are used to measure the voltage on the capacitor and to shunt current around the supercapacitor to provide balancing and prevent overvoltage. If not used this pin should be shorted to CAP3. The voltage between this pin and CAP3 is digitized and can be read in the meas_vcap4 register. The capacitance test current set by the ITST pin is pulled from this pin.

CFP (Pin 17): VCAPP5 Charge Pump Flying Capacitor Positive Terminal. Place a 0.1µF between CFP and CFN.

CFN (Pin 18): VCAPP5 Charge Pump Flying Capacitor Negative Terminal. Place a 0.1µF between CFP and CFN.

VCAPP5 (Pin 19): Charge Pump Output. The internal charge pump drives this pin to VCAP + $INTV_{CC}$ which is used as the high side rail for the OUTFET gate drive and charge current sense amplifier. Connect a 0.1µF capacitor from VCAPP5 to VCAP.

OUTFET (Pin 20): Output Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{OUT} and V_{CAP}. The gate drive receives power from the internal charge pump output VCAPP5. The source of the N-channel MOSFET should be connected to VCAP and the drain should be connected to VOUTSN. If the output ideal diode MOSFET is not used, OUTFET should be left floating.

VCAP (Pin 21): Supercapacitor Stack Voltage and Charge Current Sense Amplifier Negative Input. Connect this pin to the top of the supercapacitor stack. The voltage at this pin is digitized and can be read in the meas_vcap register.

ICAP (Pin 22): Charge Current Sense Amplifier Positive Input. The ICAP and VCAP pins measure the voltage across the sense resistor, R_{SNSC}, to provide instantaneous current signals for the control loops and ESR measurement system. The maximum charge current is $32mV/R_{SNSC}$.

VCC2P5 (Pin 23): Internal 2.5V Regulator Output. This regulator provides power to the internal logic circuitry. Decouple this pin to ground with a minimum 1µF low ESR tantalum or ceramic capacitor.

SW (Pin 24): Switch Node Connection to the Inductor. The negative terminal of the boot-strap capacitor, C_B, is connected to this pin. The voltage on this pin is also used as the source reference for the top side N-channel MOSFET gate drive. In step-down mode, the voltage swing on this pin is from a diode (external) forward voltage below ground to V_{OUT}. In step-up mode the voltage swing is from ground to a diode forward voltage above V_{OUT}.

TGATE (Pin 25): Top Gate Driver Output. This pin is the output of a floating gate driver for the top external N-channel MOSFET. The voltage swing at this pin is ground to V_{OUT} + DRV_{CC}.

BST (Pin 26): TGATE Driver Supply Input. The positive terminal of the boot-strap capacitor, C_B, is connected to this pin. This pin swings from a diode voltage drop below DRV_{CC} up to V_{OUT} + DRV_{CC}.

BGATE (Pin 27): Bottom Gate Driver Output. This pin drives the bottom external N-channel MOSFET between PGND and DRV_{CC}.

DRV_{CC} (Pin 28): Power Rail for Bottom Gate Driver. Connect to $INTV_{CC}$ or to an external supply. Decouple this pin to ground with a minimum 2.2µF low ESR tantalum or ceramic capacitor. Do not exceed 5.5V on this pin.

PIN FUNCTIONS

$INTV_{CC}$ (Pin 29): Internal 5V Regulator Output. The control circuits and gate drivers (when connected to DRV_{CC}) are powered from this supply. If not connected to DRV_{CC}, decouple this pin to ground with a minimum 1µF low ESR tantalum or ceramic capacitor.

VOUTSN (Pin 30): Input Current Limiting Amplifier Negative Input. A sense resistor, R_{SNSI}, between VOUTSP and VOUTSN sets the input current limit. The maximum input current is $32mV/R_{SNSI}$. An RC network across the sense resistor can be used to modify loop compensation. To disable input current limit, connect this pin to VOUTSP.

VOUTSP (Pin 31): Backup System Supply Voltage and Input Current Limiting Amplifier Positive Input. The voltage across the VOUTSP and VOUTSN pins are used to regulate input current. This pin also serves as the power supply for the IC. The voltage at this pin is digitized and can be read in the meas_vout register.

VOUTM5 (Pin 32): V_{OUT} – 5V Regulator. This pin is regulated to 5V below V_{OUT} or to ground if V_{OUT} < 5V. This rail provides power to the input current sense amplifier. Decouple this pin with at least 1µF to V_{OUT}.

INFET (Pin 33): Input Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{IN} and V_{OUT}. The gate drive receives power from an internal charge pump. The source of the N-channel MOSFET should be connected to V_{IN} and the drain should be connected to VOUTSP. If the input ideal diode MOSFET is not used, INFET should be left floating.

V_{IN} (Pin 34): External DC Power Source Input. Decouple this pin with at least 0.1µF to ground. The voltage at this pin is digitized and can be read in the meas_vin register.

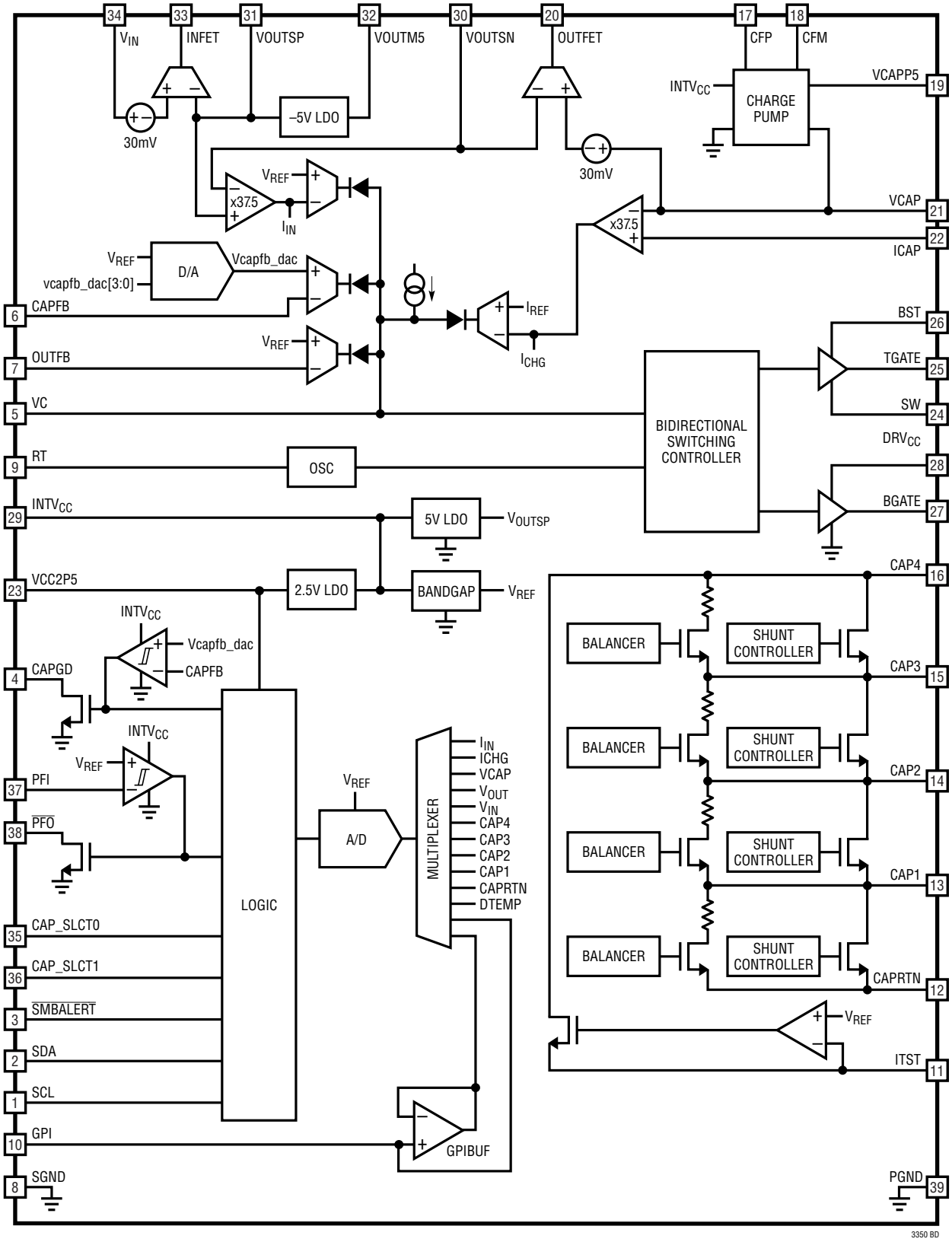
CAP_SLCT0, CAP_SLCT1 (Pins 35, 36): CAP_SLCT0 and CAP_SLCT1 set the number of super-capacitors used. Refer to Table 1 in the Applications Information section.

PFI (Pin 37): Power-Fail Comparator Input. When the voltage at this pin drops below 1.17V, $\overline{PFO}$ is pulled low and step-up mode is enabled.

$\overline{PFO}$ (Pin 38): Power-Fail Status Output. This open-drain output is pulled low when a power fault has occurred.

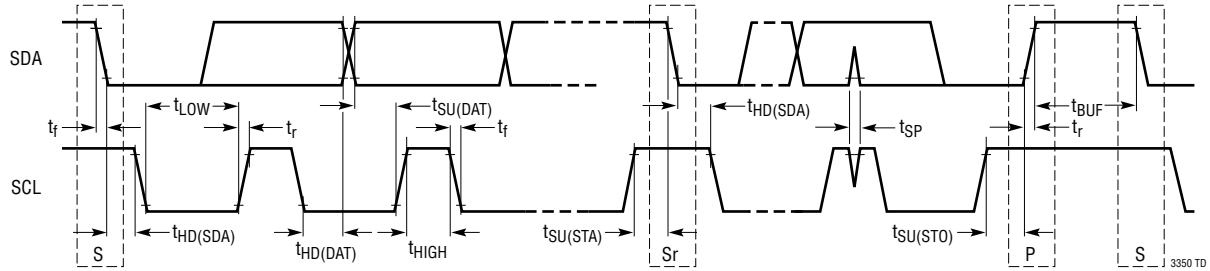
PGND (Exposed Pad Pin 39): Power Ground. The exposed pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3350 for rated thermal performance. It must be tied to the SGND pin.

BLOCK DIAGRAM



TIMING DIAGRAM

Definition of Timing for F/S Mode Devices on the I²C Bus



S = START, Sr = REPEATED START, P = STOP

OPERATION

Introduction

The LTC3350 is a highly integrated backup power controller and system monitor. It features a bidirectional switching controller, input and output ideal diodes, supercapacitor shunts/balancers, a power-fail comparator, a 14-bit ADC and I²C/SMBus programmability with status reporting.

If V_{IN} is above an externally programmable PFI threshold voltage, the synchronous controller operates in step-down mode and charges a stack of supercapacitors. A programmable input current limit ensures that the supercapacitors will automatically be charged at the highest possible charge current that the input can support. If V_{IN} is below the PFI threshold, then the synchronous controller will run in reverse as a step-up converter to deliver power from the supercapacitor stack to V_{OUT}.

The two ideal diode controllers drive external MOSFETs to provide low loss power paths from V_{IN} and V_{CAP} to V_{OUT}. The ideal diodes work seamlessly with the bidirectional controller to provide power from the supercapacitors to V_{OUT} without backdriving V_{IN}.

The LTC3350 provides balancing and overvoltage protection to a series stack of one to four supercapacitors. The internal capacitor voltage balancers eliminate the need for external balance resistors. Overvoltage protection is provided by shunt regulators that use an internal switch and an external resistor across each supercapacitor.

The LTC3350 monitors system voltages, currents, and die temperature. A general purpose input (GPI) pin is provided to measure an additional system parameter or implement a thermistor measurement. In addition, the LTC3350 can measure the capacitance and resistance of the supercapacitor stack. This provides indication of the health of the supercapacitors and, along with the V_{CAP} voltage measurement, provides information on the total energy stored and the maximum power that can be delivered.

Bidirectional Switching Controller—Step-Down Mode

The bidirectional switching controller is designed to charge a series stack of supercapacitors (Figure 1). Charging proceeds at a constant current until the supercapacitors reach their maximum charge voltage determined by the CAPFB servo voltage and the resistor divider between V_{CAP} and CAPFB. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, used in series with the inductor. The charge current loop servos the voltage across the sense resistor to 32mV. When charging begins, an internal soft-start ramp will increase the charge current from zero to full current in 2ms. The V_{CAP} voltage and charge current can be read from the meas_vcap and meas_ichrg registers, respectively.

OPERATION

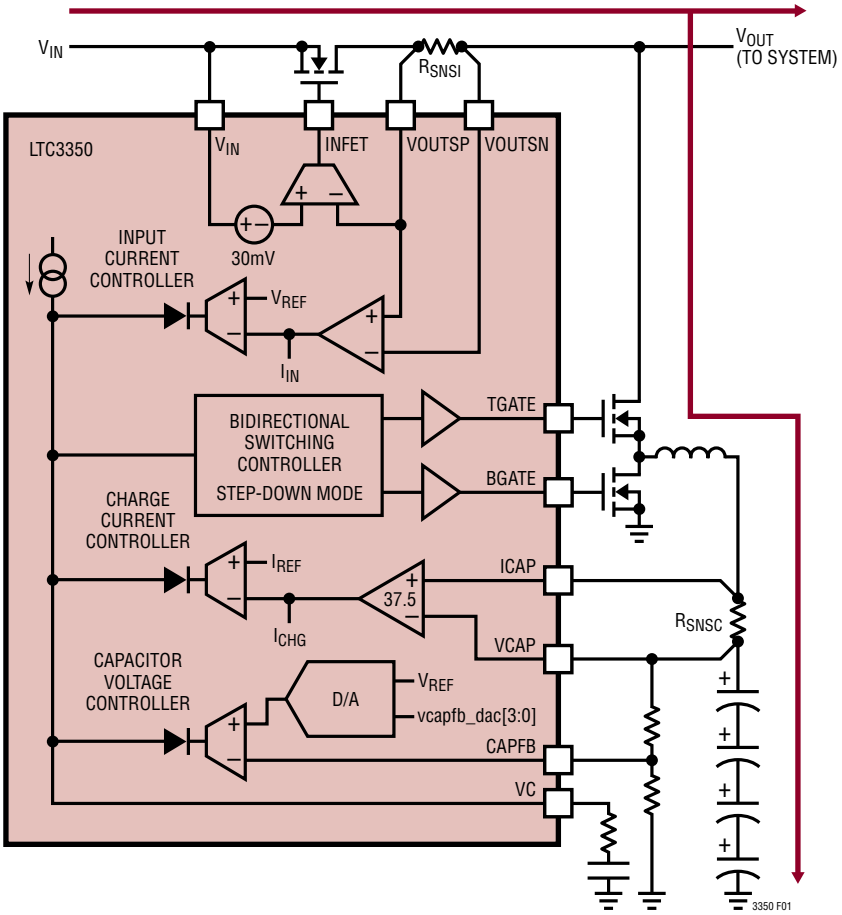


Figure 1. Power Path Block Diagram—Power Available from V_{IN}

The LTC3350 provides constant power charging (for a fixed V_{IN}) by limiting the input current drawn by the switching controller in step-down mode. The input current limit will reduce charge current to limit the voltage across the input sense resistor, R_{SNSI}, to 32mV. If the combined system load plus supercapacitor charge current is large enough to cause the switching controller to reach the programmed input current limit, the input current limit loop will reduce the charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the charge current is programmed to exceed the allowable input current, the input current will not be violated; the supercapacitor charger will reduce its current as needed. Note that the part's quiescent and gate drive currents are not included in the input current measurement.The input current can be read from the meas_iin register.

Bidirectional Switching Controller—Step-Up Mode

The bidirectional switching controller acts as a step-up converter to provide power from the supercapacitors to V_{OUT} when input power is unavailable (Figure 2). The PFI comparator enables step-up mode. V_{OUT} regulation is set by a resistor divider between V_{OUT} and OUTFB. To disable step-up mode tie OUTFB to $INTV_{CC}$.

Step-up mode can be used in conjunction with the output ideal diode. The V_{OUT} regulation voltage can be set below the capacitor stack voltage. Upon removal of input power, power to V_{OUT} will be provided from the supercapacitor stack via the output ideal diode. V_{CAP} and V_{OUT} will fall as the load current discharges the supercapacitor stack. The output ideal diode will shut off when the voltage on OUTFB falls below 1.3V and V_{OUT} will fall a PN diode (~700mV) below V_{CAP}. If OUTFB falls below 1.2V when the output

OPERATION

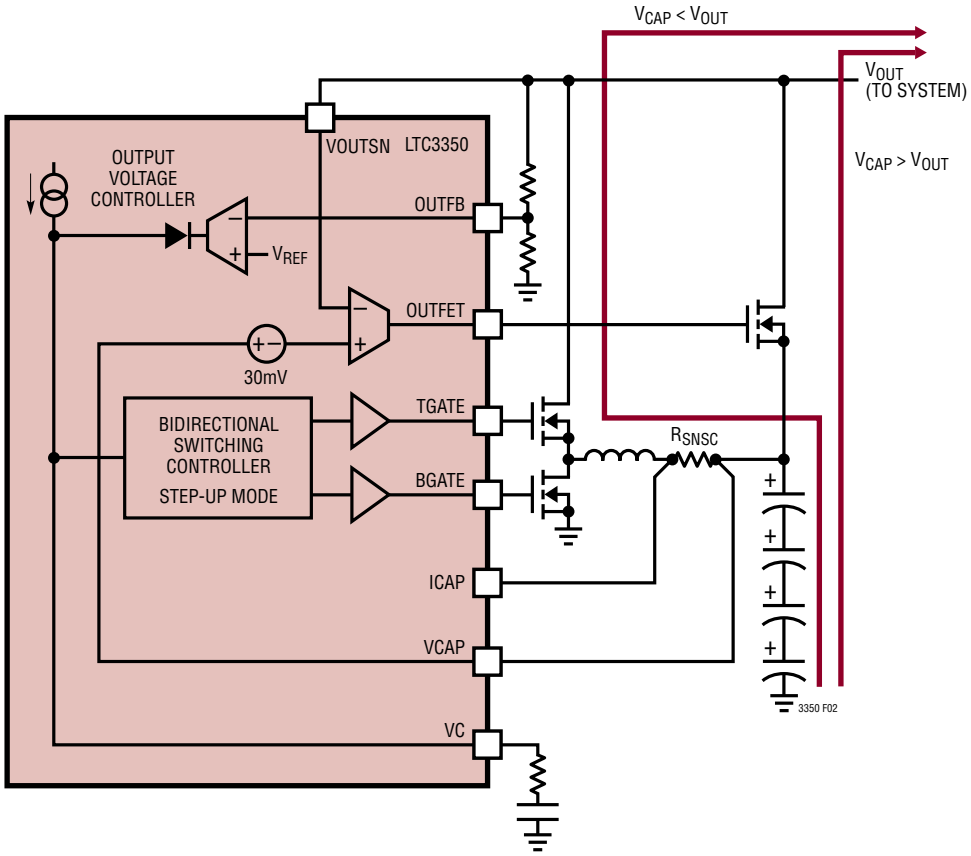


Figure 2. Power Path Block Diagram—Power Backup

ideal diode shuts off, the synchronous controller will turn on immediately. If OUTFB is above 1.2V when the output ideal diode shuts off, the load current will flow through the body diode of the output ideal diode N-channel MOSFET for a period of time until OUTFB falls to 1.2V. The synchronous controller will regulate OUTFB to 1.2V when it turns on, holding up V_{OUT} while the supercapacitors discharge to ground.

The synchronous controller in step-up mode will run nonsynchronously when V_{CAP} is less than 100mV below V_{OUT}. It will run synchronously when V_{CAP} falls 200mV below V_{OUT}.

Ideal Diodes

The LTC3350 has two ideal diode controllers that drive external N-channel MOSFETs. The ideal diodes consist of a precision amplifier that drives the gates of N-channel MOSFETs whenever the voltage at V_{OUT} is approximately 30mV (V_{FWD}) below the voltage at V_{IN} or V_{CAP}. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 30mV. At higher current levels, the MOSFETs will be in full conduction.

The input ideal diode prevents the supercapacitors from back driving V_{IN} during backup mode. A Fast-Off comparator shuts off the N-channel MOSFET if V_{IN} falls 30mV below V_{OUT}. The PFI comparator also shuts off the MOSFET during power failure.

The output ideal diode provides a path for the supercapacitors to power V_{OUT} when V_{IN} is unavailable. In addition to a Fast-Off comparator, the output ideal diode also has a Fast-On comparator that turns on the external MOSFET when V_{OUT} drops 65mV below V_{CAP}. The output ideal diode will shut off when OUTFB is just above regulation allowing the synchronous controller to power V_{OUT} in step-up mode.

OPERATION

Gate Drive Supply (DRV_{CC})

The bottom gate driver is powered from the DRV_{CC} pin. It is normally connected to the $INTV_{CC}$ pin. An external LDO can also be used to power the gate drivers to minimize power dissipation inside the IC. See the Applications Information section for details.

Undervoltage Lockout (UVLO)

Internal undervoltage lockout circuits monitor both the $INTV_{CC}$ and DRV_{CC} pins. The switching controller is kept off until $INTV_{CC}$ rises above 4.3V and DRV_{CC} rises above 4.2V. Hysteresis on the UVLOs turn off the controller if either $INTV_{CC}$ falls below 4V or DRV_{CC} falls below 3.9V.

Charging is not enabled until VOUTSN is 185mV above the supercapacitor voltage and V_{IN} is above the PFI threshold. Charging is disabled when VOUTSN falls to within 90mV of the supercapacitor voltage or V_{IN} is below the PFI threshold.

RT Oscillator and Switching Frequency

The RT pin is used to program the switching frequency. A resistor, R_T, from this pin to ground sets the switching frequency according to:

$$f_{SW}\,(MHz) = \frac{53.5}{R_T\,(k\Omega)}$$

R_T also sets the scale factor for the capacitor measurement value reported in the meas_cap register, described in the Capacitance and ESR Measurement section of this data sheet.

Input Overvoltage Protection

The LTC3350 has overvoltage protection on its input. If V_{IN} exceeds 38.6V, the switching controller will hold the switching MOSFETs off. The controller will resume switching if V_{IN} falls below 37.2V. The input ideal diode MOSFET remains on during input overvoltage.

V_{CAP} DAC

The feedback reference for the CAPFB servo point can be programmed using an internal 4-bit digital-to-analog converter (DAC). The reference voltage can be programmed from 0.6375V to 1.2V in 37.5mV increments. The DAC defaults to full scale (1.2V) and is programmed via the vcapfb_dac register.

Supercapacitors lose capacitance as they age. By initially setting the V_{CAP} DAC to a low setting, the final charge voltage on the supercapacitors can be increased as they age to maintain a constant level of stored backup energy throughout the lifetime of the supercapacitors.

Power-Fail (PF) Comparator

The LTC3350 contains a fast power-fail (PF) comparator which switches the part from charging to backup mode in the event the input voltage, V_{IN}, falls below an externally programmed threshold voltage. In backup mode, the input ideal diode shuts off and the supercapacitors power the load either directly through the output ideal diode or through the synchronous controller in step-up mode.

The PF comparator threshold voltage is programmed by an external resistor divider via the PFI pin. The output of the PF comparator also drives the gate of an open-drain NMOS transistor to report the status via the $\overline{PFO}$ pin. When input power is available the $\overline{PFO}$ pin is high impedance. When V_{IN} falls below the PF comparator threshold, $\overline{PFO}$ is pulled down to ground.

The output of the PF comparator may also be read from the chrg_pfo bit in the chrg_status register.

Charge Status Indication

The LTC3350 includes a comparator to report the status of the supercapacitors via an open-drain NMOS transistor on the CAPGD pin. This pin is pulled to ground until the CAPFB pin voltage rises to within 8% of the V_{CAP} DAC setting. Once the CAPFB pin is above this threshold, the CAPGD pin goes high impedance.

The output of this comparator may also be read from the chrg_cappg bit in the chrg_status register.

Capacitor Voltage Balancer

The LTC3350 has an integrated active stack balancer. This balancer slowly balances all of the capacitor voltages to within about 10mV of each other. This maximizes the life of the supercapacitors by keeping the voltage on each as low as possible to achieve the needed total stack voltage.

OPERATION

When the difference between any two capacitor voltages exceeds about 10mV, the capacitor with the largest voltage is discharged with a resistive balancer at about 10mA until all capacitor voltages are within 10mV. The balancers are disabled in backup mode.

Capacitor Shunt Regulators

In addition to balancing, there is a need to protect each capacitor from overvoltage during charging. The capacitors in the stack will not have exactly the same capacitance due to manufacturing tolerances or uneven aging. This will cause the capacitor voltages to increase at different rates with the same charge current. If this mismatch is severe enough or if the capacitors are being charged to near their maximum voltage, it becomes necessary to limit the voltage increase on some capacitors while still charging the other capacitors. Up to 500mA of current may be shunted around a capacitor whose voltage is approaching the programmable shunt voltage. This shunt current reduces the charge rate of that capacitor relative to the other capacitors. If a capacitor continues to approach its shunt voltage, the charge current is reduced. This protects the capacitor from overvoltage while still charging the other capacitors, although at a reduced rate of charge. The shunt voltage is programmable in the vshunt register. Shunt voltages up to 3.6V may be programmed in 183.5µV increments. The shunt regulators can be disabled by programming vshunt to zero (0x0000). The default value is 0x3999, resulting in a shunt voltage of 2.7V.

I²C/SMBus and SMBALERT

The LTC3350 contains an I²C/SMBus port. This port allows communication with the LTC3350 for configuration and reading back telemetry data. The port supports two SMBus formats, read word and write word. Refer to the SMBus specification for details of these formats. The registers accessible via this port are organized on an 8-bit address bus and each register is 16 bits wide. The "command code" (or sub-address) of the SMBus read/write word formats is the 8-bit address of each of these registers. The address of the LTC3350 is 0b0001001.

The $\overline{\text{SMBALERT}}$ pin is asserted (pulled low) whenever an enabled limit is exceeded or when an enabled status event happens (see Limit Check and Alarms and Monitor Status Register). The LTC3350 will deassert the $\overline{\text{SMBALERT}}$ pin only after responding to an SMBus alert response address (ARA), an SMBus protocol used to respond to a SMBALERT. The host will read from the ARA (0b0001100) and each part asserting SMBALERT will begin to respond with its address. The responding parts arbitrate in such a way that only the part with the lowest address responds. Only when a part has responded with its address does it release the SMBALERT signal. If multiple parts are asserting the SMBALERT signal then multiple reads from the ARA are needed. For more information refer to the SMBus specification.

Details on the registers accessible through this interface are available in the Register Map and Register Descriptions sections of this data sheet.

Analog-to-Digital Converter

The LTC3350 has an integrated 14-bit sigma-delta analog-to-digital converter (ADC). This converter is automatically multiplexed between all of the measured channels and its results are stored in registers accessible via the I²C/SMBus port. There are 11 channels measured by the ADC, each of which takes approximately 1.6ms to measure. In addition to providing status information about the system voltages and currents, some of these measurements are used by the LTC3350 to balance, protect, and measure the capacitors in the stack.

The result of the analog-to-digital conversion is stored in a 16-bit register as a signed, two's complement number. The lower two bits of this number are sub-bits. These bits are ADC outputs which are too noisy to be reliably used on any single conversion, however, they may be included if multiple samples are averaged.

The measurements from the ADC are directly stored in the meas_vcap1, meas_vcap2, meas_vcap3, meas_vcap4, meas_gpi, meas_vin, meas_vcap, meas_vout, meas_iin, meas_ichg and meas_dtemp registers.

Capacitance and ESR Measurement

The LTC3350 has the ability to measure the capacitance and equivalent series resistance (ESR) of its supercapacitor

OPERATION

stack. This measurement is performed with minimal impact to the system, and can be done while the supercapacitor backup system is online. This measurement discharges the capacitor stack by a small amount (200mV). If input power fails during this test, the part will go into backup mode and the test will terminate.

The capacitance test is performed only once the supercapacitors have finished charging. The test temporarily disables the charger, then discharges the supercapacitors by 200mV with a precision current. The discharge time is measured and used to calculate the capacitance with the result of this measurement stored in the meas_cap register. The number reported is proportional to the capacitance of the entire stack. Two different scales can be set using the ctl_cap_scale bit in the ctl_reg register. If ctl_cap_scale is set to 0 (for large value capacitor stacks), use the following equation to convert the meas_cap value to Farads:

$$C_{STACK} = \frac{R_T}{R_{TST}} \bullet 336\mu F \bullet meas\_cap$$

If ctl_cap_scale is set to 1 (for small value capactor stacks), use the following equation to convert the meas_cap value to Farads:

$$C_{STACK} = \frac{R_T}{R_{TST}} \bullet 3.36\mu F \bullet meas\_cap$$

In the two previous equations R_T is the resistor on the RT pin and R_{TST} is the resistor on the ITST pin.

The ESR test is performed immediately following the capacitance test. The switching controller is switched on and off several times. The changes in charge current and stack voltage are measured. These measurements are used to calculate the ESR relative to the charge current sense resistor. The result of this measurement is stored in the meas_esr register. The value reported in meas_esr can be converted to ohms using the following equation:

$$R_{ESR} = \frac{R_{SNSC}}{64} \bullet meas\_esr$$

where R_{SNSC} is the charge current sense resistor in series with the inductor.

The capacitance and capacitor ESR measurements do not automatically run as the other measurements do. They must be initiated by setting the ctl_strt_capesr bit in the ctl_reg register. This bit will automatically clear once the measurement begins. If the cap_esr_per register is set to a non-zero value, the measurement will be repeated after the time programmed in the cap_esr_per register. Each LSB in the cap_esr_per register represents 10 seconds.

The capacitance and ESR measurements may fail to complete for several reasons, in which case the respective mon_cap_failed or mon_esr_failed bit will be set. The capacitance test may fail due to a power failure or if the 200mV discharge trips the CAPGD comparator. The ESR test will also fail if the capacitance test fails. The ESR test uses the charger to supply a current and then measures the supercapacitor stack voltage with and without that current. If the ESR is greater than 1024 times R_{SNSC}, the ESR measurement will fail. The ESR measurement is adaptive; it uses knowledge of the ESR from previous measurements to program the test current. The capacitance and ESR tests should initially be run several times when first powering up to get the most accuracy out of the system. It is possible for the first few measurements to give low quality results or fail to complete and after running several times will complete with a quality result. The leakage on supercapacitors is initially very high after being charged. Many supercapacitor manufacturers specify the leakage current after being charged for 72 hours. It is expected that capacitor measurements conducted prior to this time will read low.

Monitor Status Register

The LTC3350 has a monitor status register (mon_status) which contains status bits indicating the state of the capacitance and ESR monitoring system. These bits are set and cleared by the capacitor monitor upon certain events during a capacitor and ESR measurement, as described in the Capacitance and ESR Measurement section.

There is a corresponding msk_mon_status register. Writing a one to any of these bits will cause the $\overline{\text{SMBALERT}}$ pin to pull low when the corresponding bit in the msk_mon_status register has a rising edge. This allows reduced polling of the LTC3350 when waiting for a capacitance or ESR measurement to complete.

OPERATION

Details of the mon_status and msk_mon_status registers can be found in the Register Descriptions section of this data sheet.

Charge Status Register

The LTC3350 charger status register (chrg_status) contains data about the state of the charger, switcher, shunts, and balancers. Details of this register may be found in the Register Description sections of this data sheet.

Limit Checking and Alarms

The LTC3350 has a limit checking function that will check each measured value against I^2C/SMBus programmable limits. This feature is optional, and all the limits are disabled by default. The limit checking is designed to simplify system monitoring, eliminating the need to continuously poll the LTC3350 for measurement data.

If a measured parameter goes outside of the programmed level of an enabled limit, the associated bit in the alarm_reg register is set high and the $\overline{\text{SMBALERT}}$ pin is pulled low. This informs the I^2C/SMBus host a limit has been exceeded. The alarms register may then be read to determine exactly which programmed limits have been exceeded.

A single ADC is shared between the 11 channels with about 18ms between consecutive measurements of the same channel. In a transient condition, it is possible for these parameters to exceed their programmed levels in between consecutive ADC measurements without setting the alarm.

Once the LTC3350 has responded to an SMBus ARA the $\overline{\text{SMBALERT}}$ pin is released. The part will not pull the pin low again until another limit is exceeded. To reset a limit that has been exceeded, it must be cleared by writing a one to the respective bit in the clr_alarms register.

A number of the LTC3350's registers are used for limit checking. Individual limits are enabled or disabled in the msk_alarms registers. Once an enabled alarm's measured value exceeds the programmed level for that alarm the alarm is set. That alarm may be cleared by writing a one to the appropriate bit of the clr_alarms register or by writing a zero to the appropriate bit to the msk_alarms register. All alarms that have been set and have not yet been cleared may be read in the alarm_reg register.

All of the individual measured voltages have a corresponding undervoltage (uv) and overvoltage (ov) alarm level. All of the individual capacitor voltages are compared to the same alarm levels, set in the cap_ov_lvl and cap_uv_lvl registers. The input current measurement has an overcurrent (oc) alarm programmed in the iin_oc_lvl register. The charge current has an undercurrent alarm programmed in the ichg_uc_lvl register.

Die Temperature Sensor

The LTC3350 has an integrated die temperature sensor monitored by the ADC and digitized to the meas_dtemp register. An alarm may be set on die temperature by setting the dtemp_cold_lvl and/or dtemp_hot_lvl registers and enabling their respective alarms in the msk_alarms register. To convert the code in the meas_dtemp register to degrees Celsius use the following:

$$T_{DIE}\ (°C) = 0.028 \bullet \text{meas\_dtemp} - 251.4$$

General Purpose Input

The general purpose input (GPI) pin can be used to measure an additional system parameter. The voltage on this pin is directly digitized by the ADC. For high impedance inputs, an internal buffer may be selected and used to drive the ADC. This buffer is enabled by setting the ctl_gpi_buffer_en bit in the ctl_reg register. With this buffer, the input range is limited from 0V to 3.5V. If this buffer is not used, the range is from 0V to 5V, however, the input stage of the ADC will draw about 0.4µA per volt from this pin. The ADC input is a switched capacitor amplifier running at about 1MHz, so this current draw will be at that frequency. The pin current can be eliminated at the cost of reduced range and increased offset by enabling the buffer.

Alarms are available for this pin voltage with levels programmed using the gpi_uv_lvl and gpi_ov_lvl registers. These alarms are enabled using the msk_gpi_uv and msk_gpi_ov bits in the msk_alarms register.

To monitor the temperature of the supercapacitor stack, the GPI pin can be connected to a negative temperature coefficient (NTC) thermistor. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used.

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Digital Configuration

Although the LTC3350 has extensive digital features, only a few are required for basic use. The shunt voltage should be programmed via the vshunt register if a value other than the default 2.7V is required. The capacitor voltage feedback reference defaults to 1.2V; it may be changed in the vcapfb_dac register.

All other digital features are optional and used for monitoring. The ADC automatically runs and stores conversions to registers (e.g., meas_vcap). Capacitance and ESR measurements only run if requested, however, they may be scheduled to repeat if desired (ctl_strt_capesr and cap_esr_per). Each measured parameter has programmable limits (e.g., vcap_uv_lvl and vcap_ov_lvl) which may trigger an alarm and SMBALERT when enabled. These alarms are disabled by default.

Capacitor Configuration

The LTC3350 may be used with one to four supercapacitors. If less than four capacitors are used, the capacitors must be populated from CAPRTN to CAP4, and the unused CAP pins must be tied to the highest used CAP pin. For example, if three capacitors are used, CAP4 should be tied to CAP3. If only two capacitors are used, both CAP4 and CAP3 should be tied to CAP2. The number of capacitors used must be programmed on the CAP_SLCT0 and CAP_SLCT1 pins by tying the pins to VCC2P5 for a one and ground for a zero as shown in Table 1. The value programmed on these pins may be read back from the num_caps register via I²C/SMBus.

Table 1

CAP_SLCT1	CAP_SLCT0	num_caps REGISTER VALUE	NUMBER OF CAPACITORS
0	0	0	1
0	1	1	2
1	0	2	3
1	1	3	4

Capacitor Shunt Regulator Programming

V_{SHUNT} is programmed via the I²C/SMBus interface and defaults to 2.7V at initial power-up. V_{SHUNT} serves to limit the voltage on any individual capacitor by turning on a shunt around that capacitor as the voltage approaches V_{SHUNT}. CAPRTN, CAP1, CAP2, CAP3 and CAP4 must be connected to the supercapacitors through resistors which serve as ballasts for the internal shunts. The shunt current is approximately V_{SHUNT} divided by twice the shunt resistance value. For a V_{SHUNT} of 2.7V, 2.7Ω resistors should be used for 500mA of shunt current. The shunts have a duty cycle of up to 75%. The power dissipated in a single shunt resistor is approximately:

$$P_{SHUNT} \approx \frac{3V_{SHUNT}^2}{16R_{SHUNT}}$$

and the resistors should be sized accordingly. If the shunts are disabled, make R_{SHUNT} 100Ω.

Since the shunt current is less than what the switcher can supply, the on-chip logic will automatically reduce the charging current to allow the shunt to protect the capacitor. This greatly reduces the charge rate once any one shunt is activated. For this reason, V_{SHUNT} should be programmed as high as possible to reduce the likelihood of it activating during a charge cycle. Ideally, V_{SHUNT} would be set high enough so that any likely capacitor mismatches would not cause the shunts to turn on. This keeps the charger operating at the highest possible charge current and reduces the charge time. If the shunts never turn on, the charge cycle completes quickly and the balancers eventually equalize the voltage on the capacitors. The shunt setting may also be used to discharge the capacitors for testing, storage or other purposes.

Setting Input and Charge Currents

The maximum input current is determined by the resistance across the VOUTSP and VOUTSN pins, R_{SNSI}. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, used in series with the inductor. The input and charge current loops servo the voltage across their respective sense resistor to 32mV. Therefore, the maximum input and charge currents are:

$$I_{IN(MAX)} = \frac{32mV}{R_{SNSI}}$$

$$I_{CHG(MAX)} = \frac{32mV}{R_{SNSC}}$$

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The peak inductor current limit, I_{PEAK}, is 80% higher than the maximum charge current and is equal to:

$$I_{PEAK} = \frac{58mV}{R_{SNSC}}$$

Note that the input current limit does not include the part's quiescent and gate drive currents. The total current drawn by the part will be $I_{IN(MAX)} + I_Q + I_G$, where I_Q is the non-switching quiescent current and I_G is the gate drive current.

Low Current Charging and High Current Backup

The LTC3350 can accommodate applications requiring low charge currents and high backup currents. In these applications, program the desired charge current using R_{SNSI}. The higher current needed during backup can be set using R_{SNSC}. The input current limit will override the charge current limit when the supercapacitors are charging while the charge current limit provides sufficient current capability for backup operation.

The charge current will be limited to $I_{CHG(MAX)}$ at low V_{CAP} (i.e., low duty cycles). As V_{CAP} rises, the switching controller's input current will increase until it reaches $I_{IN(MAX)}$. The input current will be maintained at $I_{IN(MAX)}$ and the charge current will decrease as V_{CAP} rises further.

Some applications may want to use only a portion of the input current limit to charge the supercapacitors. Two input current sense resistors placed in series can be used to accomplish this as shown in Figure 3. VOUTSP is kelvin connected to the positive terminal of R_{SNSI1} and VOUTSN is kelvin connected to the negative terminal of R_{SNSI2}. The load current is pulled across R_{SNSI1} while the input current to the charger is pulled across R_{SNSI1} and R_{SNSI2}. The input current limit is:

$$32mV = R_{SNSI1} \bullet I_{LOAD} + (R_{SNSI1} + R_{SNSI2}) \bullet I_{INCHG}$$

For example, suppose that only 2A of input current is desired to charge the supercapacitors but the system load and charger combined can pull a total of up to 4A from the supply. Setting $R_{SNSI1} = R_{SNSI2} = 8m\Omega$ will set a 4A current limit for the load + charger while setting a 2A limit for the charger. With no system load, the charger can pull up to 2A of input current. As the load pulls 0A to 4A of current the charger's input current will reduce from 2A down to 0A.

The following equation can be used to determine charging input current as a function of system load current:

$$I_{INCHG} = \frac{32mV}{R_{SNSI1} + R_{SNSI2}} - \frac{R_{SNSI1}}{R_{SNSI1} + R_{SNSI2}} \bullet I_{LOAD}$$

The contact resistance of the negative terminal of R_{SNSI1} and the positive terminal of R_{SNSI2} as well as the resistance of the trace connecting them will cause variability in the input current limit. To minimize the error, place both input current sense resistors close together with a large PCB pad area between them as the system load current is pulled from the trace connecting the two sense resistors.

Note that the backup current will flow through R_{SNSI2}. The R_{SNSI2} package should be sized accordingly to handle the power dissipation.

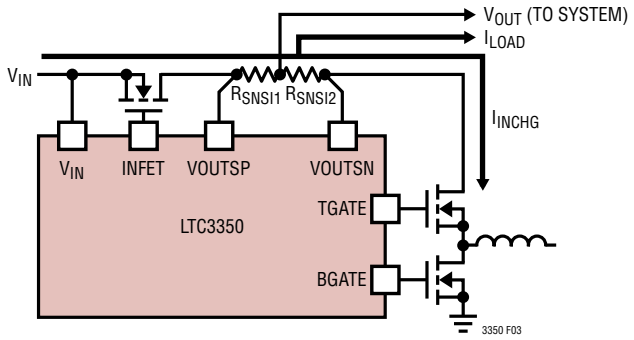

Figure 3

Setting V_{CAP} Voltage

The LTC3350 V_{CAP} voltage is set by an external feedback resistor divider, as shown in Figure 4. The regulated output voltage is determined by:

$$V_{CAP} = \left(1 + \frac{R_{FBC1}}{R_{FBC2}}\right) CAPFBREF$$

where CAPFBREF is the output of the V_{CAP} DAC, programmed in the vcapfb_dac register. Great care should be taken to route the CAPFB line away from noise sources, such as the SW line.

Power-Fail Comparator Input Voltage Threshold

The input voltage threshold below which the power-fail status pin, $\overline{PFO}$, indicates a power-fail condition and the

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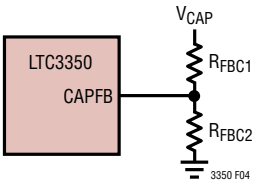

Figure 4. V_{CAP} Voltage Feedback Divider

LTC3350 bidirectional controller switches to step-up mode is programmed using a resistor divider from the V_{IN} pin to SGND via the PFI pin such that:

$$V_{IN} = \left(1+\frac{R_{PF1}}{R_{PF2}}\right) V_{PFI(TH)}$$

where $V_{PFI(TH)}$ is 1.17V. Typical values for R_{PF1} and R_{PF2} are in the range of 40k to 1M. See Figure 5.

The input voltage above which the power-fail status pin $\overline{PFO}$ is high impedance and the bidirectional controller switches to step-down mode is:

$$V_{IN} = \left(1+\frac{R_{PF1}}{R_{PF2}}\right)\left(V_{PFI(TH)} + V_{PFI(HYS)}\right)$$

where $V_{PFI(HYS)}$ is the hysteresis of the PFI comparator and is equal to 30mV.

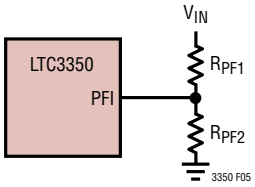

Figure 5. PFI Threshold Voltage Divider

Additional hysteresis can be added by switching in an additional resistor, R_{PF3}, in parallel with R_{PF2} when the voltage at PFI falls below 1.17V as shown in Figure 6. The falling V_{IN} threshold is the same as before but the rising V_{IN} threshold becomes:

$$V_{IN} = \left(1+\frac{R_{PF1}}{R_{RP2}}+\frac{R_{PF1}}{R_{PF3}}\right)\left(V_{PFI(TH)} + V_{PFI(HYST)}\right)$$

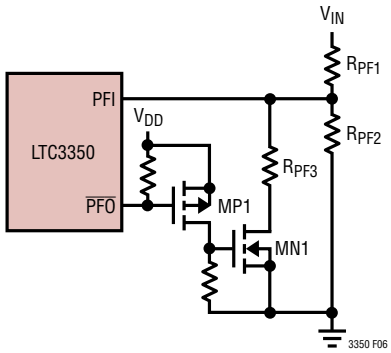

Figure 6. PFI Threshold Divider with Added Hystersis

MN1 and MP1 can be implemented with a single package N-channel and P-channel MOSFET pair such as the Si1555DL or Si1016CX. The drain leakage current of MN1, when its gate voltage is at ground, can introduce an offset in the threshold. To minimize the effect of this leakage current R_{PF1}, R_{PF2} and R_{PF3} should be between 1k and 100k.

Setting V_{OUT} Voltage in Backup Mode

The output voltage for the controller in step-up mode is set by an external feedback resistor divider, as shown in Figure 7. The regulated output voltage is determined by:

$$V_{OUT} = \left(1+\frac{R_{FBO1}}{R_{FBO2}}\right) 1.2V$$

Great care should be taken to route the OUTFB line away from noise sources, such as the SW line.

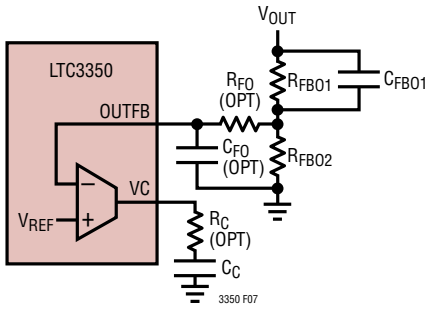

Figure 7. V_{OUT} Voltage Divider and Compensation Network

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Compensation

The input current, charge current, V_{CAP} voltage, and V_{OUT} voltage loops all require a 1nF to 10nF capacitor from the VC node to ground. When using the output ideal diode and backing up to low voltages (<8V) use 8.2nF to 10nF on VC. When not using the output ideal diode 4.7nF to 10nF on VC is recommended. For very high backup voltages (>15V) 1nF to 4.7nF is recommended.

In addition to the VC node capacitor, the V_{OUT} voltage loop requires a phase-lead capacitor, C_{FBO1}, for stability and improved transient response during input power failure (Figure 7). The product of the top divider resistor and the phase-lead capacitor should be used to create a zero at approximately 2kHz:

$$R_{FBO1} \bullet C_{FBO1} \approx \frac{1}{2\pi(2kHz)}$$

Choose an R_{FBO1} such that C_{FBO1} is ≥ 100pF to minimize the effects of parasitic pin capacitance. Because the phase-lead capacitor introduces a larger ripple at the input of the V_{OUT} transconductance amplifier, an additional RC lowpass filter from the V_{OUT} divider to the OUTFB pin may be needed to eliminate voltage ripple spikes. The filter time constant should be located at the switching frequency of the synchronous controller:

$$R_{FO} \bullet C_{FO} = \frac{1}{2\pi f_{SW}}$$

with C_{FO} > 10pF to minimize the effects of parasitic pin capacitance. For back up applications where the V_{OUT} regulation voltage is low (~5V to 6V), an additional 1k to 3k resistor, R_C, in series with the VC capacitor can improve stability and transient response.

Minimum V_{CAP} Voltage in Backup Mode

In backup mode, power is provided to the output from the supercapacitors either through the output ideal diode or the synchronous controller operating in step-up mode.

The output ideal diode provides a low loss power path from the supercapacitors to V_{OUT}. The minimum internal (open-circuit) supercapacitor voltage will be equal to the minimum V_{OUT} necessary for the system to operate plus the voltage drops due to the output ideal diode and equivalent series resistance, R_{SC}, of each supercapacitor in the stack.

Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack, each with an R_{SC} of 45mΩ. The output ideal diode forward regulation voltage is 30mV (OUTFET $R_{DS(ON)}$ < 30mΩ). The minimum open-circuit supercapacitor voltage is:

$$V_{CAP(MIN)} = 5V + 0.030V + (1A \bullet 4 \bullet 45m\Omega) = 5.21V$$

Using the synchronous controller in step-up mode allows the supercapacitors to be discharged to a voltage much lower than the minimum V_{OUT} needed to run the system. The amount of power that the supercapacitor stack can deliver at its minimum internal (open-circuit) voltage should be greater than what is needed to power the output and the step-up converter.

According to the maximum power transfer rule:

$$P_{CAP(MIN)} = \frac{V_{CAP(MIN)}^2}{4 \bullet n \bullet R_{SC}} > \frac{P_{BACKUP}}{\eta}$$

In the equation above η is the efficiency of the synchronous controller in step-up mode and n is the number of supercapacitors in the stack.

Example: System needs 5V to run and draws 1A during backup. There are four supercapacitors in the stack (n = 4), each with an R_{SC} of 45mΩ. The converter efficiency is 90%. The minimum open-circuit supercapacitor voltage is:

$$V_{CAP(MIN)} = \sqrt{\frac{4 \bullet 4 \bullet 45m\Omega \bullet 5V \bullet 1A}{0.9}} = 2.0V$$

In this case, the voltage seen at the terminals of the capacitor stack is half this voltage, or 1V, according to the maximum power transfer rule.

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Note the minimum V_{CAP} voltage can also be limited by the peak inductor current limit (180% of maximum charge current) and the maximum duty cycle in step-up mode (~90%).

Optimizing Supercapacitor Energy Storage Capacity

In most systems the supercapacitors will provide backup power to one or more DC/DC converters. A DC/DC converter presents a constant power load to the supercapacitor. When the supercapacitors are near their maximum voltage, the loads will draw little current. As the capacitors discharge, the current drawn from supercapacitors will increase to maintain constant power to the load. The amount of energy required in back up mode is the product of this constant backup power, P_{BACKUP}, and the backup time, t_{BACKUP}.

The energy stored in a stack of n supercapacitors available for backup is:

$$\frac{1}{2} nC_{SC}\left(V_{CELL(MAX)}^2 - V_{CELL(MIN)}^2\right)$$

where C_{SC}, $V_{CELL(MAX)}$ and $V_{CELL(MIN)}$ are the capacitance, maximum voltage and minimum voltage of a single capacitor in the stack, respectively. The maximum voltage on the stack is $V_{CAP(MAX)} = n \bullet V_{CELL(MAX)}$. The minimum voltage on the stack is $V_{CAP(MIN)} = n \bullet V_{CELL(MIN)}$.

Some of this energy will be dissipated as conduction loss in the ESR of the supercapacitor stack. A higher backup power requirement leads to a higher conduction loss for a given stack ESR.

The amount of capacitance needed can be found by solving the following equation for C_{SC}:

$$P_{BACKUP} \bullet t_{BACKUP} = \frac{1}{4} nC_{SC}\left[\gamma_{MAX} \bullet V_{CELL(MAX)}^2 - \gamma_{MIN} \bullet V_{CELL(MIN)}^2 - \frac{4R_{SC} \bullet P_{BACKUP}}{n} \ln\left(\frac{\gamma_{MAX} \bullet V_{CELL(MAX)}}{\gamma_{MIN} \bullet V_{CELL(MIN)}}\right)\right]$$

where:

$$\gamma_{MAX} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV_{CELL(MAX)}^2}} \text{ and,}$$

$$\gamma_{Min} = 1 + \sqrt{1 - \frac{4R_{SC} \bullet P_{BACKUP}}{nV_{CELL(MIN)}^2}}$$

R_{SC} is the equivalent series resistance (ESR) of a single supercapacitor in the stack. Note that the maximum power transfer rule limits the minimum cell voltage to:

$$V_{CELL(MIN)} = \frac{V_{CAP(MIN)}}{n} \geq \sqrt{\frac{4R_{SC} \bullet P_{BACKUP}}{n}}$$

To minimize the size of the capacitance for a given amount of backup energy, the maximum voltage on the stack, $V_{CELL(MAX)}$, can be increased. However, the voltage is limited to a maximum of 2.7V and this may lead to an unacceptably low capacitor lifetime.

An alternative option would be to keep $V_{CELL(MAX)}$ at a voltage that leads to reasonably long lifetime and increase the capacitor utilization ratio of the supercapacitor stack. The capacitor utilization ratio, α_B, can be defined as:

$$\alpha_B = \frac{V_{CELL(MAX)}^2 - V_{CELL(MIN)}^2}{V_{CELL(MAX)}^2}$$

If the synchronous controller in step-up mode is used then the supercapacitors can be run down to a voltage set by the