Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Hot Swappable Supercapacitor Charger, Backup Controller and System Monitor

FEATURES

- **Integrated Hot Swap Controller with Circuit Breaker**
- **High Efficiency Synchronous Step-Down CC/CV Charging of One to Four Series Supercapacitors**
- **Step-Up Mode in Backup Provides Greater Utilization of Stored Energy in Supercapacitors**
- **16-Bit ADC for Monitoring System Voltages/ Currents, Capacitance and ESR**
- **Programmable Undervoltage and Overvoltage Thresholds to 35V**
- V_{IN}: 4.5V to 35V, $V_{CAP(n)}$: Up to 5V per Capacitor, Charge/Backup Current: >10A
- Programmable Input Current Limit Prioritizes System Load Over Capacitor Charge Current
- All N-FET Charger Controller and PowerPath Controller
- Compact 44-Lead 4mm x 7mm QFN Package

APPLICATIONS

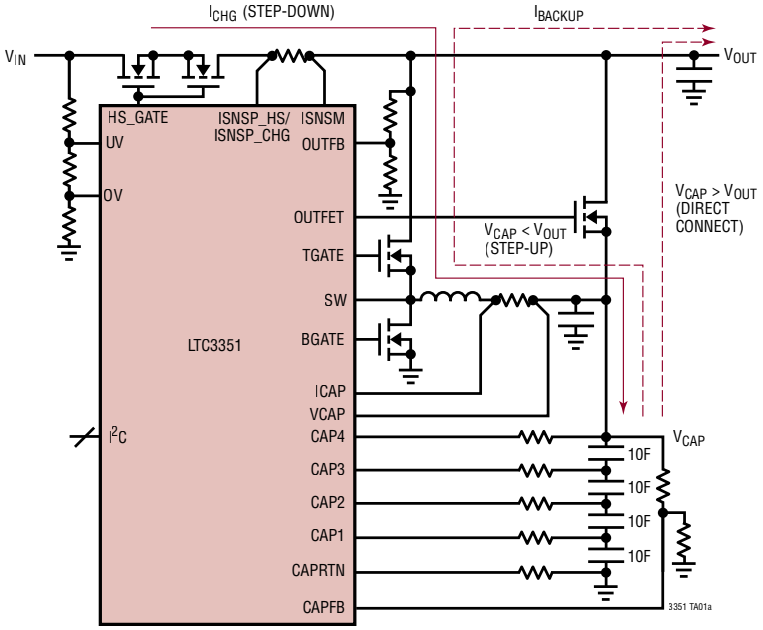
- Swappable PCIe cards with NVM
- High Current 12V Ride-Through UPS
- Servers/Mass Storage/High Availability Systems

DESCRIPTION

The LTC®3351 is a backup power controller that charges and monitors a series stack of one to four supercapacitors. The LTC3351's synchronous step-down controller drives N-channel MOSFETs for constant current/constant voltage charging with programmable input current limit. In addition, the step-down converter runs in reverse as a step-up converter to deliver power from the supercapacitor stack to the backup supply rail. Internal balancers eliminate the need for external balance resistors and each capacitor has a shunt regulator for overvoltage protection.

The LTC3351 monitors system voltages, currents, stack capacitance and ESR which can all be read over the I²C/ SMBus port. The hot swap controller uses N-channel MOSFETs for inrush control and a low loss path from the input to the output. The ideal diode controller uses an N-channel MOSFET for a low loss power path from the supercapacitors to the output. The LTC3351 is available in a thermally enhanced low profile 44-lead 4mm x 7mm x 0.75mm QFN surface mount package.

TYPICAL APPLICATION



Example Hot Swap from 12V

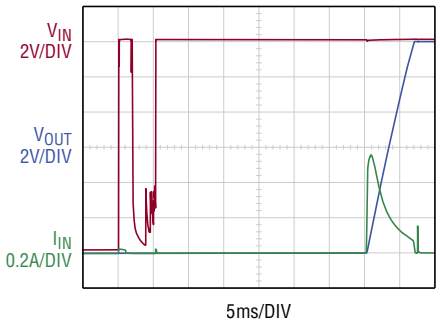


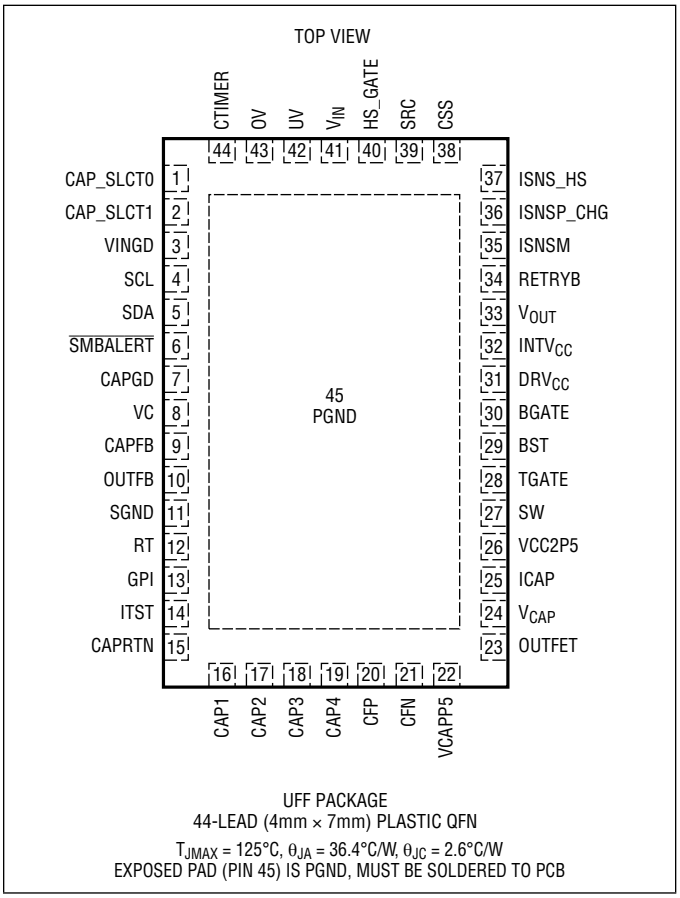
TABLE OF CONTENTS

ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_{OUT}, ISNSP_HS,ISNSP_CHG,ISNSM,
UV, OV, RETRYB, OUTFB ..... –0.3V to 40V
VCAP ..... –0.3V to 22V
CAP4-CAP3, CAP3-CAP2,
CAP2-CAP1, CAP1-CAPRTN ..... –0.3V to 5.5V
DRV_{CC}, CAPFB, $\overline{SMBALERT}$, CAPGD,
VINGD, GPI, SDA, SCL .....–0.3V to $INTV_{CC}$ + 0.3V
BST ..... –0.3V to 45.5V
CAP_SLCT0, CAP_SLCT1 ..... –0.3V to VCC2P5 + 0.3V
BST to SW ..... –0.3V to 5.5V
ISNSP_HS to ISNSM,
ISNSP_CHG to ISNSM, ICAP to VCAP... –0.3V to 0.3V
I_{INTVCC} 100mA
$I_{CAP(1,2,3,4)}$, I_{CAPRTN} 600mA
I_{CAPGD}, I_{VINGD} , $I_{\overline{SMBALERT}}$.....10mA
Operating Junction Temperature Range
(Notes 2, 3).....–40°C to 125°C
Storage Temperature Range .....–65°C to 150°C

PIN CONFIGURATION



UFF PACKAGE
44-LEAD (4mm × 7mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 36.4°C/W, θ_{JC} = 2.6°C/W
EXPOSED PAD (PIN 45) IS PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3351#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3351EUFF#PBF	LTC3351EUFF#TRPBF	3351	44-Lead (4mm x 7mm) Plastic QFN	–40°C to 125°C
LTC3351IUFF#PBF	LTC3351IUFF#TRPBF	3351	44-Lead (4mm x 7mm) Plastic QFN	–40°C to 125°C

Consult ADI Marketing for parts specified with wider operating temperature ranges.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Switching Regulator							
V_{IN}	Input Supply Voltage		●	4.5		35	V
I_Q	Input Quiescent Current, I_{VOUT} (Note 4)				2.25		mA
$V_{CAPFBHI}$	Maximum Regulated V_{CAP} Feedback Voltage	Full Scale (1111b)	●	1.188	1.2	1.212	V
V_{CAPFB_DEF}	Default V_{CAPFB_DAC} Setting	(1010b)	●	0.997	1.0125	1.028	V
$V_{CAPFBLO}$	Minimum Regulated V_{CAP} Feedback Voltage	Zero Scale (0000b)	●	0.625	0.6375	0.650	V
I_{CAPFB}	CAPFB Input Leakage Current	V_{CAPFB} = 1.2V	●	–50		50	nA
V_{OUTFB}	Regulated V_{OUT} Feedback Voltage		●	1.182	1.2	1.218	V
$V_{OUTFB(TH)}$	OUTFET Turn-Off Threshold	Falling Threshold		1.27	1.3	1.33	V
I_{OUTFB}	OUTFB Input Leakage Current	V_{OUTFB} = 1.2V	●	–50		50	nA
V_{OUTBST}	V_{OUT} Voltage in Step-Up Mode	V_{IN} = 0V	●	4.5		35	V
V_{UVLO}	$INTV_{CC}$ Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.85	4.3 4	4.45	V V
$V_{DRVUVLO}$	DRV_{CC} Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	 3.75	4.2 3.9	4.35	V V
V_{DUVLO}	V_{OUT} – V_{CAP} Differential Undervoltage Lockout	Rising Threshold Falling Threshold	● ●	160 55	200 90	240 125	mV mV
V_{OVLO}	Switcher V_{IN} Overvoltage Lockout	Rising Threshold Falling Threshold	● ●	37.7 36.3	38.6 37.2	39.5 38.1	V V
V_{VCAPP5}	Charge Pump Output Voltage	Relative to VCAP, 0V < V_{CAP} < 20V			5		V
Input Current Sense Amplifier							
V_{SNSI}	Regulated Input Current Sense Voltage (ISNSP_CHG – ISNSM)		●	31.04	32	32.96	mV
Charge Current Sense Amplifier							
V_{SNSC}	Regulated Charge Current Sense Voltage (I_{CAP} – V_{CAP})	V_{CAP} = 10V, Charge Mode	●	31.04	32	32.96	mV
V_{CMC}	Common Mode Range (ICAP, VCAP)			0		20	V
V_{PEAK}	Peak Inductor Current Sense Voltage	Active in Both Step-Up/Step-Down Modes	●	51	58	65	mV
I_{ICAP}	ICAP Pin Current	Step-Down Mode, VSNSC = 32mV Step-Up Mode, VSNSC = 32mV			27 100		µA µA
Error Amplifier							
g_{MV}	V_{CAP} Voltage Loop Transconductance				1		mmho
g_{MC}	Charge Current Loop Transconductance				64		µmho
g_{MI}	Input Current Loop Transconductance				64		µmho
g_{MO}	V_{OUT} Voltage Loop Transconductance				350		µmho
Oscillator							
f_{SW}	Switching Frequency	RT = 107k	●	493	500	507	kHz
	Maximum Programmable Frequency	RT = 53.6k			1		MHz
	Minimum Programmable Frequency	RT = 267k			200		kHz
DCMAX	Maximum Duty Cycle	Step-Down Mode, 53.6k < R_T < 267k Step-Up Mode, 53.6k < R_T < 267k		97 87	98 93	99.5	% %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers							
R_{UP-TG}	TGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-TG}$	TGATE Pull-Down On-Resistance				0.6		Ω
R_{UP-BG}	BGATE Pull-Up On-Resistance				2		Ω
$R_{DOWN-BG}$	BGATE Pull-Down On-Resistance				0.6		Ω
t_{NO}	Non-Overlap Time				50		ns
$t_{ON(MIN)}$					85		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	5.2V < V_{IN} < 35V			5		V
DV_{INTVCC}	Load Regulation	I_{INTVCC} = 50mA			–1.5	–2.5	%
Ideal Diode							
V_{FTO}	Fast On Threshold Voltage				65		mV
V_{FR}	Forward Regulation Voltage				30		mV
V_{RTO}	Reverse Turn Off Threshold Voltage				–30		mV
UV/OV Comparator							
$V_{UV/OVI(TH)}$	UV/OV Input Threshold (Rising Edge)		●	1.182	1.2	1.218	V
$V_{UV/OVI(HYS)}$	UV/OV Hysteresis				60		mV
$I_{UV/OV}$	UV/OV Input Leakage Current	$V_{UV/OV}$ = 0.5V	●	–50		50	nA
V_{VINGD}	VINGD Output Low Voltage	I_{SINK} = 5mA			300		mV
I_{VINGD}	VINGD High-Z Leakage Current	VINGD = 5V	●			1	µA
	UV Falling to VINGD Low Delay				1		µs
CAPGD							
$V_{CAPFB(TH)}$	CAPGD Rising Threshold as % of Regulated V_{CAP} Feedback Voltage	vcapfb_dac = Full Scale (1111b)	●	90	92	94	%
$V_{CAPFB(HYS)}$	CAPGD Hysteresis at CAPFB as a % of Regulated V_{CAP} Feedback Voltage	vcapfb_dac = Full Scale (1111b)			2.5		%
V_{CAPGD}	CAPGD Output Low Voltage	I_{SINK} = 5mA			200		mV
I_{CAPGD}	CAPGD High-Z Leakage Current	V_{CAPGD} = 5V	●			1	µA
Analog-to-Digital Converter							
V_{RES}	Measurement Resolution				16		Bits
V_{GPI}	General Purpose Input Voltage Range	Unbuffered Buffered		0 0		5 3.5	V V
I_{GPI}	General Purpose Input Pin Leakage Current	Buffered Input				1	µA
R_{GPI}	GPI Pin Resistance	Buffer Disabled			1.25		MΩ

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Measurement System Error							
V_{ERR}	Measurement Error (Note 5)	V_{IN} = 0V V_{IN} = 30V				100 1.5	mV %
		V_{OUT} = 5V V_{OUT} = 30V				100 1.5	mV %
		V_{CAP} = 0V V_{CAP} = 10V				100 1.5	mV %
		V_{GPI} = 0V, Unbuffered V_{GPI} = 5V, Unbuffered				2 1	mV %
		V_{CAP1} = 0V V_{CAP1} = 2V				2 1	mV %
		V_{CAP2} = 0V V_{CAP2} = 2V				2 1	mV %
		V_{CAP3} = 0V V_{CAP3} = 2V				2 1	mV %
		V_{CAP4} = 0V V_{CAP4} = 2V				2 1	mV %
		V_{SNSI} = 0mV V_{SNSI} = 32mV				200 2	µV %
		V_{SNSC} = 0mV V_{SNSC} = 32mV				200 2	µV %
CAP1 to CAP4							
R_{SHNT}	Shunt Resistance				0.5		Ω
DVCAPMAX	Maximum Shunt Operating Voltage					3.6	V
Programming Pins							
V_{ITST}	ITST Voltage	R_{TST} = 20Ω	●	1.182	1.2	1.209	V
I^2C/SMBus – SDA, SCL, SMBALERT							
$I_{IL,SDA,SCL}$	Input Leakage Low			–1		1	µA
$I_{IH,SDA,SCL}$	Input Leakage High			–1		1	µA
V_{IH}	Input High Threshold			1.5			V
V_{IL}	Input Low Threshold					0.8	V
f_{SCL}	SCL Clock Frequency					400	kHz
t_{LOW}	Low Period of SCL Clock			1.3			µs
t_{HIGH}	High Period of SCL Clock			0.6			µs
t_{BUF}	Bus Free Time Between Start and Stop Conditions			1.3			µs
$t_{HD,STA}$	Hold Time, After (Repeated) Start Condition			0.6			µs
$t_{SU,STA}$	Setup Time After a Repeated Start Condition			0.6			µs
$t_{SU,STO}$	Stop Condition Set-Up Time			0.6			µs
$t_{HD,DATO}$	Output Data Hold Time			0		900	ns
$t_{HD,DATI}$	Input Data Hold Time			0			ns
$t_{SU,DAT}$	Data Set-Up Time			100			ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
$V_{SMBALERT}$	SMBALERT Output Low Voltage	I_{SINK} = 5mA			200		mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_J = 25°C (Note 2). V_{IN} = V_{OUT} = 12V, $VDRV_{CC}$ = $VINTV_{CC}$ unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{SMBALERT}$	SMBALERT High-Z Leakage Current	$V_{SMBALERT}$ = 5V	●			1	µA
Hot Swap Controller							
$V_{IN(UVLO\_HS)}$	Hot Swap Input Supply Undervoltage Lockout	V_{IN} rising, Hot Swap operation	●	3.7	3.85	4	V
$V_{ILIM(TH)}$	Current Limit Threshold (ISNS_HS-ISNSM)	V_{OUT} < V_{IN} – 11V V_{OUT} = V_{IN}	● ●	7 46	10 48	13 50	mV mV
$I_{(OV,UV,RETRYB)}$	OV, UV, RETRYB Pin Input Current		●	–50	0	50	nA
$V_{TH(RETRYB)}$	RETRYB Threshold		●	185	200	215	mV
$V_{TIMER(TH)}$	CTIMER Pin Threshold	Rising Falling	●	1.188	1.2 0.3	1.212	mV mV
$I_{TIMER(DN)}$	CTIMER Pull Down Current		●	1.4	2	2.6	µA
$I_{TIMER(UP)}$	CTIMER Pull Up Current		●	320	400	480	µA
$I_{TIMER(RATIO)}$	CTIMER Pull-Down/Pull-Up Current		●		0.5	0.6	%
$I_{HS\_GATE(UP)}$	HS_GATE Pull Up Current		●	16	24	30	µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3351 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3351E is guaranteed to meet specifications from 0°C to 125°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3351I is guaranteed over the –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} = 36.4°C/W for the UFF package.

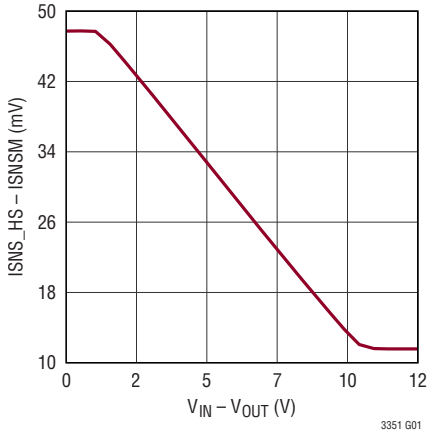
Note 3: The LTC3351 includes over temperature protection that is intended to protect the device during momentary overload conditions. When over temperature protection is active the switcher is shutdown. Junction temperature will exceed 125°C when over temperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

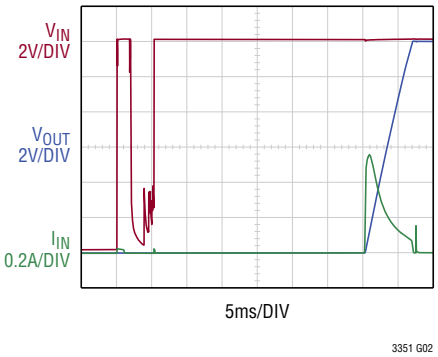
Note 5: Measurement error is the magnitude of the difference between the actual measured value and the ideal value. V_{SNSI} is the voltage between I_{SNS_CHG} and I_{SNSM}, representing input current. V_{SNSC} is the voltage between I_{CAP} and V_{CAP}, representing charge current. Error for V_{SNSI} and V_{SNSC} is expressed in µV, a conversion to an equivalent current may be made by dividing by the sense resistors, R_{SNSI} and R_{SNSC}, respectively.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

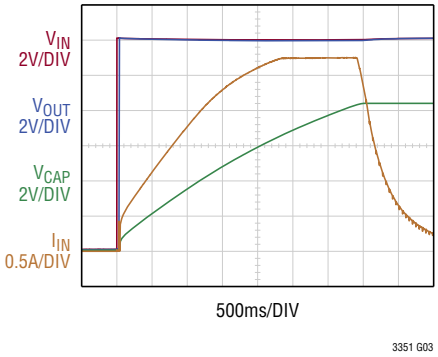
Hot Swap Current Limit Fold-Back Curve



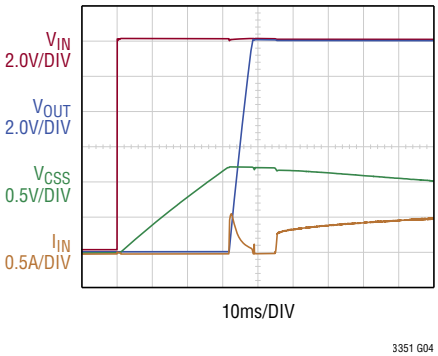
Example Hot Swap, 12V



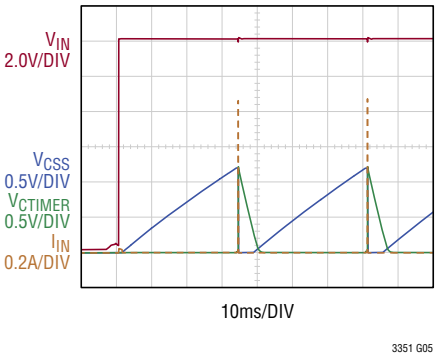
Hot Swap and Full Charge Cycle



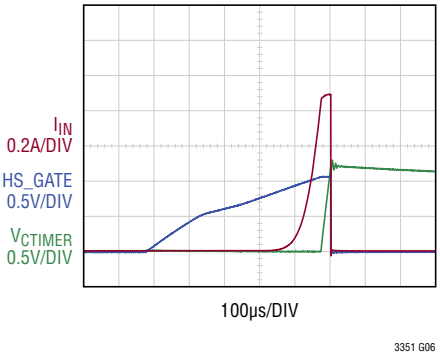
Hot Swap and Begin Charge



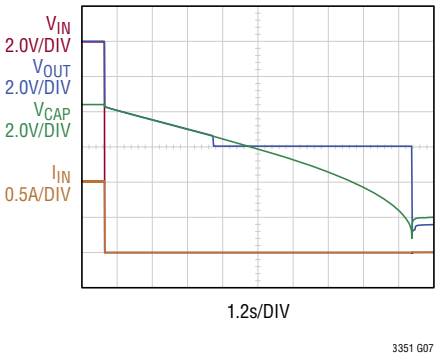
Hot Swap Startup into Shorted Output



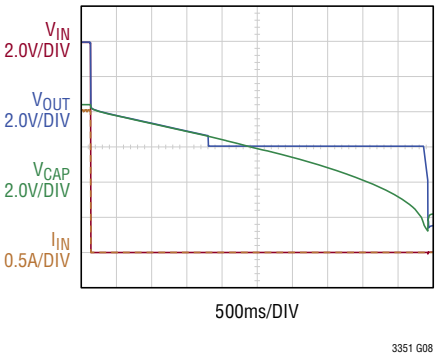
Hot Swap Short Detailed



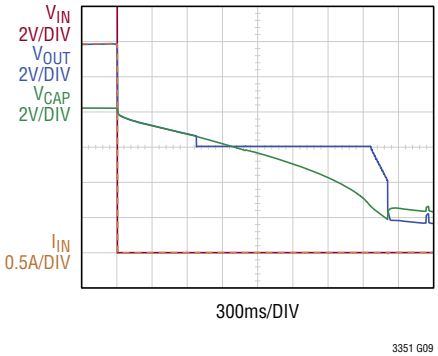
Backup Operation, 1A



Backup Operation, 2A

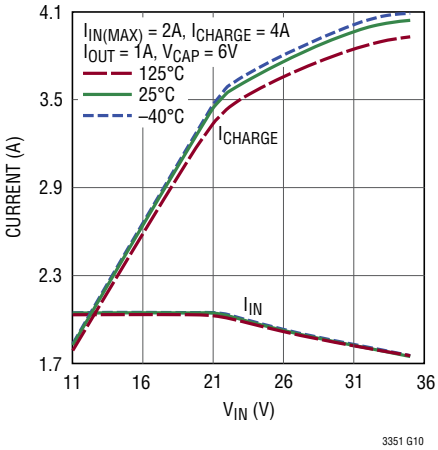


Backup Operation, 3.5A

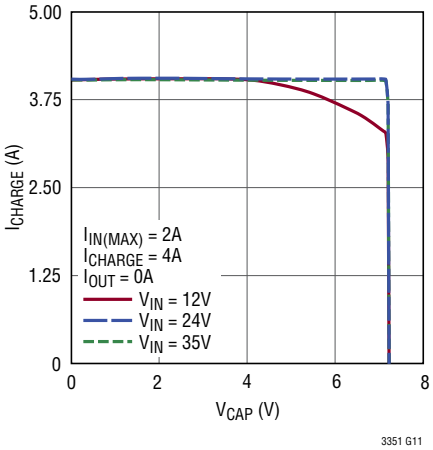


TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

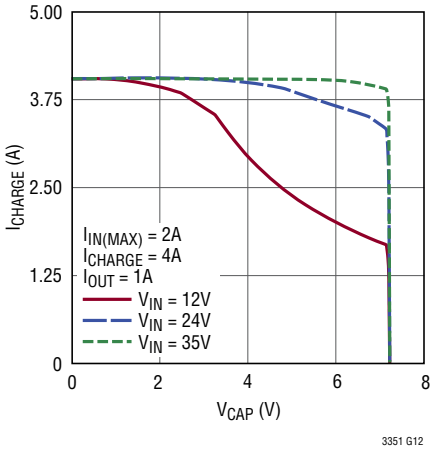
I_{IN} and I_{CHARGE} vs V_{IN}



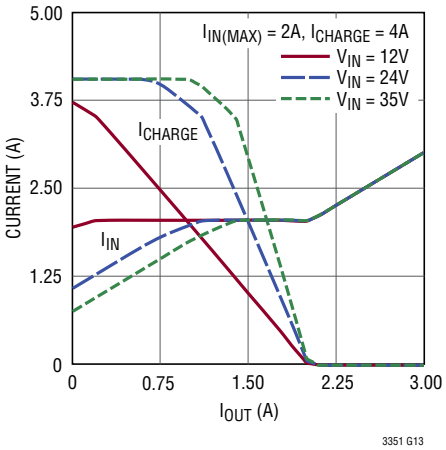
I_{CHARGE} vs V_{CAP}



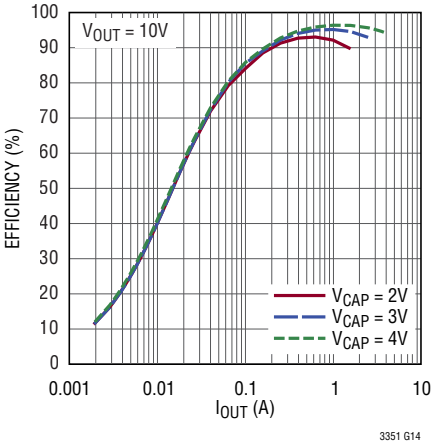
I_{CHARGE} vs V_{CAP}



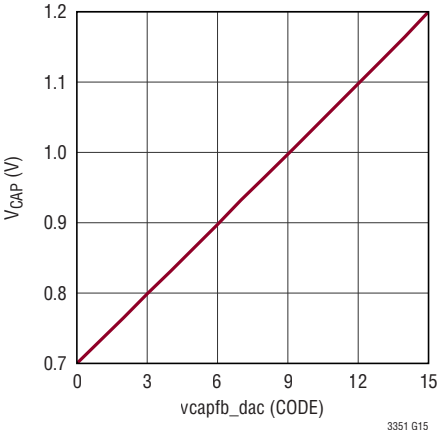
I_{IN} and I_{CHARGE} vs I_{OUT}



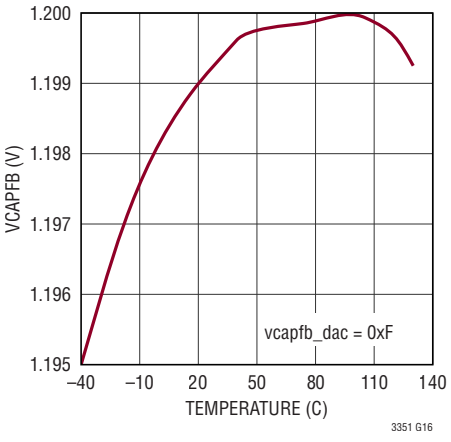
Efficiency in Boost Mode



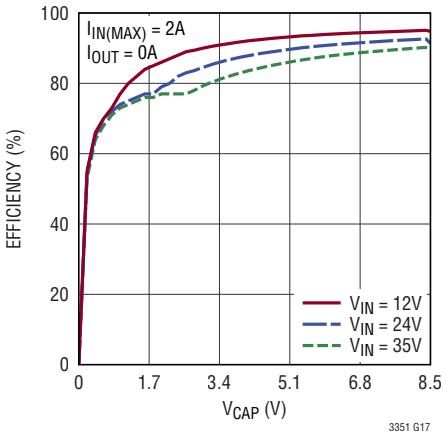
V_{CAP} vs vcapfb_dac



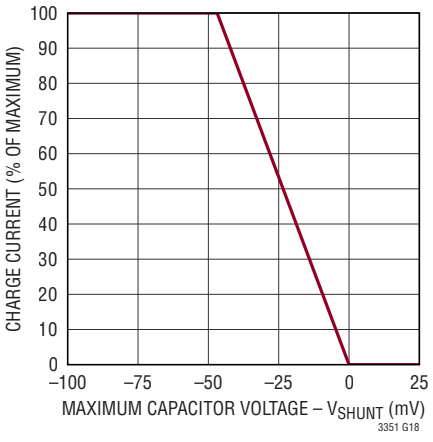
V_{CAP} vs Temperature



Charger Efficiency vs V_{CAP}



Charge Current vs Shunt Voltage



PIN FUNCTIONS

CAP_SLCT0, CAP_SLCT1 (Pins 1, 2): CAP_SLCT0 and CAP_SLCT1 set the number of super-capacitors used. Refer to Table 1 in the Applications Information section.

VINGD (Pin 3): Power-Fail Status Output. This open-drain output is pulled low when V_{OUT} is not powered from V_{IN}.

SCL (Pin 4): Clock Pin for the I^2C/SMBus Serial Port.

SDA (Pin 5): Bidirectional Data Pin for the I^2C/SMBus Serial Port.

SMBALERT (Pin 6): Interrupt Output. This open-drain output is pulled low when an alarm threshold is exceeded and will remain low until the acknowledgement of the part's response to an SMBus ARA.

CAPGD (Pin 7): Capacitor Power Good. This open-drain output is pulled low when CAPFB is below $V_{CAPFB(TH)}$.

VC (PIN 8): Control Voltage Pin. This is the compensation node for the charge current, input current, supercapacitor stack voltage and output voltage control loops. An RC network is needed between VC and SGND. There is an internal compensation resistor in series with this pin. It is 1kΩ in buck mode and 2kΩ in boost mode. Nominal voltage range for this pin is 1V to 3V.

CAPFB (Pin 9): Capacitor Stack Feedback Pin. This pin closes the feedback loop for constant voltage regulation. An external resistor divider between V_{CAP} and SGND with the center tap connected to CAPFB programs the final supercapacitor stack voltage. This pin is nominally equal to the output of the V_{CAP} DAC when the synchronous controller is charging in constant voltage mode.

OUTFB (Pin 10): Step-Up Mode Feedback Pin. This pin closes the feedback loop for voltage regulation of V_{OUT} during input power failure using the synchronous controller in step-up mode. An external resistor divider between V_{OUT} and SGND with the center tap connected to OUTFB programs the minimum backup supply rail voltage when input power is unavailable. This pin is nominally 1.2V when in backup and the synchronous controller is not in current limit. To disable step-up mode tie OUTFB to $INTV_{CC}$.

SGND (Pin 11): Signal Ground. All small-signal and compensation components should be connected to this pin, which in turn connects to PGND. SGND should connect to PGND on top metal under the LTC3351. PGND should be connected to the ground plane with vias under the exposed pad (pin 45). This should be the only connection between SGND and the ground plane.

RT (Pin 12): Timing Resistor. The switching frequency of the synchronous controller is set by placing a resistor, RT, from this pin to SGND. This resistor is always required. If not present the synchronous controller will not start.

GPI (Pin 13): General Purpose Input. The voltage on this pin is digitized directly by the ADC. For high impedance inputs an internal buffer can be selected and used to drive the ADC. The GPI pin can be connected to a negative temperature coefficient (NTC) thermistor to monitor the temperature of the supercapacitor stack. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used. Read the digitized voltage on this pin in the meas_gpi register.

ITST (Pin 14): Programming Pin for Capacitance Test Current. This current partially discharges the capacitor stack at a precise rate for capacitance measurement. This pin servos to 1.2V during a capacitor measurement. A resistor, RTST, from this pin to SGND programs the test current. The resistor on this pin must be at least 20Ω. Current flows from VCAP4 to this pin during this test and must not dissipate more than 300mW in the IC.

CAPRTN (Pin 15): Capacitor Stack Shunt Return Pin. Connect this pin to the grounded bottom plate of the first supercapacitor in the stack through a shunt resistor.

CAP1 (Pin 16): First Supercapacitor Pin. The top plate of the first supercapacitor and the bottom plate of the second supercapacitor are connected to this pin through a shunt resistor. CAP1 and CAPRTN are used to measure the voltage across the first supercapacitor and shunt current around the capacitor to provide balancing and prevent overvoltage. The voltage between this pin and CAPRTN is digitized and is read in the meas_vcap1 register.

PIN FUNCTIONS

CAP2 (Pin 17): Second Supercapacitor Pin. The top plate of the second supercapacitor and the bottom plate of the third supercapacitor are connected to this pin through a shunt resistor. CAP2 and CAP1 are used to measure the voltage across the second supercapacitor and to shunt current around the capacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP1. The voltage between this pin and CAP1 is digitized and is read in the meas_vcap2 register.

CAP3 (Pin 18): Third Supercapacitor Pin. The top plate of the third supercapacitor and the bottom plate of the fourth supercapacitor are connected to this pin through a shunt resistor. CAP3 and CAP2 are used to measure the voltage across the third supercapacitor and shunt current around the capacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP2. The voltage between this pin and CAP2 is digitized and is read in the meas_vcap3 register.

CAP4 (Pin 19): Fourth Supercapacitor Pin. The top plate of the fourth supercapacitor is connected to this pin through a shunt resistor. CAP4 and CAP3 are used to measure the voltage on the capacitor and shunt current around the supercapacitor to provide balancing and prevent overvoltage. If not used, this pin should be shorted to CAP3. The voltage between this pin and CAP3 is digitized and is read in the meas_vcap4 register. The capacitance test current set by the ITST pin is pulled from this pin.

CFP (Pin 20): VCAPP5 Charge Pump Flying Capacitor Positive Terminal. Place a 6.3V 0.1µF between CFP and CFN.

CFN (Pin 21): VCAPP5 Charge Pump Flying Capacitor Negative Terminal. Place a 6.3V 0.1µF between CFP and CFN.

VCAPP5 (Pin 22): Charge Pump Output. The internal charge pump drives this pin to V_{CAP} + $INTV_{CC}$. It is used as the high side rail for the OUTFET gate drive and charge current sense amplifier. Connect a 6.3V 0.1µF capacitor from VCAPP5 to V_{CAP}.

OUTFET (Pin 23): Output Ideal Diode Gate Drive Output. This pin controls the gate of an external N-channel MOSFET used as an ideal diode between V_{OUT} and V_{CAP}. The gate drive receives power from the internal charge pump output VCAPP5. Connect the source of the N-channel MOSFET to V_{CAP} and the drain to V_{OUT}. If the output ideal diode MOSFET is not used, OUTFET should be left floating.

V_{CAP} (Pin 24): Supercapacitor Stack Voltage and Charge Current Sense Amplifier Negative Input. Connect this pin to the top of the supercapacitor stack. The voltage at this pin is digitized and is read in the meas_vcap register.

ICAP (Pin 25): Charge Current Sense Amplifier Positive Input. The ICAP and V_{CAP} pins measure the voltage across the sense resistor, R_{SNSC}, to provide instantaneous current signals for the control loops and ESR measurement system. The maximum charge current is $32mV/R_{SNSC}$. The voltage between this pin and V_{CAP} is the charging/discharge current as read in the meas_ichg register.

VCC2P5 (Pin 26): Internal 2.5V Regulator Output. This regulator provides power to the internal logic circuitry only. Decouple this pin to SGND with a minimum 1µF low ESR ceramic capacitor.

SW (Pin 27): Switch Node Connection to the Inductor. The negative terminal of the boot-strap capacitor, CB, is connected to this pin. The voltage on this pin is also used as the source reference for the top side N-channel MOSFET gate drive. In step-down mode, the voltage swing on this pin is from a diode (external) forward voltage below ground to V_{OUT}. In step-up mode, the voltage swing is from ground to a diode forward voltage above V_{OUT}.

TGATE (Pin 28): Top Gate Driver Output. This pin is the output of a floating gate driver for the top external N-channel MOSFET. The voltage swing at this pin is ground to V_{OUT} + DRV_{CC}.

BST (Pin 29): TGATE Driver Supply Input. The positive terminal of the boot-strap capacitor, CB, is connected to this pin. This pin swings from a diode voltage drop below DRV_{CC} up to V_{OUT} + DRV_{CC}.

BGATE (Pin 30): Bottom Gate Driver Output. This pin drives the bottom external N-channel MOSFET between PGND and DRV_{CC}.

DRV_{CC} (Pin 31): Power Rail for the Bottom Gate Driver. Connect to $INTV_{CC}$ or to an external supply. Decouple this pin to ground with a minimum 6.3V 2.2µF low ESR ceramic capacitor. Do not exceed 5.5V on this pin.

PIN FUNCTIONS

$INTV_{CC}$ (Pin 32): Internal 5V Regulator Output. The control circuits and gate drivers (when connected to DRV_{CC}) are powered from this supply. If not connected to DRV_{CC}, decouple this pin to ground with a minimum 4.7µF low ESR ceramic capacitor.

V_{OUT} (Pin 33): Output Voltage Supply. This pin supplies power to the LTC3351 after the hot swap start-up has finished. The switching controller charges the capacitor stack from the voltage at this pin and the LTC3351 backs up the voltage at this pin if the input voltage goes outside the OV/UV range or an input current fault occurs.

RETRYB (Pin 34): Retry Comparator Input. The hot swap controller will not attempt to connect V_{IN} and V_{OUT} unless this pin is below 200mV. This high voltage capable pin may be connected to V_{OUT} if the system needs to be fully powered down before repowering after a power loss and backup.

ISNSM (Pin 35): Input Current Sense Pin. This is the negative input for both the hot swap current sense amplifier and the switching charger input current sense amplifier.

ISNSP_CHG (Pin 36): Input Current Sense Pin. This is the positive input for the switching charger input current sense amplifier. The switching charger will reduce charge current to keep the voltage between this pin and ISNSM to 32mV. The current is measured using the sense resistor between this pin and ISNSM and is measured by the ADC and reported in the meas_iin register.

ISNSP_HS (Pin 37): Input Current Sense Pin. This is the positive input for the hot swap input current sense amplifier. The hot swap controller will limit the voltage between this pin and ISNSM to 48mV. This pin is also the input current sense for the circuit breaker function.

CSS (Pin 38): Soft Start and Delay Capacitor Pin. A capacitor from this pin to V_{OUT} determines both the maximum dV/dt of V_{OUT} during the power up and the debounce delay from OV and UV becoming good before attempting to reconnect V_{IN} and V_{OUT}.

SRC (Pin 39): Hot Swap/Input FETs Source Pin. This pin senses the source voltage of the hot swap and input FETs.

HS_GATE (Pin 40): Hot Swap/Input FETs Gate Pin. This pin controls the external hot swap/input FETs. This pin is pulled up to, at most, V_{INTVCC} above the V_{OUT} pin.

V_{IN} (Pin 41): External DC Power Source Input and Sense Pin. For V_{IN} voltages greater than 8V, a 100Ω resistor in series with this pin is required. The voltage at this pin is digitized and is reported in the meas_vin register.

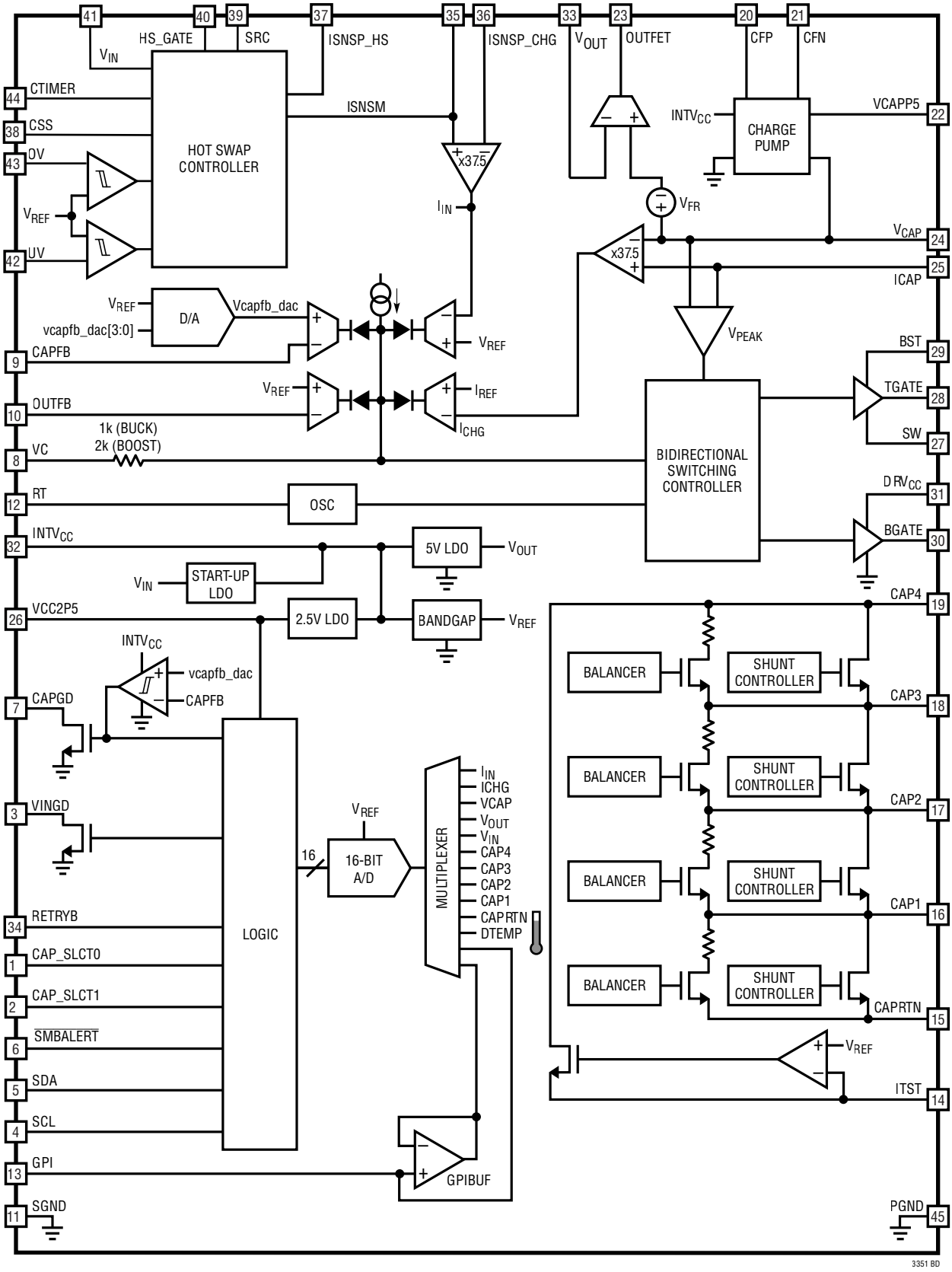
UV (Pin 42): Power-Fail Comparator Input. When the voltage at this pin drops below $V_{UV(TH)}$, the hot swap controller is disconnected, the part enters backup mode and VINGD is pulled low.

OV (Pin 43): Power-Fail Comparator Input. When the voltage at this pin exceeds $V_{OV(TH)}$, the hot swap controller is disconnected, the part enters backup mode and VINGD is pulled low.

CTIMER (Pin 44): Fault and Retry Timing Capacitor. A capacitor from this pin to SGND programs the fault and retry timing. During an over current fault condition this capacitor is charged with $I_{TIMER(UP)}$ (400µA). Once this pin voltage exceeds $V_{TIMER(TH)}$ (1.2V) a fault is declared and V_{OUT} is disconnected from V_{IN}. This pin is continuously discharged with $I_{TIMER(DN)}$ (2µA), and once it discharges to 300mV, and RETRYB is low, the hot swap controller will again attempt to reconnect V_{IN} and V_{OUT}.

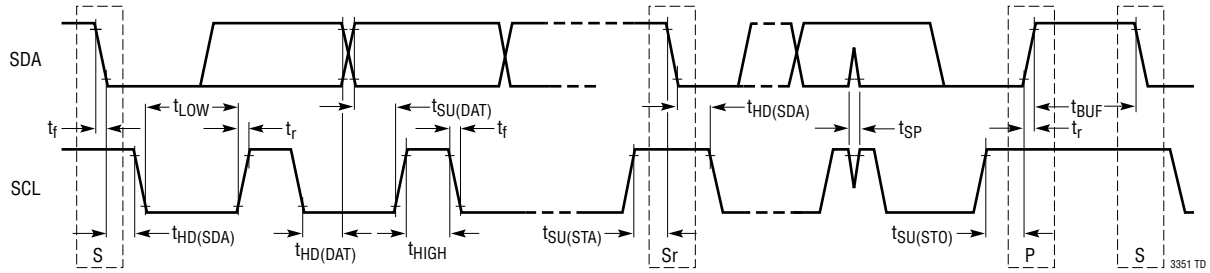
PGND (Exposed Pad Pin 45): Power Ground. For rated thermal performance connect the exposed pad to a continuous ground plane on the second layer of the printed circuit board by several vias directly under the LTC3351. Connect the exposed pad to the SGND pin on top copper.

BLOCK DIAGRAM



TIMING DIAGRAM

Definition of Timing for F/S Mode Devices on the I²C Bus



S = START, Sr = REPEATED START, P = STOP

I²C/SMBus Legend

S	START CONDITION
Sr	REPEATED START CONDITION
Rd	READ (BIT VALUE OF 1)
Wr	WRITE (BIT VALUE OF 0)
A	ACKNOWLEDGE
N	NACK
P	STOP CONDITION
PEC*	PACKET ERROR CODE
	MASTER TO SLAVE
	SLAVE TO MASTER

SMBus WRITE WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	P

SMBus WRITE WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	A	P

SMBus READ WORD PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	N	P

SMBus READ WORD WITH PEC PROTOCOL

S	SLAVE ADDRESS	Wr	A	COMMAND CODE	A	Sr	SLAVE ADDRESS	Rd	A	DATA BYTE LOW	A	DATA BYTE HIGH	A	PEC*	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	N	P

SMBus ALERT RESPONSE ADDRESS PROTOCOL WITH PEC

S	ALERT RESPONSE ADDRESS	Rd	A	DEVICE ADDRESS	Rd	A	PEC*	N	P

*USE OF PACKET ERROR CHECKING IS OPTIONAL

OPERATION

Introduction

The LTC3351 is a highly integrated backup power controller and system monitor. It features a bidirectional switching controller, hot swap controller, output ideal diode, supercapacitor shunts/balancers, under and over voltage comparators, a 16-bit ADC, and I^2C/SMBus programmability with status reporting.

If V_{IN} is within externally programmable UV/OV threshold voltages, the hot swap controller connects V_{IN} to V_{OUT} and the synchronous switching controller operates in step-down mode charging a stack of supercapacitors. A programmable input current limit ensures that the supercapacitors will automatically be charged at the highest possible charge current that the input can support. If V_{IN} goes outside the UV/OV thresholds, or if the hot swap controller's circuit breaker trips, or if a simulated failure is requested, then the hot swap controller will disconnect V_{OUT} from V_{IN} and the synchronous controller will run in reverse as a step-up converter to deliver power from the supercapacitor stack to V_{OUT}.

An ideal diode controller drives an external MOSFET to provide a low loss power path from V_{CAP} to V_{OUT}. This ideal diode works seamlessly with the bidirectional controller to provide power from the supercapacitors to V_{OUT}. The hot swap controller utilizes two back-to-back MOSFETs to control inrush, provide a short circuit breaker function and prevent back driving V_{IN} while in backup mode.

The LTC3351 provides balancing and overvoltage protection to a series stack of one to four supercapacitors. The internal capacitor voltage balancers eliminate the need for external balance resistors. Overvoltage protection is provided by shunt regulators that use an internal switch and an external resistor across each supercapacitor.

The LTC3351 monitors system voltages, currents, and its own die temperature. A general purpose input (GPI) pin is provided to measure an additional system parameter or implement a thermistor measurement. In addition, the LTC3351 can measure the capacitance and equivalent series resistance of the supercapacitor stack. This provides indication of the health of the supercapacitors and, along with the V_{CAP} voltage measurement, provides information on the total energy stored and the maximum power that can be delivered.

Operations Example

The LTC3351 is a highly integrated circuit with many features and operating modes. To better explain the operations of the LTC3351, a simplified example will be used. This example is graphically shown in Figure 1 and will be referred to throughout. Due to the widely varying time scales of the events with which the LTC3351 operates, the time axis of Figure 1 is not to scale.

The example begins with V_{IN} and V_{CAP} at 0V. V_{IN} is applied suddenly at the point labeled "hot plug". There is a very small inrush current into the drain capacitance of the hot swap FET connected to V_{IN}, this is shown as a small "spike" on the I_{IN} waveform. This "spike" is very small in either duration or amplitude, depending on the rise rate of V_{IN}. During the time labeled "debounce", the LTC3351 qualifies the input as good using the UV and OV comparators and expires an input debounce timer using the C_{SS} pin. Once this debounce time has passed, the LTC3351 begins turning on the hot swap FETs to charge the capacitance on V_{OUT} in a controlled way, during which time both the input current and rise rate of V_{OUT} are controlled. This results in a low constant I_{IN} current while the V_{OUT} capacitance is charged.

Once V_{OUT} has been charged to V_{IN}, the charger is allowed to start charging the supercapacitors. For this example; at the beginning of the charge cycle the supercapacitors are fully discharged. The charger will begin with constant current charging of the supercapacitors. Since the capacitor voltage is very low, the power delivered is very low. This low power delivery results in a low input current despite high charge current. As the voltage on the supercapacitors rises, the delivered power also rises and thus the input current also rises. This constant current phase of charging is labeled "CC Charging."

In this example I_{OUT}, the downstream system load, turns on during the constant current phase of charging. When this happens is outside the control of the LTC3351 and its timing in this example is arbitrary. Since output current

OPERATION

is supplied from V_{IN} via the hot swap FETs this step in load current directly causes a step in input current. The charge current is unaffected by this load step because the LTC3351 is not in input current limit.

As the supercapacitors charge, their voltage increases and the input current increases due to the increasing power being delivered to the supercapacitors. In this example the increasing input current reaches the input current limit at the beginning of the time labeled "CP charging." With a constant input voltage, input current limit causes the LTC3351 to effectively have an input power limit. Depending on the settings of the input current limit, charge current limit, charge voltage, system load current and input voltage the charging phase of operation may or may not reach the input current limit.

During the constant power phase of charging, the charge current decreases as the charge voltage increases to maintain constant input power. This results in a slowing rate of charge as the charger approaches constant voltage charging. Once V_{CAP} reaches the programmed charge voltage, the constant voltage phase of charging begins. This is labeled "CV charging."

During constant voltage charging, current is being delivered to the supercapacitors and there is a voltage drop across their internal ESR (equivalent series resistance). The LTC3351 holds the V_{CAP} voltage constant during this phase. Holding the V_{CAP} voltage constant allows the voltage across this ESR to fall towards zero as the internal capacitance is charged to V_{CAP}. During this time the charge current decays toward the leakage current of the capacitors.

The LTC3351 CV charges forever, waiting for a power failure, while keeping the capacitors charged, balanced and ready for backup. While fully charged and standing by for backup, the LTC3351 can also measure the ESR and capacitance of the batteries if requested (not shown in Figure 1). This is the condition the LTC3351 is likely to spend most time in, assuming input power loss is infrequent as is typically the case.

When power does fail, as labeled "power failure" in Figure 1, the OV or UV comparators detect the power failure at the input. The hot swap FET is turned off to isolate V_{OUT} from V_{IN}. Once the FET is off, V_{OUT} immediately falls to V_{CAP} (or the programmed boost voltage if it is higher, however in

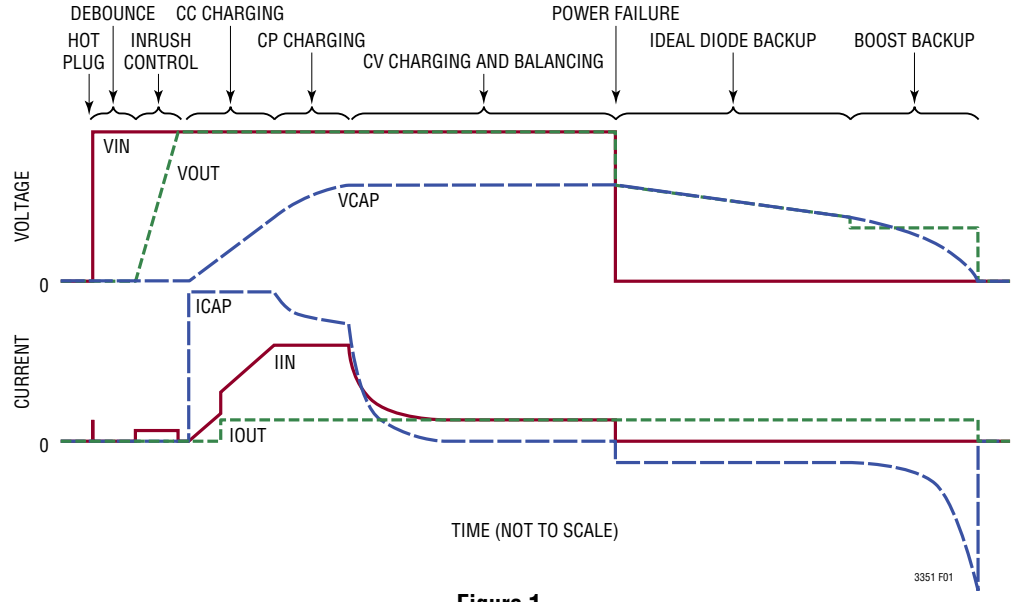


Figure 1.

OPERATION

this example it is not). The ideal diode FET between V_{CAP} and V_{OUT} is turned on during the time labeled "ideal diode backup." While operating in ideal diode backup, power is supplied directly from the capacitors without conversion. V_{CAP} is discharged during this time and V_{OUT} falls along with V_{CAP}.

Once the V_{OUT} voltage approaches the programmed boost voltage, the boost converter is turned on and the ideal diode turned off. The boost converter then supplies the output at constant voltage. As the capacitor voltage falls, the capacitor current must increase to supply the constant power load at V_{OUT}. This continues until either the boost reaches its current limit or exhausts the available energy in the capacitors. This time is labeled "boost backup."

Bidirectional Switching Controller—Step-Down Mode

The bidirectional switching controller is designed to charge a series stack of supercapacitors (Figure 2). Charging proceeds at a constant current until the supercapacitors reach their maximum charge voltage determined by the CAPFB servo voltage and the resistor divider between V_{CAP} and CAPFB. The maximum charge current is determined by the value of the sense resistor, R_{SNSC}, connected in series with the inductor. The charge current loop servos the voltage across the sense resistor to 32mV. When charging begins, an internal soft-start ramp gradually increases the charge current. The V_{CAP} voltage and charge current are read from the meas_vcap and meas_ichg registers, respectively.

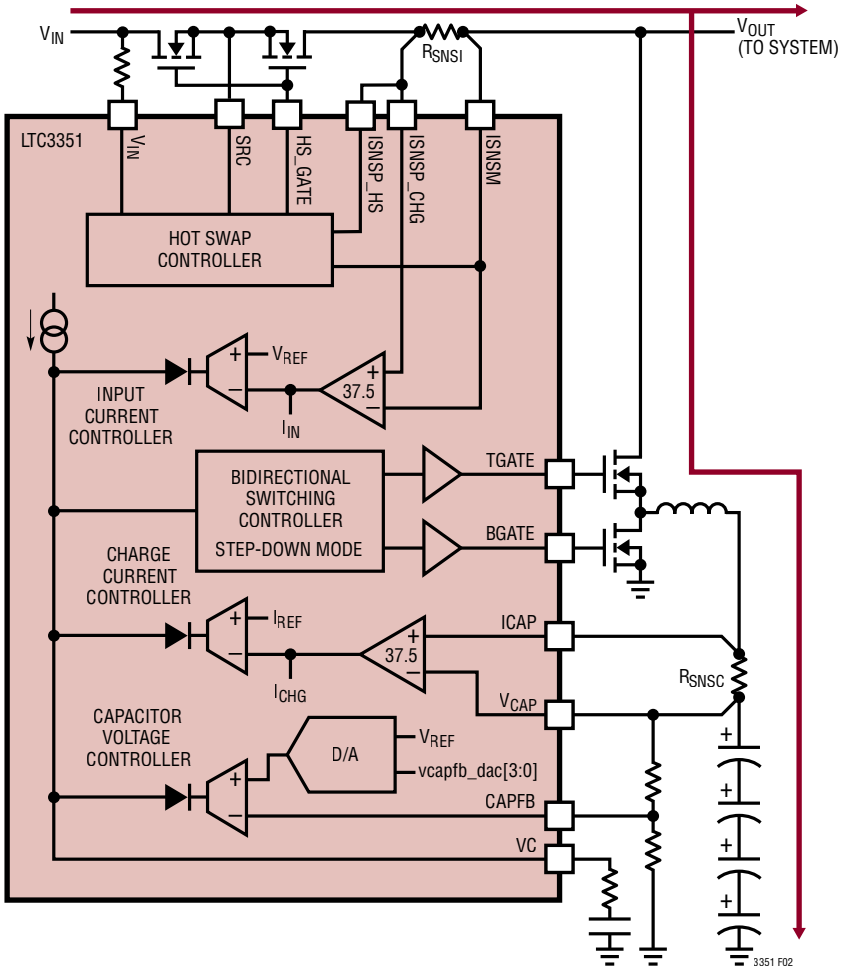


Figure 2. Power Path Block Diagram - Power Available from V_{IN}

OPERATION

The LTC3351 provides constant power charging (for a fixed V_{IN}) by limiting the input current drawn by the switching controller in step-down mode. The charger input current limit will reduce charge current to limit the voltage between ISNSP_CHG and ISNSM, typically across R_{SNSI}, to 32mV. If the combined system load plus supercapacitor charge current is large enough to cause the switching controller to reach the programmed input current limit, the input current limit loop will reduce the charge current by precisely the amount necessary to enable the external load to be satisfied. Even if the charge current is programmed to exceed the allowable input current, the input current limit will not be violated; the supercapacitor charger will reduce its current as needed. The input current is read from the meas_iin register.

Bidirectional Switching Controller—Step-Up Mode

The bidirectional switching controller acts as a step-up converter to provide power from the supercapacitors to V_{OUT} when input power is unavailable (Figure 3). VINGD low enables step-up mode. V_{OUT} regulation is set by a resistor divider between V_{OUT} and OUTFB. To disable step-up mode tie OUTFB to $INTV_{CC}$.

Step-up mode is often used with the output ideal diode. If the V_{OUT} regulation voltage is set below the capacitor stack voltage, upon removal of input power, power to V_{OUT} is provided from the supercapacitor stack via the output ideal diode. V_{CAP} and V_{OUT} will decrease as the load current discharges the supercapacitor stack. The output ideal diode will shut off and V_{OUT} will fall a PN diode (~700mV) below V_{CAP} when the voltage on OUTFB falls below 1.3V ($V_{OUTFB(TH)}$). If OUTFB falls below 1.2V when the output ideal diode shuts off, the synchronous step-up controller will turn on immediately to regulate OUTFB to 1.2V by providing power from the supercapacitor stack. If OUTFB is above 1.2V when the output ideal diode shuts off, the load current will flow through the body diode of the output ideal diode N-channel MOSFET for a period of time until OUTFB falls to 1.2V.

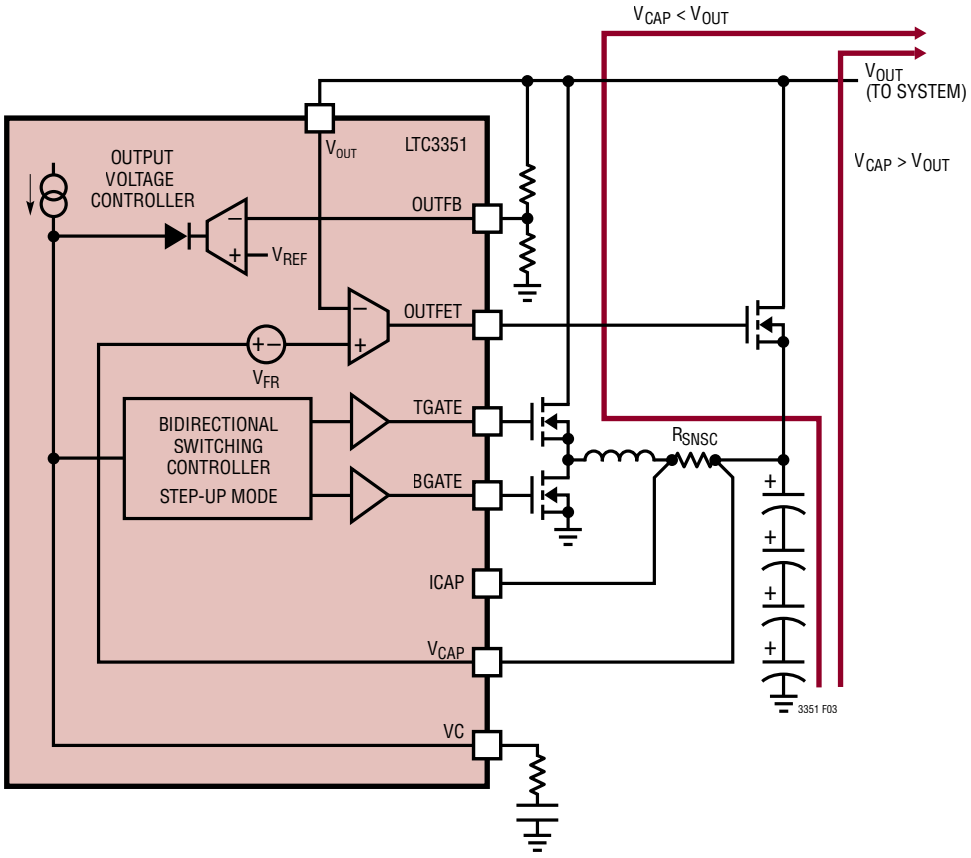


Figure 3. Power Path Block Diagram - Power Backup

OPERATION

The synchronous controller in step-up mode will run nonsynchronously when V_{CAP} is less than 90mV (V_{DUVLO} falling) below V_{OUT}. It will run synchronously when V_{CAP} falls 200mV (V_{DUVLO} rising) below V_{OUT}.

Hot Swap Controller

Upon applying power to V_{IN}, the LTC3351 will immediately turn on a strong pull down on the HS_GATE pin to prevent the external FETs from conducting current from V_{IN} to V_{OUT}. During the initial V_{IN} rise the LTC3351 may limit the rise rate of the voltage at the V_{IN} pin by drawing current through the 100Ω resistor in series with the pin. The LTC3351 will then drive the $INTV_{CC}$ pin to 3.6V using current from the V_{IN} pin. Once the $INTV_{CC}$ voltage is greater than 3.3V the hot swap turn-on sequence will begin.

If both the under voltage (UV) and (OV) comparators are in range, the CSS pin will begin to source 1µA of current, charging the C_{SS} capacitor. Once the CSS pin reaches 1.2V and the RETRYB pin is below 200mV ($V_{TH(RETRYB)}$) the LTC3351 will begin the process of connecting V_{IN} and V_{OUT} using the external FETs. The LTC3351 will begin pulling up on the HS_GATE pin using 24µA ($I_{HS\_GATE(UP)}$) of current. As V_{OUT} begins to rise, the capacitor from V_{OUT} to the CSS pin provides feedback to the LTC3351 about the rise rate of the output. Therefore, the sizing of the C_{SS} capacitor determines the maximum slew rate of V_{OUT} and the inrush current.

During the ramp up of HS_GATE and V_{OUT}, both the current limit and the circuit breaker are active. V_{IN} to V_{OUT} differential foldback reduces both the current limit and circuit breaker threshold while charging the output capacitor; this reduces the required SOA of the hot swap FETs.

If, at any time, the under voltage (UV) or overvoltage (OV) comparators go out of range, or if the CTIMER pin reaches 1.2V ($V_{TIMER(TH)}$), the LTC3351 will declare a fault and quickly turn off the external FET by grounding HS_GATE. The FET sources will be kept within a safe voltage of the gate by the SRC pin. Once a fault is declared the LTC3351's backup controller will begin supplying power to V_{OUT} from the energy stored in the capacitor stack. This will continue until either a new turn-on sequence occurs, the supercapacitor stored energy is depleted, or the boost is disabled via I^2C/SMBus.

The LTC3351 will limit the current from V_{IN} to V_{OUT} through the external FETs using the voltage across the current sense resistor(s) sensed using the ISNSP_HS and ISNSM pins. When V_{OUT} is within 1V of V_{IN} the LTC3351 will limit the voltage across the ISNSP_HS and ISNSM pins to 48mV ($V_{ILIM(TH)}$). To limit power in the external FET this limit is folded back to 10mV as the voltage from V_{IN} to V_{OUT} increases from 1V to 10V. Above 10V the limit remains at 10mV. This current limit is separate from the switching charger's input current limit. The switching charger's input current limit is unaffected by the above described fold back.

The LTC3351's CTIMER pin will source current when the input current is within 1.66% of the input current limit. As with the input current limit, this threshold is folded back as the voltage from V_{IN} to V_{OUT} increases. The current sourced from the CTIMER pin to the C_{TIMER} capacitor is about 400µA ($I_{TIMER(UP)}$). Once the voltage at the CTIMER pin exceeds 1.2V ($V_{TIMER(TH)}$ rising) a fault is declared and the turn-off sequence is initiated. The CTIMER pin has a static 2µA ($I_{TIMER(DN)}$) load that discharges the C_{TIMER} capacitor. Once a fault is declared the CTIMER pin must fall below 300mV before the turn-on sequence is re-attempted.

RETRYB Pin

The LTC3351's RETRYB pin determines if the LTC3351 tries to connect V_{IN} and V_{OUT} after a fault. The faults are UV, OV, circuit breaker (CTIMER), or a simulated fault programmed via the I^2C/SMBus port by setting ctl_hotswap_disable. If the RETRYB pin is low ($V_{TH(RETRYB)}$ below 200mV) the LTC3351 will try to connect V_{IN} and V_{OUT} using the hot swap controller. The RETRYB pin is high voltage tolerant and high impedance. A divider from V_{OUT} to RETRYB allows a precise threshold to be set. This can be used to ensure the system completely powers down following a failure before re-powering.

VINGD Pin

The VINGD pin indicates that the input voltage is within the OV/UV range and the system is powered from V_{IN}. For VINGD to be high, the voltage at UV must be above 1.2V (V_{OV} rising) the voltage at OV must be below 1.17V (V_{UV} falling), the circuit breaker must not be tripped, the hot swap must not be disabled via I^2C/SMBus, and the hot

OPERATION

swap controller must have completed connecting V_{IN} and V_{OUT}. The state of the VINGD pull down is read from the vingd bit in the sys_status register.

If UV is set to a level near or less than the charge voltage of the capacitors, V_{IN} becomes high impedance and the V_{OUT} load is very low, it is possible for a small amount of current to flow from V_{CAP} to V_{IN} through V_{OUT} due to the maximum duty cycle operation. In this condition, the high duty cycle buck is effectively a reverse low duty cycle boost. The boost has a small amount of output current that holds V_{IN} above V_{CAP} and possibly UV, causing the part to falsely indicate VINGD. Eventually V_{CAP} will be discharged below the programmed UV threshold and VINGD will indicate correctly. This situation can be avoided by programming the UV threshold at least 3% above the capacitor charge voltage.

Ideal Diode

The LTC3351 has an ideal diode controller that drives an external N-channel MOSFET between V_{CAP} and V_{OUT}. The ideal diode consists of a precision amplifier that drives the gates of N-channel MOSFETs whenever the voltage at V_{OUT} is approximately 30mV (V_{FR}) below the voltage at V_{CAP}. Within the amplifier's linear range, the small-signal resistance of the ideal diode will be quite low, keeping the forward drop near 30mV. At higher current levels, the MOSFETs will be in full conduction.

The ideal diode provides a path for the supercapacitors to power V_{OUT} when V_{IN} is unavailable or the hot swap controller is disconnected. In addition to a Fast-Off comparator, the ideal diode also has a Fast-On comparator that turns on the external MOSFET when V_{OUT} drops 65mV (V_{FTO}) below V_{CAP}. The ideal diode will shut off when OUTFB is just above regulation allowing the synchronous controller to power V_{OUT} in step-up mode.

Gate Drive Supply (DRV_{CC})

The bottom gate driver is powered from the DRV_{CC} pin, which is normally connected to the $INTV_{CC}$ pin. An external LDO can also be used to power the gate drivers to minimize power dissipation inside the LTC3351. See the Applications Information section for details.

Switcher/Charger Undervoltage Lockout (UVLO)

Internal undervoltage lockout circuits monitor both the $INTV_{CC}$ and DRV_{CC} pins. The switching controller is kept off until $INTV_{CC}$ rises above V_{UVLO} (4.3V) and DRV_{CC} rises above $V_{DRVUVLO}$ (4.2V). The controller is disabled if either $INTV_{CC}$ falls below 4V or DRV_{CC} falls below 3.9V.

Charging is disabled until V_{OUT} is V_{DUVLO} (200mV) above the supercapacitor voltage and VINGD is high. Charging is disabled when V_{OUT} falls to within 90mV of the supercapacitor voltage or when VINGD is low.

R_T Oscillator and Switching Frequency

The R_T pin is used to program the switching frequency. A resistor, R_T, from this pin to ground sets the switching frequency according to:

$$f_{SW}(MHz) = \frac{53.5}{R_T(k\Omega)}$$

R_T also sets the scale factor for the capacitor measurement value reported in the meas_cap register, described in the ESR and Capacitance Measurement section of this data sheet.

Switching Controller Input Overvoltage Protection

Input overvoltage protection turns off both switching controller switches if V_{IN} exceeds V_{OVLO} (38.6V). The controller will resume switching if V_{IN} falls below 37.2V. The hot swap controller is unaffected by this and uses its own programmable OV threshold.

V_{CAP} DAC

The feedback reference for the CAPFB servo point is programmed using an internal 4-bit digital-to-analog converter (DAC). The reference voltage is programmable from 0.6375V ($V_{CAPFBLO}$) to 1.2V ($V_{CAPFBHI}$) in 37.5mV increments. The DAC defaults to 0xA (V_{CAPFB_DEF} 1.0125V) and is programmed via the vcapfb_dac register.

Supercapacitors lose capacitance as they age. By initially setting the V_{CAP} DAC to a low setting, the final charge voltage on the supercapacitors can be increased as they age to maintain a constant level of stored backup energy throughout the lifetime of the supercapacitors. The

OPERATION

capacitance and ESR measurement system may temporarily increase this DAC to a value as much as full scale (1.2V) during the ESR test.

If using the capacitance and ESR test, the highest usable DAC setting will be determined by the voltage increase between that setting and 1.2V at the CAPFB pin, wherein the capacitor stack's voltage increases by 1.25 times the voltage specified in cap_delta_v_setting.

Charge Status Indication

The LTC3351 includes a comparator to report the status of the supercapacitors via an open-drain NMOS transistor on the CAPGD pin. This pin pulls to ground until the CAPFB pin voltage rises to within nominally 8% of the V_{CAP} DAC setting. Once the CAPFB pin is above this threshold, the CAPGD pin goes high impedance. The output of this comparator may also be read from the cappg bit in the sys_status register.

Capacitor Voltage Balancer

The LTC3351 has an integrated active stack balancer. This balancer slowly balances all of the capacitor voltages to within approximately 10mV of each other. This maximizes the life of the supercapacitors by keeping the voltage on each as low as possible to achieve the needed total stack voltage. When the difference between any two capacitor voltages exceeds approximately 10mV, the capacitor with the largest voltage is discharged with a resistive balancer (approximately 75Ω until all capacitor voltages are within 10mV). The balancers can be disabled by setting the ctl_disable_balancer bit.

Capacitor Shunt Regulators

During charging, the capacitors are protected from overvoltage. The capacitors in the stack will not have exactly the same capacitance due to manufacturing tolerances or uneven aging. This will cause the capacitor voltages to increase at different rates with the same charge current. If this mismatch is severe enough or if the capacitors are being charged to near their maximum voltage, it becomes necessary to limit the voltage increase on some capacitors while still charging the other capacitors. Up to 500mA of current may be shunted around a capacitor whose voltage is approaching the programmable shunt voltage. This shunt current reduces the charge rate of that capacitor relative to the other capacitors. If a capacitor continues to approach its shunt voltage, the stack charge current is reduced. This protects the capacitor from overvoltage while still charging the other capacitors, although at a reduced rate of charge. When shunting, the internal switch may be on more than 96% duty cycle. The shunts are disabled by setting the ctl_disable_shunt bit. The shunt voltage is programmable in the vshunt register. Shunt voltages may be programmed in 183.5µV increments. If a voltage greater than 3.6V is programmed, the charge current will be reduced as that voltage is approached but the shunt will not turn on. The default value is 0x3999, resulting in a shunt voltage of approximately 2.7V. See Register Map for more information.

I²C/SMBus and $\overline{\text{SMBALERT}}$

The LTC3351 contains an I²C/SMBus compatible port. This port allows communication with the LTC3351 for configuration and reading back telemetry data. The port supports two SMBus formats, read word and write word. These may be used with or without the packet error code (PEC) feature. Refer to the SMBus specification for details of these formats and PEC. The registers accessible via this port are organized on an 8-bit address bus and each register is 16 bits wide. The "command code" (or sub-address) of the SMBus read/write word formats is the 8-bit address of each of these registers. The address of the LTC3351 is 0b0001001.

The $\overline{\text{SMBALERT}}$ pin is asserted (pulled low) whenever an enabled limit is exceeded or when an enabled status event happens (see the Limit Checking and Alarms and the Monitor Status Register sections of this data sheet). The LTC3351 will de-assert the $\overline{\text{SMBALERT}}$ pin only after responding to a SMBus alert response address (ARA), an SMBus protocol used to respond to a $\overline{\text{SMBALERT}}$. The host will read from the ARA (0b0001100) and each part asserting $\overline{\text{SMBALERT}}$ will begin to respond with its address. The responding parts arbitrate in such a way that only the part with the lowest address responds completely. Only when a part has responded with its entire address does it release the $\overline{\text{SMBALERT}}$ signal. If multiple parts are asserting the $\overline{\text{SMBALERT}}$ signal then multiple reads

OPERATION

from the ARA are needed. For more information refer to the SMBus specification.

Details on the registers accessible through this interface are available in the Register Map section of this data sheet.

For I^2C masters unable to create the repeated start needed for the read and write word protocols, a stop followed by a start may be substituted.

Analog-to-Digital Converter

The LTC3351 has an integrated 16-bit sigma-delta analog-to-digital converter (ADC). This converter is automatically multiplexed between the measured channels. Its results are stored in registers accessible via the I^2C/SMBus port. There are 11 channels measured by the ADC, each of which takes approximately 800µs to measure. In addition to providing status information about the system voltages and currents, some of these measurements are used by the LTC3351 to balance, protect (shunt), and measure the capacitors in the stack.

The result of each analog-to-digital conversion is stored in a 16-bit register as a signed, two's complement number.

To reduce average quiescent current, the effective duty cycle of the ADC can be reduced by programming adc_wait_vin and/or adc_wait_backup. Each register inserts a delay in the ADC's measurement cycle during its respective mode of operation. Each LSB of these registers has a weight of approximately 400µs. At some times, such as when shunting or making capacitance and ESR measurement, these settings may be temporarily ignored. Measurements of individual channels may be enabled or disabled by setting the appropriate bit in adc_backup_ch_en_reg and adc_vin_ch_en_reg.

The measurements from the ADC are stored to meas_vcap1, meas_vcap2, meas_vcap3, meas_vcap4, meas_gpi, meas_vin, meas_vcap, meas_vout, meas_iin, meas_ichg and meas_dtemp.

ESR and Capacitance Measurement

The LTC3351 monitors the health of a supercapacitor stack by measuring the capacitance and the ESR. Both the capacitance and ESR are measured in a single test. The LTC3351 measures ESR by applying and measuring a current step with the high efficiency charger and measuring the change in voltage. The capacitance is measured by discharging a fixed voltage with a known current and measuring time.

The ESR and capacitance measurement sequence, initiated by setting ctl_start_cap_esr_meas, is:

1. The mon_meas_active and mon_esr_meas_active bits become high if the capacitors are charged, otherwise, mon_capesr_pending becomes high.
2. The charger is configured to charge at a pre-set current up to a full vcapfb_dac setting, this current is set using an 8 bit DAC controlled either by:
   a. An internal algorithm that selects the optimal current based on the previous capacitor measurement (assuming the LTC3351 is not in input current limit)
   b. An override setting, programmed in esr_i_override, is used if non-zero. If it is likely the LTC3351 will operate in input current limit while charging, then this should be set low enough to avoid input current limit.
3. The measurement system waits esr_i_on_settling for the current and capacitor effects to stabilize. Each LSB of esr_i_on_settling is 1024 switcher periods.
4. A series of measurements of capacitor voltages and charge currents are made. The charger is then temporarily shut off.
5. The measurement system waits esr_i_off_settling for the current and capacitor effects to stabilize. Each LSB of esr_i_off_settling is 1024 switcher periods.
6. A series of measurements of capacitor voltages and charger currents are made. From these measurements, and the previous measurements, the ESR is calculated and stored in meas_esr.
7. The capacitors will be charged to at least 1.25 • cap_delta_v_setting above their initial voltage (as measured at step 1).

   If the capacitor voltage reaches the maximum charge voltage (V_{CAPFB} = 1.2V), then the test will stop trying to charge and continue without fully charging. The test may fail later due to this. If the charger is unable

OPERATION

to reach 1.25 • cap_delta_v_setting above the initial voltage with capfb less than 1.2V, it will continue trying to charge indefinitely. This may occur if the charger is limited by the input voltage and maximum duty cycle of the buck charger. This may also occur if there is no charge current available due to system load exceeding the input current limit. If either of these conditions occurs, the test will remain in this condition indefinitely.

8. The charger is temporarily disabled. The mon_cap_meas_active bit becomes high, the mon_esr_meas_active bit becomes low and the ITST current is enabled. After a time set by cap_i_on_settling, a series of voltage measurements is made.
9. The capacitor stack is discharged a fixed voltage (set by cap_delta_v_setting) from the voltage measured in the previous step using the ITST current (1.2V/RTST, up to 60mA or 300mW). This voltage is measured using the CAP1-4 pins.
10. The time required to discharge by this fixed voltage is measured. It is then scaled for cap_delta_v_setting and stored as meas_cap.
11. The charger stays off and the ITST current stays on until the stack voltage returns to the voltage set by vcapfb_dac.
12. The charger is turned back on and the ITST current is turned off. The mon_meas_active bit goes low.

Figure 4 shows this sequence graphically.

This measurement is only initiated when the ctl_start_cap_esr_meas bit is set. The results of the measurement can be checked against limits and issue a $\overline{\text{SMBALERT}}$ if limits are exceeded, see the Limit Checking and Alarms section of this data sheet.

The measurement of Capacitance and ESR can fail if power fails during the test or if the capacitor stack is discharged below the CAPGD threshold. The test will also fail if ctl_stop_cap_esr_meas is set. If it does fail, mon_meas_failed will be set.

Monitor Status Register

The LTC3351 has a monitor status register (monitor_status_reg) containing status bits to indicate the state of the capacitance and ESR monitoring system. These bits are set and cleared by the capacitor monitor upon certain events during a capacitor and ESR measurement, as described in the ESR and Capacitance Measurement section.

There is a corresponding monitor status mask register (monitor_status_mask_reg). Writing a one to any of these bits will cause the $\overline{\text{SMBALERT}}$ pin to pull low when the corresponding bit in monitor_status_reg has a rising edge. This allows reduced polling of the LTC3351 when waiting for a capacitance or ESR measurement to complete.

Details of monitor_status_reg and monitor_status_mask_reg can be found in the Register Map section of this data sheet.

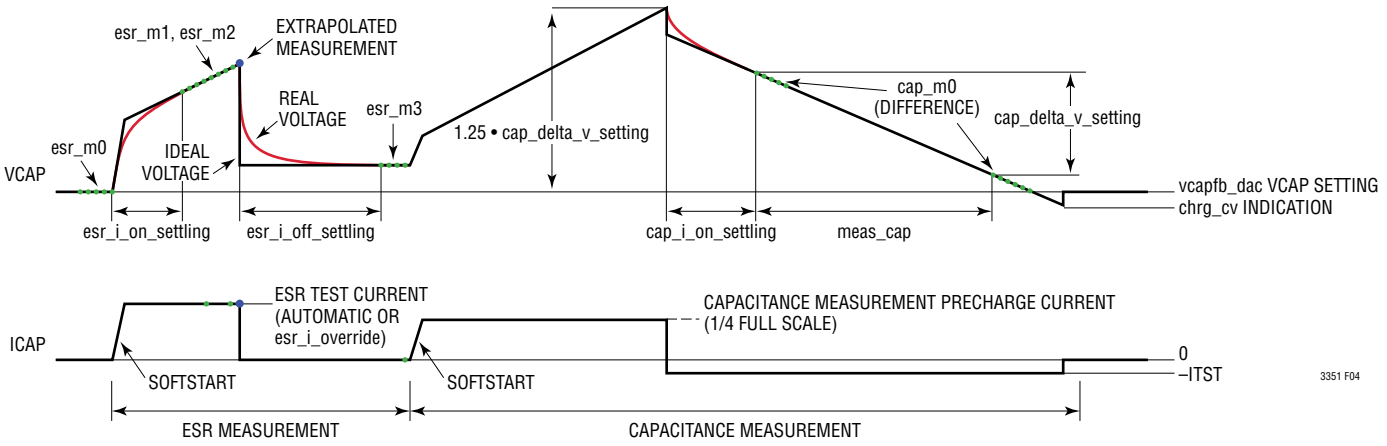


Figure 4.

OPERATION

System Status Register

The sys_status register contains data about the state of the charger, switcher and comparators. Details of this register may be found in the Register Map section of this data sheet.

Limit Checking and Alarms

The LTC3351 has a limit checking function that will check each measured value against I²C/SMBus programmable limits. This feature is optional and all of the limits are disabled by default. The limit checking is designed to simplify system monitoring, eliminating the need to continuously poll the LTC3351 for measurement data.

If a measured parameter goes outside of the programmed level of an enabled limit, the associated bit in the alarm_reg register is set high and the $\overline{\text{SMBALERT}}$ pin is pulled low. This informs the I²C/SMBus host that a limit has been exceeded. The alarm_reg may then be read to determine exactly which programmed limits have been exceeded.

A single ADC is shared between the 11 channels with about 9ms between consecutive measurements of the same channel. In a transient condition, it is possible for these parameters to exceed their programmed levels in between consecutive ADC measurements without setting the alarm.

Once the LTC3351 has responded to an SMBus ARA the $\overline{\text{SMBALERT}}$ pin is released. The LTC3351 will not pull the pin low again until another limit is exceeded. To reset a limit that has been exceeded write a zero to the respective bit in the alarm_reg register. When writing alarm_reg, zeros will clear their respective bits in the register, ones will be ignored.

A number of the LTC3351's registers are used for limit checking. Individual limits are enabled or disabled in alarm_mask_reg. Once an enabled alarm's measured value exceeds the programmed level for that alarm the alarm is set. That alarm may only be cleared by writing a zero to the appropriate bit of alarm_reg. All alarms that have been set and have not yet been cleared may be read in the alarm_reg.

All of the individual measured voltages have a corresponding undervoltage (UV) and overvoltage (OV) alarm level. All of the individual capacitor voltages are compared to the same alarm levels, set in cap_ov_lvl and cap_uv_lvl. The input current measurement has an overcurrent (OC) alarm programmed in iin_oc_lvl. The charge current has an undercurrent alarm programmed in ichg_uc_lvl.

Die Temperature Sensor

The LTC3351 has an integrated die temperature sensor monitored by the ADC and digitized to meas_dtemp. An alarm is configured on die temperature by setting dtemp_cold_lvl and/or dtemp_hot_lvl and enabling their respective alarms in alarm_mask_reg. To convert the code in the meas_dtemp register to degrees Celsius use the following:

$$T_{DIE}\ (°C) = 0.0295 \bullet \text{meas\_dtemp} - 274°C$$

General Purpose Input

The general purpose input (GPI) pin is used to measure an additional system parameter where the voltage on this pin is digitized by the ADC. For high impedance inputs, an internal buffer may be selected and used to drive the ADC. This buffer is enabled by setting the ctl_gpi_buffer_en bit in the ctl_reg register. With this buffer, the input range is limited from 0V to 3.5V. If this buffer is not used, the range is from 0V to 5V, however, the input stage of the ADC will draw about 0.8µA per volt from this pin. The ADC input is a switched capacitor amplifier running at about 2MHz, so this current draw will be at that frequency. The pin current can be eliminated at the cost of reduced range and increased offset by enabling the buffer.

Alarms are available for this pin voltage with levels programmed using gpi_uv_lvl and gpi_ov_lvl. These alarms are enabled using the mask_alarm_gpi_uv and mask_alarm_gpi_ov bits in alarm_mask_reg.

To monitor the temperature of the supercapacitor stack, the GPI pin can be connected to a negative temperature coefficient (NTC) thermistor. A low drift bias resistor is required from $INTV_{CC}$ to GPI and a thermistor is required from GPI to ground. Connect GPI to SGND if not used.

OPERATION

Internal Diodes

The LTC3351 has numerous internal diodes as part of its circuits and ESD protection structures. In normal operation, these diodes are reverse biased. Figure 5 shows all the diodes except the substrate diodes. These substrate diodes have their anode connect to ground and their cathodes connect to every pin except SW.

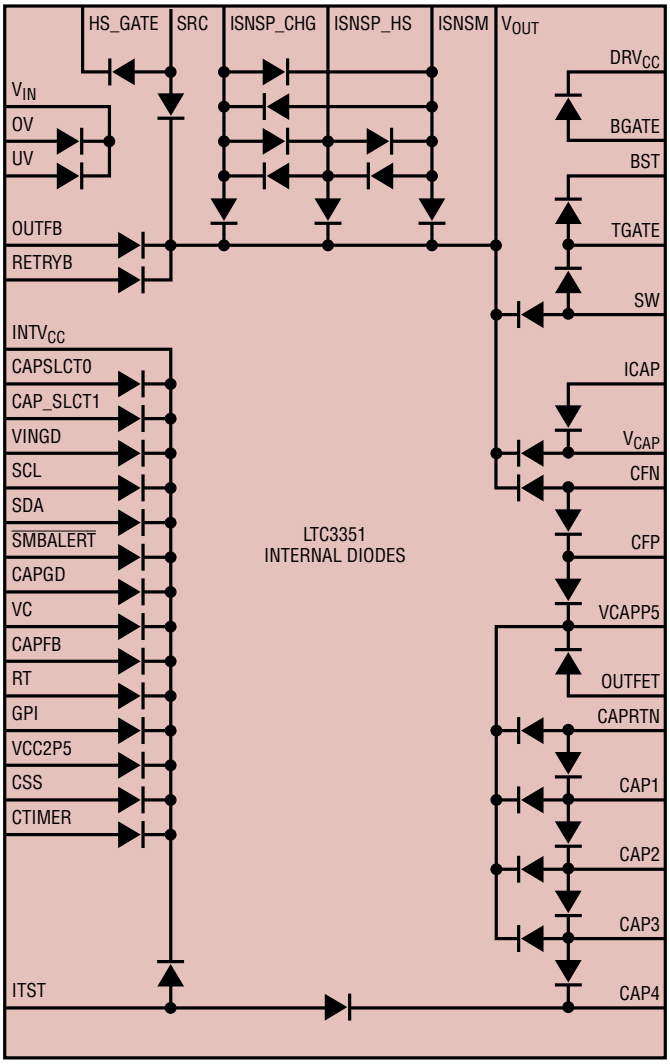


Figure 5.