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LTC3589/LTC3589-1/ LTC3589-2

8-Output Regulator with Sequencing and I²C

FEATURES

- **Triple I²C Adjustable High Efficiency Step-Down DC/DC Converters: 1.6A, 1A/1.2A, 1A/1.2A**
- **High Efficiency 1.2A Buck-Boost DC/DC Converter**
- **Triple 250mA LDO Regulators**
- **Pushbutton ON/OFF Control with System Reset**
- **Flexible Pin-Strap Sequencing Operation**
- **I²C and Independent Enable Control Pins**
- Power Good and Reset Outputs
- Dynamic Voltage Scaling and Slew Rate Control
- Selectable 2.25MHz or 1.12MHz Switching Frequency
- Always-Alive 25mA LDO Regulator
- 8µA Standby Current
- 40-Pin 6mm × 6mm × 0.75mm QFN

APPLICATIONS

- Handheld Instruments and Scanners
- Portable Industrial Devices
- Automotive Infotainment
- Medical Devices
- High End Consumer Devices
- Multirail Systems
- Supports Freescale i.MX53/51, Marvell PXA and Other Application Processors

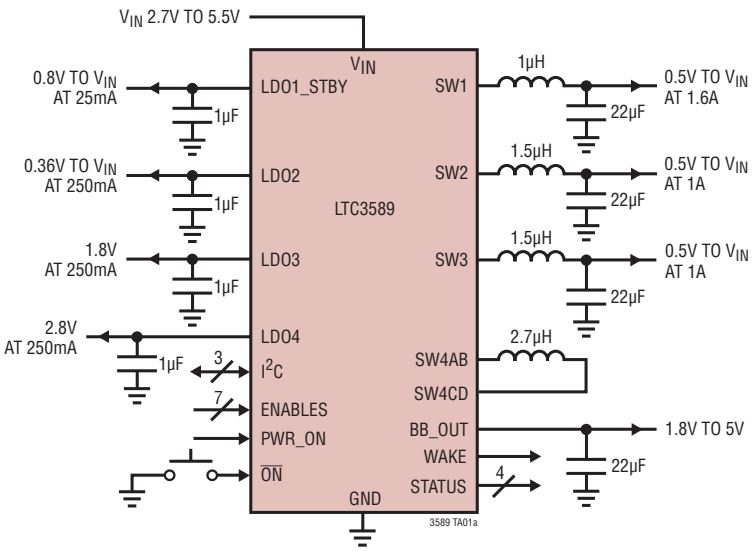
DESCRIPTION

The LTC®3589 is a complete power management solution for ARM and ARM-based processors and advanced portable microprocessor systems. The device contains three step-down DC/DC converters for core, memory and SoC rails, a buck-boost regulator for I/O at 1.8V to 5V and three 250mA LDO regulators for low noise analog supplies. An I²C serial port is used to control enables, output voltage levels, dynamic voltage scaling, operating modes and status reporting. Differences between the LTC3589, LTC3589-1, and LTC3589-2 are summarized in Table 1.

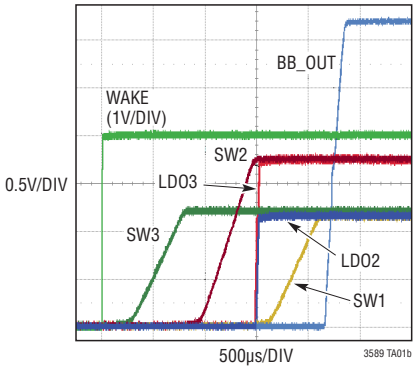
Regulator start-up is sequenced by connecting outputs to enable pins in the desired order or programmed via the I²C port. System power-on, power-off, and reset functions are controlled by pushbutton interface, pin inputs, or I²C interface.

The LTC3589 supports i.MX53/51, PXA and OMAP processors with eight independent rails at appropriate power levels. Other features include interface signals such as the VSTB pin that simultaneously toggle up to four rails between programmed run and standby output voltages. The device is available in a low profile 40-pin 6mm × 6mm exposed pad QFN package.

TYPICAL APPLICATION



Start-Up Sequence



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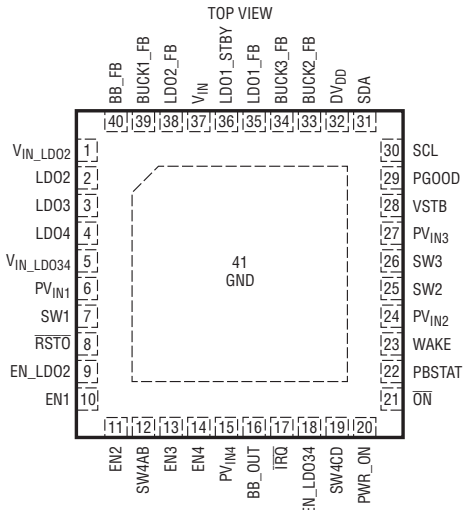
ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

V_{IN}, DV_{DD}, SW1, SW2, SW3, SW4AB, SW4CD .... –0.3V to 6V
SW1, SW2, SW3, SW4AB, SW4CD
(Transients < 1µs, Duty Cycle < 5%) ..... –2V to 7V
PV_{IN1}, PV_{IN2}, PV_{IN3}, PV_{IN4} ..... –0.3V to V_{IN} + 0.3V
V_{IN_LDO2}, V_{IN_LDO34} ..... –0.3V to V_{IN} + 0.3V
LDO1_STBY, LDO1_FB, BUCK1_FB, BUCK2_FB, BUCK3_FB, BB_FB, BB_OUT, LDO2, LDO2_FB, LDO3, LDO4, PGOOD, VSTB, EN1, EN2, EN3, EN4, EN_LDO2, EN_LDO34, EN_LDO3, $\overline{ON}$, PBSTAT, WAKE, $\overline{RSTO}$, PWR_ON, $\overline{IRQ}$, ... –0.3V to 6V
SDA, SCL ..... –0.3V to DV_{DD} + 0.3V
Operating Junction Temperature Range
(Note 2) ..... –40°C to 150°C
Storage Temperature Range ..... –65°C to 150°C

PIN CONFIGURATION

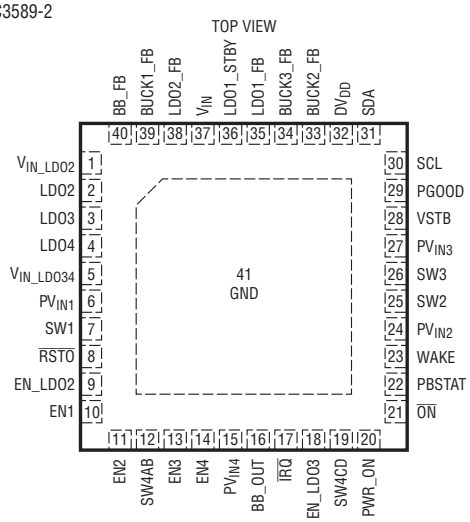
LTC3589



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

LTC3589-1/LTC3589-2



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 41) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3589EUJ#PBF	LTC3589EUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589IUJ#PBF	LTC3589IUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589HUJ#PBF	LTC3589HUJ#TRPBF	LTC3589UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C
LTC3589EUJ-1#PBF	LTC3589EUJ-1#TRPBF	LTC3589UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589IUJ-1#PBF	LTC3589IUJ-1#TRPBF	LTC3589UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589HUJ-1#PBF	LTC3589HUJ-1#TRPBF	LTC3589UJ-1	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C
LTC3589EUJ-2#PBF	LTC3589EUJ-2#TRPBF	LTC3589UJ-2	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589IUJ-2#PBF	LTC3589IUJ-2#TRPBF	LTC3589UJ-2	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C
LTC3589HUJ-2#PBF	LTC3589HUJ-2#TRPBF	LTC3589UJ-2	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	Operating Input Supply Voltage, V_{IN}		●	2.7		5.5	V
$I_{STANDBY}$	V_{IN} Standby Current	All Enables = 0V, PWR_ON = 0V, I_{LDO1} = 0mA	●		8	18	µA
f_{OSC}	Oscillator Frequency		●	1.8	2.25	2.6	MHz
Step-Down Switching Regulators 1, 2, and 3							
I_{VIN}	Pulse-Skipping Mode V_{IN} Quiescent Current per Buck Burst Mode® V_{IN} Quiescent Current per Buck	V_{FB} = 0.85V (Note 5)	● ●		120 23	200 40	µA µA
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.8V		–50		50	nA
D_X	Maximum Duty Cycle	V_{FB} = 0V		100			%
R_{SW}	SW Pull-Down Resistance	Regulators Disabled			2.5		kΩ
t_{SS}	Soft-Start Rate	(Note 6)			0.8		V/ms
$V_{FB(MAX)}$	Maximum Feedback Voltage	BxDTV1 = BxDTV2 = 11111, V_{IN} = 2.7V to 5.5V	●	0.735	0.75	0.765	V
$V_{FB(LSB)}$	Feedback LSB Step Size				12.5		mV
$V_{FB(MIN)}$	Minimum Feedback Voltage	BxDTV1 = BxDTV2 = 00000, V_{IN} = 2.7V to 5.5V	●	0.351	0.3625	0.374	V
1.6A Step-Down Switching Regulator 1							
I_{LIM1}	Peak PMOS Current Limit SW1		●	2.0	2.7		A
RP1	$R_{DS(ON)}$ of PMOS1	I_{SW1} = –100mA			180		mΩ
RN1	$R_{DS(ON)}$ of NMOS1	I_{SW1} = 100mA			110		mΩ
1.0A/1.2A Step-Down Switching Regulators 2 and 3							
$I_{LIM2, 3}$	Peak PMOS Current Limit SW2 and SW3 (LTC3589) Peak PMOS Current Limit SW2 and SW3 (LTC3589-1/ LTC3589-2)		● ●	1.5 1.8	1.9 2.3		A A
RP2, 3	$R_{DS(ON)}$ of PMOS2 and PMOS3	I_{SW1} = –100mA			250		mΩ
RN2, 3	$R_{DS(ON)}$ of NMOS2 and NMOS3	I_{SW1} = 100mA			130		mΩ
1.2A Buck-Boost Switching Regulator 4 (Buck-Boost)							
I_{VIN}	PWM Mode V_{IN} Quiescent Current Burst Mode V_{IN} Quiescent Current	V_{BB_FB} = 0.85V (Note 5)	● ●		115 19	170 35	µA µA
V_{BB_FB}	Feedback Voltage	V_{IN} = 2.7V to 5.5V	●	0.776	0.8	0.824	V
V_{OUTBB}	Output Voltage Range			1.8		5.0	V
I_{LIM4}	Peak PMOS Current Limit SW4AB		●	2.3	2.9		A
I_{PEAK4}	Forward Burst Current Limit (Switch A)	Burst Mode Operation			600		mA
I_{LIMR4}	Reverse Current Limit (Switch D)				1		A
I_{ZERO4}	Reverse Burst Current Limit (Switch D)	Burst Mode Operation			0		mA
RP4	$R_{DS(ON)}$ of Switch A and Switch D	I_{SW4AB} = I_{SW4CD} = 100mA			160		mΩ
RN4	$R_{DS(ON)}$ of Switch B and Switch C	I_{SW4AB} = I_{SW4CD} = –100mA			110		mΩ
R_{OUT4}	BB_OUT Pull-Down Resistance	Regulator Disabled			2.5		kΩ
t_{SS}	Soft-Start Rate	(Note 6)			2		V/ms
I_{FB}	Feedback Pin Input Current	V_{FB} = 0.85V		–50		50	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulators							
t_{LDO_SS}	Soft-Start Time LDO2, LDO3, LDO4				100		µs
R_{LDO_PD}	Output Pull-Down Resistance LDO2, LDO3, LDO4	LDO Disabled			2.5		kΩ
Always-On Regulator (LDO1_STBY)							
V_{LDO1_FB}	LDO1 Feedback Voltage		●	0.76	0.8	0.84	V
V_{LDO1}	LDO1 Line Regulation	I_{LDO1_STBY} = 1mA, LDO1_STBY = 1.2V, V_{IN} = 2.7V to 5.5V			0.15		%/V
	LDO1 Load Regulation	I_{LDO1} = 0.1mA to 25mA, LDO1_STBY = 1.2V			0.1		%
I_{LDO1}	Available Output Current		●	25			mA
I_{LDO1_SC}	Short-Circuit Output Current Limit				65	100	mA
V_{DROP1}	Dropout Voltage (Note 4)	I_{LDO1} = 25mA, LDO1_STBY = 3.3V			200		mV
I_{LDO1_FB}	LDO1_FB Input Current	V_{LDO1_FB} = 0.85V		–50		50	nA
LDO Regulator 2 (LDO2)							
V_{IN_LDO2}	V_{IN_LDO2} Input Voltage Range		●	1.7		V_{IN}	V
I_{VIN_LDO2}	V_{IN_LDO2} Quiescent Current V_{IN_LDO2} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		12 0	20 1	µA µA
I_{VIN}	V_{IN} Quiescent Current	EN_LDO2 = High	●		50	85	µA
$V_{FB2(MAX)}$	LDO2 Maximum Feedback Voltage	L2DTV1 = L2DTV2 = 11111	●	0.735	0.75	0.765	V
$V_{FB2(LSB)}$	LDO2 Feedback LSB Step Size				12.5		mV
$V_{FB2(MIN)}$	LDO2 Minimum Feedback Voltage	L2DTV1 = L2DTV2 = 00000 V_{IN_LDO2} = V_{IN} = 2.7V to 5.5V, I_{LDO2} = 1mA	●	0.351	0.3625	0.374	V
	LDO2 Line Regulation	I_{LDO2} =1mA, V_{IN_LDO2} = 2.7V to 5.5V			0.01		%/V
	LDO2 Load Regulation	I_{LDO2} = 1mA to 250mA			0.01		%
I_{LDO2}	LDO2 Available Output Current		●	250			mA
I_{LDO2_SC}	LDO2 Short-Circuit Current Limit			300	450	600	mA
V_{DROP2}	Dropout Voltage (Note 4)	I_{LDO2} = 200mA, V_{LDO2} = 2.5V I_{LDO2} = 200mA, V_{LDO2} = 1.2V			140 350	180 500	mV mV
I_{LDO2_FB}	LDO2_FB Input Current	V_{LDO2_FB} = 0.8V		–50		50	nA
LDO Regulator 3 (LDO3)							
V_{IN_LDO34}	V_{IN_LDO34} Input Range (LTC3589) V_{IN_LDO34} Input Range (LTC3589-1/LTC3589-2)		● ●	2.35 3.0		V_{IN} V_{IN}	V V
I_{VIN_LDO34}	V_{IN_LDO34} Quiescent Current V_{IN_LDO34} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		15 0	29 1	µA µA
I_{VIN}	V_{IN} Quiescent Current	EN_LDO3 = High	●		50	85	µA
V_{LDO3}	LDO3 Output Voltage (LTC3589) LDO3 Output Voltage (LTC3589-1/LTC3589-2)	V_{IN_LDO34} = V_{IN} = 2.7V to 5V, I_{LDO3} = 1mA	● ●	1.746 2.716	1.8 2.8	1.854 2.884	V V
	LDO3 Line Regulation	I_{LDO3} =1mA, V_{IN_LDO34} = 2.7V to 5.5V			0.01		%/V
	LDO3 Load Regulation	I_{LDO3} = 1mA to 250mA			0.05		%
I_{LDO3}	LDO3 Available Output Current		●	250			mA
I_{LDO3_SC}	LDO3 Short-Circuit Current Limit			300	450	600	mA
V_{DROP3}	LDO3 Dropout Voltage (LTC3589) (Note 4) LDO3 Dropout Voltage (LTC3589-1/LTC3589-2) (Note 4)	I_{LDO3} = 200mA, V_{LDO3} = 1.8V I_{LDO3} = 200mA, V_{LDO3} = 2.8V			190 140	250 180	mV mV

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
LDO Regulator 4 (LDO4)							
V_{IN_LDO34}	V_{IN_LDO34} Input Range (LTC3589) V_{IN_LDO34} Input Range (LTC3589-1/LTC3589-2)		● ●	2.35 1.7		V_{IN} V_{IN}	V V
I_{VIN_LDO34}	V_{IN_LDO34} Quiescent Current V_{IN_LDO34} Shutdown Current	Regulator Enabled Regulator Disabled	● ●		14 0	24 1	µA µA
I_{VIN}	V_{IN} Quiescent Current	EN_LDO4 = High	●		50	85	µA
V_{LDO4} (LTC3589)	LDO 4 Output Voltage	I_{LDO4} = 1mA, L2DTV2[6:5] = 00 L2DTV2[6:5] = 01 L2DTV2[6:5] = 10 L2DTV2[6:5] = 11	● ● ● ●	2.716 2.425 1.746 3.201	2.8 2.5 1.8 3.3	2.884 2.575 1.854 3.399	V V V V
V_{LDO4} (LTC3589-1) (LTC3589-2)	LDO 4 Output Voltage	I_{LDO4} = 1mA, L2DTV2[6:5] = 00 L2DTV2[6:5] = 01 L2DTV2[6:5] = 10 L2DTV2[6:5] = 11	● ● ● ●	1.164 1.746 2.425 3.104	1.2 1.8 2.5 3.2	1.236 1.854 2.575 3.296	V V V V
	LDO4 Line Regulation	I_{LDO4} =1mA, V_{IN_LDO34} = 2.7V to 5.5V, V_{OUT} = 1.8V			0.01		%/V
	LDO4 Load Regulation	I_{LDO4} = 1mA to 250mA			0.05		%
I_{LDO4}	LDO4 Available Output Current		●	250			mA
I_{LDO4_SC}	LDO4 Short-Circuit Current Limit			300	450	600	mA
V_{DROP4}	LDO4 Dropout Voltage (Note 4)	I_{LDO4} = 200mA, V_{LDO4} = 3.3V I_{LDO4} = 200mA, V_{LDO4} = 1.8V I_{LDO4} = 200mA, V_{LDO4} = 3.2V (LTC3589-1/ LTC3589-2)			120 190 120	160 250 160	mV mV mV
Enable Inputs							
V_{ENx_THR}	Threshold Rising	All Enables Low	●		0.8	1.2	V
V_{ENx_THR2} V_{ENx_THF2}	Threshold Rising Threshold Falling	Any Enable High Any Enable High	● ●	 0.420	0.5 0.45	0.530	V V
R_{ENX}	Input Pull-Down Resistance				4.5		MΩ
VSTB, PWR_ON Inputs							
V_{VSTB_THR} V_{VSTB_THF}	VSTB Pin Threshold Rising VSTB Pin Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
R_{VSTB}	Pull-Down Resistance				4.5		MΩ
V_{PWR_ONTHR} V_{PWR_ONTHF}	PWR_ON Pin Threshold Rising PWR_ON Pin Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
R_{PWR_ON}	Pull-Down Resistance				4.5		MΩ
I^2C Port							
DV_{DD}	DV_{DD} Input Supply Voltage		●	1.6		5.5	V
I_{DVDD}	DV_{DD} Quiescent Current	SCL/SDA = 0kHz			0.5		µA
V_{DVDD_UVLO}	DV_{DD} UVLO Level				0.8		V
ADDRESS	Device Address – Write Device Address – Read				01101000 01101001		
V_{IH} SDA, SCL V_{IL} SDA, SCL	SDA and SCL Input Threshold Rising SDA and SCL Input Threshold Falling			70		 30	$\%DV_{DD}$ $\%DV_{DD}$
I_{IHSCx} I_{ILSCx}	SDA and SCL Input Current	SDA = SCL = 0V to 5.5V		–250		250	nA
V_{OL} SDA	SDA Output Low Voltage	I_{SDA} = 3mA	●			0.4	V
f_{SCL}	SCL Clock Operating Frequency					400	kHz

ELECTRICAL CHARACTERISTICS

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SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
t_{SU_STA}	Repeated Start Condition Set-Up Time			0.6			µs
t_{SU_STO}	Stop Condition Set-Up Time			0.6			µs
$t_{HD\_DAT(O)}$	Data Hold Time Output			0		900	ns
$t_{HD\_DAT(I)}$	Data Hold Time Input			0			ns
t_{SU_DAT}	Data Set-Up Time			100			ns
t_{LOW}	SCL Clock Low Period			1.3			µs
t_{HIGH}	SCL Clock High Period			0.6			µs
t_f	Data Fall Time	C_B = Capacitance of One BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_r	Data Rise Time	C_B = Capacitance of One BUS Line (pF)		$20 + 0.1C_B$		300	ns
t_{SP}	Input Spike Suppression Pulse Width					50	ns
Pushbutton Interface							
$V_{\overline{ON}\_THR}$ $V_{\overline{ON}\_THF}$	$\overline{ON}$ Threshold Rising $\overline{ON}$ Threshold Falling		● ●	 0.4	0.8 0.7	1.2	V V
$I_{\overline{ON}}$	$\overline{ON}$ Input Current	$\overline{ON}$ = V_{IN} $\overline{ON}$ = 0V		–100	 40	100	nA µA
$t_{\overline{ON}\_PBSTAT1}$	$\overline{ON}$ Low Time to PBSTAT Low				50		ms
$t_{\overline{ON}\_PBSTAT2}$	$\overline{ON}$ High Time to PBSTAT High				0.2		µs
$t_{\overline{ON}\_WAKE}$	$\overline{ON}$ Low Time to WAKE High				400		ms
$t_{\overline{ON}\_HR}$	$\overline{ON}$ Low Time to Hard Reset				5		s
t_{PBSTAT_PW}	PBSTAT Minimum Pulse Width				50		ms
t_{PBSTAT_BK}	PBSTAT Blanking from WAKE Low				1		s
t_{WAKE_OFF}	Minimum WAKE Low Time				1		s
t_{WAKE_ON}	WAKE High Time with PWR_ON = 0V				5		s
t_{PWR_ON}	PWR_ON to WAKE High (LTC3589) PWR_ON to WAKE High (LTC3589-1/LTC3589-2)				50 2		ms ms
t_{PWR_OFF}	PWR_ON to WAKE Low (LTC3589) PWR_ON to WAKE Low (LTC3589-1/LTC3589-2)				50 2		ms ms
Status Output Pins (PBSTAT, WAKE, PGOOD, $\overline{RSTO}$, $\overline{IRQ}$)							
V_{PBSTAT}	PBSTAT Output Low Voltage	I_{PBSTAT} = 3mA			0.1	0.4	V
I_{PBSTAT}	PBSTAT Output High Leakage Current	V_{PBSTAT} = 3.8V		–0.1		0.1	µA
V_{WAKE}	WAKE Output Low Voltage	I_{WAKE} = 3mA			0.1	0.4	V
I_{WAKE}	WAKE Output High Leakage Current	V_{WAKE} = 3.8V		–0.1		0.1	µA
V_{PGOOD}	PGOOD Output Low Voltage	I_{PGOOD} = 3mA			0.1	0.4	V
I_{PGOOD}	PGOOD Output High Leakage Current	V_{PGOOD} = 3.8V		–0.1		0.1	µA
V_{PGOOD}	PGOOD Threshold Rising PGOOD Threshold Falling				–6 –8		% %
V_{NRSTO}	LDO1 Power Good Threshold Rising LDO1 Power Good Threshold Falling				–6 –8		% %
V_{UVLO}	Undervoltage Lockout Rising Undervoltage Lockout Falling				2.65 2.55	2.7	V V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = PV_{IN1} = PV_{IN2} = PV_{IN3} = PV_{IN4} = V_{IN_LDO2} = V_{IN_LDO34} = DV_{DD} = 3.8V. All regulators disabled unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{UVWARN}	Undervoltage Warning Rising Undervoltage Warning Falling				3 2.9		
$V_{\overline{RSTO}}$	$\overline{RSTO}$ Output Low Voltage	$I_{\overline{RSTO}}$ = 3mA			0.1	0.4	V
$I_{\overline{RSTO}}$	$\overline{RSTO}$ Output High Leakage Current	$V_{\overline{RSTO}}$ = 3.8V		–0.1		0.1	µA
$V_{\overline{IRQ}}$	$\overline{IRQ}$ Output Low Voltage	$I_{\overline{IRQ}}$ = 3mA			0.1	0.4	V
$I_{\overline{IRQ}}$	$\overline{IRQ}$ Output High Leakage Current	$V_{\overline{IRQ}}$ = 3.8V		–0.1		0.1	µA

Note 1: Stresses beyond those listed Under Absolute Maximum ratings may cause permanent damage to the device. Exposure to any Absolute Maximum rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3589 are tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3589E are guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3589I are guaranteed over the –40°C to 125°C operating junction temperature range and the LTC3589H are guaranteed over the full –40°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. The junction temperature (T_J in °C) is calculated from the ambient temperature (T_A in °C) and power dissipation (PD, in Watts) according to the formula:

$T_J = T_A + (PD \bullet \theta_{JA})$, where the package junction to ambient thermal impedance θ_{JA} = 33°C/W.

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: The LTC3589 include overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 150°C when overtemperature protection is active. Continuous operation above the specified maximum operating temperature may impair device reliability.

Note 4: Dropout voltage is defined as ($V_{IN} – V_{LDO}$) for LDO1 or ($V_{IN\_LDO} – V_{LDO}$) for other LDOs when V_{LDO} is 3% lower than V_{LDO} measured with V_{IN} = V_{IN_LDO} = 4.3V.

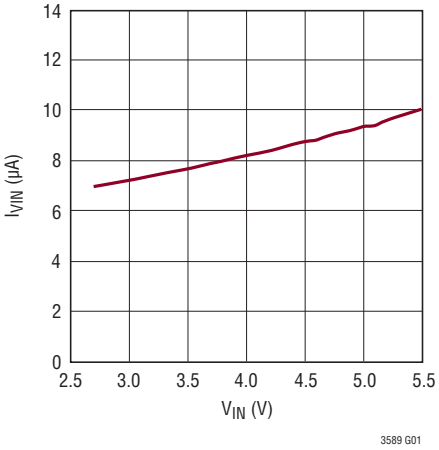
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Soft-start measured in test mode with regulator error amplifier in unity gain mode.

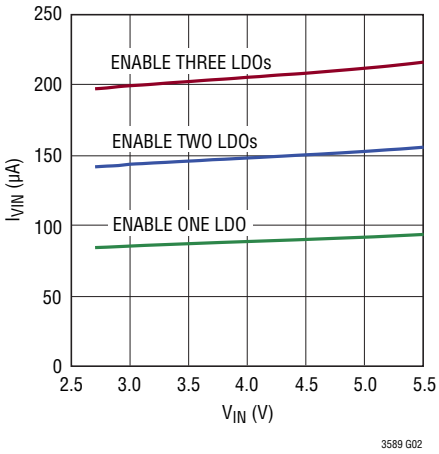
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

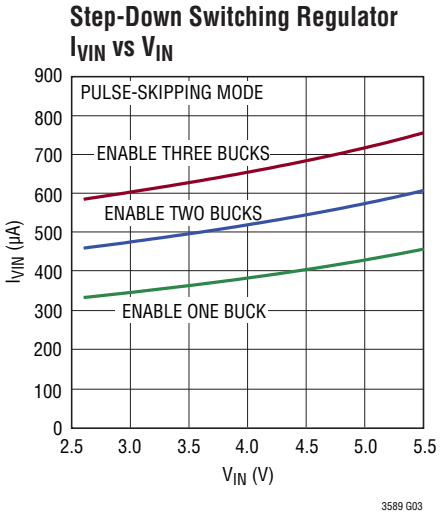
Standby I_{VIN} vs V_{IN}



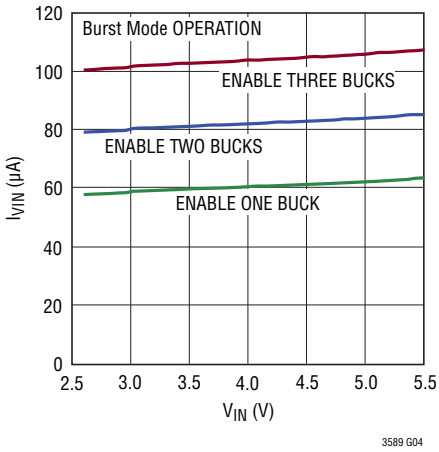
LDO2 to LDO4 I_{VIN} vs V_{IN}



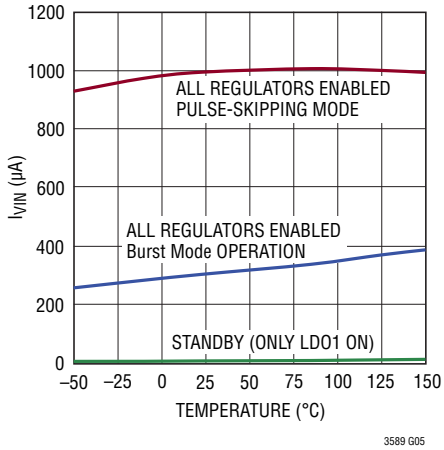
Step-Down Switching Regulator I_{VIN} vs V_{IN}



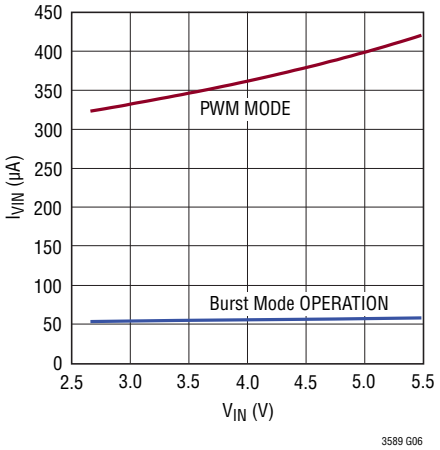
Step-Down Switching Regulator I_{VIN} vs V_{IN}



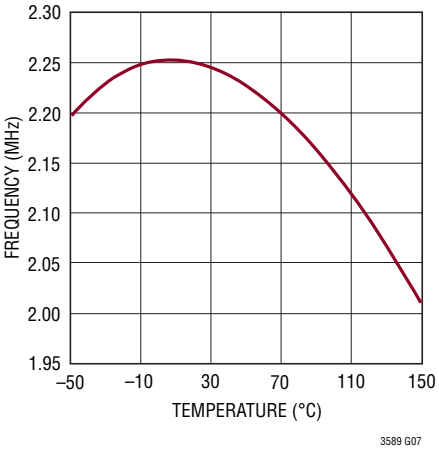
Input Supply Current vs Temperature



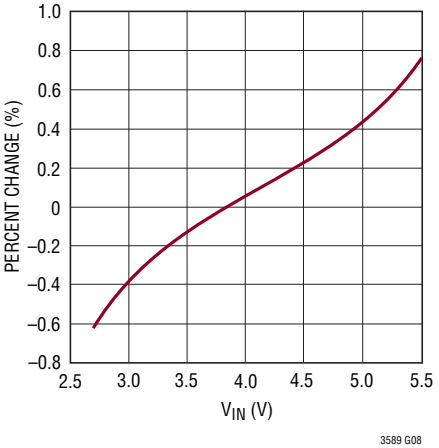
Buck-Boost I_{VIN} vs V_{IN}



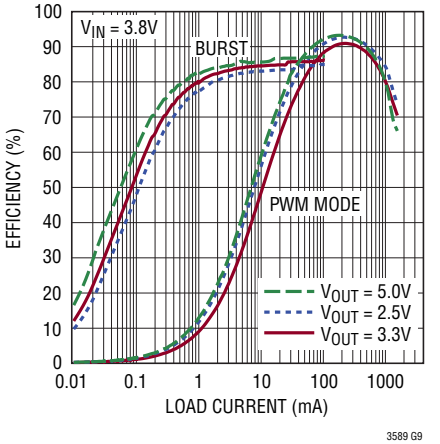
Oscillator Frequency vs Temperature



Switching Frequency Change vs V_{IN}



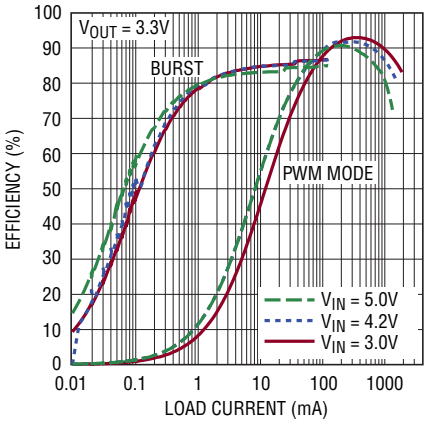
Buck-Boost Efficiency vs I_{OUT}



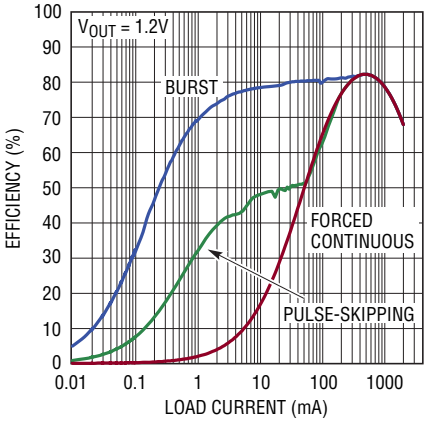
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

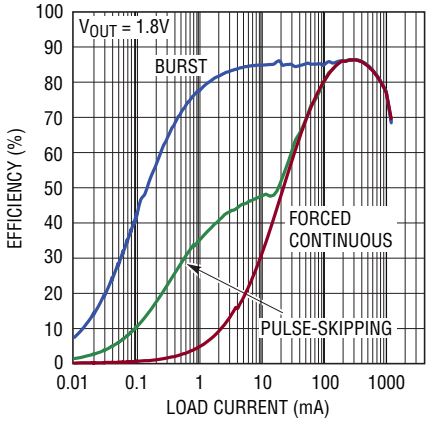
Buck-Boost Efficiency vs I_{OUT}



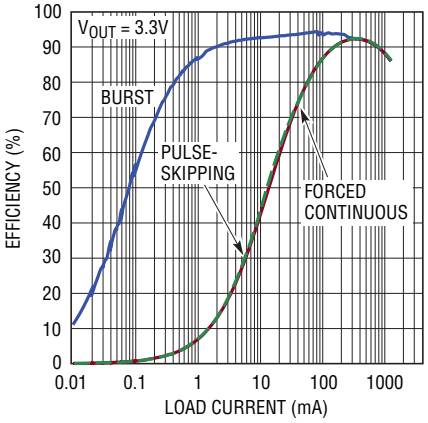
Step-Down Switching Regulator 1 Efficiency vs I_{OUT}



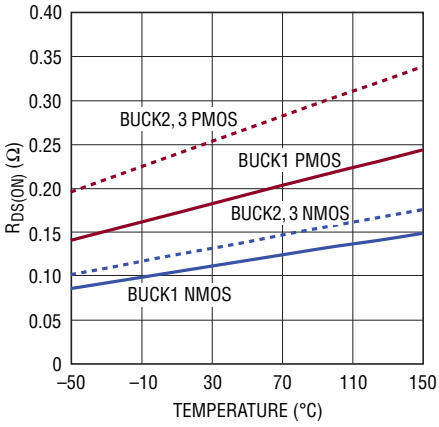
Step-Down Switching Regulator 2 Efficiency vs I_{OUT}



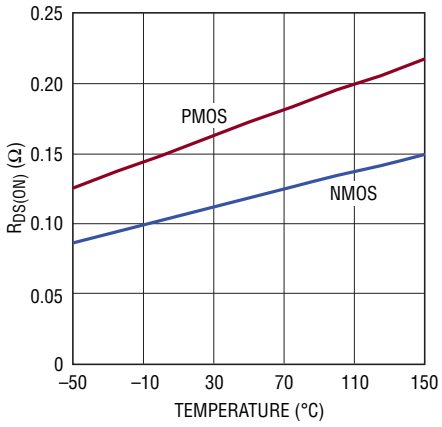
Step-Down Switching Regulator 3 Efficiency vs I_{OUT}



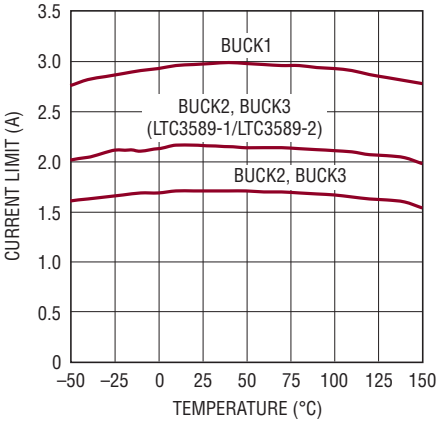
Step-Down Switching Regulator $R_{DS(ON)}$ vs Temperature



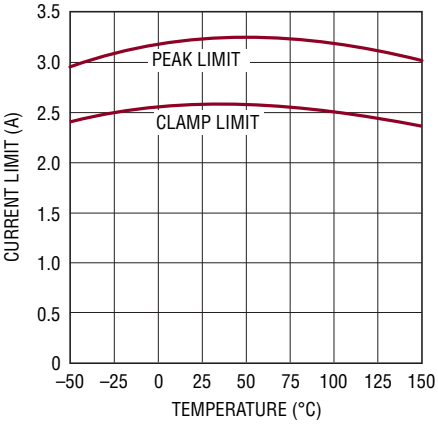
Buck-Boost $R_{DS(ON)}$ vs Temperature



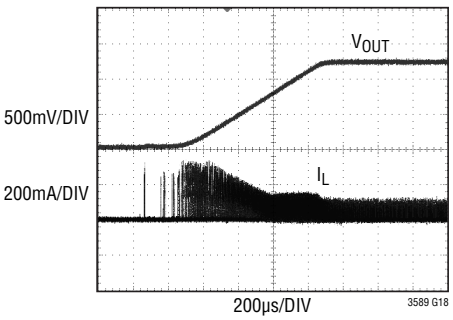
Step-Down Switching Regulator Current Limit vs Temperature



Buck-Boost Current Limit vs Temperature



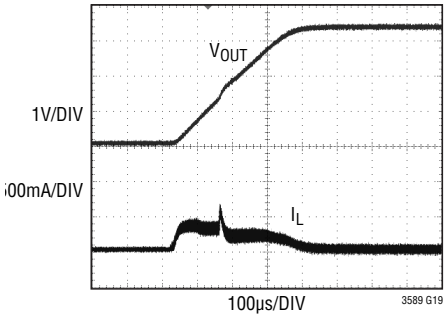
Step-Down Switching Regulator Soft-Start



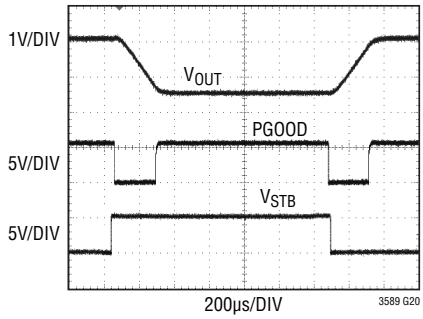
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

Buck-Boost Switching Regulator Soft-Start

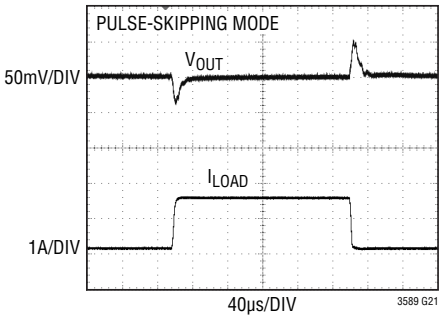


Dynamic Voltage Slew



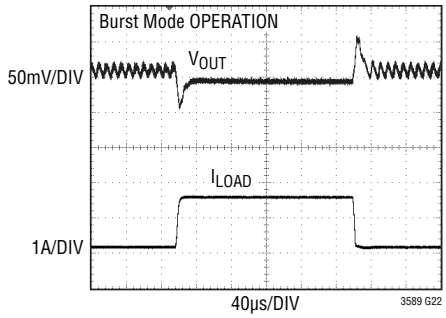
V_{RRCR} = 1.75mV/µs

Step-Down Switching Regulator 1 Load Step



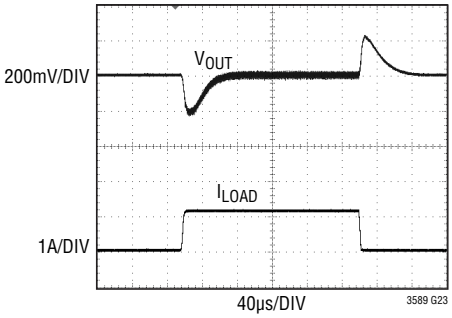
LOAD CAPACITANCE = 44µF

Step-Down Switching Regulator 1 Load Step



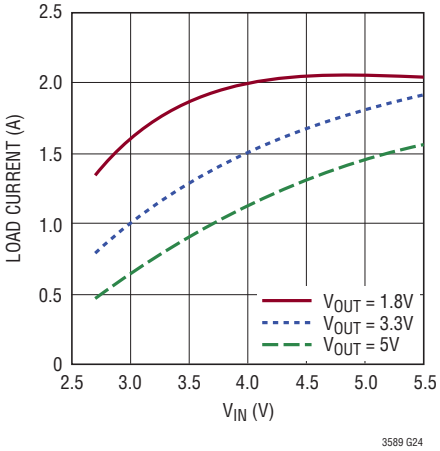
LOAD CAPACITANCE = 44µF

Buck-Boost Switching Regulator 1 Load Step

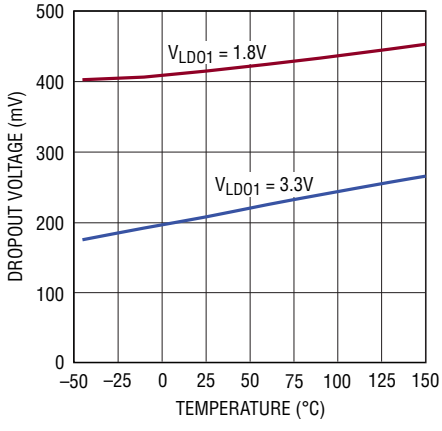


LOAD CAPACITANCE = 22µF

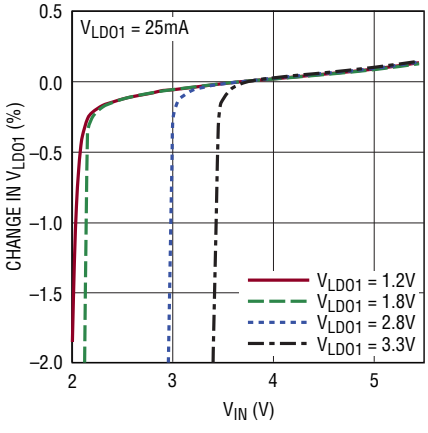
Maximum Buck-Boost Load Current vs V_{IN}



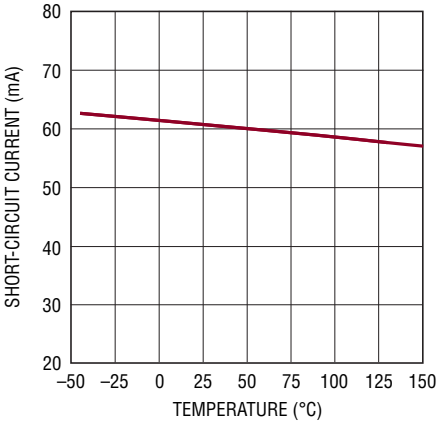
LDO1 Dropout Voltage vs Temperature



LDO1 Output Change vs V_{IN}



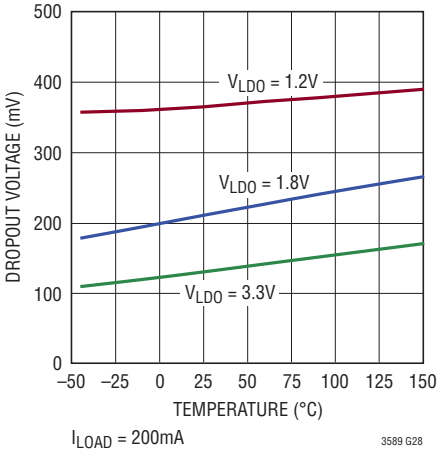
LDO1 Short-Circuit Current vs Temperature



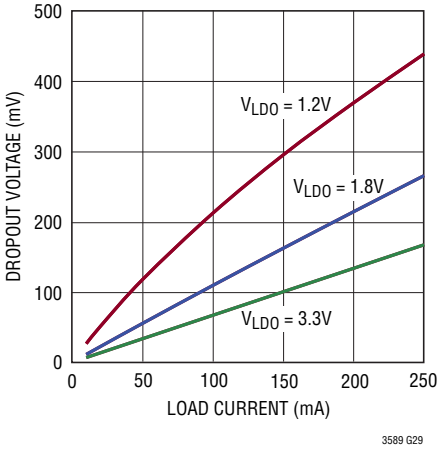
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 3.8V, T_A = 25°C, unless otherwise noted.

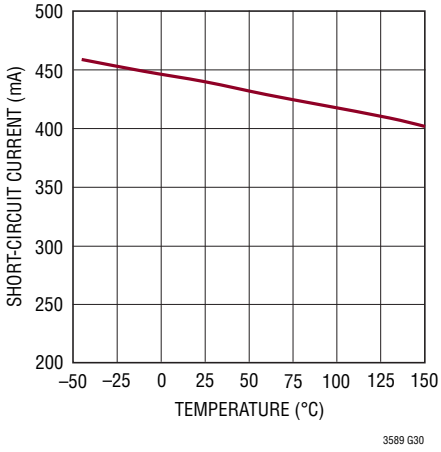
LDO2, LDO3, LDO4 Dropout Voltage vs Temperature



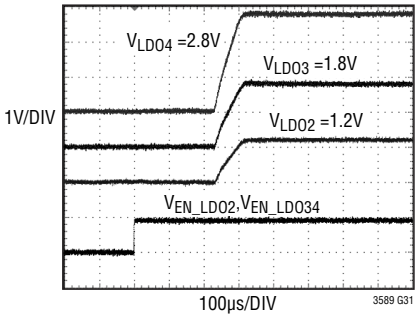
LDO2, LDO3, LDO4 Dropout Voltage vs Load Current



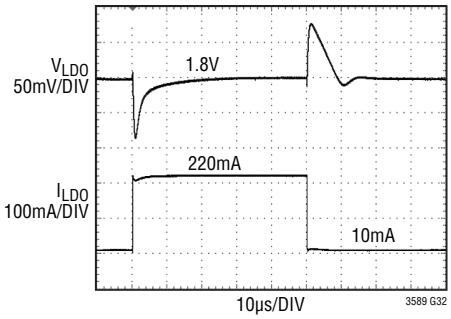
LDO2, LDO3, LDO4 Short-Circuit Current vs Temperature



LDO2, LDO3, LDO4 Enable Response

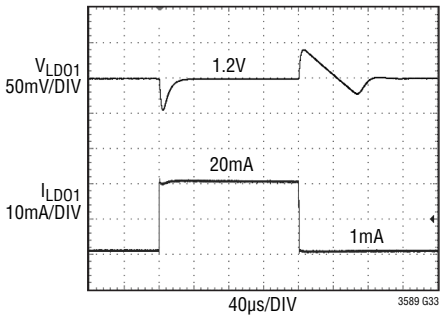


LDO2, LDO3, LDO4 Load Step Response



LOAD CAPACITANCE = 1µF

LDO1 Load Step Response



LOAD CAPACITANCE = 1µF

PIN FUNCTIONS

V_{IN_LDO2} (Pin 1): Power Input for LDO2. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO2 (Pin 2): Output Voltage of LDO2. Nominal output voltage is set with a resistor feedback divider that servos to an I^2C register controlled DAC reference. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO3 (Pin 3): Output Voltage of LDO3. Nominal output voltage is fixed at 1.8V or 2.8V (LTC3589-1/LTC3589-2). This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

LDO4 (Pin 4): Output Voltage of LDO4. Output voltage is selected via the I^2C port. This pin must be bypassed to ground with a 1µF or greater ceramic capacitor.

V_{IN_LDO34} (Pin 5): Power Input for LDO3 and LDO4. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

PV_{IN1} (Pin 6): Power Input for Step-Down Switching Regulator 1. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

SW1 (Pin 7): Switch Pin for Step-Down Switching Regulator 1. Connect one side of step-down switching regulator 1 inductor to this pin.

$\overline{RSTO}$ (Pin 8): Reset Output. Open-drain output pulls low when the always-on regulator LDO1 is below regulation and during a hard reset initiated by a pushbutton input.

EN_LDO2 (Pin 9): Enable LDO2 Logic Input. Active high input to enable LDO2. A weak pull-down forces EN_LDO2 low when left floating.

EN1 (Pin 10): Enable Step-Down Switching Regulator 1. Active high input to enable step-down switching regulator 1. A weak pull-down forces EN1 low when left floating.

EN2 (Pin 11): Enable Step-Down Switching Regulator 2. Active high input to enable step-down switching regulator 2. A weak pull-down forces EN2 low when left floating.

SW4AB (Pin 12): Switch Pin for Buck-Boost Switching Regulator 4. Connected to the buck-boost internal power switches A and B. Connect an inductor between this pin and SW4CD (Pin 19).

EN3 (Pin 13): Enable Step-Down Switching Regulator 3. Active high input to enable step-down switching regulator 3. A weak pull-down forces EN3 low when left floating.

EN4 (Pin 14): Enable Buck-Boost Switching Regulator 4. Active high input to enable buck-boost switching regulator 4. A weak pull-down forces EN4 low when left floating.

PV_{IN4} (Pin 15): Power Input for Switching Regulator 4. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

BB_OUT (Pin 16): Output Voltage of Buck-Boost Switching Regulator 4. This pin must be bypassed to ground with a 22µF or greater ceramic capacitor.

$\overline{IRQ}$ (Pin 17): Interrupt Request Output. Open-drain driver is pulled low for power good, undervoltage, and overtemperature warning and fault conditions. Clear $\overline{IRQ}$ by writing to the I^2C CLIRQ command register.

EN_LDO34 (Pin 18): LTC3589 Enable LDO3 and LDO4 Logic Input. Active high to enable LDO3 and LDO4. Disable LDO4 via I^2C software commands using I^2C command registers OVEN or L2DTV2. A weak pull-down forces EN_LDO34 low when left floating.

EN_LDO3 (Pin 18): LTC3589-1/LTC3589-2 Enable LDO3 Logic Input. Active high to enable LDO3. A weak pull-down forces EN_LDO3 low when left floating.

SW4CD (Pin 19): Switch Pin for Buck-Boost Switching Regulator 4. Connected to the buck-boost internal power switches C and D. Connect an inductor between this node and SW4AB (Pin 12).

PWR_ON (Pin 20): External Power-On. Handshaking pin to acknowledge successful power-on sequence. PWR_ON must be driven high within five seconds of WAKE going high to keep power on. It can be used to activate the WAKE output by driving high. Drive low to shut down WAKE.

PIN FUNCTIONS

$\overline{ON}$ (Pin 21): Pushbutton Input. A weak internal pull-up forces $\overline{ON}$ high when left floating. A normally open pushbutton is connected from $\overline{ON}$ to ground to force a low state on this pin.

PBSTAT (Pin 22): Pushbutton Status. Open-drain output to be used for processor interrupts. PBSTAT mirrors the status of $\overline{ON}$ pushbutton pin. PBSTAT is delayed 50ms from $\overline{ON}$ pin for debounce.

WAKE (Pin 23): System Wake Up. Open-drain driver output releases high when signaled by pushbutton activation or PWR_ON input. It may be used to initiate a pin-strapped power-up sequence by connecting to a regulator enable pin.

PVIN2 (Pin 24): Power Input for Step-Down Switching Regulator 2. Tie this pin to V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

SW2 (Pin 25): Switch Pin for Step-Down Switching Regulator 2. Connect one side of step-down switching regulator 2 inductor to this pin.

SW3 (Pin 26): Switch Pin for Step-Down Switching Regulator 3. Connect one side of step-down switching regulator 3 inductor to this pin.

PVIN3 (Pin 27): Power Input for Step-Down Switching Regulator 3. Tie this pin to the V_{IN} supply. This pin should be bypassed to ground with a 4.7µF or greater ceramic capacitor.

VSTB (Pin 28): Voltage Standby. When VSTB is low, DAC reference registers are selected by bit values in command register VCCR. When VSTB is high, the DAC registers are forced xxDVT2 registers. Tie VSTB to ground if unused.

PGOOD (Pin 29): Power Good Output. Open-drain output pulls down when any regulator falls below power good threshold and during regulator dynamic voltage slew unless disabled in I^2C register. Pulls down when all regulators are disabled.

SCL (Pin 30): Clock Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{DD}.

SDA (Pin 31): Data Input Pin for the I^2C Serial Port. The I^2C logic levels are scaled with respect to DV_{DD}.

DV_{DD} (Pin 32): Supply Voltage for I^2C Serial Port. This pin sets the logic reference level of SCL and SDA I^2C pins. DV_{DD} resets I^2C registers to power on state when driven to <1V. SCL and SDA logic levels are scaled to DV_{DD}. Connect a 0.1µF decoupling capacitor from this pin to ground.

BUCK2_FB (Pin 33): Feedback Input for Step-Down Switching Regulator 2. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 2 to this pin to ground.

BUCK3_FB (Pin 34): Feedback Input for Step-Down Switching Regulator 3. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 3 to this pin to ground.

LDO1_FB (Pin 35): Feedback Input for LDO1. Set output voltage using a resistor divider connected from LDO1_STDBY to this pin to ground.

LDO1_STDBY (Pin 36): Always-On LDO1 Output. This pin provides an always-on supply voltage useful for light loads such as a watchdog microprocessor or a real-time clock. Connect a 1µF capacitor from LDO1_STBY to ground.

V_{IN} (Pin 37): Supply Voltage Input. This pin should be bypassed to ground with a 1µF or greater ceramic capacitor.

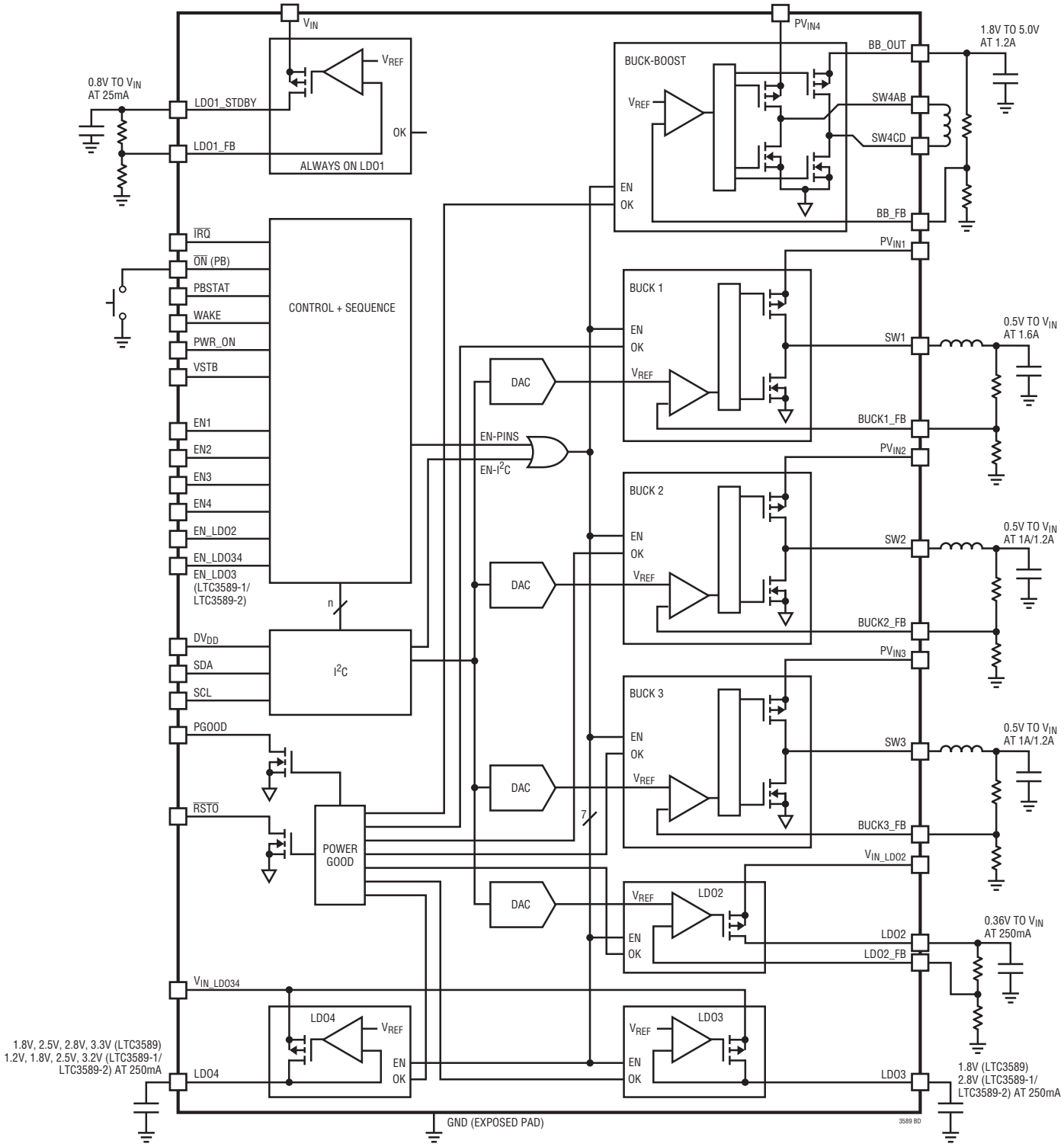
LDO2_FB (Pin 38): Feedback Input for LDO2. Set full-scale output voltage using a resistor divider connected from LDO2_OUT to this pin to ground.

BUCK1_FB (Pin 39): Feedback Input for Step-Down Switching Regulator 1. Set full-scale output voltage using resistor divider connected from the output of step-down switching regulator 1 to this pin to ground.

BB_FB (Pin 40): Feedback Input for Buck-Boost Switching Regulator 4. Set the output voltage using resistor divider connected from BB_OUT to this pin to ground.

GND (Exposed Pad Pin 41): Ground. The Exposed Pad must be connected to a continuous ground plane on the second layer of the printed circuit board by several interconnect vias directly under the LTC3589 for maximum heat transfer.

BLOCK DIAGRAM



OPERATION

INTRODUCTION

The LTC3589 is a complete power management solution for portable microprocessors and peripheral devices. It generates a total of eight voltage rails for supplying power to the processor core, SDRAM, system memory, PC cards, always-on real-time clock and HDD functions. Supplying the voltage rails are an always-on low quiescent current 25mA LDO, one 1.6A and two 1A (1.2A for LTC3589-1/LTC3589-2) step-down regulators, a 1.2A buck-boost regulator, and three 250mA low dropout regulators. Supporting the multiple regulators is a highly configurable power-on sequencing capability, dynamic voltage slewing DAC output voltage control, a pushbutton interface controller, regulator control via an I^2C interface, and extensive status and interrupt outputs.

The LTC3589 operates over an input supply range of 2.7V to 5.5V. The input supplies for the 250mA LDO regulators may operate as low as 1.7V to limit power loss at low output voltages.

The always-on LDO1 provides a resistor programmable output voltage as low as 0.8V and is capable of supplying 25mA. With only the always-on LDO active the LTC3589 draws just 8µA (typical). Always-on LDO1 will continue to operate with V_{IN} levels as low as 2.0V (typical) to maintain memory and RTC function as long as possible.

Each of the 250mA LDO regulators has unique output voltage configurations. LDO3 has a fixed 1.8V (2.8V for LTC3589-1/LTC3589-2) output. LDO4 has four output levels selectable via the I^2C interface. Its possible outputs are 1.8V, 2.5V, 2.8V, and 3.3V (1.2V, 1.8V, 2.5V, 3.2V for LTC3589-1/LTC3589-2). LDO2 has a dynamically slewing DAC set point reference and an external feedback pin to set the output voltage range with a resistive divider. Each LDO draws 50µA (typical) quiescent current.

The LTC3589 includes three internally compensated constant frequency current mode step-down switching regulators two capable of supplying 1A of output current and one capable of supplying 1.6A. The LTC3589-1/LTC3589-2 step-down regulators can supply 1.2A, 1.2A, and 1.6A. Step-down regulator switching frequencies of 2.25MHz or 1.125MHz are independently selected for each step-down regulator using the I^2C command registers. The power-on default frequency is 2.25MHz. Each of the step-down regulators have dynamically slewing DAC input references and external feedback pins to set output voltage range. The step-down regulators three operating modes, pulse-skipping, burst, or forced continuous, are set using the I^2C interface. In pulse-skipping mode the regulator will support 100% duty cycle. For best efficiency at low output loads select Burst Mode operation. Forced continuous mode minimizes output voltage ripple at light loads.

The 4-switch buck-boost DC/DC voltage mode converter generates a user-programmable output voltage rail from 1.8V to 5V. Utilizing a proprietary switching algorithm, the buck-boost converter maintains high efficiency and low noise operation with input voltages that are above, below or equal to the required output rail. The buck-boost error amplifier uses a fixed 0.8V reference and the output voltage is set by an external resistor divider. Burst Mode operation is enabled through the I^2C control registers. No external compensation components are required for the buck-boost converter.

The reference inputs for the three step-down regulators and LDO2 are 5-bit D to A converters with up-down ramping at selectable slew rates. The slew endpoint voltages and select bits are stored in I^2C registers for each DAC. A select bit in the I^2C command registers chooses which register to use for each target voltage. Variable reference slew rates from 0.88mV/µs to 7mV/µs are selectable in the I^2C register. Each of the four DACs has independent voltage, voltage select, and slew rate control registers.

The LTC3589 is equipped with a pushbutton control circuit that will activate the WAKE output, indicate pushbutton status via the PBSTAT pin, and initiate a hard reset shutdown of the regulators. Grounding the $\overline{ON}$ pin with the pushbutton for 400ms will force the WAKE pin to release HIGH. The WAKE pin output can be tied to the enable pin of the first regulator in a power-on sequence. Once in the power-on state, subsequent pushes of the button longer than 50ms are mirrored by the PBSTAT output. Holding $\overline{ON}$ LOW for five seconds disables all the regulators, pulls down the WAKE pin, and pulls down $\overline{RSTO}$ for one second to indicate to the processor that a hard reset occurred. All regulator enables and pushbutton inputs are inhibited for one second following the hard reset.

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The LTC3589 has flexible options for enabling and sequencing the regulator enables. The regulators are enabled using input pins or the I²C serial port. To define a power-on sequence tie the enable of the first regulator to be powered up to the WAKE pin. Connect the first regulators output to the enable pin of the second regulator, and so on. One or more regulators may be started in any sequence. Each enable pin has a 200µs (typical) delay between the pin and the internal enable of the regulator. When the system controllers are satisfied that power rails are up, the controller must drive PWR_ON HIGH to keep WAKE active. To ensure correct start-up sequencing, the regulators outputs are monitored by voltage comparators which require each output to discharge below 300mV before re-enabling. A software control command register function is available which sets the regulators to effectively ignore their enable pins but respond to I²C register enables. This function enables software-only control of any combination of pin-strapped regulators and is useful for implementing system power saving modes. Keep-alive mode exempts selected regulators from turning off during normal shutdown. In keep-alive mode, the LTC3589 powers down normally and is ready for the next start-up sequence, but selected regulators are kept on to power memory or other functions during system standby modes.

The LTC3589 will shut down all regulators and pull down the WAKE pin under high temperature, V_{IN} undervoltage, and extended low regulator output voltage conditions. Status of a hard shutdown is reported by the $\overline{IRQ}$ status pin and the IRQSTAT status register.

The I²C serial port on the LTC3589 contains 13 command registers for controlling each of the regulators, one read-only register for monitoring each regulators power good status, one read-only register for reading the cause of an $\overline{IRQ}$ event, and one clear IRQ command register. The LTC3589 I²C supports random addressing of any register.

LTC3589, LTC3589-1, AND LTC3589-2 FUNCTIONAL COMPARISON

Table 1. summarizes the functional differences between the LTC3589, LTC3589-1, and LTC3589-2.

Table 1. LTC3589, LTC3589-1, and LTC3589-2 Functional Differences

	LTC3589	LTC3589-1	LTC3589-2
Power-On Inhibit Enable Delay	1 second	<2ms	<2ms
Buck2 Current Output	1A	1.2A	1.2A
Buck3 Current Output	1A	1.2A	1.2A
PGOOD Fault Timeout	Enabled by Default. I²C Disable.	Disabled by Default. I²C Enable.	Disabled by Default. I²C Enable.
PWR_ON to WAKE Delay	50ms	2ms	2ms
LDO3 V_{OUT}	1.8V	2.8V	2.8V
LDO4 V_{OUT} * Indicates Default V_{OUT}	1.8V, 2.5V, 2.8V*, 3.3V	1.2V*, 1.8V, 2.5V, 3.2V	1.2V*, 1.8V, 2.5V, 3.2V
Default LDO4 Enable	LDO34_EN Pin	I²C	I²C
Wait to Enable Until Output < 300mV	Yes by Default. I²C Select.	Yes by Default. I²C Select.	No by Default. I²C Select.
Insert 2k Discharge Resistor When Disabled	Yes if Start-Up is Wait to Enable Until Output < 300mV	Yes if Start-Up is Wait to Enable Until Output < 300mV	Always

Details of the operation of the LTC3589 are found in the following sections.

ALWAYS-ON LDO

The LTC3589 includes a low quiescent current low dropout regulator that remains powered whenever a valid supply is present on V_{IN}. The always-on LDO will remain active until V_{IN} drops below 2.0V (typical). This is below the 2.5V

OPERATION

undervoltage threshold in effect for the rest of the LTC3589 circuits. The always-on LDO is used to provide power to a standby microcontroller, real-time clock, or other keep-alive circuits. The LDO is guaranteed to support a 25mA load. A 1µF low impedance ceramic bypass capacitor from LDO1_STBY to GND is required for compensation. A power good monitor pulls $\overline{RSTO}$ LOW for a minimum of 14ms (typical) whenever LDO1_STBY is 8% below its regulation target. An LDO1_STBY undervoltage condition is reported in the PGOOD status register. The output voltage of LDO1 is set with a resistor divider connected from LDO1_STBY to the feedback pin LDO1_FB, as shown in Figure 1.

$$V_{LDO1\_STBY} = 0.8 \bullet \left(1 + \frac{R1}{R2}\right)(V)$$

Typical values for R1 are in the range of 40k to 1M.

LDO1_STBY is protected from short-circuits and overloading.

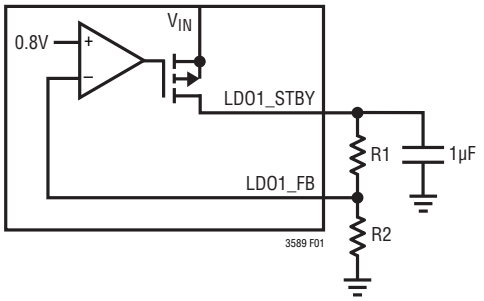

Figure 1. Always-On LDO Application Circuit

250mA LDO REGULATORS

Three LDO regulators on the LTC3589 will each deliver up to 250mA output. The LDO regulators are enabled by pin input or I²C command register. Pin EN_LDO2 enables LDO2 and the LTC3589 EN_LDO34 pin enables LDO3 and LDO4 together. An I²C command register bit is available to decouple LDO4 from pin EN_LDO34 so that LDO4 is under command register control only. The LTC3589-1/LTC3589-2 EN_LDO3 pin enables LDO3 only. LDO4 is controlled using the I²C command registers. All the regulators have current limit protection circuits. Default operation for the LTC3589 is when an LDO regulator is disabled, a 2.5k pull-down resistor is connected to its output.

To help reduce LDO power loss in the system, the regulators have dedicated supply inputs that may be lower than the main V_{IN} supply. Connect a low ESR 1µF capacitor to each of the output pins LDO2, LDO3, and LDO4.

LDO Regulator 2

One of the LTC3589 dynamic slewing DACs serves as the reference input of LDO2. The output range of LDO2 is set using an external resistor divider connected from LDO2 to the feedback pin LDO2_FB, as shown in Figure 2. Set the output voltage of LDO2 using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (0.3625 + L2DTVx \bullet 0.0125)(V)$$

L2DTVx is the five bit word contained in the LDO2 dynamic target voltage 1 (L2DTV1) or the LDO2 dynamic target voltage 2 (L2DTV2) command registers. The default value of L2DTVx[4-0] is 11001 to output a reference voltage of 0.675V. LDO2 is enabled by writing bit 4 in the output voltage enable (OVEN) command register to 1 or driving the EN_LDO2 pin high. Whenever the command is given to slew LDO2 DAC reference to a lower voltage an integrated 2.5k pull-down resistor is connected to LDO2 output.

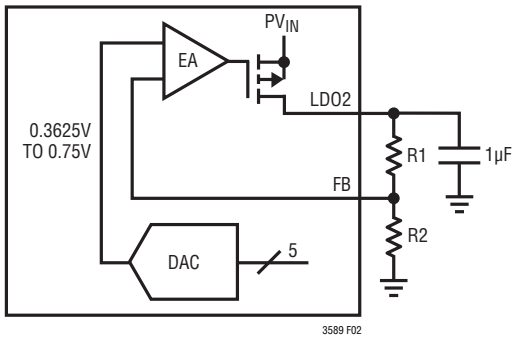

Figure 2. LDO2 Application Circuit

OPERATION

Table 2. Shows the I²C command register settings used to control LDO2.

Table 2. LDO 2 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[4]	0* 1	Disable Enable
SCR2[4] LTC3589/ LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
SCR2[4] LTC3589-2	0* 1	Enable Immediately Wait for Output Below 300mV Before Enable
VCCR[7]	0* 1	Select Register L2DTV1 (V1) Reference Select Register L2DTV2 (V2) Reference
VCCR[6]	1	Initiate Dynamic Voltage Slew
VRRCR[7-6]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
L2DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
L2DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
L2DTV1[7]	0* 1	Shutdown LDO2 Normally Keep LDO2 Alive
L2DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2

* Denotes Default Power-On Value

LDO Regulator 3

LDO3 is a fixed 1.8V or 2.8V (LTC3589-1/LTC3589-2) output regulator. LDO3 is enabled by driving pin EN_LDO34 or EN_LDO3 high or by writing command register OVEN[5] to 1.

Table 3 shows the I²C command register settings used to control LDO3.

Table 3. LDO 3 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[5]	0* 1	Disable Enable
SCR2[5] LTC3589 LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
SCR2[5] LTC3589-2	0* 1	Enable Immediately Wait for Output Below 300mV Before Enable

* Denotes Default Power-On Value

LDO Regulator 4

LDO4 has four output voltage options that are controlled by the contents of command register bits L2DTV2[6] and L2DTV2[5]. When pin EN_LDO34 is low, LDO3 and LDO4 are controlled by writing to command register bits OVEN[5] and OVEN[6] respectively. By default, the LTC3589 pin EN_LDO34 enables and disables LDO3 and LDO4 simultaneously when command register bits OVEN[5] and OVEN[6] are low. When command register bit L2DTV2[7] is high, control of LDO4 is disconnected from pin EN_LDO34 and controlled by command register bit OVEN[6] regardless of the status of EN_LDO34. The LTC3589-1/LTC3589-2 pin EN_LDO3 enables only LDO3. Control of LDO4 on the LTC3589-1/LTC3589-2 is under I²C control only. Table 4 shows the I²C command register settings that control LDO4.

Table 4. LTC3589 LDO4 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
OVEN[6]	0* 1	Disable Enable
SCR2[6]	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
L2DTV2[6-5]	00* 01 10 11	V_{LDO4} = 2.8V V_{LDO4} = 2.5V V_{LDO4} = 1.8V V_{LDO4} = 3.3V
L2DTV2[7]	0* 1	LDO4 Enable Controlled by EN_LDO34 LDO4 Enable Controlled by OVEN[6]
LTC3589-1/LTC3589-2 LDO4 Command Register Settings		
OVEN[6]	0* 1	Disable Enable
SCR2[6] LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
SCR2[6] LTC3589-2	0* 1	Enable Immediately Wait for Output Below 300mV Before Enable
L2DTV2[6-5]	00* 01 10 11	V_{LDO4} = 1.2V V_{LDO4} = 1.8V V_{LDO4} = 2.5V V_{LDO4} = 3.2V
L2DTV2[7]	0* 1	Unused

* Denotes Default Power-On Value

OPERATION

STEP-DOWN SWITCHING REGULATORS

Output Voltage Programming

Each of the step-down converters uses a dynamically slewing DAC output for its reference. The full-scale output voltage is set by using a resistor divider connected from the step-down switching regulator output to the feedback pins (B1_FB, B2_FB, and B3_FB), as shown in Figure 3. Set the output voltage of step-down switching regulators using the following formula:

$$V_{OUT} = \left(1 + \frac{R1}{R2}\right) \bullet (0.3625 + BxDTVx \bullet 0.0125)(V)$$

BxDTVx is the decimal value of the five bit binary number in the I^2C BxDTV1 or BxDTV2 command registers. BxDTV1 and BxDTV2 default to 11001 to output a reference voltage of 0.675V. Typical values for R1 are in the range of 40k to 1M. The capacitor C_{FB} cancels the pole created by the feedback resistors and the input capacitance on the FB pin and also helps to improve load step transient response. A value of 10pF is recommended for most applications. Experimentation with capacitor sizes between 10pF and 33pF may yield improved transient response.

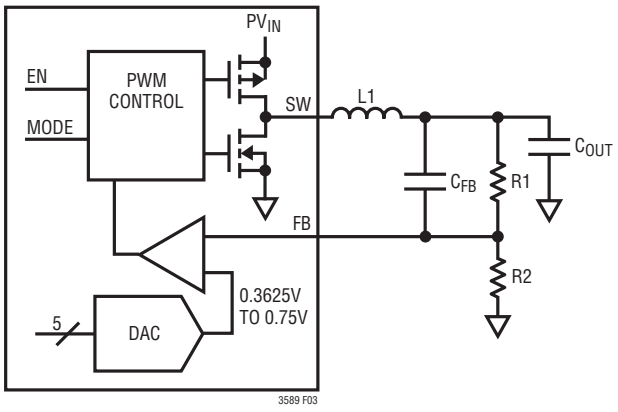

Figure 3. Step-Down Switching Regulator Application Circuit

Operating Modes

The step-down switching regulators include three possible operating modes to meet the noise and power needs of a variety of applications.

In pulse-skipping mode, at the start of every cycle, a latch is set that turns on the main P-channel MOSFET switch. During the cycle, a current comparator compares the peak inductor current to the output of an error amplifier. The output of the current comparator resets the latch. At this time the P-channel MOSFET switch turns off and the N-channel MOSFET synchronous rectifier turns on. The N-channel MOSFET synchronous rectifier will turn off when the end of the clock cycle is reached or if the inductor current drops through zero. Using this method of operation, the error amplifier adjusts the peak inductor current to deliver the required output power. All necessary loop compensation is internal to the step-down switching regulator requiring only a single ceramic output capacitor for stability. At light loads in pulse-skipping mode, the inductor current may reach zero on each pulse that will turn off the N-channel MOSFET synchronous rectifier. In this case the switch node (SW1, SW2, or SW3) goes HIGH impedance and the switch node will ring. This is discontinuous operation and is normal behavior for a switching regulator. At very light loads in pulse-skipping mode, the step-down switching regulators will automatically skip pulses as needed to maintain output regulation. At high duty cycle ($V_{OUTX} > V_{IN}/2$) it is possible for the inductor current to reverse at light loads causing the step-down switching regulator to operate continuously. When operating continuously, regulation and low noise output voltage are maintained, but input operating current will increase to a few milliamps.

In the forced continuous mode of operation, the inductor current is allowed to be less than zero over the full range of duty cycles. Operating in forced continuous mode is a lower noise option at light loads than pulse-skipping operation but with the drawback of higher V_{IN} current due to the continuous operation of the MOSFET switch

OPERATION

and rectifier. Since the inductor current is allowed to be negative in forced continuous operation the step-down switching regulator has the ability to sink output current. The LTC3589 automatically forces the step-down switching regulator into forced continuous mode when dynamically slewing the DAC voltage reference down.

When the LTC3589 step-down switching regulators are in Burst Mode operation, they automatically switch between fixed frequency pulse-skipping operation and hysteretic Burst Mode control as a function of the load current. At light loads the step-down switching regulators control the inductor current directly and use a hysteretic control loop to minimize both noise and switching losses. While in Burst Mode operation, the output capacitor is charged to a voltage slightly higher than the regulation point. The step-down switching regulator then goes into a low power sleep mode during which the output capacitor provides the load current. In sleep mode, most of the switching regulator's circuitry is powered off to conserve battery power. When the output voltage drops below the regulation point the regulator's circuitry is powered on and another burst cycle begins. As the load current increases, the time between burst cycles decreases. Above a load current about one-quarter rated output load, the step-down switching regulators will switch to low noise constant-frequency PWM operation.

Set the mode of operation for the step-down switching regulators by using the I^2C command register SCR1. Each of the three regulators has independent mode control.

A step-down switching regulator may enter a dropout condition when its input voltage drops to near its programmed output voltage. For example, a discharging battery voltage of 3.4V dropping to the regulators programmed output voltage of 3.3V. When this happens the duty cycle of the P-channel MOSFET switch is increased until it turns on continuously with 100% duty cycle. In dropout, the regulators output voltage equals the regulators input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor DC resistance.

Table 5, Table 6, and Table 7 show the I^2C command register settings used to control the step-down switching regulators.

Table 5. Step-Down Switching Regulator 1 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[1-0]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[0]	0* 1	Disable Enable
SCR2[0] LTC3589/ LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
SCR2[0] LTC3589-2	0* 1	Enable Immediately Wait for Output Below 300mV Before Enable
VCCR[1]	0* 1	Select Register B1DTV1 (V1) Reference Select Register B1DTV2 (V2) Reference
VCCR[0]	1	Initiate Dynamic Voltage Slew
VRRCR[1-0]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B1DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B1DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B1DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B1DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B1DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B1DTV2[7]	0* 1	Shutdown Regulator 1 Normally Keep Regulator 1 Alive

* Denotes Default Power-On Value

Soft-Start

Soft-start is accomplished by gradually increasing the input reference voltage on each step-down switching regulator from 0V to the dynamic reference DAC output level at a rate of 0.8V/ms. This allows each output to rise slowly, helping minimize inrush current required to charge up the regulator output capacitor. A soft-start cycle

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occurs whenever a regulator is enabled either initially or while powering up following a fault condition. A soft-start cycle is not triggered by a change of operating modes or a dynamic voltage slew. During soft-start the converter is forced to pulse-skipping mode regardless of the settings in the SCR1 command register.

Table 6. Step-Down Switching Regulator 2 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[3-2]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[1]	0* 1	Disable Enable
SCR2[1] LTC3589/ LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable immediately
SCR2[1] LTC3589-2	0* 1	Enable immediately Wait for Output Below 300mV Before Enable
VCCR[3]	0* 1	Select Register B2DTV1 (V1) Reference Select Register B2DTV2 (V2) Reference
VCCR[2]	1	Initiate Dynamic Voltage Slew
VRRCR[3-2]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B2DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B2DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B2DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B2DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B2DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B2DTV2[7]	0* 1	Shutdown Regulator 2 Normally Keep Regulator 2 Alive

* Denotes Default Power-On Value

Since slowing the slew rate of the switch nodes causes efficiency loss, the slew rate of the step-down switching regulators is adjustable using the I²C command register B1DTV1 bits 6 and 7. Optimize efficiency or EMI as necessary with four different slew rate settings. The power-on default is the fastest slew rate, highest efficiency setting.

Table 7. Step-Down Switching Regulator 3 Command Register Settings

COMMAND REGISTER[BIT]	VALUE	SETTING
SCR1[5-4]	00* 01 10	Pulse-Skipping Mode Burst Mode Operation Forced Continuous Mode
OVEN[2]	0* 1	Disable Enable
SCR2[2] LTC3589/ LTC3589-1	0* 1	Wait for Output Below 300mV Before Enable Enable Immediately
SCR2[2] LTC3589-2	0* 1	Enable Immediately Wait for Output Below 300mV Before Enable
VCCR[5]	0* 1	Select Register B3DTV1 (V1) Reference Select Register B3DTV2 (V2) Reference
VCCR[4]	1	Initiate Dynamic Voltage Slew
VRRCR[5-4]	00 01 10 11*	Reference Slew Rate = 0.88mV/µs Reference Slew Rate = 1.75mV/µs Reference Slew Rate = 3.5mV/µs Reference Slew Rate = 7mV/µs
B3DTV1[5]	0* 1	Force PGOOD Low When Slewing Normal PGOOD Operation When Slewing
B3DTV1[4-0]	11001*	DAC Dynamic Target Voltage V1
B3DTV2[4-0]	11001*	DAC Dynamic Target Voltage V2
B3DTV2[5]	0* 1	2.25MHz Switching Frequency 1.125MHz Switching Frequency
B3DTV2[6]	0* 1	Switch on Clock Phase 1 Switch on Clock Phase 2
B3DTV2[7]	0* 1	Shutdown Regulator 3 Normally Keep Regulator 3 Alive

* Denotes Default Power-On Value

Switching EMI Control

The step-down switching regulators contain new patent pending circuitry to limit the edge rate of the switch nodes SW1, SW2, and SW3. This new circuitry controls the transition of the switch node over a period of a few nanoseconds, significantly reducing radiated EMI and conducted supply noise while maintaining high efficiency.

Operating Frequency

The switching frequency of each of the LTC3589 step-down switching regulators may be independently set using I²C command register bits B1DTV2[5], B2DTV2[5] and B3DTV2[5]. The power-on default frequency is 2.25MHz. Writing bit BxDTV2[5] HIGH will reduce the switching frequency to 1.125MHz. Selection of the operating

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frequency is determined by desired efficiency, component size and converter duty cycle.

Operation at lower frequency improves efficiency by reducing internal gate charge and switching losses but requires larger inductance and capacitance values for comparable output ripple voltage. The lowest duty cycle of the step-down switching regulator is determined by the converters minimum on-time. Minimum on-time is the shortest time duration that the converter is capable of turning its top PMOS on and off again. The time consists of the gate charge time plus internal delays associated with peak current sensing. The minimum on-time of the LTC3589 is approximately 90ns. If the duty cycle falls below what can be accommodated by the minimum on-time, the converter will begin to skip cycles. The output voltage will continue to be regulated but the ripple voltage and current will increase. With the switching frequency set to 2.25MHz, the minimum supported duty cycle is 20%. Switching at 1.125MHz the converter can support a 10% duty cycle.

Phase Selection

To reduce the cycle by cycle peak current drawn by the switching regulators, the clock phase of each of the LTC3589 step-down switching regulators can be set using I^2C command register bits B1DTV2[6], B2DTV2[6] and B3DTV2[6]. The internal full-rate clock has a nominal duty cycle of 20% while the half-rate clocks have a 50% duty cycle. Setting the command register bits high will delay the start of each converter switching cycle by 20% or 50% depending on the selected operating frequency.

Inductor Selection

The choice of step-down switching regulator inductor influences the efficiency of the converter and the magnitude of the output voltage ripple. Larger inductance values reduce inductor current ripple and therefore lower output voltage ripple. A larger value inductor improves efficiency by lowering the peak current to be closer to the average output current. Larger inductors, however, generally have higher series resistance that counters the efficiency advantage of reduced peak current.

Inductor ripple current is a function of switching frequency, inductance, V_{IN}, and V_{OUT}, as shown in this equation:

$$\Delta I_L = \frac{1}{f \bullet L} \bullet V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In an example application the LTC3589 step-down switching regulator 3 has a maximum load of 1A, V_{IN} equals 3.8V, and V_{OUT} is set for 1.2V. A good starting design point for inductor ripple is 30% of output current or 300mA. Using the equation for ripple current, a 1.2µH inductor should be selected.

An inductor with low DC resistance will improve converter efficiency. Select an inductor with a DC current rating at least 1.5 times larger than the maximum load current to ensure the inductor does not saturate during normal operations. If short-circuit is a possible condition, the inductor should be rated to handle the maximum peak current specified for the step-down converter. Table 8 shows inductors that work well with the step-down switching regulators.

Input/Output Capacitor Selection

Low ESR (equivalent series resistance) ceramic capacitors should be used at both the output and input supply of the switching regulators. Only X5R or X7R ceramic capacitors should be used because they retain their capacitance over wider voltage and temperature ranges than other ceramic types. A 22µF capacitor is sufficient for the step-down switching regulator outputs. For good transient response and stability the output capacitor should retain at least 10µF of capacitance over operating temperature and bias voltage. Place at least 4.7µF decoupling capacitance as close as possible to each PV_{IN} pin. Refer to Table 12 for recommended ceramic capacitor manufacturers.

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BUCK-BOOST SWITCHING REGULATOR

Output Voltage Programming

Set the output voltage of the LTC3589 buck-boost switching regulator using an external resistor divider connected from BB_OUT to the feedback pin BB_FB and to GND, as shown in Figure 4.

$$V_{BB\_OUT} = 0.8 \bullet \left(1 + \frac{R1}{R2}\right)(V)$$

The value of R1 plays a role in setting the dynamics of the buck-boost voltage mode control loop. In general, a larger value for R1 will increase stability but reduce the speed of the transient response. A good starting point is to choose R1 equal to 1MΩ and calculate the value of R2 needed to set the target output voltage. If a large output capacitor is used, the bandwidth of the converter is reduced and R1 may be reduced to improve transient response. If a large inductor or small output capacitor is used then a larger R1 should be used to bring the loop toward more stable operation.

Table 8. Inductors for Step-Down Switching Regulator 1

MANUFACTURERS	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft	XPL4020-102ML	1.0	0.029	4.00	4.2 × 4.2 × 2.0
	XPL4020-152ML	1.5	0.036	3.60	4.2 × 4.2 × 2.0
	XPL4020-222ML	2.2	0.060	2.60	4.2 × 4.2 × 2.0
	LPS6225-222ML	2.2	0.045	3.90	6.0 × 6.0 × 2.0
	LPS6225-332ML	3.3	0.055	3.50	6.0 × 6.0 × 2.0
	LPS6225-472ML	4.7	0.065	3.00	6.0 × 6.0 × 2.0
Cooper	SD14-1R2-R	1.2	0.034	3.35	5.2 × 5.2 × 1.45
	SD14-1R5-R	1.5	0.039	2.91	5.2 × 5.2 × 1.45
	SD14-2R0-R	2.0	0.045	2.56	5.2 × 5.2 × 1.45
	SD25-2R2-R	2.2	0.031	2.80	5.2 × 5.2 × 2.5
Sumida	CDRH5D16NP-3R3N	3.3	0.045	2.60	5.6 × 5.6 × 1.8
TDK	VLF5014ST-1R0N2R7	1.0	0.050	2.7	4.8 × 4.6 × 1.4
	VLF5014st-2R2N2R3	2.2	0.073	2.3	4.8 × 4.6 × 1.4
	VLCF5020T-2R2N2R6-1	2.2	0.071	2.6	5.0 × 5.0 × 2.0
TOKO	1124BS-1R2N	1.2	0.047	2.9	4.5 × 4.7 × 1.8
	1124BS-1R8N	1.8	0.056	2.7	4.5 × 4.7 × 1.8
Tokin	H-DI-0520-2R2	2.2	0.048	2.6	5.3 × 5.3 × 2.0
	H-DI-0630-2R4	2.4	0.028	2.5	6.3 × 6.3 × 3.0
	H-DI-0630-3R8	3.8	0.040	2	6.3 × 6.3 × 3.0
Wurth	744042001	1.0	0.028	2.60	4.8 × 4.8 × 1.8
	744052002	2.5	0.030	2.4	5.8 × 5.8 × 1.8
	744053003	3.0	0.024	2.8	5.8 × 5.8 × 2.8
	7440530047	4.7	0.030	2.4	5.8 × 5.8 × 2.8
	7440430022	2.2	0.023	2.5	4.8 × 4.8 × 2.8

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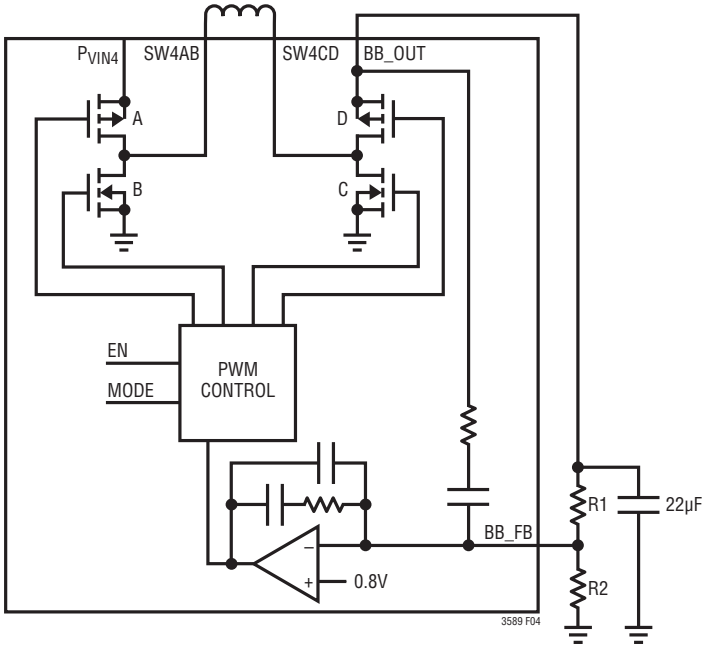

Figure 4. Buck-Boost Switching Regulator Application Circuit

Table 9. Inductors for Step-Down Switching Regulators 2 and 3

MANUFACTURERS	PART NUMBER	VALUE (µH)	DCR (Ω)	MAX DC CURRENT (A)	SIZE (mm) W × L × H
Coilcraft	XPL4020-102ML	1.0	0.029	4.00	4.2 × 4.2 × 2.0
	XPL4020-152ML	1.5	0.036	3.60	4.2 × 4.2 × 2.0
	XPL4020-472ML	4.7	0.130	1.90	4.2 × 4.2 × 2.0
Cooper	SD14-1R2-R	1.2	0.034	3.35	5.2 × 5.2 × 1.45
	SD14-3R2-R	3.2	0.066	2.00	5.2 × 5.2 × 1.45
	SD25-3R3-R	3.3	0.038	2.21	4.8 × 4.8 × 2.5
Sumida	CDRH5D16NP-4R7N	4.7	0.064	2.05	5.6 × 5.6 × 1.8
	CDRH38D16RHPNP-3R3M	3.3	0.059	1.46	4.2 × 4.2 × 1.8
TDK	VLF5014ST-2R2N2R3	2.2	0.073	2.3	4.8 × 4.6 × 1.4
	VLCF5020T-2R7N2R2-1	2.7	0.083	2.2	5.0 × 5.0 × 2.0
	VLCF5020T-3R3N2R0-1	3.3	0.096	2	5.0 × 5.0 × 2.0
TOKO	1124BS-2R4N	2.4	0.065	2.30	4.5 × 4.7 × 1.8
	1124BS-3R3N	3.3	0.074	2.10	4.5 × 4.7 × 1.8
Tokin	H-DI-0520-3R3	3.3	0.062	2.00	5.3 × 5.3 × 2.0
	H-DI-0520-4R7	4.7	0.090	1.80	5.3 × 5.3 × 2.0
	H-DI-0630-3R8	3.8	0.040	2.00	6.3 × 6.3 × 3.0
	H-DI-0630-4R7	4.7	0.043	1.90	6.3 × 6.3 × 3.0
Wurth	744043004	4.7	0.052	1.55	5.0 × 5.0 × 3.0
	744052002	2.5	0.030	2.4	5.8 × 5.8 × 1.8
	7440530047	4.7	0.030	2.4	5.8 × 5.8 × 2.8
	744042003	3.3	0.055	1.95	4.8 × 4.8 × 1.8
	7440430022	2.2	0.023	2.5	4.8 × 4.8 × 2.8