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LINEAR TECHNOLOGY

LTC3619

400mA/800mA Synchronous Step-Down DC/DC with Average Input Current Limit

FEATURES

- **Programmable Average Input Current Limit: ±5% Accuracy**
- **Dual Step-Down Outputs: Up to 96% Efficiency**
- **Low Ripple (<25mV$_{P-P}$) Burst Mode® Operation: I$_Q$ = 50µA**
- **Input Voltage Range: 2.5V to 5.5V**
- **Output Voltage Range: 0.6V to 5V**
- **2.25MHz Constant-Frequency Operation**
- **Power Good Output Voltage Monitor for Each Channel**
- **Low Dropout Operation: 100% Duty Cycle**
- **Independent Internal Soft-Start for Each Channel**
- Current Mode Operation for Excellent Line and Load Transient Response
- ±2% Output Voltage Accuracy
- Short-Circuit Protected
- Shutdown Current ≤ 1µA
- Available in Small Thermally Enhanced 10-Lead MSE and 3mm × 3mm DFN Packages

APPLICATIONS

- High Peak Load Current Applications
- USB Powered Devices
- Supercapacitor Charging
- Radio Transmitters and Other Handheld Devices

DESCRIPTION

The LTC®3619 is a dual monolithic synchronous buck regulator using a constant frequency, current mode architecture.

The input supply voltage range is 2.5V to 5.5V, making it ideal for Li-Ion and USB powered applications. 100% duty cycle capability provides low dropout operation, extending the run time in battery-operated systems. Low output voltages are supported with the 0.6V feedback reference voltage. Channel 1 and channel 2 can supply 400mA and 800mA output current, respectively.

The LTC3619's programmable average input current limit is ideal for USB applications and for point-of-load power supplies because the LTC3619's limited input current will still allow its output to deliver high peak load currents without collapsing the input supply. When the sum of both channels' currents exceeds the input current limit, channel 2 is current limited while channel 1 remains regulated. The operating frequency is internally set at 2.25MHz allowing the use of small surface mount inductors. Internal soft-start reduces in-rush current during start-up. The LTC3619 is available in small MSOP and 3mm × 3mm DFN packages and is also available in a low noise, high efficiency pulse-skipping version, LTC3619B.

TYPICAL APPLICATION
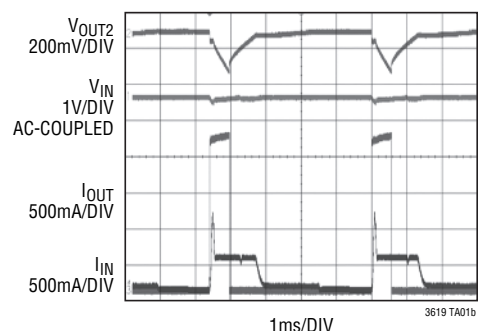
Dual Monolithic Buck Regulator in 10-Lead 3mm × 3mm DFN

I$_{LIM}$ = 475mA
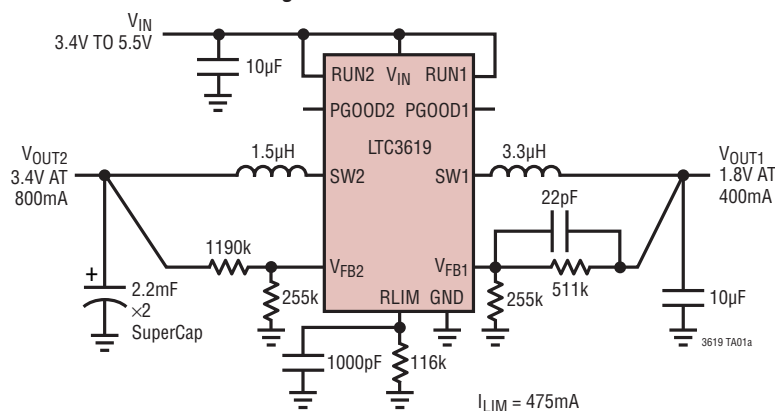
GSM Pulse Load

V$_{IN}$ = 5V, 500mA COMPLIANT,
I$_{LOAD}$ = 0A TO 2.2A, CHANNEL 1 UNLOADED

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) .... −0.3 to 6V
V_{FB1}, V_{FB2} .... −0.3V to V_{IN} + 0.3V
RUN1, RUN2, RLIM .... −0.3V to V_{IN} + 0.3V
SW1, SW2 .... −0.3V to V_{IN} + 0.3V
PGOOD1, PGOOD2 .... −0.3V to V_{IN} + 0.3V
P-Channel SW Source Current (DC) (Note 2)
    Channel 1 .... 600mA
    Channel 2 .... 1A
N-Channel SW Source Current (DC) (Note 2)
    Channel 1 .... 600mA
    Channel 2 .... 1A

Peak SW Source and Sink Current (Note 2)
    Channel 1 .... 900mA
    Channel 2 .... 2A
Operating Junction Temperature Range
    (Notes 3, 6, 8) .... −40°C to 125°C
Storage Temperature Range .... −65°C to 125°C
Lead Temperature (Soldering, 10 sec)
    MSOP Package .... 300°C
Reflow Peak Body Temperature .... 260°C

PIN CONFIGURATION

TOP VIEW

V_{FB1}	1	10	V_{FB2}
RUN1	2	9	RUN2
RLIM	3	8	PGOOD2
PGOOD1	4	7	SW2
SW1	5	6	V_{IN}

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DD PACKAGE
10-LEAD (3mm × 3mm) PLASTIC DFN
T_{JMAX} = 125°C, $θ_{JA}$ = 40°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

TOP VIEW

V_{FB1}	1	10	V_{FB2}
RUN1	2	9	RUN2
RLIM	3	8	PGOOD2
PGOOD1	4	7	SW2
SW1	5	6	V_{IN}

11

MSE PACKAGE
10-LEAD PLASTIC MSOP
T_{JMAX} = 125°C, $θ_{JA}$ = 45°C/W
EXPOSED PAD (PIN 11) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3619EDD#PBF	LTC3619EDD#TRPBF	LFKM	10-Lead (3mm × 3mm) Plastic DFN	−40°C to 85°C
LTC3619IDD#PBF	LTC3619IDD#TRPBF	LFKM	10-Lead (3mm × 3mm) Plastic DFN	−40°C to 125°C
LTC3619EMSE#PBF	LTC3619EMSE#TRPBF	LTFKN	10-Lead Plastic MSOP	−40°C to 85°C
LTC3619IMSE#PBF	LTC3619IMSE#TRPBF	LTFKN	10-Lead Plastic MSOP	−40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 5V, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN}	V_{IN} Operating Voltage Range		●	2.5		5.5	V
V_{UV}	V_{IN} Undervoltage Lockout	V_{IN} Low to High	●		2.1	2.5	V

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ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at $T_A = 25°C$, $V_{IN} = 5V$, unless otherwise noted. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{FB}	Feedback Pin Input Current		●			±30	nA
V_{FBREG}	Feedback Voltage (Channels 1, 2)	LTC3619E, $-40°C \leq T_J \leq 85°C$ LTC3619I, $-40°C \leq T_J \leq 125°C$	● ●	0.588 0.582	0.600 0.600	0.612 0.618	V V
$\Delta V_{LINEREG}$	V_{FB} Line Regulation	$V_{IN} = 2.5V$ to $5.5V$ (Note 7)			0.01	0.25	%/V
$\Delta V_{LOADREG}$	V_{FB} Load Regulation (Channel 1) V_{FB} Load Regulation (Channel 2)	$I_{LOAD} = 0mA$ to $400mA$ (Note 7) $I_{LOAD} = 0mA$ to $800mA$ (Note 7)			0.5 0.5		% %

I_S	Supply Current
	    Active Mode (Note 4)
	    Sleep Mode
	    Shutdown
		
		 $V_{FB1} = V_{FB2} = 0.95 \times V_{FBREG}$
		 $V_{FB} = 1.05 \times V_{FBREG}$, $V_{IN} = 5.5V$
		 $V_{RUN1} = V_{RUN2} = 0V$, $V_{IN} = 5.5V$
					
					 600
					 50
						
						 875
						 100
						 1
							
							 μA
							 μA
							 μA

f_{OSC}	Oscillator Frequency	$V_{FB} = 0.6V$	●	1.8	2.25	2.7	MHz

$I_{LIM(PEAK)}$	Peak Switch Current Limit
	    Channel 1 (400mA)
	    Channel 2 (800mA)
		$V_{IN} = 5V$, $V_{FB} < V_{FBREG}$, Duty Cycle <35%		
				 550
				 1200
					
					 800
					 1600
							
							 mA
							 mA

$I_{INLIM (PEAK)}$	Input Average Current Limit	RLIM = 116k RLIM = 116k, LTC3619E RLIM = 116k, LTC3619I	 ● ●	450 437 427	475 475 475	500 513 523	mA mA mA

$R_{DS(ON)}$	Channel 1 (Note 5)
	    Top Switch On-Resistance
	    Bottom Switch On-Resistance
	 Channel 2 (Note 5)
	    Top Switch On-Resistance
	    Bottom Switch On-Resistance
		
		 $V_{IN} = 5V$, $I_{SW} = 100mA$
		 $V_{IN} = 5V$, $I_{SW} = 100mA$
		
		 $V_{IN} = 5V$, $I_{SW} = 100mA$
		 $V_{IN} = 5V$, $I_{SW} = 100mA$
					
					 0.45
					 0.35
					
					 0.27
					 0.25
							
							 Ω
							 Ω
							
							 Ω
							 Ω

$I_{SW(LKG)}$	Switch Leakage Current	$V_{IN} = 5V$, $V_{RUN} = 0V$			0.01	1	μA
$t_{SOFTSTART}$	Soft-Start Time	V_{FB} from 0.06V to 0.54V		0.3	0.95	1.3	ms
V_{RUN}	RUN Threshold High		●	0.4	1	1.2	V
I_{RUN}	RUN Leakage Current		●		0.01	1	μA

PGOOD	Power Good Threshold
	   Entering Window
	     V_{FB} Ramping Up
	     V_{FB} Ramping Down
	   Leaving Window
	     V_{FB} Ramping Up
	     V_{FB} Ramping Down
				
				 −5
				 5
				
					 −7
					 7
					
					 9
					 −9
						
						 11
						 −11
							
							 %
							 %
							
							 %
							 %

PGOOD Blanking	Power Good Blanking Time	PGOOD Rising and Falling, $V_{IN} = 5V$			90		μs
R_{PGOOD}	Power Good Pull-Down On-Resistance			8	15	30	Ω
I_{PGOOD}	PGOOD Leakage Current	$V_{PGOOD} = 5V$				±1	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Guaranteed by long term current density limitations.

Note 3: The LTC3619 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3619E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the −40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3619I is guaranteed to meet specified performance over the full −40°C to 125°C operating junction temperature range.

Note 4: Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency.

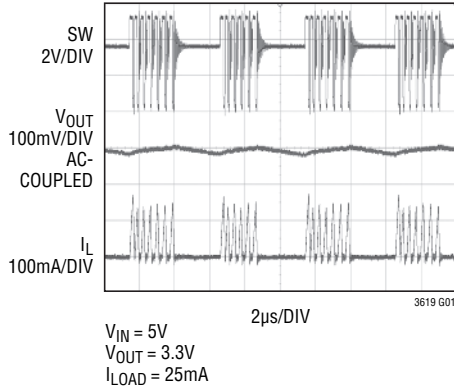**Note 5:** The switch on-resistance is guaranteed by correlation to wafer level measurements.

Note 6: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. Junction temperature will exceed 125°C when overtemperature protection is active. Continuous operation above the specified maximum operating junction temperature may impair device reliability.

Note 7: The converter is tested in a proprietary test mode that connects the output of the error amplifier to the SW pin, which is connected to an external servo loop.
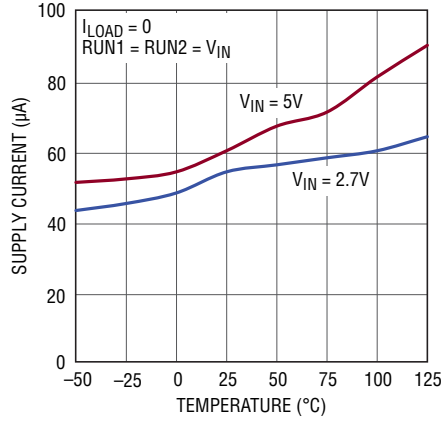
Note 8: T_J is calculated from the ambient temperature T_A and the power dissipation as follows: $T_J = T_A + (P_D)(\theta_{JA}°C/W)$.

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 5V$, unless otherwise noted.

Burst Mode Operation

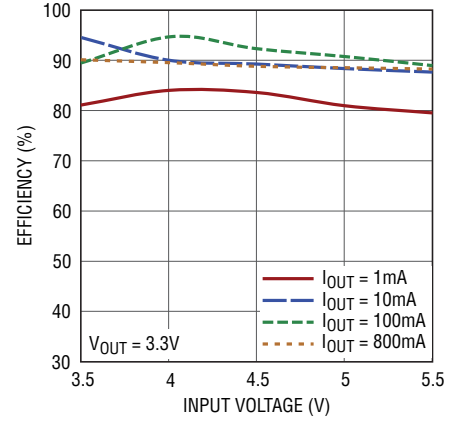

SW
2V/DIV

V_{OUT}
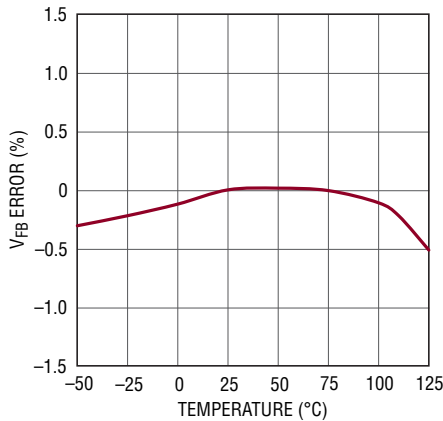100mV/DIV
AC-
COUPLED

I_L
100mA/DIV

2µs/DIV

3619 G01

$V_{IN} = 5V$
$V_{OUT} = 3.3V$
$I_{LOAD} = 25mA$

Supply Current vs Temperature

$I_{LOAD} = 0$
RUN1 = RUN2 = V_{IN}

$V_{IN} = 5V$

$V_{IN} = 2.7V$

3619 G02

Efficiency vs Input Voltage (Channel 2)

$I_{OUT} = 1mA$
$I_{OUT} = 10mA$
$I_{OUT} = 100mA$
$I_{OUT} = 800mA$

$V_{OUT} = 3.3V$

3619 G02

Regulated Voltage vs Temperature

3619 G04

Oscillator Frequency vs Temperature

$V_{IN} = 2.7V$
$V_{IN} = 3.6V$
$V_{IN} = 4.2V$
$V_{IN} = 5V$

3619 G05
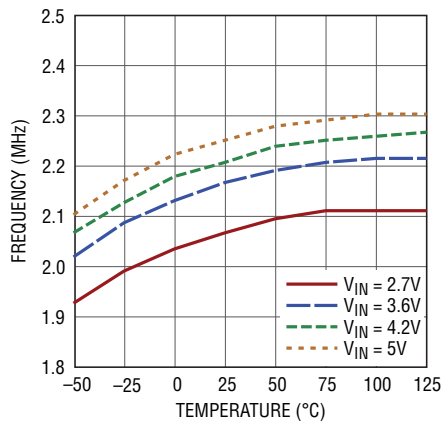
Switch Leakage vs Input Voltage

CHANNEL 1
CHANNEL 2

MAIN SWITCH

SYNCHRONOUS SWITCH

3619 G06
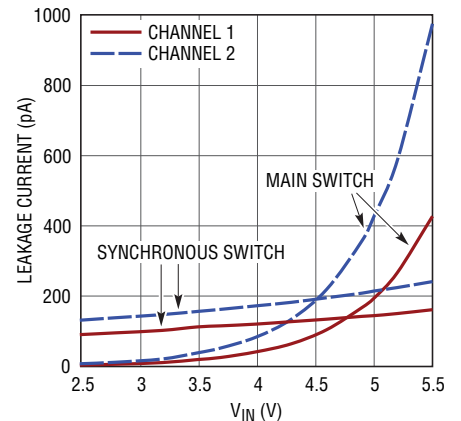
Switch On-Resistance vs Input Voltage

CHANNEL 1
CHANNEL 2

MAIN SWITCH

SYNCHRONOUS SWITCH

3619 G07

Switch On-Resistance vs Temperature

CHANNEL 1

MAIN SWITCH

SYNCHRONOUS SWITCH

$V_{IN} = 2.7V$
$V_{IN} = 3.6V$
$V_{IN} = 5V$

3619 G08

Switch On-Resistance vs Temperature

CHANNEL 2

(PFET)
MAIN SWITCH

(NFET)
SYNCHRONOUS SWITCH

$V_{IN} = 2.7V$
$V_{IN} = 3.6V$
$V_{IN} = 5V$

3619 G09

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LINEAR
TECHNOLOGY

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 5V$, unless otherwise noted.

Efficiency vs Load Current

EFFICIENCY (%) vs OUTPUT CURRENT (A)

$V_{OUT} = 3.3V$
CHANNEL 1

$V_{IN} = 3.6V$
$V_{IN} = 4.2V$
$V_{IN} = 5V$

3619 G10

Efficiency vs Load Current

EFFICIENCY (%) vs OUTPUT CURRENT (A)

$V_{OUT} = 3.3V$
CHANNEL 2

$V_{IN} = 3.6V$
$V_{IN} = 4.2V$
$V_{IN} = 5V$

3619 G11

Efficiency vs Load Current

EFFICIENCY (%) vs OUTPUT CURRENT (A)

$V_{OUT} = 1.2V$
CHANNEL 1

$V_{IN} = 2.7V$
$V_{IN} = 3.6V$
$V_{IN} = 4.2V$
$V_{IN} = 5V$

3619 G12

Efficiency vs Load Current

EFFICIENCY (%) vs OUTPUT CURRENT (A)

$V_{OUT} = 1.2V$
CHANNEL 2

$V_{IN} = 2.7V$
$V_{IN} = 3.6V$
$V_{IN} = 4.2V$
$V_{IN} = 5V$

3619 G13

Load Regulation (Channel 1)

V_{OUT} ERROR (%) vs LOAD CURRENT (mA)

$V_{OUT} = 1.8V$
$V_{OUT} = 2.5V$
$V_{OUT} = 3.3V$

3619 G14

Load Regulation (Channel 2)

V_{OUT} ERROR (%) vs LOAD CURRENT (mA)

$V_{OUT} = 1.8V$
$V_{OUT} = 2.5V$
$V_{OUT} = 3.3V$

3619 G15

Line Regulation

V_{OUT} ERROR (%) vs V_{IN} (V)

$V_{OUT} = 1.8V$
$I_{LOAD} = 100mA$
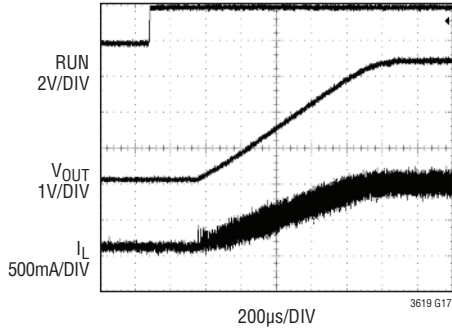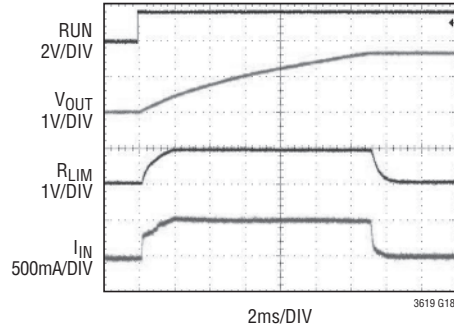
3619 G16

3619fa

TYPICAL PERFORMANCE CHARACTERISTICS $T_A = 25°C$, $V_{IN} = 5V$, unless otherwise noted.
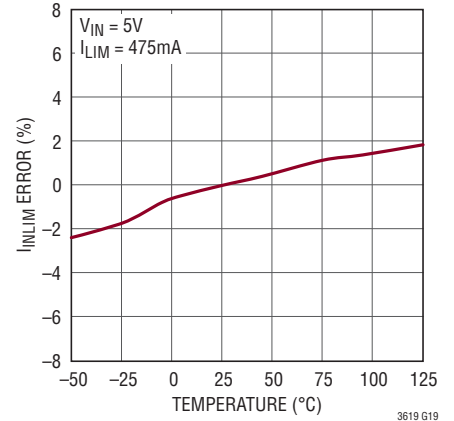
Start-Up from Shutdown

$V_{IN} = 5V$, $V_{OUT} = 3.3V$
$R_{LOAD} = 7\Omega$
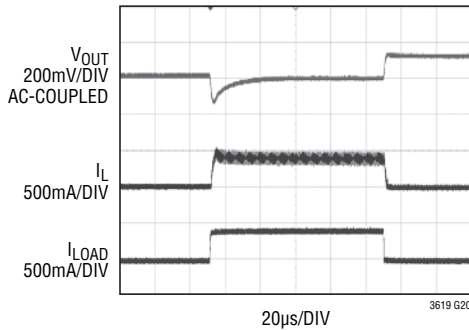$C_{LOAD} = 4.7\mu F$

Start-Up from Shutdown (Channel 2)

$V_{IN} = 5V$, $V_{OUT} = 3.4V$
R_L = NO LOAD, $C_L = 4.4mF$
$C_{LIM} = 2200pF$, $I_{LIM} = 500mA$

Average Input Current Limit vs Temperature

Load Step (Channel 1)

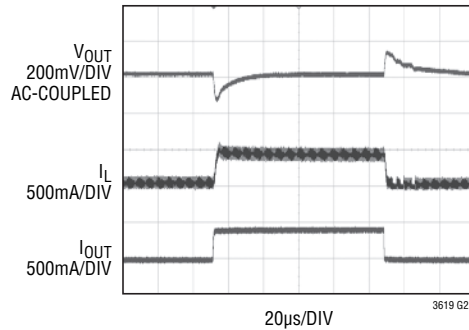

$V_{IN} = 5V$, $V_{OUT} = 3.3V$
I_{LOAD} = 0A TO 400mA
$C_L = 4.7\mu F$

Load Step (Channel 1)

$V_{IN} = 5V$, $V_{OUT} = 3.3V$
I_{LOAD} = 40mA TO 400mA
$C_L = 4.7\mu F$

3619fa

PIN FUNCTIONS (DD/MSE)

V_{FB1} (Pin 1/Pin 1): Regulator 1 Output Feedback. Receives the feedback voltage from the external resistive divider across the regulator 1 output. Nominal voltage for this pin is 0.6V.

RUN1 (Pin 2/Pin 2): Regulator 1 Enable. Forcing this pin to V_{IN} enables regulator 1, while forcing it to GND causes regulator 1 to shut down.

RLIM (Pin 3/Pin 3): Average Input Current Limit Program Pin. Place a resistor and capacitor in parallel from this pin to ground.

PGOOD1 (Pin 4/Pin 4): Open-Drain Logic Output. PGOOD1 is pulled to ground the voltage on the V_{FB1} pin is not within power good threshold.

SW1 (Pin 5/Pin 5): Regulator 1 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

V_{IN} (Pin 6/Pin 6): Main Power Supply. Must be closely de-coupled to GND.

SW2 (Pin 7/Pin 7): Regulator 2 Switch Node Connection to the Inductor. This pin swings from V_{IN} to GND.

PGOOD2 (Pin 8/Pin 8): Open-Drain Logic Output. PGOOD2 is pulled to ground the voltage on the V_{FB2} pin is not within power good threshold.

RUN2 (Pin 9/Pin 9): Regulator 2 Enable. Forcing this pin to V_{IN} enables regulator 2, while forcing it to GND causes regulator 2 to shut down.

V_{FB2} (Pin 10/Pin 10): Regulator 2 Output Feedback. Receives the feedback voltage from the external resistive divider across the regulator 2 output. Nominal voltage for this pin is 0.6V.

GND (Pin 11/Pin 11): Ground. Bottom Exposed Pad. Connect to the (–) terminal of C_{OUT}, and the (–) terminal of C_{IN}. The Exposed Pad must be soldered to PCB.

FUNCTIONAL DIAGRAM
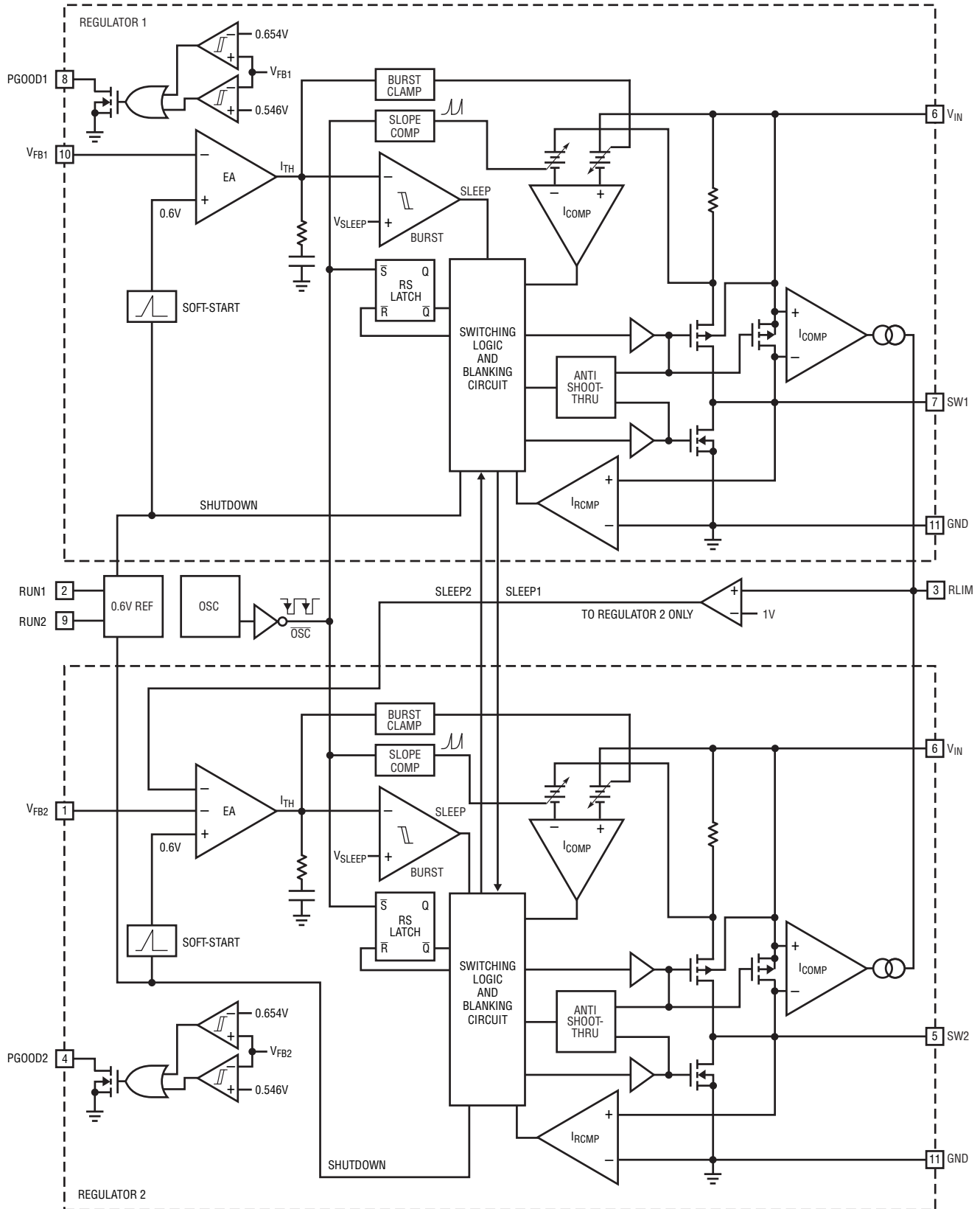
OPERATION

The LTC3619 uses a constant-frequency, current mode architecture. The operating frequency is set at 2.25MHz. Both channels share the same clock and run in-phase.

The output voltage is set by an external resistor divider returned to the V_{FB} pins. An error amplifier compares the divided output voltage with a reference voltage of 0.6V and regulates the peak inductor current accordingly.

The LTC3619 continuously monitors the input current of both channels. When the sum of the currents of both channels exceeds the programmed input current limit set by an external resistor, R_{LIM}, channel 2 is current limited while channel 1 remains regulated.

Main Control Loop

During normal operation, the top power switch (P-channel MOSFET) is turned on at the beginning of a clock cycle when the V_{FB} voltage is below the reference voltage. The current into the inductor and the load increases until the peak inductor current (controlled by I_{TH}) is reached. The RS latch turns off the synchronous switch and energy stored in the inductor is discharged through the bottom switch (N-channel MOSFET) into the load until the next clock cycle begins, or until the inductor current begins to reverse (sensed by the I_{RCMP} comparator).

The peak inductor current is controlled by the internally compensated I_{TH} voltage, which is the output of the error amplifier. This amplifier regulates the V_{FB} pin to the internal 0.6V reference by adjusting the peak inductor current accordingly.

When the input current limit is engaged, the peak inductor current will be lowered, which then reduces the switching duty cycle and V_{OUT}. This allows the input voltage to stay regulated when its programmed current output capability is met.

Light Load Operation

The LTC3619 will automatically transition from continuous operation to Burst Mode operation when the load current is low. During relatively light loads, the peak inductor current (as set by I_{TH}) remains fixed at approximately 60mA and 120mA for channel 1 and channel 2, respectively. The PMOS switch operates intermittently based on load demand. By running cycles periodically, the switching losses are minimized. The duration of each burst event can range from a few cycles at light load to almost continuous cycling with short sleep intervals at moderate loads. During the sleep intervals, the load current is being supplied solely from the output capacitor. A majority of the internal circuitry is shut off to conserve quiescent current. As the output voltage droops, the error amplifier output rises above the sleep threshold, signaling the burst comparator to un-trip and turns the top MOSFET on. This cycle repeats at a rate that is dependent on load demand.

Dropout Operation

When the input supply voltage decreases toward the output voltage the duty cycle increases to 100%, which is the dropout condition. In dropout, the PMOS switch is turned on continuously with the output voltage being equal to the input voltage minus the voltage drops across the internal P-channel MOSFET and the inductor.

An important design consideration is that the $R_{DS(ON)}$ of the P-channel switch increases with decreasing input supply voltage (see Typical Performance Characteristics). Therefore, the user should calculate the worst-case power dissipation when the LTC3619 is used at 100% duty cycle with low input voltage (see Thermal Considerations in the Applications Information section).

Soft-Start

In order to minimize the inrush current on the input bypass capacitor, the LTC3619 slowly ramps up the output voltage during start-up. Whenever the RUN1 or RUN2 pin is pulled high, the corresponding output will ramp from zero to full-scale over a time period of approximately 950µs. This prevents the LTC3619 from having to quickly charge the output capacitor and thus supplying an excessive amount of instantaneous current.

OPERATION

When the output is loaded heavily, for example, with millifarad of capacitance, it may take longer than 950μs to charge the output to regulation. If the output is still low after the soft-start time, the LTC3619 will try to quickly charge the output capacitor. In this case, the input current limit (after it engages) can prevent excessive amount of instantaneous current that is required to quickly charge the output. See the Channel 2 Start-Up from Shutdown curve in the Typical Performance Characteristics section. After input current limit is engaged, the output slowly ramps up to regulation while limited by its 500mA of input current.

Short-Circuit Protection

When either regulator output is shorted to ground, the corresponding internal N-channel switch is forced on for a longer time period for each cycle in order to allow the inductor to discharge, thus preventing inductor current runaway. This technique has the effect of decreasing switching frequency. Once the short is removed, normal operation resumes and the regulator output will return to its nominal voltage.

Input Current Limit

Internal current sense circuitry in each channel measures the inductor current through the voltage drop across the power PFET switch and forces the same voltage across the small sense PFET. The voltage across the small sense PFET generates a current representing 1/55,000th of the inductor current during the on-cycle. The current out of RLIM pin is the summed representation of the inductor currents from both channels, which can be expressed in the following equation.

$$I_{RLIM} = I_{OUT1} \bullet D1 \bullet K1 + I_{OUT2} \bullet D2 \bullet K2,$$

where $D1 = V_{OUT1}/V_{IN}$ and $D2 = V_{OUT2}/V_{IN}$ are the duty cycle of channel 1 and 2, respectively.

K1 is the ratio $R_{DS(ON)}$ (power PFET)/$R_{DS(ON)}$(sense PFET) of channel 1, and K2 is the ratio $R_{DS(ON)}$(power PFET)/$R_{DS(ON)}$ (sense PFET) of channel 2. The ratio of the power PFET to the sense PFET is trimmed to within 2%.

Given that both PFETs are carefully laid out and matched, their temperature and voltage coefficient effects will be similar and their terms be canceled out in the equation. In that case, the constants K1 and K2 will only be dependent on area scaling, which is trimmed to within 2%. Thus, the I_{RLIM} current will track the input current very well over varying temperature and V_{IN}.

The RLIM pin can be grounded to disable input current limit function.

Programming Input Current Limit

Selection of one external R_{LIM} resistor will program the input current limit. The current limit can be programmed from 200mA up to I_{PEAK} current. As the input current increases, R_{LIM} voltage will follow. When R_{LIM} reaches the internal comparator threshold of 1V, channel 2's power PFET on-time will be shortened, thereby, limiting the input current.

Use the following equation to select the R_{LIM} resistance that corresponds to the input current limit.

$$R_{LIM} = 55k / I_{DC}$$

I_{DC} is the input current (at V_{IN}) to be limited. The following are some R_{LIM} values with the corresponding current limit.

R_{LIM}	I_{DC}
91.6k	600mA
110k	500mA
137.5k	400mA

Selection of C_LIM Capacitance

Since I_{RLIM} current is a function of the inductor current, its dependency on the duty cycle cannot be ignored. Thus, a C_{LIM} capacitor is needed to integrate the I_{RLIM} current and smooth out transient currents. The LTC3619 is stable with any size capacitance >100pF at the RLIM pin.

Each application input current limit will call for different C_{LIM} value to optimize its response time. Using a large C_{LIM} capacitor requires longer time for the RLIM pin voltage to charge. For example, consider the application 500mA input current limit, 5V input and 1A, 2.5V output with a 50% duty

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cycle. When an instantaneous 1A output pulse is applied, the current out of the RLIM pin becomes 1A/55k = 18.2µA during the 50% on-time or 9.1µA full duty cycle. With a C_{LIM} capacitor of 1µF, R_{LIM} of 116k, and using I = CdV/dt, it will take 110ms for C_{LIM} to charge from 0V to 1V. This is the time after which the LTC3619 will start input current limiting. Any current within this time must be considered in each application to determine if it is tolerable.

Figure 1a shows V_{IN} (I_{IN}) current below input current limit with a C_{LIM} capacitor of 0.1µF. Channel 1 is unloaded to simplify calculations. When the load pulse is applied, under the specified condition, I_{LIM} current is 1.1A/55k•0.66 = 13.2µA, where 0.66 is the duty cycle. It will take a little more than 7.5ms to charge the C_{LIM} capacitor from 0V to 1V, after which the LTC3619 begins to limit input current. The I_{IN} current is not limited during this 7.5ms time and is more than 725mA. This current transient may cause the input supply to temporarily droop if the supply current compliance is exceeded, but recovers after the input current limit engages. The output will continue to deliver the required current load while the output voltage droops to allow the input voltage to remain regulated during input current limit.

For applications with short load pulse duration, a smaller C_{LIM} capacitor may be the better choice as in the example

shown in Figure 1b. Channel 1 is unloaded for simplification. In this example, a 577µs, 0A to 2A output pulse is applied once every 4.7ms. A C_{LIM} capacitor of 2.2nF requires 92µs for V_{RLIM} to charge from 0 to 1V. During this 92µs, the input current limit is not yet engaged and the output must deliver the required current load. This may cause the input voltage to droop if the current compliance is exceeded. Depending on how long this time is, the V_{IN} supply decoupling capacitor can provide some of this current before V_{IN} droops too much. In applications with a bigger V_{IN} supply decoupling capacitor and where V_{IN} supply is allowed to droop closer to dropout, the C_{LIM} capacitor can be increased slightly. This will delay the start of input current limit and artificially regulated V_{OUT} before input current limit is engaged. In this case, within the 577µs load pulse, V_{OUT} voltage will stay artificially regulated for 92µs out of the total 577µs before the input current limit activates. This approach may be used if a faster recovery on the output is desired.

Selecting a very small C_{LIM} will speed up response time but it can put the device within threshold of interfering with normal operation and input current limit in every few switching cycles. This may be undesirable in terms of noise. Use 2πRC >> 100/clock frequency (2.25MHz) as a starting point, R being R_{LIM}, C being C_{LIM}.
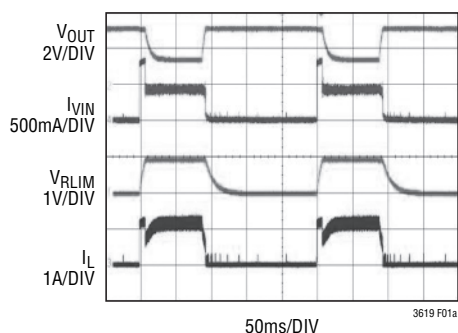
V_{IN} = 5V, 500mA COMPLIANT,
R_{LIM} = 116k, C_{LIM} = 0.1µF
I_{LOAD} = 0A TO 1.1A, C_{OUT} = 2.2mF, V_{OUT} = 3.3V
I_{LIM} = 475mA, CHANNEL 1 UNLOADED

Figure 1a. Input Current Limit Within 100ms Load Pulses
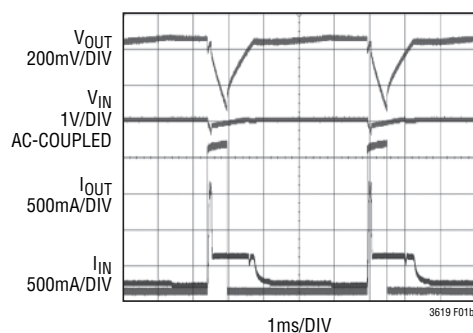
V_{IN} = 5V, 500mA COMPLIANT,
R_{LIM} = 116k, C_{LIM} = 2200pF
I_{LOAD} = 0A TO 2A, C_{OUT} = 2.2mF, V_{OUT} = 3.3V
I_{LIM} = 475mA, CHANNEL 1 NOT LOADED

Figure 1b. Input Current Limit Within 577µs, 2A Repeating Load Pulses

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A general LTC3619 application circuit is shown in Figure 2. External component selection is driven by the load requirement, and begins with the selection of the inductor L. Once the inductor is chosen, C_{IN} and C_{OUT} can be selected.

Inductor Selection

Although the inductor does not influence the operating frequency, the inductor value has a direct effect on ripple current. The inductor ripple current DI_L decreases with higher inductance and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_O \cdot L} \cdot \left(1 - \frac{V_{OUT}}{V_{IN}} \right) \quad (1)$$

Accepting larger values of DI_L allows the use of low inductances, but results in higher output voltage ripple, greater core losses, and lower output current capability. A reasonable starting point for setting ripple current is 40% of the maximum output load current. So, for a 800mA regulator, DI_L = 320mA (40% of 800mA).

The inductor value will also have an effect on Burst Mode operation. The transition to low current operation begins when the peak inductor current falls below a level set by the internal burst clamp. Lower inductor values result in higher ripple current which causes the transition to occur at lower load currents. This causes a dip in efficiency in the upper range of low current operation. Furthermore, lower inductance values will cause the bursts to occur with increased frequency.

Inductor Core Selection

Different core materials and shapes will change the size/current and price/current relationship of an inductor. Toroid or shielded pot cores in ferrite or permalloy materials are small and do not radiate much energy, but generally cost more than powdered iron core inductors with similar electrical characteristics. The choice of which style inductor to use often depends more on the price versus size requirements, and any radiated field/EMI requirements, than on what the LTC3619 requires to operate. Table 1 shows some typical surface mount inductors that work well in LTC3619 applications.

Input Capacitor (C_{IN}) Selection

In continuous mode, the input current of the converter is a square wave with a duty cycle of approximately V_{OUT}/V_{IN}. To prevent large voltage transients, a low equivalent series resistance (ESR) input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} \approx I_{MAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}}$$

Where the maximum average output current I_{MAX} equals the peak current minus half the peak-to-peak ripple current, $I_{MAX} = I_{LIM} - DI_L/2$. This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case is commonly used to design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours lifetime. This makes it advisable to further
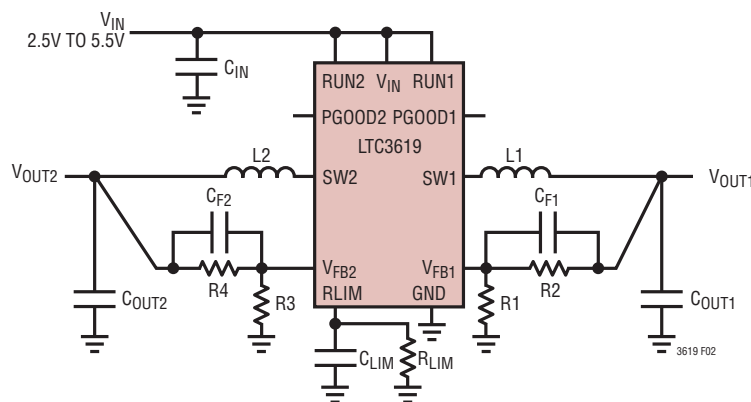

Figure 2. LTC3619 General Schematic

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Table 1. Representative Surface Mount Inductors

MANUFACTURER	PART NUMBER	VALUE	MAX DC CURRENT	DCR	HEIGHT
Coilcraft	LPS4012-152ML	1.5µH	2200mA	0.070Ω	1.2mm
	LPS4012-222ML	2.2µH	1750mA	0.100Ω	1.2mm
	LPS4012-332ML	3.3µH	1450mA	0.100Ω	1.2mm
	LPS4012-472ML	4.7µH	1450mA	0.170Ω	1.2mm
	LPS4018-222ML	2.2µH	2300mA	0.070Ω	1.8mm
	LPS4018-332ML	3.3µH	2000mA	0.080Ω	1.8mm
	LPS4018-472ML	4.7µH	1800mA	0.125Ω	1.8mm
FDK	FDKMIPF2520D	4.7µH	1100mA	0.11Ω	1mm
	FDKMIPF2520D	3.3µH	1200mA	0.1Ω	1mm
	FDKMIPF2520D	2.2µH	1300mA	0.08Ω	1mm
Murata	LQH32CN4R7M23	4.7µH	450mA	0.2Ω	2mm
Panasonic	ELT5KT4R7M	4.7µH	950mA	0.2Ω	1.2mm
Sumida	CDRH2D18/LD	4.7µH	630mA	0.086Ω	2mm
	CDH38D11SNP-3R3M	3.3µH	1560mA	0.115Ω	1.2mm
	CDH38D11SNP-2R2M	2.2µH	1900mA	0.082Ω	1.2mm
Taiyo Yuden	CB2016T2R2M	2.2µH	510mA	0.13Ω	1.6mm
	CB2012T2R2M	2.2µH	530mA	0.33Ω	1.25mm
	CB2016T3R3M	3.3µH	410mA	0.27Ω	1.6mm
	NR30102R2M	2.2µH	1100mA	0.1Ω	1mm
	NR30104R7M	4.7µH	750mA	0.19Ω	1mm
TDK	VLF3010AT4R7-MR70	4.7µH	700mA	0.28Ω	1mm
	VLF3010AT3R3-MR87	3.3µH	870mA	0.17Ω	1mm
	VLF3010AT2R2-M1R0	2.2µH	1000mA	0.12Ω	1mm
	VLF4012AT-2R2M1R5	2.2µH	1500mA	0.076Ω	1.2mm
	VLF5012ST-3R3M1R7	3.3µH	1700mA	0.095Ω	1.2mm
	VLF5014ST-2R2M2R3	2.2µH	2300mA	0.059Ω	1.4mm

derate the capacitor, or choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet the size or height requirements of the design. An additional 0.1µF to 1µF ceramic capacitor is also recommended on V_{IN} for high frequency decoupling when not using an all-ceramic capacitor solution.

Output Capacitor (C_{OUT}) Selection

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically, once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. The output ripple DV_{OUT} is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8f_0 C_{OUT}} \right)$$

where f_0 = operating frequency, C_{OUT} = output capacitance and DI_L = ripple current in the inductor. For a fixed output voltage, the output ripple is highest at maximum input voltage since DI_L increases with input voltage.

If tantalum capacitors are used, it is critical that the capacitors are surge tested for use in switching power supplies. An excellent choice is the AVX TPS series of surface mount tantalum. These are specially constructed and tested for low ESR so they give the lowest ESR for a given volume. Other capacitor types include Sanyo POSCAP, Kemet KO-CAP, and Sprague 593D and 595D series. Consult the manufacturer for other specific recommendations.

Using Ceramic Input and Output Capacitors

Higher values, lower cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications. Because the LTC3619 control loop does not depend on the output capacitor's ESR for stable operation, ceramic capacitors can be used freely to achieve very low output ripple and small circuit size.

However, care must be taken when ceramic capacitors are used at the input. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through

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long wires, a load step at the output can induce ringing at the input, V_{IN}. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at V_{IN}, large enough to damage the part. For more information, see Application Note 88.

When choosing the input and output ceramic capacitors, choose the X5R or X7R dielectric formulations. These dielectrics have the best temperature and voltage characteristics of all the ceramics for a given value and size.

Setting the Output Voltage

The LTC3619 regulates the V_{FB1} and V_{FB2} pins to 0.6V during regulation. Thus, the output voltage is set by a resistive divider, Figure 2, according to the following formula:

$$V_{OUT} = 0.6V\left(1 + \frac{R2}{R1}\right) \qquad (2)$$

Keeping the current small (<10μA) in these resistors maximizes efficiency, but making it too small may allow stray capacitance to cause noise problems or reduce the phase margin of the error amp loop.

To improve the frequency response of the main control loop, a feedback capacitor (C_F) may also be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor or the SW line.

Checking Transient Response

The regulator loop response can be checked by looking at the load transient response. Switching regulators take several cycles to respond to a step in load current. When a load step occurs, V_{OUT} immediately shifts by an amount equal to $DI_{LOAD} \cdot ESR$, where ESR is the effective series resistance of C_{OUT}. DI_{LOAD} also begins to charge or discharge C_{OUT} generating a feedback error signal used by the regulator to return V_{OUT} to its steady-state value. During this recovery time, V_{OUT} can be monitored for overshoot or ringing that would indicate a stability problem.

The initial output voltage step may not be within the bandwidth of the feedback loop, so the standard second order overshoot/DC ratio cannot be used to determine the phase margin. In addition, feedback capacitors (C_{F1} and

C_{F2}) can be added to improve the high frequency response, as shown in Figure 2. Capacitor C_F provides phase lead by creating a high frequency zero with R2 which improves the phase margin.

The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance. For a detailed explanation of optimizing the compensation components, including a review of control loop theory, refer to Application Note 76.

In some applications, a more severe transient can be caused by switching in loads with large (>1μF) input capacitors. The discharged input capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can deliver enough current to prevent this problem if the switch connecting the load has low resistance and is driven quickly. The solution is to limit the turn-on speed of the load switch driver. A Hot Swap™ controller is designed specifically for this purpose and usually incorporates current limiting, short-circuit protection, and soft-starting.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

% Efficiency = 100% − (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four sources usually account for the losses in LTC3619 circuits: 1) V_{IN} quiescent current, 2) switching losses, 3) I^2R losses, 4) other system losses.

1. The V_{IN} current is the DC supply current given in the Electrical Characteristics which excludes MOSFET driver and control currents. V_{IN} current results in a small (<0.1%) loss that increases with V_{IN}, even at no load.

2. The switching current is the sum of the MOSFET driver and control currents. The MOSFET driver current re-

APPLICATIONS INFORMATION

sults from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from V_{IN} to ground. The resulting dQ/dt is a current out of V_{IN} that is typically much larger than the DC bias current. In continuous mode, $I_{GATECHG} = f_O(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the internal top and bottom MOSFET switches. The gate charge losses are proportional to V_{IN} and thus their effects will be more pronounced at higher supply voltages.

3. I^2R losses are calculated from the DC resistances of the internal switches, R_{SW}, and external inductor, R_L. In continuous mode, the average output current flows through inductor L, but is "chopped" between the internal top and bottom switches. Thus, the series resistance looking into the SW pin is a function of both top and bottom MOSFET $R_{DS(ON)}$ and the duty cycle (DC) as follows:

$$R_{SW} = (R_{DS(ON)TOP}) \bullet (DC) + (R_{DS(ON)BOT}) \bullet (1 - DC)$$

The $R_{DS(ON)}$ for both the top and bottom MOSFETs can be obtained from the Typical Performance Characteristics curves. Thus, to obtain I^2R losses:

$$I^2R \text{ losses} = I_{OUT}^2 \bullet (R_{SW} + R_L)$$

4. Other "hidden" losses, such as copper trace and internal battery resistances, can account for additional efficiency degradations in portable systems. It is very important to include these "system" level losses in the design of a system. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. Other losses, including diode conduction losses during dead-time, and inductor core losses, generally account for less than 2% total additional loss.

Thermal Considerations

In a majority of applications, the LTC3619 does not dissipate much heat due to its high efficiency. In the unlikely event that the junction temperature somehow reaches approximately 150°C, both power switches will be turned off and the SW node will become high impedance. The goal of the following thermal analysis is to determine whether

the power dissipated causes enough temperature rise to exceed the maximum junction temperature (125°C) of the part. The temperature rise is given by:

$$T_{RISE} = P_D \bullet \theta_{JA}$$

where P_D is the power dissipated by the regulator and θ_{JA} is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, T_J, is given by:

$$T_J = T_{RISE} + T_{AMBIENT}$$

As a worst-case example, consider the case when the LTC3619 is in dropout on both channels at an input voltage of 2.7V with a load current of 400mA and 800mA and an ambient temperature of 70°C. From the Typical Performance Characteristics graph of Switch Resistance, the $R_{DS(ON)}$ of the switch is 0.58Ω and 0.33Ω. Therefore, power dissipated by each channel is:

$$P_{D1} = I_{OUT}^2 \bullet R_{DS(ON)} = 93mV$$
$$P_{D2} = I_{OUT}^2 \bullet R_{DS(ON)} = 212mV$$

Given that the thermal resistance of a properly soldered DFN package is approximately 40°C/W, the junction temperature of an LTC3619 device operating in a 70°C ambient temperature is approximately:

$$T_J = (0.305W \bullet 40°C/W) + 70°C = 82.2°C$$

which is well below the absolute maximum junction temperature of 125°C.

PC Board Layout Considerations

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the LTC3619. These items are also illustrated graphically in the layout diagrams of Figures 3a and 3b. Check the following in your layout:

1. Does the capacitor C_{IN} connect to the power V_{IN} (Pin 6) and GND (Pin 11) as closely as possible? This capacitor provides the AC current of the internal power MOSFETs and their drivers.

2. Are the respective C_{OUT} and L closely connected? The (–) plate of C_{OUT} returns current to GND and the (–) plate of C_{IN}.

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3. The resistor divider, R1 and R2, must be connected between the (+) plate of C_{OUT1} and a ground sense line terminated near GND (Pin 11). The feedback signals V_{FB1} and V_{FB2} should be routed away from noisy components and traces, such as the SW lines (Pins 5 and 7), and their trace length should be minimized.

4. Keep sensitive components away from the SW pins, if possible. The input capacitor C_{IN}, C_{LIM} and the resistors R1, R2, R3 and R4, R_{LIM} should be routed away from the SW traces and the inductors.

5. A ground plane is preferred, but if not available, keep the signal and power grounds segregated with small signal components returning to the GND pin at a single point. These ground traces should not share the high current path of C_{IN} or C_{OUT}.

6. Flood all unused areas on all layers with copper. Flooding with copper will reduce the temperature rise of power components. These copper areas should be connected to V_{IN} or GND.
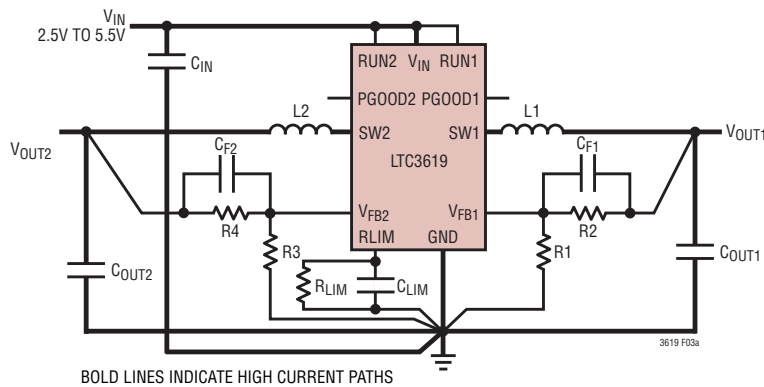

BOLD LINES INDICATE HIGH CURRENT PATHS

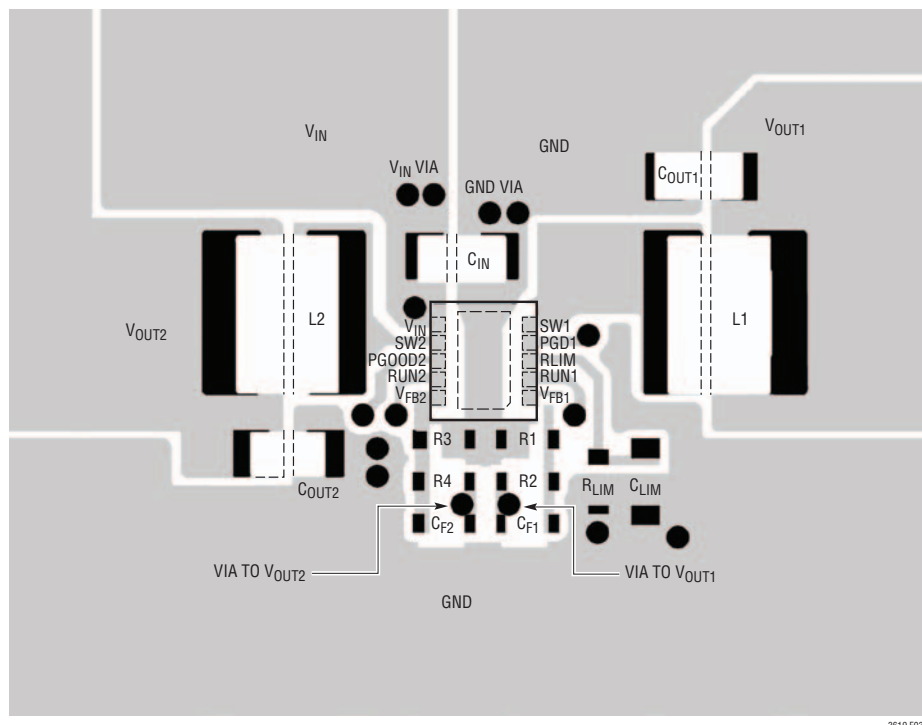**Figure 3a. LTC3619 Layout Diagram (See Board Layout Checklist)**

Figure 3b. LTC3619 Suggested Layout

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Design Example

As a design example, consider using the LTC3619 in a USB-GSM application, with $V_{IN} = 5V$, $I_{INMAX} = 500mA$, with the output of channel 2 charging a SuperCap of 4.4mF. The load on each channel requires a maximum of 400mA and 800mA in active mode and 2mA in standby mode. The output voltages are $V_{OUT1} = 1.8V$ and $V_{OUT2} = 3.4V$.

Start with channel 1. First, calculate the inductor value for about 40% ripple current (160mA in this example) at maximum V_{IN}. Using a derivation of Equation 1:

$$L1 = \frac{1.8V}{2.25MHz \cdot (160mA)} \cdot \left(1 - \frac{1.8V}{5V}\right) = 3.2\mu H$$

For the inductor, use the closest standard value of 3.3µH.

A 10µF ceramic capacitor should be more than sufficient for this output capacitor. As for the input capacitor, a typical value of $C_{IN} = 10\mu F$ should suffice, if the source impedance is very low.

The feedback resistors program the output voltage. To maintain high efficiency at light loads, the current in these resistors should be kept small. Choosing 10µA with the 0.6V feedback voltage makes R1~60k. A close standard 1% resistor is 59k. Using Equation 2.

$$R2 = \left(\frac{V_{OUT}}{0.6} - 1\right) \cdot R1 = 118k$$

An optional 22pF feedforward capacitor (C_{F1}) may be used to improve transient response.

Using the same analysis for channel 2 ($V_{OUT2} = 3.4V$), the results are:

L2 = 1.5µH

R3 = 59k

R4 = 276k

A feedforward capacitor is not used on channel 2 since the 4.4mF SuperCap will inhibit any fast output voltage transients.

Figure 4 shows the complete schematic for this example, along with the efficiency curve and transient response. Input current limit is set at 475mA average current, $R_{LIM} = 116k$, $C_{LIM} = 1000pF$. See Programming Input Current Limit for selecting R_{LIM} and Selection of C_{LIM} Capacitance for C_{LIM}.
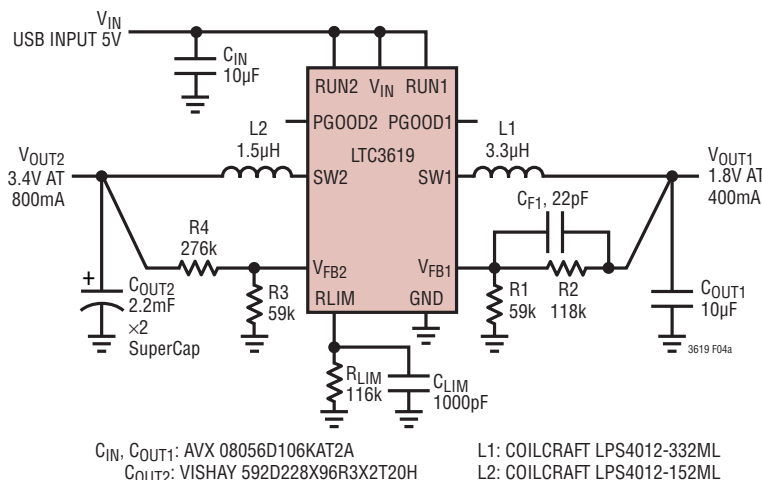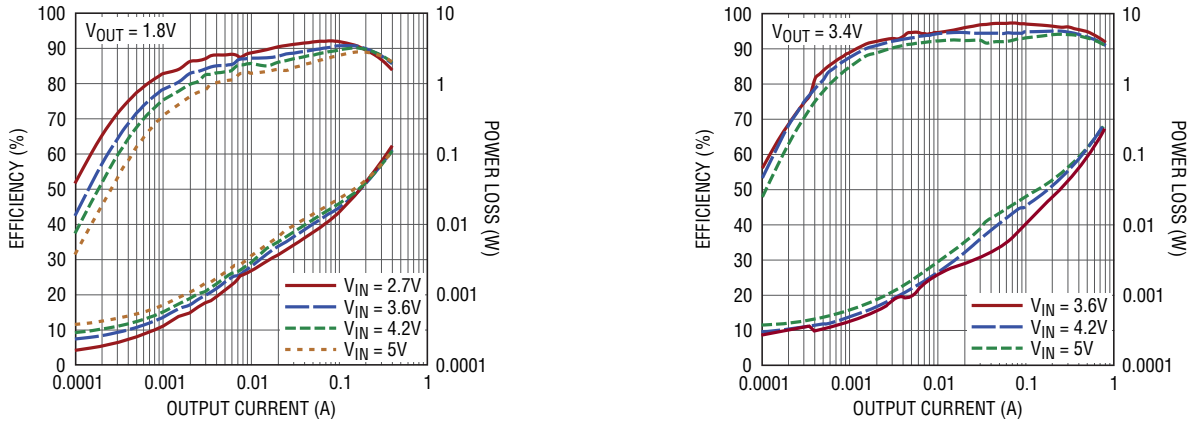
Figure 4a. Design Example Circuit

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Figure 4b. Efficiency and Power Loss vs Output Current
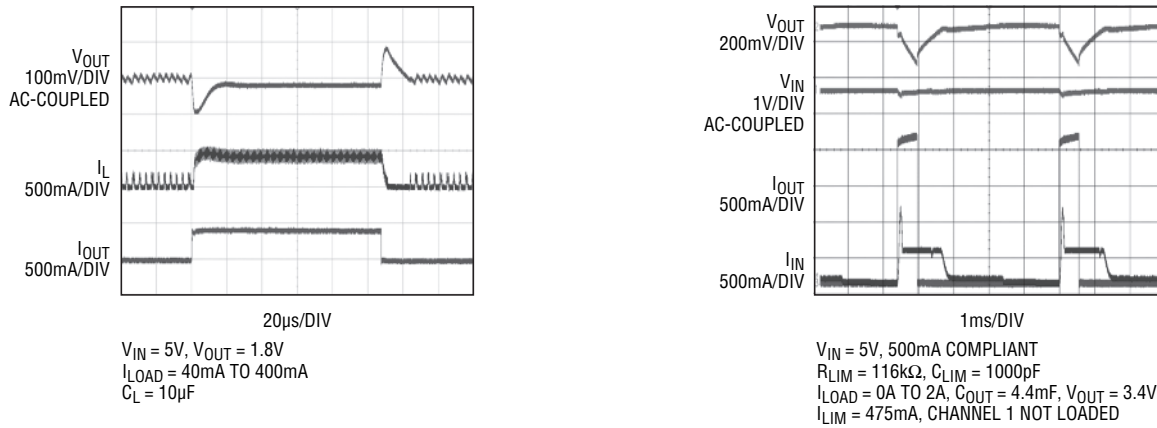
Figure 4c. Transient Response

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PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

DD Package
10-Lead Plastic DFN (3mm × 3mm)
(Reference LTC DWG # 05-08-1699 Rev C)

RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

3.55 ±0.05

1.65 ±0.05
2.15 ±0.05 (2 SIDES)

0.70 ±0.05

PACKAGE OUTLINE

0.25 ±0.05

0.50 BSC

2.38 ±0.05 (2 SIDES)

PIN 1 TOP MARK (SEE NOTE 6)

3.00 ±0.10 (4 SIDES)

0.200 REF

0.75 ±0.05

0.00 – 0.05

R = 0.125 TYP

0.40 ±0.10

6

10

1.65 ±0.10 (2 SIDES)

PIN 1 NOTCH R = 0.20 OR 0.35 × 45° CHAMFER

(DD) DFN REV C 0310

5

1

0.25 ±0.05

0.50 BSC

2.38 ±0.10 (2 SIDES)

BOTTOM VIEW—EXPOSED PAD

NOTE:
1. DRAWING TO BE MADE A JEDEC PACKAGE OUTLINE M0-229 VARIATION OF (WEED-2).
   CHECK THE LTC WEBSITE DATA SHEET FOR CURRENT STATUS OF VARIATION ASSIGNMENT
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE
   MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE
   TOP AND BOTTOM OF PACKAGE

PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

MSE Package
10-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1664 Rev H)

BOTTOM VIEW OF
EXPOSED PAD OPTION

1.88 ±0.102
(.074 ±.004)

0.889 ±0.127
(.035 ±.005)

5.23
(.206)
MIN

1.68 ±0.102
(.066 ±.004)

3.20 – 3.45
(.126 – .136)

0.305 ± 0.038
(.0120 ±.0015)
TYP

0.50
(.0197)
BSC

RECOMMENDED SOLDER PAD LAYOUT

1.88
(.074)

1.68
(.066)

DETAIL "B"

0.29
REF

0.05 REF
DETAIL "B"
CORNER TAIL IS PART OF
THE LEADFRAME FEATURE.
FOR REFERENCE ONLY
NO MEASUREMENT PURPOSE

3.00 ±0.102
(.118 ±.004)
(NOTE 3)

10 9 8 7 6

0.497 ±0.076
(.0196 ±.003)
REF

4.90 ±0.152
(.193 ±.006)

3.00 ±0.102
(.118 ±.004)
(NOTE 4)

1 2 3 4 5

DETAIL "A"

0.254
(.010)

GAUGE PLANE

0° – 6° TYP

0.53 ±0.152
(.021 ±.006)

DETAIL "A"

0.18
(.007)

SEATING
PLANE

1.10
(.043)
MAX

0.86
(.034)
REF

0.17 – 0.27
(.007 – .011)
TYP

0.50
(.0197)
BSC

0.1016 ±0.0508
(.004 ±.002)

MSOP (MSE) 0911 REV H

NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD
   SHALL NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

| REV	DATE	DESCRIPTION	PAGE NUMBER
A	10/12	Clarified Note 3 in Electrical Characteristics table	3
		Clarified Load Step on Typical Performance Characteristics curves	6
		Modified soft-start timing in Soft-Start section	9, 10
		Clarified device orientation on Suggested Layout	16

TYPICAL APPLICATION

Dual 400mA/800mA Buck Converter, I_{LIM} = 500mA
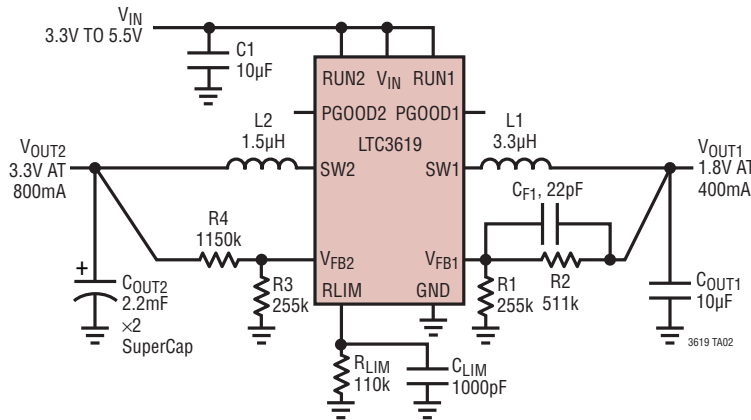
C1, C_{OUT1}: AVX 08056D106KAT2A
C_{OUT2}: VISHAY 592D228X96R3X2T20H

L1: COILCRAFT LPS4012-332ML
L2: COILCRAFT LPS4012-152ML

Dual 400mA/800mA Buck Converter, I_{LIM} = 475mA or Disabled
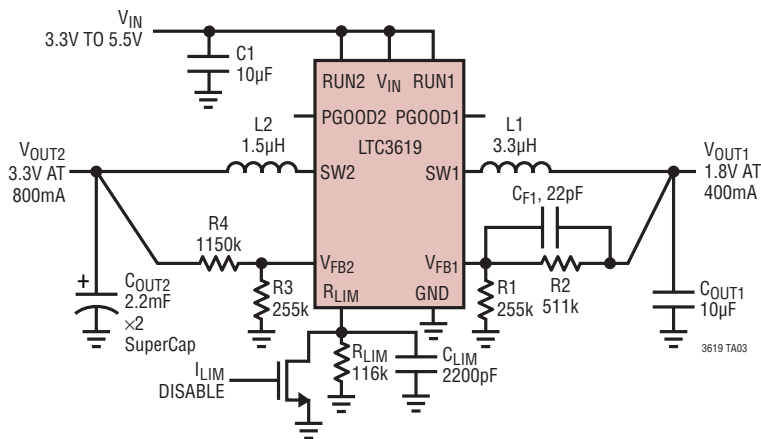
C1, C_{OUT1}: AVX 08056D106KAT2A
C_{OUT2}: VISHAY 592D228X96R3X2T20H

L1: COILCRAFT LPS4012-332ML
L2: COILCRAFT LPS4012-152ML

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3127	1.2A I_{OUT}, 1.6MHz, Synchronous Buck-Boost DC/DC Converter with Adjustable Input Current Limit	94% Efficiency, $V_{IN(MIN)}$ = 1.8V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 18μA, I_{SD} < 1μA, 3mm × 3mm DFN-MSOP10E
LTC3125	1.2A I_{OUT}, 1.6MHz, Synchronous Boost DC/DC Converter with Adjustable Input Current Limit	94% Efficiency, $V_{IN(MIN)}$ = 1.8V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MAX)}$ = 5.25V, I_Q = 15μA, I_{SD} < 1μA, 2mm × 3mm DFN-8
LTC3417A/ LTC3417A-2	Dual 1.5A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.3V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.8V, I_Q = 125μA, I_{SD} = <1μA, TSSOP-16E, 3mm × 5mm DFN-16
LTC3407A/ LTC3407A-2	Dual 600mA/600mA, 1.5MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40μA, I_{SD} = <1μA, MS10E, 3mm × 3mm DFN-10
LTC3548/LTC3548-1/ LTC3548-2	Dual 400mA and 800mA I_{OUT}, 2.25MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.5V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 40μA, I_{SD} = <1μA, MS10E, 3mm × 3mm DFN-10
LTC3546	Dual 3A/1A, 4MHz, Synchronous Step-Down DC/DC Converter	95% Efficiency, $V_{IN(MIN)}$ = 2.3V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MIN)}$ = 0.6V, I_Q = 160μA, I_{SD} = <1μA, 4mm × 5mm QFN-28
LTC3442	1.2A, I_{OUT}, 2MHz, Synchronous Buck-Boost DC/DC Converter with Input Current Limit	95% Efficiency, $V_{IN(MIN)}$ = 2.4V, $V_{IN(MAX)}$ = 5.5V, $V_{OUT(MAX)}$ = 2.4V to 5.25V, I_Q = 50μA, I_{SD} = <1μA, 3mm × 4mm DFN-12

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