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Active Clamp Forward Controller and Gate Driver

FEATURES

- **Supports Self-Starting Secondary-Side Control**
- **Direct Flux Limit™ Guarantees No Saturation**
- **Active Clamp Drive with Delay Adjustment**
- **On-Chip Bridge Rectifier Eliminates Need for Separate Gate Drive Bias Supply**
- **Wide Input Supply Range: 8V and Up (Limited Only by External Components)**
- **Linear Regulator Controller for Fast Start-Up**
- High Speed Gate Drivers
- Precision UVLO with Adjustable Hysteresis
- Overcurrent Protection
- Overtemperature Protection
- Adjustable Start-Up Frequency and Soft-Start
- Tiny 16-Lead MSOP Package

APPLICATIONS

- Isolated Battery Chargers
- Isolated 48V Telecommunication Systems
- Servers and Embedded Computing
- Automotive and Heavy Equipment

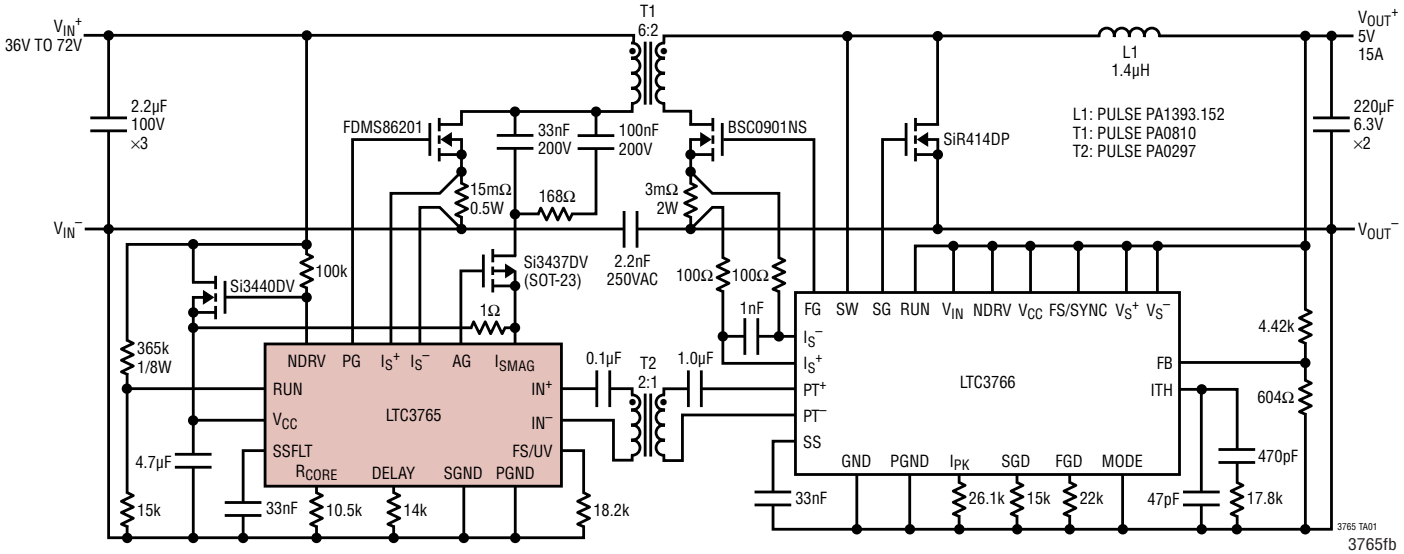
DESCRIPTION

The LTC®3765 is a start-up controller and gate driver for use in a self-starting secondary-side control forward converter. When combined with the LTC3766 secondary-side synchronous forward controller, a complete isolated power supply is created using a minimum of discrete parts. A proprietary scheme is used to multiplex gate drive signals and bias power across the isolation barrier through a small pulse transformer. The LTC3765 contains an on-chip bridge rectifier that extracts gate drive bias power from this pulse transformer, eliminating the need for a separate bias supply. A precision undervoltage lockout circuit and linear regulator controller ensure a quick and well-controlled start-up.

The LTC3765 includes an active clamp output for driving an external PMOS, as well as an adjustable delay to optimize efficiency. The active clamp architecture reduces voltage stress on the main power switch, and provides the highest possible efficiency. Overcurrent protection and the Direct Flux Limit guarantee no transformer saturation without compromising transient response.

TYPICAL APPLICATION

36V-72V to 5V/15A Active Clamp Isolated Forward Converter

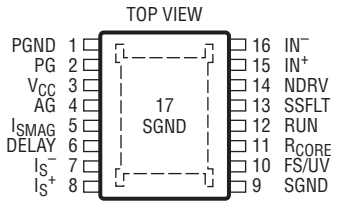


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{CC}, NDRV Voltages ..... –0.3V to 15V
(NDRV-V_{CC}) Voltage ..... –0.3V to 6V
IN^+, IN^-, SSFLT Voltages ..... –0.3V to 15V
I_{SMAG} Voltage ..... –5V to 18V
RUN Voltage ..... –0.3V to 12V
DELAY, R_{CORE}, FS/UV, I_S^+, I_S^- Voltages ..... –0.3V to 6V
Operating Junction Temperature Range (Notes 2, 3)
LTC3765E,LTC3765I ..... –40°C to 125°C
LTC3765H ..... –40°C to 150°C
LTC3765MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PIN CONFIGURATION



MSE PACKAGE
16-LEAD PLASTIC MSOP

T_{JMAX} = 150°C, θ_{JA} = 45°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 17) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3765EMSE#PBF	LTC3765EMSE#TRPBF	3765	16-Lead Plastic MSOP	–40°C to 125°C
LTC3765IMSE#PBF	LTC3765IMSE#TRPBF	3765	16-Lead Plastic MSOP	–40°C to 125°C
LTC3765HMSE#PBF	LTC3765HMSE#TRPBF	3765	16-Lead Plastic MSOP	–40°C to 150°C
LTC3765MPMSE#PBF	LTC3765MPMSE#TRPBF	3765	16-Lead Plastic MSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{CC} Supply							
V_{CCOP}	Operating Voltage Range			7.7		14.5	V
V_{CCUV}	V_{CC} Undervoltage Lockout	V_{CC} Rising V_{CC} Falling Hysteresis	● ●	7.1 6.7	7.4 7.0 400	7.7 7.3	V V mV
V_{CCLR}	Linear Regulator Output Voltage	(Note 4)		8.0	8.5	9.0	V
$t_{r(VCC)}$	Rise Time of V_{CC}				35		µs
I_{CP}	NDRV Charge Pump Output Current	V_{CC} = 5V, V_{NDRV} = 8V			35		µA
I_{CC}	DC Supply Current	V_{RUN} = 1.5V (Note 5)			1.7		mA
V_{RF}	Rectifier Total Forward Drop	I_{CC} = 25mA (Note 6)			1		V
Run Control/Undervoltage Lockout (RUN)							
V_{RUN}	RUN Pin Threshold	V_{RUN} Rising V_{RUN} Falling	● ●	1.22 1.17	1.25 1.20	1.28 1.23	V V
I_{HYST}	RUN Pin Hysteresis Current	V_{RUN} = 1V	●	4.0	5.0	6.0	µA
I_{RUN}	RUN Pin Leakage Current	V_{RUN} = 1.5V		–10	0	10	nA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{CC} = 12V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Drivers (PG, AG, DELAY)							
V_{OHPG}	PG High Output Voltage	I_{PG} = –100mA			11		V
I_{PUPG}	PG Peak Pull-Up Current				2.5		A
R_{PDPG}	PG Pull-Down Resistance	I_{PG} = 100mA			1.3		Ω
t_{rPG}	PG Rise Time	20% to 80%, C_{PG} = 4.7nF			20		ns
t_{fPG}	PG Fall Time	20% to 80%, C_{PG} = 4.7nF			20		ns
R_{PUAG}	AG Pull-Up Resistance	I_{AG} = –10mA			12		Ω
R_{PDAG}	AG Pull-Down Resistance	I_{AG} = 10mA			9		Ω
t_{DAG}	AG Turn-On Delay Time				180		ns
t_{DPG}	PG Turn-On Delay Time	R_{DELAY} = 0Ω R_{DELAY} = 10kΩ R_{DELAY} = 50kΩ		 120 390	40 140 460	 160 530	ns ns ns
Oscillator (FS/UV) and Soft-Start (SSFLT)							
f_{OSC}	Oscillator Frequency	R_{FS} = 75kΩ R_{FS} = 10kΩ			75 430		kHz kHz
DC_{MAX}	Oscillator Maximum Duty Cycle	V_{SSFLT} = 3.5V			70		%
V_{FSUVH}	FS/UV Output High	V_{RUN} = 1V			5		V
I_{FSUV}	FS/UV Pull-Up Current	V_{RUN} = 1V, $V_{FS/UV}$ = 1.5V			50		µA
$I_{SS(C)}$	Soft-Start Charge Current	V_{RUN} = 1.3V, V_{SSFLT} = 1V V_{RUN} ≥ 3.75V, V_{SSFLT} = 1V			–4 –1.6	 –0.5	µA µA
$I_{SS(D)}$	Soft-Start Discharge Current	Timing Out After Fault, V_{SSFLT} = 2V			1.25		µA
V_{FLTH}	Fault Output High	V_{CC} = 6.7V		5.75	6.5		V
V_{FLTD}	Fault Detection Voltage				5	5.5	V
Overcurrent (I_S^+, I_S^-) and Direct Flux Limit (I_{SMAG}, R_{CORE})							
V_{IS}	Overcurrent Threshold	$V_{ISTH} = V_{IS}^+ – V_{IS}^-$	●	130	150	170	mV
V_{ISMAG}^-	I_{SMAG} Limit Negative Threshold	Relative to SGND or V_{CC}		–1.15	–1	–0.85	V
V_{ISMAG}^+	I_{SMAG} Limit Positive Threshold	Relative to SGND or V_{CC}		0.85	1	1.15	V
M_{ISMAG}	I_{SMAG} Replicated Slope	R_{CORE} = 50kΩ, V_{RUN} = 1.25V R_{CORE} = 50kΩ, V_{RUN} = 6.25V R_{CORE} = 10kΩ, V_{RUN} = 1.25V R_{CORE} = 10kΩ, V_{RUN} = 6.25V			75 375 335 1700		mV/µs mV/µs mV/µs mV/µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3765 is tested under pulsed-load conditions such that $T_J \approx T_A$. The LTC3765E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3765I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3765H is guaranteed over the –40°C to 150°C operating junction temperature range and the LTC3765MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperature greater than 125°C. The junction temperature (T_J) is calculated from the ambient temperature (T_A) and power dissipation (P_D) according to the formula:

$$T_J = T_A + (P_D \bullet 45°C/W)$$

Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

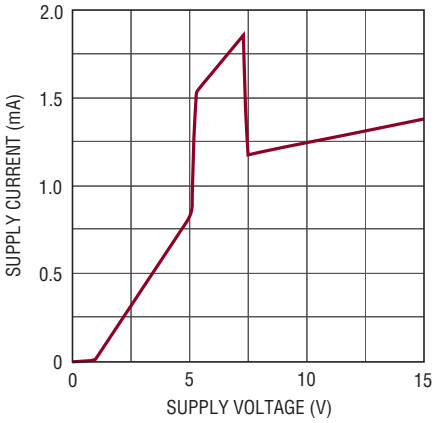
Note 4: The linear regulator output voltage is measured with a Vishay Siliconix Si3440DV N-channel MOSFET external pass device.

Note 5: I_{CC} is the sum of current into NDRV and V_{CC}.

Note 6: Rectifier forward voltage drop is the sum of the drop across the rectifier diode and synchronous switch.

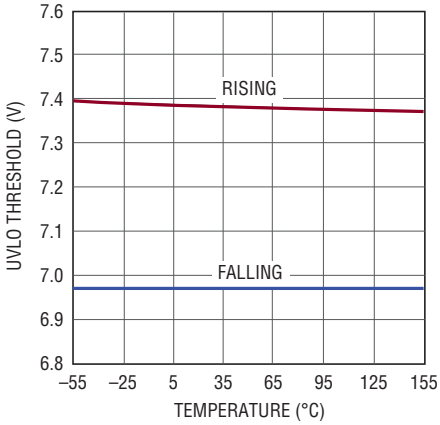
TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} Supply Current vs Supply Voltage



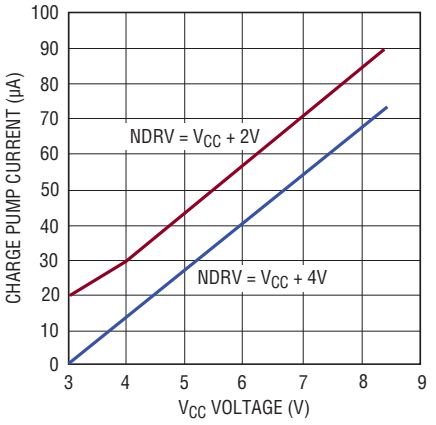
3765 G01

V_{CC} UVLO Thresholds vs Temperature



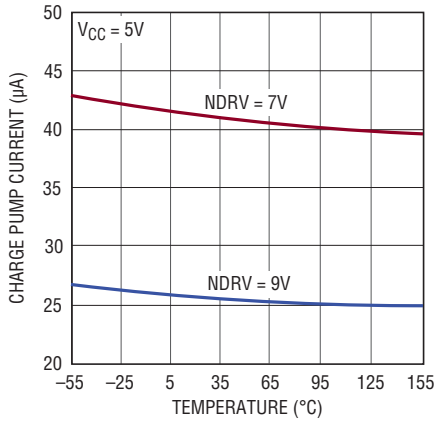
3765 G02

Charge Pump Output Current vs V_{CC} Supply Current



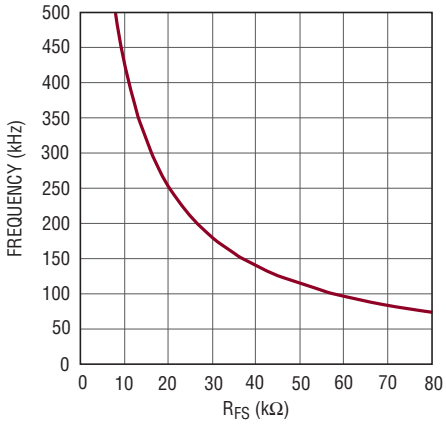
3765 G03

Charge Pump Output Current vs Temperature



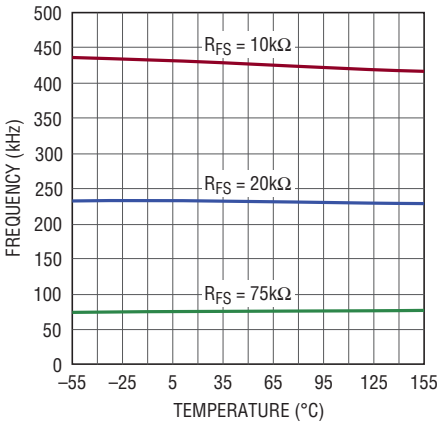
3765 G04

Start-Up Oscillator Frequency vs R_{FS} Resistor Value



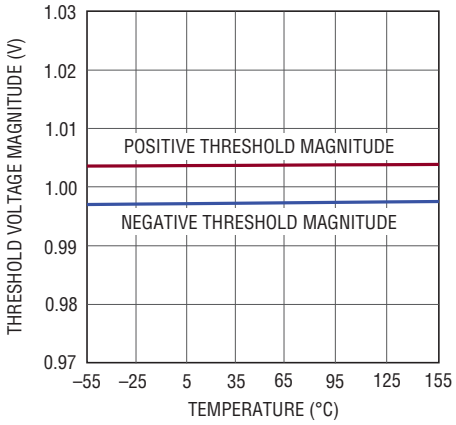
3765 G05

Start-Up Oscillator Frequency vs Temperature



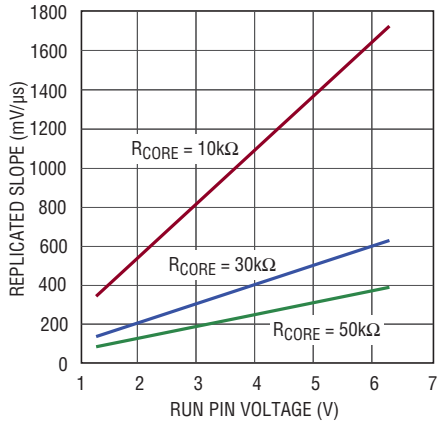
3765 G06

I_{SMAG} Thresholds vs Temperature



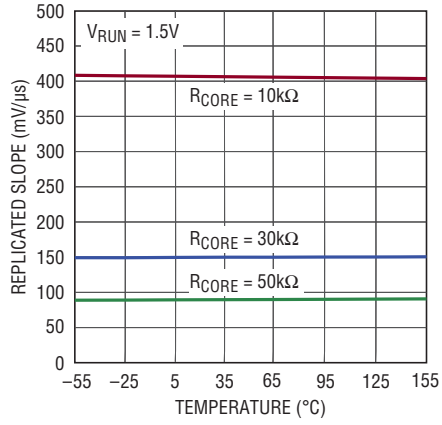
3765 G07

I_{SMAG} Replicated Slope vs RUN Pin Voltage and R_{CORE}



3765 G08

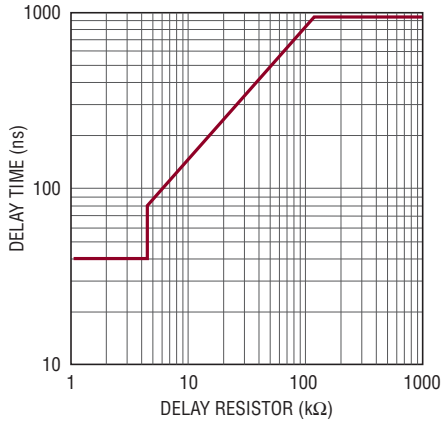
I_{SMAG} Replicated Slope vs Temperature



3765 G09

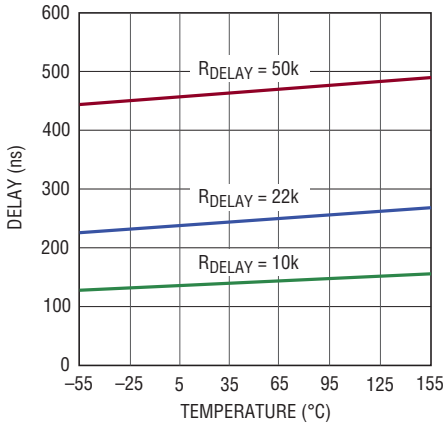
TYPICAL PERFORMANCE CHARACTERISTICS

PG Rising Delay Time vs DELAY Pin Resistor



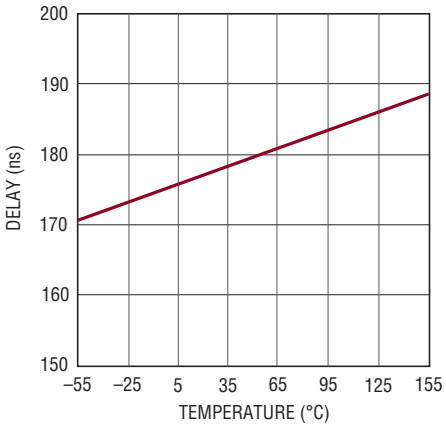
3765 G10

PG Rising Delay vs Temperature



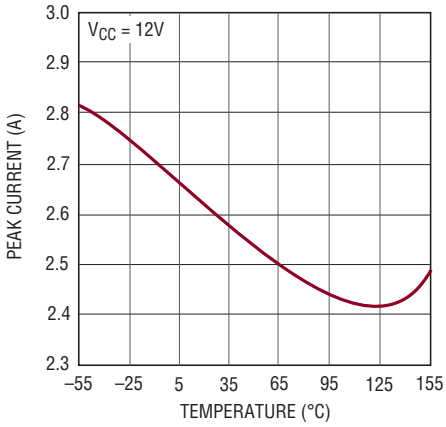
3764 G11

AG Falling Delay Time vs Temperature



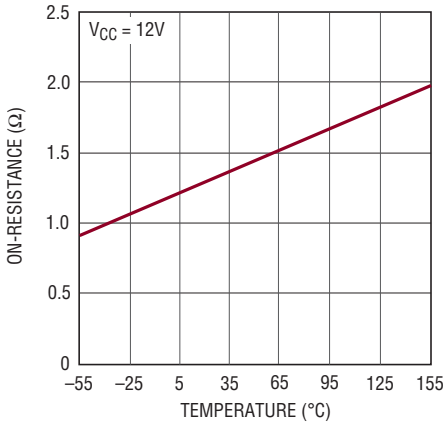
3765 G12

PG Peak Pull-Up Current vs Temperature



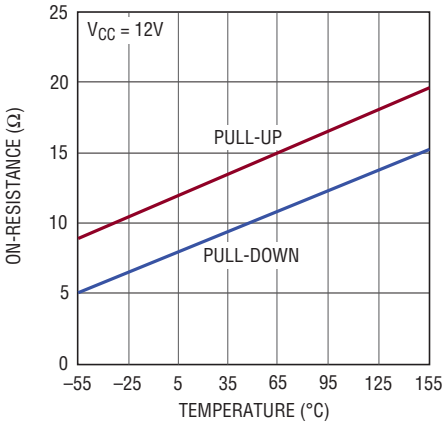
3765 G13

PG Pull-Down Resistance vs Temperature



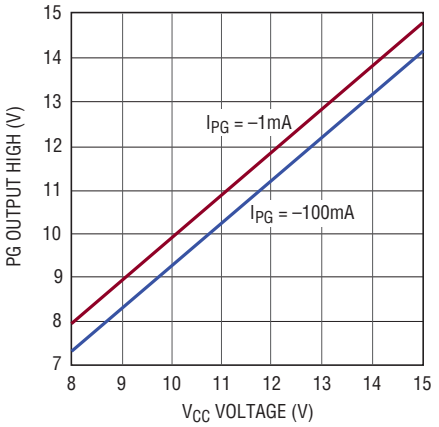
3765 G14

AG On-Resistance vs Temperature



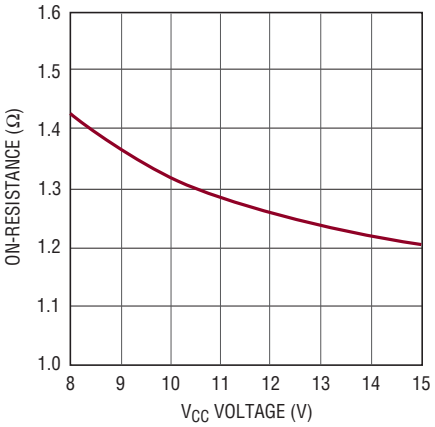
3765 G15

PG Output High Voltage vs V_{CC} Supply Voltage



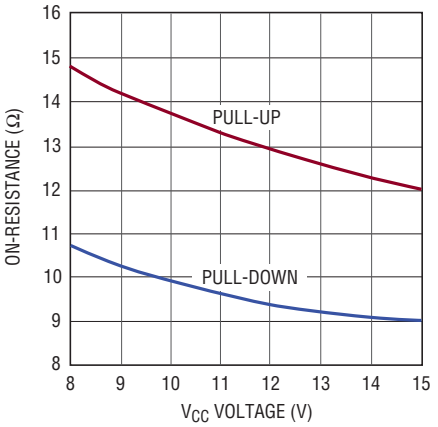
3765 G16

PG Pull-Down Resistance vs V_{CC} Supply Voltage



3765 G17

AG On-Resistance vs V_{CC} Supply Voltage



3765 G18

PIN FUNCTIONS

PGND (Pin 1): Power Ground. Ground return for the high current gate drivers.

PG (Pin 2): Primary Gate. Gate drive for the primary switch NMOS.

V_{CC} (Pin 3): Main Supply Pin. A ceramic bypass capacitor should be tied between this pin and ground.

AG (Pin 4): Active Gate. Gate drive for the active clamp PMOS. This drive output is "in phase" with the PG output. Connect to the gate of a PMOS through a capacitive level-shift circuit.

I_{SMAG} (Pin 5): Magnetizing Current Sense Pin. Connect to a current sense resistor in series with the source of the active clamp PMOS. This pin limits the magnetizing current of the main transformer to prevent core saturation when the active clamp is on.

DELAY (Pin 6): Primary Gate Rising Delay Adjustment. A resistor from this pin to ground sets the AG rising to PG rising dead time, which is critical for optimizing efficiency.

I_S^-, I_S^+ (Pin 7, Pin 8): Inputs to the Overcurrent Comparator. Connect across a current sense resistor in series with the source of the primary NMOS.

FS/UV (Pin 10): Oscillator Frequency Set and Undervoltage Indicator. A resistor to ground sets the switching frequency during start-up. When the RUN pin is low, the V_{CC} supply is undervoltage, or the overtemperature protection is active, a 50µA current source pulls this pin to the lesser of V_{CC} and 5V as an indicator.

R_{CORE} (Pin 11): Transformer Core Saturation Limit. A resistor from R_{CORE} to ground proportional to transformer core parameters internally replicates the magnetizing current slope when the primary NMOS is on. This slope in combination with the voltage on the I_{SMAG} and RUN pins limits the on-time of the NMOS to prevent saturation. See Applications Information.

RUN (Pin 12): Run Control and Undervoltage Lockout (UVLO). Connect to a resistor divider to monitor the input voltage V_{IN}, which is required for proper operation of the Direct Flux Limit. Converter operation is enabled for $V_{RUN} > 1.25V$. Hysteresis is a fixed 50mV with an additional 5µA hysteresis current that combines with the resistor divider to comprise the total UVLO hysteresis voltage.

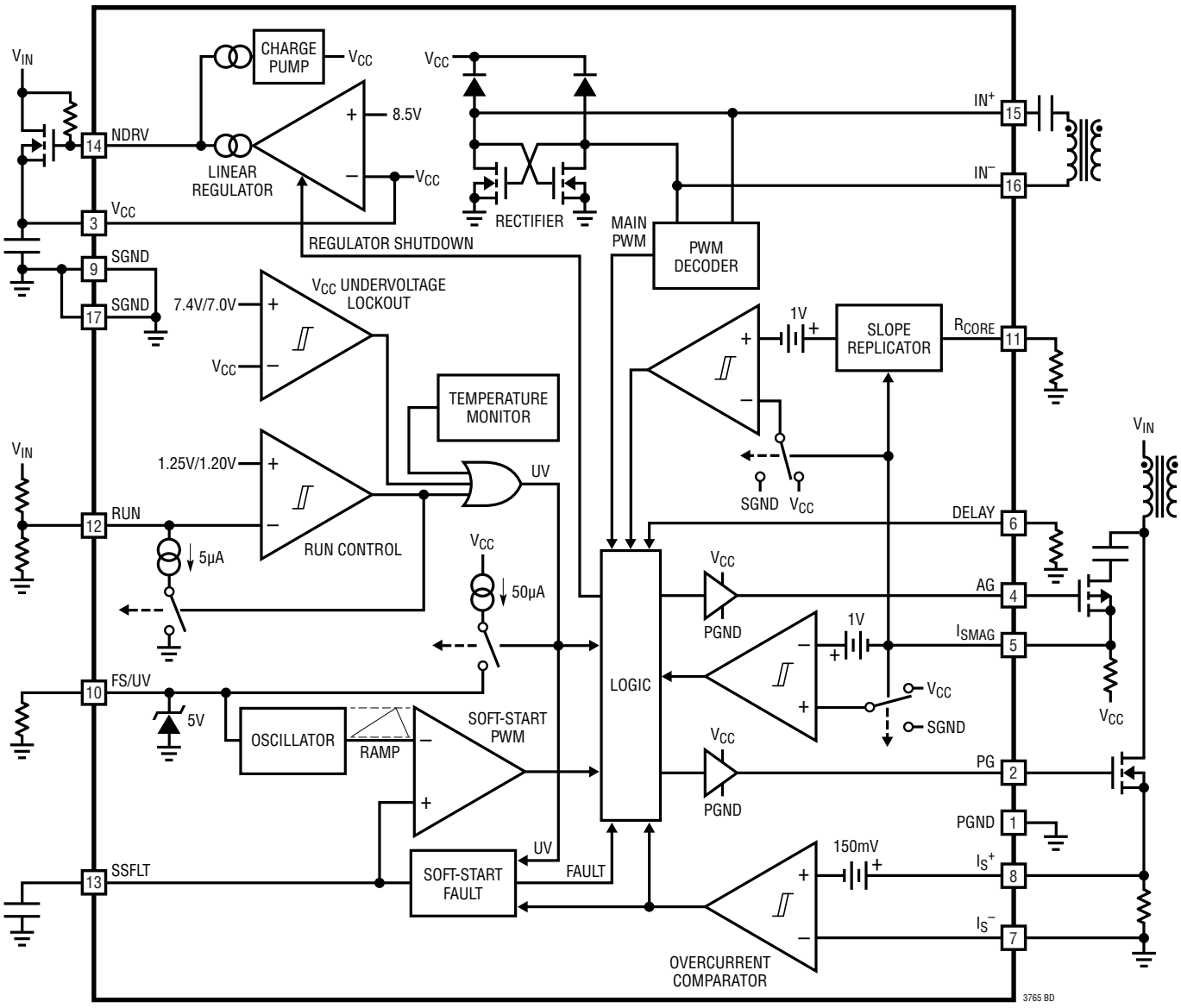
SSFLT (Pin 13): Combination Soft-Start and Fault Indicator. A capacitor to ground sets the duty cycle ramp-up rate during primary-side start-up. To indicate a fault, the SSFLT pin is momentarily pulled above 6V.

NDRV (Pin 14): Drive for External Linear Regulator. Connect to the gate of an NMOS and connect a pull-up resistor to the main input voltage, V_{IN}. An internal charge pump drives this pin above V_{IN} for low input voltage applications.

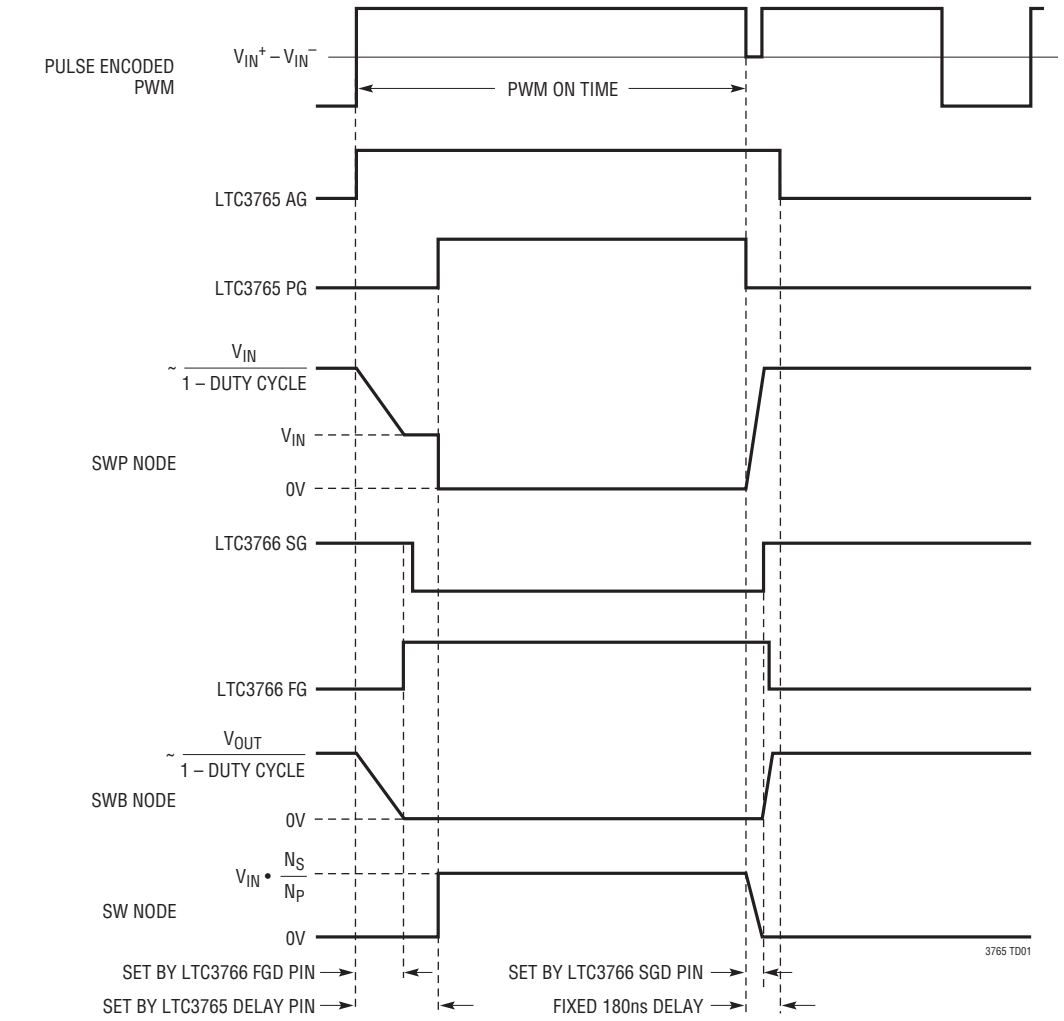
IN^+, IN^- (Pin 15, Pin 16): Inputs from Pulse Transformer. Connect through a DC restoring capacitor to the output winding of a pulse transformer. The input winding of the pulse transformer is driven by the LTC3766. After performing an initial open-loop start-up, the LTC3765 detects and decodes pulse encoded PWM information at these pins, and then turns control of the PG and AG switching over to the LTC3766 secondary-side controller. Additionally, an internal bridge rectifier on the IN^+/IN^- pins extracts DC power from the pulse transformer and delivers it to the V_{CC} pin.

SGND (Pin 9, Exposed Pad Pin 17): Signal Ground. The exposed pad metal of the package provides good thermal contact to the printed circuit board. It must be soldered to a ground plane for rated thermal performance.

BLOCK DIAGRAM



TIMING DIAGRAM



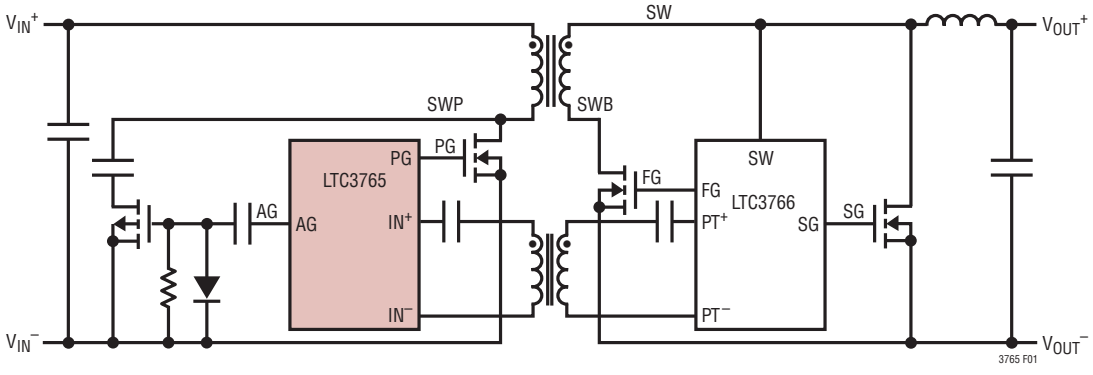


Figure 1. Reference Schematic for Timing Diagram

OPERATION

The LTC3765 is a forward converter start-up controller and gate driver for use in a single-switch forward converter with active clamp reset. When connected through a pulse transformer to the LTC3766 secondary-side synchronous forward controller, it forms a highly efficient forward converter with secondary-side regulation, galvanic isolation between input and output, and synchronous rectification. The LTC3765 and LTC3766 bias voltages are generated from a proprietary self-starting architecture which eliminates the need for an additional bias supply.

Linear Regulator

The LTC3765 features an external series pass linear regulator controller that eliminates the long start-up time associated with a conventional trickle charger. The NDRV pin regulates the gate of an external NMOS transistor to ramp up the V_{CC} supply with a well controlled 35µs ramp time to the 8.5V regulation point. For low input supply voltage applications where the threshold of the external NMOS transistor limits the V_{CC} voltage, an internal charge pump boosts NDRV to a voltage higher than V_{IN} so that the external NMOS can be fully enhanced.

Self-Starting Start-up

When power is first applied and when the RUN pin and V_{CC} have satisfied their respective start-up requirements, the LTC3765 begins open-loop operation using its own internal oscillator. Power is supplied to the secondary by switching the gate drivers with a gradually increasing duty cycle from 0% to 70% as controlled by the rate of rise of the voltage on the SSFLT pin. A peak charge circuit powered from an auxiliary winding off of the main transformer allows the LTC3766 to begin operation even for small duty cycles. When the LTC3766 has adequate voltage to satisfy its start-up requirements, it provides duty cycle information through the pulse transformer as shown in Figure 2. The LTC3765 detects this signal and transfers control of the gate drivers to the LTC3766. The LTC3765 turns off the linear regulator and, through an on-chip rectifier, also extracts power from this signal.

Gate Drive Encoding

The LTC3766 secondary-side forward controller sends a pulse-encoded signal through a small pulse transformer and series DC restore capacitor to the IN^+ and IN^- pins of the LTC3765. After a brief start-up sequence to establish a communication lock between the two parts, the LTC3765 extracts clock and duty cycle information from the signal and uses it to control the PG and AG gate driver outputs.

Figure 2 shows how the LTC3766 drives the pulse transformer in a complementary fashion, with a duty cycle of 79%. At the appropriate time during the positive cycle, the LTC3766 applies a short (150ns) zero voltage pulse across the pulse transformer, indicating the end of the PG "on" time.

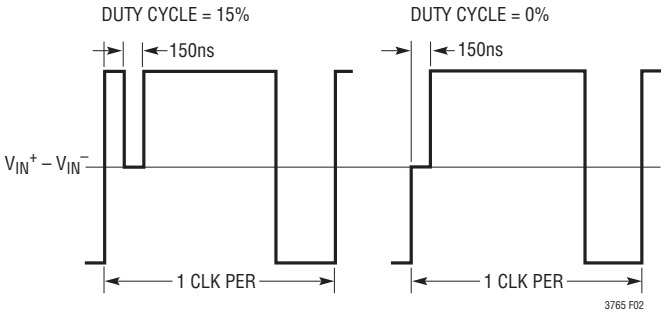


Figure 2. Gate Drive Multiplexing Scheme

Gate Drivers and Delay Adjustment

The active clamp gate driver (AG) and the primary switch gate driver (PG) are "in-phase," with a programmable overlap time set by the DELAY pin. In an active clamp forward converter topology, the delay time between the active clamp PMOS turn-off and the primary switch NMOS turn-on is critical for optimizing efficiency. When the active clamp is on, the drain of the primary NMOS, or primary switch node (SWP), is driven to a voltage of approximately $V_{IN}/(1 – \text{Duty Cycle})$ by the main transformer. When the active clamp turns off, the current in the magnetizing inductance of the transformer ramps this voltage linearly down to V_{IN}. Transitional power loss in the primary switch is minimized by turning it on when this voltage is at a minimum.

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The delay time between the primary switch turn-off and the active clamp turn-on is substantially less critical. Relative to the power loss due to turning on the primary switch, the power loss from switching the active clamp is significantly less. This difference results from both the lower current that the active clamp switches and the natural resonance of the system which facilitates zero voltage switching.

When the primary switch turns off, the main transformer leakage inductance is biased with the peak ripple current of the inductor reflected through the transformer. This current drives the voltage across the active clamp PMOS quickly to 0V. Turning on the PMOS after this transition results in minimal switching power loss. The LTC3765 active clamp turn on delay is internally fixed to 180ns.

V_{IN} Undervoltage Lockout

The RUN pin of the LTC3765 has precise thresholds and programmable hysteresis, which allows it to be used as an accurate voltage monitor on the input supply. An external resistive divider from V_{IN} to the RUN pin ensures that operation is disabled when V_{IN} is too low.

Additionally, when the RUN pin is below its threshold, a 5µA current is pulled by the pin. This current, combined with the external resistive divider, increases the hysteresis beyond the internal minimum of 4%.

Soft-Start

The SSFLT pin combines a programmable soft-start ramp for self-starting applications with a fault indicator. If either the V_{CC} or the RUN pin voltages are below their thresholds, the SSFLT pin is internally grounded. When both of these voltages rise above their thresholds, the SSFLT pin is released and current flows out of the pin into an external capacitor. As the capacitor charges from 1V to 3V, the duty cycle of the gate drivers increases linearly from 0% to 70%, with a switching frequency set by a resistor from FSUV to ground. The LTC3766 should begin sending pulses and take control of the duty cycle before the soft-start pin reaches 3V; however, if the voltage reaches 3.5V, the linear regulator turns off to avoid excessive power dissipation in the linear regulator pass device. With the linear regulator off, the supply will soon drop below the V_{CC} falling UVLO threshold, and the LTC3765 will fault and restart.

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. Although the active clamp technique provides a suitable reset voltage during steady-state operation, the sudden increase in duty cycle caused in response to a load step can cause the transformer flux to accumulate or "walk," potentially leading to saturation. This occurs because the reset voltage on the active clamp capacitor cannot keep up with the rapidly changing duty cycle. This effect is most pronounced at low input voltage, where the voltage loop demands a greater increase in duty cycle due to the lower voltage available to ramp up the current in the output inductor.

Traditionally, transformer core saturation has been avoided both by limiting the maximum duty cycle of the converter and by slowing down the loop to limit the rate at which the duty cycle changes. Limiting the maximum duty cycle helps the converter avoid saturation for a load step at low input voltage since the duty cycle maximum is clamped; however, transformer saturation can also easily occur at higher input voltage where the maximum duty cycle clamp is ineffective. Limiting the rate of duty cycle change in the loop to a point at which the active clamp capacitor can sufficiently track the change in duty cycle results in a very poor transient response of the overall converter. Furthermore, this technique is not guaranteed to prevent transformer saturation under all operating conditions. Neither of these traditional techniques will prevent the transformer from saturating when starting up into a pre-biased output, where the duty cycle can quickly change from 0% to 75%.

The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. During a reset cycle, when the active clamp PMOS is on, the magnetizing current is directly measured and limited through a sense resistor in series with the PMOS source. When the PMOS turns off and the main NMOS switch turns on, the LTC3765 generates an accurate internal estimate of the magnetizing current based on the sensed input voltage on the RUN pin and transformer core parameters customized to the particular

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core by a resistor from the R_{CORE} pin to ground. The magnetizing current is then limited during the on-time by this accurate internal approximation. Unlike previous methods, the Direct Flux Limit directly measures and monitors flux accumulation and guarantees that the transformer will not saturate, even when starting into a pre-biased output, without compromising transient response.

Additional Protection Features

The LTC3765 contains additional features to protect the circuit in the event of a persistent abnormal condition. Overcurrent and overtemperature monitors ensure reliable operation even in abnormal conditions.

The overcurrent monitor is implemented with an external sense resistor in series with the source of the primary NMOS. When the differential voltage between the current-sense pins, I_S^+ and I_S^-, exceeds 150mV, the primary NMOS is immediately turned off and a fault is initiated.

The internal overtemperature monitor is set at 165°C, with 20°C of hysteresis. This is helpful for limiting the temperature of the DC/DC converter in the event of a failure or abnormal condition. If the internal temperature exceeds this level, switching immediately stops and a fault is flagged.

Fault Indicator

A fault is initiated when any of the following conditions are encountered: overcurrent trip, overtemperature trip, communication loss with the LTC3766, V_{CC} falling below its UVLO threshold, or the RUN pin falling below its threshold. The SSFLT pin is used to indicate these faults, to communicate the fault in a polyphase system, and to optionally lockout on a fault.

When a fault occurs, switching stops immediately and the SSFLT pin is rapidly pulled up to above 5.75V as an indicator. The LTC3766 will detect that switching has stopped and will also fault and restart. As soon as the fault clears, the voltage on the SSFLT pin will slowly discharge to allow time for the LTC3766 to prepare for a restart. When the SSFLT voltage reaches 0.7V, the pin is momentarily grounded, and the soft-start sequence begins again. A fault can optionally be "locked out" by adding a 5.6V Zener diode from SSFLT to ground. This will inhibit the restart until the SSFLT pin is externally grounded, the diode clamp is removed, or the input supply collapses.

In a PolyPhase® application, the SSFLT pins of the LTC3765s should all be tied together. This not only ensures that all of the LTC3765 phases begin their open-loop start-up simultaneously, but also provides a means for communicating a fault condition. If one LTC3765 detects a fault, it pulls the combined SSFLT node to above 6V. When the voltage rises above 5V, the other LTC3765s detect this and stop switching until the common SSFLT pin has discharged.

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RUN Pin Resistor Selection

Normal operation is enabled when the voltage on the RUN pin rises above its 1.25V threshold. As shown in Figure 3, the RUN pin is typically used with an external resistive divider as an accurate undervoltage lockout (UVLO) on the V_{IN} supply. A 5µA current is pulled by the RUN pin when it is below its threshold that, when combined with the value chosen for R1, increases the UVLO hysteresis beyond the internal minimum of 4%. When used in this manner, the values for R1 and R2 can be calculated from the desired rising and falling UVLO thresholds by the following equations:

$$R1 = \frac{V_{IN(RISING)} - 1.042 \bullet V_{IN(FALLING)}}{5\mu A}$$

$$R2 = \frac{1.2 \bullet R1}{V_{IN(FALLING)} - 1.2}$$

A 1nF capacitor in parallel with R2 is recommended to filter out noise coupling from the high slew nodes to the RUN pin. Be aware that the absolute maximum voltage on the RUN pin is 12V. Therefore, the following relationship between the maximum V_{IN} voltage expected and the falling V_{IN} UVLO threshold must be satisfied:

$$V_{IN(MAX)} < 10 \bullet V_{IN(FALLING)}$$

Run/Stop control can also be implemented by connecting a small NMOS to the RUN pin as shown in Figure 3. Turning on the NMOS grounds the RUN pin and prevents the LTC3765 from running.

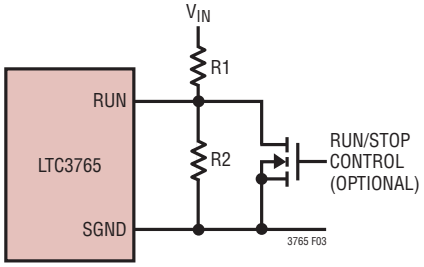

Figure 3. Resistive Voltage Divider for V_{IN} UVLO and Optional Run/Stop Control

The RUN pin is also used to sense the input voltage for the Direct Flux Limit. **A resistive divider from V_{IN} must be connected to the RUN pin for proper operation of the Direct Flux Limit.**

Linear Regulator

The linear regulator eliminates the long start-up times associated with a conventional trickle charger by using an external NMOS to quickly charge the capacitor connected to the V_{CC} pin. The typical configuration for the linear regulator is shown in Figure 4.

The NDRV pin sinks up to 1mA of current through R_{NDRV} to regulate the voltage on V_{CC}. The minimum value of R_{NDRV} can therefore be computed from:

$$R_{NDRV} > \frac{V_{IN(MAX)} - (8.5V + V_{TH})}{1mA}$$

where V_{TH} is the threshold voltage of the external NMOS.

The maximum value of the R_{NDRV} resistor is limited by the 10µA bias current pulled by NDRV that is required to power the internal linear regulator circuit. When the V_{CC} supply is above a minimum voltage that is a function of the MOSFET threshold, an internal charge pump provides all of the NDRV bias current; however, when V_{CC} is below this voltage, the charge pump is not active and the NDRV resistor must supply this current. Thus, a maximum value of R_{NDRV} for the charge pump start-up can be calculated as:

$$R_{NDRV} < \frac{V_{IN(MIN)} - 1.6V_{TH} - 1.2V}{20\mu A}$$

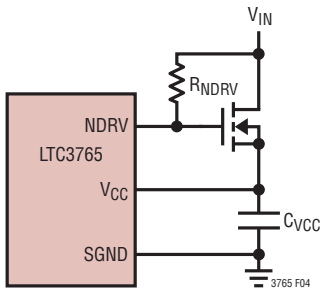

Figure 4. Typical Linear Regulator Configuration

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These two equations result in a wide range of values for R_{NDRV}. For many applications, a 100k resistor will satisfy these requirements.

The rate of charge of V_{CC} from 0V to 8.5V is controlled by the LTC3765 to be approximately 35µs regardless of the size of the capacitor connected to the V_{CC} pin. The charging current for this capacitor can be approximated as:

$$I_{C1} = \frac{8.5V}{35\mu s} C1$$

The external NMOS should be chosen so that the I_{C1} capacitor charging current in the equation above does not exceed the safe operating area (SOA) of the NMOS.

Excessive values of C1 are unnecessary and should be avoided. Typically values in the 1µF to 10µF range work well. A standard 3V threshold NMOS should be used when possible to better tolerate a high voltage start-up transient; however, a logic-level NMOS may be used for applications that require low voltage start-up. Since the NMOS is on continuously only during the brief start-up period, a small SOT-23 package can be used.

If an 8.5V to 14.5V supply is available in the system that can be used to power V_{CC}, the linear regulator is not needed and should be disabled by tying NDRV to V_{CC}. The external supply should be connected to the V_{CC} pin through a series diode if the LTC3766 is configured to overdrive V_{CC} when it begins switching.

Low Input Voltage Start-Up

The minimum value of R_{NDRV} is further constrained if low voltage (V_{IN} < 10V) start-up is required. In this application, the previous equation for the maximum value of R_{NDRV} must be satisfied to start the charge pump. Additionally, the charge pump current flows through R_{NDRV} to raise the NDRV voltage above V_{IN} so that the external MOSFET can be fully enhanced. R_{NDRV} therefore needs to be large enough that the limited charge pump current can raise the NDRV voltage to this level. Lower threshold logic-level MOSFETs are preferred for low voltage start-up not only because the MOSFET requires a lower NDRV voltage above V_{IN}, but also because the charge pump current increases as the NDRV-V_{CC} difference decreases, which is approximately the MOSFET threshold. For a given threshold voltage, R_{NDRV} should be chosen so that it meets the following relationship, keeping in mind that the previous equation for the maximum value of R_{NDRV} must also be met.

$$R_{NDRV} > \left(\frac{V_{TH(MAX)}}{5 - V_{TH(MAX)}} \right) \bullet 100k$$

In this equation, V_{TH} is the maximum threshold voltage of the external MOSFET. Table 1 below shows typical values of R_{NDRV} for common input voltage ranges.

Table 1. Typical R_{NDRV} Values

V_{IN} RANGE	$V_{TH(MAX)}$	R_{NDRV} RANGE	TYPICAL R_{NDRV}
8V to 36V	2V	70k to 180k	125k
36V to 72V	4V	60k to 1.4M	150k

Setting the Overcurrent Limit

The overcurrent limit for the LTC3765 is principally a safety feature to protect the converter. The current that flows in series through the transformer primary winding and the primary switch is sensed by a resistor (R_{SENSE}) connected between the source of the switch and ground. The voltage across this resistor is sensed by the I_S^+ and I_S^- pins. If the difference between I_S^+ and I_S^- exceeds 150mV, the LTC3765 immediately turns off the primary NMOS and, if SSFLT is not grounded, faults. The overcurrent comparator is blanked for approximately 200ns after PG goes high to avoid false trips due to noise.

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Choose the overcurrent trip current I_{TRIP} to be less than the maximum pulsed drain current rating of the primary NMOS but greater than the sum of the peak inductor current at full load and the current required to charge the output capacitor at start-up, reflected through the transformer. The sense resistor value, R_{SENSE}, can be calculated from the 150mV trip threshold and the primary-side trip current from the following equation:

$$R_{SENSE} = \frac{150mV}{I_{TRIP}}$$

The R_{SENSE} resistor should be verified to have sufficient margin over the maximum operating current of the converter, which typically occurs at start-up into a full load.

In a self-starting application at full load, the linearly increasing duty cycle determined by the soft-start capacitor (C_{SS}) ramps the output voltage with a fixed rate independent of the output capacitor value. Larger output capacitance requires a proportionally larger charging current to maintain the output voltage ramp rate. Since additional output capacitance is generally distributed through a system and may not be exactly known, the sense resistor and soft-start capacitor should be chosen with sufficient margin to ensure that the overcurrent comparator does not trip on start-up. An upper bound for the available current to charge the output capacitor can be calculated as shown in the following equation:

$$I_{CHG} < \frac{150mV}{R_{SENSE} \bullet N_S/N_P} - 1.4I_{LOAD(MAX)}$$

where N_S/N_P is the turns ratio of the transformer and the factor of 1.4 accounts for the typical 40% ripple current in the inductor. To ensure that the overcurrent comparator does not trip on start-up, the soft-start capacitor should be chosen so that only a fraction of the charging current calculated above is available to charge the output capacitor. Using 10% of the maximum charging current generally allows for sufficient margin. This establishes a lower bound on the soft-start capacitor value, which can be computed from:

$$C_{SS} > 600 \bullet 10^{-9} \bullet V_{IN(MAX)} \bullet N_S/N_P \left(\frac{C_{OUT}}{0.1 \bullet I_{CHG}} \right)$$

where C_{OUT} is the output capacitor value and $V_{IN(MAX)}$ is the maximum input voltage. The soft-start capacitor value should be in the range of 10nF to 1µF. Do not use a value less than 10nF. The soft-start capacitor also determines the relative timing of the output voltage rise and the LTC3766 bias supply rise. The value chosen should be verified with the equations in the following Self-Starting Start-Up section to ensure that the bias supply rises before the output voltage is close to the regulation point.

Care should be taken with the routing of the I_S^+ and I_S^- traces to avoid noise pickup. The traces should be Kelvin-sensed off of the sense resistor and routed right beside each other on an inner layer of the PCB. Avoid routing near high voltage, high slew rate nodes such as the drain of the primary NMOS and the drain of the active clamp PMOS.

Depending on PCB layout and the shielding of the traces going to the I_S^+ and I_S^- pins, it is sometimes necessary to add a small amount of filtering as shown in Figure 5. Typically, values of R_{FL} = 100Ω and C_{FL} = 200pF to 1nF will provide adequate filtering of noise pickup without significantly degrading the overcurrent response time.

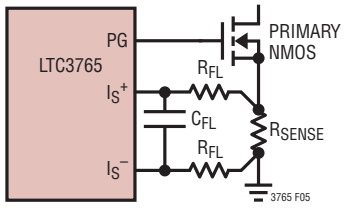

Figure 5. Overcurrent Sense Filtering

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Self-Starting Start-Up

When starting up, the LTC3765 begins switching in an open-loop fashion to supply power to the secondary side LTC3766. When the LTC3766 has adequate bias voltage and has met other conditions for start-up, it begins sending both duty cycle information and power through the pulse transformer connected to the IN^+/IN^- pins.

The LTC3765's start-up switching frequency is set by a resistor from FSUV to ground. Since the internal oscillator is only used in start-up, the frequency accuracy is not critical; however, avoid setting the frequency excessively low, as this will cause high currents in the transformer and inductor. To minimize the impact on the transition due to the duty cycle handoff from the LTC3765 to the LTC3766, this frequency should be set to the approximately the same frequency as the LTC3766. The frequency set resistor (R_{FS}) value can be selected using the following equation:

$$R_{FS} = \frac{6.2 \bullet 10^9}{f_{SW}} - 4.5k$$

Table 2 shows standard 5% resistor values of R_{FS} for common switching frequencies.

Table 2. Standard R_{FS} Resistor Values for Common Frequencies

FREQUENCY	R_{FS} VALUE
150kHz	36k
200kHz	27k
250kHz	20k
275kHz	18k
350kHz	13k

The internal oscillator generates a ramp that is compared with the voltage on the SSFLT pin to generate a duty cycle. The internal oscillator has an offset that prevents switching until SSFLT reaches approximately 1V. When V_{CC} is undervoltage or the RUN pin is below its threshold, the SSFLT pin is internally grounded and the drivers therefore do not switch.

When start-up conditions have been met, the SSFLT pin is released and a current is sourced out of the pin to charge an external capacitor connected from SSFLT to ground. Initially, a 60µA current is sourced out of the pin; however, this current is reduced to approximately 4µA when PG begins switching. The 60µA initial current reduces delay due to charging the external capacitor to 1V, where switching begins.

During the open-loop start-up, the output voltage rises much more quickly at high line than at low line for a given duty cycle ramp rate. This has the potential to overvoltage the output before the LTC3766 has begun switching, particularly at no load. To avoid this situation, the 4µA soft-start current is modulated by the RUN pin voltage, which monitors V_{IN} through a resistive divider. When the RUN pin voltage increases from 1.3V to 3.75V, the soft-start current decreases from 4µA to 1.6µA.

As the external soft-start capacitor gradually charges from 1V to 3V, the duty cycle increases linearly from 0% to 70%. For SSFLT voltages above 3V, the duty cycle is clamped at approximately 70% to allow for adequate active clamp reset time. When the SSFLT voltage reaches 3.5V, if duty cycle information has not been received at the IN^+ and IN^- pins, the voltage is held and the linear regulator is turned off. The PG and AG gate drivers will continue to switch at 70% duty cycle and the V_{CC} supply will decrease until it reaches its falling undervoltage lockout threshold. At that point, the LTC3765 will fault, turn on the linear regulator, and gradually reset the SSFLT capacitor for a restart attempt.

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In many applications, the LTC3766 supply is initially biased by this open-loop duty cycle ramp. The maximum duty cycle that the LTC3765 can provide therefore dictates whether the LTC3766 has adequate bias for start-up. The maximum duty cycle is typically 70%; however, the setting of the DELAY pin (t_{DPG}) decreases the maximum on-time. Therefore, the maximum duty cycle during start-up is 70%-($t_{DPG} \bullet f_{SW} \bullet 100\%$). Be sure to allow adequate margin between this maximum duty cycle and the duty cycle required to bias the LTC3766.

In some applications, the LTC3766 is biased from a peak charge circuit from an auxiliary winding of the main transformer. This configuration is shown in Figure 6. Since the LTC3765 open-loop start-up powers both the peak charge circuit and the output voltage, the primary design constraint on the soft-start capacitor value is to ensure that the output does not overvoltage before the LTC3766 has adequate bias to take control. A good rule of thumb is to select the soft-start capacitor so that the LTC3766 has adequate supply voltage before the output voltage has risen to half of its regulation point.

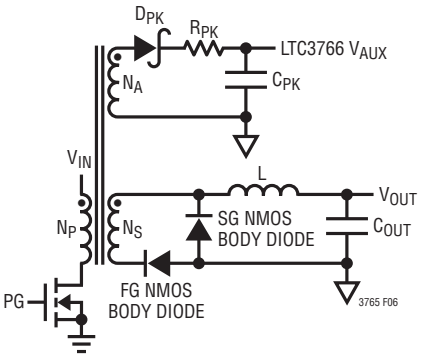

Figure 6. Peak Charge Circuit for Biasing the LTC3766 in a Self-Starting Application

For the peak charge circuit of Figure 6, choose the value of C_{PK} based on the capacitance required to bias the LTC3766. Then choose the auxiliary winding turns ratio N_A/N_P to give a peak charge voltage at minimum V_{IN} of approximately 30% more than the required V_{CC} of the LTC3766.

A lower bound on the primary-side soft-start capacitor (C_{SS}) value was previously calculated in the overcurrent section to ensure that the overcurrent comparator does not trip on start-up into a full load. The value should generally be in the range of 10nF to 1µF. Choosing too small of a value for C_{SS} could potentially charge the output voltage too quickly at no load or cause an overcurrent trip when starting into full load. Choosing too large a value will create additional delay in the start-up, during which time the linear regulator will be providing the current to switch the primary NMOS. Extremely long start-up times should be avoided to avoid excessive power dissipation in the linear regulator pass device. A value of 33nF is a good starting point for most applications.

The soft-start capacitor value should be verified by comparing the time for the peak charge circuit to deliver adequate bias to the LTC3766 to the time that the output voltage rises to half of its regulated value. The time until the LTC3766 receives bias and takes control can be approximated by:

$$t_{BIAS} \approx 10^3 \bullet \sqrt{R_{EQ} \bullet C_{PK} \bullet C_{SS}} + 150\mu s$$

where R_{EQ} is the sum of R_{PK} and the series resistance of diode D_{PK}.

The time for the output voltage to reach half of its regulated value can then be estimated by the following equation, where V_{OUT} is the final regulated output voltage:

$$t_{OUT} \approx 10^4 \bullet \left(\frac{C_{SS}^2 \left(V_{OUT}/2\right)^2 L \bullet C_{OUT} \bullet f_{SW}}{\left(V_{IN(MIN)} \bullet N_S/N_P\right)^2} \right)^{1/3}$$

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The above equation assumes that there is no load current, which is the worst-case condition for output voltage rise. If t_{OUT} is less than t_{BIAS}, then the soft-start capacitor value should be increased. Note that these equations are approximations and the actual times will vary somewhat with circuit parameters.

Gate Drivers

The active clamp gate driver (AG) and the primary switch gate driver (PG) are "in-phase," with a programmable overlap time set by the DELAY pin. Traditionally in active clamp drivers, the AG driver must be level-shifted as shown in the circuit in Figure 7a to drive the active clamp PMOS gate from approximately V_D to $–V_{CC} + V_D$, where V_D is the forward voltage drop across the Schottky diode D_{AG}. A silicon diode can be used instead of a Schottky barrier diode; however, the forward voltage of the diode does subtract from the available gate drive of the active clamp PMOS. This is particularly important at the minimum V_{CC} UVLO falling threshold.

The resistor, R_{AG}, ensures that the active clamp PMOS is off when not being driven. The active clamp level-shift circuit components can be chosen with few constraints. The time constant formed by R_{AG} and C_{AG} should be designed to be substantially longer than the switching period of the controller. A 0.1µF capacitor for C_{AG} and a 10k resistor for R_{AG} result in a 1ms time constant, which provides sufficient margin for the 75kHz to 500kHz frequency range available in the LTC3766.

Alternatively, the active clamp PMOS source can be returned to the V_{CC} supply bypass capacitor, as shown in Figure 7b. In this configuration, the level-shift circuit comprised of C_{AG}, D_{AG} and R_{AG} is not needed. The AG output drives the gate of the PMOS between V_{CC} and ground.

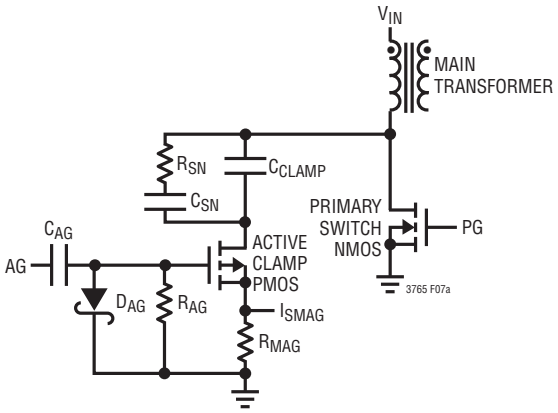

Figure 7a. Traditional AG and PG Driver Configuration

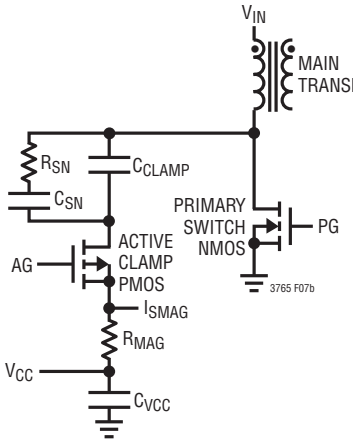

Figure 7b. Alternative AG and PG Driver Configuration

Unlike the configuration in Figure 7a, the main transformer leakage current spike and magnetizing current return to the V_{CC} bypass capacitor. The V_{CC} capacitor should be increased to prevent excessive ripple on the supply and a low impedance plane should be used to route V_{CC}. The

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ripple on the V_{CC} capacitor (C_{VCC}) due to the magnetizing current can be approximated by the following equation:

$$\Delta V_{CC} = \frac{V_{OUT}(N_P/N_S)}{6.8 \bullet C_{VCC} \bullet L_{MAG} \bullet f_{SW}^2}\left(1 - \frac{V_{OUT}(N_P/N_S)}{V_{IN(MAX)}}\right)$$

In general, a 4.7µF capacitor is a good choice for most application circuits when the active clamp current is returned to V_{CC}.

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. Although the active clamp technique provides a suitable reset voltage during steady-state operation, the sudden increase in duty cycle caused in response to a pre-bias output or a load step can cause the transformer flux to accumulate or "walk," potentially leading to saturation. This occurs because the reset voltage on the active clamp capacitor cannot keep up with the rapidly changing duty cycle. This effect is most pronounced at low input voltage, where the voltage loop demands a greater increase in duty cycle due to the lower voltage available to ramp up the current in the output inductor.

The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. During a reset cycle, when the active clamp PMOS is on, the magnetizing current is sensed by a resistor (R_{MAG}) connected to the source of the PMOS. The voltage across this resistor is sensed by the I_{SMAG} pin. Both the traditional and alternative configurations for the active clamp driver, shown previously in Figures 7a and 7b, are supported. In the traditional configuration, if the voltage on the I_{SMAG} pin is less than –1V, the active clamp PMOS is turned off. Similarly for the alternative configuration of Figure 7b, if the voltage on the I_{SMAG} pin is less than (V_{CC} – 1V), the active clamp PMOS is turned off. The I_{SMAG} pin therefore directly monitors and limits the magnetizing current to prevent core saturation in the negative direction.

Choose the magnetizing current sense resistor value to limit the transformer saturation current (I_{SAT}):

$$R_{MAG} = \frac{1V}{I_{SAT}}$$

where the saturation current is calculated from the maximum flux density (B_{MAX}), area of the core in cm^2 (A_C), number of turns on the primary (N_P), and typical magnetizing inductance ($L_{MAG(TYP)}$) from the following formula:

$$I_{SAT} = \frac{B_{MAX} \bullet A_C \bullet N_P}{10^8 \bullet L_{MAG(TYP)}}$$

For a transformer designed for 2000 gauss operating flux density, which is typical for a ferrite core, set B_{MAX} to 2700 gauss to keep sufficiently far from saturation over temperature. For the Pulse PA08xx series power transformers used in the Typical Applications section, $A_C = 0.59cm^2$. For the Pulse PA09xx series power transformers, $A_C = 0.81cm^2$.

Be sure to use the typical value for the magnetizing inductance in this formula. Using a minimum value for L_{MAG}, which is generally specified in transformer data sheets, artificially limits the flux swing. In general, multiplying the minimum value by 1.25 gives a good estimate for the typical value.

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When the NMOS is on, the magnetizing current and reflected inductor current are both flowing through the NMOS. The inductor current is generally much larger than the magnetizing current, which makes the magnetizing current difficult to measure directly. Therefore, when the NMOS is on the LTC3765 internally replicates the magnetizing current based on transformer core parameters, the voltage on the I_{SMAG} pin at the end of the previous reset cycle, and the sensed input voltage on the RUN pin. **The RUN pin must be connected to a resistive divider from V_{IN} to ground for proper operation of the Direct Flux Limit.**

At the end of the reset cycle, the voltage on the I_{SMAG} pin is sampled and held internally. This voltage is an accurate measurement of the magnetizing current. When the NMOS turns on, an internal ramp proportional to the RUN pin voltage divided by the R_{CORE} resistor increases the internal replicated magnetizing current. If this internal voltage exceeds 1V (or V_{CC} + 1V for the alternative AG configuration of Figure 7b), then the NMOS is turned off to prevent core saturation.

When the NMOS is turned off due to a Direct Flux Limit, the secondary-side switch node falls. The LTC3766 detects this prematurely falling switch node and turns off the forward gate to allow the transformer core to reset. This switch node behavior is indistinguishable from a primary-side shutdown; therefore, if the switch node falls prematurely for 19 consecutive cycles, the LTC3766 concludes that a primary-side shutdown has occurred and will fault.

Choose R_{CORE} based on the RUN pin divider network and the transformer core parameters:

$$R_{CORE} = \frac{R2}{R1+R2}\left(\frac{B_{MAX} \bullet A_C \bullet N_P}{0.030}\right) - 2k\Omega$$

where R1 and R2 comprise the divider network on the RUN pin, with R1 from V_{IN} to the RUN pin and R2 from the RUN pin to ground. B_{MAX} is typically 2700 gauss for a transformer designed to operate at 2000 gauss, A_C is the area of the core in cm^2, and N_P is the number of turns on the primary winding of the transformer.

The internal approximation of the magnetizing current is linear, which is accurate if the transformer flux density is kept sufficiently far from saturation. As the flux density approaches saturation, the magnetizing inductance of the transformer decreases and the magnetizing current increases rapidly. Depending on the particular core properties, it may be necessary to additionally decrease B_{MAX} in the equations above.

In a resonant reset application, the active clamp is replaced by a single reset capacitor. In this configuration, the transformer core is reset every cycle and is less likely to saturate; however, the transformer can still saturate during certain transient conditions. The Direct Flux Limit can also be configured to prevent core saturation in this application. Connect the R_{MAG} sense resistor in series with the ground side of the resonant reset capacitor and use the equation above for R_{CORE} to prevent saturation in a forward converter with resonant reset. The Direct Flux Limit may be disabled by tying I_{SMAG} to ground and floating the R_{CORE} pin; however, disabling the Direct Flux Limit leaves the application circuit open to transformer saturation and is not recommended.

Active Clamp Capacitor

The active clamp capacitor, C_{CLAMP}, stores the average reset voltage of the transformer over many cycles. The voltage on the clamp capacitor is generated by the transformer core reset current, and will intrinsically adjust to the optimal reset voltage regardless of other parameters. The voltage across the capacitor at full load is approximately given by:

$$V_{CL} = \frac{V_{IN}^2}{V_{IN} - 1.15\left(V_{OUT} \bullet N_P/N_S\right)}$$

N_P/N_S is the main transformer turns ratio. The factor of 1.15 accounts for typical losses and delays. When PG and AG are low, the bottom side of the clamp capacitor is grounded, placing the reset voltage V_{CL} on the SWP node in Figure 1. When PG and AG are high, the topside of the capacitor is grounded, and the voltage on the bottom side of the capacitor is $-V_{CL}$. Therefore the voltage seen on the

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capacitor is also the voltage seen at the drains of the PG and AG MOSFETs.

As shown in Figure 8, the V_{CL} voltage has a minimum when the converter is operating at 50%. For a given range on V_{IN}, therefore, the maximum clamp voltage ($V_{CL(MAX)}$) will occur either at the minimum or maximum V_{IN}, depending on which input voltage causes the converter to operate furthest from 50% duty cycle. The maximum V_{CL} voltage can be determined by substituting the maximum and minimum values of V_{IN} into this equation and selecting the larger of the two. In order to leave room for overshoot, choose a capacitor whose voltage rating is greater than this maximum V_{CL} voltage by 50% or more. Typically, a good quality (X7R) ceramic capacitor is a good choice for C_{CLAMP}. Also, be sure to account for the voltage coefficient of the capacitor. Many ceramic capacitors will lose as much as 50% of their value at their rated voltage.

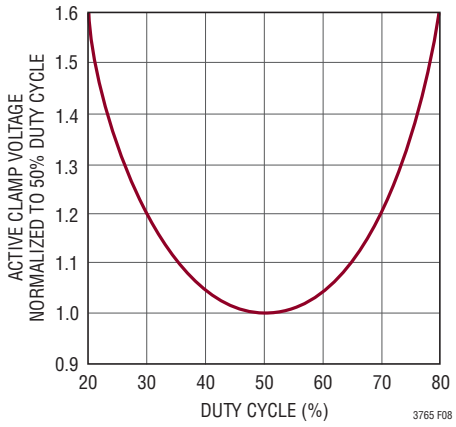

Figure 8. Active Clamp Capacitor Voltage vs Duty Cycle

In addition to voltage rating, another design constraint on C_{CLAMP} occurs because of the resonance between the magnetizing inductance of the main transformer with the clamp capacitor. The magnetizing inductance L_{MAG} and C_{CLAMP} form a high-Q resonant system that results in a sinusoidal ripple on the capacitor voltage. **To avoid the problems associated with this resonance, always use an RC snubber in parallel with the clamp capacitor as shown in Figures 7a and 7b.** Choose values for the clamp capacitor and the snubber components according to the following equations, where f_{SW} is the frequency set by the LTC3766 FS pin:

$$C_{CLAMP} = \frac{1}{2L_{MAG}} \bullet \left(\frac{4}{2 \bullet \pi \bullet f_{SW}} \right)^2$$

$$C_{SN} = 6C_{CLAMP}$$

$$R_{SN} = \frac{1}{1 - \left(\frac{V_{OUT}}{V_{IN(MIN)}} \bullet \frac{N_P}{N_S} \right)} \sqrt{\frac{L_{MAG}}{C_{CLAMP}}}$$

Be careful to account for the effect of voltage coefficient for both C_{SN} and C_{CLAMP} to ensure that the above relationship is maintained. In addition to dampening the resonance of the active clamp, the RC snubber also minimizes the peak voltage stress seen by the primary-side MOSFETs and reduces the effect of this LC resonance on the closed-loop transient response.

Setting the Gate Drive Delay

The active clamp gate driver (AG) and the primary switch gate driver (PG) switch "in-phase," with a programmable overlap time set by the DELAY pin. The PG falling to AG falling delay (t_{DAG}) is fixed at 180ns since the timing of this edge has little impact on efficiency. The AG rising to PG rising delay (t_{DPG}) is critical for optimizing efficiency and must be set in conjunction with the LTC3766 forward gate and synchronous gate delays. Refer to the LTC3766 data sheet for the procedure to determine the optimal delay times for a particular application. The primary gate delay time is set by a resistor from the DELAY pin to ground, according to the following equation:

$$R_{DELAY} = \left(t_{DPG} - 45ns \right) \bullet \frac{1k\Omega}{9.5ns}$$

In a system where the active clamp is not desired, for example in a forward converter using resonant reset, this delay can be set to a minimum by grounding the delay pin.

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Maximum Duty Cycle

During the delay time between AG rising and PG rising, power is not transferred from the input supply to the output supply. In most forward converter systems, the maximum on-time is artificially limited by the delay, which then drives a trade-off between the optimal delay time and the maximum achievable duty cycle. The LTC3765 and LTC3766 implement a unique system in which the PG and FG rising delays are reduced as the demanded duty cycle approaches maximum duty cycle. This allows for greater input voltage range variation over traditional forward converters.

Be cautious with component selection when designing with high duty cycles. Recall that the voltage on the drain of the primary switch is equal to $V_{IN}/(1-D)$, where D is the duty cycle. This voltage increases dramatically as the duty cycle approaches 100%. The LTC3766 limits the maximum duty cycle to 79% in order to reset the transformer core without excessive voltage stress on the primary switch.

Pulse Transformer

The pulse transformer that connects the LTC3766 PT^+/PT^- outputs to the LTC3765 IN^+/IN^- inputs functions as the communication link between the secondary-side controller and the primary-side gate driver, as shown in Figure 9.

Refer to the LTC3766 data sheet to determine the turns ratio and volt-second specifications for the pulse transformer. Keep in mind that the amplitude of the signals on the IN^+ and IN^- pins should be in the range of 4V to 15V to ensure proper operation.

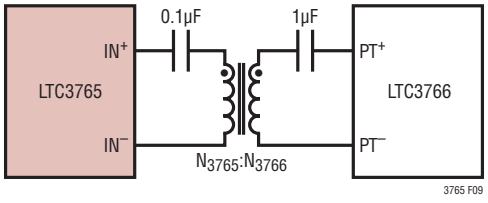


Figure 9. Pulse Transformer Connection

Furthermore, an additional constraint on the IN^+/IN^- voltage is present when V_{CC} bias is extracted from the signal. The internal rectifier drops approximately 1V between the IN^+ and IN^- pins and V_{CC}. Therefore, the signal on the IN^+ and IN^- pins should be at least 9V to keep the V_{CC} supply above its falling UVLO threshold.

The 1µF and 0.1µF capacitors in series with the pulse transformer of Figure 9 are for blocking and restoring the DC level of the signal. These values are appropriate for most LTC3765/LTC3766 applications.

Bypassing and Grounding

The LTC3765 requires proper bypassing on the V_{CC} supply due to its high speed switching (nanoseconds) and large AC currents (Amperes). Careless component placement and PCB trace routing may cause excessive ringing and undershoot/overshoot.

To obtain the optimal performance from the LTC3765:

A. Use a low inductance, low impedance ground plane to reduce any ground drop and stray capacitance. Remember that the LTC3765 switches greater than 2A peak currents and any significant ground drop will degrade signal integrity.

B. Mount a bypass capacitor as close as possible between the V_{CC} pin and ground plane.

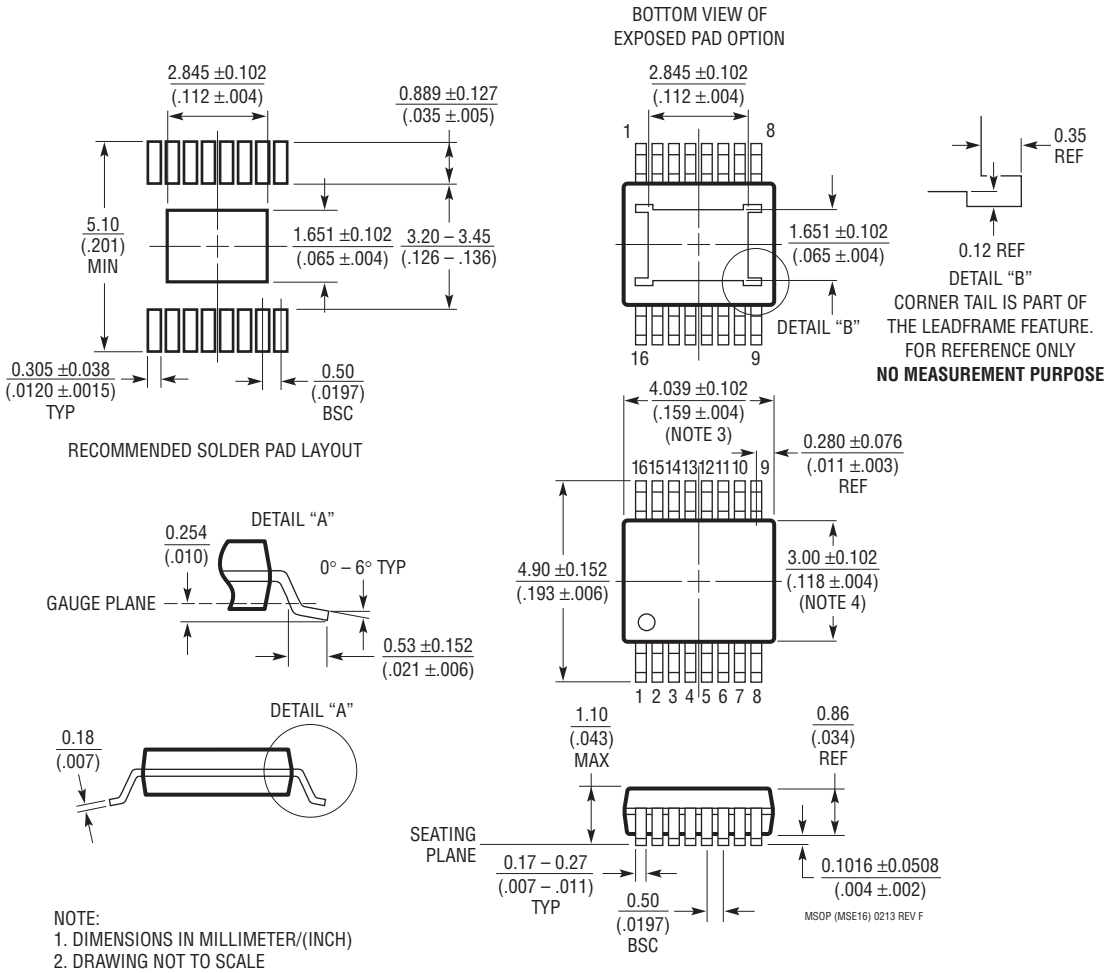
C. Plan the power/ground routing carefully. Know where the large load switching current is coming from and going to. Maintain separate ground return paths for the signal pins and the output power stage.

D. Keep the copper traces between the driver output pins and the load short and wide.

E. Solder the exposed pad on the back side of the LTC3765 package to the ground plane. The exposed pad is internally electrically connected to the SGND pin; however, rated thermal performance will only be achieved if the exposed pad is soldered to a low impedance ground plane.

PACKAGE DESCRIPTION

MSE Package
16-Lead Plastic MSOP, Exposed Die Pad
(Reference LTC DWG # 05-08-1667 Rev F)



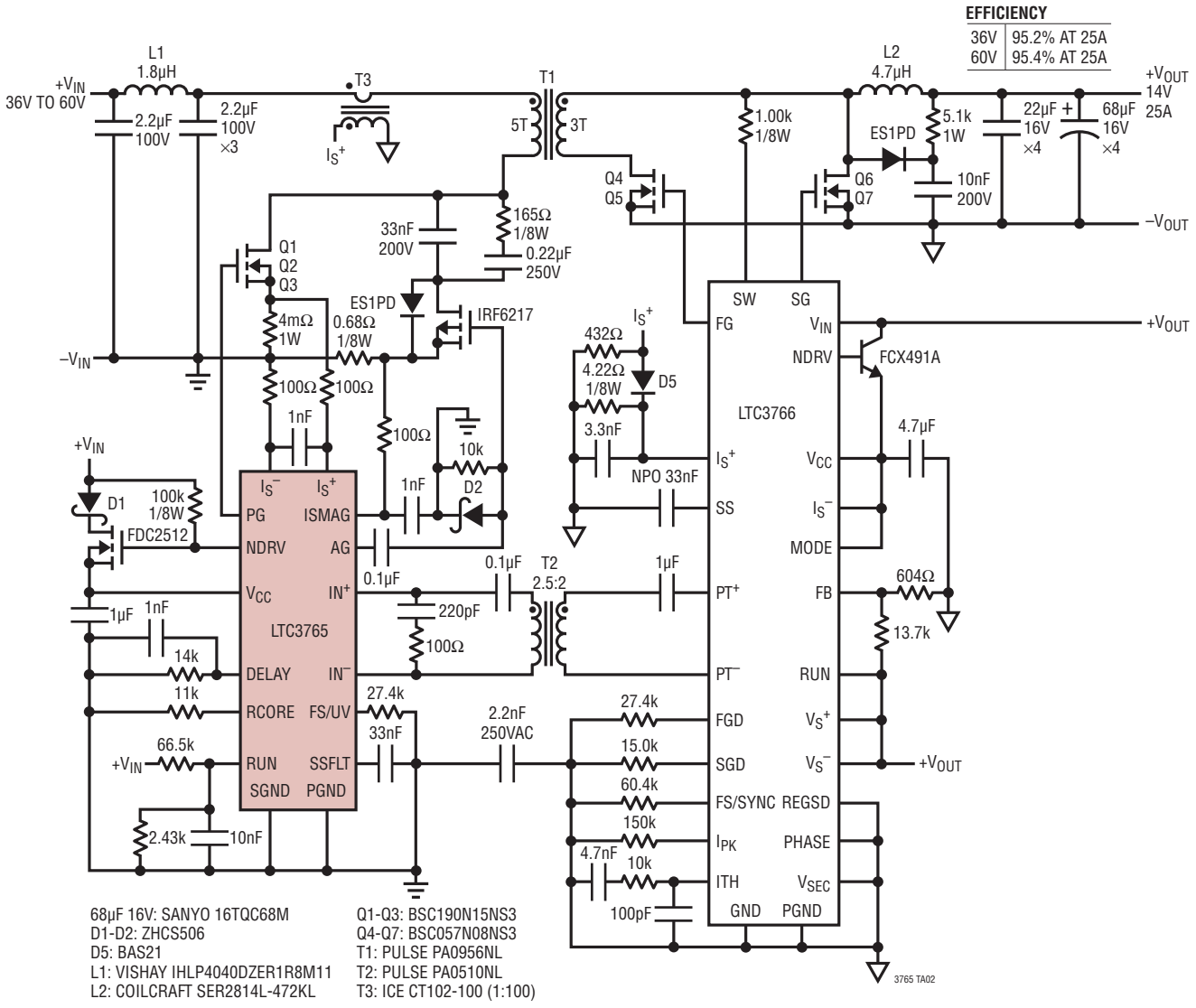
NOTE:
1. DIMENSIONS IN MILLIMETER/(INCH)
2. DRAWING NOT TO SCALE
3. DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
   MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
4. DIMENSION DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
   INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.152mm (.006") PER SIDE
5. LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.102mm (.004") MAX
6. EXPOSED PAD DIMENSION DOES INCLUDE MOLD FLASH. MOLD FLASH ON E-PAD SHALL
   NOT EXCEED 0.254mm (.010") PER SIDE.

REVISION HISTORY

REV	DATE	DESCRIPTION	PAGE NUMBER
A	1/12	Removed ThinSOT and No R_{SENSE} from disclaimer.	1
		Changed Fault Output High condition to V_{CC} = 6.7V (V_{CC} UVLO Min Falling).	3
		Updated PG Rising Delay Typical Performance graphs.	5
		Changed 6V to 5.75V to match Electrical Characteristics table.	11
		Added text to explain open-loop start-up maximum duty cycle	16
		Added text to clarify what value of magnetizing inductance to use in the Direct Flux Limit equations.	18
		Added text to show the drop of the internal rectifier from IN^+/IN^- to V_{CC} for when V_{CC} is biased by the LTC3766.	21
		16-lead MSE package updated.	22
B	11/13	Changed $I_{SS(C)}$ Condition from "=" to "≥".	3
		Added Max limit to –0.5µA	3

TYPICAL APPLICATION

36V-60V to 14V at 25A Isolated 350W Bus Converter



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC3766	Secondary Side Synchronous Forward Controller	Direct Flux Limit, Multiphase Capable, Works in Conjunction with LTC3765
LTC3705/LTC3726	Isolated Synchronous No Opto 2-Switch Forward Controller Chip Set	Suitable for Medium Power 24V and 48V Input Applications
LT1952/LT1952-1	Isolated Synchronous Forward Controllers	Suitable for Medium Power 24V and 48V Input Applications
LTC3723-1/LTC3723-2	Synchronous Push-Pull and Full-Bridge Controllers	High Efficiency with On-Chip MOSFET Drivers
LTC3721-1	Nonsynchronous Push-Pull and Full-Bridge Controllers	Minimizes External Components, On-Chip MOSFET Drivers
LTC3722/LTC2722-2	Synchronous Isolated Full Bridge Controllers	Suitable for High Power 24V and 48V Input Applications

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