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High Efficiency, Secondary-Side Synchronous Forward Controller

FEATURES

- **Direct Flux Limit™ Guarantees No Saturation**
- **Fast and Accurate Average Current Limit**
- **Clean Start-Up Into Pre-Biased Output**
- **Secondary-Side Control for Fast Transient Response**
- **Simple, Self-Starting Architecture**
- **Synchronous MOSFET Reverse Current Limit**
- **PolyPhase® Operation Eases High-Power Design**
- True Remote Sense Differential Amplifier
- Remote Sense Reverse Protection
- High Voltage Linear Regulator Controller
- Internal LDO Powers Gate Drive from V_{OUT}
- Overtemperature/Overvoltage Protection
- Low Profile 4mm × 5mm QFN and Narrow 28-Lead SSOP Packages

APPLICATIONS

- Isolated 48V Telecommunication Systems
- Isolated Battery Chargers
- Automotive and Military Systems
- Industrial, Avionics and Heavy Equipment

DESCRIPTION

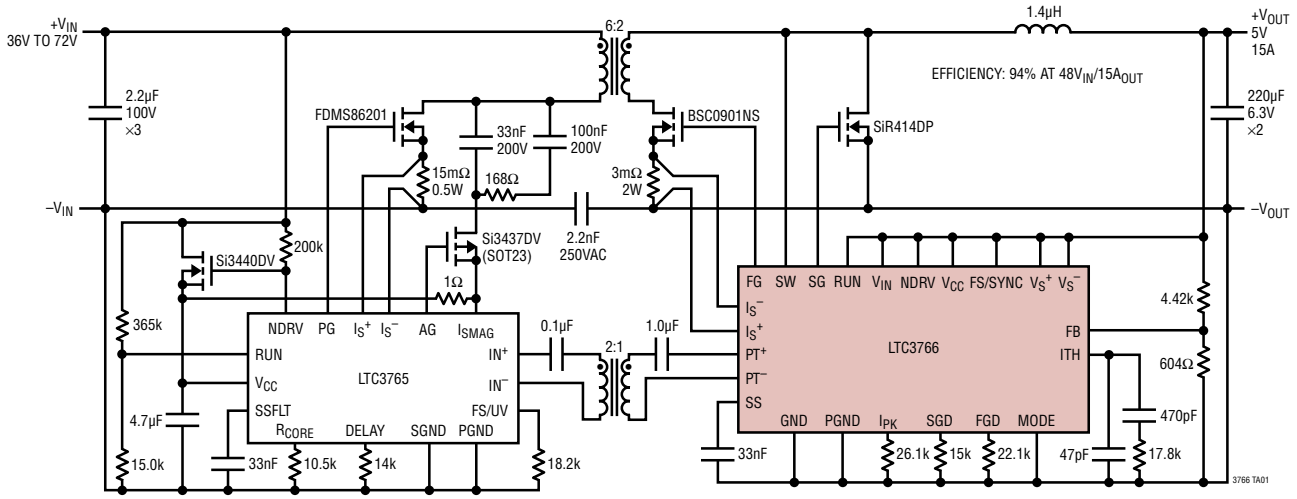
The LTC®3766 is a PolyPhase-capable secondary-side controller for synchronous forward converters. When used in conjunction with the LTC3765 active-clamp forward controller and gate driver, the part creates a complete isolated power supply that combines the power of multi-phase operation with the speed of secondary-side control.

The LTC3766 has been designed to simplify the design of active clamp forward converters. Working in concert with the LTC3765, the LTC3766 forms a robust, self-starting converter that eliminates the need for the separate bias regulator that is commonly used in secondary-side control applications. A precision current-limit coupled with clean start-up into a pre-biased load make the LTC3766 an excellent choice for high-power battery charger applications.

The LTC3766 provides extensive remote sensing and output protection features, while Direct Flux Limit guarantees no transformer saturation without compromising transient response. A linear regulator controller and internal bypass LDO are also provided to simplify the generation of the secondary-side bias voltage.

TYPICAL APPLICATION

36V – 72V to 5V/15A Active Clamp Isolated Forward Converter

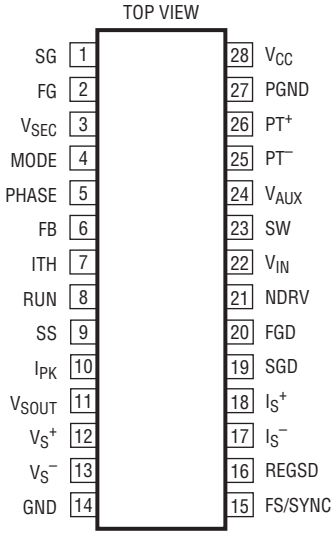


ABSOLUTE MAXIMUM RATINGS (Note 1)

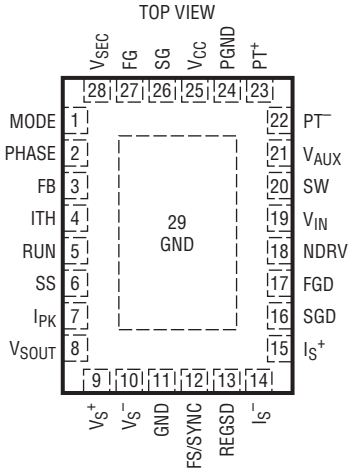
V_{CC} Voltage ..... –0.3V to 12V
V_{IN} Voltage ..... –0.3V to 33V
RUN Voltage ..... –0.3V to 33V
SW
  Low Impedance Source ..... –5V to 40V
  Current Fed ..... 2mA DC or 0.2A for <1µs Into Pin*
V_{AUX}, V_S^+, V_S^-, V_{SOUT}, NDRV Voltages ..... –0.3V to 16V
ITH, I_S^+, REGSD Voltages ..... –0.3V to 6V
PHASE Voltage ..... –0.3V to 6V
I_S^-, SGD, FGD Voltages ..... –0.3V to 12V
FS/SYNC, FB, MODE Voltages ..... –0.3V to 12V
V_{SEC} Voltage ..... –0.3V to 3V
I_{PK}, SS Voltages ..... –0.3V to 4V
Operating Junction Temperature Range (Notes 2,3)
  LTC3766E, LTC3766I ..... –40°C to 125°C
  LTC3766H ..... –40°C to 150°C
  LTC3766MP ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
  GN Package ..... 300°C

*The LTC3766 contains an internal 50V clamp that limits the voltage on the SW pin.

PIN CONFIGURATION



GN PACKAGE
28-LEAD NARROW PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UFD PACKAGE
28-LEAD (4mm × 5mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 43°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

http://www.linear.com/product/LTC3766#orderinfo

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3766EGN#PBF	LTC3766EGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3766IGN#PBF	LTC3766IGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 125°C
LTC3766HGN#PBF	LTC3766HGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–40°C to 150°C
LTC3766MPGN#PBF	LTC3766MPGN#TRPBF	LTC3766GN	28-Lead Narrow Plastic SSOP	–55°C to 150°C
LTC3766EUFD#PBF	LTC3766EUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3766IUFD#PBF	LTC3766IUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3766HUFD#PBF	LTC3766HUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–40°C to 150°C
LTC3766MPUFD#PBF	LTC3766MPUFD#TRPBF	3766	28-Lead (4mm × 5mm) Plastic QFN	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Regulated Feedback Voltage	(Note 4) ITH = 1.2V	●	0.592	0.600	0.608	V
I_{FB}	Feedback Input Current	(Note 4)			2	50	nA
$\Delta V_{FB(LINREG)}$	Feedback Voltage Line Regulation	V_{IN} = 5V to 32V, ITH = 1.2V			0.001		%/V
$\Delta V_{FB(LOADREG)}$	Feedback Voltage Load Regulation	Measured in Servo Loop, ITH = 0.5V to 2V	●		–0.01	–0.1	%
V_{ISAVG}	Average Current Sense Threshold	Resistor Sense (RS) Mode Current Transformer (CT) Mode		47 0.66	55 0.73	63 0.80	mV V
V_{ISADJ}	Current Sense Ripple Compensation	RS Mode CT Mode V_{SW} = 10V, V_S^+ = 5V, FS/SYNC = V_{CC}, R_{IPK} = 23.7k			10 140		mV mV
V_{ISOC}	Overcurrent Shutdown Threshold	RS Mode: V_{IS}^- = 0V CT Mode: V_{IS}^- = V_{CC}		86 1.22	100 1.33	113 1.44	mV V
I_{SIN}	I_S^+ and I_S^- Input Current				280	500	nA
g_m	Error Amplifier g_m			2.2	2.7	3.2	mS
R_{EA}	Error Amplifier Output Resistance	(Note 7)			5		MΩ
$I_{SOFT(C)}$	Soft-Start Charge Current	V_{SS} = 2V		4	5	6	µA
$I_{SOFT(D)}$	Soft-Start Discharge Current	V_{SS} = 2V			3		µA
V_{RUNR}	RUN Pin On Threshold	V_{RUN} Rising	●	1.18	1.22	1.26	V
V_{RUNF}	RUN Pin Off Threshold	V_{RUN} Falling	●	1.13	1.17	1.21	V
I_{RUN}	RUN Pin Hysteresis Current	V_{RUN} = 0.5V		2.2	3.0	3.6	µA
$t_{ON(MIN)}$	Minimum Controllable On Time				200		ns
D_{MAX}	Maximum Duty Cycle	FGD = SGD = GND		77	79	81	%
$\Delta V_{SEC(TH)}$	Volt-Second Limit Threshold Accuracy	2V ≤ V_{SW} < 5V 5V ≤ V_{SW} ≤ 40V		–6 –4		6 4	% %
R_{VSDN}	Volt-Second Discharge Resistance				75		Ω
V_{SWCL}	SW Clamp Voltage	I_{SW} = 1mA		43	51	60	V
$\Delta V_{FB(OV)}$	Output Overvoltage Threshold	V_{FB} Rising		15	17	19	%

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Drivers and Control							
FG, SG R_{UP}	FG, SG Driver Pull-Up On-Resistance				1.5		Ω
FG, SG R_{DOWN}	FG, SG Driver Pull-Down On-Resistance				1.0		Ω
PT^+, PT^- R_{UP}	PT^+, PT^- Driver Pull-Up Resistance				1.5		Ω
PT^+,PT^- R_{DOWN}	PT^+, PT^- Driver Pull-Down Resistance				1.5		Ω
t_{FGD}	FGD Delay	R_{FGD} = 10kΩ R_{FGD} = 100kΩ		50 436	65 545	80 654	ns ns
t_{SGD}	SGD Delay	R_{SGD} = 15kΩ R_{SGD} = 50kΩ		60 195	75 230	90 265	ns ns
$V_{SW(REV)}$	SG Reverse Overcurrent SW Threshold	LV MODE HV MODE		66 140	73 148	79 156	mV mV
$I_{SW(REV)}$	SG Reverse Overcurrent Adjust Current	LV MODE HV MODE		–86 –34.5	–103 –42	–120 –49	µA µA
V_{CC} Supply							
V_{CCOP}	V_{CC} Operating Voltage Range			5		10	V
I_{CC}	Supply Current Normal Mode Shutdown	 $V_{FS/SYNC}$ = V_{CC} = 7V (Note 5) V_{RUN} = GND			 5 210		 mA µA
V_{UVLOR}	UV Lockout Rising	V_{CC} Rising, LV MODE V_{CC} Rising, HV MODE	● ●	4.6 7.7	4.7 7.9	4.8 8.1	V V
V_{UVLOF}	UV Lockout Falling	V_{CC} Falling, LV MODE V_{CC} Falling, HV MODE	● ●	3.8 6.7	3.9 6.9	4.0 7.1	V V
V_{REGSD}	REGSD Threshold Voltage	V_{REGSD} Rising			1.21		V
$I_{REGSD(C)}$	REGSD Charge Current	V_{REGSD} = 0.7V			13		µA
$I_{REGSD(D)}$	REGSD Discharge Current	V_{REGSD} = 0.7V			3		µA
V_{AUX} Supply							
V_{AUXOP}	V_{AUX} Operating Voltage Range			5		15	V
V_{CCVAUX}	Regulated V_{CC} Output Voltage	V_{AUX} = 15V, LV MODE V_{AUX} = 15V, HV MODE		6.7 8.1	7.0 8.5	7.3 8.9	V V
V_{AUXLR}	V_{CC} Load Regulation	I_{CC} = 0mA to 120mA, V_{AUX} = 8V, LV MODE			0.8	2	%
V_{AUXSWP}	V_{AUX} Switchover Voltage Rising	V_{AUX} Ramping Positive, LV MODE V_{AUX} Ramping Positive, HV MODE		4.50 7.65	4.70 8.00	4.88 8.35	V V
V_{AUXSWN}	V_{AUX} Switchover Voltage Falling	V_{AUX} Ramping Negative, LV MODE V_{AUX} Ramping Negative, HV MODE		4.30 7.35	4.50 7.70	4.70 8.05	V V
R_{AUX}	V_{AUX} Dropout Resistance	I_{CC} = 120mA, V_{AUX} = 4.9V			1.7	2.5	Ω
R_{PSL}	V_{AUX} Pre-Switchover Load	V_{AUX} = 4V			920		Ω
V_{IN} Supply							
V_{INOP}	V_{IN} Operating Voltage Range			5		32	V
V_{INCL}	V_{IN} Clamp Voltage	I_{VIN} = 2mA, V_{RUN} = GND		28	30	32	V
I_{CLMAX}	V_{IN} Clamp Current Limit	V_{IN} = 33V, V_{RUN} = GND		3.8	5.5	7.2	mA
V_{CCVIN}	Regulated V_{CC} Output Voltage	LV MODE (Note 6) HV MODE (Note 6)		6.7 8.1	7.2 8.5	7.3 8.9	V V
I_{IN}	Supply Current Operating Shutdown	 $V_{FS/SYNC}$ = V_{CC} V_{RUN} = GND			 900 450	1200	 µA µA
V_{INUVLO}	V_{IN} Undervoltage Lockout	V_{IN} Rising		2.6	3.2	3.8	V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. (Note 2) V_{IN} = 15V, GND = PGND = 0V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Oscillator and Phase-Locked Loop							
$I_{FS/SYNC}$	FS/SYNC Pin Sourcing Current				20		µA
f_{HIGH}	Oscillator High Frequency Set Point	$V_{FS/SYNC} = V_{CC}$		234	275	316	kHz
Δf ($R_{FS/SYNC}$)	Oscillator Resistor Set Accuracy	18.75kΩ < $R_{FS/SYNC}$ < 125kΩ	●	–12		12	%
$f_{PLL(RANGE)}$	PLL Sync Frequency Range			100		500	kHz
Differential Amplifier							
A_{DA}	Gain	1.5V ≤ V_{SOUT} ≤ 15V, V_{IN} = 20V		0.99	1	1.01	V/V
$CMRR_{DA}$	Common Mode Rejection Ratio	V_{IN} = 20V			75		dB
R_{INP}	V_S^+ Input Resistance	V_{IN} = 20V			120		kΩ
R_{INM}	V_S^- Input Resistance	V_{IN} = 20V			160		kΩ
I_{OH}	Output Sourcing Current	V_{IN} = 20V, V_S^+ = 5V, V_{SOUT} = 2.5V	●	0.8	3.0		mA
V_{IN}-V_{OHST}	Output High Fault Threshold	V_S^+ Rising			1.2	1.5	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3766E is guaranteed to meet specifications from 0°C to 85°C with specifications over the –40°C to 125°C operating junction temperature range assured by design, characterization and correlation with statistical process controls. The LTC3766I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3766H is guaranteed over the –40°C to 150°C operating junction temperature range, and the LTC3766MP is tested and guaranteed over the –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

Note 3: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

$$T_J = T_A + (P_D \bullet \theta_{JA}°C/W)$$

where θ_{JA} is 95°C/W for the SSOP and 43°C/W for the QFN package.

Note 4: The LTC3766 is tested in a feedback loop that servos V_{FB} to a voltage near the internal 0.6V reference voltage to obtain the specified ITH voltage (V_{ITH} = 1.2V).

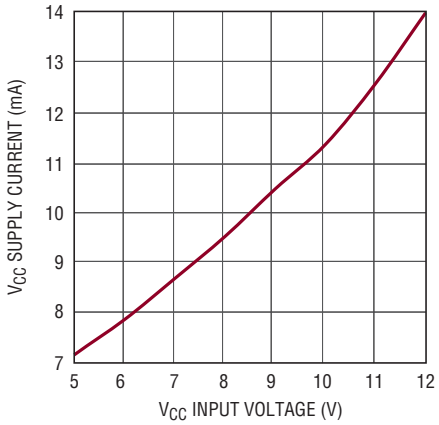
Note 5: Operating supply current is measured in test mode. Dynamic supply current is higher due to the internal gate charge being delivered at the switching frequency. See Typical Performance Characteristics.

Note 6: The V_{IN} Regulator employs an external pass device to produce the regulated V_{CC} output voltage. The LTC3766 is tested using a 2N3904 NPN transistor as an external pass device.

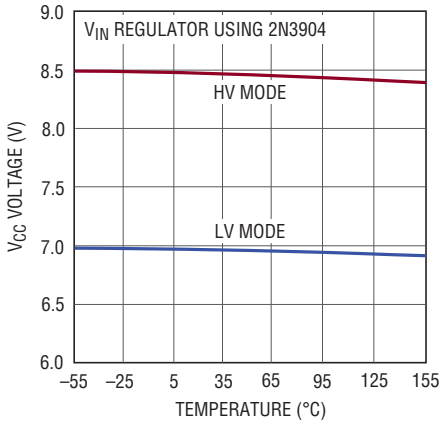
Note 7: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

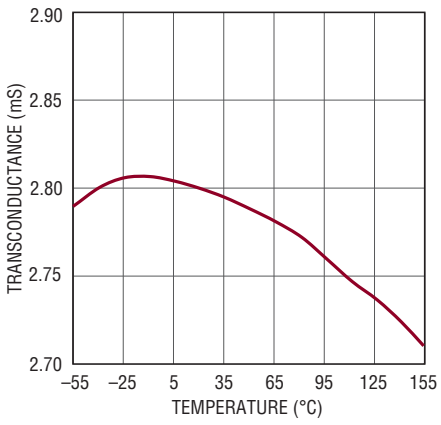
V_{CC} Supply Current vs V_{CC} Voltage



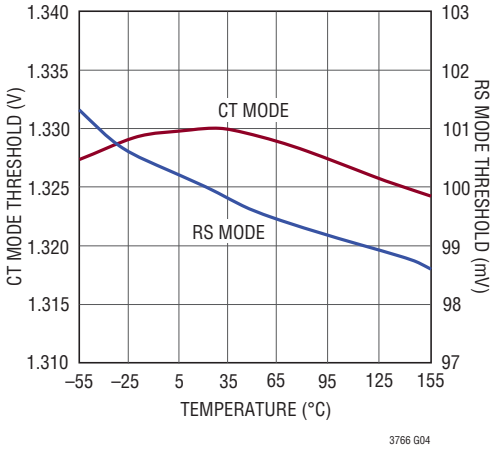
V_{CC} Regulator Output Voltage vs Temperature



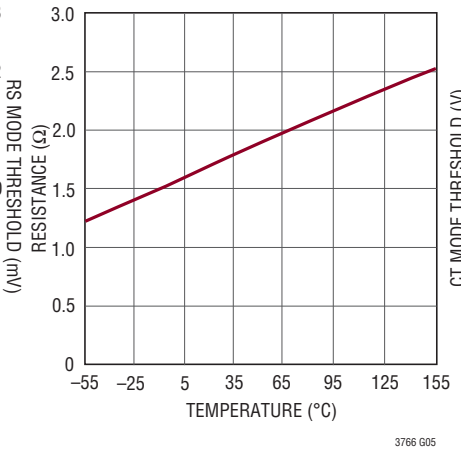
Error Amplifier Transconductance vs Temperature



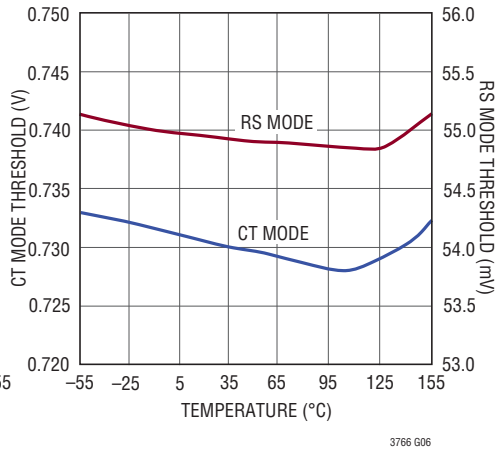
Overcurrent Shutdown Threshold vs Temperature



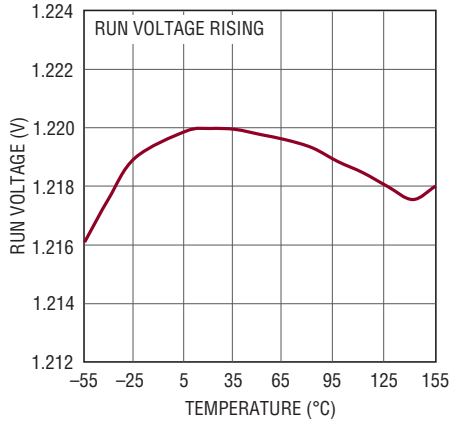
V_{AUX} Drop-Out Resistance vs Temperature



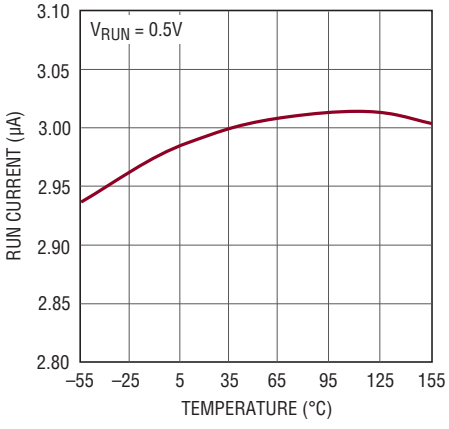
Average Current Sense Threshold vs Temperature



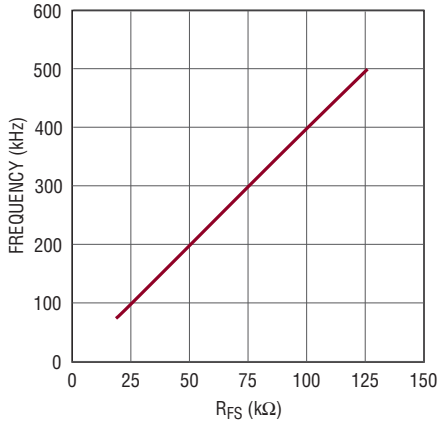
RUN Threshold vs Temperature



RUN Hysteresis Current vs Temperature

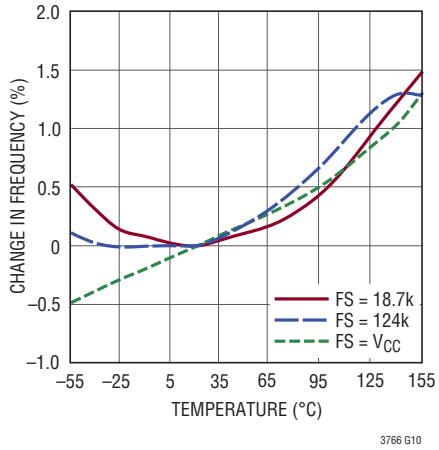


Oscillator Frequency vs R_{FS}

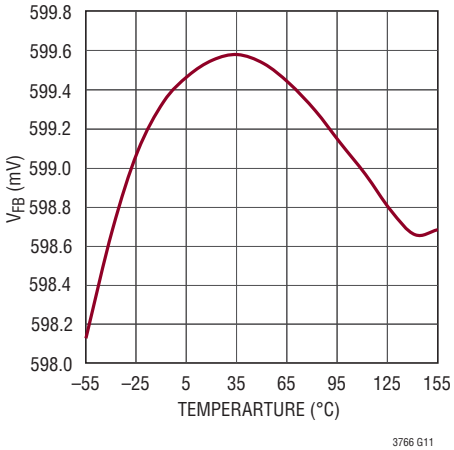


TYPICAL PERFORMANCE CHARACTERISTICS

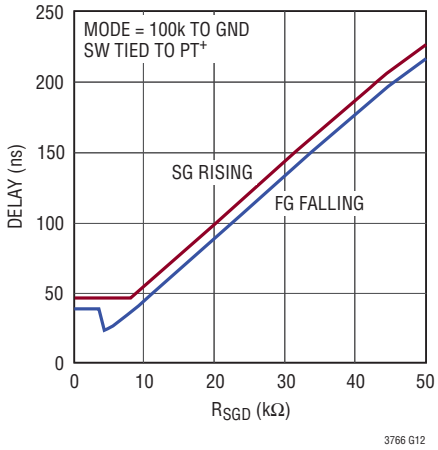
Oscillator Frequency vs Temperature



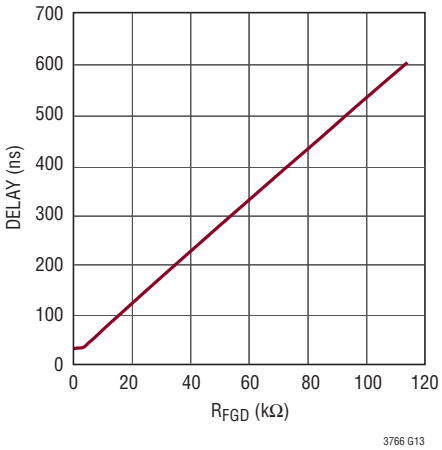
FB Voltage vs Temperature



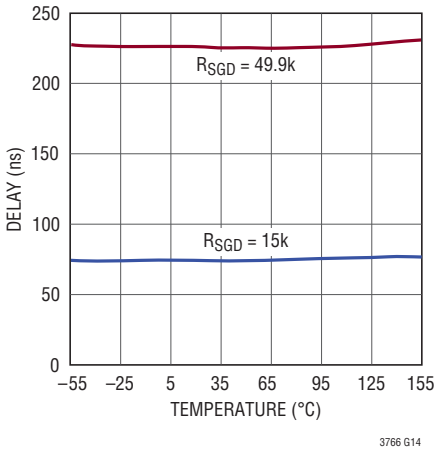
SGD Delay vs Resistance



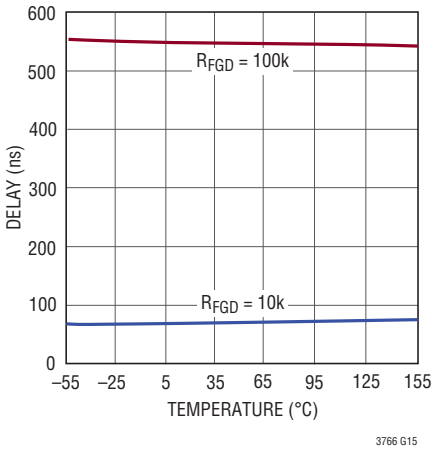
FGD Delay vs Resistance



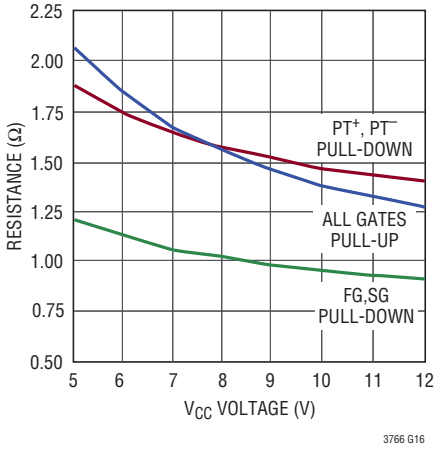
SGD Delay vs Temperature



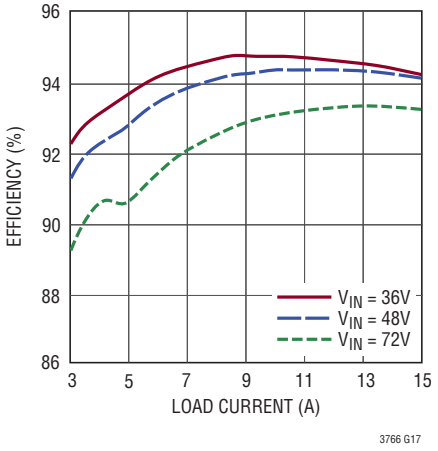
FGD Delay vs Temperature



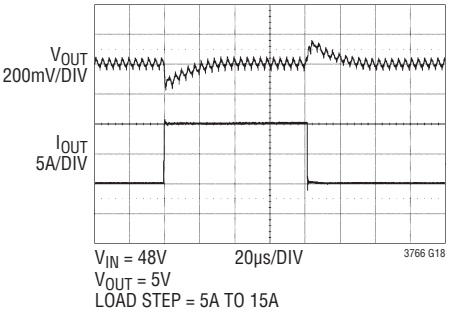
Gate Driver On-Resistance vs V_{CC} Voltage



Efficiency (Figure 39 Circuit)



Load Step (Figure 39 Circuit)



PIN FUNCTIONS (SSOP/QFN)

SG (Pin 1/Pin 26): Gate Drive for the Synchronous MOSFET.

FG (Pin 2/Pin 27): Gate Drive for the Forward MOSFET.

V_{SEC} (Pin 3/Pin 28): Volt-Second Limit. Connect a resistor from SW to V_{SEC}, and a capacitor from V_{SEC} to GND to set the maximum volt-second product that is applied to the main power transformer. The PWM on-time is terminated when the V_{SEC} voltage exceeds the internally generated threshold. Tie to GND if not used.

MODE (Pin 4/Pin 1): For normal isolated applications using the LTC3765, tie to either GND or V_{CC} to set the operating voltage to either low voltage or high voltage modes respectively, as needed to drive the gates of the synchronous and forward MOSFETs. For nonisolated applications, tie to ground through either a 100k or 50k resistor to activate standalone mode (for low voltage or high voltage operation respectively). In this mode, the PT^+ pin may be directly connected to the gate of a primary-side MOSFET, and a reference clock signal is generated on the PT^- pin. In standalone mode, the FGD pin is ignored and the associated delay is set adaptively.

PHASE (Pin 5/Pin 2): Control Input to the Phase Selector. This pin determines the phasing of the internal controller CLK relative to the synchronizing signal at the FS/SYNC pin.

FB (Pin 6/Pin 3): The Inverting Input of the Main Loop Error Amplifier. Tie to V_{CC} or other voltage greater than 2.5V to enable slave mode in PolyPhase applications.

ITH (Pin 7/Pin 4): The Output of the Main Loop Error Amplifier. Place compensation components between the ITH pin and GND.

RUN (Pin 8/Pin 5): Run Control Input. Holding this pin below 1.22V will shut down the IC and reset the soft-start and REGSD pins to 0V.

SS (Pin 9/Pin 6): Soft-Start Inputs. A capacitor to ground sets the ramp time of the output voltage.

I_{PK} (Pin 10/Pin 7): Peak Current Limit Inductor Ripple Cancellation. This pin is used to adjust the peak current limit based on the amount of inductor current ripple, thereby providing a constant average output current during current limit. Place a resistor to GND that is proportional to the main output inductor. Leave this pin floating for constant peak current limit. Minimize parasitic capacitance on this pin.

V_{SOUT}, V_S^+, V_S^- (Pins 11, 12, 13/Pins 8, 9, 10): V_{SOUT} is the output of a precision, unity-gain differential amplifier. Tie V_S^+ and V_S^- to the output of the main DC/DC converter to achieve true remote differential sensing. Also, V_S^+ is used for directly sensing the output voltage for inductor ripple cancellation. Do not exceed the output sourcing current specification on the V_{SOUT} pin or a fault will be generated. See the Applications Information section for details.

GND (Pin 14/Pin 11, Exposed Pad Pin 29): Signal Ground and Kelvin Sense for SG Reverse Overcurrent. Connect to power ground at the source of the synchronous MOSFET. The exposed pad must be soldered to PCB ground for rated thermal performance.

FS/SYNC (Pin 15/Pin 12): Combination Frequency Set and Sync Pin. Tie to V_{CC} to run at 275kHz. Place a resistor to ground at this pin to set the frequency between 75kHz and 500kHz. To synchronize, drive this pin with a clock signal to achieve PLL synchronization from 100kHz to 500kHz. Sources 20µA of current.

REGSD (Pin 16/Pin 13): Regulator Shutdown Timer. Place a capacitor to ground to limit the time allowed for the high voltage linear regulator controller to operate. When the REGSD voltage exceeds 1.21V, the linear regulator is shut down. This pin sources 13µA of current when the linear regulator is active.

I_S^- (Pin 17/Pin 14): Negative Input to the Current Sense Circuit. Connect to the negative end of a low side current sense resistor. When using a current sense transformer, tie this pin to V_{CC} for single-ended sensing on I_S^+ with a higher maximum trip level.

I_S^+ (Pin 18/Pin 15): Positive Input to the Current Sense Circuit. Connect to the positive end of a low side current sense resistor or to the output of a current sense transformer.

SGD (Pin 19/Pin 16): Synchronous Gate Rising Edge Delay. A resistor to GND sets the delay from primary gate turn-off (PT^+ falling) to SG rising (and FG falling). This delay is used to optimize the dead time between the turn-off of the primary-side MOSFET and the turn-on of SG. Tie SGD to GND to set this delay adaptively based on the falling edge of the SW pin voltage. See Setting the Gate Driver Delays in the Applications Information section.

PIN FUNCTIONS (SSOP/QFN)

FGD (Pin 20/Pin 17): Forward Gate Rising Edge Delay. A resistor to GND sets the delay from PT^+ rising to FG rising (and SG falling). This delay is used to optimize the dead time between the turn-off of SG and the turn-on of the primary-side MOSFET. In standalone mode (100k or 50k resistor on MODE), this dead time is set adaptively and the FGD pin can be grounded. See Setting the Gate Driver Delays in the Applications Information section.

NDRV (Pin 21/Pin 18): Drive Output for the External Pass Device of the High Voltage Linear Regulator Controller. Connect to the base (NPN) or gate (MOSFET) of an external N-type device. Tie to V_{CC} pin if only using the internal LDO (V_{AUX} pin).

V_{IN} (Pin 22/Pin 19): Connect to a higher voltage bias supply when using the linear regulator controller. The V_{IN} pin supplies bias to the internal standby and monitoring circuits, the linear regulator controller, and the differential amplifier. Tie to V_{AUX} pin if only using the internal LDO.

SW (Pin 23/Pin 20): Connect (Kelvin) to the drain of the synchronous MOSFET. This input is used for adaptive shoot-through prevention and leading-edge blanking, monitoring the high level SW node voltage and SG reverse-current protection. When SW is high, the voltage on this pin is internally measured for use in the inductor ripple cancellation and volt-second limit circuits. When SW is low and SG is high, this pin sources a small current and is used for SG reverse overcurrent protection. A resistor can be placed between the SW pin and the drain of the synchronous MOSFET to adjust the SG reverse-over current threshold. The SW pin is internally clamped to 50V.

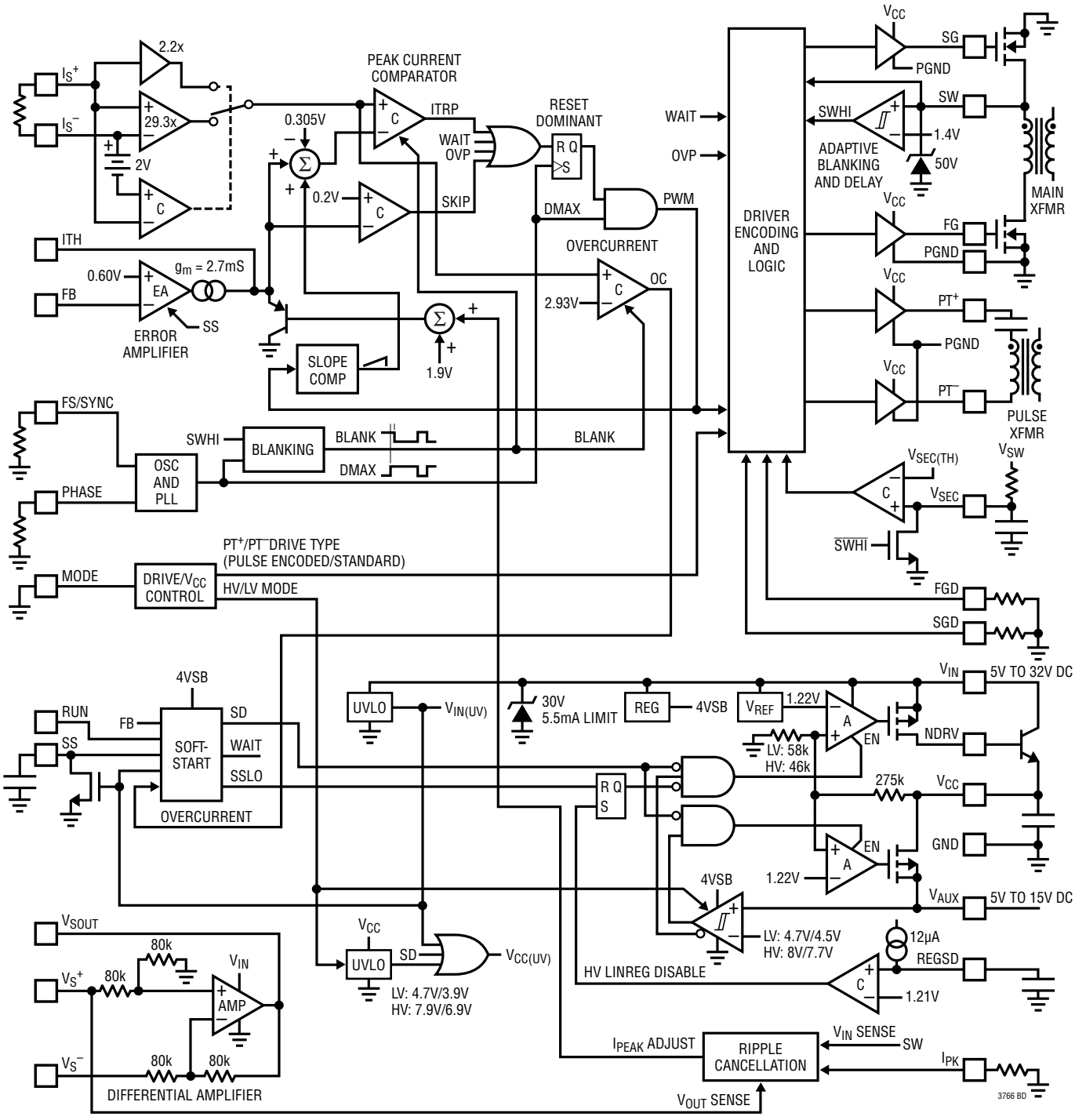
V_{AUX} (Pin 24/Pin 21): Auxiliary Power Input. This is the power input to an internal LDO that is connected to V_{CC}. Whenever V_{AUX} is greater than 4.7V (or 8V for high voltage mode), this LDO will supply power to V_{CC}, bypassing the main linear regulator that is powered from V_{IN}. See V_{AUX} Connection in the Applications Information section. Do not exceed 16V on the V_{AUX} pin.

PT^-, PT^+ (Pin 25, 26/Pin 22, 23): Pulse Transformer Driver Outputs. For most applications, these connect to a pulse transformer through a series DC-blocking capacitor. The PWM information is multiplexed together with DC power and sent through the pulse transformer to the primary side. The PWM signal is then decoded by the LTC3765 active clamp forward controller and gate driver. In standalone mode (100k or 50k resistor on MODE), the PT^+ pin has a standard PWM signal and may be directly connected to the gate of a primary-side MOSFET, while a reference clock is generated on the PT^- pin.

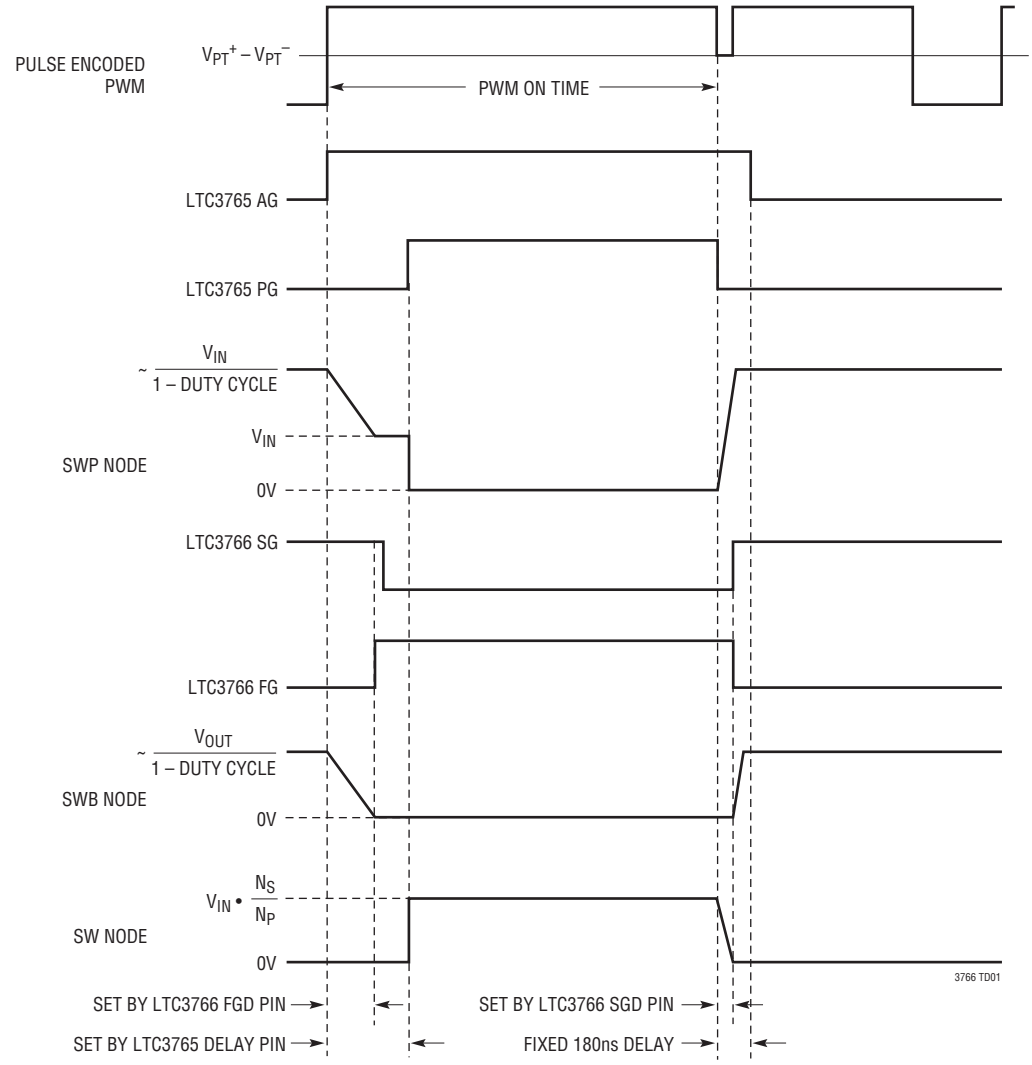
PGND (Pin 27/Pin 24): Gate Driver Ground Pin. Connect to power ground at the source of the synchronous MOSFET.

V_{CC} (Pin 28/Pin 25): Main V_{CC} Input for All Driver and Control Circuitry.

BLOCK DIAGRAM



TIMING DIAGRAM



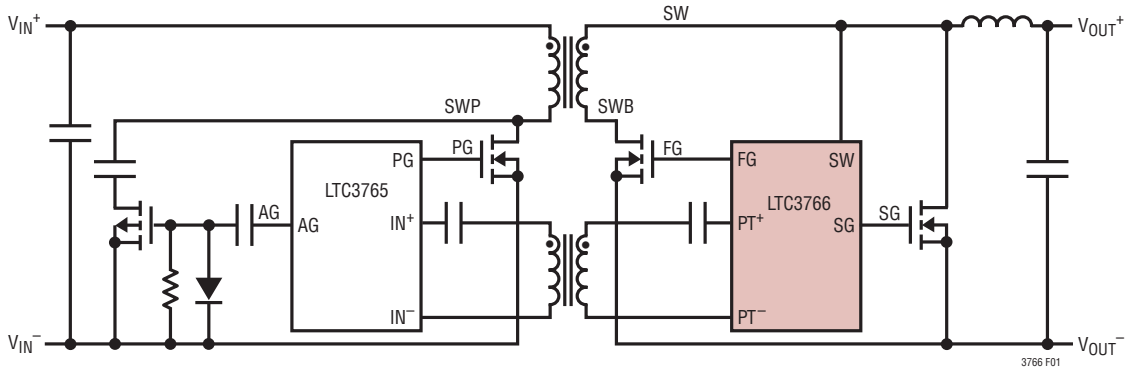


Figure 1. Reference Schematic for Timing Diagram

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The LTC3766 is a secondary-side PWM controller designed for use in a forward converter with active clamp reset and synchronous rectification. When used in conjunction with the LTC3765 active-clamp forward controller and gate driver, it forms a highly efficient and robust isolated power supply with a minimum number of external components. By making use of a secondary-side control architecture, the LTC3766 is able to provide exceptional transient response while directly monitoring the load to ensure that both output voltage and output current are precisely controlled. This architecture provides superior performance and greater simplicity, and is particularly well suited to high power battery charger applications.

Self-Starting Start-Up

In most applications, the LTC3766 will be used with the LTC3765 to create a self-starting forward converter with secondary-side control. Since there is initially no bias voltage available on the secondary side, the LTC3765 must manage the start-up in an open-loop fashion on the primary side. When power is first applied on the primary side, the LTC3765 begins an open-loop soft-start using its own internal oscillator. Power is supplied to the secondary by switching the main primary-side MOSFET with a gradually increasing duty cycle from 0% to 70%, as controlled by the rate of rise of the voltage on the SSFLT pin. On the secondary side, bias voltage can be generated directly from the main transformer using a peak charge circuit, or other technique as appropriate. When the LTC3766 has adequate voltage to satisfy its start-up requirements, it provides duty cycle information through the pulse transformer as shown in Figure 2. The LTC3765 detects this signal and transfers control of the gate drivers to the LTC3766, which continues the soft-start of the output voltage. Typically, this hand-off from primary to secondary occurs when the output voltage is less than one half of its final level. The LTC3765 then turns off the linear regulator and, through an on-chip rectifier, extracts bias power for the primary-side MOSFETs from this signal.

Linear Regulators

In general, the bias voltage generated on the secondary side is higher than the level desired for operation of the forward and synchronous MOSFETs. Consequently, the LTC3766 contains a high voltage linear regulator controller as well as a 15V V_{AUX} bypass regulator with an internal PMOS, either of which can be used to regulate the voltage on the V_{CC} pin. The linear regulator controller is used by tying the NDRV pin to the base or gate of an external N-type pass device. The LTC3766 V_{IN} pin provides bias to the linear regulator controller as well as to internal standby and monitoring circuitry. If adequate voltage is detected on the V_{AUX} pin, then the V_{AUX} bypass regulator will be activated and the high voltage linear regulator controller will be shut down to reduce power loss. Alternatively, if only the V_{AUX} regulator is needed, then the NDRV pin can be tied off to V_{CC}, while V_{IN} is tied to V_{AUX}. This flexible arrangement of two linear regulators allows for the convenient and efficient generation of V_{CC} bias voltage for a wide array of applications.

Using the MODE pin, the output voltage of both linear regulators can be set to either 7V or 8.5V, depending on the level needed to drive the gates of the forward and synchronous MOSFETs. Note that the undervoltage lockout (UVLO) set points as well as V_{AUX} switchover levels are adjusted along with the V_{CC} regulation levels. This ensures that the MOSFETs are only switched when there is adequate gate drive voltage.

Run Control and Soft-Start

The main on/off control for the LTC3766 is the RUN pin. This pin features precision thresholds with both internal and externally adjustable hysteresis. This pin can be used to monitor the secondary-side bias voltage or main output voltage, thereby controlling the point at which hand-off from primary to secondary side occurs. Alternatively, it can be driven directly with a control signal. In nonisolated applications when the LTC3766 is used standalone, this pin can be used as an undervoltage lockout by monitoring the main power supply input voltage. See Nonisolated Applications in the Applications Information section for details.

The LTC3766 will begin a soft-start sequence when the RUN pin is high, adequate voltage is present on both the V_{IN} and V_{CC} pins, and switching is detected on the SW pin. Note that the LTC3766 must see switching on the SW pin prior to initiating a soft-start sequence to ensure that the LTC3765 is ready for control hand-off. The soft-start sequence begins by first measuring the voltage on the FB pin and then rapidly pre-setting the soft-start capacitor voltage to a level that corresponds to the output voltage,

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V_{OUT}. This is done to provide a smooth ramp on the output voltage as control is transferred from primary to secondary, as well as to avoid any unnecessary start-up delay. Once the soft-start capacitor has been pre-set to the appropriate level, the LTC3766 then sends a brief sequence of pulses through the pulse transformer to establish a communication lock between the LTC3766 and the LTC3765. At this point, the LTC3766 assumes control of the primary-side MOSFETs, and the soft-start capacitor begins charging with a constant current of 5µA, continuing the soft-start of the main output voltage. Note that the soft-start voltage is used to limit the effective level of the reference into the error amplifier. This technique maintains closed-loop control of the output voltage during the secondary-side soft-start interval.

Gate Drive Encoding

Since the LTC3766 controller normally resides on the secondary side of an isolation barrier, communication to the primary-side gate driver must be done through a small pulse transformer. A common scheme for communicating gate drive (PWM) information makes use of short pulses and relies on receiver latches to "remember" whether power MOSFETs should be either on or off. However, this system is prone to get into the wrong state, and has difficulty distinguishing a loss of signal from a legitimate zero duty cycle signal. To alleviate these concerns, the LTC3766 uses a proprietary gate drive encoding scheme that reliably maintains constant contact across the isolation barrier without introducing any delay.

The LTC3766 encodes PWM information onto the PT^+ and PT^- outputs, which are in turn connected to a small pulse transformer through a DC-blocking capacitor. These outputs are driven in a complementary fashion, with a constant 79% duty cycle. This results in a stable volt-second balance, so that the signal amplitude transferred across the pulse transformer is constant. As shown in Figure 2, the beginning of the interval when (V_{PT}^+-V_{PT}^-) is positive approximately coincides with the turn-on of the main primary-side MOSFET. Likewise, the beginning of the interval when (V_{PT}^+-V_{PT}^-) is negative coincides with the maximum duty cycle (forced turn-off of main primary-side MOSFET). At the appropriate time during the positive interval, the end of the "on" time (PWM going low) is signaled by briefly applying a zero-volt differential across the pulse transformer. In the event that a zero duty-cycle signal needs to be sent, this is accomplished naturally by placing the zero-voltage differential at the beginning of the positive interval. In this manner, any duty cycle from 0% to the maximum of 79% can be sent across the pulse transformer without delay. Figure 2 illustrates the operation of this encoding scheme.

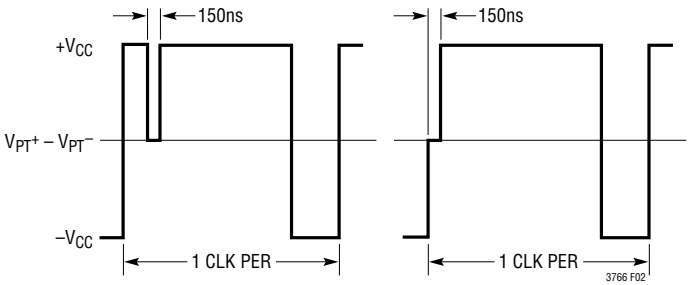

Figure 2: Gate Drive Encoding Scheme (MODE = GND or MODE = V_{CC})

On the primary side, the LTC3765 receives the signal from the pulse transformer through a DC restoring capacitor. After communication lock has been established between the two parts, the LTC3765 extracts clock and duty cycle information from the signal and uses it to control its gate driver outputs. Note that, except for a tiny pulse, this scheme is constantly applying a differential voltage across the pulse transformer. Therefore, the LTC3765 can almost instantly detect a loss of signal and shut off the power MOSFETs.

Forward Converter and Main Loop Operation

Once communication lock has been established between the LTC3766 and the LTC3765, the LTC3766 will have control over the switching of the primary-side MOSFETs. During normal operation, the main primary-side MOSFET (connected to PG on the LTC3765) is turned on somewhat after the forward MOSFET on the secondary side. This applies the input voltage across the transformer, causing the SW node on the secondary side to rise. Since the SW node voltage is greater than the output voltage, the inductor current ramps upward. When the current in the inductor has ramped up to the peak value as commanded by the voltage on the ITH pin, the current sense comparator trips, turning off the primary-side MOSFET. After a short delay,

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the forward MOSFET is turned off and the synchronous MOSFET is turned back on, causing the inductor current to ramp back downwards. At the next rising edge of the LTC3766 internal clock, the cycle repeats as the synchronous MOSFET is turned off and the forward and main primary-side MOSFETs are again turned on. The LTC3766 error amplifier senses the main output voltage, and adjusts the ITH voltage to obtain the peak inductor current needed to keep the output voltage at the desired regulation level.

In some applications, there can be considerable resistive voltage drops between the main output voltage and the load. To address this, the LTC3766 contains a precision differential amplifier, which can be used to remotely sense a load voltage as high as 15V.

Current Sensing, Slope Compensation and Blanking

The LTC3766 supports current sensing either with a current sense resistor or with an isolated current transformer. When using a current sense resistor, the I_S^+ and I_S^- pins operate differentially, and the maximum peak current threshold is approximately 75mV. Normally, the current sense resistor is placed in the source of the forward MOSFET to minimize power loss. If a current transformer is used to sense the primary-side switch current, then the I_S^- input should be tied to V_{CC} and the I_S^+ pin to the output of the current transformer. This causes the gain of the internal current sense amplifier to be reduced, so that the maximum peak current threshold is increased to approximately 1V.

As with any PWM controller that uses constant-frequency peak current control, slope compensation is needed to provide current-loop stability and improve noise margin. The LTC3766 has fixed internal slope compensation. The amount of slope has been chosen to be adequate for a wide range of applications. Normally, the use of slope compensation would have a negative impact on the accuracy of the current limit, but the LTC3766 uses a proprietary circuit to nullify the effect of slope compensation on the current limit performance.

Since the LTC3766 current loop is sensing switch current, leading edge blanking is needed to avoid a current comparator false trip due to the MOSFET turn-on current spike. The LTC3766 uses the voltage on the SW pin (tied to the drain of the synchronous MOSFET) to implement an adaptive leading-edge blanking of approximately 180ns. The blanking of the current comparator begins only after the voltage on SW has risen above 1.4V. This adaptive blanking is essential because of the potentially long delay from the time that PT+ rises to the time that the SW node rises, and current begins ramping up in the output inductor. This blanking also minimizes the need for external filtering.

Gate Driver Delay Adjustment

As in all forward converters, the main transformer core must be properly reset so as to maintain a balanced volt-second product and prevent saturation. This job is handled on the primary side by the LTC3765, which features an active clamp gate driver. The active clamp MOSFET works together with a capacitor to generate an optimal reset voltage for the main transformer. This optimal reset voltage minimizes voltage stress on the main primary-side MOSFET and maximizes the utilization of the power transformer core by reducing the magnetic flux density excursion.

In general, the active clamp MOSFET is switched in a complimentary fashion to the main primary-side MOSFET. Since the active clamp MOSFET is a PMOS, the active clamp gate driver (AG) and the main primary-side gate driver (PG) voltages are therefore “in-phase,” with a programmable overlap time set by the LTC3765 DELAY pin.

The delay time between the active clamp PMOS turn-off and the primary switch NMOS turn-on is critical for optimizing efficiency. When the active clamp is on, the drain of the primary NMOS, or primary switch node (SWP), is driven to a voltage of approximately $V_{IN}/(1–D)$ by the main transformer. When the active clamp turns off, the current in the magnetizing inductance of the transformer ramps this voltage linearly down to V_{IN}. Power loss is minimized by turning on the primary switch when the SWP voltage is at a minimum. A resistor from the LTC3765 DELAY pin to ground sets a fixed time for the PG turn-on delay.

The delay time between the primary switch turn-off and the active clamp turn-on is substantially less critical. When the primary switch turns off, the main transformer leakage inductance is biased with the peak current of the inductor reflected through the transformer. This current drives the voltage across the active clamp PMOS quickly to 0V. Turning on the PMOS after this transition results in

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minimal switching power loss. The LTC3765 active clamp turn on delay is internally fixed to 180ns, which normally achieves zero voltage switching on the active clamp PMOS.

On the secondary side, the turn-on delay of the forward gate (FG) and synchronous gate (SG) MOSFETs are adjusted by the FGD and SGD pins respectively. These delays are set using resistors to GND so as to minimize the dead time (when the load current is being carried by MOSFET body diodes) while avoiding shoot-through with the primary-side MOSFETs. A shoot-through condition exists if either the PG and SG gates, or the AG and FG gates are high at the same time. Note that the SG MOSFET turn-on delay has a minimum limit that is established by the falling edge of the SW node. The SG pin will normally not go high until SW has fallen below 0.5V. After a 180ns timeout, however, the SG pin will go high regardless of the SW voltage. Refer to Delay Resistor Selection in the Applications Information section for more detailed information. In standalone mode (100k or 50k resistor on MODE), the dead time between PG and SG is set adaptively to prevent shoot-through.

Frequency Setting and Synchronization

The LTC3766 uses a single pin to set the operating frequency or to synchronize the internal oscillator to a reference clock using and on-chip phase-locked loop (PLL). The FS/SYNC pin sources a 20µA current, and it may be tied to V_{CC} for fixed 275kHz operation or have a single resistor to GND to set the switching frequency to $f_{SW} = 4R_{FS}$. If a clock signal (>2V) is detected at the FS pin, the LTC3766 will automatically synchronize to the falling edge of this signal using an internal PLL.

Current Limit and Inductor Ripple Cancellation

Since the LTC3766 utilizes peak current control, the peak inductor current is limited when the load current demand increases above the current limit set point. The peak current limit is established by an internal clamp on the maximum level of the ITH voltage. The average current, however, will be less than the peak current by an amount equal to one-half of the inductor ripple current. During current limit, this ripple current will change significantly with variations in V_{IN}, V_{OUT} and switching frequency. Without inductor ripple cancellation, this variation in ripple current would also result in an average output current that changes significantly, even though the peak current is held at a constant value.

In order to keep the average current approximately constant during current limit, the LTC3766 cancels the effect of the ripple current by adjusting the value of the peak current limit (or ITH clamp level) in proportion to the amount of inductor ripple current. This is achieved by generating an internal ramp that mimics the inductor current ramp, and then adding the amplitude of this internal ramp to the ITH clamp voltage on a cycle-by cycle basis. During the on time, the slope of the inductor current is given by:

$$\frac{dI_L}{dt} = \frac{V_{SW} - V_S^+}{L}$$

The LTC3766 establishes a voltage on the I_{PK} pin of $(V_{SW} - V_S^+)/15$, which is one-fifteenth of the voltage across the output inductor during the on-time when SW is high. By choosing a resistor R_{IPK} that is proportional to the value of the output inductor ($R_{IPK} = KL$), the current flowing in R_{IPK} becomes proportional to the slope of the inductor current:

$$I_{RIPK} = \frac{V_{SW} - V_S^+}{15R_{IPK}} = \frac{V_{SW} - V_S^+}{15KL}$$

During the time when SW is high, the LTC3766 uses the R_{IPK} current to create an internal ramp by charging an on-chip capacitor C_{RIP}. The slope of this internal ramp voltage is given by:

$$\frac{dV_{RAMP}}{dt} = \frac{I_{RIPK}}{C_{RIP}} = \frac{V_{SW} - V_S^+}{15KLC_{RIP}}$$

The amplitude of this internal ramp is then added to the ITH clamp level dynamically. By choosing the appropriate value of R_{IPK}, therefore, the average current during current limit will be essentially independent of changes in ripple current.

As is the case with all DC/DC converters that maintain constant frequency operation, a cycle by cycle current limit is only effective at duty cycles where the on time is greater than the minimum controllable on-time. Under short-circuit conditions, for example, the LTC3766 limits

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the current using a separate overcurrent comparator. When this overcurrent comparator is tripped, the LTC3766 generates a fault followed by a soft-start retry. This hiccup mode overcurrent protection is highly effective at minimizing power losses under short-circuit conditions.

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. Although the active clamp technique provides a suitable reset voltage during steady-state operation, the sudden increase in duty cycle caused in response to a load step can cause the transformer flux to accumulate or "walk," potentially leading to saturation. This occurs because the reset voltage on the active clamp capacitor cannot keep up with the rapidly changing duty cycle. This effect is most pronounced at low input voltage, where the voltage loop demands a greater increase in duty cycle due to the lower voltage available to ramp up the current in the output inductor.

Traditionally, transformer core saturation has been avoided either by limiting the maximum duty cycle of the converter or by slowing down the loop to limit the rate at which the duty cycle changes. Limiting the maximum duty cycle does help the converter avoid saturation for a load step at low input voltage, since the duty cycle maximum is clamped; however, transformer saturation can also easily occur at higher input voltage where the maximum duty cycle clamp is ineffective. Limiting the rate of duty cycle change such that the active clamp capacitor can sufficiently track the duty cycle change also helps to prevent saturation in many situations, but results in a very poor transient response. Neither of these traditional techniques is guaranteed to prevent the transformer from saturating in all situations. For example, saturation can easily occur using these traditional techniques when starting up into a pre-biased output, where the duty cycle can quickly change from 0% to 75%. Moreover, neither of these traditional techniques is able to prevent saturation in the negative direction, which can result from sudden decreases in duty cycle.

The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. During a reset cycle, when the active clamp PMOS is on, the magnetizing current is directly measured and limited through a sense resistor in series with the PMOS source. This prevents saturation in the negative direction. When the PMOS turns off and the main NMOS switch turns on, the LTC3765 generates an accurate internal estimate of the magnetizing current based on the sensed input voltage on the LTC3765 RUN pin and transformer core parameters customized to the particular core by a resistor from the LTC3765 R_{CORE} pin to ground. The magnetizing current is then limited during the on-time by this accurate internal approximation. Unlike previous methods, the Direct Flux Limit directly measures and monitors flux accumulation and guarantees that the transformer will not saturate in either direction, even when starting into a pre-biased output. This technique also provides the best possible transient response, as it will temporarily allow very high duty cycles, only limiting the duty cycle when absolutely necessary. Moreover, this technique prevents overcurrent damage to the active clamp PMOS, which is a potentially significant weakness in many active clamp forward converter designs.

Additional Protection Features

The LTC3766 contains a wide array of protection features, which protect the DC/DC converter in the event that abnormal conditions persist. In general, protections features are either classified as a fault or a limit. When a fault is detected, all switching stops and the LTC3766 initiates a soft-start retry. Faults of this nature include overcurrent, overtemperature, differential amplifier miswire and communication-lock fault.

An overcurrent fault occurs if the peak current exceeds approximately 133% of its normal value during current limit. Note that when inductor ripple cancellation is used, the value of the peak current during current limit will vary with inductor current ripple. The overtemperature fault is set at 165°C, with 20°C of hysteresis. This is helpful for limiting the temperature of the DC/DC converter in the event of some external device failure or other abnormal condition. The differential amplifier wiring fault is generated if the inputs on the differential amplifier are reversed, or if there is not enough voltage on the V_{IN} pin to support the voltage needed on V_{SOUT}. This is important to avoid an overvoltage condition on the output.

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Finally, since it is essential that the LTC3766 be in constant communication with the LTC3765, a loss of communication lock will also generate a fault. A lock condition is detected by monitoring the SW node voltage, and ensuring that it is both rising and falling as it should in response to the PWM signal being sent to the primary side. If the SW node voltage is not rising and falling in an appropriate manner, than a lock fault is generated. In particular, if the SW node does not rise within approximately 800ns of PT^+ rising, then a fault is immediately generated. Likewise, if the SW node does not fall within approximately 180ns of PT^+ falling, then a fault will also be generated, but only if this condition persists and the LTC3766 is operating at maximum duty cycle.

In addition to the four protection features that generate faults, there are also four protection features that establish a clamp or limit, without generating a fault. First, the LTC3766 contains a precision volt-second clamp. This feature is not needed when the LTC3766 is used in conjunction with the LTC3765, which incorporates the Direct Flux Limit feature. If the LTC3766 is used standalone, however, the volt-second limit can be used by placing a resistor from the SW node to the V_{SEC} pin and a capacitor from V_{SEC} to GND. When the SW node is low, the capacitor is discharged by an on-chip NMOS. When the SW node is high, the capacitor on V_{SEC} is charged. If the capacitor voltage exceeds an internally generated threshold, then the main primary switch will be turned off, thereby limiting the volt-second product applied to the main transformer. To compensate for the exponential nature of the RC charging circuit, the LTC3766 adjusts the threshold of the volt-second comparator according to:

$$V_{SEC(TH)} = 0.6 - \frac{0.16}{V_{SW(HI)}}$$

where $V_{SW(HI)}$ is the voltage on the SW pin during the on-time of the primary switch. This keeps the volt-second limit essentially constant for SW node voltages in the range of 2V to 40V.

Second, in the event that the main output voltage exceeds its regulation target by more than 17%, the LTC3766 will detect an overvoltage condition. If this happens, the LTC3766 will immediately turn off the main primary MOSFET and turn on the synchronous MOSFET. This has the effect of pulling down the output voltage to protect the load from potential damage. Overvoltage protection is not latched, and normal operation is restored when the output voltage has been reduced to within 15% of its regulation level.

Third, the LTC3766 contains an adjustable synchronous MOSFET reverse overcurrent. This is accomplished by monitoring the SW voltage when the synchronous MOSFET is on (SG pin is high). If the voltage on SW exceeds a pre-determined threshold, then the synchronous MOSFET will be turned off, protecting it from potentially damaging current levels. This SW threshold for reverse overcurrent detection can be reduced by placing a resistor in series with the SW pin, which sources a current when the SG pin is high. Note that the SG reverse overcurrent threshold and the SW pin source current are adjusted based on the state of the MODE pin. This is done to accommodate the use of either high voltage or low voltage MOSFETs, which normally have significantly different on resistances. In an overvoltage condition, the SG reverse overcurrent will override the overvoltage protection and force SG low, essentially regulating the reverse SG MOSFET current at a high level while the overvoltage condition persists. However, the SG reverse overcurrent is only active after the LTC3766 has achieved communication lock.

Finally, the REGSD pin can be used to limit the amount of time that the high voltage linear regulator controller is active. This is particularly useful when the LTC3766 is used standalone in a nonisolated forward converter. In this application, the pass device of the linear regulator controller may be dissipating considerable power. When the linear regulator controller is active, the REGSD pin sources a 13µA current. If a capacitor from REGSD to GND charges to a voltage greater than 1.21V, then linear regulator controller is disabled.

Gate Driver Mode Control

In addition to being used in conjunction with the LTC3765, the LTC3766 can also be used standalone in a nonisolated forward converter application. In this case, the MODE pin can be used to disable gate drive encoding by tying MODE to GND through either a 100k (for V_{CC} = 7V operation) or 50k (for V_{CC} = 8.5V operation) resistor. This causes a normal PWM signal to appear on PT^+ and a reference clock to appear on PT^-.

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Secondary-Side Bias and Start-Up

In most applications, the LTC3766 will receive its bias voltage from a supply that is generated on the secondary side. The manner in which the secondary bias is generated depends upon the output voltage as well as the variation in the input voltage of the DC/DC converter. In all applications, however, the secondary bias must always come up before the output reaches the regulation level. This is essential to avoid an overvoltage condition on the output, since the initial start-up is performed from the primary side in an open-loop fashion. See Generating the Secondary-Side Bias for more information.

Note that the LTC3766 will not begin a soft-start sequence and initiate switching until the RUN pin is high, adequate voltage is present on both the V_{IN} and V_{CC} pins, and switching is detected on the SW pin. The LTC3766 looks for switching on the SW pin to ensure that the LTC3765 is active and ready for control hand-off. For switching to be detected, the SW node waveform must have at least eight consecutive pulses in the range of 50kHz to 700kHz. The SW node waveform must also have a peak that is greater than 1.4V and a valley that is less than 0.5V. In standalone mode, the LTC3766 begins the soft-start sequence without waiting for a switching waveform to be detected on the SW pin.

Linear Regulator Operation

The LTC3766 contains two linear regulators that are used to regulate the available bias voltage down to a level suitable for driving MOSFETs. If the bias supply voltage is greater than 15V, then the high voltage linear regulator controller may be used. This makes use of an external N-type pass device. Place a capacitor of 0.22µF or greater on V_{IN} and 1µF or greater on V_{CC}. If the bias supply connected to the V_{IN} pin has a relatively high output impedance, it may be necessary to use a larger capacitor on V_{IN} to prevent the V_{IN} pin voltage from dropping when the V_{CC} capacitor is being charged. The V_{CC} charge rate during linear regulator start-up is set by the LTC3766 to approximately 0.5V/µs, which will create at charging current of $(0.5 \bullet 10^6)\ C_{VCC}$. Care should be taken to ensure that this charging current does not exceed the SOA of the N-type pass device, particularly when operating at higher V_{IN} voltages. The V_{CC} regulation level can be set to either 7V or 8.5V as desired using the MODE pin. See the section on V_{CC} and Drive Mode Selection for details.

The LTC3766 also contains a 15V internal bypass LDO. If the voltage on the V_{AUX} pin exceeds the V_{AUX} switchover threshold, then the high voltage linear regulator is disabled, and an internal PMOS-pass LDO uses the V_{AUX} voltage to supply power to V_{CC}. This allows the high voltage linear regulator to be used for initial start-up and the higher efficiency bypass LDO to be used during normal operation. Figure 3 illustrates such a configuration that uses both linear regulators.

If the voltage on the V_{AUX} pin is below the switchover threshold, then the V_{AUX} pin is internally loaded with a resistance of approximately 920Ω. This internal load is removed after the V_{AUX} regulator is enabled, and is used to ensure that the V_{AUX} supply is reasonably stiff before the bypass regulator is activated.

In some cases, it is desirable to use the high voltage linear regulator only briefly during start-up, so as to limit the temperature rise in the external pass device. To accomplish this, place a capacitor on the REGSD pin to ground (see Figure 3) such that:

$$C_{RSD} = \frac{t_{HVREG}(13\mu A)}{1.21V}$$

where t_{HVREG} is the time that the high voltage regulator will operate. When the high voltage regulator is operating, a 13µA current is sourced from the REGSD pin, and when it is shut down (e.g., the bypass regulator is active), a 3µA current is sinked into the REGSD pin. If the REGSD voltage exceeds 1.21V, the high voltage regulator

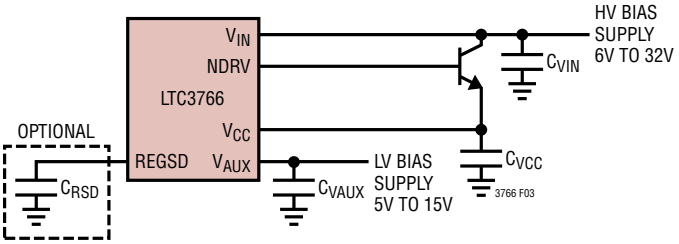

Figure 3. Typical Linear Regulator Connections

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is disabled. Choose a time t_{HVREG} that is greater than the normal start-up time. After start-up, if the voltage on the V_{AUX} pin drops, the high-voltage linear regulator will be re-energized, but only for a limited time.

When used with a bias supply that is between 5V and 10V, the V_{CC} pin can be directly connected to the bias supply as shown in Figure 4a. Note that the V_{IN} and NDRV pins must also be connected to the bias supply for proper operation of internal circuitry. When a bias supply between 6V and 15V is available, the V_{AUX} bypass linear regulator can be used standalone as shown in Figure 4b. In this case, proper start-up is assured by connecting the NDRV pin to V_{CC}. Since there is no external pass device on NDRV, however, the effective UVLO levels will be dictated by the V_{AUX} switchover thresholds instead of the V_{CC} UVLO thresholds. Rather than relying on the V_{AUX} thresholds, the start-up and shutdown levels are normally set by using the RUN pin to monitor the bias supply voltage as shown in Figure 4b. See the RUN Pin Operation section for details.

For applications where the available bias supply is greater than 30V, the LTC3766 also contains a current-limited 30V clamp on the V_{IN} pin. This clamp can sink up to 3.5mA

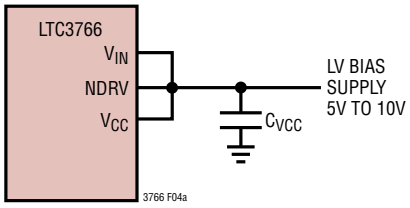

Figure 4a. No Linear Regulator Used

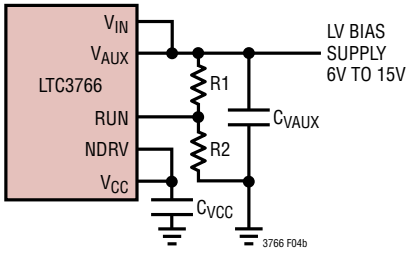

Figure 4b. V_{AUX} Regulator Used Standalone

to allow the V_{IN} pin to be used as a shunt regulator. This is especially useful in nonisolated applications where the LTC3766 is used standalone. See the Nonisolated Applications section for more information.

RUN Pin Operation

Normal operation is enabled when the voltage on RUN rises above its 1.22V threshold. As shown in Figure 5, the RUN pin can be used with an external resistor divider to enable the LTC3766 operation based on a sensed voltage V_X. In self-starting applications, V_X is normally either the converter output voltage (V_{OUT}) or a bias voltage. In

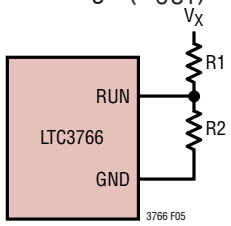

Figure 5. Using the RUN Pin to Determine Start-Up

nonisolated applications, V_X is normally the converter input voltage (V_{IN}). See Nonisolated Applications for more information on the use of the RUN pin in nonisolated applications.

A 3µA current is pulled into the RUN pin when it is below its threshold that, when combined with the value chosen for R1, increases the hysteresis beyond the internal amount of 4%. When used in this manner, the values for R1 and R2 can be calculated from the desired rising and falling V_X thresholds by the following equations:

$$R1 = \frac{V_{X(RISING)} - 1.043 \bullet V_{X(FALLING)}}{3\mu A}$$

$$R2 = \frac{1.17 \bullet R1}{V_{X(FALLING)} - 1.17}$$

In self-starting applications where the LTC3765 performs an open-loop soft-start, the voltage V_X can be tied to V_{OUT} of the converter ($V_X = V_{OUT}$) to inhibit the LTC3766 start-up until the output voltage is above a given level. This

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sets the exact output voltage at which soft-start control is handed off from primary to secondary. This hand-off output voltage should be set high enough so as to avoid pulse-skipping operation when the LTC3766 initially takes control. If excessive pulse skipping occurs in applications that use a peak charge circuit to generate bias voltage, this can cause the bias supply to fall, preventing proper start-up. To preclude this possibility, use the RUN pin to inhibit the LTC3766 start-up until the output voltage is at least:

$$V_{OUT(ON)} > 300ns \frac{N_S f_{SW} V_{IN(MAX)}}{N_P}$$

Note that in self-starting applications, direct RUN/STOP control should be handled only on the primary side using the LTC3765. If the LTC3765 gets disabled, the LTC3766 will sense that the primary side is no longer switching and automatically shut down. To avoid a possible output overvoltage, do not manually disable the LTC3766 unless the LTC3765 is also manually disabled.

If the RUN pin function is not needed, it can be tied directly to the V_{IN} pin.

Setting the Switching Frequency and Synchronization

The switching frequency of the LTC3766 is set using the FS/SYNC pin. This pin sources a 20µA current, and a resistor to ground on this pin sets the switching frequency to a value equal to:

$$f_{SW} = 4R_{FS}$$

Alternatively, the FS/SYNC pin can be tied to V_{CC}, which sets the switching frequency to a fixed value of 275kHz. In general, a higher switching frequency will result in a smaller size for inductors and transformers, but at the cost of reduced efficiency. Although the LTC3766 can operate from 75kHz to 500kHz, the best balance between efficiency and size for a forward converter is found when operating between 150kHz and 350kHz.

If a clock signal (>2V) is detected at the FS pin, the LTC3766 will automatically synchronize to the falling edge of this signal. Table 1 summarizes the operation of the FS/SYNC pin.

Table 1

FS/SYNC PIN	SWITCHING FREQUENCY
V_{CC}	275kHz
R_{FS} to GND	$f_{SW} = 4R_{FS}$
Reference Clock	$f_{SW} = f_{REF}$ (100kHz to 500kHz)

In PolyPhase applications, synchronization can be achieved by tying the PT⁻ pin of the master to the FS/SYNC pin of each slave. The relative phase delay of each slave is set using the PHASE pin. Any one of five preset values can be selected as shown in Table 2. Note that the phase delay is relative to the falling edge of the incoming reference clock on the FS/SYNC pin, since the falling edge of PT⁻ corresponds to the beginning of the PWM cycle.

Table 2

PHASE PIN	PHASE DELAY	APPLICATION
GND	180°	2-Phase and 4-Phase
25k to GND	240°	3-Phase
50k to GND	120°	3-Phase
100k to GND	90°	4-Phase
100k to V_{CC}	270°	4-Phase

In general, the external synchronizing clock should be present before the LTC3766 is enabled, so that the switching frequency has stabilized before the gate drivers begin switching. In some applications, however, it may be necessary to synchronize the LTC3766 after it has begun switching. In this case, the circuit in Figure 6 can be used.

Using the circuit Figure 6, the LTC3766 will run at 275kHz until the 3.3V – 5V amplitude synchronization signal V_{SYNC} begins toggling. This circuit creates a 100ns low-pulse at the FS/SYNC pin, which ensures a smooth transition into synchronization. As shown in Figure 6, the V_{CC} pin can

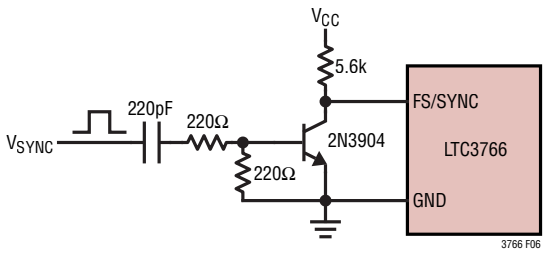

Figure 6. Synchronization After LTC3766 Start-Up

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normally be used to provide the pull-up voltage, which must be between 5V and 12V. In addition, the rise time of the voltage on the FS/SYNC pin must be less than 200ns. Consequently, parasitic capacitance on the FS/SYNC pin must be minimized.

Once the LTC3766 has been synchronized, do not remove the external synchronizing clock unless the LTC3766 is also shut down. Removal of the external clock after synchronization will result in operation at low frequencies for a period of time, which can lead to very high currents in external power components.

Setting the Output Voltage

The LTC3766 output voltage is set by an external feedback resistor divider placed across the output as shown in Figure 7. The regulated output voltage is determined by:

$$V_{OUT} = 0.6V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

Be careful to keep these divider resistors very close to the FB pin to minimize the trace length and noise pick-up on the sensitive FB signal. Using a low resistance (<2k) for the output voltage divider also minimizes noise on the FB pin. If the remote sense amplifier is used, then the divider should be placed between the V_{SOUT} pin and GND. See the Remote Sensing section for details.

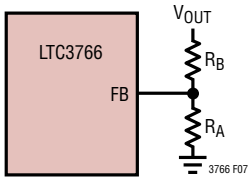

Figure 7. Setting the Output Voltage

Selecting the Main Transformer

The job of the transformer in a forward converter is to step the voltage either up or down while providing isolation between the primary and secondary grounds. Ideally, this transformer would not store any energy (it would have infinite magnetizing inductance). Note that this objective is very different from that of the transformer used in a flyback converter. The transformer used in a flyback converter is really a coupled inductor, the purpose of which is to store energy during the primary-side on time and then deliver it to the secondary during the off-time. In a forward converter, by contrast, the power is transferred during the primary-side on-time, and the off-time is used to recover the small amount of energy that was inadvertently stored in the core of the transformer.

For nearly all applications, an off-the-shelf transformer can be selected. Transformers using planar winding technology are widely available and are a good choice for minimizing leakage inductance as well as component height. There are two basic items to consider in selecting an appropriate family of off-the-shelf transformers: 1) the isolation requirements and 2) the power level requirements. If the application circuit has specific isolation requirements, choose a family of transformers whose isolation level satisfies that requirement. In addition to an isolation voltage rating, the application may require a transformer with certification from a particular agency, or it may require a specific type of isolation (e.g., basic or functional). In terms of power level, choose a family of transformers whose rated power level exceeds that of the required amount of output power. Be careful to allow for room to "grow," as the power requirements of many electronic systems tend to increase throughout development.

Once a family of transformers has been selected, the next step is to choose a suitable transformer from within that family. This mainly consists of choosing the correct number of primary and secondary turns (N_P and N_S). The value of N_S can be calculated from:

$$N_S = \frac{10^8 V_{OUT}}{f_{SW} A_C B_M}$$

where A_C is the cross-sectional area of the core in cm^2 (as normally given in the transformer data sheet) and B_M is the maximum AC flux density desired. For the Pulse PA08xx series power transformers used in the Typical Applications

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section, $A_C = 0.59cm^2$. For the Pulse PA09xx series power transformers, $A_C = 0.81cm^2$. For the Champs-Tech G45 and PQ26 power transformers, $A_C = 0.55cm^2$ and $A_C = 1.21cm^2$ respectively. Most high frequency transformers use a ferrite core material. Consequently, selecting a maximum AC flux density of 2000 gauss is normally a good starting point, provided that the switching frequency is between 150kHz and 350kHz. This value of B_M leaves headroom during transients and avoids excessive core losses. Note that the choice of B_M together with switching frequency will determine the amount of core loss for a given transformer. Consult the transformer data sheet to evaluate the resulting core loss and temperature rise. In some cases, it may be necessary to increase N_S somewhat in order to reduce B_M and the associated temperature rise. In all cases, be sure to stay well below the saturation flux density of the transformer core.

Once the value of has N_S been selected, the required transformer turns ratio can be calculated from

$$\frac{N_P}{N_S} = \frac{D_{MAX} V_{IN(MIN)}}{V_{OUT}}$$

where $V_{IN(MIN)}$ is the minimum input voltage and D_{MAX} is the maximum duty cycle. Although the LTC3766 has a maximum duty cycle of 79% (D_{MAX} = 0.79), normally a lower value of D_{MAX} is chosen in the above equation so that there is duty cycle headroom to accommodate load transients when operating at minimum input voltage. A value for D_{MAX} of 0.65 to 0.70 is appropriate for most applications.

Having selected a particular transformer, calculate the copper losses associated with the transformer winding. These losses are highest when operating at maximum duty cycle and full load. However, it is better to evaluate copper losses at the nominal operating point of 50% duty cycle, where the losses are approximately:

$$P_{CU} = \frac{(I_{MAX})^2}{2}\left(R_{SEC} + \left(\frac{N_S}{N_P}\right)^2 R_{PRI}\right)$$

where R_{PRI} and R_{SEC} are the primary and secondary winding resistances respectively, and I_{MAX} is the maximum output current. An optimal transformer design has a reasonable balance between copper and core losses. If they are significantly different, then adjust the number of secondary turns (and recalculate the needed turns ratio) to achieve such a balance.

Inductor Value Calculation

The selection of an output inductor is essentially the same as for a buck converter. For a given input and output voltage, the inductor value and operating frequency determine the ripple current. The ripple current ΔI_L increases with higher V_{IN} and decreases with higher inductance:

$$\Delta I_L = \frac{V_{OUT}}{f_{SW} L}\left(1 - \frac{V_{OUT}}{V_{IN}} \bullet \frac{N_P}{N_S}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. Note that a lower inductance can improve transient response and help to reduce the flux swing seen by the main transformer. A reasonable starting point for setting the ripple current is $\Delta I_L = 0.4(I_{OUT(MAX)})$ for nominal V_{IN}. The maximum ΔI_L occurs at the maximum input voltage.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of the more expensive ferrite cores. Actual core loss is essentially independent of core size for a fixed inductor value but it is very dependent on the inductance selected. As the inductance increases, core losses decrease. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core losses and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates “hard,” which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

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Active Clamp Capacitor

The active clamp capacitor, C_{CL}, stores the average reset voltage of the transformer over many cycles. The voltage on the clamp capacitor is generated by the transformer core reset current, and will intrinsically adjust to the optimal reset voltage regardless of other parameters. The voltage across the capacitor at full load is approximately given by:

$$V_{CL} = \frac{V_{IN}^2}{V_{IN} - 1.15\left(V_{OUT} \bullet \frac{N_P}{N_S}\right)}$$

N_P/N_S is the main transformer turns ratio. The factor of 1.15 accounts for typical losses and delays. When PG and AG on the LTC3765 are low, the bottom side of the clamp capacitor is grounded, placing the reset voltage, V_{CL}, on the SWP node. When PG and AG are high, the top side of the capacitor is grounded, and the voltage on the bottom side of the capacitor is $-V_{CL}$. Therefore the voltage seen on the capacitor is also the voltage seen at the drains of the PG and AG MOSFETs.

As shown in Figure 8, the V_{CL} voltage has a minimum when the converter is operating at 50%. For a given range on V_{IN}, therefore, the maximum clamp voltage ($V_{CL(MAX)}$) will occur either at the minimum or maximum V_{IN}, depending on which input voltage causes the converter to operate furthest from 50% duty cycle. The maximum V_{CL} voltage can be determined by substituting the maximum and minimum values of V_{IN} into this equation and selecting the larger of the two. In order to leave room for overshoot, choose a capacitor whose voltage rating is greater than this maximum V_{CL} voltage by 50% or more. Typically, a good quality (X7R) ceramic capacitor is a good choice for C_{CL}. Also, be sure to account for the voltage coefficient of the capacitor. Many ceramic capacitors will lose as much as 50% of their value at their rated voltage.

The value of the clamp capacitor should be high enough to minimize the capacitor ripple voltage, thereby reducing the voltage stress seen by the MOSFETs. However, a larger clamp capacitor will ultimately result a slower transient response to avoid transformer saturation during load transients. While Direct Flux Limit will automatically limit the PWM on-time only as needed to prevent saturation, a larger clamp capacitor will require a longer time to charge or discharge in response to a load transient. Consequently, the value of the clamp capacitor represents a compromise between transient response and MOSFET voltage stress. A reasonable value for the clamp capacitor can be calculated using the following:

$$C_{CL} = \frac{1}{2L_M} \bullet \left(\frac{4}{2\pi f_{SW}}\right)^2$$

An additional design constraint on C_{CL} occurs because of the resonance between the magnetizing inductance L_M of the main transformer and the clamp capacitor C_{CL}. If the Q of this resonance is too high, it will result in increased voltage stress on the primary-side MOSFET during load

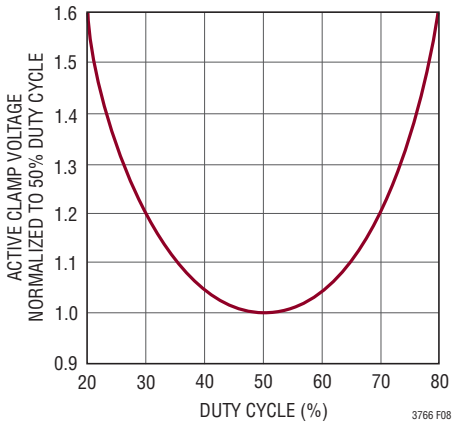

Figure 8. V_{CL} Voltage vs Duty Cycle

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transients. Also, a high Q resonance between L_M and C_{CL} complicates the compensation of the voltage loop, and can cause oscillations under certain conditions. **To avoid the problems associated with this resonance, always use an RC snubber in parallel with the clamp capacitor as shown in Figure 9.** The values for this RC snubber can then be calculated using:

$$R_{CS} = \frac{1}{1-\left(\frac{V_O}{V_{IN(MIN)}} \bullet \frac{N_P}{N_S}\right)} \sqrt{\frac{L_M}{C_{CL}}}$$

and

$$C_{CS} = 6C_{CL}$$

Figure 9 shows a typical arrangement of the active clamp capacitor with an RC snubber. Be careful to account for the effect of voltage coefficient for both C_{CS} and C_{CL} to ensure that the above relationship between C_{CS} and C_{CL} is maintained.

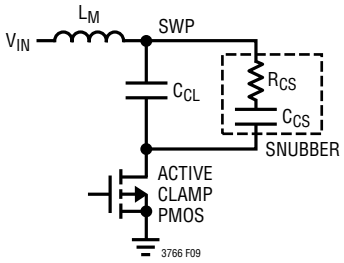

Figure 9. Active Clamp Capacitor and Snubber

Direct Flux Limit

In active clamp forward converters, it is essential to establish an accurate limit to the transformer flux density in order to avoid core saturation during load transients or when starting up into a pre-biased output. The LTC3765 and LTC3766 implement a new unique system for monitoring and directly limiting the flux accumulation in the transformer core. Unlike previous methods, the Direct Flux Limit directly measures and monitors flux accumulation and guarantees that the transformer will not saturate in either direction, even when starting into a pre-biased output. This technique also provides the best possible transient response, as it will temporarily allow very high duty cycles, only limiting the duty cycle when absolutely necessary. Moreover, this technique prevents overcurrent damage to the active clamp PMOS, which is a potentially significant weakness in many active clamp forward converter designs.

Since the Direct Flux Limit functionality is implemented in the LTC3765 on the primary side, there is nothing to adjust on the secondary side. See the LTC3765 data sheet for details on using this feature. Note that if the LTC3765 terminates the PG MOSFET on-time prematurely to limit flux accumulation, the LTC3766 will sense a premature falling on the SW node. In response, the LTC3766 will automatically terminate the FG on-time, thereby allowing the transformer core to reset. A premature falling on the SW node will also occur whenever the LTC3765 has shut down for any reason. Consequently, if the LTC3766 detects 19 consecutive premature SW node falling edges on the SW pin, it will generate a lock fault and shut down.

Primary-Side Power MOSFET Selection

On the primary side, the peak-to-peak drive levels for both the N-channel main switch and the P-channel active clamp switch are determined by the voltage on the V_{CC} pin of the LTC3765. This voltage is normally provided through the pulse transformer, and is typically set in the range of 8.5V to 12V. Note that even in applications where a logic-level MOSFET may be used on the primary side, the V_{CC} voltage on the LTC3765 must still be in this range for proper operation.

Selection of the N-channel MOSFET involves careful consideration of the requirements for breakdown voltage (BV_{DSS}) and maximum drain current, while balancing the losses associated with the on-resistance and parasitic capacitances. In an active clamp topology, the maximum drain voltage seen by this MOSFET is approximately:

$$V_{DS(PG)} = 1.2 \bullet V_{CL(MAX)}$$

where $V_{CL(MAX)}$ is the maximum active clamp voltage given above in the Active Clamp Capacitor section. The factor

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of 1.2 has been added to allow margin for ringing and ripple on the clamp capacitor. It is important to select the lowest possible voltage rating for this MOSFET in order to maximize efficiency. Note that the RC snubber on the active clamp capacitor (see Figure 10) reduces the peak voltage stress on the primary-side MOSFET without adding to operating losses. Also, the leakage inductance of the main transformer at full load can cause considerable ripple on the active clamp capacitor, pushing up the peak voltage stress seen by the primary-side MOSFET. This ripple can be reduced by using a larger active clamp capacitor and a proportionally larger RC snubber capacitor. See Active Clamp Capacitor section for more information.

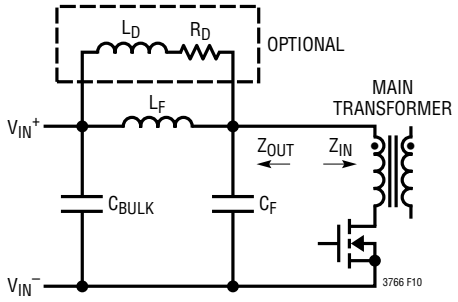

Figure 10. Input Filter with Optional Damping Network

Once the required BV_{DSS} of the N-channel MOSFET is known, choose a MOSFET with the lowest available on-resistance ($R_{DS,ON}$) that has been optimized for switching applications (low Q_G). In most applications, the MOSFET will be used at a drain current that is a fraction of the maximum rated current, so this rating is not normally a consideration. The total losses associated with the N-channel MOSFET at maximum output current can be estimated using:

$$P_{PG} = \left(\frac{N_S}{N_P}\right)\frac{V_{OUT}(I_{MAX})^2}{V_{IN}}(1+\delta)R_{DS(ON)} + \left(\frac{N_S}{N_P}\right)\frac{V_{CL}I_{MAX}R_{DR}Q_{GD}f_{SW}}{2V_{MILLER}} + Q_{GTOT}V_{CC}f_{SW}$$

where δ is the temperature dependence of the on-resistance and V_{CL} is the active clamp voltage (see Active Clamp Capacitor section). R_{DR} (approximately 1.7Ω for the LTC3765) is the gate drive output resistance at the MOSFET's miller plateau voltage, V_{MILLER}. The values of Q_{DG}, Q_{GTOT} and V_{MILLER} can be taken from the V_{GS} versus Q_G curve that is typically provided in a MOSFET data sheet. Q_{GD} is the change in gate charge (Q_G) during the region where the V_{GS} voltage is approximately constant and equal to miller voltage, V_{MILLER}. The total gate charge (Q_{GTOT}) is the gate charge when $V_{GS} = V_{CC}$. The three parts in the above equation represent conduction losses, transition losses and gate drive losses respectively. Highest efficiency is obtained by selecting a MOSFET that achieves a balance between conduction losses and the sum of transition and gate drive losses. Note that the above equation for P_{PG} is an approximation that includes assumptions. First, it is assumed that the turn-on transition losses are relatively small because of the leakage inductance in the main transformer. Also, it is assumed that the energy stored in this leakage inductance at primary-switch turn-off is completely recovered by the active clamp capacitor. For most applications, these assumptions are valid and the above equation is a good approximation.

The active clamp P-channel MOSFET has the same BV_{DSS} requirement as that of the N-channel MOSFET. Since the P-channel MOSFET only handles the magnetizing current, it is normally much smaller (typically a SOT package). To accommodate abnormal transients, use a P-channel MOSFET that has a pulsed drain current rating of 2A or higher. Also, note that when the N-channel MOSFET turns off, the leakage inductance will momentarily force the reflected load current into the body diode of the P-channel MOSFET. Consequently, the body diode should be rated to handle a pulsed forward current of:

$$I_{D(MAX)} = \left(\frac{N_S}{N_P}\right)I_{MAX}$$

In some cases, it may be more practical to add a separate diode in parallel with the body diode of the P-channel MOSFET.