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60V Low I_Q Synchronous Boost Controller

FEATURES

- **Synchronous Operation for Highest Efficiency and Reduced Heat Dissipation**
- **Wide V_{IN} Range: 4.5V to 60V (65V Abs Max); Operates Down to 2.3V After Start-Up**
- **Output Voltage Up to 60V**
- **±1% 1.200V Reference Voltage**
- **R_{SENSE} or Inductor DCR Current Sensing**
- **100% Duty Cycle Capability for Synchronous MOSFET**
- **Low Quiescent Current: 28µA**
- Phase-Lockable Frequency (75kHz to 850kHz)
- Programmable Fixed Frequency (50kHz to 900kHz)
- Power Good Output Voltage Monitor
- Low Shutdown Current: 4µA
- Internal LDO Powers Gate Drive from VBIAS or $EXTV_{CC}$
- Thermally Enhanced Low Profile 24-Pin 4mm × 4mm QFN Package and 20-Lead TSSOP Package

APPLICATIONS

- Industrial
- Automotive
- Medical
- Military

DESCRIPTION

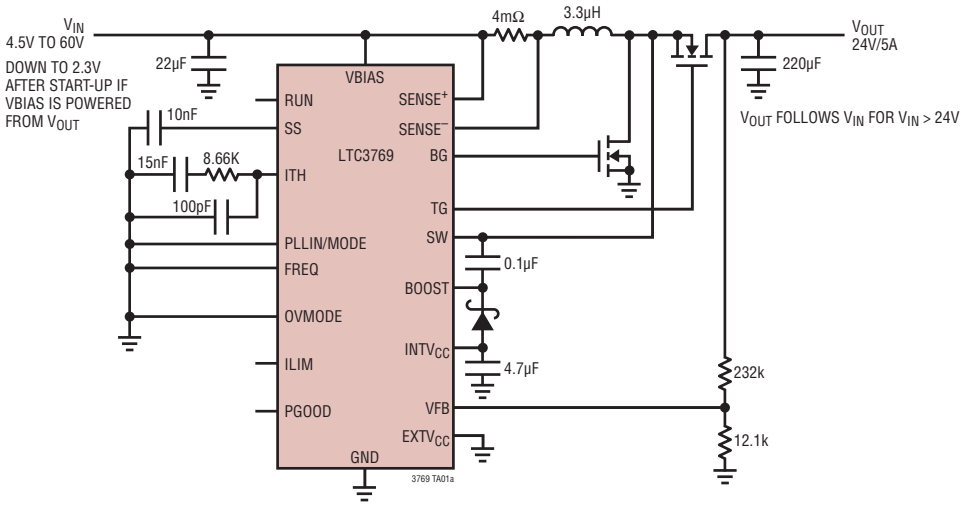
The LTC®3769 is a high performance single output synchronous boost converter controller that drives an all N-channel power MOSFET stage. Synchronous rectification increases efficiency, reduces power losses and eases thermal requirements, simplifying high power boost applications. The 28µA no-load quiescent current extends operating run time in battery-powered systems.

A 4.5V to 60V input supply range encompasses a wide range of system architectures and battery chemistries. When biased from the output of the boost converter or another auxiliary supply, the LTC3769 can operate from an input supply as low as 2.3V after start-up. The operating frequency can be set within a 50kHz to 900kHz range or synchronized to an external clock using the internal PLL.

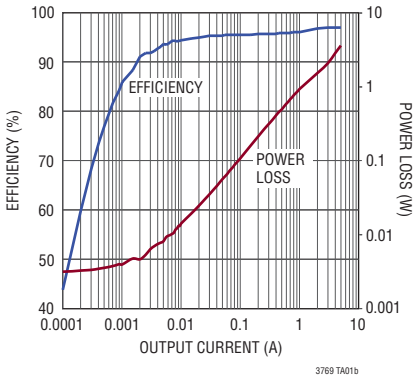
The SS pin ramps the output voltage during start-up. The PLLIN/MODE pin selects Burst Mode® operation, pulse-skipping mode or forced continuous mode at light loads.

TYPICAL APPLICATION

120W, 12V to 24V/5A Synchronous Boost Converter



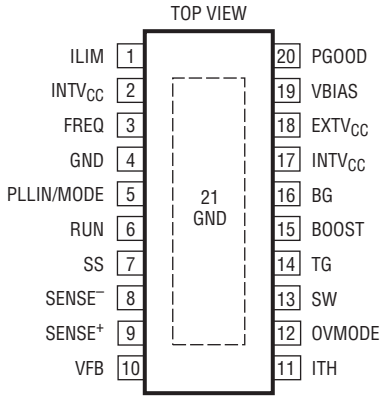
Efficiency and Power Loss vs Output Current



ABSOLUTE MAXIMUM RATINGS (Notes 1, 3)

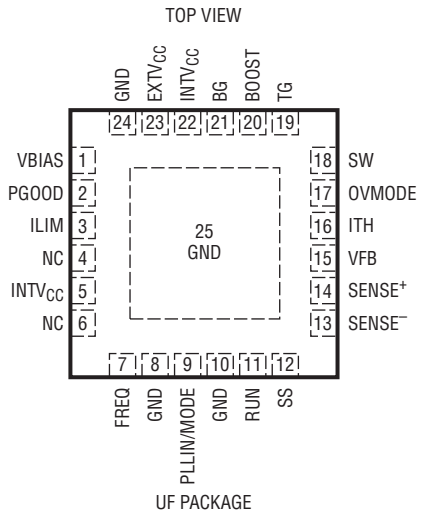
VBIAS ..... –0.3V to 65V
BOOST ..... –0.3V to 71V
SW ..... –5V to 65V
RUN ..... –0.3V to 8V
Maximum Current Sourced into Pin
From Source >8V 100µA
PGOOD, PLLIN/MODE ..... –0.3V to 6V
$INTV_{CC}$, (BOOST - SW) ..... –0.3V to 6V
$EXTV_{CC}$ ..... –0.3V to 14V
$SENSE^+$, $SENSE^-$ ..... –0.3V to 65V
($SENSE^+$ - $SENSE^-$) ..... –0.3V to 0.3V
ILIM, SS, ITH, FREQ, PHASMD, VFB ..... –0.3V to $INTV_{CC}$
Operating Junction Temperature
Range (Note 2) ..... –55°C to 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) SSOP ..... 300°C

PIN CONFIGURATION



FE PACKAGE
20-LEAD PLASTIC TSSOP

T_{JMAX} = 150°C, θ_{JA} = 38°C/W
EXPOSED PAD (PIN 21) IS GND, MUST BE SOLDERED TO PCB



UF PACKAGE
24-LEAD (4mm × 4mm) PLASTIC QFN

T_{JMAX} = 150°C, θ_{JA} = 47°C/W
EXPOSED PAD (PIN 25) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3769EUF#PBF	LTC3769EUF#TRPBF	3769	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3769IUF#PBF	LTC3769IUF#TRPBF	3769	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 125°C
LTC3769HUF#PBF	LTC3769HUF#TRPBF	3769	24-Lead (4mm × 4mm) Plastic QFN	–40°C to 150°C
LTC3769MPUF#PBF	LTC3769MPUF#TRPBF	3769	24-Lead (4mm × 4mm) Plastic QFN	–55°C to 150°C
LTC3769EFE#PBF	LTC3769EFE#TRPBF	LTC3769FE	20-Lead Plastic SSOP	–40°C to 125°C
LTC3769IFE#PBF	LTC3769IFE#TRPBF	LTC3769FE	20-Lead Plastic SSOP	–40°C to 125°C
LTC3769HFE#PBF	LTC3769HFE#TRPBF	LTC3769FE	20-Lead Plastic SSOP	–40°C to 150°C
LTC3769MPFE#PBF	LTC3769MPFE#TRPBF	LTC3769FE	20-Lead Plastic SSOP	–55°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, VBIAS = 12V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
VBIAS	Chip Bias Voltage Operating Range			4.5		60	V
V_{IN}	SENSE Pins Common Mode Range (BOOST Converter Input Supply Voltage)			2.3		60	V
V_{OUT}	Regulated Output Voltage Range			V_{IN}		60V	V
V_{FB}	Regulated Feedback Voltage	I_{TH} = 1.2V (Note 4)	●	1.188	1.200	1.212	V
	Feedback Current	(Note 4)			±5	±50	nA
	Reference Line Voltage Regulation	VBIAS = 6V to 60V			0.002	0.02	%/V
	Output Voltage Load Regulation (Note 4)	Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V	●		0.01	0.1	%
		Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2V	●		–0.01	–0.1	%
	Error Amplifier Transconductance	I_{TH} = 1.2V			2		mmho
I_Q	Input DC Supply Current (VBIAS Pin) Pulse-Skipping or Forced Continuous Mode Sleep Mode Shutdown	(Note 5) RUN = 5V; V_{FB} = 1.25V (No Load) RUN = 5V; V_{FB} = 1.25V (No Load) RUN = 0V			 0.9 28 4	 45 10	 mA µA µA
	SW Pin Current	V_{SW} = 12V; V_{BOOST} = 16.5V; FREQ = 0V, Forced Continuous or Pulse-Skipping Mode			700		µA
UVLO	$INTV_{CC}$ Undervoltage Lockout Thresholds	V_{INTVCC} Ramping Up V_{INTVCC} Ramping Down	● ●	 3.6	4.1 3.8	4.3 	V V
V_{RUN}	RUN Pin ON Threshold	V_{RUN} Rising	●	1.18	1.28	1.38	V
	RUN Pin Hysteresis				100		mV
	RUN Pin Hysteresis Current	V_{RUN} > 1.28V			4.5		µA
	RUN Pin Current	V_{RUN} < 1.28V			0.5		µA
	Soft-Start Charge Current	V_{SS} = GND		7	10	13	µA
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 1.1V, I_{LIM} = $INTV_{CC}$ V_{FB} = 1.1V, I_{LIM} = Float V_{FB} = 1.1V, I_{LIM} = GND	● ● ●	90 68 42	100 75 50	110 82 56	mV mV mV
	$SENSE^+$ Pin Current	V_{FB} = 1.1V, I_{LIM} = Float			200	300	µA
	$SENSE^-$ Pin Current	V_{FB} = 1.1V, I_{LIM} = Float				±1	µA
	Top Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Top Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Bottom Gate Rise Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Bottom Gate Fall Time	C_{LOAD} = 3300pF (Note 6)			20		ns
	Top Gate Pull-Up Resistance				1.2		Ω
	Top Gate Pull-Down Resistance				1.2		Ω
	Bottom Gate Pull-Up Resistance				1.2		Ω
	Bottom Gate Pull-Down Resistance				1.2		Ω
	Top Gate Off to Bottom Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			30		ns
	Bottom Gate Off to Top Gate On Switch-On Delay Time	C_{LOAD} = 3300pF (Each Driver)			30		ns
	Maximum BG Duty Factor				96		%
$t_{ON(MIN)}$	Minimum BG On-Time	(Note 7)			110		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C, VBIAS = 12V, unless otherwise noted (Note 2).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$INTV_{CC}$ Linear Regulator							
	Internal V_{CC} Voltage	6V < V_{BIAS} < 60V, V_{EXTVCC} = 0		5.2	5.4	5.6	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 50mA			0.5	2	%
	Internal V_{CC} Voltage	6V < V_{EXTVCC} < 13V		5.2	5.4	5.6	V
	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 40mA, V_{EXTVCC} = 8.5V			0.5	2	%
	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.8	5	V
	$EXTV_{CC}$ Hysteresis				250		mV
Oscillator and Phase-Locked Loop							
	Programmable Frequency	R_{FREQ} = 25k R_{FREQ} = 60k R_{FREQ} = 100k		335	105 400 760	465	kHz kHz kHz
f_{LOW}	Lowest Fixed Frequency	V_{FREQ} = 0V		320	350	380	kHz
	Highest Fixed Frequency	V_{FREQ} = $INTV_{CC}$		488	535	585	kHz
	Synchronizable Frequency	PLLIN/MODE = External Clock	●	75		850	kHz
PGOOD Output							
	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.2	0.4	V
	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
	PGOOD Trip Level	V_{FB} with Respect to Set Regulated Voltage V_{FB} Ramping Negative Hysteresis		 –12	 –10 2.5	 –8	 % %
		V_{FB} Ramping Positive Hysteresis		8	10 2.5	12	% %
	PGOOD Delay	PGOOD Going High to Low			45		µs
	OV Protection Threshold	V_{FB} Ramping Positive, OVMODE = 0V		1.296	1.32	1.344	V
BOOST Charge Pump							
	BOOST Charge Pump Available Output Current	V_{SW} = 12V; V_{BOOST} – V_{SW} = 4.5V; FREQ = 0V, Forced Continuous or Pulse-Skipping Mode			55		µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3769 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTC3769E is guaranteed to meet specifications from 0°C to 85°C junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3769I is guaranteed over the –40°C to 125°C operating junction temperature range, the LTC3769H is guaranteed over the –40°C to 150°C operating temperature range and the LTC3769MP is tested and guaranteed over the full –55°C to 150°C operating junction temperature range. High junction temperatures degrade operating lifetimes; operating lifetime is derated for junction temperatures greater than 125°C. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula: $T_J = T_A + (P_D \bullet \theta_{JA})$, where θ_{JA} = 47°C/W for the QFN package and θ_{JA} = 38°C/W for the TSSOP package.

Note 3: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 4: The LTC3769 is tested in a feedback loop that servos V_{FB} to the output of the error amplifier while maintaining I_{TH} at the midpoint of the current limit range.

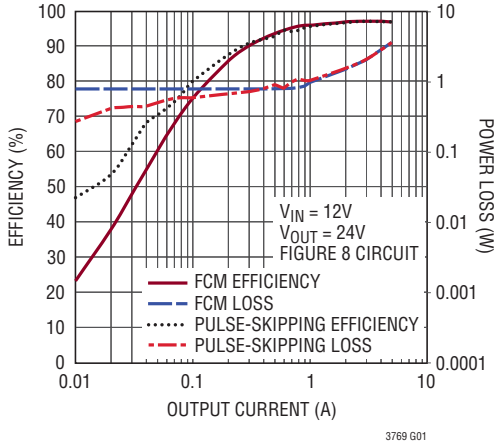
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

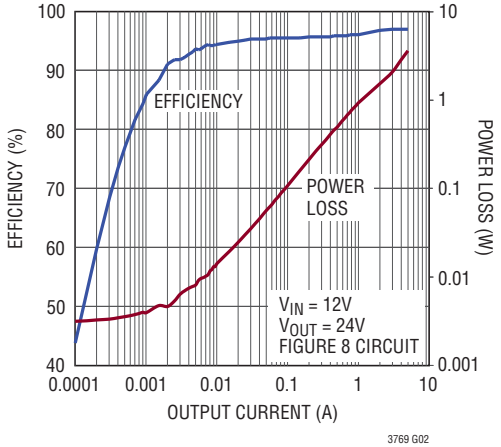
Note 7: See Minimum On-Time Considerations in the Applications Information section.

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

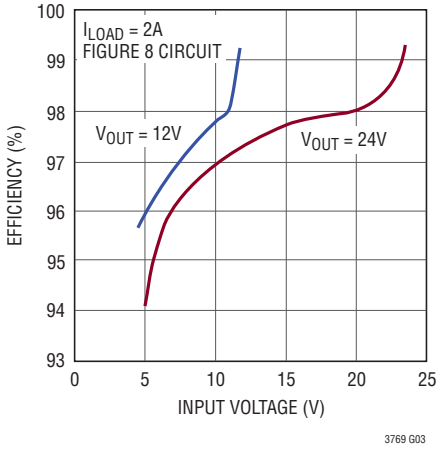
Efficiency and Power Loss vs Output Current



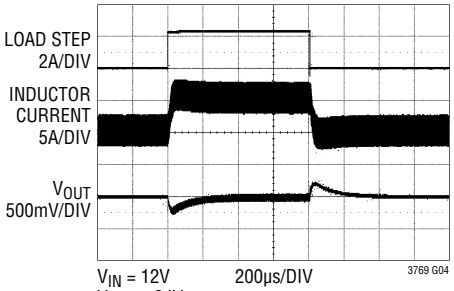
Efficiency and Power Loss vs Output Current



Efficiency vs Input Voltage

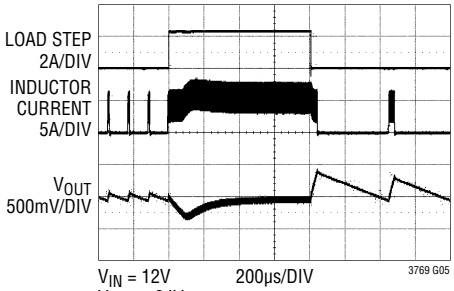


Load Step Forced Continuous Mode



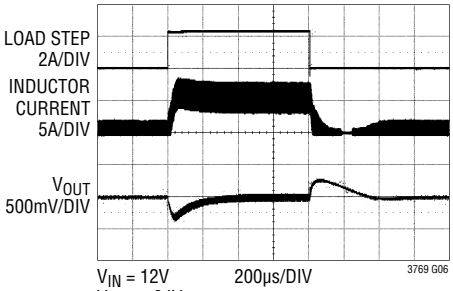
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Load Step Burst Mode Operation



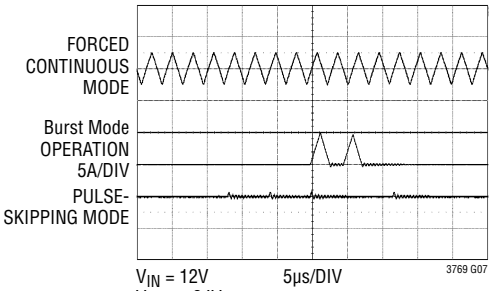
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Load Step Pulse-Skipping Mode



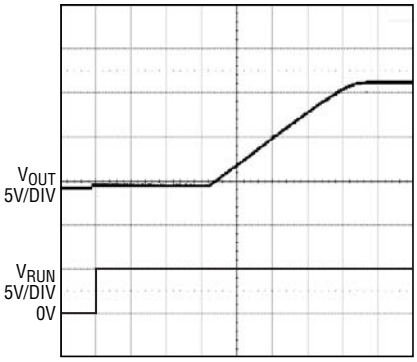
VIN = 12V 200µs/DIV
VOUT = 24V
LOAD STEP FROM 200mA TO 2.5A
FIGURE 8 CIRCUIT

Inductor Currents at Light Load



VIN = 12V 5µs/DIV
VOUT = 24V
ILOAD = 200µA
FIGURE 8 CIRCUIT

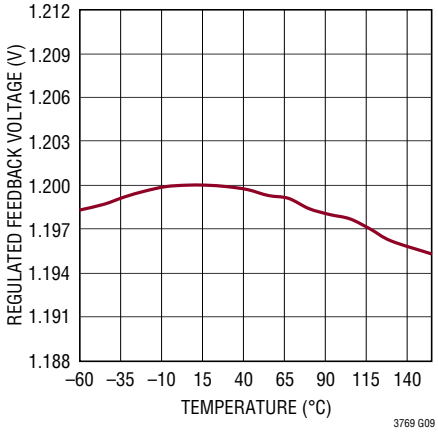
Soft Start-Up



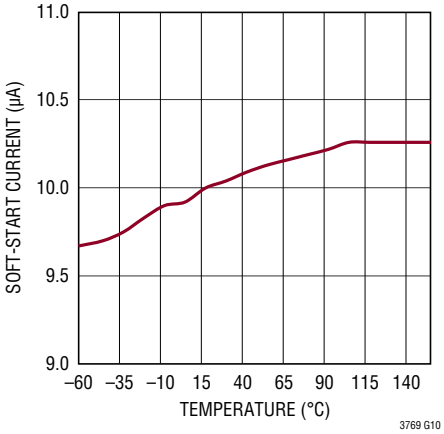
VIN = 12V 20ms/DIV
VOUT = 24V
FIGURE 8 CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

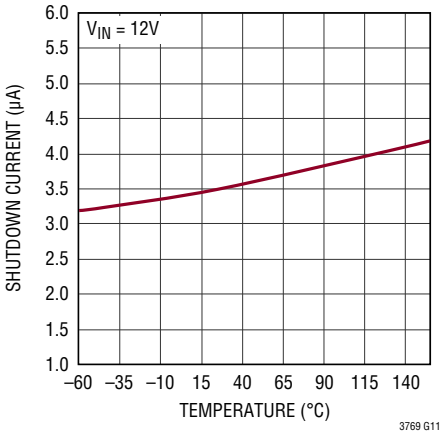
Regulated Feedback Voltage vs Temperature



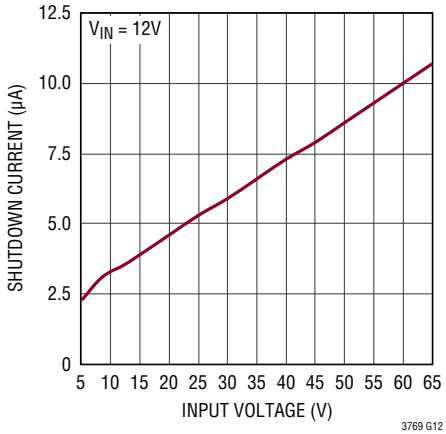
Soft-Start Pull-Up Current vs Temperature



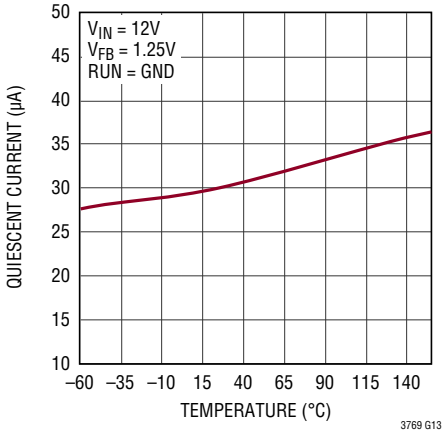
Shutdown Current vs Temperature



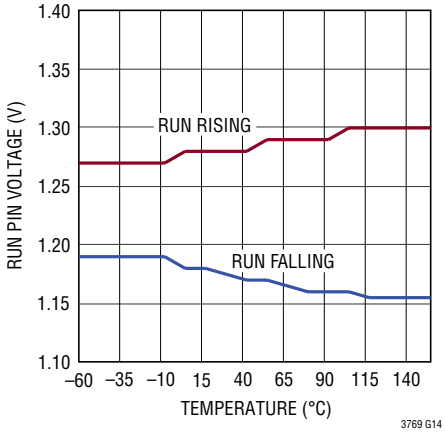
Shutdown Current vs Input Voltage



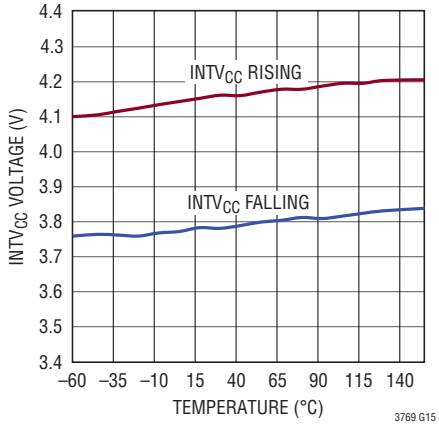
Quiescent Current vs Temperature



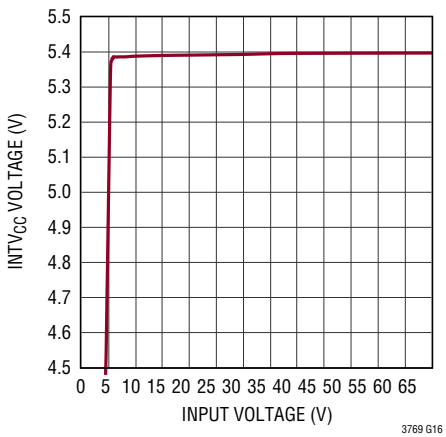
Shutdown (RUN) Threshold vs Temperature



Undervoltage Lockout Threshold vs Temperature

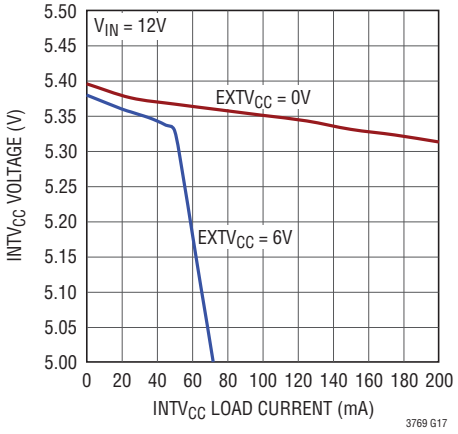


$INTV_{CC}$ Line Regulation



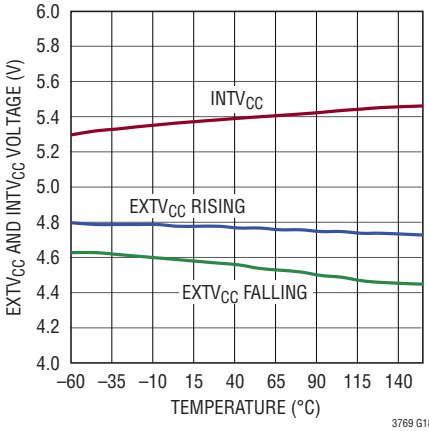
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

$INTV_{CC}$ vs $INTV_{CC}$ Load Current



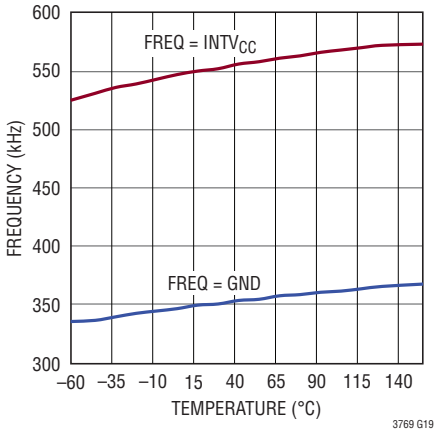
3769 G17

$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature



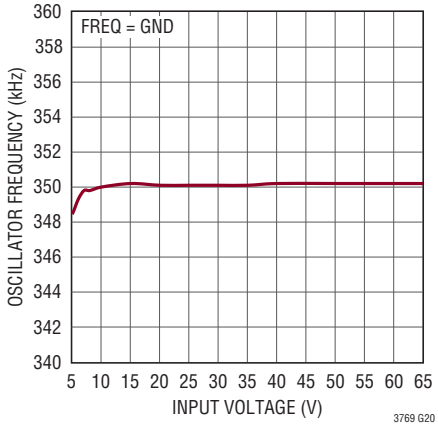
3769 G18

Oscillator Frequency vs Temperature



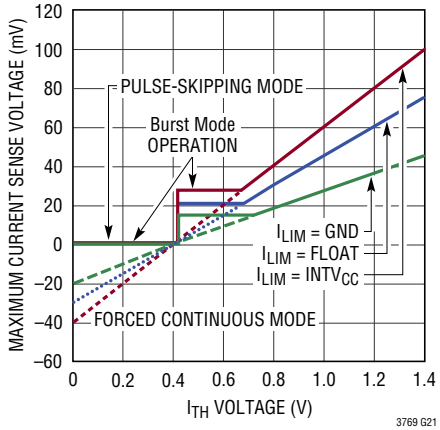
3769 G19

Oscillator Frequency vs Input Voltage



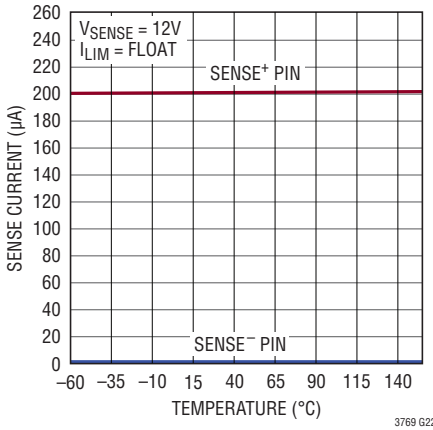
3769 G20

Maximum Current Sense Threshold vs I_{TH} Voltage



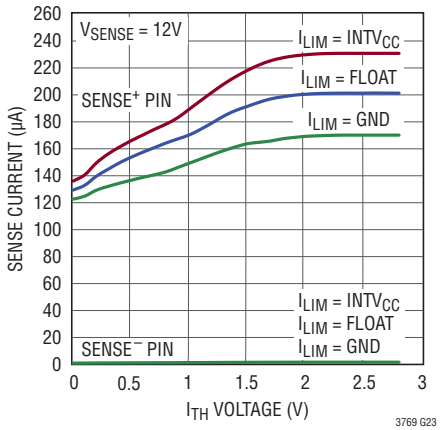
3769 G21

SENSE Pin Input Current vs Temperature



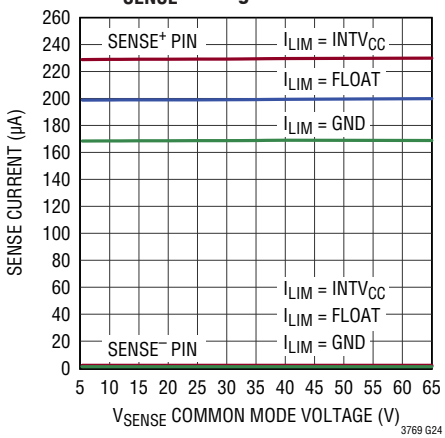
3769 G22

SENSE Pin Input Current vs I_{TH} Voltage



3769 G23

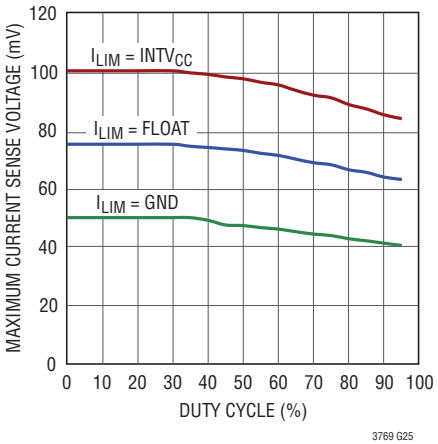
SENSE Pin Input Current vs V_{SENSE} Voltage



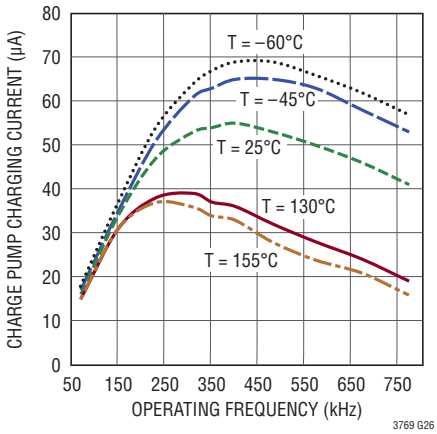
3769 G24

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

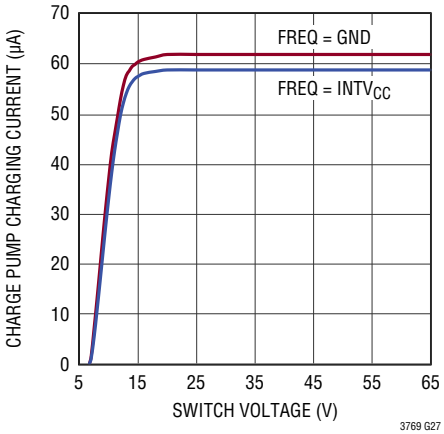
Maximum Current Sense Threshold vs Duty Cycle



Charge Pump Charging Current vs Operating Frequency



Charge Pump Charging Current vs Switch Voltage



PIN FUNCTIONS (QFN/TSSOP)

VBIAS (Pin 1/Pin 19): Main Supply Pin. It is normally tied to the input supply V_{IN} or to the output of the boost converter. A bypass capacitor should be tied between this pin and the signal ground pin. The operating voltage range on this pin is 4.5V to 60V (65V abs max).

PGOOD (Pin 2/Pin 20): Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is more than ±10% away from the regulated output voltage. To avoid false trips the output voltage must be outside the range for 45µs before this output is activated.

ILIM (Pin 3/Pin 1): Current Comparator Sense Voltage Range Input. This pin is used to set the peak current sense voltage in the current comparator. Connect this pin to SGND, leave floating or connect to $INTV_{CC}$ to set the peak current sense voltage to 50mV, 75mV or 100mV, respectively.

$INTV_{CC}$ (Pins 5, 22/Pins 2, 17): Output of Internal 5.4V LDO. Power supply for control circuits and gate drivers. Decouple pin 22/17 to GND with a minimum 4.7µF low ESR ceramic capacitor. Connect pin 5/2 to pin 22/17 with a trace on the printed circuit board.

FREQ (Pin 7/Pin 3): Frequency Control Pin for the Internal VCO. Connecting the pin to GND forces the VCO to a fixed low frequency of 350kHz. Connecting the pin to $INTV_{CC}$ forces the VCO to a fixed high frequency of 535kHz. The frequency can be programmed from 50kHz to 900kHz by connecting a resistor from the FREQ pin to GND. The resistor and an internal 20µA source current create a voltage used by the internal oscillator to set the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

GND (Pin 8, 10, 24, Exposed Pad Pin 25/ Pin 4, Exposed Pad Pin 21): Ground. All ground pins must be connected and the exposed pad must be soldered to the PCB for rated electrical and thermal performance.

PLLIN/MODE (Pin 9/Pin 5): External Synchronization Input to Phase Detector and Forced Continuous Mode Input. When an external clock is applied to this pin, the phase-locked loop will force the rising edge of BG to be synchronized with the rising edge of the external clock. When an external clock is applied to this pin, the OVMODE pin is used to determine how the LTC3769 operates at light load. When not synchronizing to an external clock, this

PIN FUNCTIONS (QFN/TSSOP)

input determines how the LTC3769 operates at light loads. Pulling this pin to ground selects Burst Mode operation. An internal 100k resistor to ground also invokes Burst Mode operation when the pin is floated. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V selects pulse-skipping operation. This can be done by adding a 100k resistor between the PLLIN/MODE pin and $INTV_{CC}$.

RUN (Pin 11/Pin 6): Run Control Input. Forcing this pin below 1.28V shuts down the controller. Forcing this pin below 0.7V shuts down the entire LTC3769, reducing quiescent current to approximately 4µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. Once running, a 4.5µA current is sourced from the RUN pin allowing the user to program hysteresis using the resistor values.

SS (Pin 12/Pin 7): Output Soft-Start Input. A capacitor to ground at this pin sets the ramp rate of the output voltage during start-up.

$SENSE^-$ (Pin 13/Pin 8): Negative Current Sense Comparator Input. The (–) input to the current comparator is normally connected to the negative terminal of a current sense resistor connected in series with the inductor.

$SENSE^+$ (Pin 14/Pin 9): Positive Current Sense Comparator Input. The (+) input to the current comparator is normally connected to the positive terminal of a current sense resistor. The current sense resistor is normally placed at the input of the boost controller in series with the inductor. This pin also supplies power to the current comparator. The common mode voltage range on $SENSE^+$ and $SENSE^-$ pins is 2.3V to 60V (65V abs max).

VFB (Pin 15/Pin 10): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider connected across the output.

ITH (Pin 16/Pin 11): Current Control Threshold and Error Amplifier Compensation Point. The voltage on this pin sets the current trip threshold.

OVMODE (Pin 17/Pin 12): Overvoltage Mode Selection Input. This pin is used to select how the LTC3769 operates when the output feedback voltage (V_{FB}) is overvoltage (>110% of its normal regulated point of 1.2V). It is also used to determine the light-load mode of operation when the LTC3769 is synchronized to an external clock through the PLLIN/MODE pin.

When OVMODE is tied to ground, overvoltage protection is enabled and the top MOSFET gate (TG) is turned on continuously until the overvoltage condition is cleared. When OVMODE is grounded, the LTC3769 operates in forced continuous mode when synchronized. There is an internal weak pull-down resistor that pulls the OVMODE pin to ground when it is left floating.

When OVMODE is tied to $INTV_{CC}$, overvoltage protection is disabled and TG is not forced on during an overvoltage event. Instead, the state of TG is determined by the mode of operation selected by the PLLIN/MODE pin and the inductor current. See the Operation section for more details. When OVMODE is tied to $INTV_{CC}$, the LTC3769 operates in pulse-skipping mode when synchronized.

SW (Pin 18/Pin 13): Switch Node. Connect to the source of the synchronous N-channel MOSFET, the drain of the main N-channel MOSFET and the inductor.

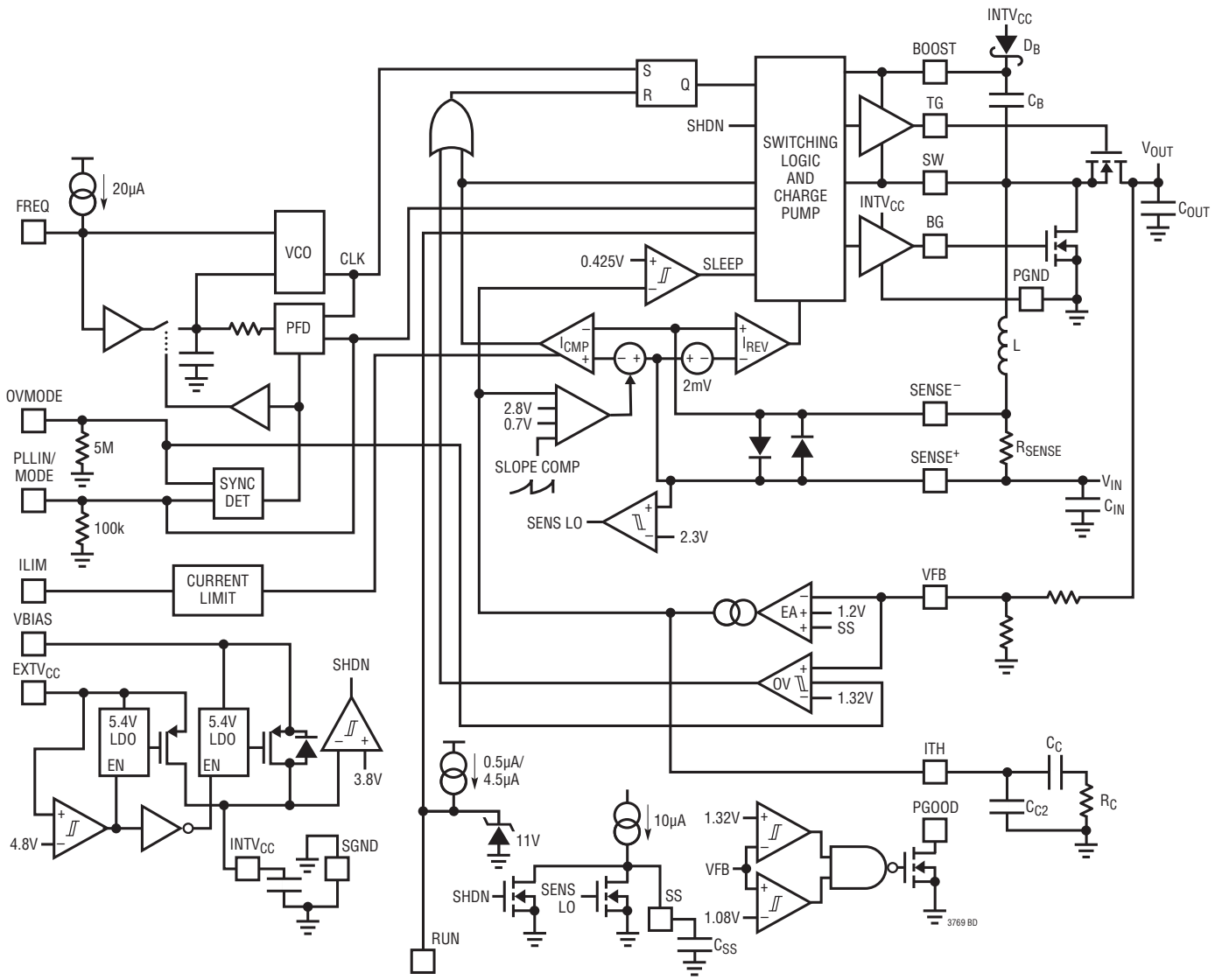
TG (Pin 19/Pin 14): Top Gate. Connect to the gate of the synchronous N-channel MOSFET.

BOOST (Pin 20/Pin 15): Floating power supply for the synchronous N-channel MOSFET. Bypass to SW with a capacitor and supply with a Schottky diode connected to $INTV_{CC}$.

BG (Pin 21/Pin 16): Bottom Gate. Connect to the gate of the main N-channel MOSFET.

$EXTV_{CC}$ (Pin 23/Pin 18): External Power Input to an internal LDO Connected to $INTV_{CC}$. This LDO supplies $INTV_{CC}$ power, bypassing the internal LDO powered from V_{BIAS} whenever $EXTV_{CC}$ is higher than 4.7V. See $EXTV_{CC}$ Connection in the Applications Information section. Do not float or exceed 14V on this pin. Connect to ground if not used.

BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3769 uses a constant-frequency, current mode step-up architecture. During normal operation, each external bottom MOSFET is turned on when the clock for that channel sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the ITH pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the VFB pin (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground), to the internal 1.200V reference voltage. In a boost converter, the required inductor current is determined by the load current, V_{IN} and V_{OUT}. When the load current increases, it causes a slight decrease in VFB relative to the reference, which causes the EA to increase the ITH voltage until the average inductor current in each channel matches the new requirement based on the new load current.

After the bottom MOSFET is turned off each cycle, the top MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator, I_{REV}, or the beginning of the next clock cycle.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is tied to a voltage less than 4.8V, the VBIAS LDO (low dropout linear regulator) supplies 5.4V from VBIAS to $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.8V, the VBIAS LDO is turned off and an $EXTV_{CC}$ LDO is turned on. Once enabled, the $EXTV_{CC}$ LDO supplies 5.4V from $EXTV_{CC}$ to $INTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from an external source, thus removing the power dissipation of the VBIAS LDO.

Shutdown and Start-Up (RUN and SS Pins)

The LTC3769 can be shut down using the RUN pin. Pulling this pin below 1.28V shuts down the main control loops. Pulling this pin below 0.7V disables the controller and most internal circuits, including the $INTV_{CC}$ LDOs. In this state, the LTC3769 draws only 4µA of quiescent current.

NOTE: Do not apply a heavy load to the boost converter for an extended time while the LTC3769 is in shutdown. The top MOSFET is turned off during shutdown and the output load may cause excessive dissipation in the body diode.

The RUN pin may be externally pulled up or driven directly by logic. When driving the RUN pin with a low impedance source, do not exceed the absolute maximum rating of 8V. The RUN pin has an internal 11V voltage clamp that allows the RUN pin to be connected through a resistor to a higher voltage (for example, V_{IN}), as long as the maximum current into the RUN pin does not exceed 100µA. An external resistor divider connected to V_{IN} can set the threshold for converter operation. Once running, a 4.5µA current is sourced from the RUN pin allowing the user to program hysteresis using the resistor values.

The start-up of the controller's output voltage V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the 1.2V internal reference, the LTC3769 regulates the VFB voltage to the SS pin voltage instead of the 1.2V reference. This allows the SS pin to be used to program a soft-start by connecting an external capacitor from the SS pin to SGND. An internal 10µA pull-up current charges this capacitor creating a voltage ramp on the SS pin. As the SS voltage rises linearly from 0V to 1.2V (and beyond up to $INTV_{CC}$), the output voltage rises smoothly to its final value.

Light Load Current Operation—Burst Mode Operation, Pulse-Skipping or Continuous Conduction (PLLIN/MODE Pin)

The LTC3769 can be enabled to enter high efficiency Burst Mode operation, constant-frequency, pulse-skipping mode or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to ground (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to $INTV_{CC}$. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 1.2V and less than $INTV_{CC}$ – 1.3V.

When the controller is enabled for Burst Mode operation, the minimum peak current in the inductor is set to

OPERATION

approximately 30% of the maximum sense voltage even though the voltage on the ITH pin indicates a lower value. If the average inductor current is higher than the required current, the error amplifier EA will decrease the voltage on the ITH pin. When the ITH voltage drops below 0.425V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode much of the internal circuitry is turned off and the LTC3769 draws only 28µA of quiescent current. In sleep mode the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low and the controller resumes normal operation by turning on the bottom external MOSFET on the next cycle of the internal oscillator.

When the controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the top external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous current operation.

In forced continuous operation or when clocked by an external clock source to use the phase-locked loop (see the Frequency Selection and Phase-Locked Loop section), the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the ITH pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output voltage ripple and less interference to audio circuitry, as it maintains constant-frequency operation independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode, the LTC3769 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external bottom MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN/MODE Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3769's controllers can be selected using the FREQ pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the FREQ pin can be tied to SGND, tied to $INTV_{CC}$, or programmed through an external resistor. Tying FREQ to SGND selects 350kHz while tying FREQ to $INTV_{CC}$ selects 535kHz. Placing a resistor between FREQ and SGND allows the frequency to be programmed between 50kHz and 900kHz, as shown in Figure 7.

A phase-locked loop (PLL) is available on the LTC3769 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. The LTC3769's phase detector adjusts the voltage (through an internal lowpass filter) of the VCO input so that the turn-on of the external bottom MOSFET is 180° out-of-phase to the rising edge of the external clock source. When synchronized, the LTC3769 will operate in forced continuous mode of operation if the OVMODE pin is grounded. If the OVMODE pin is tied to $INTV_{CC}$, the LTC3769 will operate in pulse-skipping mode of operation when synchronized.

The VCO input voltage is prebiased to the operating frequency set by the FREQ pin before the external clock is applied. If prebiased near the external clock frequency, the PLL loop only needs to make slight changes to the VCO input in order to synchronize the rising edge of the external clock's to the rising edge of BG1. The ability to prebias the loop filter allows the PLL to lock-in rapidly without deviating far from the desired frequency.

OPERATION

The typical capture range of the LTC3769's PLL is from approximately 55kHz to 1MHz, and is guaranteed to lock to an external clock source whose frequency is between 75kHz and 850kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling). The recommended maximum amplitude for low level and minimum amplitude for high level of external clock are 0V and 2.5V, respectively.

Operation When V_{IN} > Regulated V_{OUT}

When V_{IN} rises above the regulated V_{OUT} voltage, the boost controller can behave differently depending on the mode, inductor current and V_{IN} voltage. In forced continuous mode, the control loop works to keep the top MOSFET on continuously once V_{IN} rises above V_{OUT}. The internal charge pump delivers current to the boost capacitor to maintain a sufficiently high TG voltage. The amount of current the charge pump can deliver is characterized by two curves in the Typical Performance Characteristics section.

In pulse-skipping mode, if V_{IN} is between 100% and 110% of the regulated V_{OUT} voltage, TG turns on if the inductor current rises above a certain threshold and turns off if the inductor current falls below this threshold. This threshold current is set to approximately 6%, 4% or 3% of the maximum ILIM current when the ILIM pin is grounded, floating or tied to $INTV_{CC}$, respectively. If the controller is programmed to Burst Mode operation under this same V_{IN} window, then TG remains off regardless of the inductor current.

If the OVMODE pin is grounded and V_{IN} rises above 110% of the regulated V_{OUT} voltage in any mode, the controller turns on TG regardless of the inductor current. In Burst Mode operation, however, the internal charge pump turns off if the chip is asleep. With the charge pump off, there would be nothing to prevent the boost capacitor from discharging, resulting in an insufficient TG voltage needed to keep the top MOSFET completely on. To prevent excessive power dissipation across the body diode of the top MOSFET in this situation, the chip can be switched over to forced continuous mode to enable the charge pump; a Schottky diode can also be placed in parallel with the top MOSFET.

Power Good

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when the VFB pin voltage is not within ±10% of the 1.2V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low (shut down). When the VFB pin voltage is within the ±10% requirement, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V (abs max).

Overvoltage Mode Selection

The OVMODE pin is used to select how the LTC3769 operates during an overvoltage event, defined as when the output feedback voltage (V_{FB}) is greater than 110% of its normal regulated point of 1.2V. It is also used to determine the light-load mode of operation when the LTC3769 is synchronized to an external clock through the PLLIN/MODE pin.

The OVMODE pin is a logic input that should normally be tied to $INTV_{CC}$ or grounded. Alternatively, the pin can be left floating, which allow a weak internal resistor to pull it down to ground.

OVMODE = $INTV_{CC}$: An overvoltage event causes the error amplifier to pull the ITH pin low. In Burst Mode operation, this causes the LTC3769 to go to sleep and TG and BG are held off. In pulse-skipping mode, BG is held off and TG will turn on if the inductor current is positive. In forced continuous mode, TG (and BG) will switch on and off as the LTC3769 will regulate the inductor current to a negative peak value (corresponding to ITH = 0V) to discharge the output.

When OVMODE is tied to $INTV_{CC}$, the LTC3769 operates in pulse-skipping mode when synchronized.

In summary, with OVMODE = $INTV_{CC}$, the inductor current is not allowed to go negative (reverse from output to input) except in forced continuous mode, where it does reverse current but in a controlled manner with a regulated negative peak current. OVMODE should be tied to $INTV_{CC}$ in applications where the output voltage may sometimes be above its regulation point (for example, if the output

OPERATION

is a battery or if there are other power supplies driving the output) and no reverse current flow from output to input is desired.

OVMODE Grounded or Left Floating: When OVMODE is grounded or left floating, overvoltage protection is enabled and TG is turned on continuously until the overvoltage condition is cleared, regardless of whether Burst Mode operation, pulse-skipping mode, or forced continuous mode is selected by the PLLIN/MODE pin. This can cause large negative inductor currents to flow from the output to the input if the output voltage is higher than the input voltage.

Note however that in Burst Mode operation, the LTC3769 is in sleep during an overvoltage condition, which disables the internal oscillator and BOOST-SW charge pump. So the BOOST-SW voltage may discharge (due to leakage) if the overvoltage conditions persists indefinitely. If BOOST-SW discharges, then by definition TG would turn off.

When OVMODE is grounded or left floating, the LTC3769 operates in forced continuous mode when synchronized.

OVMODE should be tied to ground or left floating in circuits, such as automotive applications, where the input voltage can often be above the regulated output voltage and it is desirable to turn on TG to “pass through” the input voltage to the output.

Operation at Low SENSE Pin Common Mode Voltage

The current comparator in the LTC3769 is powered directly from the $SENSE^+$ pin. This enables the common mode voltage of the $SENSE^+$ and $SENSE^-$ pins to operate at as low as 2.3V, which is below the UVLO threshold. Figure 10 shows a typical application in which the controller’s VBIAS is powered from V_{OUT} while the V_{IN} supply can go as low as 2.3V. If the voltage on $SENSE^+$ drops below 2.3V, the SS pin will be held low. When the SENSE voltage returns to the normal operating range, the SS pin will be released, initiating a new soft-start cycle.

BOOST Supply Refresh and Internal Charge Pump

The top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each cycle through an external diode when the bottom MOSFET turns on. There are two considerations for keeping the BOOST supply at the required bias level. During start-up, if the bottom MOSFET is not turned on within 200µs after UVLO goes low, the bottom MOSFET will be forced to turn on for ~400ns. This forced refresh generates enough BOOST-SW voltage to allow the top MOSFET ready to be fully enhanced instead of waiting for the initial few cycles to charge up. There is also an internal charge pump that keeps the required bias on BOOST. The charge pump always operates in both forced continuous mode and pulse-skipping mode. In Burst Mode operation, the charge pump is turned off during sleep and enabled when the chip wakes up. The internal charge pump can normally supply a charging current of 55µA.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3769 application circuit. The LTC3769 can be configured to use either inductor DCR (DC resistance) sensing or a discrete sense resistor (R_{SENSE}) for current sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it does not require current sensing resistors and is more power-efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 2.3V to 60V. The current sense resistor is normally placed at the input of the boost controller in series with the inductor.

The SENSE+ pin also provides power to the current comparator. It draws ~200µA during normal operation. There is a small base current of less than 1µA that flows into the SENSE– pin. The high impedance SENSE– input to the current comparators allows accurate DCR sensing.

Filter components mutual to the sense lines should be placed close to the LTC3769, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes.

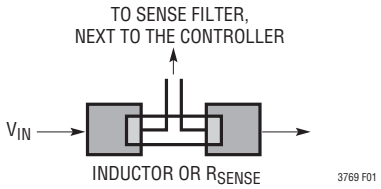
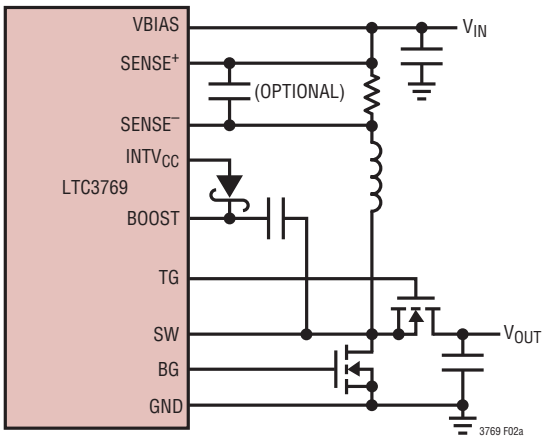
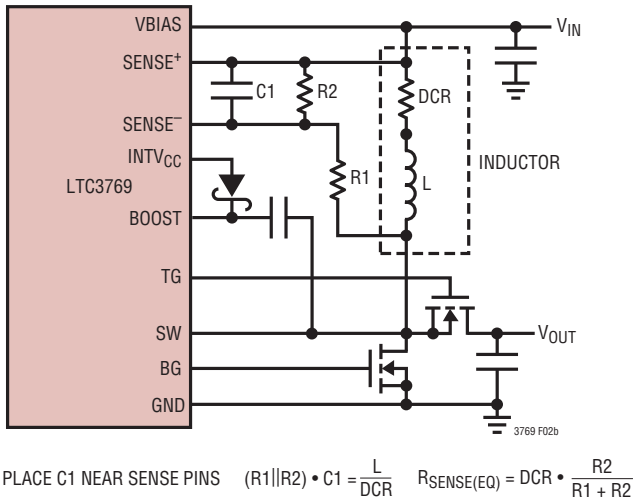


Figure 1. Sense Lines Placement with Inductor or Sense Resistor



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

APPLICATIONS INFORMATION

Sense Resistor Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$. When the ILIM pin is grounded, floating or tied to $INTV_{CC}$, the maximum threshold is set to 50mV, 75mV or 100mV, respectively. The current comparator threshold sets the peak of the inductor current, yielding a maximum average inductor current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

The actual value of I_{MAX} depends on the required output current $I_{OUT(MAX)}$ and can be calculated using:

$$I_{MAX} = I_{OUT(MAX)} \bullet \left(\frac{V_{OUT}}{V_{IN}} \right)$$

When using the controller in low V_{IN} and very high voltage output applications, the maximum inductor current and correspondingly the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for boost regulators operating at greater than 50% duty factor. A curve is provided in the Typical Performance Characteristics section to estimate this reduction in peak inductor current level depending upon the operating duty factor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3769 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor can be less than 1mΩ for high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor could reduce the efficiency by a few percent compared to DCR sensing.

If the external R1||R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature. Consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the inductor value calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{MAX} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for the maximum inductor temperature ($T_{L(MAX)}$) is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.1µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the $SENSE^-$ pin's ±1µA current.

The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

APPLICATIONS INFORMATION

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at $V_{IN} = 1/2V_{OUT}$:

$$P_{LOSS\_R1} = \frac{(V_{OUT} - V_{IN}) \bullet V_{IN}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. Why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge and switching losses. Also, at higher frequency the duty cycle of body diode conduction is higher, which results in lower efficiency. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at $V_{IN} = 1/2V_{OUT}$.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease. Once the value of L is known, an inductor with low DCR and low core losses should be selected.

Power MOSFET Selection

Two external power MOSFETs must be selected for the LTC3769: one N-channel MOSFET for the bottom (main) switch, and one N-channel MOSFET for the top (synchronous) switch.

The peak-to-peak gate drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5.4V during start-up (see $EXTV_{CC}$ pin connection). Consequently, logic-level threshold MOSFETs must be used in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturer's data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in VDS. This result is then multiplied by the ratio of the application applied VDS to the gate charge curve specified VDS. When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT} - V_{IN}}{V_{OUT}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN}}{V_{OUT}}$$

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If the maximum output current is $I_{OUT(MAX)}$ the MOSFET power dissipation at maximum output current is given by:

$$P_{MAIN} = \frac{(V_{OUT} - V_{IN})V_{OUT}}{V^2_{IN}} \bullet I^2_{OUT(MAX)} \bullet (1+\delta) \bullet R_{DS(ON)} + k \bullet V_{OUT}{}^3 \bullet \frac{I_{OUT(MAX)}}{V_{IN}} \bullet C_{MILLER} \bullet f$$

$$P_{SYNC} = \frac{V_{IN}}{V_{OUT}} \bullet I^2_{OUT(MAX)} \bullet (1+\delta) \bullet R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$. The constant k, which accounts for the loss caused by reverse recovery current, is inversely proportional to the gate drive current and has an empirical value of 1.7.

Both MOSFETs have I^2R losses while the bottom N-channel equation includes an additional term for transition losses, which are highest at low input voltages. For high V_{IN} the high current efficiency generally improves with larger MOSFETs, while for low V_{IN} the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the bottom switch duty factor is low or during overvoltage when the synchronous switch is on close to 100% of the period.

The term (1+ δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

C_{IN} and C_{OUT} Selection

The input ripple current in a boost converter is relatively low (compared with the output ripple current), because this current is continuous. The input capacitor C_{IN} voltage rating should comfortably exceed the maximum input voltage. Although ceramic capacitors can be relatively tolerant of overvoltage conditions, aluminum electrolytic capacitors are not. Be sure to characterize the input voltage for any possible overvoltage transients that could apply excess stress to the input capacitors.

The value of C_{IN} is a function of the source impedance, and in general, the higher the source impedance, the higher the required input capacitance. The required amount of input capacitance is also greatly affected by the duty cycle. High output current applications that also experience high duty cycles can place great demands on the input supply, both in terms of DC current and ripple current.

In a boost converter, the output has a discontinuous current, so C_{OUT} must be capable of reducing the output voltage ripple. The effects of ESR (equivalent series resistance) and the bulk capacitance must be considered when choosing the right capacitor for a given output ripple voltage. The steady ripple voltage due to charging and discharging the bulk capacitance in a single phase boost converter is given by:

$$V_{RIPPLE} = \frac{I_{OUT(MAX)} \bullet (V_{OUT} - V_{IN(MIN)})}{C_{OUT} \bullet V_{OUT} \bullet f} V$$

where C_{OUT} is the output filter capacitor.

The steady ripple due to the voltage drop across the ESR is given by:

$$\Delta V_{ESR} = I_{L(MAX)} \bullet ESR$$

Multiple capacitors placed in parallel may be needed to meet the ESR and RMS current handling requirements. Dry tantalum, special polymer, aluminum electrolytic and ceramic capacitors are all available in surface mount packages. Ceramic capacitors have excellent low ESR characteristics but can have a high voltage coefficient. Capacitors are now available with low ESR and high ripple current ratings (e.g., OS-CON and POSCAP).

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Setting Output Voltage

The LTC3769 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 3. The regulated output voltage is determined by:

$$V_{OUT} = 1.2V\left(1+\frac{R_B}{R_A}\right)$$

Great care should be taken to route the VFB line away from noise sources, such as the inductor or the SW line. Also place the feedback resistor divider close to the VFB pin and keep the VFB node as small as possible to avoid noise pickup.

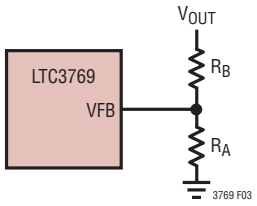

Figure 3. Setting Output Voltage

Soft-Start (SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the SS pin. When the voltage on the SS pin is less than the internal 1.2V reference, the LTC3769 regulates the VFB pin voltage to the voltage on the SS pin instead of 1.2V.

Soft-start is enabled by simply connecting a capacitor from the SS pin to ground, as shown in Figure 4. An internal 10µA current source charges the capacitor, providing a linear ramping voltage at the SS pin. The LTC3769 will regulate the VFB pin (and hence, V_{OUT}) according to the voltage on the SS pin, allowing V_{OUT} to rise smoothly from V_{IN} to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{1.2V}{10\mu A}$$

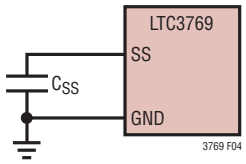

Figure 4. Using the SS Pin to Program Soft-Start

$INTV_{CC}$ Regulators

The LTC3769 features two separate internal P-channel low dropout linear regulators (LDO) that supply power at the $INTV_{CC}$ pin from either the VBIAS supply pin or the $EXTV_{CC}$ pin depending on the connection of the $EXTV_{CC}$ pin. $INTV_{CC}$ powers the gate drivers and much of the LTC3769's internal circuitry. The VBIAS LDO and the $EXTV_{CC}$ LDO regulate $INTV_{CC}$ to 5.4V. Each of these can supply at least 50mA and must be bypassed to ground with a minimum of a 4.7µF ceramic capacitor. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3769 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the VBIAS LDO or the $EXTV_{CC}$ LDO. When the voltage on the $EXTV_{CC}$ pin is less than 4.8V, the VBIAS LDO is enabled. In this case, power dissipation for the IC is highest and is equal to VBIAS • I_{INTVCC}. The gate charge current is dependent on operating frequency, as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, at 70°C ambient temperature, the LTC3769 $INTV_{CC}$ current is limited to less than 19mA in the QFN package from a 60V VBIAS supply when not using the $EXTV_{CC}$ supply:

T_J = 70°C + (19mA)(60V)(47°C/W) = 125°C

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In the TSSOP package, the $INTV_{CC}$ current is limited to less than 24mA from a 60V supply when not using the $EXTV_{CC}$ supply:

$T_J = 70°C + (24mA)(60V)(38°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

When the voltage applied to $EXTV_{CC}$ rises above 4.8V, the V_{IN} LDO is turned off and the $EXTV_{CC}$ LDO is enabled. The $EXTV_{CC}$ LDO remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.55V. The $EXTV_{CC}$ LDO attempts to regulate the $INTV_{CC}$ voltage to 5.4V, so while $EXTV_{CC}$ is less than 5.4V, the LDO is in dropout and the $INTV_{CC}$ voltage is approximately equal to $EXTV_{CC}$. When $EXTV_{CC}$ is greater than 5.4V, up to an absolute maximum of 14V, $INTV_{CC}$ is regulated to 5.4V.

Significant thermal gains can be realized by powering $INTV_{CC}$ from an external supply. Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to 75°C in a QFN package:

$T_J = 70°C + (19mA)(5V)(47°C/W) = 75°C$

and from 125°C to 75°C in the TSSOP package:

$T_J = 70°C + (24mA)(5V)(38°C/W) = 75°C$

The following list summarizes possible connections for $EXTV_{CC}$:

$EXTV_{CC}$ Grounded. This will cause $INTV_{CC}$ to be powered from the internal 5.4V regulator resulting in an efficiency penalty at high V_{BIAS} voltages.

$EXTV_{CC}$ Connected to an External Supply. If an external supply is available in the 5V to 14V range, it may be used to provide power. Ensure that $EXTV_{CC}$ is always lower than or equal to VBIAS.

Topside MOSFET Driver Supply (C_B, D_B)

An external bootstrap capacitor C_B connected to the BOOST pin supplies the gate drive voltage for the topside MOSFET. Capacitor C_B in the Block Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate and source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{OUT} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the output voltage: $V_{BOOST} = V_{OUT} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external diode D_B must be greater than $V_{OUT(MAX)}$.

The external diode D_B can be a Schottky diode or silicon diode, but in either case it should have low leakage and fast recovery. Pay close attention to the reverse leakage at high temperatures, where it generally increases substantially.

The topside MOSFET driver includes an internal charge pump that delivers current to the bootstrap capacitor from the BOOST pin. This charge current maintains the bias voltage required to keep the top MOSFET on continuously during dropout/overvoltage conditions. The Schottky/silicon diode selected for the topside driver should have a reverse leakage less than the available output current the charge pump can supply. Curves displaying the available charge pump current under different operating conditions can be found in the Typical Performance Characteristics section.

A leaky diode D_B in the boost converter can not only prevent the top MOSFET from fully turning on but it can also completely discharge the bootstrap capacitor C_B and create a current path from the input voltage to the BOOST pin to $INTV_{CC}$. This can cause $INTV_{CC}$ to rise if the diode leakage exceeds the current consumption on $INTV_{CC}$. This is particularly a concern in Burst Mode operation

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where the load on $INTV_{CC}$ can be very small. The external Schottky or silicon diode should be carefully chosen such that $INTV_{CC}$ never gets charged up much higher than its normal regulation voltage.

Fault Conditions: Overtemperature Protection

At higher temperatures, or in cases where the internal power dissipation causes excessive self heating on-chip (such as an $INTV_{CC}$ short to ground), the overtemperature shutdown circuitry will shut down the LTC3769. When the junction temperature exceeds approximately 170°C, the overtemperature circuitry disables the $INTV_{CC}$ LDO, causing the $INTV_{CC}$ supply to collapse and effectively shut down the entire LTC3769 chip. Once the junction temperature drops back to approximately 155°C, the $INTV_{CC}$ LDO turns back on. Long term overstress (T_J > 125°C) should be avoided as it can degrade the performance or shorten the life of the part.

Since the shutdown may occur at full load, beware that the load current will result in high power dissipation in the body diodes of the top MOSFETs. In this case, the PGOOD output may be used to turn the system load off.

Phase-Locked Loop and Frequency Synchronization

The LTC3769 has an internal phase-locked loop (PLL) comprised of a phase frequency detector, a lowpass filter and a voltage-controlled oscillator (VCO). This allows the turn-on of the bottom MOSFET to be locked signal applied to 180 degrees out-of-phase to the rising edge of the external clock. The phase detector is an edge-sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the VCO input. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the VCO input. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage at the VCO input is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the internal filter capacitor, C_{LP}, holds the voltage at the VCO input.

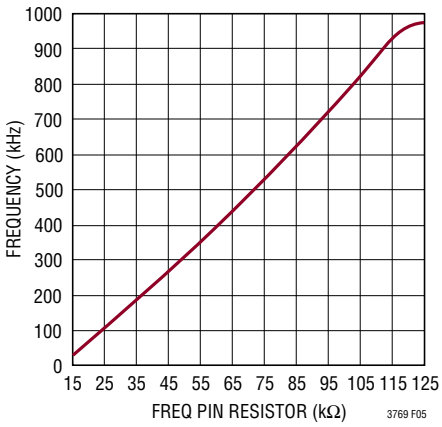

Figure 5. Relationship Between Oscillator Frequency and Resistor Value at the FREQ Pin

Typically, the external clock (on the PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Note that the LTC3769 can only be synchronized to an external clock whose frequency is within range of the LTC3769's internal VCO, which is nominally 55kHz to 1MHz. This is guaranteed to be between 75kHz and 850kHz.

Rapid phase locking can be achieved by using the FREQ pin to set a free-running frequency near the desired synchronization frequency. The VCO's input voltage is prebiased at a frequency corresponding to the frequency set by the FREQ pin. Once prebiased, the PLL only needs to adjust the frequency slightly to achieve phase lock and synchronization. Although it is not required that the free-running frequency be near external clock frequency, doing so will prevent the operating frequency from passing through a large range of frequencies as the PLL locks.

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Table 1 summarizes the different states in which the FREQ pin can be used.

Table 1.

FREQ PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	350kHz
$INTV_{CC}$	DC Voltage	535kHz
Resistor	DC Voltage	50kHz to 900kHz
Any of the Above	External Clock	Phase Locked to External Clock

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that the LTC3769 is capable of turning on the bottom MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit.

In forced continuous mode, if the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles but the output will continue to be regulated. More cycles will be skipped when V_{IN} increases. Once V_{IN} rises above V_{OUT}, the loop keeps the top MOSFET continuously on. The minimum on-time for the LTC3769 is approximately 110ns.

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the greatest improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc., are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, five main sources usually account for most of the losses in LTC3769 circuits: 1) IC VBIAS current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) bottom MOSFET transition losses, 5) body diode conduction losses.

1. The VBIAS current is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents. VBIAS current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge, dQ, moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. DC I^2R losses. These arise from the resistances of the MOSFETs, sensing resistor, inductor and PC board traces and cause the efficiency to drop at high output currents.

4. Transition losses apply only to the bottom MOSFET(s), and become significant only when operating at low input voltages. Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\frac{V_{OUT}^3}{V_{IN}} \bullet I_{OUT(MAX)} \bullet C_{RSS} \bullet f$$

5. Body diode conduction losses are more significant at higher switching frequency. During the dead time, the loss in the top MOSFET is $I_{OUT} \bullet V_{DS}$, where V_{DS} is around 0.7V. At higher switching frequency, the dead time becomes a good percentage of switching cycle and causes the efficiency to drop.

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Other hidden losses, such as copper trace and internal battery resistances, can account for an additional efficiency degradation in portable systems. It is very important to include these system-level losses during the design phase.

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to $\Delta I_{LOAD} \bullet ESR$, where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT}, generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP® compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The availability of the ITH pin not only allows optimization of control loop behavior, but it also provides a DC coupled and AC filtered closed loop response test point. The DC step, rise time and settling at this test point truly reflects the closed loop response. Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The ITH external components shown in the Figure 10 circuit will provide an adequate starting point for most applications.

The ITH series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly to optimize transient response once the final PC layout is complete and the particular output capacitor type and value have been determined. The output capacitors must be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and ITH pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop.

Placing a power MOSFET and load resistor directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the ITH pin signal which is in the feedback loop and is the filtered and compensated control loop response.

The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If RC is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately $25 \bullet C_{LOAD}$. Thus, a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Design Example

As a design example, assume V_{IN} = 12V (nominal), V_{IN} = 22V (max), V_{OUT} = 24V, $I_{OUT(MAX)}$ = 4A, $V_{SENSE(MAX)}$ = 75mV, and f = 350kHz.

The inductance value is chosen first based on a 30% ripple current assumption. Tie the FREQ pin to GND, generat-

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ing 350kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{IN}}{f \bullet L}\left(1 - \frac{V_{IN}}{V_{OUT}}\right)$$

The largest ripple happens when V_{IN} = 1/2V_{OUT} = 12V, where the average maximum inductor current is:

$$I_{MAX} = I_{OUT(MAX)} \bullet \left(\frac{V_{OUT}}{V_{IN}}\right) = 8A$$

A 6.8µH inductor will produce a 31% ripple current. The peak inductor current will be the maximum DC value plus one half the ripple current, or 9.25A.

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{75mV}{9.25A} = 0.008\Omega$$

Choosing 1% resistors: R_A = 5k and R_B = 95.3k yields an output voltage of 24.072V.

The power dissipation on the top side MOSFET can be easily estimated. Choosing a Vishay Si7848BDP MOSFET results in: $R_{DS(ON)}$ = 0.012Ω, C_{MILLER} = 150pF. At maximum input voltage with T (estimated) = 50°C:

$$P_{MAIN} = \frac{(24V - 12V)\,24V}{(12V)^2} \bullet (4A)^2 \bullet \left[1 + (0.005)(50°C - 25°C)\right] \bullet 0.012\Omega + (1.7)(24V)^3 \frac{4A}{12V}(150pF)(350kHz) = 0.84W$$

C_{OUT} is chosen to filter the square current in the output. The maximum output current peak is:

$$I_{OUT(PEAK)} = 8 \bullet \left(1 + \frac{31\%}{2}\right) = 9.3A$$

A low ESR (5mΩ) capacitor is suggested. This capacitor will limit output voltage ripple to 46.5mV (assuming ESR dominates the ripple).

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 6. Figure 7 illustrates the current waveforms present in the synchronous regulator operating in the continuous mode. Check the following in your layout:

1. Put the bottom N-channel MOSFET MBOT and the top N-channel MOSFET MTOP1 in one compact area with C_{OUT}.
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the bottom N-channel MOSFET and the capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the source terminals of the bottom MOSFETs.
3. Does the LTC3769 VFB pin's resistive divider connect to the (+) terminal of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground and placed close to the VFB pin. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the sense resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers' current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and GND pins can help improve noise performance substantially.

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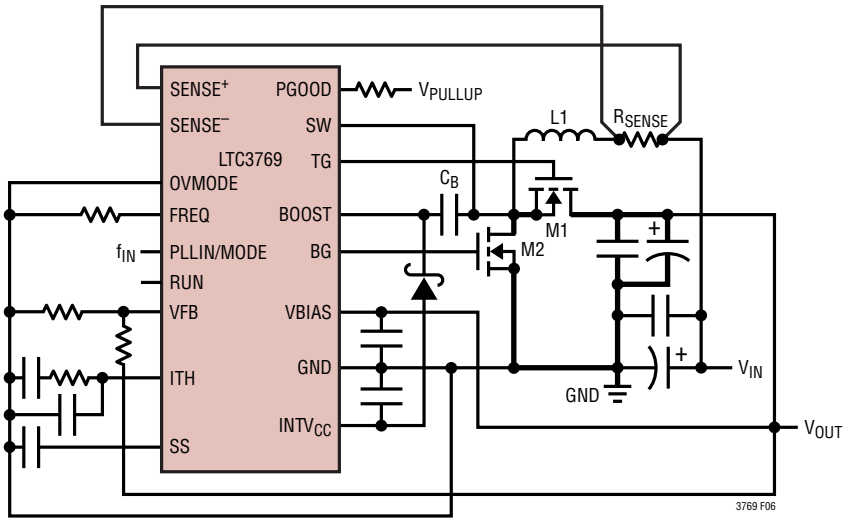

Figure 6. Recommended Printed Circuit Layout Diagram

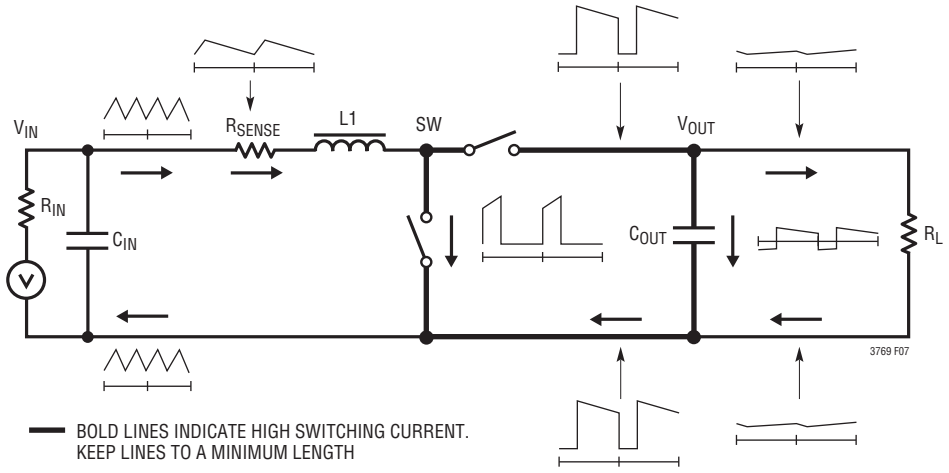

Figure 7. Branch Current Waveforms