Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

High Speed Dual, Multiphase Step-Down DC/DC Controller

FEATURES

- **Fixed Frequency, Peak Current Mode Control**
- **±0.5% Output Accuracy Over Temperature**
- **Optimized for Low V_{OUT} Applications (Up to 3.3V)**
- **Dual or Single Output, Multiphase Operation**
- **Wide V_{IN} Range: 4.5V to 30V Operation**
- **High Speed Differential Remote Sense Amplifier**
- **Inductor DCR or Sense Resistor Capable**
- **Adjustable Peak Current Sense Voltage: 24mV to 85mV**
- **Very Low Duty Cycle Operation: $t_{ON(MIN)}$ = 65ns (Typ)**
- Powerful Internal Gate Drivers
- Output Voltage Soft-Start, Tracking and Sequencing
- Programmable Load Line for Reduced C_{OUT}
- Clock Input and Output for Up to 12-Phase Operation
- Fixed Frequency Operation from 250kHz to 750kHz
- PLL Synchronization from 150kHz Up to 900kHz
- Selectable CCM or DCM Operation
- Available in 5mm × 7mm QFN and G36 Packages

APPLICATIONS

- Network Servers
- High Current ASIC Supplies
- Low Voltage Power Distribution

DESCRIPTION

The LTC®3811 is a dual, PolyPhase® synchronous step-down switching regulator controller optimized for output voltages up to 3.3V. The LTC3811 includes high bandwidth error amplifiers as well as a high speed differential remote sense amplifier. The sense voltage range is programmable from 24mV to 85mV, allowing the use of either the inductor DCR or a discrete sense resistor. Multiphase operation is made possible using the MODE/SYNC input, the CLKOUT output and the PHASEMODE control pin, allowing 1-, 2-, 3-, 4-, 6- or 12-phase operation.

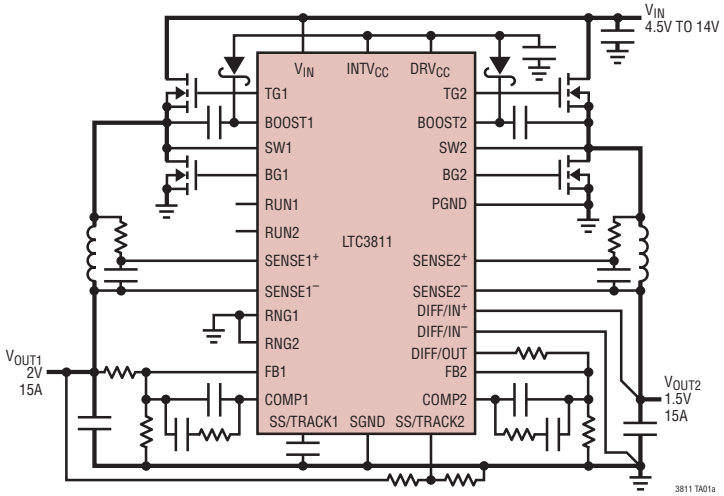
Large internal gate drivers minimize switching losses and allow the use of multiple power MOSFETs connected in parallel for high current applications.

The operating frequency of the LTC3811 can be programmed from 250kHz to 750kHz and can also be synchronized to an external clock using the internal PLL.

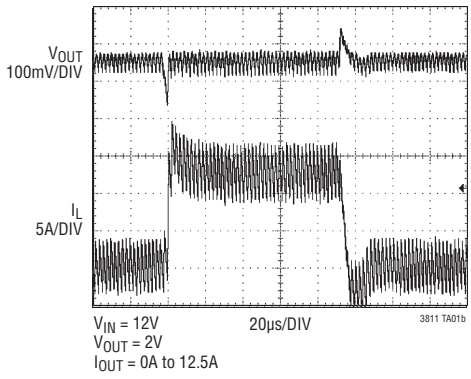
Tracking and sequencing are possible with the LTC3811, and soft-start is programmed with an external capacitor. Shutdown reduces supply current to 20µA.

TYPICAL APPLICATION

Dual Output, 2-Phase Tracking Core and I/O Supply



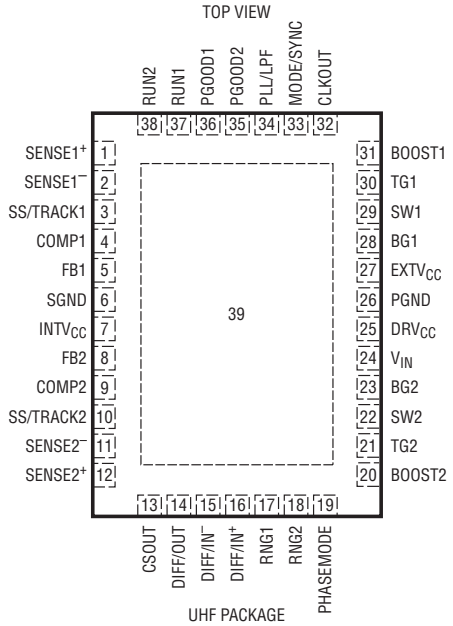
Load Step



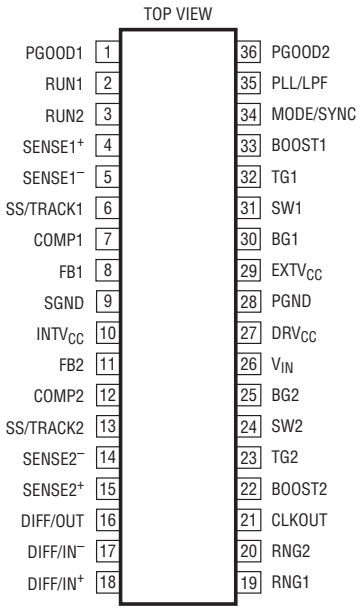
ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... –0.3V to 30V
Topside Driver Voltages
(BOOST1, BOOST2) ..... –0.3V to 37V
Switch Voltage (SW1, SW2) ..... –5V to 30V
BOOST1 – SW1, BOOST2 – SW2 ..... –0.3V to 7V
DRV_{CC}, $INTV_{CC}$, $EXTV_{CC}$, RUN1, RUN2, DIFF/IN$^+$, DIFF/IN$^-$, PHASEMODE, PGOOD1, PGOOD2, MODE/SYNC Voltages ..... –0.3V to 7V
FB1, FB2, RNG1, RNG2, SS/TRACK1, SS/TRACK2, PLL/LPF, SENSE1$^+$, SENSE1$^-$, SENSE2$^+$, SENSE2$^-$ Voltages ..... –0.3V to $INTV_{CC}$
DRV_{CC} LDO RMS Output Current 100mA
Operating Temperature Range (Note 2) ..... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP Package ..... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB



G PACKAGE
36-LEAD PLASTIC SSOP WIDE
T_{JMAX} = 125°C, θ_{JA} = 100°C/W

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3811EUHF#PBF	LTC3811EUHF#TRPBF	3811	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 85°C
LTC3811EG#PBF	LTC3811EG#TRPBF	LTC3811EG	36-Lead Plastic SSOP Wide	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, MODE/SYNC = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Input Supply							
V_{IN}	Operating Input Voltage Range			4.5		30	V
I_Q	Total Quiescent Supply Current Continuous Mode (Note 4) Shutdown Mode	 $V_{FB1,2}$ = 0.7V $V_{RUN1,2}$ = 0V	 ● ●		 10.5 20	 20 40	 mA µA
RUN Pin ON/OFF Control							
I_{RUN}	RUN Pin Input Leakage	$V_{RUN1,2}$ = 3.3V		–1		1	µA
$V_{IL(RUN)}$	Low Level RUN Input Threshold					0.3	V
$V_{IH(RUN)}$	High Level RUN Input Threshold			1.8			V
Error Amplifier Characteristics (Both Channels)							
V_{FB1}, V_{FB2}	Feedback Voltage Accuracy	(Note 5)	 ●	598 597	600	602 603	mV mV
I_{FB1}, I_{FB2}	Feedback Pin Input Current	V_{COMP} = 1.25V (Note 5)		–100		100	nA
$\Delta V_{FB}/\Delta V_{IN}$	Line Regulation	4.5V ≤ V_{IN} ≤ 30V (Note 5)	●		0.002	0.02	%/V
$\Delta V_{FB}/\Delta V_{COMP}$	Load Regulation	ΔV_{COMP} = 1.25V to 1.5V (Note 5)	●	–0.1	–0.01		%
$f_{0dB(EA)}$	Error Amplifier Unity Gain Crossover Frequency	(Note 6)			8		MHz
$V_{OH(EA)}$	Error Amplifier Maximum Output Voltage (Internally Clamped)	V_{FB} = 0.54V, No Load			2.6		V
$V_{OL(EA)}$	Error Amplifier Minimum Output Voltage	V_{FB} = 0.66V, No Load			10		mV
$V_{FB(OFF)}$	FB Voltage Threshold to Disable Error Amplifier Output	$V_{INTVCC} – V_{FB}$			0.3		V
Soft-Start/Tracking							
I_{SS1}, I_{SS2}	SS/TRACK1, SS/TRACK2 Charging Currents	$V_{SS/TRACK1}$ = $V_{SS/TRACK2}$ = 0.3V			–2.5		µA
R_{SS1}, R_{SS2}	SS/TRACK1, SS/TRACK2 Pull-Down Resistance in Shutdown	V_{RUN1} = V_{RUN2} = 0V			1		kΩ
Differential Amplifier							
A_V	Differential Mode Gain, $\Delta V_{DIFF/OUT}/\Delta V_{DIFF/IN}$	$\Delta V_{DIFF/IN}$ = 1V to 3.5V, $I_{DIFF/OUT}$ = –100µA		0.995	1.000	1.005	V/V
$V_{OS(DIFF)}$	Output Offset Voltage, $V_{DIFF/OUT} – V_{DIFF/IN}$+	$V_{DIFF/IN}$+ = 1.25V, $V_{DIFF/IN}$– = 0V, $I_{DIFF/OUT}$ = –100µA		–6		6	mV
R_{IN}	Input Resistance	Measured at $V_{DIFF/IN}$+			160		kΩ
$PSRR_{DIFF}$	Power Supply Rejection Ratio	7V ≤ V_{IN} ≤ 30V			100		dB
$V_{DM(DIFF)}$	Maximum Differential Mode Input Voltage	$V_{DIFF/IN}$+ – $V_{DIFF/IN}$–, Measured at $V_{DIFF/OUT}$, $I_{DIFF/OUT}$ = –100µA				5.5	V
I_{MAX}+	Maximum Sink Current			2			mA
I_{MAX}–	Maximum Source Current					–2	mA
$f_{0dB(DIFF)}$	Unity Gain Bandwidth	(Note 6)			8		MHz
Current Comparators							
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (V_{SENSE}+ – V_{SENSE}–)	V_{FB} = 0.575V, V_{CM} = 1.25V V_{RNG} = 0V V_{RNG} = $INTV_{CC}$ V_{RNG} = 2V		 14 32.5 60	 24 50 85	 34 67.5 110	 mV mV mV
$V_{SENSE(MIN)}$	Minimum Current Sense Threshold (V_{SENSE}+ – V_{SENSE}–)	V_{FB} = 0.625V, V_{CM} = 1.25V V_{RNG} = 0V V_{RNG} = $INTV_{CC}$ V_{RNG} = 2V			 –21 –41 –67		 mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, MODE/SYNC = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SENSE}	Total Sense Pin Current (V_{SENSE}+ + V_{SENSE}–)	V_{CM} = 1.25V			–1.5		µA
$V_{CM(CS)}$	V_{SENSE}+, V_{SENSE}– Pin Common Mode Input Voltage Range			0		3.5	V
Voltage Position Amplifier (QFN Package Only)							
g_m	Voltage Position Transconductance, $\Delta I_{CSOUT}/\Delta V_{SENSE}$ (Note 8)	V_{SENSE1}+ – V_{SENSE1}– = V_{SENSE2}+ – V_{SENSE2}– = ±50mV, V_{CM} = 1.25V, V_{CSOUT} = 1.25V			5.0		mS
$I_{OS(VP)}$	Output Offset Current, Measured at CSOUT	V_{SENSE1}+ – V_{SENSE1}– = V_{SENSE2}+ – V_{SENSE2}– = 1.25V, V_{CSOUT} = 1.25V		–40		40	µA
Multiphase Oscillator and Phase-Lock Loop (Note 9)							
f_{NOM}	Nominal Frequency	$V_{PLL/LPF}$ Pin Floating, MODE/SYNC = DC Voltage		450	500	550	kHz
f_{LOW}	Lowest Frequency	$V_{PLL/LPF}$ = 0V, MODE/SYNC = DC Voltage		200	250	300	kHz
f_{HIGH}	Highest Frequency	$V_{PLL/LPF}$ = $INTV_{CC}$, MODE/SYNC = DC Voltage		650	750	850	kHz
$f_{SYNC(MIN)}$	Minimum Synchronizable Frequency	MODE/SYNC = External Clock			125	175	kHz
$f_{SYNC(MAX)}$	Maximum Synchronizable Frequency	MODE/SYNC = External Clock		900	1000		kHz
$I_{PLL/LPF}$	Phase Detector Output Current Sinking Sourcing	 $f_{MODE/SYNC} < f_{OSC}$ $f_{MODE/SYNC} > f_{OSC}$			 –4.3 5.1		 µA µA
θ1 – θ2	Channel 1 to Channel 2 Phase Relationship (Note 9)	$V_{PHASMODE}$ = 0V $V_{PHASMODE}$ = 50% $INTV_{CC}$ $V_{PHASMODE}$ = $INTV_{CC}$			180 180 120		deg deg deg
θ1 – θ_{CLKOUT}	Channel 1 to CLKOUT Phase Relationship (Note 9)	$V_{PHASMODE}$ = 0V $V_{PHASMODE}$ = 50% $INTV_{CC}$ $V_{PHASMODE}$ = $INTV_{CC}$			90 60 240		deg deg deg
$V_{OL(CLKOUT)}$	Low Level CLKOUT Output Voltage	R_{CLK} = 50k to Ground				0.2	V
$V_{OH(CLKOUT)}$	High Level CLKOUT Output Voltage	R_{CLK} = 50k to Ground		4.0	5.8		V
$R_{MODE/SYNC}$	MODE/SYNC Input Resistance				75		kΩ
$V_{IL(MODE/SYNC)}$	Low Level MODE/SYNC Input Threshold					0.3	V
$V_{IH(MODE/SYNC)}$	High Level MODE/SYNC Input Threshold			1.8			V
Power Good Indicators							
$V_{OL(PGOOD)}$	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.12	0.30	V
$I_{PGOOD(OFF)}$	PGOOD Leakage Current	V_{PGOOD} = 6V				1.0	µA
$\Delta V_{FB(OV)}$	ΔV_{FB}, PGOOD Overvoltage Threshold	$V_{FB(OV)}$ – $V_{FB(NOM)}$ in Percent		7	10	13	%
$\Delta V_{FB(UV)}$	ΔV_{FB}, PGOOD Undervoltage Threshold	$V_{FB(UV)}$ – $V_{FB(NOM)}$ in Percent		–13	–10	–7	%
$\Delta V_{FB(HYST)}$	ΔV_{FB}, PGOOD Comparator Hysteresis	UV or OV Comparator			12		mV
$t_{PG(FAULT)}$	Delay from UV/OV Condition to PGOOD Falling				145		µs
$t_{PG(OK)}$	Delay from UV/OV Fault Recovery to PGOOD Rising				38		µs
Thermal Protection							
T_{JSD}	Thermal Shutdown Junction Temperature	(Note 6)			165		°C
$T_{JSD(HYST)}$	Thermal Shutdown Junction Temperature Hysteresis	(Note 6)			25		°C

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_J = 25°C. V_{IN} = 12V, MODE/SYNC = 0V, unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
DRV_{CC} Linear Regulator							
V_{DRVCC}	LDO Regulator Output Voltage	V_{EXTVCC} = 0V	●	5.6	6.0	6.4	V
$\Delta V_{DRVCC(LOAD)}$	DRV_{CC} Load Regulation	I_{LOAD} = 0mA to 50mA		–2.0	–0.5		%
$\Delta V_{DRVCC(LINE)}$	DRV_{CC} Line Regulation	ΔV_{IN} = 8.5V to 30V			0.01	0.2	%/V
$V_{DRVCC(UVLO)}$	LDO Regulator Undervoltage Threshold	DRV_{CC} Rising			3.7		V
$V_{DRVCC(HYST)}$	LDO Regulator Undervoltage Hysteresis				0.56		V
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	I_{DRVCC} = 20mA, $EXTV_{CC}$ Rising			4.5		V
$V_{EXTVCC(HYST)}$	$EXTV_{CC}$ Switchover Hysteresis	I_{DRVCC} = 20mA			400		mV
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Voltage Drop	I_{DRVCC} = 20mA, V_{EXTVCC} = 5V			100		mV
Gate Drivers							
t_r (TG1, TG2)	Top Gate Rise Time	C_L = 3300pF (Note 6)			20		ns
t_f (TG1, TG2)	Top Gate Fall Time	C_L = 3300pF (Note 6)			10		ns
t_r (BG1, BG2)	Bottom Gate Rise Time	C_L = 3300pF (Note 6)			20		ns
t_f (BG1, BG2)	Bottom Gate Fall Time	C_L = 3300pF (Note 6)			10		ns
$R_{DS(ON)(TG)}$ TG1, TG2	Top Gate Pull-Down NMOS On-Resistance	TG to SW			0.9		Ω
$R_{DS(ON)(BG)}$ BG1, BG2	Bottom Gate Pull-Down NMOS On-Resistance	BG to PGND			0.9		Ω
$I_{PK(TG)}$ TG1, TG2	Top Gate (TG) Peak Source Current				1.0		A
$I_{PK(BG)}$ BG1, BG2	Bottom Gate (BG) Peak Source Current				1.0		A
t_{DEAD1}	Bottom Gate Off to Top Gate On Deadtime	(Note 6)			30		ns
t_{DEAD2}	Top Gate Off to Bottom Gate On Deadtime	(Note 6)			30		ns
$t_{ON(MIN)}$	Minimum On-Time	V_{COMP} = 1.25V (Note 6, 7)			65		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Unless otherwise specified, all voltages are relative to SGND and all currents are positive into a pin.

Note 2: The LTC3811E is guaranteed to meet performance specifications from 0°C to 85°C temperature. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formula:

$$T_J = T_A + (P_D \bullet TBD°C/W)$$

Note 4: The dynamic input supply current is higher due to power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information for more information.

Note 5: The error amplifiers are measured in a feedback loop using an external servo operational amplifier that drives the V_{FB} pin and regulates V_{COMP} to be equal to the external control voltage.

Note 6: Guaranteed by design, not subject to test.

Note 7: The minimum on-time condition corresponds to an inductor peak-to-peak ripple current of 50% of I_{MAX}. See Applications Information for more details.

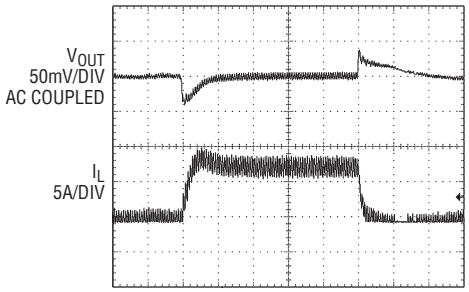
Note 8: The voltage positioning amplifier operates as a transconductance amplifier, where the input voltages are the $SENSE^+$ to $SENSE^-$ potentials for both channels. The amplifier output current flows through an external resistor in order to program the amount of voltage droop at full load.

Note 9: The PHASEMODE function is only available in the QFN package. The 36-lead GW package has a fixed channel 1-to-channel 2 phase relationship of 180°C and a channel 1-to-CLKOUT phase relationship of 90°C. The version in the 36-lead GW package is therefore optimized for 2- and 4-phase operation.

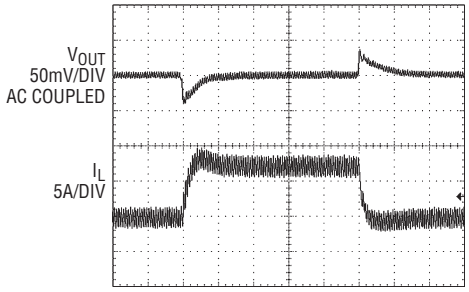
Note 10: Rise and fall times are measured at 10% and 90% levels.

TYPICAL PERFORMANCE CHARACTERISTICS

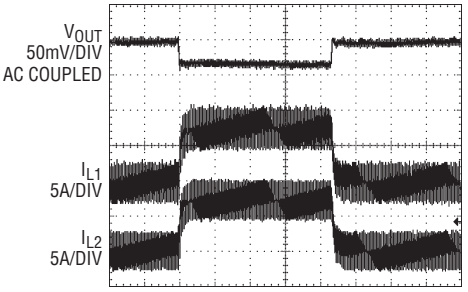
Load Step (Pulse Skip Mode)



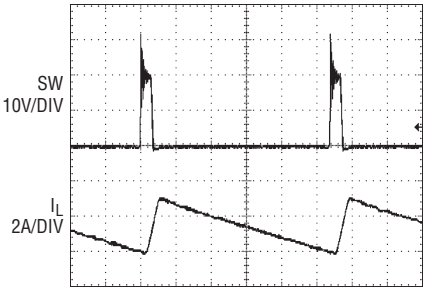
Load Step (Forced Continuous)



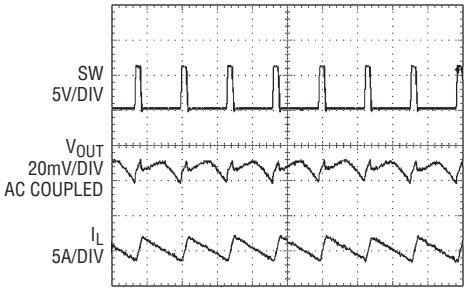
Load Step (Forced Continuous with Voltage Positioning)



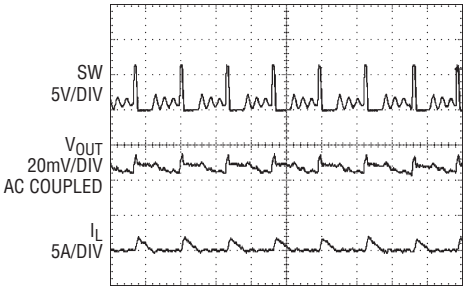
Low Duty Cycle Waveforms



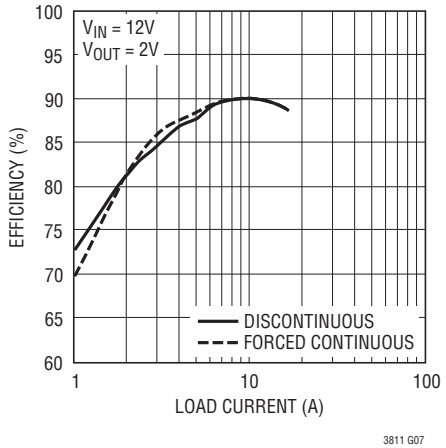
Light Load Waveforms (Forced Continuous Mode)



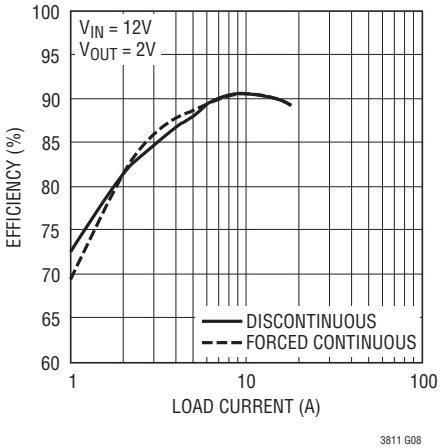
Light Load Waveforms (Pulse Skip Mode)



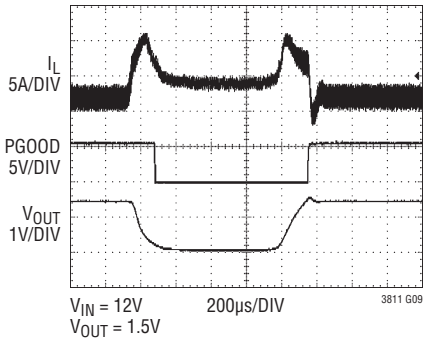
Efficiency vs Load Current with R_{SENSE} = 1.5mΩ



Efficiency vs Load Current with DCR Sensing

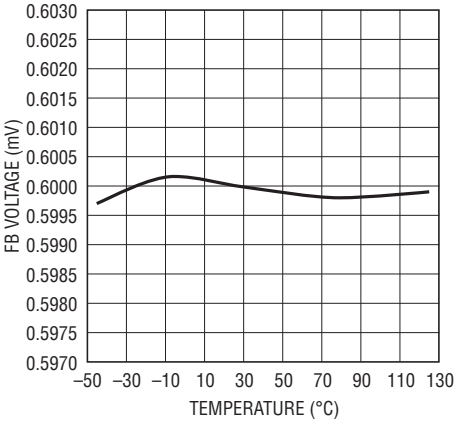


Short-Circut Waveforms

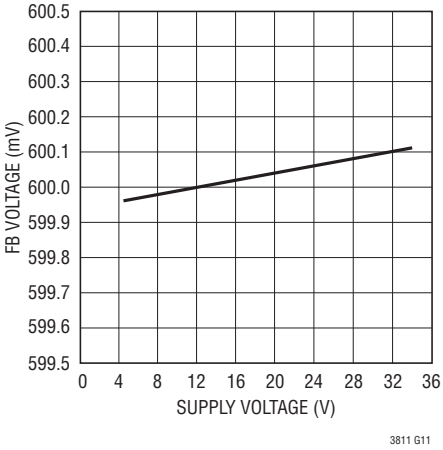


TYPICAL PERFORMANCE CHARACTERISTICS

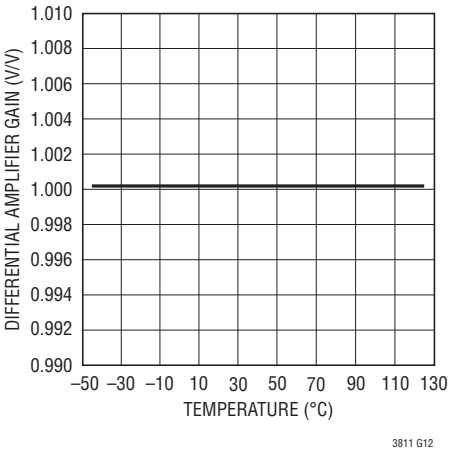
FB Voltage vs Temperature



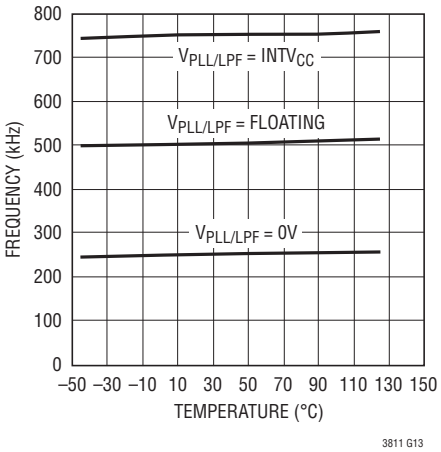
FB Voltage Line Regulation



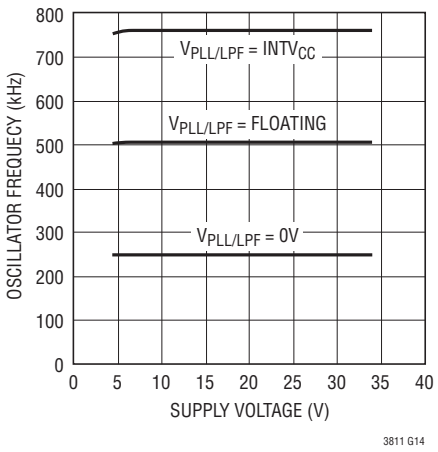
Differential Amplifier Gain vs Temperature



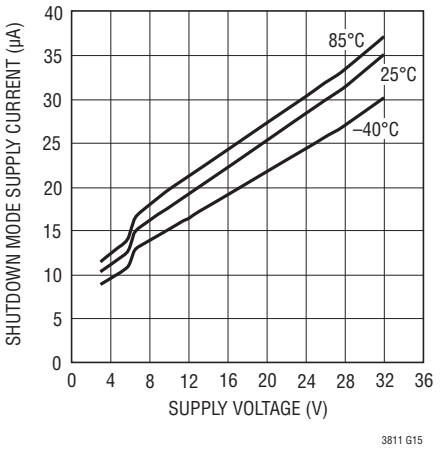
Oscillator Frequency vs Temperature



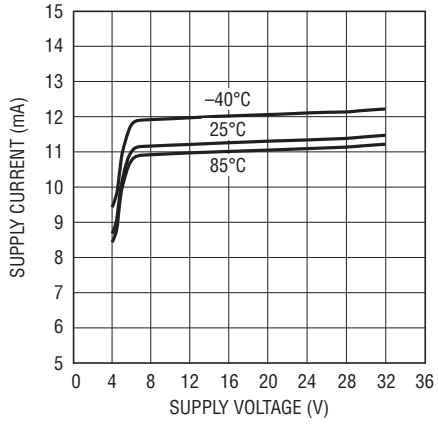
Oscillator Frequency vs Supply Voltage



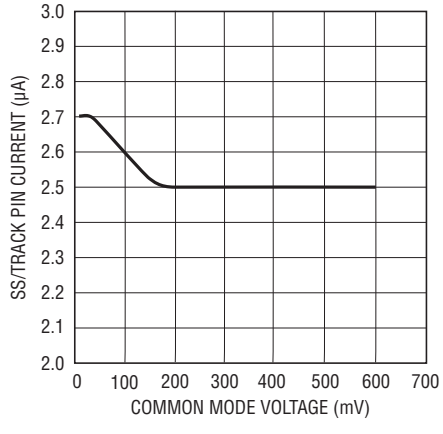
Shutdown Mode Supply Current vs Supply Voltage



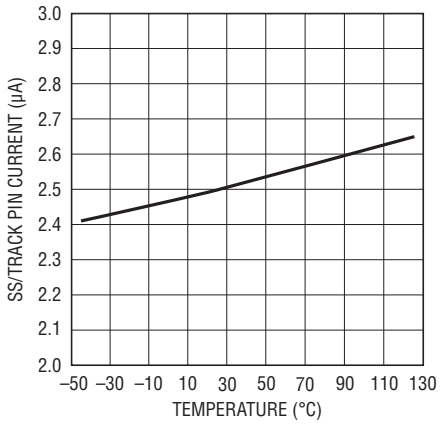
Supply Current vs Supply Voltage



SS/TRACK Pin Current vs Common Mode Voltage

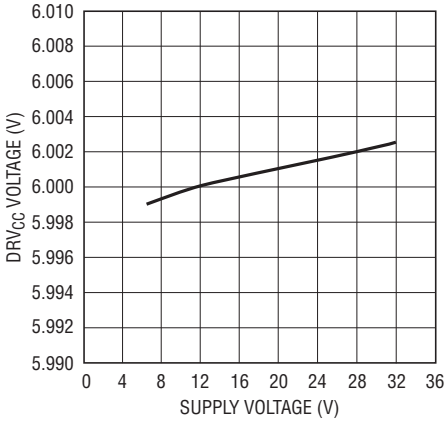


SS/TRACK Pin Current vs Temperature

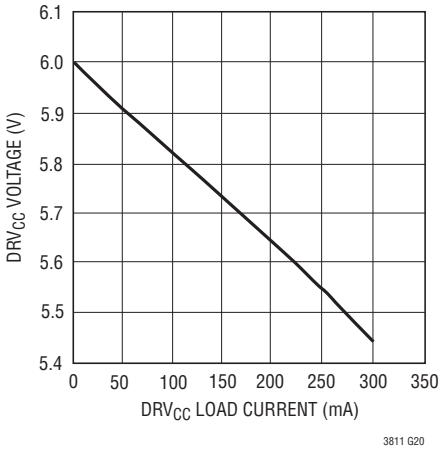


TYPICAL PERFORMANCE CHARACTERISTICS

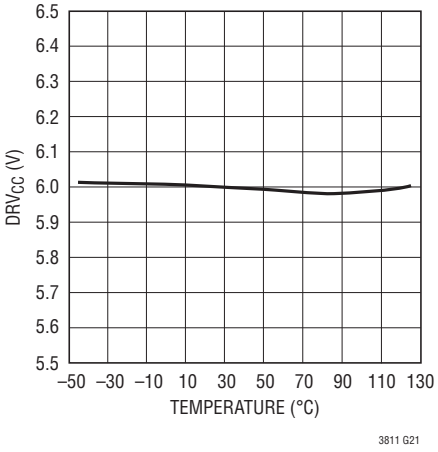
DRV_{CC} Line Regulation



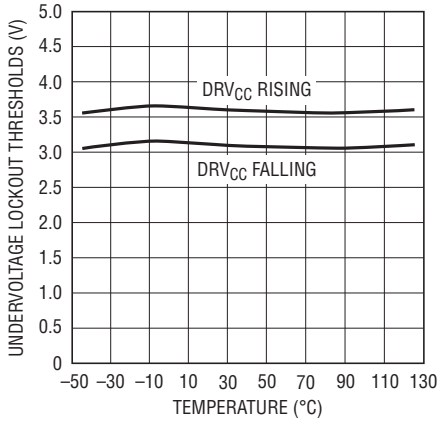
DRV_{CC} Load Regulation



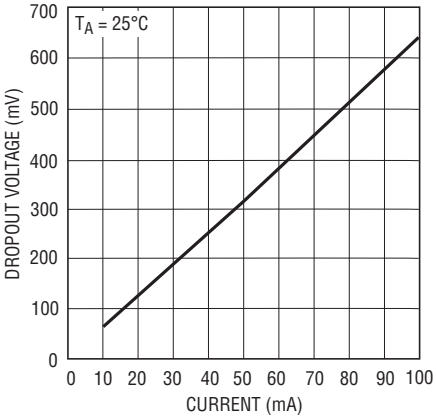
DRV_{CC} vs Temperature



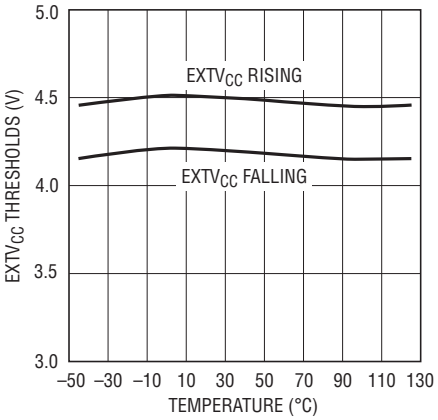
DRV_{CC} Undervoltage Lockout Thresholds vs Temperature



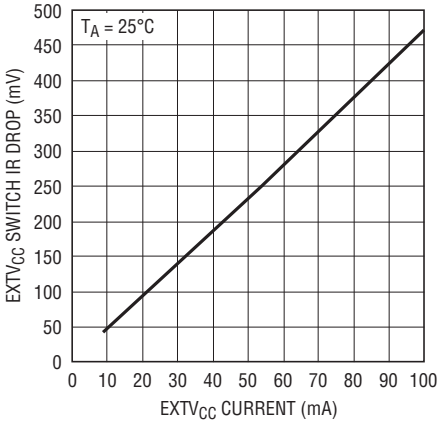
LDO Dropout Voltage vs Current



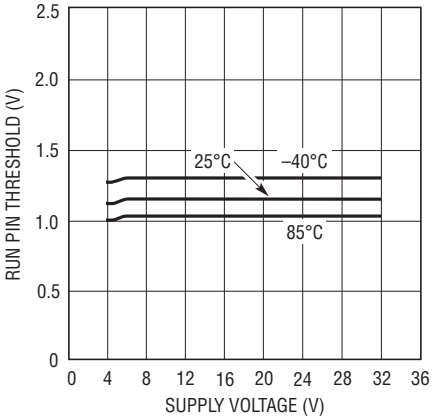
$EXTV_{CC}$ Thresholds vs Temperature



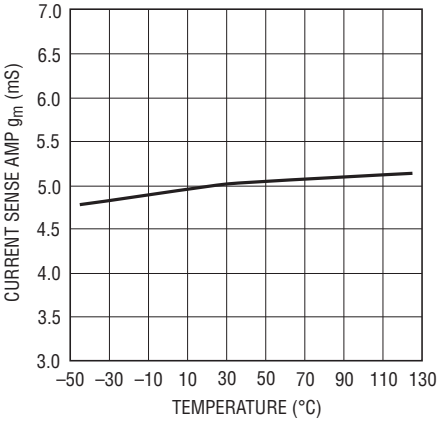
$EXTV_{CC}$ Switch IR Drop vs Current



RUN Pin Threshold vs Supply Voltage

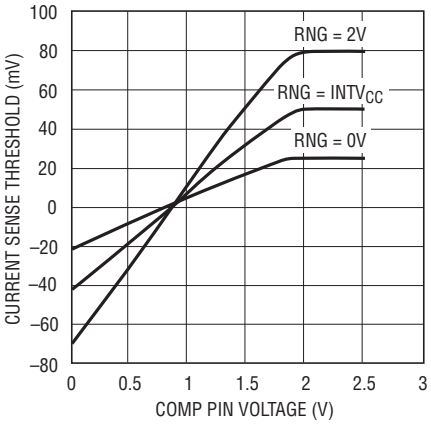


Current Sense Amplifier g_m vs Temperature

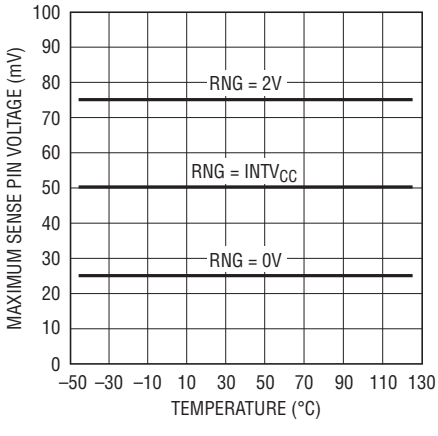


TYPICAL PERFORMANCE CHARACTERISTICS

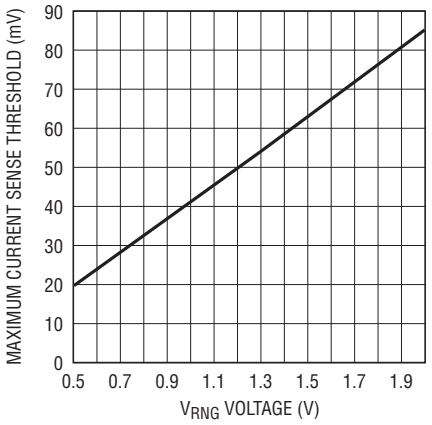
Current Sense Threshold vs COMP Pin Voltage



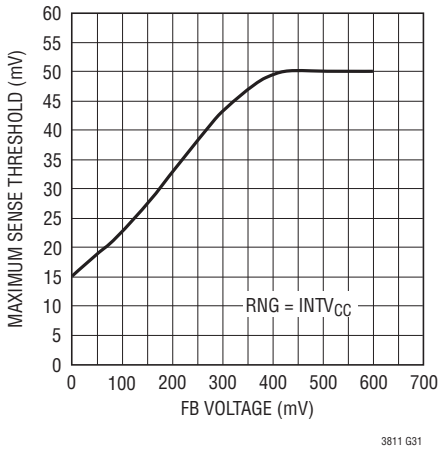
Maximum SENSE Pin Voltage vs Temperature



Maximum Current Sense Threshold vs V_{RNG} Voltage

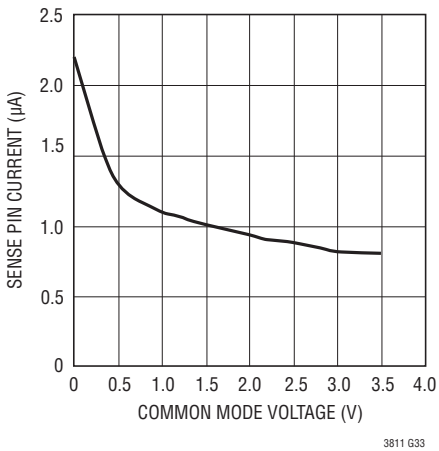


Foldback Current Limit

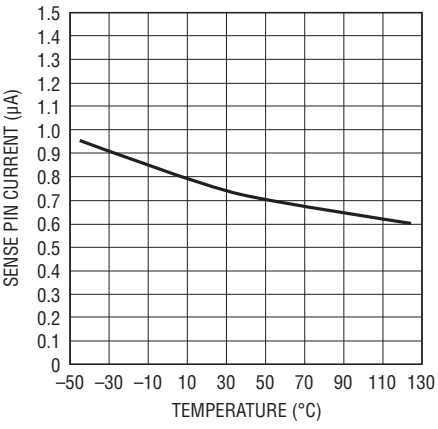


Maximum SENSE Pin Threshold vs Duty Cycle

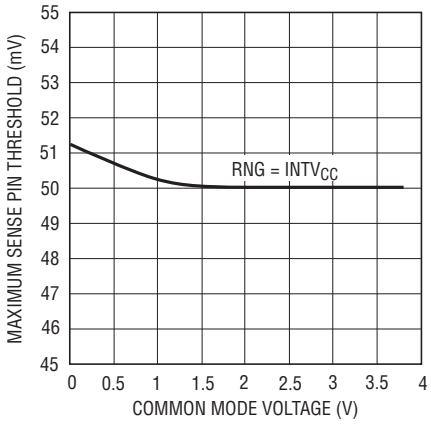
SENSE Pin Current vs Common Mode Voltage



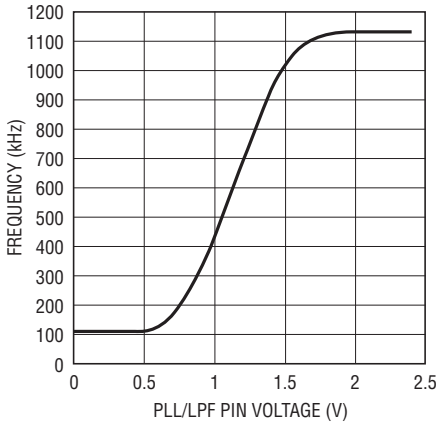
SENSE Pin Current vs Temperature



Maximum SENSE Pin Threshold vs Common Mode Voltage

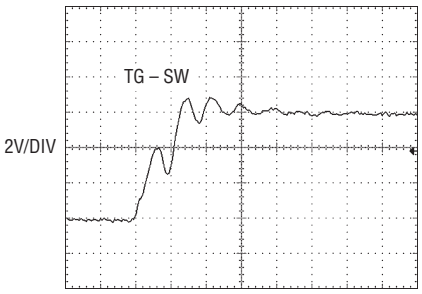


Frequency vs PLL/LPF Pin Voltage

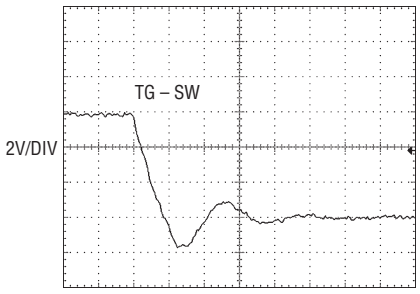


TYPICAL PERFORMANCE CHARACTERISTICS

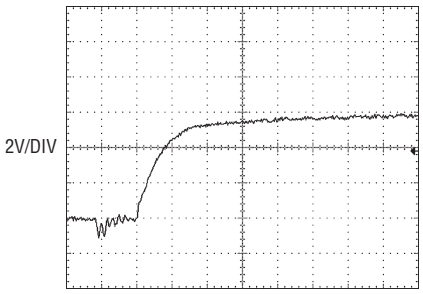
Top Gate Turn-On Waveform Driving Renesas RJK0305DPB



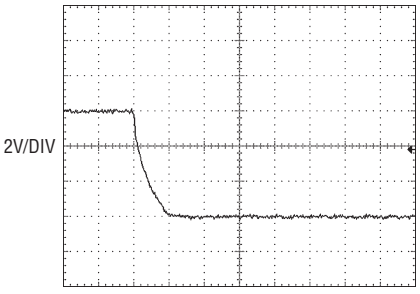
Top Gate Turn-Off Waveform Driving Renesas RJK0305DPB



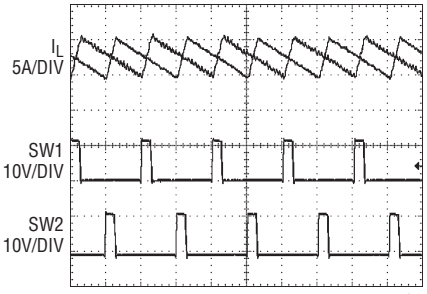
Bottom Gate Turn-On Waveform Driving Renesas RJK0301DPB



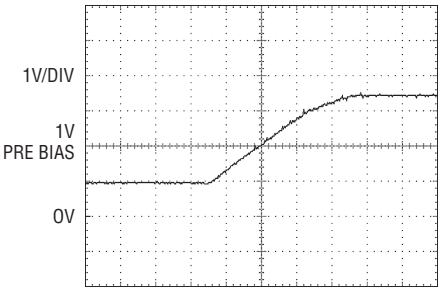
Bottom Gate Turn-Off Waveform Driving Renesas RJK0301DPB



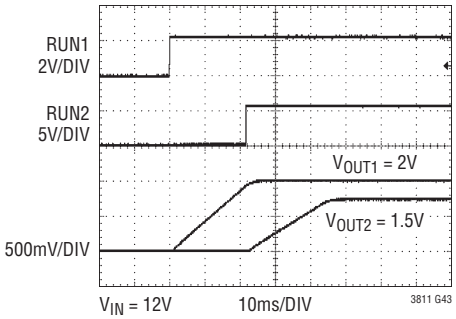
Single Output, 2-Phase Current Sharing Waveforms



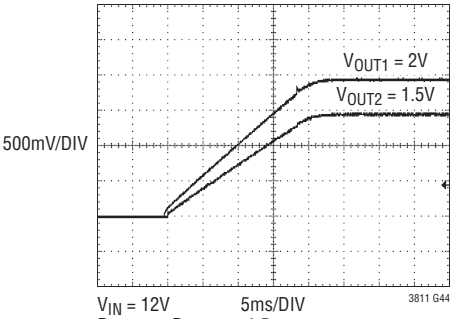
Start-Up Into a Pre-Biased Output Capacitor



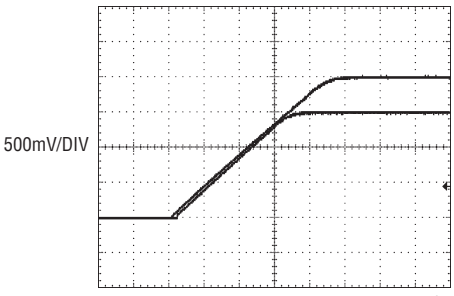
Sequenced Start-Up



Ratiometric Tracking Start-Up



Coincident Tracking Start-Up



PIN FUNCTIONS

BG1, BG2: High Current Gate Driver Outputs for the N-Channel Lower Power MOSFETs.

BOOST1, BOOST2: Bootstrapped Supply Inputs to the Topside Floating Drivers. A low ESR (X5R or better) ceramic bypass capacitor should be connected between the BOOST pin and the SW pin as close as possible to the IC.

CLKOUT: A Digital Output Used for Daisy-Chaining Multiple LTC3811 ICs in Multiphase Systems. The PHASEMODE pin voltage controls the phase relationship between the channel 1 TG signal and CLKOUT.

COMP1, COMP2: Error Amplifier Output Voltages. The error amplifiers in the LTC3811 are high bandwidth, low offset true operational amplifiers that have low output impedance. As a result, the outputs of two active error amplifiers cannot be directly connected together! For multiphase operation, connecting the FB pin of a slave error amplifier to $INTV_{CC}$ will disable the output of that amplifier. Multiphase operation can then be achieved by connecting all of the COMP pins together and using one channel as the master and all of the others as slaves. The FB and COMP pins are also used for compensating the control loop of the converter.

CSOUT (QFN Only): Output of the Voltage Positioning g_m Amplifier. This pin allows the user to program the amount of voltage droop in the output voltage at high load current. The output of the voltage positioning g_m amplifier is a bi-directional current proportional to the ($SENSE^+$ – $SENSE^-$) voltages for both channels. The g_m is internally fixed to 5mS. Forcing the g_m amplifier output current through a low value external resistor will program the amount of voltage droop seen at the output. See Applications Information for more details regarding voltage positioning.

DIFF/IN$^+$: Remote Sense Differential Amplifier Positive Input. A low offset, high bandwidth operational amplifier is configured with four precision 80k resistors for a non-inverting gain of one. This pin is normally connected to the positive terminal of the decoupling capacitor at the load.

DIFF/IN$^-$: Remote Sense Differential Amplifier Negative Input. This pin is normally connected to the negative terminal of the decoupling capacitor at the remote load. The DIFF/IN^+ and DIFF/IN^- PCB traces should be routed as close as possible and parallel to each other from the IC to the output capacitor.

DIFF/OUT: Remote Sense Differential Amplifier Output Voltage, Configured for a Noninverting Gain of One. The voltage at the DIFF/OUT pin is normally connected through an external resistor divider to the FB pin of one channel. The bottom of the divider should be connected to the SGND pin of the IC.

DRV_{CC}: Output of the Internal 6V Low Dropout Regulator (LDO), Supply Pin for the Bottom Gate Drivers and Output of the PMOS $EXTV_{CC}$ Switch. A low ESR (X5R or better) 4.7µF ceramic bypass capacitor should be connected between the DRV_{CC} pin and the PGND pin, as close as possible to the IC.

Exposed Pad (QFN Only): The Exposed Pad of the QFN Leadframe is PGND.

$EXTV_{CC}$: External Power Supply Input to an Internal PMOS Power Switch Connected Between $EXTV_{CC}$ (Drain) and DRV_{CC} (Source). This pin allows an external supply to be used for the high current gate drivers, thereby reducing power dissipation in the LDO and increasing efficiency. When $EXTV_{CC}$ exceeds 4.5V (rising), the high current PMOS switch turns on and shorts $EXTV_{CC}$ to DRV_{CC}, bypassing the internal LDO. See Applications Information for more details.

PIN FUNCTIONS

FB1, FB2: Error Amplifier Feedback Input Pins. The error amplifiers in the LTC3811 are high bandwidth, low offset true operational amplifiers. If differential remote sensing is not used, the FB pin should be connected to a resistor divider from the output of the power supply to SGND with the resistors placed close to the IC. In normal regulation the voltage at the FB pin is 0.6V. If remote sensing is used the FB pin should be connected to a resistor divider from the output of the differential amplifier to SGND. For multiphase operation, connecting the FB pin of a slave error amplifier to $INTV_{CC}$ will disable the output of that amplifier, allowing amplifier outputs to be connected in parallel.

$INTV_{CC}$: Supply Pin for All of the Internal Low Voltage Analog and Digital Control Circuitry, Electrically Isolated from the DRV_{CC} Pin. The $INTV_{CC}$ supply is normally derived by connecting a low value resistor (1Ω) from the output of the LDO (DRV_{CC}) to $INTV_{CC}$ and connecting a 0.1µF low ESR (X5R or better) ceramic bypass capacitor connected from $INTV_{CC}$ to SGND. This RC decoupling configuration prevents gate driver switching noise from coupling into the analog control circuitry. The $INTV_{CC}$ decoupling capacitor should be connected as close as possible to the IC pins.

MODE/SYNC: Mode Control and PLL Synchronization Input. This pin programs the operating mode and serves as the sync input to the internal phase-lock loop (PLL). Connecting this pin to $INTV_{CC}$ forces continuous operation (regardless of the load current) and connecting it to SGND allows discontinuous mode operation at light load. Applying an external clock between 175kHz and 900kHz will cause the operating frequency to synchronize to the clock.

PGND: Power Supply Return Path for the Bottom Side Gate Drivers, Connected to the Sources of the Lower Power MOSFETs. PGND should also be connected to the negative terminal of the DRV_{CC} decoupling capacitor as close as possible to the IC. PGND is electrically isolated from the SGND pin. The Exposed Pad on the bottom of the QFN package is PGND.

PGOOD1, PGOOD2: An Open-Drain NMOS Power Good Output. This output turns on, pulling down the PGOOD pin, when the FB voltage falls out of a ±10% regulation window. The PGOOD monitor circuit contains a 130µs nuisance filter to prevent short duration UV and OV transients from triggering the PGOOD output on, and a 30µs filter for the recovery from a fault condition.

PHASEMODE (QFN Only): The PHASEMODE pin voltage programs the phase relationship between the channel 1 and channel 2 rising TG signals, as well as the phase relationship between the channel 1 TG signal and CLKOUT.

PLL/LPF: Frequency Set and PLL Lowpass Filter Input. When not synchronized, this pin can be used to program the operating frequency. Connecting this pin to SGND forces 250kHz operation and connecting it to $INTV_{CC}$ forces 750kHz operation. Connecting the PLL/LPF pin to a voltage between 0.4V and 2V forces 500kHz operation. When synchronizing to an external clock, this pin serves as the lowpass filter input for the PLL. A series resistor and capacitor connected from PLL/PLF to SGND compensate the PLL feedback loop.

RNG1, RNG2: The voltage at this pin programs the sense voltage range for peak current mode control. Connecting this pin to SGND programs a peak sense voltage of 24mV and connecting it to $INTV_{CC}$ programs a peak sense voltage of 50mV. Alternatively, the sense voltage range can be linearly programmed by programming the RNG pin from 0.6V to 2V with a divider from $INTV_{CC}$ to SGND.

RUN1, RUN2: On/Off Input Pin for Each Controller.

$SENSE1^+$, $SENSE2^+$: Positive Inputs to the Current Comparators and Voltage Positioning g_m Amplifier. The COMP pin voltage programs the current comparator offset in order to set the peak current trip threshold. The LTC3811 is capable of sensing current using a discrete resistor in series with the inductor, or by indirectly sensing the voltage drop across the DCR of the inductor. See Applications Information for more details.

PIN FUNCTIONS

SENSE1⁻, SENSE2⁻: Negative Inputs to the Current Comparators and Voltage Positioning g_m Amplifier. The common mode input voltage range for the current comparators is 0V to 3.5V.

SW1, SW2: Bootstrapped Supply Return Paths for the Topside Gate Drivers, Connected to the Sources of the Upper Power MOSFETs.

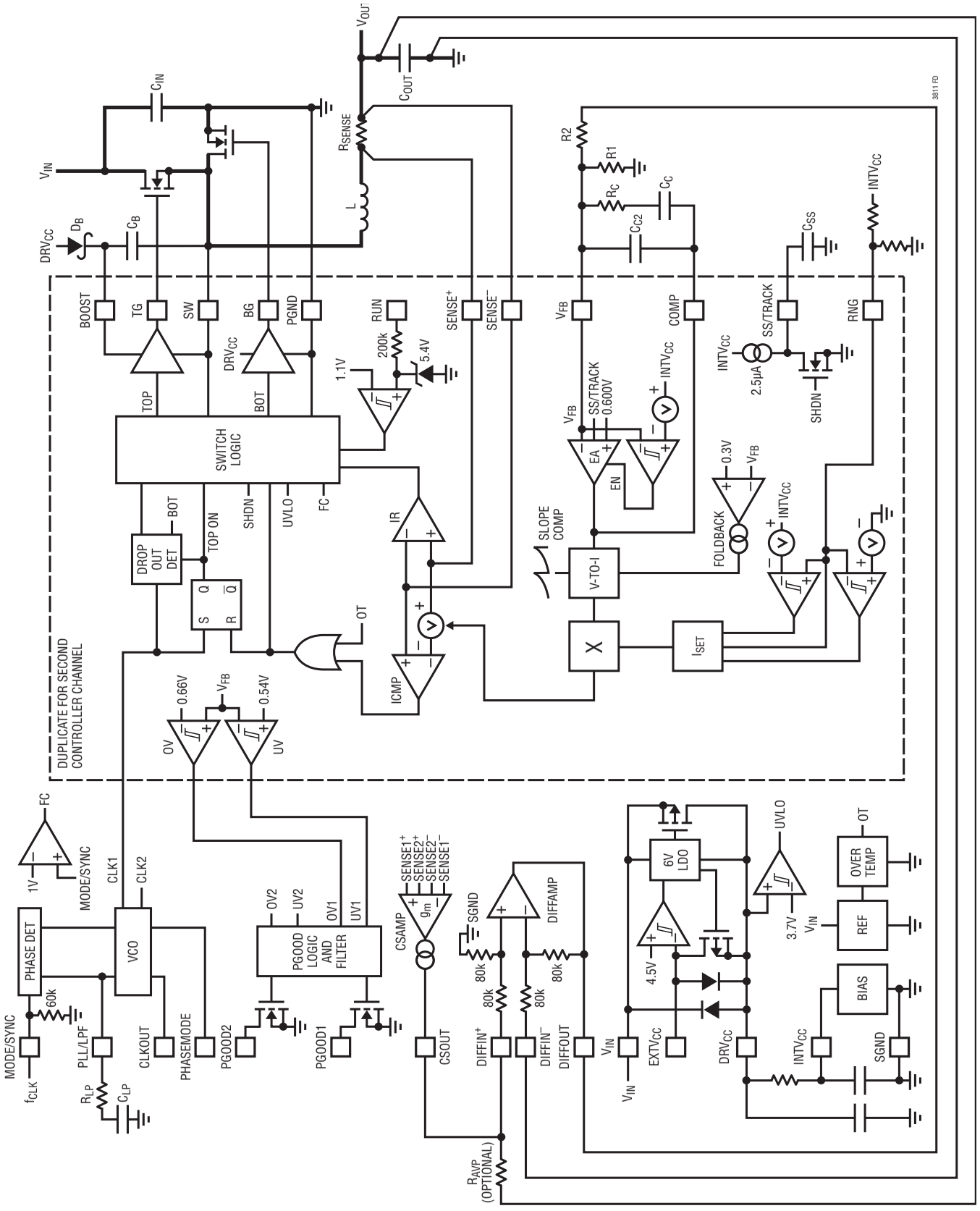
SGND: Signal Ground Pin for the IC. Common to both controllers, this pin should be connected to the negative terminals of the V_{OUT} and $INTV_{CC}$ decoupling capacitors and should be routed separately from any high current paths on the PC board.

SS/TRACK1, SS/TRACK2: Combined Soft-Start and Tracking Inputs. For soft-start operation, connecting a capacitor from this pin to ground will control the voltage ramp at the output of the power supply. An internal 2.5µA current source will charge the capacitor and thereby control an extra input on the reference side of the error amplifier. For tracking operation, this input allows the start-up of a secondary output to track a primary output according to a ratio established by a resistor divider from the primary output to the secondary error amplifier track pin. For coincident tracking of both outputs at start-up, a resistor divider with values equal to those connected to the secondary FB pin from the secondary output should be used to connect the secondary track input from the primary output.

TG1, TG2: High Current Gate Driver Outputs for the N-Channel Upper Power MOSFETs.

V_{IN}: Main Supply Input. A low ESR ceramic bypass capacitor should be connected between this pin and SGND.

FUNCTIONAL DIAGRAM



OPERATION (Refer to the Functional Diagram)

Main Control Loop

The LTC3811 uses a constant frequency peak current mode control architecture. During normal operation, the top MOSFET is turned on each cycle when the oscillator sets the PWM latch and turned off when the main current comparator (ICMP) resets the latch. The peak current at which comparator ICMP resets the latch is controlled by the voltage on the COMP pin, which is the output of the error amplifier. The remote sense amplifier (DIFFAMP) produces a signal equal to the differential voltage sensed across the output capacitor and re-references it to the local IC ground reference (SGND). The FB pin receives a portion of this voltage feedback signal and compares it to the internal 0.6V reference. When the load current increases it causes a slight decrease in the FB pin voltage relative to the 0.6V reference, which in turn causes the COMP pin voltage to rise until the average inductor current is equal to the load current.

The top MOSFET drivers are biased from a floating bootstrap capacitor, C_B, which is normally recharged during the off-time through an external Schottky diode. When V_{IN} decreases to a voltage close to V_{OUT}, however, the loop may enter dropout and attempt to turn on the top MOSFET continuously. A dropout detector senses this condition and forces the top MOSFET to turn off every 10th cycle for one third of a cycle to recharge the bootstrap capacitor.

Differences Between the QFN and G36 Package Options

The LTC3811 is offered in two package options, a 38-pin QFN and a 36-pin SSOP. The full featured QFN package option has no leads and an exposed lead frame that needs to be soldered to the PCB, whereas the 36-pin SSOP has leads and is therefore slightly easier to solder to a PCB and to debug in the lab.

The primary electrical difference between the QFN and SSOP options is the SSOP version lacks the CSOUT and PHASEMODE pins. With no CSOUT pin, the SSOP version has no provision for output voltage positioning. With no PHASEMODE input (it is internally connected to SGND), the SSOP version is limited to 2-phase and 4-phase applications.

In addition to differences in pinout, another difference between the two package options is their thermal resistance. The QFN package, by virtue of its exposed lead frame, has a junction-to-ambient thermal resistance of only 34°C/W, whereas the SSOP package has a thermal resistance of 100°C/W. The power dissipation of the IC is a function of the input voltage, the gate charge of the external power MOSFETs and the operating frequency. The gate charge losses can be partially mitigated by using the $EXTV_{CC}$ input to supply power to the IC, but users should beware that high input voltage applications using very high gate charge power MOSFETs, that also need to operate at high frequency, should only be attempted using the QFN package option. More details covering thermal management are given later in this data sheet.

Supplying Power to the LTC3811

The LTC3811 features several power supply input pins and multiple ways of supplying power to the gate drivers and low voltage analog control circuitry.

The first method of supplying power to the IC uses the internal low dropout linear regulator (LDO) that draws power from V_{IN} and regulates DRV_{CC} to 6V, as shown in Figure 1. The DRV_{CC} input supplies power to the internal gate drivers, which are capable of very high peak transient charge (1A) and discharge (5A) currents. The DRV_{CC} supply should be decoupled to PGND with a minimum of 4.7µF low ESR ceramic (X5R or better) capacitance. If multiple power MOSFETs are being driven in parallel for high current applications it is recommended that this capacitance

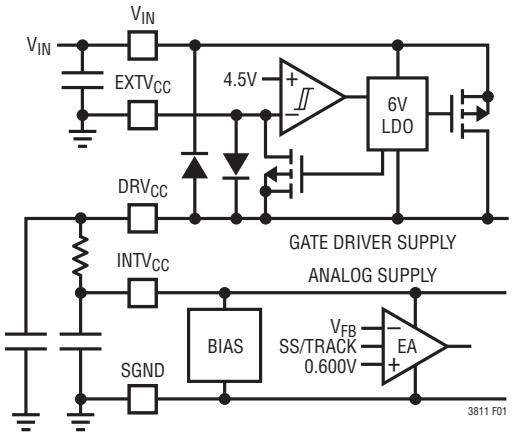


Figure 1. Supplying Power to the LTC3811 from V_{IN}

OPERATION (Refer to the Functional Diagram)

be increased to 10µF. Because of the high peak current capability of the gate driver, it is essential that this capacitor be placed as close as possible to DRV_{CC} and PGND pins, and on the same PCB layer as the IC.

The $INTV_{CC}$ pin supplies power to all of the low voltage analog circuitry and is electrically isolated from DRV_{CC}. The $INTV_{CC}$ supply is normally derived from DRV_{CC} through an RC filter, in order to prevent gate driver supply noise from coupling into sensitive analog control circuitry. Typical values for this RC filter consist of a 1Ω resistor from DRV_{CC} to $INTV_{CC}$ and a 0.1µF low ESR ceramic capacitor from $INTV_{CC}$ to SGND. The $INTV_{CC}$ capacitor should be placed as close as possible to the $INTV_{CC}$ and SGND pins and on the same PCB layer as the IC.

A third power supply pin, $EXTV_{CC}$, serves as an auxiliary input for applications where the power dissipation in the internal LDO is excessive, or where maximum efficiency is essential. This configuration is shown in Figure 2. When the $EXTV_{CC}$ pin is left open or is connected to a voltage less than 4.5V, the internal 6V LDO supplies DRV_{CC} power from V_{IN}. If $EXTV_{CC}$ is tied to an external power supply greater than 4.5V, however, the 6V LDO is turned off and power is supplied to DRV_{CC} through a 5Ω PMOS switch from $EXTV_{CC}$. For 4.5V < $EXTV_{CC}$ < 7V this PMOS switch is on and DRV_{CC} is approximately equal to $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the gate driver and control power to be derived from a high efficiency external source, dramatically reducing power dissipation on the IC.

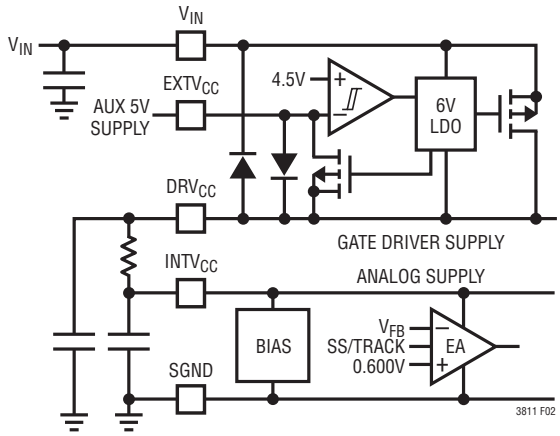


Figure 2. Supplying Power to the LTC3811 from $EXTV_{CC}$

Using an External 5V Supply to Measure Dynamic Quiescent Current

When a voltage above 4.5V is applied to the $EXTV_{CC}$ pin, the internal LDO in the LTC3811 is switched off and the power is supplied by the external 5V power supply as shown in Figure 2. Under these conditions, the quiescent current at the V_{IN} pin of the IC is very low (less than 1mA), and most of the current required to power the analog control circuitry and the gate drivers flows into the $EXTV_{CC}$ pin. As a result, this auxiliary supply can be used as a diagnostic tool in order to measure the total current for thermal calculations. In order to match the actual condition when the internal LDO is on, the voltage applied to $EXTV_{CC}$ when the measurements are taken should be 6V (the same as the regulated LDO output voltage).

Once the total quiescent current for the application is known, the power dissipation, P_D, on the IC will be approximately I_{EXTVCC} times V_{IN}, since the gate drive current and control circuitry quiescent current would be required to flow through the V_{IN} pin. The junction temperature of the IC can then be estimated using the following well-known formula:

$$T_J = T_A + (P_D \bullet R_{\theta JA})$$

If the maximum junction temperature is close to the Absolute Maximum Rating for the particular device being used, the use of an auxiliary supply and the $EXTV_{CC}$ pin may be required. Alternatively, lower gate charge MOSFETs should be used or the switching frequency should be reduced.

Operation at Low Supply Voltage

The LTC3811 control circuit has a minimum input voltage of 4.5V, making it a good choice for applications that experience low supply conditions. However, care should be taken to determine the minimum gate drive supply voltage in order to choose the optimum power MOSFETs. Important parameters that can affect the minimum gate drive voltage are the minimum input voltage (V_{IN}), the LDO dropout voltage, and the $EXTV_{CC}$ supply voltage, if an external gate drive supply is being used.

OPERATION (Refer to the Functional Diagram)

If the internal LDO is supplying power to the gate driver and the input voltage is low enough for the LDO to be in dropout, then the minimum gate drive supply voltage is:

$$V_{DRVCC} = V_{IN(MIN)} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total gate drive current and the quiescent current of the IC (typically 10mA). A curve of dropout voltage vs output current for the LDO is shown in the Typical Performance Characteristics. The temperature coefficient of the LDO dropout voltage is approximately +4000ppm/°C.

The total Q-current ($I_{Q(TOT)}$) flowing in the LDO is the sum of the controller quiescent current (typically 10mA) and the total gate charge drive current.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f$$

If an external supply is being used to supply power to the gate driver through the $EXTV_{CC}$ pin, then the minimum gate drive supply voltage is:

$$V_{DRVCC} = V_{EXTVCC} - I_{Q(TOT)} \bullet R_{EXTVCC}$$

The resistance of the internal $EXTV_{CC}$ PMOS switch is typically 5Ω at 25°C and has a temperature coefficient of approximately 3400ppm/°C.

After the calculations have been completed, it is important to measure the gate drive waveforms (BG-to-PGND and TG-to-SW) and the gate driver supply voltage (DRV_{CC}-to-PGND) over all operating conditions (low V_{IN}, mid V_{IN}, and high V_{IN}, as well as from light load-to-full load) to ensure adequate power MOSFET enhancement. Consult the power MOSFET data sheet to determine the actual $R_{DS(ON)}$ for the measured V_{GS}, and verify your thermal calculations by measuring the component temperatures using an infrared camera.

On/Off Control Using the RUN Pin

The two channels of the LTC3811 can be independently turned on and off using the RUN1 and RUN2 pins. Pulling either of these pins low shuts down the main control loop for that channel. Pulling both pins low disables both controllers and most of the internal circuitry, including the DRV_{CC} low dropout regulator (LDO). In shutdown mode (both RUN pins low) the LTC3811 typically draws only 20µA of current.

The RUN pins may be externally pulled up or driven directly by logic. Be careful not to exceed the 7V absolute maximum rating on this pin.

Soft-Start and Tracking Using the SS/TRACK Pin

The start-up of each controller's output voltage V_{OUT} is normally controlled by the voltage on the SS/TRACK pin for that channel. The SS/TRACK pin represents a 2nd noninverting input to the error amplifier, as shown in Figure 3. The error amplifier is configured so that the lower of the two noninverting inputs (the SS/TRACK pin or the 0.6V reference) controls the feedback loop. That is, when the voltage on the SS/TRACK pin is less than the 0.6V internal reference, the LTC3811 regulates the FB pin voltage to be approximately equal to the SS/TRACK pin voltage instead of the internal 0.6V reference. This allows the user to connect a capacitor from the SS/TRACK pin to SGND to program the soft-start of the power supply output. An internal 2.5µA current source charges this capacitor, creating a voltage ramp on the SS/TRACK pin. As the SS/TRACK pin voltage rises from 0V to 0.6V, the output voltage, V_{OUT}, rises smoothly from 0V to its final value. Once the soft-start interval is over, the internal 2.5µA current source will continue to charge the SS/TRACK capacitor up to a maximum voltage equal to $INTV_{CC}$.

Alternately, the SS/TRACK pin can be used to force the start-up of V_{OUT} to track the voltage of another supply. Typically, this requires connecting the SS/TRACK pin to an external divider from the other supply to ground (see Applications Information).

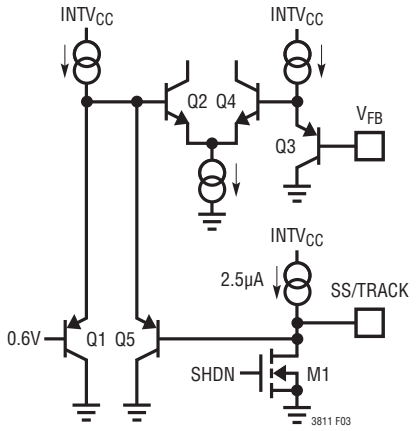


Figure 3. Simplified LTC3811 Error Amplifier Input Stage

OPERATION (Refer to the Functional Diagram)

The SS/TRACK pin has an internal open-drain NMOS pull-down transistor that turns on when the corresponding RUN pin is pulled low to disable that controller, when the voltage on the DRV_{CC} pin is below 3.7V (the rising undervoltage lockout threshold), or during an overtemperature condition. During an undervoltage lockout, UVLO, or overtemperature, OT, condition, both controllers are disabled and the external MOSFETs are held off.

In multiphase applications, one master error amplifier is used to control all of the phase current comparators. The FB pins for the unused error amplifiers are connected to $INTV_{CC}$ in order to three-state these amplifier outputs. As a result, the SS/TRACK pins for the unused error amplifiers should be left open.

Programming the Operating Mode

The MODE/SYNC pin serves to either program the operating mode or to synchronize the operating frequency to an external clock using the internal PLL. Connecting the MODE/SYNC pin to ground programs pulse-skip mode operation and connecting the pin to $INTV_{CC}$ programs forced continuous operation, as shown in Table 1. In pulse-skip mode the inductor current is not allowed to reverse, resulting in discontinuous mode, DCM, operation at light load. Pulse-skip mode is ideal for applications where light load efficiency is a higher priority than transient response. In forced continuous mode, the synchronous switch turns on after the primary switch turns off and remains on for the duration of the clock cycle, regardless of the load current. Forced continuous mode is ideal for applications needing optimized transient response, or for systems where constant frequency operation is important.

Certain applications can result in the startup of the converter into a non-zero load voltage, where residual charge is stored on the output capacitor at the onset of converter switching. In order to prevent a reversal of current in the inductor under these conditions, pulse-skip operation is asserted at startup until the FB pin reaches the lower PGOOD threshold of 0.54V. Once the FB pin voltage exceeds 0.54V, the operating mode is determined by the voltage on the MODE/SYNC pin.

When the operating frequency of the converter is synchronized to an external clock using the MODE/SYNC pin, the operating mode will always be forced continuous. Forcing continuous mode operation results in constant frequency operation and a more predictable noise spectrum from the converter.

Table 1

MODE/SYNC	OPERATING MODE	DESCRIPTION
SGND	Pulse-Skip	DCM Operation at Light Load
$INTV_{CC}$	Forced Continuous	CCM from No Load to Full Load
External Clock	Forced Continuous	Operating Frequency Synchronized Using Internal PLL (CCM)

Frequency Selection and the Phase-Lock Loop

The selection of the switching frequency is a tradeoff between efficiency, transient response and component size. Low frequency operation increases efficiency by reducing MOSEFT switching losses, but requires a larger inductor and output capacitor to maintain low output ripple.

The switching frequency of the LTC3811's controllers can be selected using the PLL/LPF pin. If the MODE/SYNC pin is not being driven by an external clock, the PLL/LPF pin can be tied to SGND, left open or tied to $INTV_{CC}$ to select 250kHz, 500kHz or 750kHz, respectively, as shown in Table 2.

Table 2

PLL/LPF	MODE/SYNC	FREQUENCY
SGND	0V or $INTV_{CC}$ (DC)	250kHz
Floating	0V or $INTV_{CC}$ (DC)	500kHz
$INTV_{CC}$	0V or $INTV_{CC}$ (DC)	750kHz
RC Filter to SGND	Connected to External Clock	Phase Locked to External Clock

A phase-lock loop is available on the LTC3811 to synchronize the internal oscillator to an external clock source connected to the MODE/SYNC pin. In this case, a series RC network connected from the PLL/LPF pin to SGND serves as the PLL's loop filter. The PLL/LPF pin is both the output of the phase detector and the input to the voltage controlled oscillator, VCO. The LTC3811 phase detector adjusts the voltage on the PLL/LPF pin to align the rising edge of TG1 to the leading edge of the external clock signal. The turn-on of the second channel TG2 will depend upon the voltage on the PHASEMODE pin as shown in the Electrical Characteristics.

OPERATION (Refer to the Functional Diagram)

The typical capture range of the LTC3811's PLL is approximately 125kHz to 1.1MHz, with a guarantee over all manufacturing variations to be between 175kHz and 900kHz. The amplitude of the sync pulse to the LTC3811 should be greater than 1.8V and the minimum pulse width should be greater than 200ns.

Using the CLKOUT and PHASEMODE Pins in Multiphase Applications

The LTC3811 features two pins (CLKOUT and PHASEMODE) that allow multiple LTC3811 ICs to be daisy-chained together in multiphase applications. The clock output signal on the CLKOUT pin can be used to synchronize additional power stages in a multiphase power supply solution feeding a single high current output or even separate outputs. The PHASEMODE pin is used to adjust the phase relationship between channel 1 and channel 2, as well as the phase relationship between channel 1 and CLKOUT, as summarized in Table 3. The phases are calculated relative to the zero degrees, defined as the rising edge of the top gate driver output of channel 1, TG1.

The PHASEMODE input comparators are referenced to an internal divider from $INTV_{CC}$ that has 33% and 67% $INTV_{CC}$ thresholds. For 6-phase operation, connect PHASEMODE to an external divider from $INTV_{CC}$ with equal value resistors (e.g., 100k), so that PHASEMODE is always 50% of $INTV_{CC}$.

Table 3

# PHASES	IC #	PHASEMODE	CLKOUT CONNECTS TO
2	1	0V	N/A
3	1	$INTV_{CC}$	MODE/SYNC of IC # 2
	2	0V	N/A
4	1	0V	MODE/SYNC of IC # 2
	2	0V	N/A
6	1	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	2	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	3	50% $INTV_{CC}$	N/A
12	1	50% $INTV_{CC}$	MODE/SYNC of IC # 2
	2	50% $INTV_{CC}$	MODE/SYNC of IC # 3
	3	0V	MODE/SYNC of IC # 4
	4	50% $INTV_{CC}$	MODE/SYNC of IC # 5
	5	50% $INTV_{CC}$	MODE/SYNC of IC # 6
	6	50% $INTV_{CC}$	N/A

Remote Sensing Using the Differential Amplifier

The LTC3811 has a differential amplifier for true remote sensing of the output voltage. The sensing connections should be returned from the load back to the differential amplifier's inputs through a common, tightly coupled pair of PCB traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PCB traces, as well as ground loop disturbances. The differential amplifier output signal is typically divided down and compared with the internal precision 0.6V voltage reference by the error amplifier.

The differential amplifier utilizes four precision internal resistors to enable instrumentation-type measurement of the output voltage. The amplifier has a gain of 1.000, contains a CMOS rail-to-rail output stage, and is optimized for low input offset and high bandwidth.

The output voltage is set by an external resistive divider according to the following formula:

$$V_{OUT} = 0.6 \bullet \left[1 + \frac{R2}{R1}\right]$$

where R2 and R1 are the upper and lower divider resistors, respectively. The differential amplifier was optimized for divider currents in the range of 100µA to 600µA, meaning that R1 in the equation above should be 1k to 6k.

Using the LTC3811 Operational Error Amplifiers in Multiphase Applications

The LTC3811 error amplifiers are true operational amplifiers, meaning that they have high DC gain and low output impedance. In previous generations of multiphase controllers, such as the LTC1628 family, the error amplifiers were transconductance amplifiers, meaning that they could be connected in parallel for multiphase applications.

Multiphase applications using the LTC3811 will use one operational error amplifier as the master and will disable all of the slave phase error amplifiers. Typically, the channel 1 amplifier for phase = 0° will be used as the master and phases 2 through n (up to 12 phases) will serve as slaves. To disable the slave error amplifiers but still use their current comparators and power stages, connect the

OPERATION (Refer to the Functional Diagram)

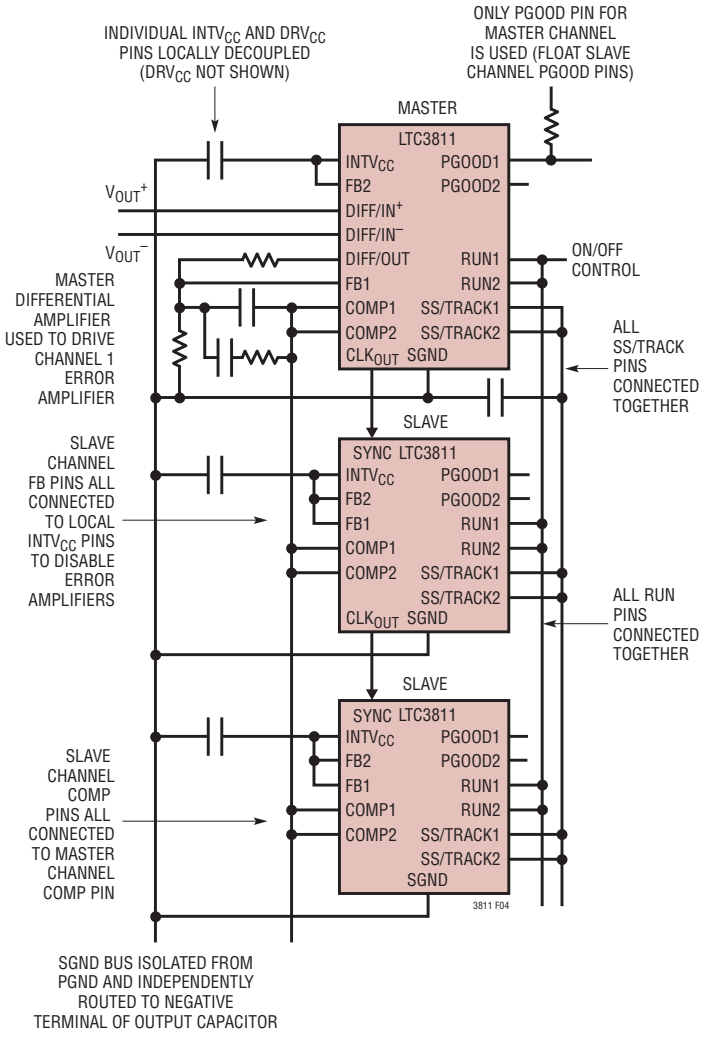


Figure 4. LTC3811 Error Amplifier Configuration for Multiphase Operation

FB pin of a slave phase to $INTV_{CC}$. As shown in the Functional Diagram, a comparator detects when the FB pin is shorted to $INTV_{CC}$ and three-states this amplifier's output and input. The COMP pins for all of the phases can then be shorted together in order to provide compensation for the feedback loop, as shown in Figure 4.

Theory and Benefits of Multiphase Operation

Why the need for multiphase operation? Up until the multiphase family, constant frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor.

With multiphase operation, the two channels of the dual-switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. *The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.*

Figure 5 illustrates the benefits of multiphase operation. Current ripple at the input is reduced by a factor of 1.41 (square root of 2), reducing the size and cost of the input capacitor. In addition, since power losses are proportional to I_{RMS}^2, significant efficiency improvements in the input power path components (batteries, switches, protection circuitry and PCB traces) can be achieved. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current.

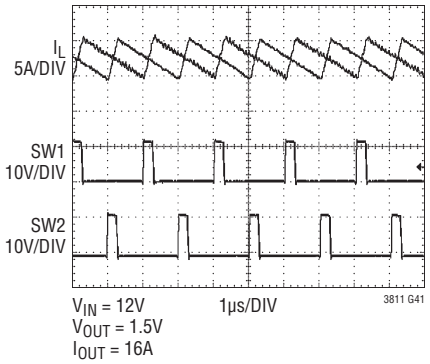


Figure 5. 2-Phase, Single Output Current Sharing Waveforms

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}).

Figure 6 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the

OPERATION (Refer to the Functional Diagram)

x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. As shown in Figure 6, the zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \quad \text{where } k = 1, 2, ..., N-1$$

So the number of phases used can be selected to minimize the output ripple current and therefore the output ripple voltage at the given input and output voltages. In applications having a highly varying input voltage, additional phases will produce the best results.

Accepting larger values of ΔI_L allows the use of low inductances, but can result in higher output voltage ripple. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4(I_{OUT})/N$, where N is the number of channels and I_{OUT} is the total load current. Remember, the maximum ΔI_L occurs at the maximum input voltage. The individual inductor ripple currents are constant determined by the inductor, input and output voltages.

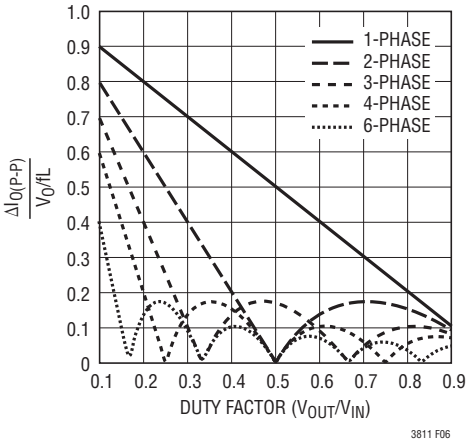


Figure 6. Normalized Peak Output Current vs Duty factor [$I_{RMS} \approx 0.3(\Delta I_{O(P-P)})$]

Power Good Pins (PGOOD1, PGOOD2)

Each PGOOD pin is connected to the open drain of an internal N-channel pull-down MOSFET. The MOSEFT turns on and pulls the PGOOD pin low when the corresponding FB pin is outside a ±10% window around the 0.6V reference voltage. The PGOOD pin is also pulled low when the corresponding RUN pin is low, or during an undervoltage lockout or overtemperature condition. When the FB pin voltage is within the ±10% window, the internal PGOOD MOSFET is turned off and the pin is normally pulled up by an external resistor. The absolute maximum voltage rating of the PGOOD pins is 7V.

The PGOOD logic contains separate filters depending on whether the controller is entering or exiting a fault condition. When the FB pin is exiting a fault condition (such as during normal output voltage start-up, prior to regulation), the PGOOD pin will remain low for an additional 30µs. This allows the output voltage to reach steady-state regulation and prevents the enabling of a heavy load from re-triggering a UVLO condition. When the FB pin is entering either an undervoltage, UV, or overvoltage, OV, fault condition, the PGOOD pin will remain high 130µs after the onset of the fault. This non-integrating filter prevents noise or short duration overload conditions from triggering the PGOOD outputs and causing a false system reset. Figure 7 illustrates the timing diagram for a hypothetical undervoltage event on the FB pin, and the resulting PGOOD waveform.

In multiphase applications, one error amplifier is used to control all of the phase current comparators. In addition, since the FB pins for the unused error amplifiers are connected to $INTV_{CC}$ (in order to three-state these amplifiers), the PGOOD outputs for these amplifiers will be asserted. In order to prevent falsely reporting a fault condition, the

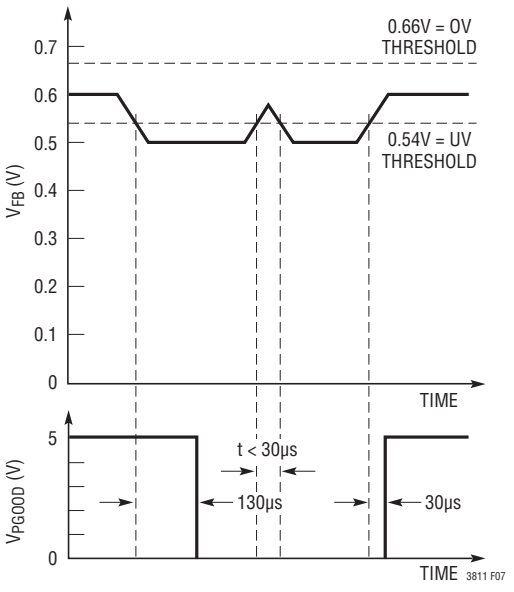


Figure 7. PGOOD Filter Timing Diagram

OPERATION (Refer to the Functional Diagram)

PGOOD outputs for the unused error amplifiers should be left open. Only the PGOOD output for the master control error amplifier should be connected to the fault monitor.

Fault Conditions: Current Limit and Foldback

One of the main advantages of the LTC3811 is the fact that the maximum inductor current is inherently limited due to the use of peak current mode control. The maximum sense voltage is controlled by the voltage on the RNG pins and the maximum DC output current is:

$$I_{LIMIT} = \frac{V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \bullet \Delta I_L$$

The current limit value should be checked to ensure that $I_{LIMIT(MIN)} > I_{OUT(MAX)}$. The minimum value of the current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the largest power losses in the converter.

To further limit current in the event of an output short-circuit to ground, the LTC3811 includes foldback current limiting. When the FB pin falls below 0.3V (50% of its nominally regulated value), the foldback circuit is activated, progressively lowering the peak current limit in proportion to the severity of the overcurrent or short circuit condition. If the FB pin reaches 0V, the peak current sense threshold will be reduced to 30% of its maximum value. The foldback current limit transfer function is shown in Figure 8.

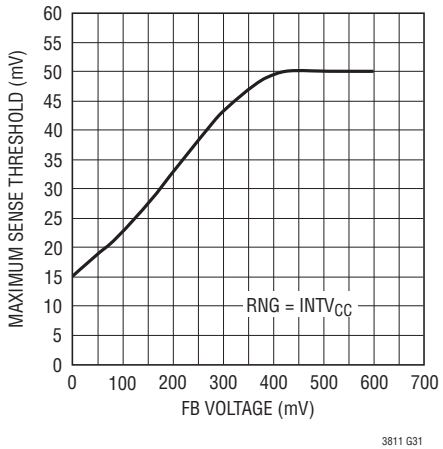


Figure 8. Current Foldback Charactistic

Under short-circuit conditions with very low duty cycles, the LTC3811 may begin to skip pulses in order to limit the maximum current. In this situation the bottom MOSFET will be dissipating most of the power; however this will be less than in normal operation at maximum load. In this case the short circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of the LTC3811 (about 65ns), the input voltage, and the inductor value, according to the following equation:

$$\Delta I_{L(SC)} = t_{ON(MIN)} \bullet \frac{V_{IN}}{L}$$

The resulting short-circuit current is

$$I_{SC} = \frac{0.3 \bullet V_{SENSE(MAX)}}{R_{SENSE}} - \frac{1}{2} \bullet \Delta I_{L(SC)}$$

Depending upon the ratio of the DC value of the current limit to the maximum load current and the percentage ripple current in the inductor, it is possible that the converter will operate in discontinuous mode when V_{FB} = 0V (a so-called “dead short”). In this case, the short-circuit current of the converter will be:

$$I_{SC} = \frac{\Delta I_{L(SC)}}{2} = t_{ON(MIN)} \bullet \frac{V_{IN}}{2 \bullet L}$$

In order for the converter to start up properly with a nonlinear load, the foldback current limiting circuit in the LTC3811 is disabled during the initial soft-start interval. When the FB pin voltage reaches 0.54V, the soft-start interval is terminated and the foldback circuit is enabled.

In the event the converter is turned on into a shorted load, the foldback circuit will be disabled until the SS/TRACK pin reaches 0.54V. This ensures that the converter will still limit the maximum current to a safe level and reduce the peak power dissipated with a shorted load.

APPLICATIONS INFORMATION

Duty Cycle Considerations

The duty cycle for a buck converter is well known:

$$D = \frac{V_{OUT}}{V_{IN}} = t_{ON} \bullet f$$

Rearranging, the minimum on-time for a given application can be calculated:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)} \bullet f}$$

For a given input and output voltage, it is important to know how close the minimum on-time of the application comes to the minimum on-time of the control IC. The LTC3811 has a typical minimum on-time of 65ns, allowing both high input to output ratios and high frequency operation.

In an application circuit, if the IC's minimum on-time exceeds the value required in the duty cycle equations, the converter will begin to skip pulses and operate at a fraction of the intended frequency. This frequency division will result in higher current and voltage ripple and is of particular concern in forced continuous applications with low ripple currents at light loads.

Setting the Output Voltage

The LTC3811 output voltages are each set by external feedback resistor dividers, according to the following equation:

$$V_{OUT} = 0.6V \bullet \left[1 + \frac{R2}{R1}\right]$$

Care should be taken to place the output divider resistors and the compensation components as close as possible to the IC FB and SGND pins, in order to prevent switching noise from coupling into the signal path. This configuration is shown in Figure 9. The top of R2 is normally routed to the top of the output capacitor, or to the output of the differential amplifier, if remote sensing is being employed.

Because the common mode range of the current comparator input stages is 0V to 3.5V, the output voltage range is limited from 0.6V to 3.3V.

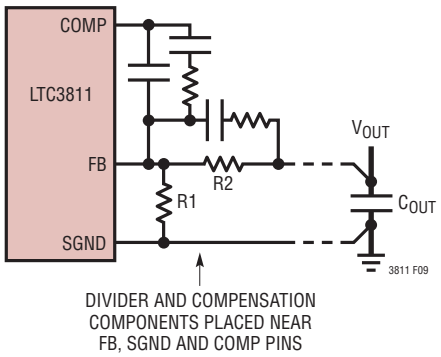


Figure 9. Output Divider and Compensation Component Placement

Sensing the Output Voltage with a Differential Amplifier

The LTC3811 includes a low offset, unity gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing both SENSE$^+$ and SENSE$^-$ greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget.

The LTC3811 differential amplifier has a typical output slew rate of 8V/µs and has rail-to-rail output drive capability. The amplifier is configured for unit gain, meaning that the difference between SENSE$^+$ and SENSE$^-$ is translated to DIFFOUT, relative to SGND.

Care should be taken to route the SENSE$^+$ and SENSE$^-$ PCB traces parallel to each other all the way to the terminals of the output capacitor or remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the SENSE$^+$ and SENSE$^-$ traces should be shielded by a low impedance ground plane to maintain signal integrity.

Choosing the Inductor Value and Saturation Current Rating

The operating frequency and inductor value are interrelated in that higher operating frequencies allow the use of smaller inductors and capacitors. Higher frequency operation also results in higher switching and gate drive losses, so a basic tradeoff exists between size and efficiency.

APPLICATIONS INFORMATION

For CCM operation, the inductor value can be chosen using the following equation:

$$L = \frac{V_{OUT}}{f \bullet \Delta I_L}\left[1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right]$$

Choosing a larger value of ΔI_L allows the use of a lower value inductor, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting the ripple current is 40% to 50% of the maximum output current, or:

$$\Delta I_L = 0.4 \bullet I_{OUT(MAX)}$$

The inductor saturation current rating needs to be higher than the peak inductor current during an overload condition. If $I_{OUT(MAX)}$ is the maximum rated load current, then the maximum overload current, I_{MAX}, would normally be chosen to be some factor (e.g., 30%) greater than $I_{OUT(MAX)}$:

$$I_{MAX} = 1.3 \bullet I_{OUT(MAX)}$$

$$I_{L(PK)} = I_{MAX} + \frac{1}{2} \bullet \Delta I_L$$

For a 40% ripple application, the minimum saturation current rating of the inductor would therefore be:

$$I_{L(PK)} = 1.5 \bullet I_{O(MAX)}$$

In other words, for an application with 40% inductor ripple current and a maximum output current 30% greater than the full load current, the inductor's saturation current rating needs to be at least 1.5 times the maximum output current.

Inductor Core Selection

Once the value of L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core losses found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but is very dependent on the inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core materials exhibit "hard" saturation, meaning that the inductance collapses abruptly when the peak current capability is exceeded. This results in an abrupt increase in inductor ripple current and output voltage ripple. **Do not allow the core to saturate!**

Programming the Maximum Sense Voltage Using the RNG Pin

The RNG pin can be used in two different ways in order to program the maximum peak current sense voltage. The easiest way to program the peak sense voltage is to tie the RNG pin to either ground or $INTV_{CC}$. Connecting the RNG pin to ground results in a 24mV peak sense voltage and connecting it to $INTV_{CC}$ programs in a 50mV peak sense voltage. Alternately, an external resistor divider from $INTV_{CC}$ to ground can be used to set the RNG pin between 0.6V and 2V, resulting in a nominal peak sense voltage range of 24mV to 85mV. Figure 10 illustrates the transfer function from the RNG pin to the peak sense voltage, which closely follows the following equation for $0.6V < V_{RNG} < 2V$:

$$V_{SENSE(MAX)} = 0.0436 \bullet V_{RNG} - 0.0022$$

In general, the accuracy of the SENSE pin threshold will scale with the peak sense voltage defined by the RNG

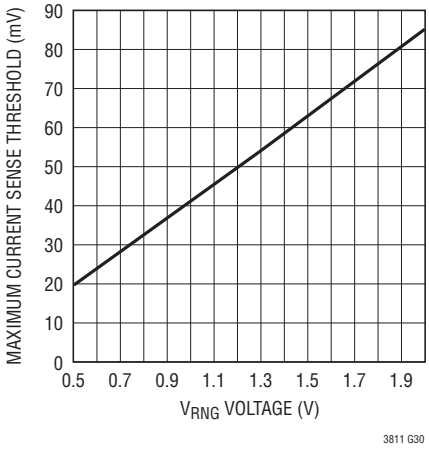


Figure 10. Maximum Current Sense Threshold vs RNG Pin Voltage

APPLICATIONS INFORMATION

pin. For applications requiring maximum current limit accuracy, a higher peak sense voltage (e.g., 85mV) should be chosen. An additional benefit of a higher peak SENSE pin threshold is a slight reduction in the minimum on-time of the controller. That is, for a given ripple current in the inductor, a higher peak sense voltage results in higher SENSE pin dV/dt, speeding up the input stage of the current comparator slightly. For applications where high efficiency and tight current limit accuracy are both important, the peak current sense voltage can be reduced to as low as 24mV.

In multiphase applications, only one error amplifier is used to control all of the phase current comparators. As a result, in multiphase applications all of the RNG pins should all be tied to the same potential, in order to program the same power stage g_m for each phase.

SENSE+ and SENSE– Pins

The common mode input voltage range of the current comparators is 0V to 3.5V. Continuous linear operation is provided throughout this range, allowing output voltages between 0.6V (the reference input to the error amplifiers) and 3.3V. The SENSE+ and SENSE– pins are also the inputs to the voltage positioning current sense g_m amplifier. Under normal operation, a small current of about 1.5µA flows out of the SENSE inputs and represents the total base current of the two vertical PNP input stages (one in the current comparator and one in the voltage positioning current sense amplifier). When the common mode voltage is lower than about 0.4V, the current flowing out of the SENSE pins increases, up to about 2.2µA at V_{SENSE} = 0V. Figure 11 illustrates the change in the SENSE pin current as a function of common mode voltage.

Sensing Techniques Using Low Value Resistors

For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 24mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible.

A typical sensing circuit using a discrete resistor is shown in Figure 12. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

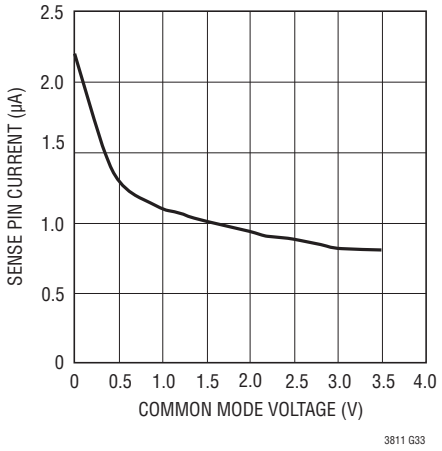


Figure 11. SENSE Pin Input Bias Current vs Common Mode (Output) Voltage

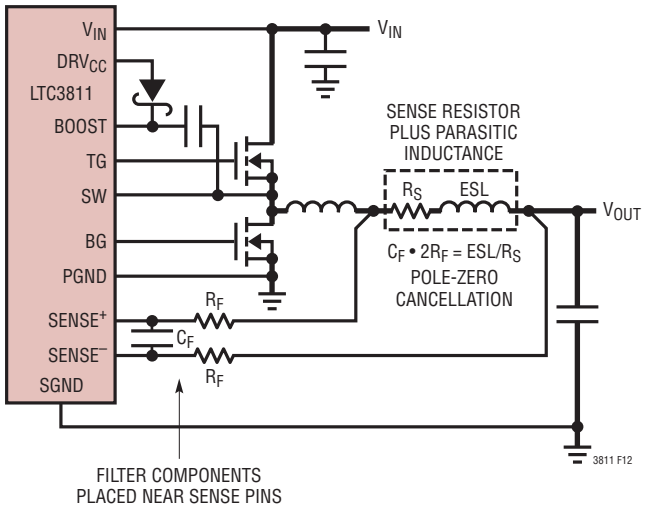


Figure 12. Using a Resistor to Sense Current with the LTC3811