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Single-Phase Wide V_{IN} Range DC/DC Controller for Intel IMVP-6/IMVP-6.5 CPUs

FEATURES

- **Supports 7-Bit IMVP-6/IMVP-6.5 VID Code and Features**
- **Wide V_{IN} Range: 4.5V to 36V Operation with Optional Line Feedforward Compensation**
- **$t_{ON(MIN)}$ < 35ns, Capable of Very Low Duty Cycle**
- **Temperature Compensated Inductor DCR or Sense Resistor Output Current Monitoring**
- **Differential Remote Output Voltage Sensing with Programmable Active Voltage Positioning**
- Phase-Lockable Fixed Frequency: 150kHz to 550kHz
- Programmable UVLO, Preset V_{OUT} at Boot-Up
- Programmable Slow Slew Rate Sleep State Exit
- Internal LDO for Single Supply Operation
- Overvoltage and Overcurrent Protection
- PWRGD and VRTT# Thermal Throttling Flags
- Power Optimization During Sleep and Light Load
- 38-Pin Thermally Enhanced eTSSOP and 5mm × 7mm QFN Packages

APPLICATIONS

- Embedded Computing
- Mobile Computers, Internet Devices
- Navigation Displays

DESCRIPTION

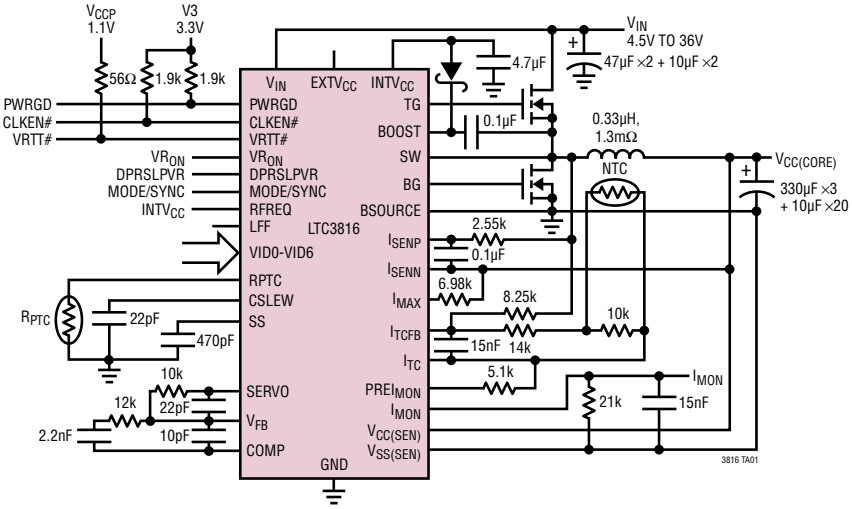
The LTC®3816 is a single-phase synchronous step-down DC/DC switching regulator controller that drives N-channel power MOSFETs in a constant-frequency voltage mode architecture. The controller's leading edge modulation topology allows extremely low output voltages and supports a phase-lockable switching frequency up to 550kHz. The output voltage is programmed using a 7-bit VID code.

The LTC3816 features all of the IMVP-6/IMVP-6.5 requirements, including start-up to a preset boot voltage, differential remote output voltage sensing with programmable active voltage positioning, I_{MON} output current reporting, power optimization during sleep state, and fast or slow slew rate sleep state exit.

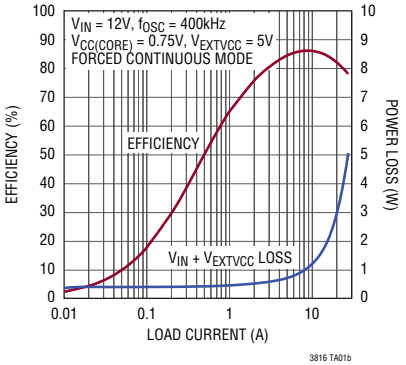
Fault protection features include input undervoltage lockout, cycle-by-cycle current limit, output overvoltage protection, and PWRGD and overtemperature flags.

TYPICAL APPLICATION

High Efficiency, Synchronous IMVP-6/ IMVP-6.5 Step-Down Controller



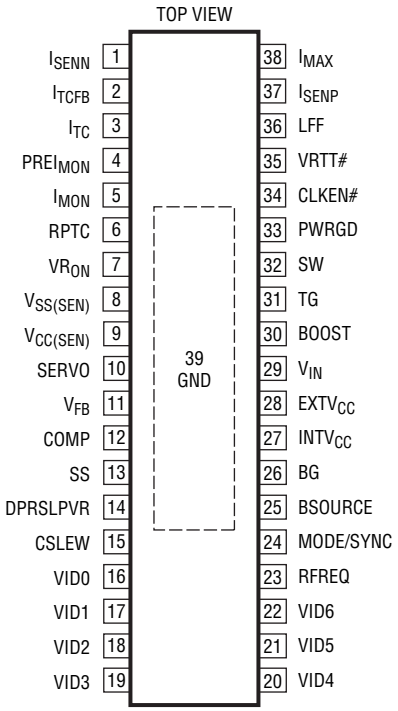
Efficiency and Power Loss vs Load Current



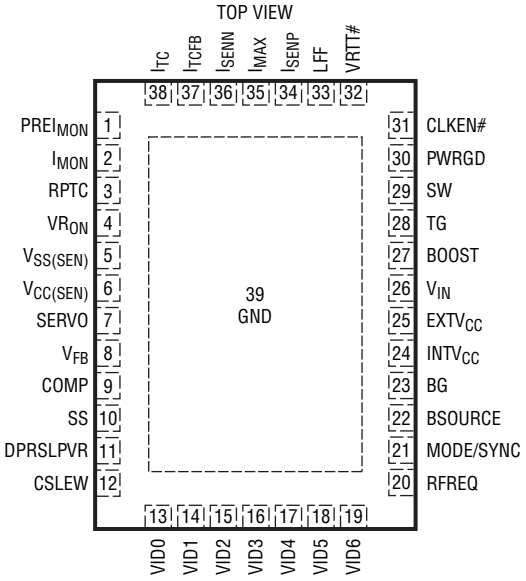
ABSOLUTE MAXIMUM RATINGS (Notes 1, 8)

Input Supply Voltage (V_{IN}) ..... –0.3V to 40V
Topside Driver Voltage (BOOST) ..... –0.3V to 46V
Switch Voltage (SW) ..... –5V to 40V
$INTV_{CC}$, $EXTV_{CC}$, (BOOST-SW) ..... –0.3V to 6V
I_{SENN}, I_{TCFB}, $PREI_{MON}$, I_{MON}, RPTC, VR_{ON}, $V_{CC(SEN)}$, V_{FB}, SS, VID*n*, RFREQ, MODE/SYNC, LFF, I_{SENP}, I_{MAX} ..... –0.3V to $INTV_{CC}$ + 0.3V
PWRGD, CLKEN# ..... –0.3V to 6V
DPRSLPVR, VRTT# ..... –0.3V to 3.3V
$V_{SS(SEN)}$, BSOURCE ..... –0.3V to 0.3V
$INTV_{CC}$ RMS Output Current 50mA
Operating Junction Temperature Range (Note 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Lead Temperature (Soldering, 10sec)
eTSSOP ..... 300°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC eTSSOP
T_{JMAX} = 125°C, θ_{JA} = 29°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3816EFE#PBF	LTC3816EFE#TRPBF	LTC3816FE	38-Lead Plastic eTSSOP	–40°C to 125°C
LTC3816IFE#PBF	LTC3816IFE#TRPBF	LTC3816FE	38-Lead Plastic eTSSOP	–40°C to 125°C
LTC3816EUHF#PBF	LTC3816EUHF#TRPBF	3816	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3816IUHF#PBF	LTC3816IUHF#TRPBF	3816	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating junction temperature ranges.
*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, BSOURCE = $EXTV_{CC}$ = 0V, VR_{ON} = 5V, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Input and $INTV_{CC}$ Linear Regulator							
V_{IN}	V_{IN} Supply Voltage Range	$V_{INTVCC} > V_{UVLO}$	●	4.5		36	V
I_{VIN}	V_{IN} Supply Current Normal Mode Shutdown	 $V_{BOOST} = V_{INTVCC}$, f_{OSC} = 400kHz (Note 4) VR_{ON} = 0V			 11 27	 100	 mA µA
$INTV_{CC}$	Internal V_{CC} Voltage		●	4.9	5.2	5.5	V
$V_{INTVCC(LINE)}$	Line Regulation	7.5V < V_{IN} < 36V				±1.0	%
$V_{INTVCC(LOAD)}$	Load Regulation	Load = 0mA to 20mA			–0.25	–1.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive		4.25	4.50	4.75	V
$V_{EXTVCC(HYS)}$	$EXTV_{CC}$ Hysteresis				0.4		V
$V_{EXTVCC(DROP)}$	$EXTV_{CC}$ Voltage Drop	Load = 20mA, V_{EXTVCC} = 5V			40	100	mV
V_{UVLO}	$INTV_{CC}$ Undervoltage Reset	$INTV_{CC}$ Ramping Positive		3.7	3.9	4.1	V
	Undervoltage Hystersis				0.4		V
Switcher Control Loop							
$V_{CC(CORE)}$	$V_{CC(CORE)} = (V_{CC(SEN)} - V_{SS(SEN)})$	$V_{CC(CORE)}$ > 0.75V (Note 5) 0.5V ≤ $V_{CC(CORE)}$ ≤ 0.75V (Note 5) 0.3V ≤ $V_{CC(CORE)}$ < 0.5V (Note 5)	● ● ●			±0.75 ±6 ±10	% mV mV
$\Delta V_{CC(CORE)}$	$V_{CC(CORE)}$ Voltage Line Regulation	V_{IN} = 7.5V to 36V (Note 5)			±0.002		%/V
A_{EA}	Error Amplifier DC Gain	No load			80		dB
f_{BW}	Error Amplifier Unity-Gain Bandwidth	(Note 6)			20		MHz
I_{COMP}	Error Amplifier Output Source Current Error Amplifier Output Sink Current	V_{COMP} = 0V V_{COMP} = 5V		 5	–1.5		mA mA
$I_{VCC(SEN)}$	$V_{CC(SEN)}$ Input Current	$V_{ISENN} = V_{CC(SEN)}$, 0V ≤ $V_{CC(SEN)}$ ≤ 1.5V				±30	µA
$I_{VSS(SEN)}$	$V_{SS(SEN)}$ Input Current	$V_{SS(SEN)}$ = 0V				–60	µA
I_{VFB}	V_{FB} Input Current	0V ≤ V_{FB} ≤ 2V				±0.1	µA
I_{ITCFB}	I_{TCFB} Input Current	0V ≤ V_{ITCFB} ≤ 1.5V				±0.1	µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, BSOURCE = $EXTV_{CC}$ = 0V, VR_{ON} = 5V, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{BOOT}	Core Supply Start-Up Voltage	V_{IMON} = $INTV_{CC}$ (IMVP-6 Configuration) V_{IMON} < 1.1V (IMVP-6.5 Configuration)			1.2 1.1		V V
V_{OVF}	Overvoltage Fault Threshold	V_{IMON} = $INTV_{CC}$ (IMVP-6 Configuration) V_{IMON} < 1.1V (IMVP-6.5 Configuration)	● ●		1.65 1.53	1.7 1.55	V V
I_{SS}	SS Pull-Up Current	V_{SS} = 0V			–1		µA
I_{CSLEW}	CSLEW Pull-Up Current	V_{CSLEW} = 0V IMVP-6 and $V_{DPRSLPVR}$ = $INTV_{CC}$ IMVP-6.5 or $V_{DPRSLPVR}$ = 0V			 –10 –40		 µA µA
I_{RPTC}	RPTC Source Current	RPTC = 0V		–90	–100	–110	µA
V_{RPTC}	RPTC Thermal Shutdown Threshold				0.47		V
I_{MAX}	I_{MAX} Source Current	V_{IMAX} = 0V, 1× Current Limit Duration V_{IMAX} = 0V, 2× Current Limit Duration	●	–9	–10 –20	–11	µA µA
$t_{IMAX2×}$	2× Current Limit Duration 2× Current Limit Period			35	45 630		µs µs
V_{ILIM}	Current Comparator Offset	V_{IMAX} = 1.0V, V_{ILIM} = V_{ISENP} – V_{IMAX}				±3	mV
V_{IREV}	Reverse-Current Comparator Offset	V_{ISENN} = 1.0V, V_{IREV} = V_{ISENP} – V_{ISENN}				±2	mV
I_{ISENP}	I_{SENP} Input Current	0V ≤ V_{ISENP} ≤ 1.5V				±1	µA
I_{ISENN}	I_{SENN} Input Current	0V ≤ V_{ISENN} ≤ 1.5V				±20	µA
V_{IMON}	IMVP-6/IMVP-6.5 Selection Threshold				2.4		V
I_{VRON}	Regulator On Source Current	VR_{ON} = 0V			–1		µA
VR_{ON}	Regulator On Threshold Regulator Power-Down Threshold	Rising Edge Falling Edge		1.18	1.2 0.65	1.22	V V
Oscillator and Drivers							
f_{OSC}	Oscillator Frequency	RFREQ Floats V_{RFREQ} = 0V V_{RFREQ} = 2.5V		375 180 530	400 210 580	425 240 640	kHz kHz kHz
f_{SYNC}	Minimum Synchronization Input Frequency Maximum Synchronization Input Frequency			 550		150	kHz kHz
V_{SYNC}	MODE/SYNC Synchronization Threshold				1.6		V
I_{RFREQ}	RFREQ Source Current	V_{RFREQ} = 0V		–9	–10	–11	µA
V_{MODE}	MODE/SYNC Force Continuous Threshold	V_{IMON} = $INTV_{CC}$ (IMVP-6 Configuration) V_{IMON} < 1.1V (IMVP-6.5 Configuration)			1.6 0.5		V V
DC_{MAX}	Maximum TG Duty Cycle	MODE/SYNC = 0, RFREQ Floats			90		%
$t_{ON(MIN)}$	TG Minimum Pulse Width	(Note 6)			35		ns
t_{DEAD}	Driver Dead-Time				30		ns
TG R_{UP}	TG Driver Pull-Up On-Resistance	TG High, I_{OUT} = –100mA (Note 7)			2.6		Ω
TG R_{DOWN}	TG Driver Pull-Down On-Resistance	TG Low, I_{OUT} = 100mA (Note 7)			1.2		Ω
BG R_{UP}	BG Driver Pull-Up On-Resistance	BG High, I_{OUT} = –100mA (Note 7)			2.6		Ω
BG R_{DOWN}	BG Driver Pull-Down On-Resistance	BG Low, I_{OUT} = 100mA (Note 7)			0.9		Ω

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, BSOURCE = $EXTV_{CC}$ = 0V, VR_{ON} = 5V, unless otherwise noted. (Notes 2, 3)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
VID, DPRSLPVR, LFF Parameters							
$V_{IL(VID)}$	VID Input Low Threshold					0.3	V
$V_{IH(VID)}$	VID Input High Threshold			0.7			V
I_{VID}	VID Input Leakage Current	0V ≤ V_{VID} ≤ 5V				±1	µA
$V_{DPRSLPVR}$	DPRSLPVR Input Threshold	V_{IMON} = $INTV_{CC}$ (IMVP-6 Configuration)			1.6		V
I_{LFF}	LFF Pull-Up Current	V_{LFF} = 0V			–1		µA
V_{LFF}	LFF Input Threshold				1		V
PWRGD, CLKEN#, VRTT#							
V_{PWRGD}	Positive Power Good Threshold Negative Power Good Threshold	With Respect to VID $V_{CC(CORE)}$		150 –240	175 –270	200 –300	mV mV
I_{LEAK}	PWRGD, CLKEN# Leakage Current VRTT# Leakage Current	V_{PWRGD} = $V_{CLKEN\#}$ = 5V $V_{VRTT\#}$ = 3.3V				10 100	µA µA
V_{OL}	PWRGD, CLKEN# Output Low Voltage VRTT# Output Low Voltage	I_{OUT} = 2mA I_{OUT} = 20mA			0.1 0.075	0.3 0.18	V V
t_{PWRGD}	PWRGD Glitch Filter	Power Good to Power Bad			750		µs
$t_{CLKEN\#}$	CLKEN# Falling Edge Delay	Rising V_{BOOT} Edge to CLKEN# Falling Edge	●	50	75	100	µs
$t_{CLK(PWRGD)}$	CLKEN# to PWRGD Rising Edge Delay		●	5	10	20	ms
$t_{VR(PWRGD)}$	VR_{ON} to PWRGD Falling Edge Delay	VR_{ON} Falling Edge			100		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

Note 3: The LTC3816 is tested under pulse load conditions such that $T_J \approx T_A$. The LTC3816E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. LTC3816I specifications are guaranteed over the full –40°C to 125°C operating junction temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors. T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula,

LTC3816EFE: $T_J = T_A + (P_D \bullet 29°C/W)$

LTC3816EUHF: $T_J = T_A + (P_D \bullet 34°C/W)$

Note 4: The dynamic input supply current is a function of the power MOSFET gate charging ($Q_G \bullet f_{OSC}$). See Applications Information for more information.

Note 5: The LTC3816 is measured in a feedback loop that adjusts $V_{CC(SEN)} - V_{SS(SEN)}$ to achieve a specified COMP pin voltage. The AITC amplifier is configured as an inverter with gain = –1.

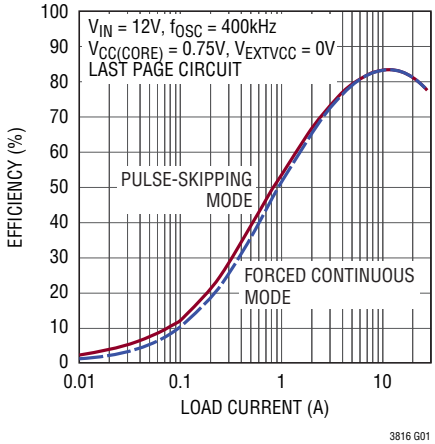
Note 6: Guaranteed by design, not subject to test.

Note 7: On-resistance limit is guaranteed by design and correlation with statistical process controls.

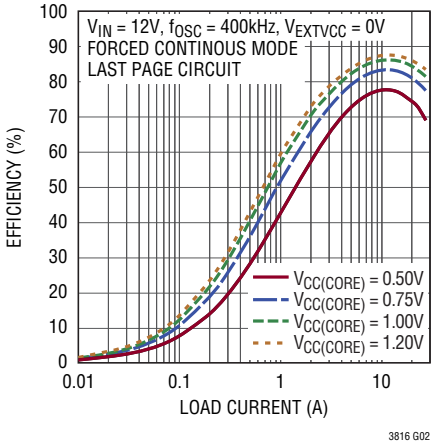
Note 8: The LTC3816 includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

TYPICAL PERFORMANCE CHARACTERISTICS

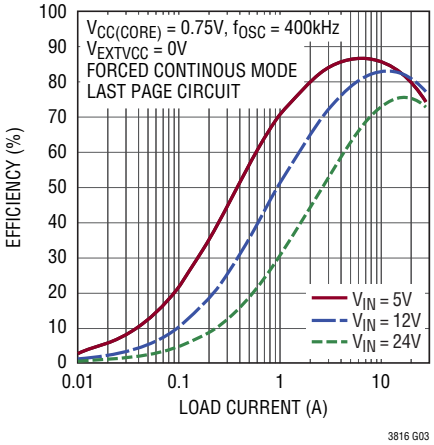
Efficiency vs Load Current



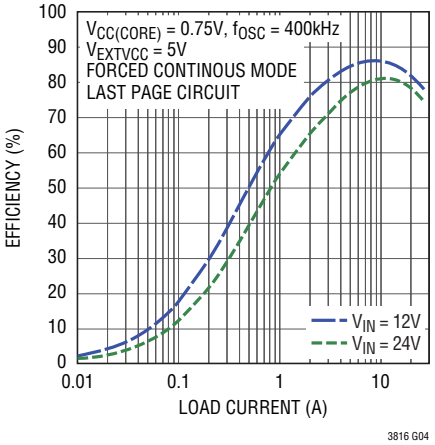
Efficiency vs $V_{CC(CORE)}$



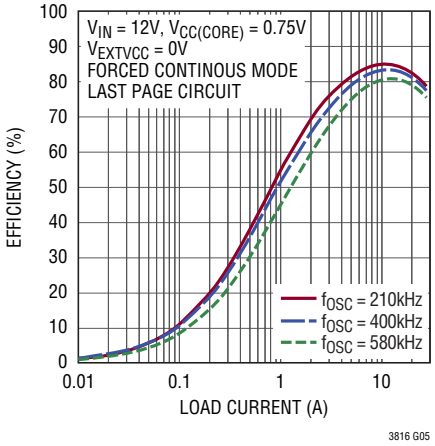
Efficiency vs V_{IN} with V_{EXTVCC} = 0V



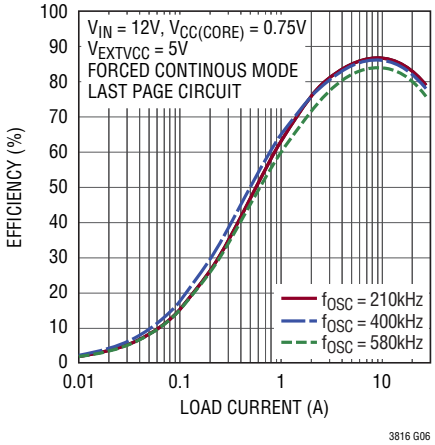
Efficiency vs V_{IN} with V_{EXTVCC} = 5V



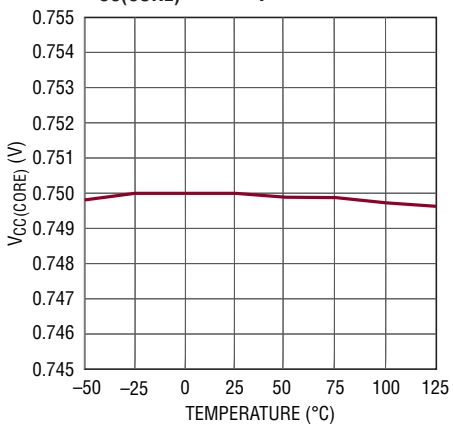
Efficiency vs f_{OSC} with V_{EXTVCC} = 0V



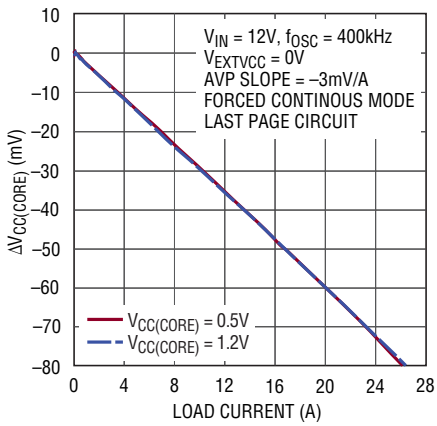
Efficiency vs f_{OSC} with V_{EXTVCC} = 5V



$V_{CC(CORE)}$ vs Temperature

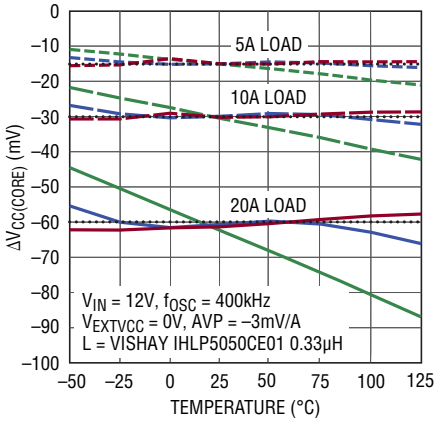


Load Regulation with AVP Slope = –3mV/A

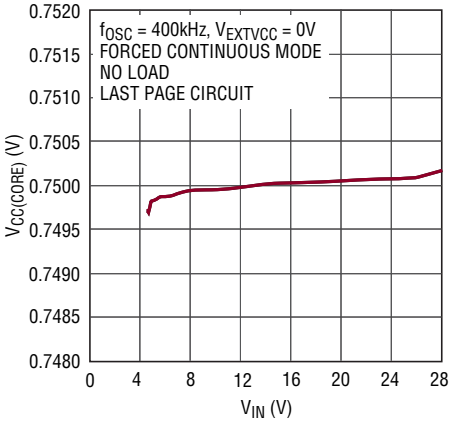


TYPICAL PERFORMANCE CHARACTERISTICS

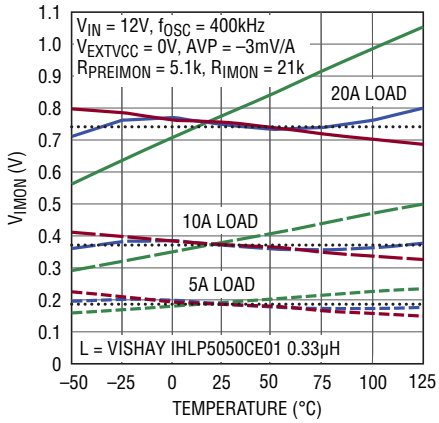
Load Regulation vs Temperature



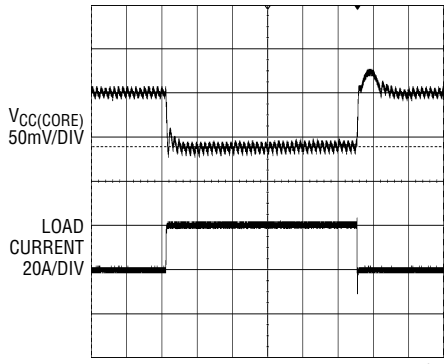
Line Regulation



V_{IMON} vs Temperature

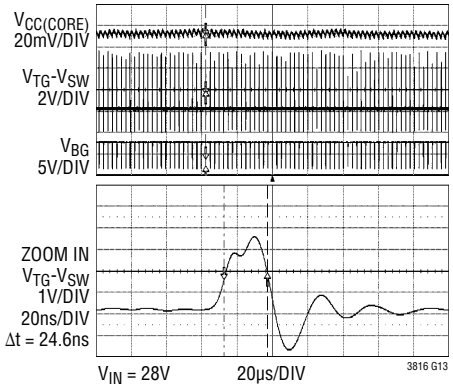


Load Step in Forced Continuous Mode



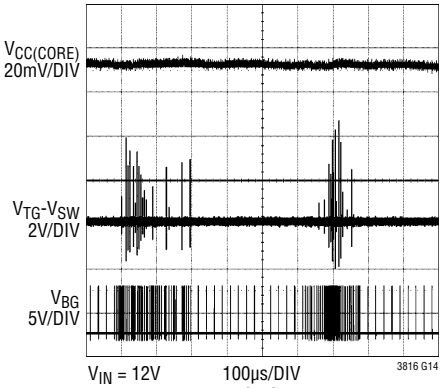
VIN = 12V 20µs/DIV
VCC(CORE) = 0.75V
fOSC = 400kHz
FORCED CONTINUOUS MODE
AVP SLOPE = –3mV/A

Narrow TG Pulse Width with Low $V_{CC(CORE)}$ Ripple



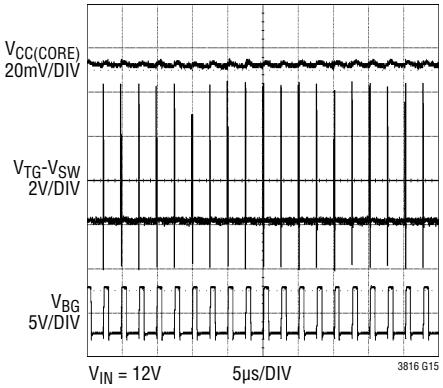
VIN = 28V 20µs/DIV
VCC(CORE) = 0.5V (ILOAD = 0.5A)
fOSC = 400kHz
FORCED CONTINUOUS MODE

Pulse-Skipping Mode at No Load with Low $V_{CC(CORE)}$ Ripple



VIN = 12V 100µs/DIV
VCC(CORE) = 0.75V, NO LOAD
fOSC = 400kHz
PULSE-SKIPPING MODE

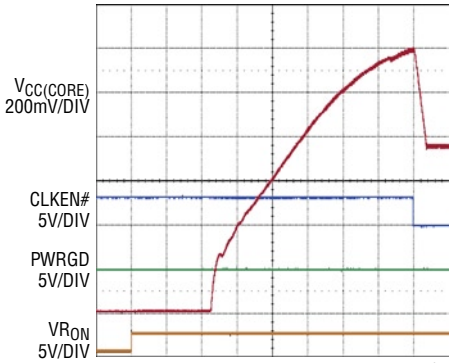
Pulse-Skipping Mode at 0.2A Load



VIN = 12V 5µs/DIV
VCC(CORE) = 0.75V (ILOAD = 0.2A)
fOSC = 400kHz
PULSE-SKIPPING MODE

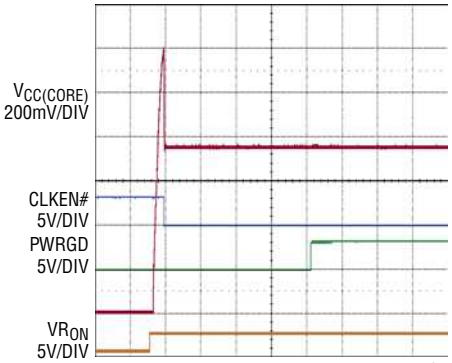
TYPICAL PERFORMANCE CHARACTERISTICS

Start-Up to V_{BOOT}



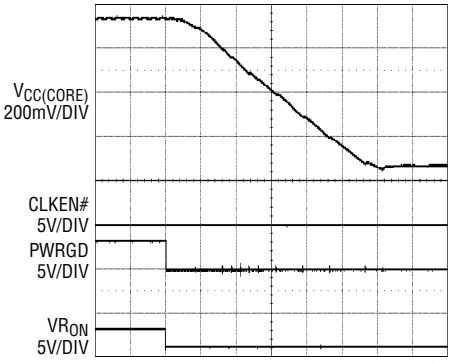
V_{IN} = 12V 100µs/DIV
IMVP6 CONFIGURATION
C_{SS} = 470pF
VID = 0.75V
NO LOAD

V_{BOOT} to PWRGD Delay



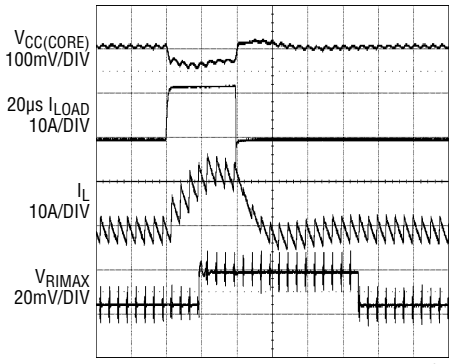
V_{IN} = 12V 2ms/DIV
IMVP6 CONFIGURATION
C_{SS} = 470pF
VID = 0.75V
NO LOAD

VR_{ON} Shutdown



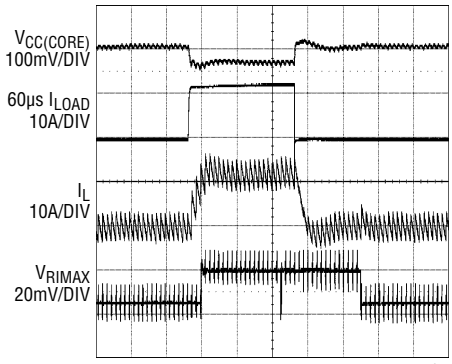
V_{IN} = 12V 10µs/DIV
VID = 0.75V
NO LOAD

Momentary Overcurrent, 45µs I_{MAX} Pulse



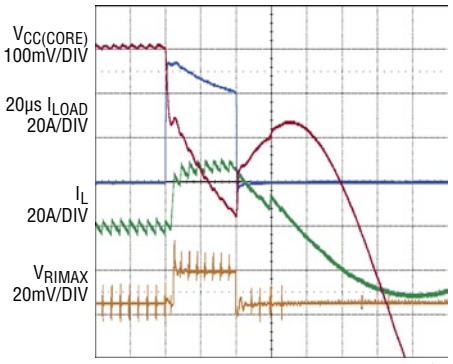
V_{IN} = 12V 10µs/DIV
$V_{CC(CORE)}$ = 1V
R_{IMAX} = 1.5k
R_{SENSE} = 1mΩ
FORCED CONTINUOUS MODE

Momentary Overcurrent, 90µs I_{MAX} Pulse



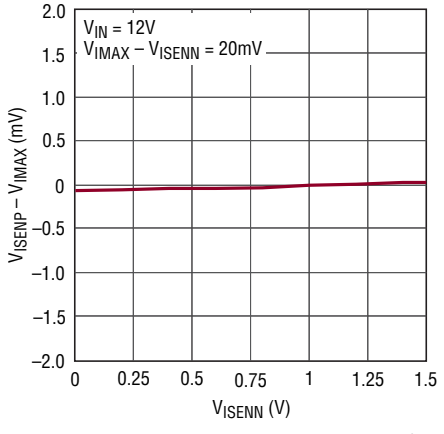
V_{IN} = 12V 20µs/DIV
$V_{CC(CORE)}$ = 1V
R_{IMAX} = 1.5k
R_{SENSE} = 1mΩ
FORCED CONTINUOUS MODE

2x Overcurrent

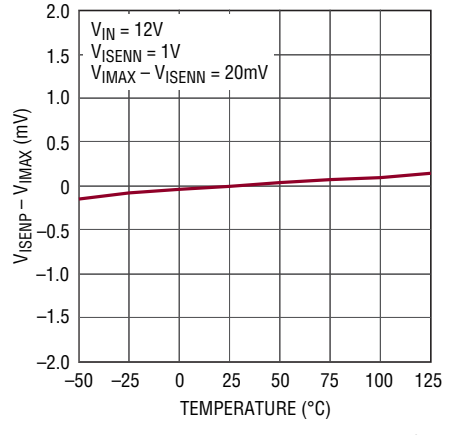


V_{IN} = 12V 10µs/DIV
$V_{CC(CORE)}$ = 1V
R_{IMAX} = 1.5k
R_{SENSE} = 1mΩ
FORCED CONTINUOUS MODE

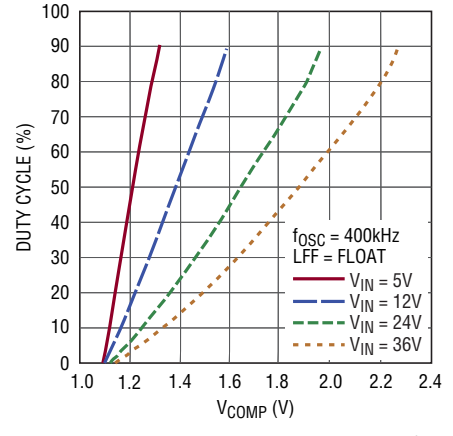
Current Comparator Offset vs Common Mode Range



Current Comparator Offset vs Temperature

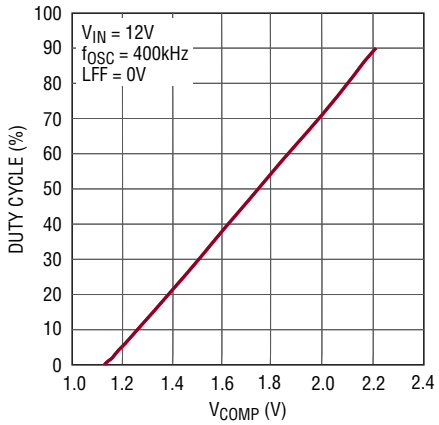


Duty Cycle vs V_{COMP} with Line Feedforward



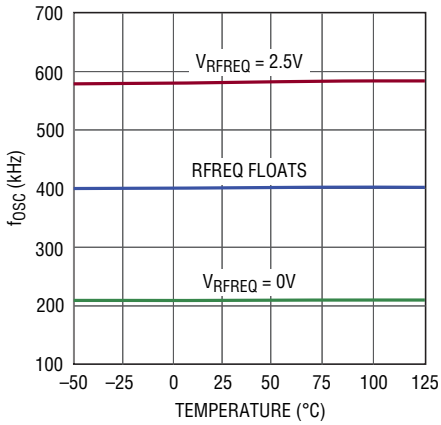
TYPICAL PERFORMANCE CHARACTERISTICS

Duty Cycle vs V_{COMP} without Line Feedforward



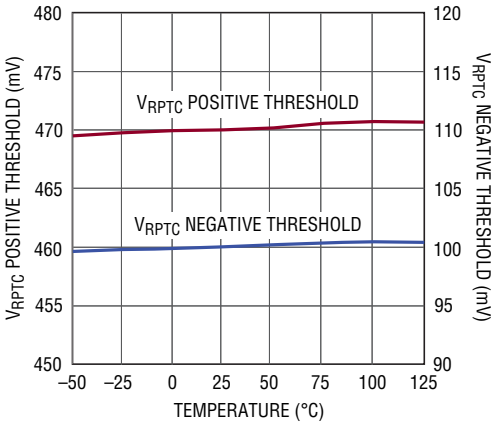
3816 G25

f_{OSC} vs Temperature



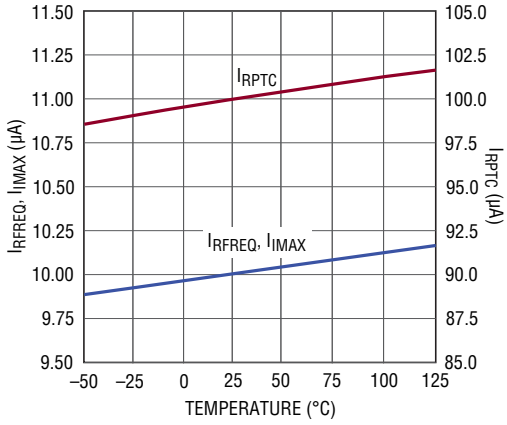
3816 G26

V_{RPTC} vs Temperature



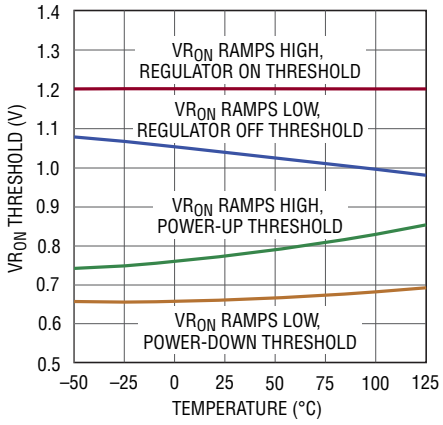
3816 G27

I_{IMAX}, I_{RFREQ} and I_{RPTC} vs Temperature



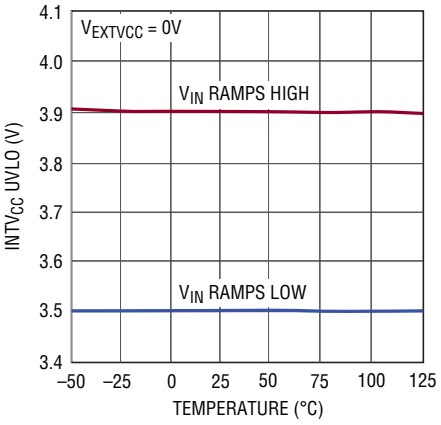
3816 G28

VR_{ON} vs Temperature



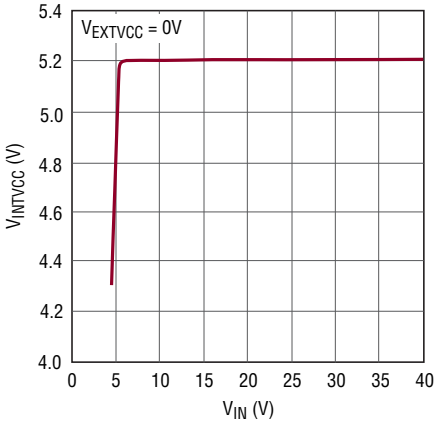
3816 G29

$INTV_{CC}$ UVLO vs Temperature



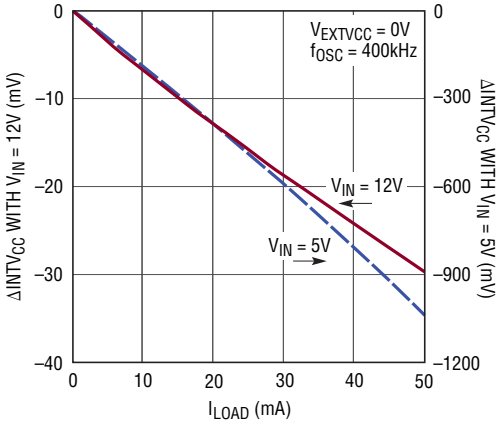
3816 G30

$INTV_{CC}$ Line Regulation



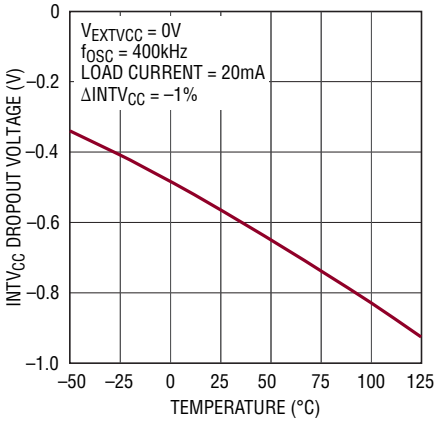
3816 G31

$INTV_{CC}$ Load Regulation



3816 G32

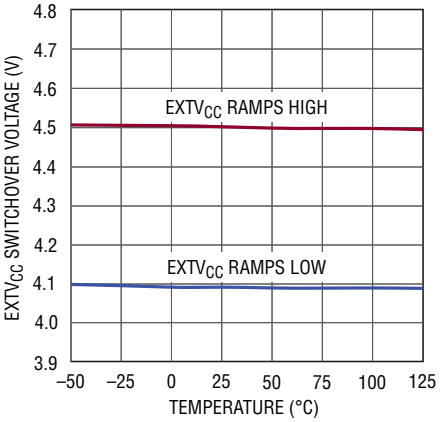
$INTV_{CC}$ Dropout vs Temperature



3816 G33

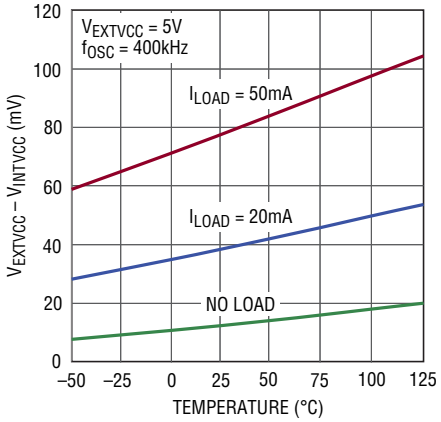
TYPICAL PERFORMANCE CHARACTERISTICS

$EXTV_{CC}$ Switchover Voltage vs Temperature



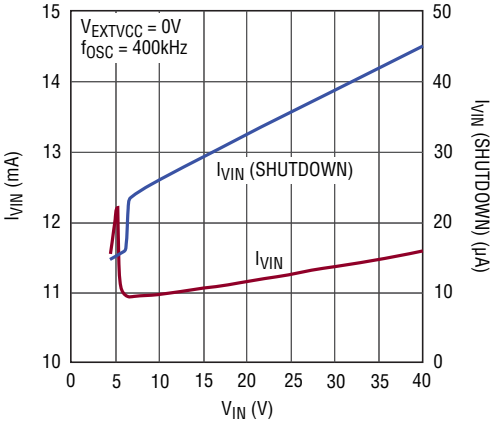
3816 G34

$EXTV_{CC}$ Voltage Drop vs Temperature



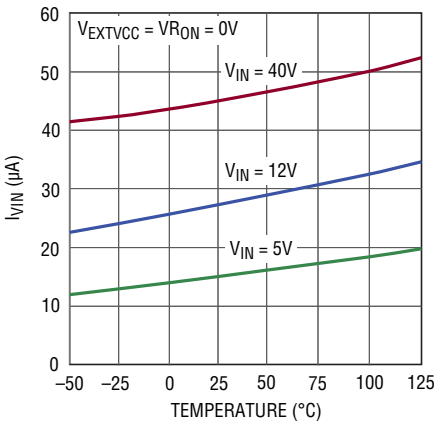
3816 G35

I_{VIN}



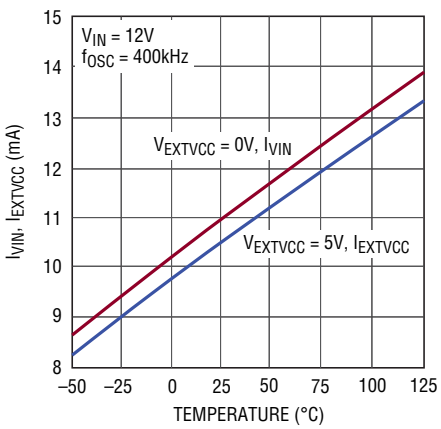
3816 G36

I_{VIN} (Shutdown) vs Temperature



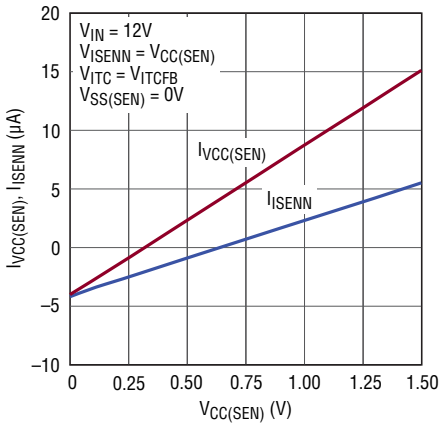
3816 G37

I_{VIN} and I_{EXTVCC} vs Temperature



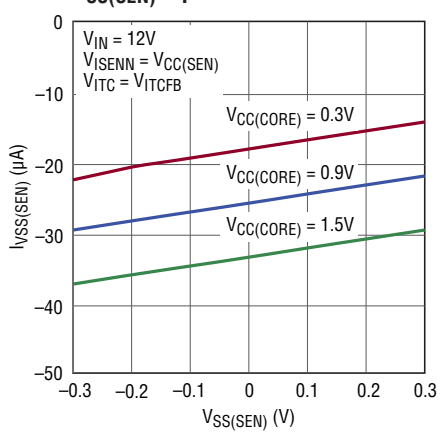
3816 G38

$V_{CC(SEN)}$ and I_{SENN} Input Current vs Common Mode Range



3816 G39

$V_{SS(SEN)}$ Input Current



3816 G40

PIN FUNCTIONS (eTSSOP/QFN)

I_{SENN} (Pin 1/Pin 36): Current Sense Negative Input. Connect this pin to the negative terminal of the current sense resistor or the negative terminal of the inductor DCR lowpass filter.

I_{TCFB} (Pin 2/Pin 37): Inductor DCR Temperature Compensation Amplifer Feedback Input. To derive the temperature compensated voltage dropped across the inductor DCR, connect a resistor from the SW node to this pin. An NTC network, in parallel with a capacitor, forms the feedback path of this amplifier. For applications that use a discrete resistor for current sensing, replace the NTC network with a resistor.

I_{TC} (Pin 3/Pin 38): Inductor DCR Temperature Compensation Amplifer Output. The I_{MON} circuitry and the error amplifier obtain the temperature compensated DCR voltage through this amplifier.

$PREI_{MON}$ (Pin 4/Pin 1): I_{MON} Current Output Setting. $PREI_{MON}$ is servoed to the I_{SENN} potential. A resistor from PRE_{IMON} to I_{TC} sets the I_{MON} output current. For the IMVP-6 configuration, connect this pin to $INTV_{CC}$.

I_{MON} (Pin 5/Pin 2): IMVP-6/IMVP-6.5 Configuration Selection and Output Current Monitor. Connect this pin to $INTV_{CC}$ to select the IMVP-6 configuration. At start-up, the switcher V_{OUT} is ramped to 1.2V (V_{BOOT}). In deeper sleep mode, the controller enables the slow V_{OUT} slew rate. Connect a resistor to $V_{SS(SEN)}$ to select the IMVP-6.5 configuration. In this case, V_{BOOT} equals 1.1V, slow slew rate is disabled and the I_{MON} current source is proportional to the load. In the IMVP-6.5 configuration, this pin is internally clamped to 1.1V with respect to the $V_{SS(SEN)}$ pin.

RPTC (Pin 6/Pin 3): Nonlinear PTC Thermistor Input. Connect to a nonlinear PTC thermistor for MOSFET or inductor temperature sensing. This pin is pulled up by a 100µA current source. If the potential at RPTC is higher than 0.47V, thermal flag VRTT# is pulled low. RPTC is sensitive to noise pickup. Avoid coupling high frequency switching signals to this pin. If required, bypass this pin with a capacitor to GND.

VR_{ON} (Pin 7/Pin 4): Voltage Regulator Enable Input. The VR_{ON} pin power-up threshold is 1.2V. When forced below 0.65V, a power-down sequence is initiated where the $V_{CC(CORE)}$ output is ramped down near 0V before the IC is put into a low current shutdown mode. The VR_{ON} pin has an internal 1µA pull-up current.

$V_{SS(SEN)}$ (Pin 8/Pin 5): Processor $V_{CC(CORE)}$ Negative Terminal Voltage Sense. Negative input of the differential sense amplifier. Connect to the processor $V_{SS(SEN)}$ pin.

$V_{CC(SEN)}$ (Pin 9/Pin 6): Processor $V_{CC(CORE)}$ Positive Terminal Voltage Sense. Positive input of the differential sense amplifier. Connect to the processor $V_{CC(SEN)}$ pin.

SERVO (Pin 10/Pin 7): Error Amplifier AC Input. The controller servos the switcher output voltage to the VID DAC voltage through the error amplifier.

V_{FB} (Pin 11/Pin 8): Error Amplifier Negative Input Pin. V_{FB} is servoed to 1.3V.

COMP (Pin 12/Pin 9): Error Amplifier Output. The COMP pin is connected directly to the error amplifier output and the input of the line feedforward circuit. Use an RC network between the COMP pin and the V_{FB} pin to compensate the feedback loop for stability and optimum transient response.

SS (Pin 13/Pin 10): Soft-Start Input. The SS pin has an internal 1µA current source pull-up. A capacitor connected to this pin controls the output voltage start-up. SS is forced low if VR_{ON} or PWRGD is low, or if an overvoltage or overcurrent fault occurs. If the potential at SS is less than 0.3V, the I_{MAX} sourcing current is reduced to 2.5µA and the current limit threshold is reduced to 25% of its nominal value.

DPRSLPVR (Pin 14/Pin 11): Deeper Sleep Mode. For the IMVP-6 configuration, 25µs after DPRSLPVR is asserted high, the controller enables the V_{OUT} slow slew rate transition. To disable slow slew rate mode, force DPRSLPVR low. Upon power-up, the DPRSLPVR input is ignored until PWRGD is asserted.

PIN FUNCTIONS (eTSSOP/QFN)

CSLEW (Pin 15/Pin 12): VID DAC Slew Rate Control. CSLEW is internally pulled up by a current source. Add a capacitor to program the VID DAC transition slew rate. If slow slew rate is selected, a 100pF capacitor connected to CSLEW results in a VID DAC slew rate of 1.25mV/µs. When slow slew rate is disabled, a 100pF capacitor results in a VID DAC slew rate of 5mV/µs. Avoid coupling high frequency switching signals to this pin. For the IMVP-6.5 configuration, the slow slew rate function is disabled.

VID0-VID6 (Pins 16-22/Pins 13-19): VID DAC Voltage Control Logic Inputs. See Table 1.

RFREQ (Pin 23/Pin 20): Frequency Setting. The voltage on the RFREQ pin determines the free-running operating frequency. The RFREQ pin has an internal 10µA current source pull-up allowing the switching frequency to be programmed by a single external resistor to GND. Alternatively, this pin can be driven with a DC voltage source to control the frequency of the internal oscillator. Floating this pin or shorting this pin to $INTV_{CC}$ allows the controller to run at a fixed 400kHz frequency.

MODE/SYNC (Pin 24/Pin 21): Mode Select/Synchronization Input. This pin is pulled up by an internal 1µA current source. Floating this pin or shorting it to $INTV_{CC}$ enables pulse-skipping mode. Shorting this pin to ground configures forced continuous mode. During frequency synchronization, the phase-locked loop forces the controller to operate in continuous mode with the falling top gate signal synchronized to the falling edge of the MODE/SYNC input pulse. During start-up, the controller is forced to run in pulse-skipping mode.

BSOURCE (Pin 25/Pin 22): Bottom MOSFET Source. Connect this pin to the source of the bottom power MOSFET. Do not short BSOURCE to the LTC3816 exposed pad directly.

BG (Pin 26/Pin 23): Bottom Gate Drive. The BG pin drives the gate of the bottom N-channel synchronous switch MOSFET.

$INTV_{CC}$ (Pin 27/Pin 24): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. The $INTV_{CC}$ pin must be decoupled to GND with a minimum 4.7µF low ESR ceramic capacitor (X5R or better).

$EXTV_{CC}$ (Pin 28/Pin 25): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.5V. Do not exceed 6V on this pin.

V_{IN} (Pin 29/Pin 26): Main Supply Pin. A bypass capacitor should be connected from this pin to the GND pin.

BOOST (Pin 30/Pin 27): Top Gate Driver Supply. The BOOST pin should be decoupled to the SW node with a 0.1µF low ESR (X5R or better) ceramic capacitor. An external Schottky diode from $INTV_{CC}$ to BOOST creates a complete floating charge-pumped supply from BOOST to SW.

TG (Pin 31/Pin 28): Top Gate Drive. The TG pin drives the top N-channel MOSFET with a voltage swing equal to $INTV_{CC}$ superimposed on the switch node voltage.

PIN FUNCTIONS (eTSSOP/QFN)

SW (Pin 32/Pin 29): Switching Node. Connect SW to the source of the upper power MOSFET and to the negative terminal of the BOOST pin decoupling capacitor.

PWRGD (Pin 33/Pin 30): Open-Drain Power Good Output/Power Bad Latchoff Input. PWRGD is an open-drain output pin and can be connected to other open-drain outputs to implement wire-ORing. PWRGD is externally pulled high 10ms after the output regulates. After start-up, if a fault condition causes PWRGD to go low, or PWRGD is externally pulled low, the regulator output voltage is actively ramped to 0V and PWRGD remains latched low until either the power is cycled or VR_{ON} toggles. PWRGD has a 750µs de-glitch delay and is masked for 100µs after the VID code changes. In deeper sleep mode, the PWRGD comparators are disabled and not allowed to de-assert the PWRGD pin.

CLKEN# (Pin 34/Pin 31): Open-Drain Clock Enable Indicator. 75µs after $V_{CC(CORE)}$ reaches the V_{BOOT} voltage, CLKEN# pulls low to enable the processor phase-locked loop.

VRTT# (Pin 35/Pin 32): Open-Drain Output for Voltage Regulator Thermal Throttling. The VRTT# pin pulls low if the RPTC voltage exceeds 0.47V or if the control IC junction temperature exceeds 150°C.

LFF (Pin 36/Pin 33): Line Feedforward. This pin has a 1µA pull-up current source to $INTV_{CC}$. Floating this pin or connecting it to $INTV_{CC}$ enables the line feedforward compensation. Connect this pin to GND to disable the line feedforward compensation.

I_{SENP} (Pin 37/Pin 34): Current Sense Positive Input. Connect this pin to the positive terminal of the current sense resistor or to the output of the inductor DCR lowpass filter.

I_{MAX} (Pin 38/Pin 35): Current Comparator Threshold Setting. The I_{MAX} pin has an internal 10µA pull-up current source, allowing the current limit comparator threshold to be programmed by a single external resistor. The controller allows a momentary 45µs overcurrent event to occur within a period of 630µs. See Current Sense and Current Limit in Applications Information.

GND (Exposed Pad Pin 39/Exposed Pad Pin 39): Ground. The soft-start and slew rate control capacitors as well as the frequency setting and thermal shutdown resistors should return to this exposed pad ground pin. This GND pin should also be connected to the negative terminals of the local voltage regulator output capacitors through vias to the PCB ground plane.

FUNCTIONAL DIAGRAM

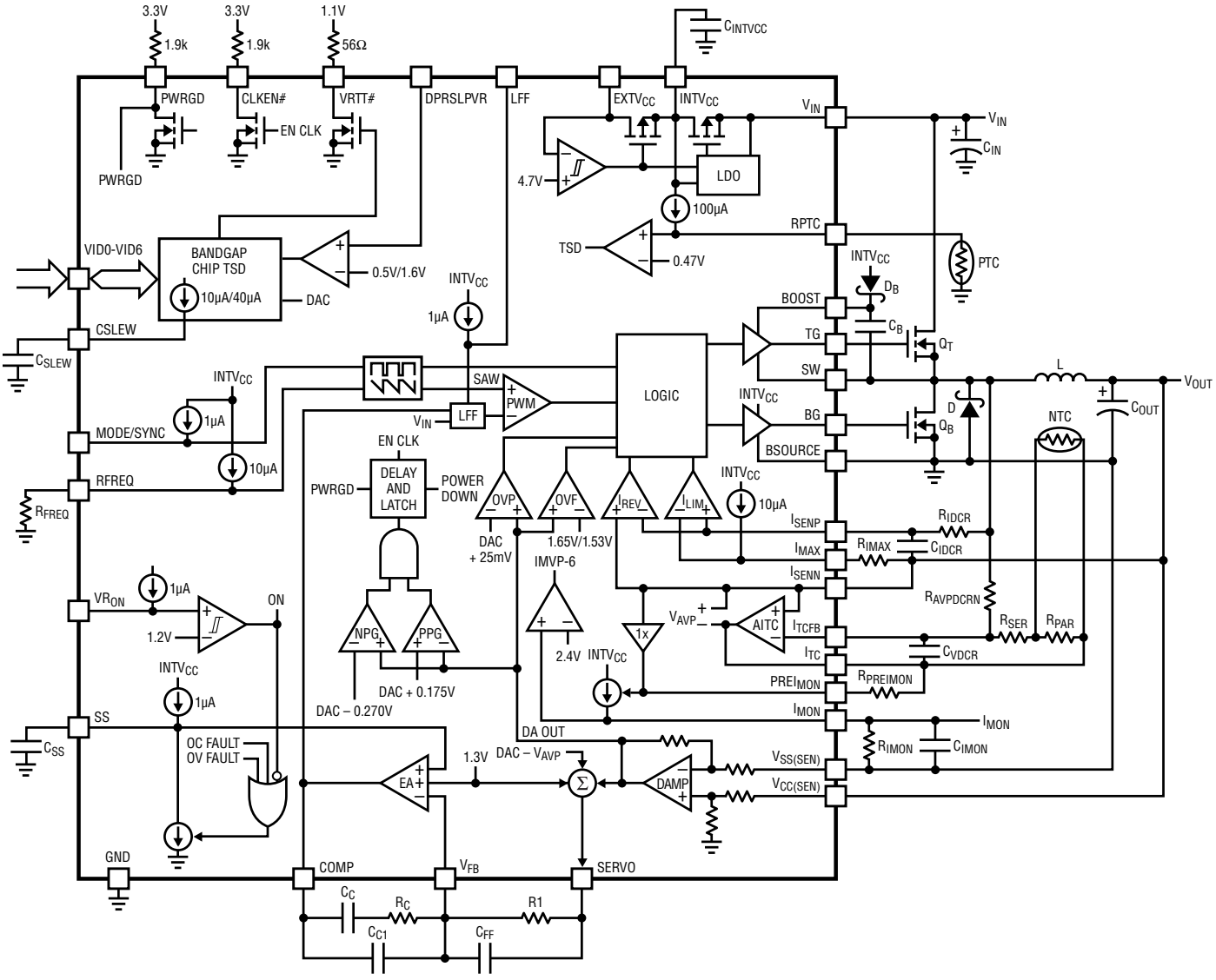


Figure 1. Functional Diagram

OPERATION (Refer to Funtional Diagram)

Table 1. IMVP-6/IMVP-6.5 VID Output Voltage Programming

VID6	VID5	VID4	VID3	VID2	VID1	VID0	$V_{CC(CORE)}$
0	0	0	0	0	0	0	1.5000
0	0	0	0	0	0	1	1.4875
0	0	0	0	0	1	0	1.4750
0	0	0	0	0	1	1	1.4625
0	0	0	0	1	0	0	1.4500
0	0	0	0	1	0	1	1.4375
0	0	0	0	1	1	0	1.4250
0	0	0	0	1	1	1	1.4125
0	0	0	1	0	0	0	1.4000
0	0	0	1	0	0	1	1.3875
0	0	0	1	0	1	0	1.3750
0	0	0	1	0	1	1	1.3625
0	0	0	1	1	0	0	1.3500
0	0	0	1	1	0	1	1.3375
0	0	0	1	1	1	0	1.3250
0	0	0	1	1	1	1	1.3125
0	0	1	0	0	0	0	1.3000
0	0	1	0	0	0	1	1.2875
0	0	1	0	0	1	0	1.2750
0	0	1	0	0	1	1	1.2625
0	0	1	0	1	0	0	1.2500
0	0	1	0	1	0	1	1.2375
0	0	1	0	1	1	0	1.2250
0	0	1	0	1	1	1	1.2125
0	0	1	1	0	0	0	1.2000
0	0	1	1	0	0	1	1.1875
0	0	1	1	0	1	0	1.1750
0	0	1	1	0	1	1	1.1625
0	0	1	1	1	0	0	1.1500
0	0	1	1	1	0	1	1.1375
0	0	1	1	1	1	0	1.1250
0	0	1	1	1	1	1	1.1125
0	1	0	0	0	0	0	1.1000
0	1	0	0	0	0	1	1.0875
0	1	0	0	0	1	0	1.0750
0	1	0	0	0	1	1	1.0625
0	1	0	0	1	0	0	1.0500
0	1	0	0	1	0	1	1.0375
0	1	0	0	1	1	0	1.0250
0	1	0	0	1	1	1	1.0125
0	1	0	1	0	0	0	1.0000
0	1	0	1	0	0	1	0.9875
0	1	0	1	0	1	0	0.9750
0	1	0	1	0	1	1	0.9625
0	1	0	1	1	0	0	0.9500
0	1	0	1	1	0	1	0.9375
0	1	0	1	1	1	0	0.9250
0	1	0	1	1	1	1	0.9125
0	1	1	0	0	0	0	0.9000
0	1	1	0	0	0	1	0.8875
0	1	1	0	0	1	0	0.8750
0	1	1	0	0	1	1	0.8625
0	1	1	0	1	0	0	0.8500
0	1	1	0	1	0	1	0.8375
0	1	1	0	1	1	0	0.8250
0	1	1	0	1	1	1	0.8125
0	1	1	1	0	0	0	0.8000
0	1	1	1	0	0	1	0.7875
0	1	1	1	0	1	0	0.7750
0	1	1	1	0	1	1	0.7625
0	1	1	1	1	0	0	0.7500
0	1	1	1	1	0	1	0.7375
0	1	1	1	1	1	0	0.7250
0	1	1	1	1	1	1	0.7125

VID6	VID5	VID4	VID3	VID2	VID1	VID0	$V_{CC(CORE)}$
1	0	0	0	0	0	0	0.7000
1	0	0	0	0	0	1	0.6875
1	0	0	0	0	1	0	0.6750
1	0	0	0	0	1	1	0.6625
1	0	0	0	1	0	0	0.6500
1	0	0	0	1	0	1	0.6375
1	0	0	0	1	1	0	0.6250
1	0	0	0	1	1	1	0.6125
1	0	0	1	0	0	0	0.6000
1	0	0	1	0	0	1	0.5875
1	0	0	1	0	1	0	0.5750
1	0	0	1	0	1	1	0.5625
1	0	0	1	1	0	0	0.5500
1	0	0	1	1	0	1	0.5375
1	0	0	1	1	1	0	0.5250
1	0	0	1	1	1	1	0.5125
1	0	1	0	0	0	0	0.5000
1	0	1	0	0	0	1	0.4875
1	0	1	0	0	1	0	0.4750
1	0	1	0	0	1	1	0.4625
1	0	1	0	1	0	0	0.4500
1	0	1	0	1	0	1	0.4375
1	0	1	0	1	1	0	0.4250
1	0	1	0	1	1	1	0.4125
1	0	1	1	0	0	0	0.4000
1	0	1	1	0	0	1	0.3875
1	0	1	1	0	1	0	0.3750
1	0	1	1	0	1	1	0.3625
1	0	1	1	1	0	0	0.3500
1	0	1	1	1	0	1	0.3375
1	0	1	1	1	1	0	0.3250
1	0	1	1	1	1	1	0.3125
1	1	0	0	0	0	0	0.3000
1	1	0	0	0	0	1	0.2875
1	1	0	0	0	1	0	0.2750
1	1	0	0	0	1	1	0.2625
1	1	0	0	1	0	0	0.2500
1	1	0	0	1	0	1	0.2375
1	1	0	0	1	1	0	0.2250
1	1	0	0	1	1	1	0.2125
1	1	0	1	0	0	0	0.2000
1	1	0	1	0	0	1	0.1875
1	1	0	1	0	1	0	0.1750
1	1	0	1	0	1	1	0.1625
1	1	0	1	1	0	0	0.1500
1	1	0	1	1	0	1	0.1375
1	1	0	1	1	1	0	0.1250
1	1	0	1	1	1	1	0.1125
1	1	1	0	0	0	0	0.1000
1	1	1	0	0	0	1	0.0875
1	1	1	0	0	1	0	0.0750
1	1	1	0	0	1	1	0.0625
1	1	1	0	1	0	0	0.0500
1	1	1	0	1	0	1	0.0375
1	1	1	0	1	1	0	0.0250
1	1	1	0	1	1	1	0.0125
1	1	1	1	0	0	0	0.0000
1	1	1	1	0	0	1	0.0000
1	1	1	1	0	1	0	0.0000
1	1	1	1	0	1	1	0.0000
1	1	1	1	1	0	0	0.0000
1	1	1	1	1	0	1	0.0000
1	1	1	1	1	1	0	0.0000
1	1	1	1	1	1	1	0.0000

OPERATION (Refer to Funtional Diagram)

The LTC3816 is a constant frequency, voltage mode DC/DC step-down controller that complies with the Intel IMVP-6/IMVP-6.5 specifications. The 7-bit VID code programs the switcher output voltage as specified in Table 1. Figure 2 shows the timing diagram. Upon start-up, the switcher output soft-start ramps to the V_{BOOT} voltage. 75µs after reaching the V_{BOOT} power good threshold, which is about 45mV below V_{BOOT}, the controller forces the CLKEN# pin low and the VID code is loaded. Next, the output is servoed to its VID DAC potential. 10ms after regulation, PWRGD pulls high to indicate that the switcher is regulating and has completed its start-up phase.

The LTC3816 uses two external synchronous N-channel MOSFETs. A floating topside driver and a simple external charge pump provide full gate drive to the upper MOSFET. The controller uses a leading edge modulation architecture to allow extremely low duty cycles and fast load step response. In a typical LTC3816 switching cycle, the PWM comparator turns on the top MOSFET to charge the output capacitor. An internal clock resets the top MOSFET and turns on the bottom MOSFET to reduce the output charging current. This switching cycle repeats itself at an internally fixed frequency, or in synchronization with an external oscillator.

The top gate duty cycle is controlled by the voltage feedback loop which includes an internal differential amplifier that senses the differential output voltage between the $V_{CC(SEN)}$ and $V_{SS(SEN)}$ pins. The AITC amplifier monitors the inductor current and computes the load dependent output droop required to implement the active voltage positioning features in IMVP-6/IMVP-6.5. The IC servos the differential output voltage to the VID DAC voltage minus the small load dependent AVP droop.

The LTC3816 feedback loop is capable of dynamically changing the regulator output to different VID DAC voltages. Upon receiving a new VID code, the LTC3816 regulates to its new potential with a programmable slew rate which is selected to prevent the converter from generating audible noise. The switcher output load current can be monitored by measuring the I_{MON} pin potential. The LTC3816 forces the I_{MON} pin voltage to be proportional to the average load current with a gain configured by the $R_{PREIMON}$ and R_{IMON} resistors.

The LTC3816 includes an onboard current limit circuit that senses the inductor current through an external sense resistor or the inductor DCR. The peak inductor current can be controlled by selecting the current limit R_{IMAX} resistance. The LTC3816 current limit architecture allows momentary overcurrent events for a predefined duration (see the Current Sense and Current Limit sections). Upon current limit, the top gate is shut off, the SS external capacitor is discharged to limit the top gate duty cycle, and the switcher output voltage is reduced until the load fault is removed.

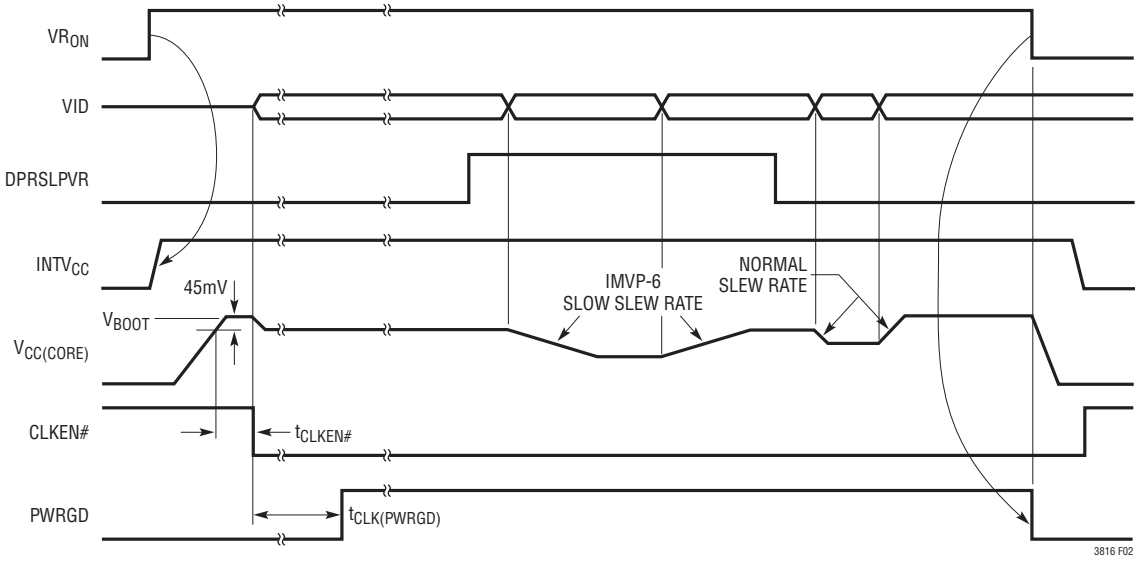


Figure 2. LTC3816 Power-Up and Power-Down Timing Diagram

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LDO, $INTV_{CC}/EXTV_{CC}$ POWER SUPPLY

The LTC3816 is designed to operate with a wide range of V_{IN} input voltages. The IC includes a 5.2V LDO to power the driver and control circuits. The LDO output, $INTV_{CC}$ should be bypassed with a minimum 4.7µF low ESR ceramic capacitor. The $INTV_{CC}$ regulator can supply up to 50mA of total LTC3816 quiescent current, $I_{Q(TOT)}$, which consists of the static supply current, I_Q, and the current required to charge the gate capacitance, $Q_{G(TOT)}$, of the top and bottom power MOSFETs.

$$I_{Q(TOT)} = I_Q + Q_{G(TOT)} \bullet f_{OSC}$$

$$P_{DISS} = V_{IN} \bullet (I_Q + Q_{G(TOT)} \bullet f_{OSC})$$

$$T_J = T_A + P_{DISS} \bullet \theta_{JA}$$

The value of $Q_{G(TOT)}$ can be obtained from the MOSFET data sheets. For high V_{IN} and high frequency operation, care must be taken to ensure that the maximum junction temperature T_{JMAX} of the IC is never exceeded.

When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.5V, the 5.2V LDO powers $INTV_{CC}$. If $EXTV_{CC}$ is taken above 4.5V, the LDO is turned off and an internal switch connects $INTV_{CC}$ to $EXTV_{CC}$. Do not apply greater than 6V to the $EXTV_{CC}$ pin, and ensure that $EXTV_{CC} < V_{IN} + 0.3V$ unless $EXTV_{CC}$ is shorted to the V_{IN} supply. Using the $EXTV_{CC}$ pin allows $INTV_{CC}$ to be powered from an external source reducing LDO losses and improving the regulator efficiency, especially at high V_{IN}. When the $EXTV_{CC}$ pin is used, the chip power dissipation reduces to:

$$P_{DISS} = V_{EXTVCC} \bullet (I_Q + Q_{G(TOT)} \bullet f_{OSC})$$

If the V_{IN} supply is low enough for the $INTV_{CC}$ LDO to enter dropout, the output voltage of the LDO becomes:

$$V_{INTVCC(DROPOUT)} = V_{IN} - V_{DROPOUT}$$

The LDO dropout voltage is a function of the total quiescent current $I_{Q(TOT)}$, V_{IN} voltage and junction temperature. The temperature coefficient of the LDO dropout voltage is approximately 6400ppm/°C. To enable proper operation, make sure that the LDO output voltage meets the $INTV_{CC}$ undervoltage and minimum MOSFET gate driver requirements. If V_{IN} is connected to a fixed 5V supply, it is advisable to short $EXTV_{CC}$ to V_{IN}. In this case, the $INTV_{CC}$ output voltage becomes:

$$V_{INTVCC(EXTVCC)} = V_{EXTVCC} - I_{Q(TOT)} \bullet R_{EXTVCC}$$

where R_{EXTVCC} is the internal $EXTV_{CC}$ switch on-resistance. It has a typical value of 2Ω at 25°C and has a temperature coefficient of approximately 4000ppm/°C.

UNDERVOLTAGE LOCKOUT AND SHUTDOWN

A precision undervoltage lockout (UVLO) comparator monitors the $INTV_{CC}$ voltage and enables soft-start operation once $INTV_{CC}$ is above 3.9V. For power supplies that start-up slowly, the gate drivers could begin switching when V_{IN} is well below its steady-state value. The high inrush current through the input power cable could cause the V_{IN} supply to dip below the UVLO threshold and result in hiccup operation at start-up. This problem can be easily overcome by adding a V_{IN} UVLO function as shown in Figure 3. Connect an external resistive divider from V_{IN} to VR_{ON}. Set the resistive divider according to the following equation:

$$V_{UVLO} = 1.2V = V_{IN(UVLO)} \frac{R_{ON1}}{R_{ON1} + R_{ON2}}$$

where $V_{IN(UVLO)}$ is the desired V_{IN} UVLO threshold. The resistances are normally chosen so that the error caused by the internal 1µA pull-up current has a negligible effect on the UVLO threshold. Be careful not to allow the resistive divider output voltage to exceed the 6V maximum rating of the VR_{ON} pin.

If the external resistive divider is not used, upon power-up, the VR_{ON} pin is pulled up by an internal 1µA pull-up current. The LTC3816 can be put into a low power shut-

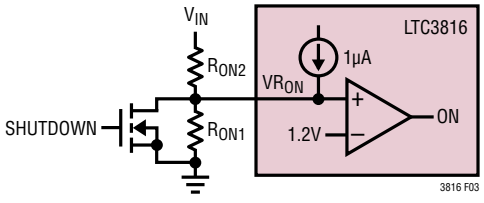

Figure 3. V_{IN} UVLO Circuit

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down mode by pulling the VR_{ON} pin below 0.65V. In the shutdown mode, the internal circuitry and the $INTV_{CC}$ regulator are off and the supply current drops well below 100µA. When the VR_{ON} pin voltage is between 0.65V and 1.2V, the $INTV_{CC}$ regulator and internal circuitry power up but the driver outputs remain low.

TOPSIDE MOSFET DRIVER SUPPLY

An external bootstrap capacitor, C_B, connected from the BOOST pin to the SW pin supplies the topside gate driver as shown in Figure 1. Capacitor C_B is charged though the external diode, D_B, from $INTV_{CC}$ when the SW pin is low. When the topside MOSFET is turned on, the top driver places the C_B voltage across the gate source of the top MOSFET. This enhances the MOSFET and turns on the top switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply:

$$V_{BOOST} = V_{IN} + V_{INTVCC}$$

The value of the boost capacitor, C_B, needs to be at least 100 times that of the total input capacitance of the topside MOSFET. The reverse breakdown of the external Schottky diode, D_B, must be greater than $V_{IN(MAX)}$.

IMVP-6/IMVP-6.5 SELECTION AND V_{BOOT} VOLTAGE

The LTC3816 can be configured to meet either IMVP-6 or IMVP-6.5 requirements. To select IMVP-6 operation, short both I_{MON} and $PREI_{MON}$ to $INTV_{CC}$. At start-up, when VR_{ON} is asserted, the switcher output ramps to V_{BOOT} = 1.2V regardless of the VID code. To configure IMVP-6.5 operation, connect a resistor from I_{MON} to $V_{SS(SEN)}$ and another resistor from $PREI_{MON}$ to I_{TC}. The I_{MON} and $PREI_{MON}$ resistance set the I_{MON} gain (see the I_{MON} section). The V_{BOOT} voltage for IMVP-6.5 is 1.1V.

SOFT-START OPERATION

The start-up of V_{OUT} is controlled by the LTC3816's SS pin. When the voltage at the SS pin is less than 1.3V, the LTC3816 regulates the V_{FB} voltage to the SS pin voltage instead of 1.3V. This allows the user to program the soft-start of the regulator output with a capacitor from the SS pin to GND. An internal 1µA current source charges this capacitor, creating a voltage ramp on the SS pin. As the SS pin voltage rises from 0V to 1.3V, the output voltage, V_{OUT}, rises smoothly from 0V to its V_{BOOT} value. Once the soft-start interval is over, the internal current source continues charging the SS capacitor until the SS potential is internally clamped at about 2.7V. For the IMVP-6 configuration, a 1000pF SS capacitor generates roughly a 1.6ms start-up time. With the IMVP-6.5 configuration, the start-up time is about 1.5ms.

During severe overload conditions, the LTC3816 discharges the SS capacitor to lower the switcher output voltage. If the potential at SS is forced below 0.3V, the controller reduces its I_{MAX} sourcing current from 10µA to 2.5µA and cuts the short-circuit current to about 25% of its nominal value.

CURRENT SENSE AND CURRENT LIMIT

The LTC3816 features an onboard cycle-by-cycle user-programmable current limit circuit that controls the peak inductor current. The I_{MAX} pin has an internal 10µA pull-up current source, allowing the maximum load current $I_{LOAD(MAX)}$ to be programmed by a single external resistor R_{IMAX} connected between the I_{MAX} and I_{SENN} pins.

$$I_{L(PEAK)} = \frac{I_{IMAX} \bullet R_{IMAX}}{R_{SENSE}}$$

$$I_{LOAD(MAX)} < I_{LIMIT} = I_{L(PEAK)} - \frac{\Delta I_L}{2} = \frac{I_{IMAX} \bullet R_{IMAX}}{R_{SENSE}} - \frac{\Delta I_L}{2}$$

where $I_{L(PEAK)}$ is the peak inductor current, I_{IMAX} is the I_{MAX} pin pull-up current, R_{SENSE} is the current sense resistor value and ΔI_L is the inductor ripple current.

$$\Delta I_L = \frac{1}{f_{OSC} \bullet L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Note that the output ripple current varies with the switching frequency, inductor value and duty cycle. Hence, the current limit value should be checked on the application board to ensure that $I_{LOAD(MAX)} < I_{LIMIT}$ under all operating conditions and temperature variations.

For current sensing using a low value sense resistor, the sense resistor parasitic inductance must be considered to

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achieve accurate current sensing. Figure 4 shows a real current sensing resistor, R_{SENSE}, which can be modeled with an ideal resistance, R_{SEN}, in series with its parasitic ESL. As shown in Figure 4, the voltage across the sense resistor includes the voltage across the parasitic inductor which is a strong function of inductor ripple current and the switching frequency. This effectively reduces the current limit threshold, typically by more than 30%. The voltage across the sense resistor can be extracted from a lowpass filter placed close to the controller input sense pins as shown in Figure 4. The voltage across the sensing capacitor, C_{ISR}, is:

$$V_{CISR} = I_L \bullet R_{SEN} \left[\frac{1 + \frac{sESL}{R_{SEN}}}{1 + sR_{ISR} \bullet C_{ISR}} \right]$$

In the frequency domain, the second term in the above equation must be equal to 1 to ensure that the voltage across the filter capacitor is independent of operating frequency. To meet this requirement, the value of the RC filter should fulfill the following condition:

$$R_{ISR} \bullet C_{ISR} = \frac{ESL}{R_{SEN}}$$

The ESL value can be obtained from the manufacturer's data sheet or estimated with an oscilloscope, as shown in the Figure 4 waveform, using the following equation:

$$ESL = \frac{V_{ESL(ON)} + \left|V_{ESL(OFF)}\right|}{\Delta I_L \left(\frac{1}{t_{ON}} + \frac{1}{t_{OFF}} \right)}$$

where t_{ON} is the TG on time and t_{OFF} is the TG off time.

For high efficiency applications, the inductor DCR provides a method of sensing the inductor current without incurring additional power loss from a sense resistor. The DCR of the inductor represents the small amount of resistance in the copper winding, which can be less than 1mΩ for today's low value, high current inductors. Figure 5 shows a simplified inductor model, which can be modeled with an ideal inductor, L, in series with its parasitic DCR. The DCR value can be obtained from the inductor manufacturer's

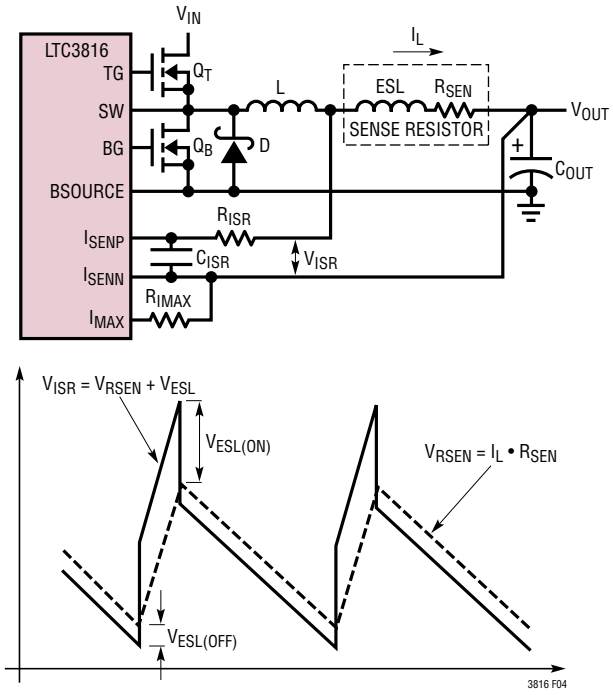

Figure 4. Current Limit Sensing Using a Low Value Sense Resistor

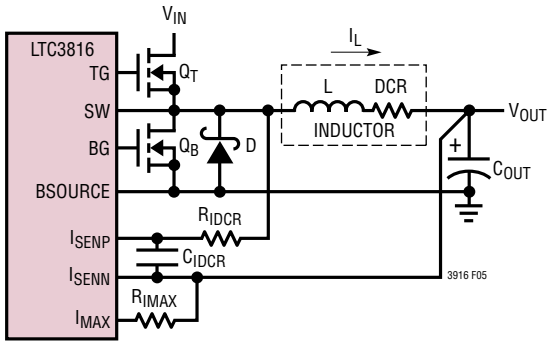

Figure 5. Current Limit Sensing Using Inductor DCR

data sheet. Similar to the sense resistor application circuit, the voltage across the inductor DCR can be extracted from a lowpass filter and the current limit threshold is given by the following equation:

$$I_{L(PEAK)} = \frac{I_{IMAX} \bullet R_{IMAX}}{R_{DCR}}$$

$$I_{LOAD(MAX)} < I_{LIMIT} = I_{L(PEAK)} - \frac{\Delta I_L}{2} = \frac{I_{IMAX} \bullet R_{IMAX}}{R_{DCR}} - \frac{\Delta I_L}{2}$$

$$\text{if } R_{IDCR} \bullet C_{IDCR} = \frac{L}{R_{DCR}}$$

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Note that the value of R_{DCR} must account for its temperature coefficient, which is approximately 0.39%/°C.

The current limit architecture of the LTC3816 allows short durations of instantaneous overload. Upon power-up, the current limit threshold is set to 1×, equal to I_{LIMIT}. The load is limited to I_{LIMIT} until the switcher output reaches its V_{BOOT} potential. Beyond this point, during the VID DAC slewing interval, the I_{MAX} sourcing current automatically switches from 10µA to 20µA and the current limit threshold increases to 2× to enable the output capacitor voltage to track the DAC transition. If the controller detects that there is an overload condition when the DAC is not slewing, the current limit threshold increases to 2× for a duration of 45µs. If the overload interval is shorter than 45µs, the IC allows another overcurrent event within the next 630µs, as shown in Figure 6a. However, if an overload occurs within the 630µs following the second event, the controller current limits, as shown in Figure 6b.

If the overload condition persists for more than 45µs, the LTC3816 allows the 2× current limit to continue for another cycle. After 90µs, the I_{MAX} current returns to 10µA, and the output load is limited to 1× for the next 630µs as shown in Figure 6c. Figure 6d shows the condition when a repetitive overload event triggers current limit.

Figure 6e shows that at any instant, if the load current is above 1× for more than 90µs, or higher than 2×, the controller enters current limit. Under this condition, the TG duty cycle is reduced and the SS capacitor is discharged

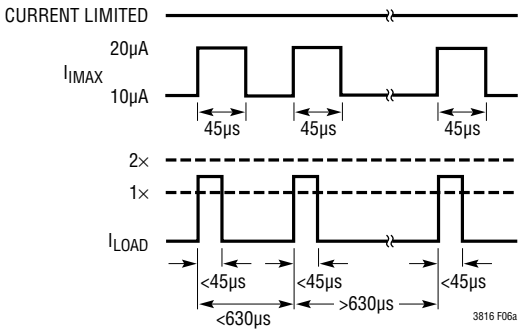

Figure 6a. Permissible Overload

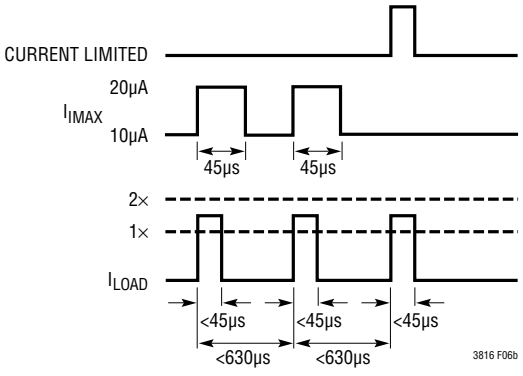

Figure 6b. Repeated Overload Triggers Current Limit

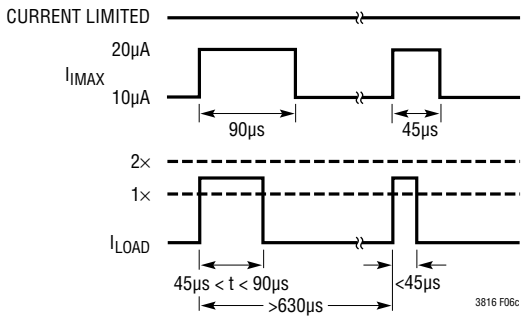

Figure 6c. Allowable Longer Overload Condition

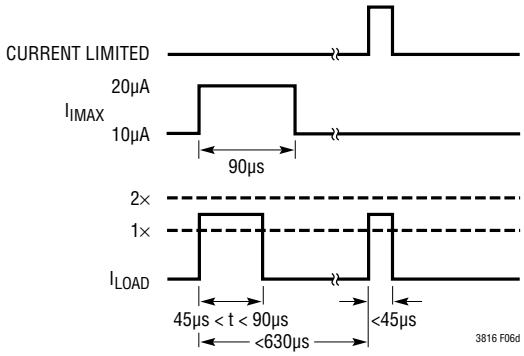

Figure 6d. Allowable Longer Overload Condition, Followed by Repeated Overload Triggers Current Limit

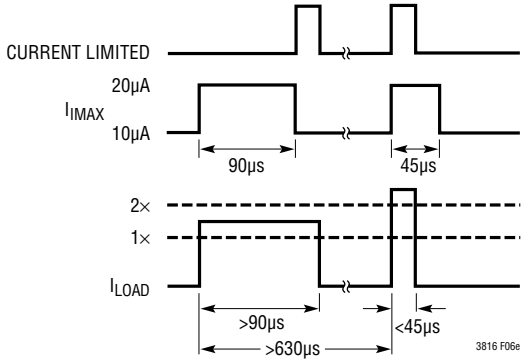

Figure 6e. Long Overload or Excessive Loading Triggers Current Limit Condition

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to lower the regulator output voltage. This current limit condition persists until the fault condition disappears or the controller detects a low output voltage fault and forces the switcher output to latch off. Once the output voltage is lower than the power good threshold, the controller limits the maximum load to 1× to reduce the short-circuit current.

ACTIVE VOLTAGE POSITIONING (AVP)

In a conventional buck converter, the feedback control regulates the output voltage to the same level for the entire load range as shown in Figure 7a. The peak-to-peak output voltage spikes resulting from the load step must be smaller than the voltage tolerance window.

To reduce the regulator output voltage peak-to-peak perturbation resulting from a load transient, the LTC3816 modulates the output voltage based on the output loading current. The built-in AVP circuit lowers the output voltage proportional to the load current as shown in Figure 7b. Figure 7c shows the transient response with the AVP function. The AVP voltage droop reduces the peak-to-peak output voltage perturbation. As a result, the AVP topology requires fewer capacitors at the regulator output to achieve the same voltage tolerance window.

The AVP circuit obtains the load current information from the sense resistor or the inductor DCR as shown in Figure 8. The voltage drop across the sense resistor is extracted

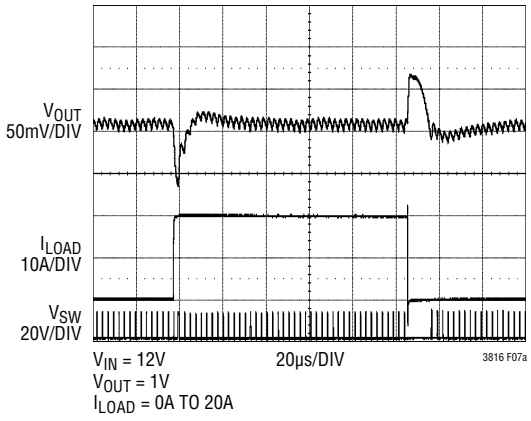

Figure 7a. Transient Waveform Without AVP. The Transient Peak-to-Peak Spike ≈ 130mV. The AITC Amplifier is Configured as a Unity-Gain Amplifier

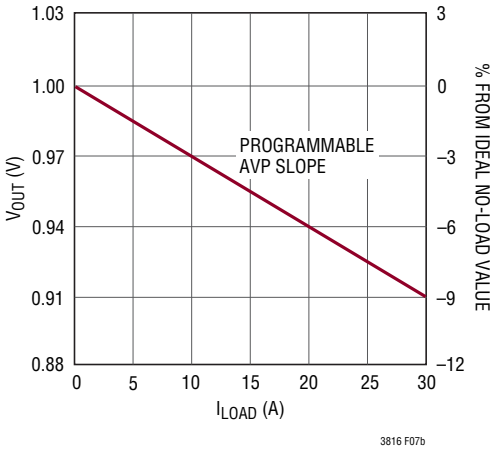

Figure 7b. AVP DC Transfer Curve

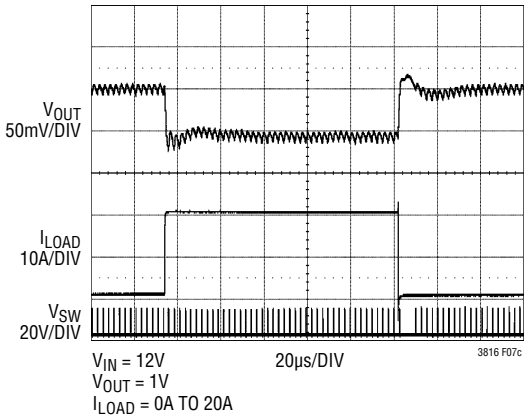

Figure 7c. Transient Waveform with AVP Slope = –3mV/A, Using The Same Inductor and Output Capacitor as Figure 7a. The Transient Peak-to-Peak Perturbation is Reduced to About 85mV

by the AITC amplifier and summed with the differential amplifier output voltage. The resulting output is servoed to the VID DAC voltage. At higher load current, the voltage drop across the sense resistor increases, resulting in a lower switcher output voltage. Typically, the system requirement defines the amount of AVP gain ensuring that the output voltage remains within the regulator supply tolerance band over the full range of load conditions. Figure 8 includes the components required to compensate for the sense resistor parasitic inductance. The AVP DC transfer function is:

$$V_{OUT} = V_{DAC} - A_{AVP(SR)} \bullet I_L = V_{DAC} - A_{G(SR)} \bullet I_L \bullet R_{SEN}$$

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where $A_{AVP(SR)}$ is the AVP gain with sense resistor configuration and $A_{G(SR)}$ is the sense resistor gain:

$$A_{AVP(SR)} = A_{G(SR)} \bullet R_{SEN} \text{ and } A_{G(SR)} = \frac{R_{VSR}}{R_{AVPSR}}.$$

$$R_{VSR} \bullet C_{VSR} = \frac{ESL}{R_{SEN}}$$

Figure 9 shows the AVP configuration with current sense implemented using the inductor DCR. The AVP DC transfer function is:

$$V_{OUT} = V_{DAC} - A_{AVP(DCR)} \bullet I_L = V_{DAC} - A_{G(DCR)} \bullet I_L \bullet R_{DCR}$$

where:

$$A_{AVP(DCR)} = A_{G(DCR)} \bullet R_{DCR} \text{ and } A_{G(DCR)} = \frac{R_{VDCR}}{R_{AVPDCR}}$$

$$R_{VDCR} \bullet C_{VDCR} = \frac{L}{R_{DCR}}$$

TEMPERATURE COMPENSATED ACTIVE VOLTAGE POSITIONING (AVP) WITH INDUCTOR DCR

The inductor DCR AVP configuration improves the regulator efficiency by eliminating the power losses associated with a sense resistor. However, without proper temperature compensation, the positive temperature coefficient of the inductor DCR, 0.39%/°C, may compromise the output voltage accuracy. As the temperature of the inductor rises, its DCR value increases, resulting in a greater V_{OUT} droop rate (higher AVP gain). To compensate for the DCR temperature shift, replace the resistor R_{VDCR} in Figure 9 with an NTC resistor placed as close as possible to the inductor. Ideally, the NTC resistor should have the same temperature as the inductor. As temperature increases, the NTC resistance drops, resulting in a reduction in the AITC amplifier voltage gain. This compensates for the increase in DCR resistance and maintains the AVP gain. The NTC resistor, however, is highly nonlinear and must be linearized. Figure 10 shows

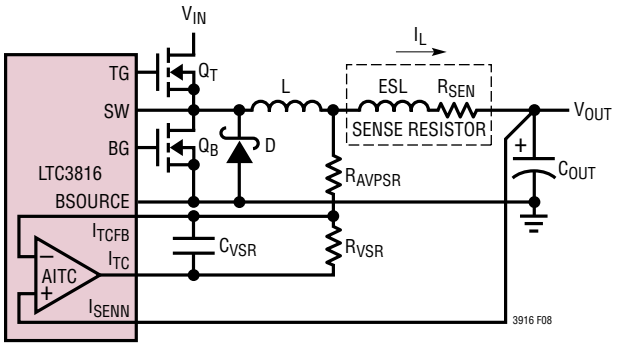

Figure 8. AVP Configuration with a Sense Resistor

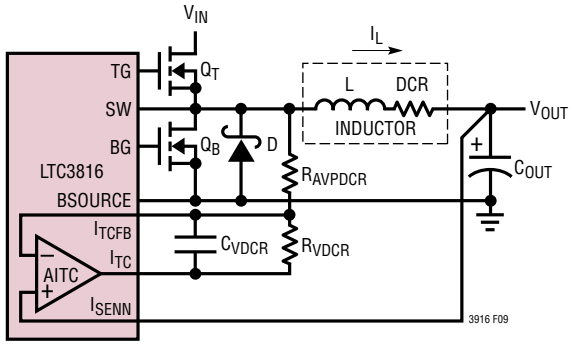

Figure 9. AVP Configuration with Inductor DCR Current Sense

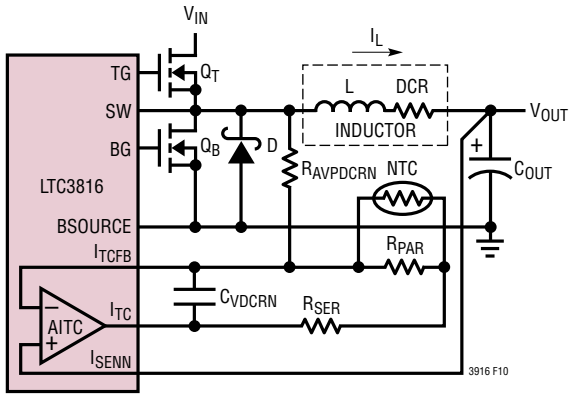

Figure 10. AVP with Inductor DCR Current Sense and NTC Temperature Compensation

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the NTC compensation network. To determine the component values, first, select the NTC with room temperature resistance approximately equal to R_{VDCR} that has the smallest temperature coefficient (β constant in the NTC data sheet. Using an NTC with a higher β constant generates a less optimal temperature compensation). Next, calculate the resistances R_{PAR} and R_{SER} from the following equations where the NTC resistances at different temperatures is obtained from the manufacturer's data sheet.

$$R_{PAR} = R_{NTC} \text{ at } 25°C$$

$$R_{SER} \approx \frac{10}{3}\left[\left(R_{PAR} \| \left(R_{NTC} \text{ at } 0°C\right)\right) - \left(R_{PAR} \| \left(R_{NTC} \text{ at } 75°C\right)\right)\right] - \left(R_{PAR} \| \left(R_{NTC} \text{ at } 25°C\right)\right)$$

Note that the above equations optimize temperature compensation at hot. At extreme cold temperature, the temperature compensation is less effective.

With the NTC resistor network, the temperature compensated AVP transfer function becomes:

$$V_{OUT} = V_{DAC} - A_{AVP(DCRN)} \bullet I_L = V_{DAC} - A_{G(DCRN)} \bullet I_L \bullet R_{DCR}$$

where $A_{AVP(DCRN)}$ and $A_{G(DCRN)}$ are the AVP and DCR gain using the inductor DCR current sense with NTC temperature compensation configuration.

$$A_{AVP(DCRN)} = A_{G(DCRN)} \bullet R_{DCR} \text{ and } A_{G(DCRN)} = \frac{R_{NTCNET}}{R_{AVPDCRN}}$$

$$C_{VDCRN} = \frac{L}{R_{NTCNET} \bullet R_{DCR}}$$

$$R_{NTCNET} = \left[R_{SER} + \left(R_{PAR} \| R_{NTC}\right)\right]$$

Figure 11a shows the room temperature AVP DC transfer curves obtained using inductor DCR current sense with and without NTC temperature compensation. There is only a slight difference in the transfer curve at heavy load. Figure 11b shows the AVP transfer curve obtained at 125°C, it shows the improvement in AVP accuracy with the NTC resistor network.

Figure 12 shows another easy way to compensate for the inductor DCR temperature coefficient. In this configuration, a linear PTC resistor is connected from the SW node to the I_{TCFB} pin. The PTC thermistor's temperature coefficient of 0.411%/°C compensates for the change in DCR

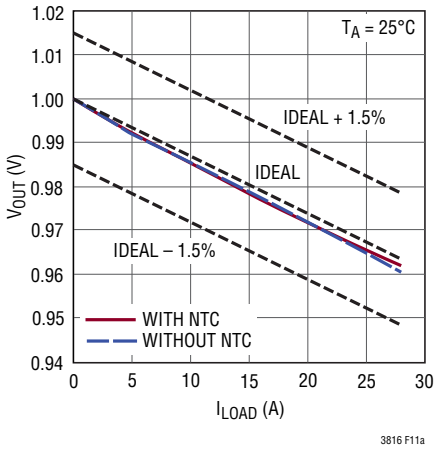

Figure 11a. AVP Transfer Curve Using Vishay IHLP-5050CE-01 0.33µH (DCR = 1.3mΩ) Inductor DCR Current Sense with $A_{G(DCRN)}$ = 1 at T_A = 25°C

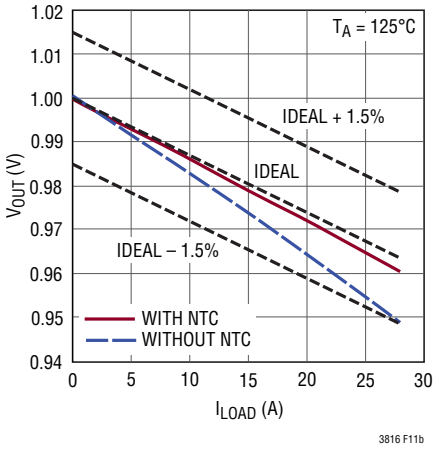

Figure 11b. Same Setup as Figure 11a. Improvement in AVP Accuracy with NTC Temperature Compensation Network at T_A = 125°C

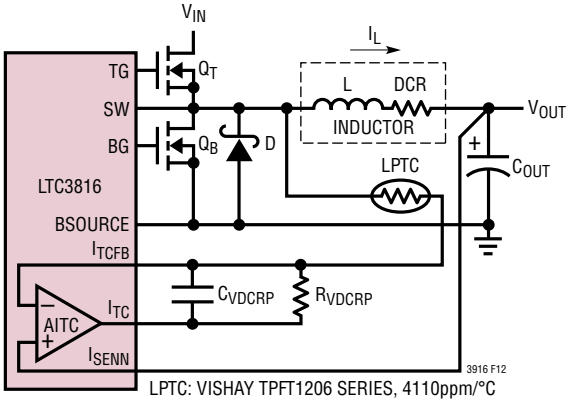

Figure 12. AVP Using Inductor DCR Current Sense with Linear PTC Temperature Compensation

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resistance (0.39%/°C) and produces a near perfect AVP slope across temperature.

$$V_{OUT} = V_{DAC} - A_{AVP(DCRP)} \bullet I_L = V_{DAC} - A_{G(DCRP)} \bullet I_L \bullet R_{DCR}$$

where:

$$A_{AVP(DCRP)} = A_{G(DCRP)} \bullet R_{DCR} \text{ and } A_{G(DCRP)} = \frac{R_{VDCRP}}{R_{LPTC}}$$

$$C_{VDCRP} = \frac{L}{R_{VDCRP} \bullet R_{DCR}}$$

I_{MON}

To facilitate CPU monitoring of load current in an IMVP-6.5 application, the LTC3816 forces the I_{MON} pin voltage to be proportional to the average load current. As shown in Figure 13, the AITC and the unity-gain amplifiers force the voltage across the resistor $R_{PREIMON}$ to be equal to the voltage drop across the sense resistor. A current is supplied to R_{IMON} that is three times greater than the current in $R_{PREIMON}$. The voltage across the R_{IMON} resistor is equal to:

$$V_{IMON} = 3 \bullet \left(I_L \bullet R_{SEN}\right) \frac{R_{VSR}}{R_{AVPSR}} \bullet \frac{R_{IMON}}{R_{PREIMON}}$$

To prevent the ground difference between the CPU and the regulator from affecting the I_{MON} voltage accuracy, the negative terminal of the resistor R_{IMON} should be connected directly to the CPU $V_{SS(SEN)}$ pin. Depending on the output load requirements, the I_{MON} voltage gain can be programmed by changing the ratio of the R_{IMON} and $R_{PREIMON}$ resistances. A capacitor should be added in parallel with the resistor R_{IMON} to remove the switching ripple. The value of the capacitor C_{IMON} is determined by the following equation:

$$C_{IMON} = \frac{t_{IMON}}{R_{IMON}}$$

where t_{IMON} is the I_{MON} time constant and must be larger than 300µs.

In the IMVP-6.5 configuration, the I_{MON} pin potential is internally clamped to 1.1V with respect to the $V_{SS(SEN)}$ pin voltage. Forcing the $PREI_{MON}$ pin to $INTV_{CC}$ configures the LTC3816 as an IMVP-6 regulator.

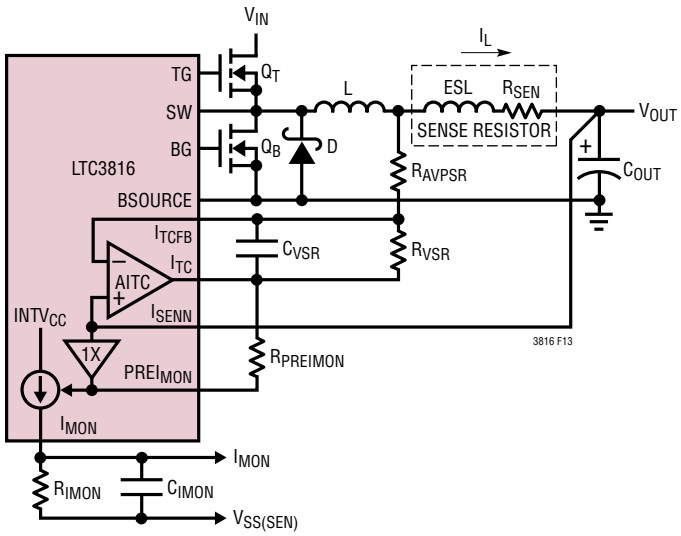

Figure 13. I_{MON} Configuration

FEEDBACK CONTROL

The LTC3816 feedback loop consists of the line feedforward circuit, the modulator, the external inductor, the output capacitor, the AITC and differential amplifier, and the feedback amplifier with its compensation network. All of these components affect loop behavior and need to be accounted for in the loop compensation.

Line Feedforward and Modulator

The modulator consists of the PWM generator, the output MOSFET drivers and the external MOSFETs themselves. The modulator gain varies linearly with the input voltage. The line feedforward circuit compensates for this change in gain and provides a constant gain from the error amplifier output to the SW node regardless of input voltage. From a feedback loop point of view, the combination of the line feedforward circuit and the modulator looks like a linear voltage transfer function from COMP to the SW node and has a gain roughly equal to:

$$A_{MOD} \approx 25V/V \approx 28dB$$

It has a fairly benign AC behavior at typical loop compensation frequencies with significant phase shift appearing at half the switching frequency.

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LC Filter

The external inductor and output capacitor combination causes a second order LC roll-off at the output with 180° of phase shift. At higher frequencies, the reactance of the output capacitor approaches its ESR, and the roll-off due to the capacitor stops, leaving –20dB/decade and 90° of phase shift. Beyond the ESR zero, the ceramic capacitor creates a high frequency pole. The LC filter transfer function, poles and zero locations are given by the following equations:

$$A_{LC} = \frac{V_{OUT}}{V_{SW}} \approx \frac{1+sR_{ESR} \bullet C_{BULK}}{\left(s^2 L_L C_{OUT} + sR_L C_{OUT} + 1\right)} \bullet \frac{1}{1+sR_{ESR}\dfrac{C_{BULK} \bullet C_{CER}}{C_{OUT}}}$$

$$f_{LC(DOUBLE\_POLE)} = \frac{1}{2\pi\sqrt{L_L C_{OUT}}}$$

$$f_{ESR(ZERO)} = \frac{1}{2\pi \bullet R_{ESR} \bullet C_{BULK}}$$

$$f_{CER(POLE)} = \frac{1}{2\pi \bullet R_{ESR}\dfrac{C_{BULK} \bullet C_{CER}}{C_{OUT}}}$$

where:

R_L includes DCR, sense resistance, PCB trace resistance and the turn-on resistance of the power MOSFET.

L_L includes the inductor inductance, PCB trace inductance and sense resistor ESL.

$C_{OUT} = C_{BULK} + C_{CER}$

AITC and Differential Amplifiers

With the sense resistor configuration, the AITC and the differential amplifiers add a double zero and a pole in the vicinity of the feedback loop crossover frequency, f_C, and multiple poles at higher frequencies. The simplified low frequency transfer function from the regulator output node to the SERVO pin, as shown in Figure 14a, is given by the following equation:

$$\frac{V_{SERVO}}{V_{OUT}} \approx \frac{1+sA_{(SR)}+s^2B_{(SR)}}{1+sR_{ESR} \bullet C_{BULK}}$$

where:

$A_{(SR)} = R_{ESR} \bullet C_{BULK} + A_{G(SR)} \bullet R_{SEN} \bullet C_{OUT}$

$B_{(SR)} = A_{G(SR)} \bullet R_{SEN} \bullet R_{ESR} \bullet C_{BULK} \bullet C_{CER}$

Similarly, for the DCR configuration with NTC compensation, the simplified low frequency transfer function is given by:

$$\frac{V_{SERVO}}{V_{OUT}} \approx \frac{1+sA_{(DCR)}+s^2B_{(DCR)}}{1+sR_{ESR} \bullet C_{BULK}}$$

where:

$A_{(DCR)} = R_{ESR} \bullet C_{BULK} + A_{G(DCR)} \bullet R_{DCR} \bullet C_{OUT}$

$B_{(DCR)} = A_{G(DCRN)} \bullet R_{DCR} \bullet R_{ESR} \bullet C_{BULK} \bullet C_{CER}$

Note that with either the sense resistor or the DCR current sense configuration, the AVP circuitry introduces a pole at the same location as the LC lowpass filter ESR zero. This cancels the increase in gain and phase caused by the ESR zero. Fortunately, the zero in the AVP transfer function is typically within the closed-loop bandwidth and provides a beneficial phase boost at the crossover frequency.

Error Amplifier

The error amplifier provides most of the low frequency loop gain and servos the switcher output voltage to the VID DAC potential minus the AVP droop. After selecting the inductor, the output capacitor and the AVP component values, the control loop is compensated by tailoring the frequency response of the error amplifier. A typical LTC3816 application uses Type 3 compensation to frequency compensate the feedback loop. Figure 14a and Figure 14b show the LTC3816 error amplifier Type 3 configuration. The transfer function of this amplifier is given by the following equation:

$$\frac{V_{COMP}}{V_{SERVO}} = -\frac{\left(1+sR_C \bullet C_C\right)\left(1+sR1 \bullet C_{FF}\right)}{sR1\left(C_C + C_{C1}\right)\left(1+sR_C\dfrac{C_C \bullet C_{C1}}{C_C + C_{C1}}\right)}$$

The error amplifier component values can be obtained using the following guidelines.