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Dual, 2-Phase Step-Down Controller with Tracking

FEATURES

- **Dual, 180° Phased Controllers Reduce Required Input Capacitance and Power Supply Induced Noise**
- **Tracking for Both Outputs**
- **Constant Frequency Current Mode Control**
- **Wide V_{IN} Range: 4.5V to 28V Operation**
- **Power Good Output Voltage Indicator**
- **Adjustable Soft-Start Current Ramping**
- **Foldback Output Current Limiting–Disabled at Start-Up**
- **No Reverse Current During Soft-Start Interval**
- Clock Output for 3-, 4-, 6-Phase Operation
- Dual N-Channel MOSFET Synchronous Drive
- ±1% Output Voltage Accuracy
- Phase-Lockable Fixed Frequency 260kHz to 550kHz
- OPTI-LOOP® Compensation Minimizes C_{OUT}
- Very Low Dropout Operation: 99% Duty Cycle
- Output Overvoltage Protection
- Small 28-Lead SSOP and 5mm × 5mm QFN Packages

APPLICATIONS

- Telecom Infrastructure
- ASIC Power Supply
- Industry Equipment

DESCRIPTION

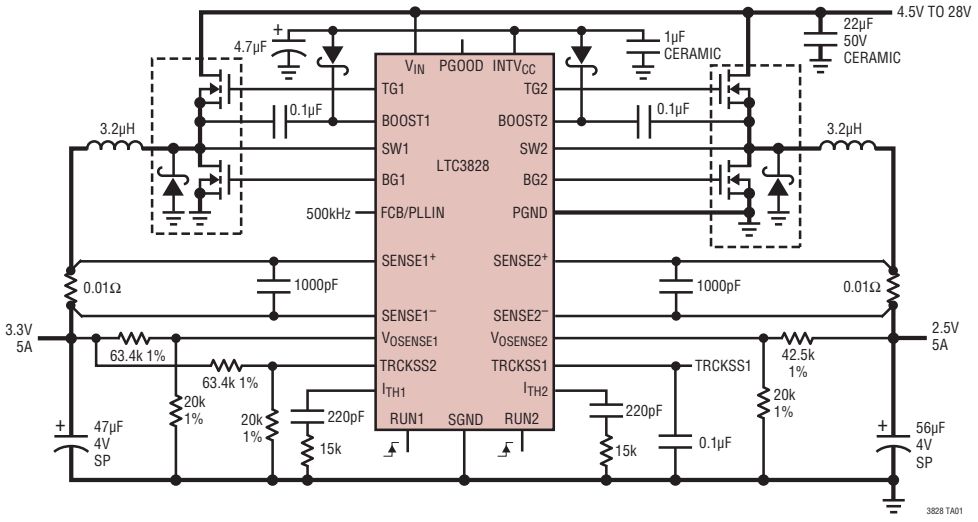
The LTC®3828 is a dual high performance step-down switching regulator controller that drives all N-channel synchronous power MOSFET stages. A constant frequency current mode architecture allows for a phase-lockable frequency of up to 550kHz. The TRCKSS pin provides both soft-start and tracking functions. Multiple LTC3828s can be daisy-chained in applications requiring more than two voltages to be tracked.

OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The precision 0.8V reference and power good output indicator are compatible with a wide 4.5V to 28V (30V maximum) input supply range, encompassing all battery chemistries.

The RUN pins control their respective channels independently. The FCB/PLLIN pin selects among Burst Mode® operation, skip-cycle mode and continuous current mode. Current foldback limits MOSFET dissipation during short-circuit conditions. Reverse current and current foldback functions are disabled during soft-start.

TYPICAL APPLICATION

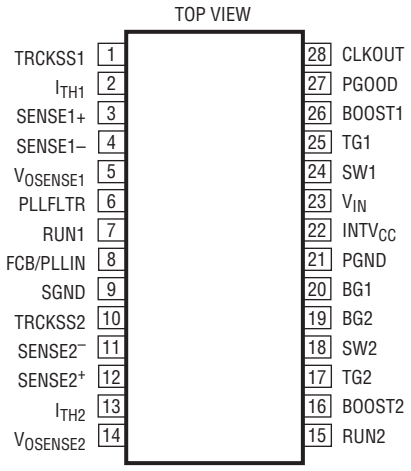
High Efficiency Dual 2.5V/3.3V Step-Down Converter with Tracking



ABSOLUTE MAXIMUM RATINGS (Note 1)

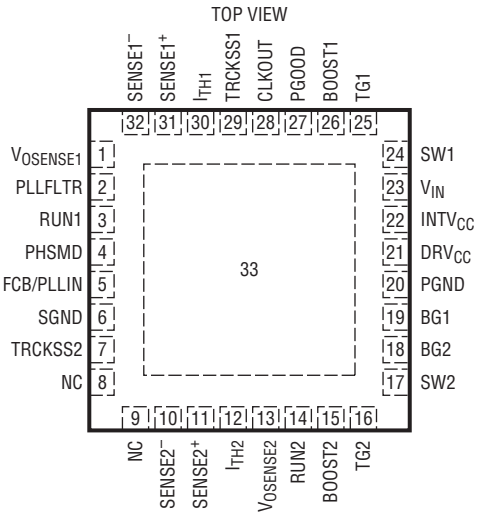
Input Supply Voltage (V_{IN}) ..... 30V to –0.3V
Top Side Driver Voltages
BOOST1, BOOST2..... 36V to –0.3V
Switch Voltage (SW1, SW2) ..... 30V to –5V
$INTV_{CC}$, DRV_{CC}, RUN1, RUN2, (BOOST1-SW1),
(BOOST2-SW2)..... 7V to –0.3V
$SENSE1^+$, $SENSE2^+$, $SENSE1^–$,
$SENSE2^–$ Voltages ..... (1.1)$INTV_{CC}$ to –0.3V
FCB/PLLIN, PLLFLTR, CLKOUT,
PHSMD Voltage ..... $INTV_{CC}$ to –0.3V
TRCKSS1, TRCKSS2..... $INTV_{CC}$ to –0.3V
PGOOD..... 5.5V to –0.3V
I_{TH1}, I_{TH2}, $V_{OSENSE1}$, $V_{OSENSE2}$ Voltages ... 2.7V to –0.3V
Peak Output Current <10µs (TG1, TG2, BG1, BG2).... 3A
$INTV_{CC}$ Peak Output Current (Note 8) 50mA
Operating Temperature Range (Note 7)
LTC3828E..... –40°C to 85°C
Junction Temperature (Note 2) ..... 125°C
Storage Temperature Range..... –65°C to 125°C
Reflow Peak Body Temperature (UH Package)..... 260°C
Lead Temperature (Soldering, 10 sec)
G Package..... 300°C

PIN CONFIGURATION



G PACKAGE
28-LEAD PLASTIC SSOP

T_{JMAX} = 125°C, θ_{JA} = 95°C/W



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3828EG#PBF	LTC3828EG#TRPBF	LTC3828EG	28-Lead Plastic SSOP	–40°C to 85°C
LTC3828EUH#PBF	LTC3828EUH#TRPBF	3828	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN1, 2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
$V_{OSENSE1, 2}$	Regulated Feedback Voltage	(Note 3); $I_{TH1, 2}$ Voltage = 1.2V	●	0.792	0.800	0.808	V
$I_{VOSENSE1, 2}$	Feedback Current	(Note 3)			±5	±50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.6V to 28V (Note 3)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 3) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2.0V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
$g_{m1, 2}$	Transconductance Amplifier g_m	$I_{TH1, 2}$ = 1.2V; Sink/Source 5µA; (Note 3)			1.3		mmho
$g_{mGBW1, 2}$	Transconductance Amplifier GBW	$I_{TH1, 2}$ = 1.2V; (Note 3)			3		MHz
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 4) V_{OUT1} = 5V $V_{RUN/SS1, 2}$ = 0V			 2 20	 3 100	 mA µA
V_{FCB}	Forced Continuous Threshold		●	0.76	0.800	0.84	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.85V		–0.50	–0.18	–0.1	µA
$V_{BINHIBIT}$	Burst Inhibit (Constant Frequency) Threshold	Measured at FCB pin			4.3	4.8	V
UVLO	Undervoltage Lockout	V_{IN} Ramping Down	●		3.5	4	V
V_{OVL}	Feedback Overvoltage Lockout	Measured at $V_{OSENSE1, 2}$	●	0.84	0.86	0.88	V
I_{SENSE}	Sense Pins Total Source Current	(Each Channel); $V_{SENSE1^-, 2^-}$ = $V_{SENSE1^+, 2^+}$ = 0V		–90	–65		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.4		%
$I_{TRCKSS1,2}$	Soft-Start Charge Current	$V_{TRCKSS1, 2}$ = 0.2V		0.5	1.2		µA
$V_{RUN1, 2}$ ON	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising		1.0	1.5	2.0	V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{OSENSE1, 2}$ = 0.7V,$V_{SENSE1^-, 2^-}$ = 5V $V_{OSENSE1, 2}$ = 0.7V,$V_{SENSE1^-, 2^-}$ = 5V	 ●	62 60	75 75	85 88	mV mV
 TG1, 2 tr TG1, 2 tf	TG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 55 55	 100 100	 ns ns
 BG1, 2 tr BG1, 2 tf	BG Transition Time: Rise Time Fall Time	(Note 5) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 65 55	 120 100	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			60		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			80		ns
$t_{ON(MIN)}$	Minimum On-Time	Tested with a Square Wave (Note 6)			120		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 30V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.2	2.0	%
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	$V_{PLLFLTR}$ = 1.2V		360	400	440	kHz
f_{LOW}	Lowest Frequency	$V_{PLLFLTR}$ = 0V		230	260	290	kHz
f_{HIGH}	Highest Frequency	$V_{PLLFLTR}$ ≥ 2.4V		480	550	590	kHz
$I_{PLLFLTR}$	Phase Detector Output Current Sinking Capability Sourcing Capability	$V_{PLLFLTR}$ = 1.2V $f_{PLLIN} < f_{NOM}$ $f_{PLLIN} > f_{NOM}$			 –17 17		 µA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN1, 2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±1	µA
V_{PG}	PGOOD Trip Level, Either Controller	V_{OSENSE} with Respect to Set Output Voltage V_{OSENSE} Ramping Down V_{OSENSE} Ramping Up		 –6 6	 –7.5 7.5	 –9.5 9.5	 % %

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3828UH: $T_J = T_A + (P_D \bullet 34°C/W)$

LTC3828G: $T_J = T_A + (P_D \bullet 95°C/W)$

Note 3: The IC is tested in a feedback loop that servos $V_{ITH1, 2}$ to a specified voltage and measures the resultant $V_{OSENSE1, 2}$.

Note 4: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 5: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 6: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see minimum on-time considerations in the Applications Information section).

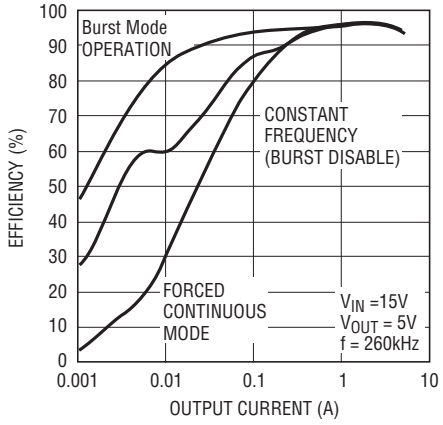
Note 7: The LTC3828E is guaranteed to meet performance specifications over the –40°C to 85°C operating temperature range as assured by design, characterization and correlation with statistical process controls.

Note 8: This parameter is guaranteed by design.

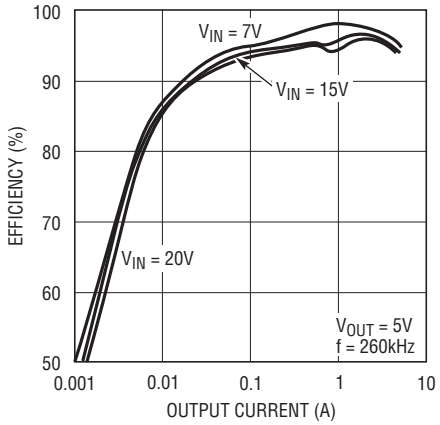
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C unless otherwise noted.

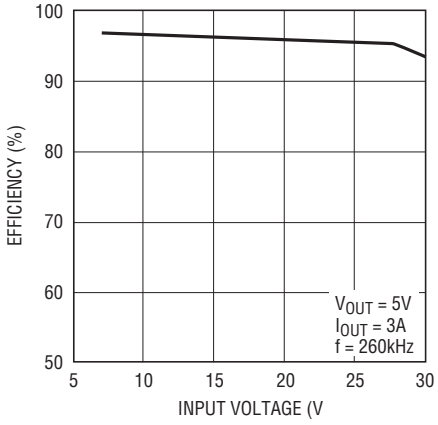
Efficiency vs Output Current and Mode (Figure 14)



Efficiency vs Output Current (Figure 14)

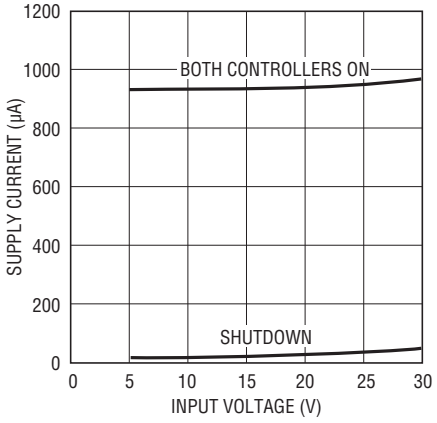


Efficiency vs Input Voltage (Figure 14)



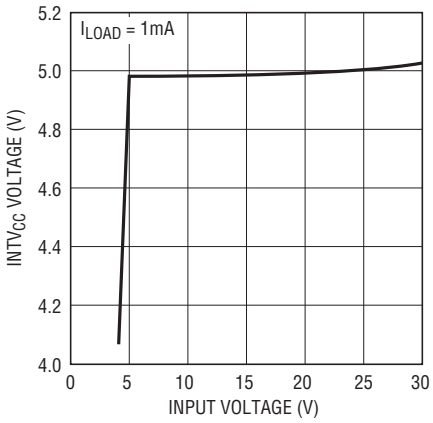
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Supply Current vs Input Voltage (Figure 14)



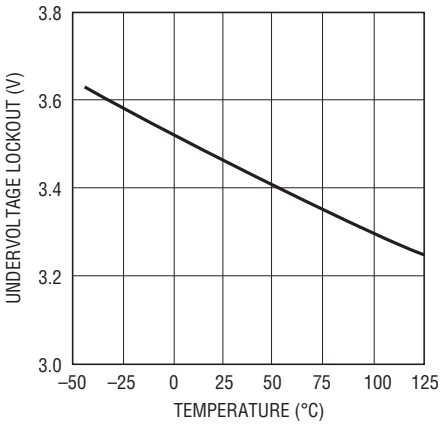
3828 G04

Internal 5V LDO Line Regulation



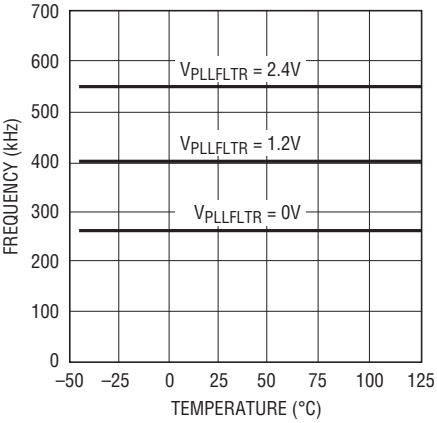
3828 G05

Undervoltage Lockout vs Temperature



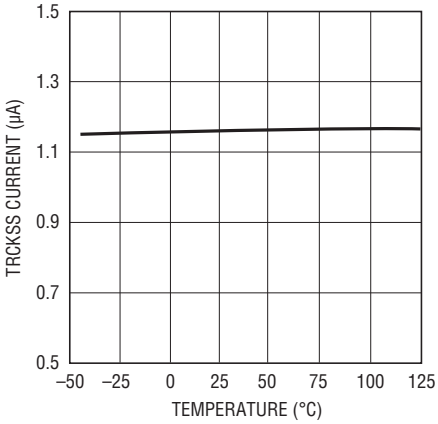
3828 G06

Oscillator Frequency vs Temperature



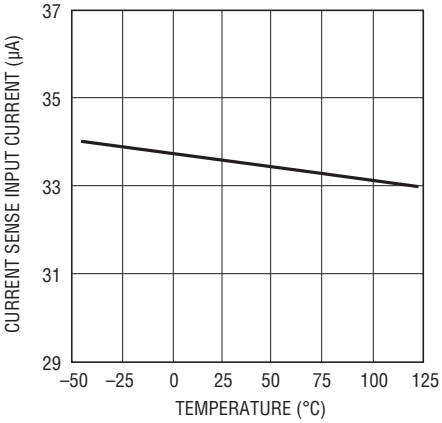
3828 G07

TRCKSS Current vs Temperature



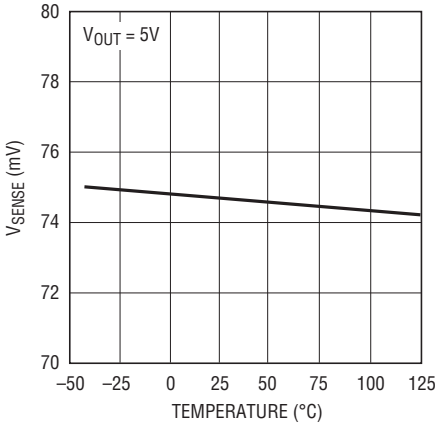
3828 G08

Current Sense Pin Input Current vs Temperature



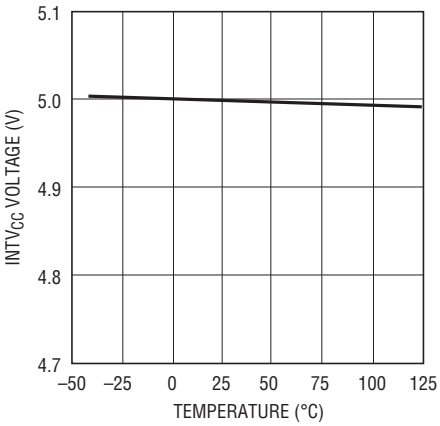
3828 G09

Maximum Current Sense Threshold vs Temperature



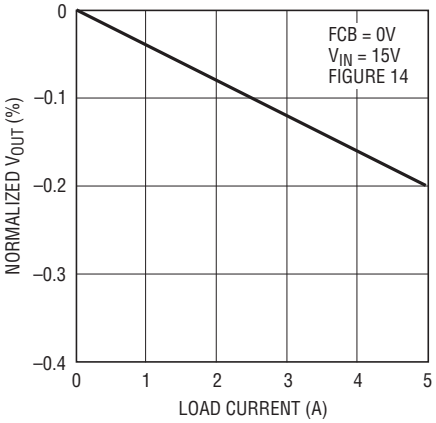
3828 G10

INTVCC Voltage vs Temperature



3828 G11

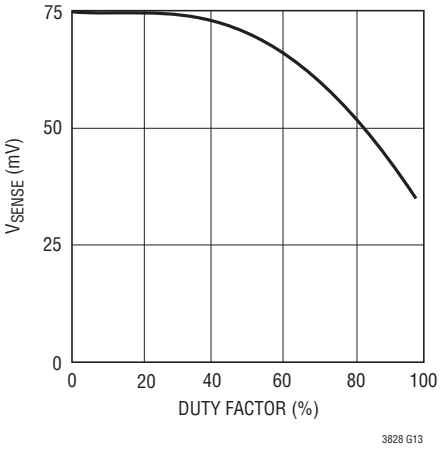
Load Regulation



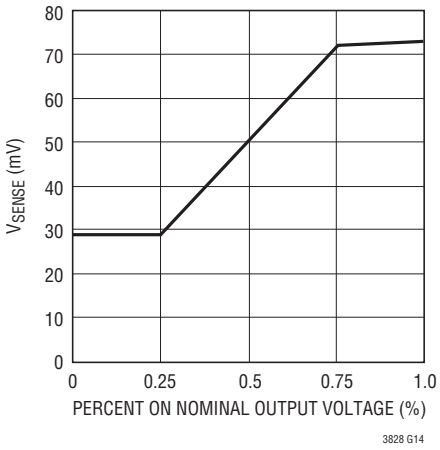
3828 G12

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

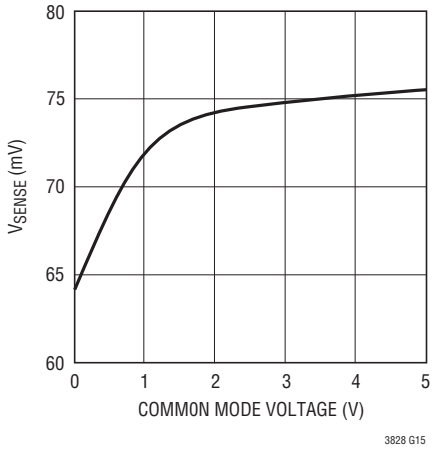
Maximum Current Sense Threshold vs Duty Factor



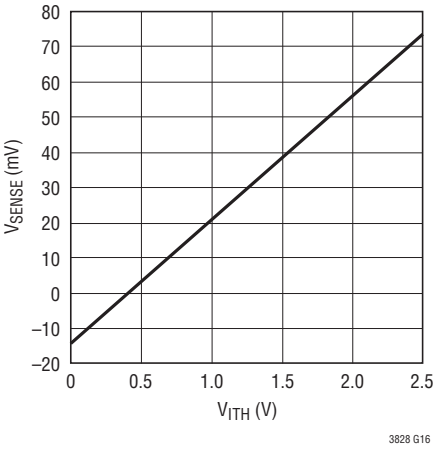
Maximum Current Sense Threshold vs Percent of Nominal Output Voltage (Foldback)



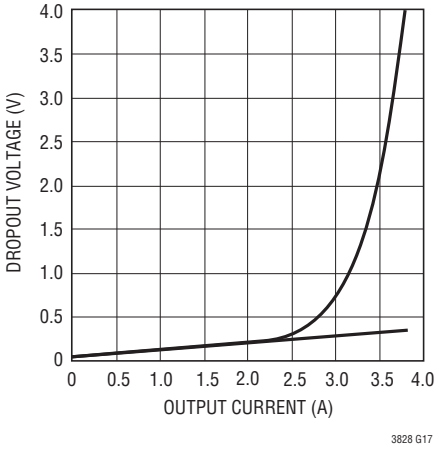
Maximum Current Sense Threshold vs Sense Common Mode Voltage



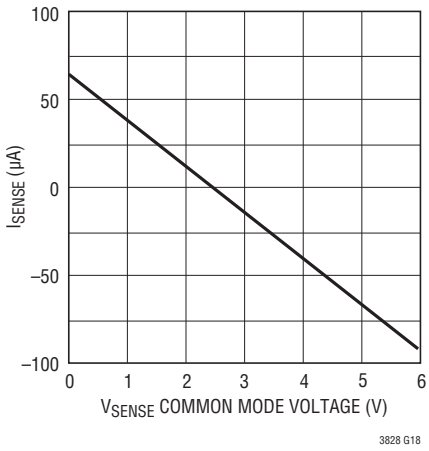
Current Sense Threshold vs I_{TH} Voltage



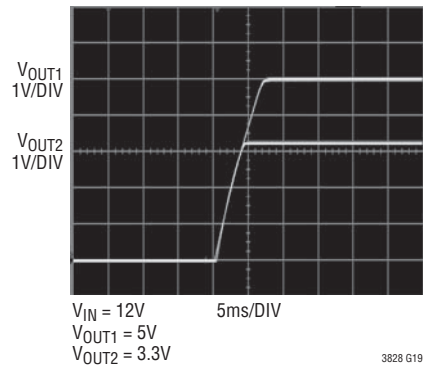
Dropout Voltage vs Output Current (Figure 14)



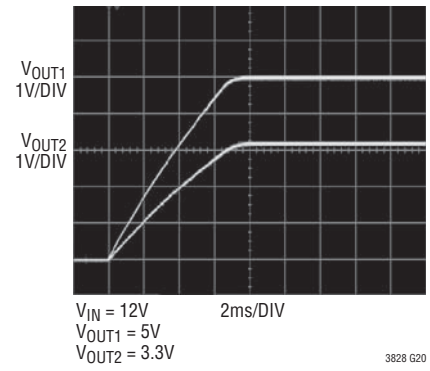
SENSE Pins Total Source Current



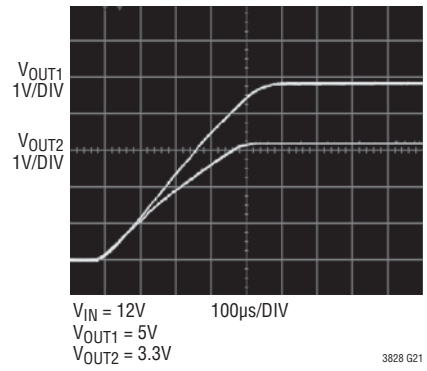
Soft Start-Up (Figure 14, with Coincident Tracking)



Soft Start-Up (Figure 14, with Ratiometric Tracking)

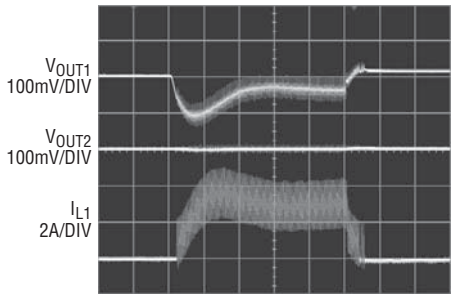


Soft Start-Up (Figure 14, with Internal Soft Start-Up)



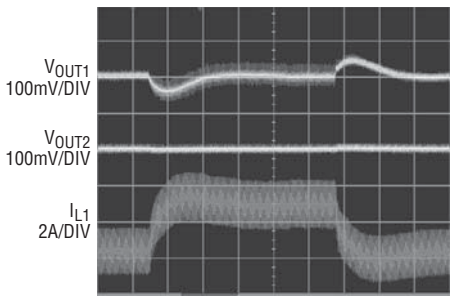
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C unless otherwise noted.

Load Step: Burst Mode Operation (Figure 14)



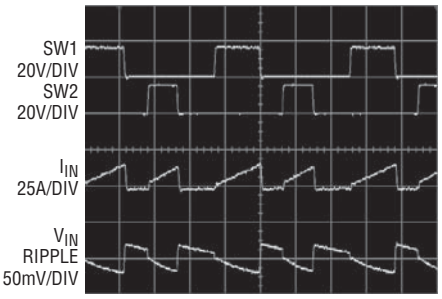
V_{IN} = 12V 50µs/DIV
V_{OUT1} = 5V
V_{OUT2} = 3.3V
LOAD STEP = 0A TO 3A
WITH RATIOMETRIC TRACKING
3828 G22

Load Step: Continuous Mode (Figure 14)



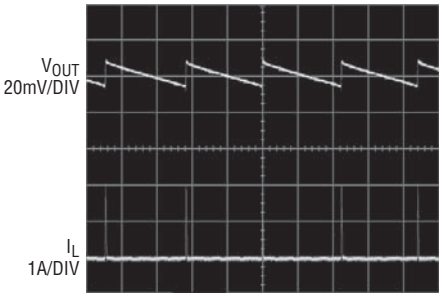
V_{IN} = 12V 50µs/DIV
V_{OUT1} = 5V
V_{OUT2} = 3.3V
LOAD STEP = 0A TO 3A
WITH RATIOMETRIC TRACKING
3828 G23

Input Source/Capacitor Instantaneous Current (Figure 14)



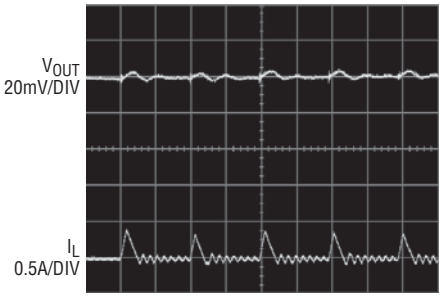
V_{IN} = 12V 500ns/DIV
V_{OUT1} = 5V
V_{OUT2} = 3.3V
$I_{OUT5} = I_{OUT3.3}$ = 2A
3828 G24

Burst Mode Operation (Figure 14)



V_{IN} = 12V 100µs/DIV
V_{OUT} = 5V
V_{FCB} = OPEN
I_{OUT} = 20mA
3828 G25

Constant Frequency (Burst Inhibit) Operation (Figure 14)



V_{IN} = 12V 2µs/DIV
V_{OUT} = 5V
V_{FCB} = 5V
I_{OUT} = 20mA
3828 G26

PIN FUNCTIONS (SSOP/QFN)

I_{TH1}, I_{TH2} (Pins 2, 13/Pins 30, 12): Error Amplifier Output and Switching Regulator Compensation Point. Each associated channels' current comparator trip point increases with this control voltage.

PHSMD (Pin 4, QFN Only): Control input to phase selector which determines the phase relationship between controller 1, controller 2 and the clockout signal.

$V_{OSENSE1}$, $V_{OSENSE2}$ (Pins 5, 14/Pins 1, 13): Error Amplifier Feedback Input. Receives the remotely-sensed feedback voltage for each controller from an external resistive divider across the output.

PLLFLTR (Pin 6/Pin 2): Filter Connection for Phase-Locked Loop. Alternatively, this pin can be driven with an AC or DC voltage source to vary the frequency of the internal oscillator.

FCB/PLLIN (Pin 8/Pin 5): Forced Continuous Control Input and External Synchronization Input to Phase Detector. Pulling this pin below 0.8V will force continuous synchronous operation. Feeding an external clock signal will synchronize the LTC3828 to the external clock.

PIN FUNCTIONS (SSOP/QFN)

SGND (Pin 9/Pin 6): Small-Signal Ground. Common to both controllers, this pin must be routed separately from high current grounds to the common (–) terminals of the C_{OUT} capacitors.

TRCKSS2, TRCKSS1 (Pins 10, 1/Pins 7, 29): Soft-Start and Output Voltage Tracking Inputs. When one channel is configured to be the master of two outputs a capacitor to ground at this pin sets the ramp rate. The slave channel tracks the output of the master channel by reproducing the V_{FB} voltage of the master channel with a resistor divider and applying that voltage to its track pin. An internal 1.2µA soft-start current is always charging these pins.

SENSE2$^-$, SENSE1$^-$ (Pins 11, 4/Pins 10, 32): The (–) Input to the Differential Current Comparators.

SENSE2$^+$, SENSE1$^+$ (Pins 12, 3/Pins 11, 31): The (+) Input to the Differential Current Comparators. The I_{TH} pin voltage and controlled offsets between the SENSE$^-$ and SENSE$^+$ pins in conjunction with R_{SENSE} set the current trip threshold.

RUN2, RUN1 (Pins 15, 7/Pins 14, 3): Run Control Inputs. Forcing RUN pins below 1V would shut down the circuitry required for that particular channel. Forcing the RUN pins over 2V would turn on the IC.

BOOST2, BOOST1 (Pins 16, 26/Pins 15, 26): Bootstrapped Supplies to the Topside Floating Drivers. Capacitors are connected between the boost and switch pins and Schottky diodes are tied between the boost and $INTV_{CC}$ pins. Voltage swing at the boost pins is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

TG2, TG1 (Pins 17, 25/Pins 16, 25): High Current Gate Drives for Top N-Channel MOSFETs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

SW2, SW1 (Pins 18, 24/Pins 17, 24): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

BG2, BG1 (Pins 19, 20/Pins 18, 19): High Current Gate Drives for Bottom (Synchronous) N-Channel MOSFETs. Voltage swing at these pins is from ground to $INTV_{CC}$.

PGND (Pin 21/Pin 20): Driver Power Ground. Connects to the sources of bottom (synchronous) N-channel MOSFETs, anodes of the Schottky rectifiers and the (–) terminal(s) of C_{IN}.

DRV_{CC} (Pin 21 QFN Only): External Power Input to Gate Drives. It can be connected with $INTV_{CC}$ together and use $INTV_{CC}$ as gate drives power supply.

$INTV_{CC}$ (Pin 22/Pin 22): Output of the Internal 5V Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 4.7µF tantalum or other low ESR capacitor.

V_{IN} (Pin 23/Pin 23): Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

PGOOD (Pin 27/Pin 27): Open-Drain Logic Output. PGOOD is pulled to ground when the voltage on either V_{OSENSE} pin is not within ±7.5% of its set point.

CLKOUT (Pin 28/Pin 28): Output clock signal available to daisy-chain other controller ICs for additional MOSFET driver stages/phases.

NC (Pins 8, 9 QFN Only): These “no connect” pins are not tied internally to anything. On the PC layout, these pin landings should be connected to the SGND plane under the IC.

Exposed Pad (Pin 33, QFN Only): Signal Ground. Must be soldered to the PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.

BLOCK DIAGRAM

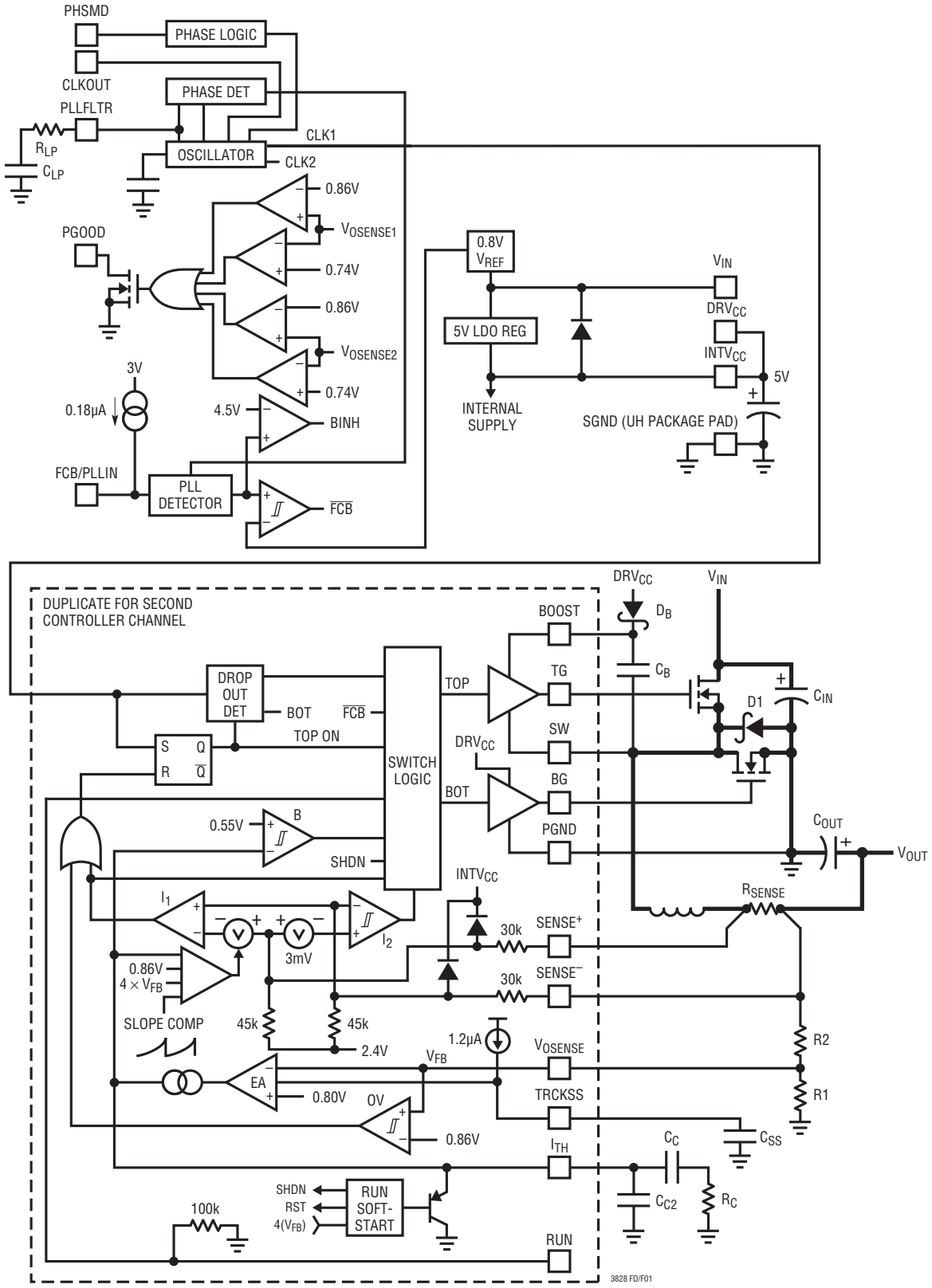


Figure 1

OPERATION (Refer to Functional Diagram)

Main Control Loop

The IC uses a constant frequency, current mode step-down architecture with the two controller channels operating 180 degrees out of phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_1, resets the RS latch. The peak inductor current at which I_1 resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The V_{OSENSE} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{OSENSE} relative to the 0.8V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by current comparator I_2, or the beginning of the next cycle.

The top MOSFET drivers are biased from floating bootstrap capacitor, C_B, which normally is recharged during each off cycle through an external diode when the top MOSFET turns off. As V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about 400ns every tenth cycle to allow C_B to recharge.

The main control loop is shut down by pulling the RUN pin low. When the RUN pin reaches 1.5V, the main control loop is enabled. When both RUN1 and RUN2 are low, all controller functions are shut down, including the 5V regulator.

Low Current Operation

The FCB/PLLIN pin is a multifunction pin providing two functions: 1) to accept external clock signal; and 2) to select among three modes of light load operations. When the FCB/PLLIN pin voltage is below 0.75V, the controller forces continuous PWM current mode operation. In this mode, the top and bottom MOSFETs are alternately turned on to maintain the output voltage independent of direction of inductor current. When the FCB/PLLIN pin is below V_{INTVCC} – 0.7V but greater than 0.8V, the controller enters Burst Mode operation. Burst Mode operation sets a minimum output current level before inhibiting the top switch and turns off the synchronous MOSFET(s) when the inductor current goes negative. This combination of requirements will, at low currents, force the I_{TH} pin below a voltage threshold that will temporarily inhibit turn-on of both output MOSFETs until the output voltage drops. There is 60mV of hysteresis in the burst comparator B tied to the I_{TH} pin. This hysteresis produces output signals to the MOSFETs that turn them on for several cycles, followed by a variable "sleep" interval depending upon the load current. The resultant output voltage ripple is held to a very small value by having the hysteretic comparator after the error amplifier gain block. When the FCB/PLLIN pin voltage is above 4.8V, the controller operates in constant frequency mode and the synchronous MOSFET is turned off when inductor current nears zero in each cycle.

In order to prevent erratic operation if no external connections are made to the FCB/PLLIN pin, the FCB/PLLIN pin has a 0.18µA internal current source pulling the pin high.

The following table summarizes the possible states available on the FCB/PLLIN pin:

Table 1

FCB/PLLIN PIN	CONDITION
0V to 0.75V	Forced Continuous Both Controllers (Current Reversal Allowed—Burst Inhibited)
0.85V < $V_{FCB/PLLIN}$ < 4.3V or Open	Minimum Peak Current Induces Burst Mode Operation No Current Reversal Allowed
>4.8V	Burst Mode Operation Disabled Constant Frequency Mode Enabled No Current Reversal Allowed No Minimum Peak Current

Besides providing a logic input to select light load operation mode, the FCB/PLLIN pin acts as the input for external clock synchronization. Upon detecting the presence of an external clock signal, channel 1 will lock on to this external clock and this will be followed by channel 2 (see Frequency Synchronization section). The LTC3828 defaults to forced continuous mode when sychronized to an external clock.

OPERATION (Refer to Functional Diagram)

Frequency Synchronization

The phase-locked loop allows the internal oscillator to be synchronized to an external source via the FCB/PLLIN pin. The output of the phase detector at the PLLFLTR pin is also the DC frequency control input of the oscillator that operates over a 260kHz to 550kHz range corresponding to a DC voltage input from 0V to 2.4V. When locked, the PLL aligns the turn on of the top MOSFET to the rising edge of the synchronizing signal.

The internal master oscillator runs at a frequency twelve times that of each phase switching frequency. The PHSMD pin (UH package only) determines the relative phases between the internal controllers as well as the CLKOUT signal as shown in Table 2. The phases tabulated are relative to zero phase being defined as the rising edge of the top gate (TG1) driver output of controller 1.

Table 2

V_{PHSMD}	GND	OPEN	$INTV_{CC}$
Controller 1	0°	0°	0°
Controller 2	180°	180°	240°
CLKOUT	60°	90°	120°

The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or separate outputs. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A 2-phase, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

In the G28 package, CLKOUT is 90° out of phase with channel 1 and channel 2.

Constant Frequency Operation

When the FCB/PLLIN pin is tied to $INTV_{CC}$, Burst Mode operation is disabled and the forced minimum output current requirement is removed. This provides constant frequency, discontinuous current (preventing reverse inductor current) operation over the widest possible output current range. This constant frequency operation is not as efficient as Burst Mode operation, but does provide a lower noise, constant frequency operating mode down to approximately 1% of the designed maximum output current.

Continuous Current (PWM) Operation

Tying the FCB/PLLIN pin to ground will force continuous current operation. This is the least efficient operating mode, but may be desirable in certain applications. The output can source or sink current in this mode. When sinking current while in forced continuous operation, current will be forced back into the main power supply potentially boosting the input supply level.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>7.5%) as well as other more serious conditions that may overvoltage the output. In this case, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Power Good (PGOOD) Pin

The PGOOD pin is connected to an open drain of an internal MOSFET. The MOSFET turns on and pulls the pin down when the enabled channel's output is not within ±7.5% of the nominal output level as determined by the feedback resistor divider. When the enabled channel's output meets the ±7.5% requirement, the MOSFET is turned off within 10µs and the pin is allowed to be pulled up by an external resistor to source of up to 5.5V. If either channel 1 or channel 2 is shut down by driving its RUN pin low, PGOOD will ignore the state of that channel's ouput.

Foldback Current

Foldback current limiting is activated when the output voltage falls below 70% of its nominal level. If a short is present, a safe, low output current is provided due to internal current foldback and actual power wasted is low due to the efficient nature of the current mode switching regulator. This function is disabled at start-up.

OPERATION (Refer to Functional Diagram)

THEORY AND BENEFITS OF 2-PHASE OPERATION

The LTC3728 and the LTC3828 family of dual high efficiency DC/DC controllers brings the considerable benefits of 2-phase operation to portable applications for the first time. Notebook computers, PDAs, handheld terminals and automotive electronics will all benefit from the lower input filtering requirement, reduced electromagnetic interference (EMI) and increased efficiency associated with 2-phase operation.

Why the need for 2-phase operation? Up until the 2-phase family, constant-frequency dual switching regulators operated both channels in phase (i.e., single-phase operation). This means that both switches turned on at the same time, causing current pulses of up to twice the amplitude of those for one regulator to be drawn from the input capacitor and battery. These large amplitude current pulses increased the total RMS current flowing from the input capacitor, requiring the use of more expensive input capacitors and increasing both EMI and losses in the input capacitor and battery.

With 2-phase operation, the two channels of the dual-switching regulator are operated 180 degrees out of phase. This effectively interleaves the current pulses drawn by the switches, greatly reducing the overlap time where they add together. *The result is a significant reduction in total RMS input current, which in turn allows less expensive input capacitors to be used, reduces shielding requirements for EMI and improves real world operating efficiency.*

Figure 2 compares the input waveforms for a representative single-phase dual switching regulator to the LTC3828 2-phase dual switching regulator. An actual measurement of the RMS input current under these conditions shows that 2-phase operation dropped the input current from $2.6A_{RMS}$ to $1.9A_{RMS}$. While this is an impressive reduction in itself, remember that the power losses are proportional to I_{RMS}^2, meaning that the actual power wasted is reduced by a factor of 1.86. The reduced input ripple voltage also means less power is lost in the input power path, which could include batteries, switches, trace/connector resistances and protection circuitry. Improvements in both conducted and radiated EMI also directly accrue as a result of the reduced RMS input current and voltage.

Of course, the improvement afforded by 2-phase operation is a function of the dual switching regulator's relative duty cycles which, in turn, are dependent upon the input voltage V_{IN} (Duty Cycle = V_{OUT}/V_{IN}). Figure 3 shows how the RMS input current varies for single-phase and 2-phase operation for 3.3V and 5V regulators over a wide input voltage range.

It can readily be seen that the advantages of 2-phase operation are not just limited to a narrow operating range, but in fact extend over a wide region. A good rule of thumb for most applications is that 2-phase operation will reduce the input capacitor requirement to that for just one channel operating at maximum current and 50% duty cycle.

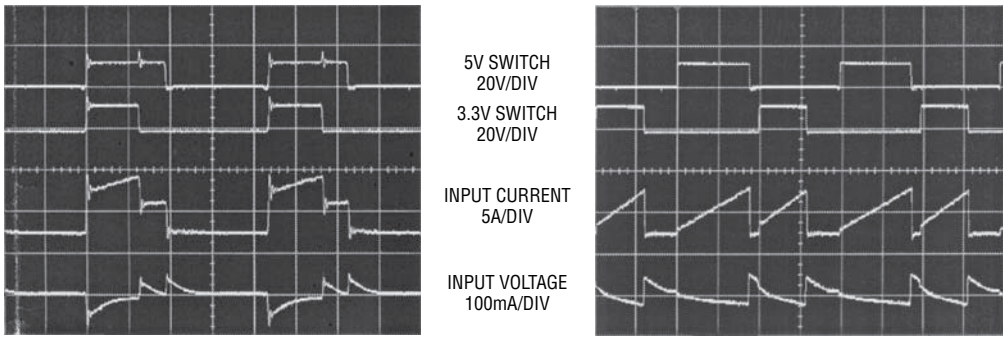


Figure 2. Input Waveforms Comparing Single-Phase (a) and 2-Phase (b) Operation for Dual Switching Regulators Converting 12V to 5V and 3.3V at 3A Each. The Reduced Input Ripple with the LTC3828 2-Phase Regulator Allows Less Expensive Input Capacitors, Reduces Shielding Requirements for EMI and Improves Efficiency

OPERATION (Refer to Functional Diagram)

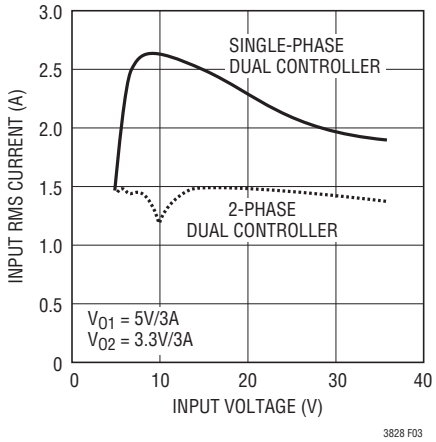


Figure 3. RMS Input Current Comparison

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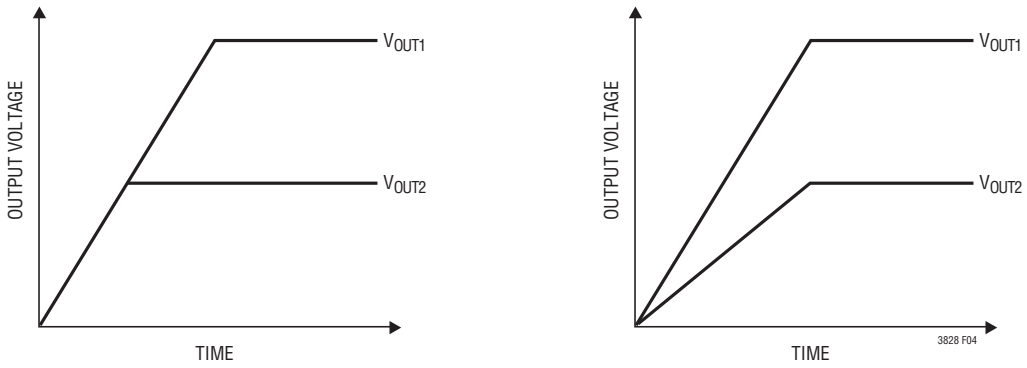
Output Voltage Tracking

The LTC3828 allows the user to program how the channel outputs ramp up by means of the TRCKSS pins. Through these pins, the channel outputs can be set up to either coincidentally or ratiometrically tracking, as shown in Figure 4.

The TRCKSS pins act as clamps on the channels' reference voltages. V_{OUT} is referenced to the TRCKSS voltage when the TRCKSS < 0.8V and to the internal precision reference when TRCKSS > 0.8V.

To implement the tracking in Figure 4a, connect an extra resistive divider to the output of the master channel and connect its midpoint to the slave channel's TRCKSS pin. The ratio of this divider should be selected the same as that of channel 2's feedback divider (Figure 5). **In this tracking mode, the master channel's output must be set higher than slave channel's output.** To implement the ratiometric tracking in Figure 4b, no extra divider is needed; simply connect one of TRCKSS pins to the other channel's V_{FB} pin (Figure 5).



(4a) Coincident Tracking

(4b) Ratiometric Tracking

Figure 4. Two Different Modes of Output Voltage Tracking

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By selecting different resistors, the LTC3828 can achieve different modes of tracking including the two in Figure 4. Figure 6 helps to explaining the tracking function. At the input stage of an error amplifier, two diodes are used to clamp the equivalent reference voltage and an additional diode is used to match the shifted common mode voltage. The top two current sources are of the same value. When the TRCKSS voltage is low, switch S1 is on and V_{OSENSE} follows the TRCKSS voltage. When the TRCKSS voltage is close to 0.8V, the reference voltage, switch S1, is off and V_{OSENSE} follows the reference voltage. The regulation for both channels' outputs are not affected by the tracking mode. In the ratiometric tracking mode, the two channels do not exhibit cross talk.

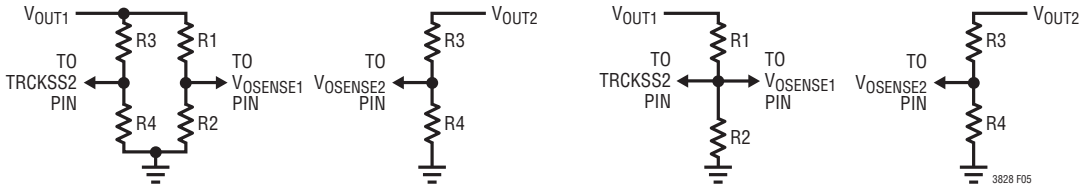
The number of resistors in Figure 5a can be further reduced with the scheme in Figure 7.

In a system that requires more than two tracked supplies, multiple LTC3828s can be daisy-chained through the TRCKSS1 pin. TRCKSS1 clamps channel 1's reference in the same manner TRCKSS2 clamps channel 2. To eliminate the possibility of multiple LTC3828s coming on at different times, only the master LTC3828's TRCKSS1 pin should be connected to a soft-start capacitor. Figure 8 shows the circuit with four outputs. Three of them are programmed in the coincident mode while the fourth one tracks ratiometrically. If output tracking is not needed, the TRCKSS pins are used as soft start-up pins. The capacitors connected to those pins set the soft-start ramping up speed.

Figure 15 is a basic LTC3828 application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value. Next, the power MOSFETs and D1 are selected. Finally, C_{IN} and C_{OUT} are selected. The circuit shown in Figure 15 is configured for operation up to an input voltage of 28V (limited by the external MOSFETs).

R_{SENSE} Selection For Output Current

R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold of 75mV/R_{SENSE} and an input common mode range of SGND



(5a) Coincident Tracking Setup

(5b) Ratiometric Tracking Setup

Figure 5. Setup for Coincident and Ratiometric Tracking

$$\left(\frac{R1}{R2}=\frac{V_{OUT1}}{0.8}-1,\frac{R3}{R4}=\frac{V_{OUT2}}{0.8}-1\right)T$$

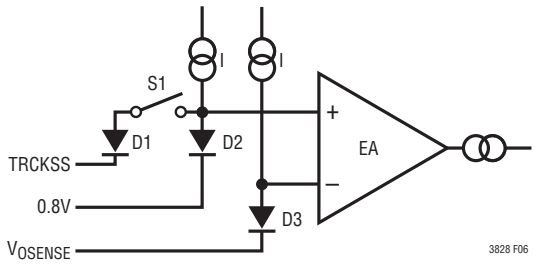


Figure 6. Equivalent Input Circuit of Error Amplifier of Channel 2

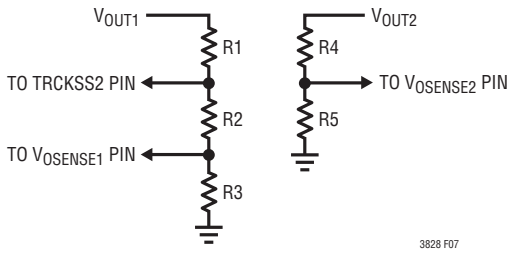
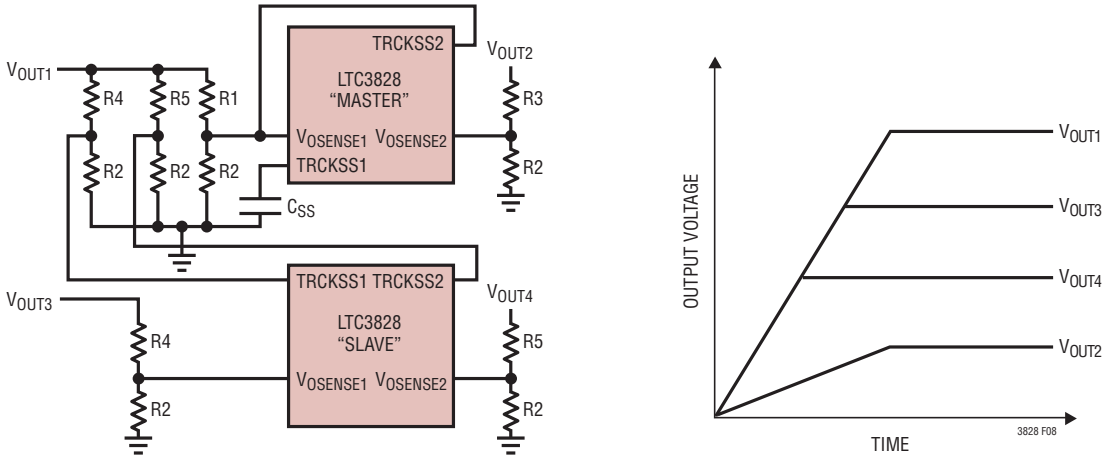


Figure 7. Alternative Setup for Coincident Tracking

$$\left(\frac{R1+R2}{R3}=\frac{V_{OUT1}}{0.8}-1,\frac{R1}{R2+R3}=\frac{R4}{R5}=\frac{V_{OUT2}}{0.8}-1\right)$$

APPLICATIONS INFORMATION



(8a) Circuit Setup **(8b) Output Voltage**

Figure 8. Four Outputs with Tracking and Ratiometric Sequencing

$$\left(\frac{R1}{R2}=\frac{V_{OUT1}}{0.8}-1,\frac{R3}{R2}=\frac{V_{OUT2}}{0.8}-1\frac{R4}{R2}=\frac{V_{OUT3}}{0.8}-1,\frac{R5}{R2}=\frac{V_{OUT4}}{0.8}-1\right)$$

to 1.1(INTV$_{CC}$). The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = \frac{50mV}{I_{MAX}}$$

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency

The IC uses a constant frequency phase-lockable architecture with the frequency determined by an internal capacitor. This capacitor is charged by a fixed current plus an additional current which is proportional to the voltage applied to the PLLFLTR pin. Refer to Phase-Locked Loop and Frequency Synchronization in the Applications Information section for additional information.

A graph for the voltage applied to the PLLFLTR pin vs frequency is given in Figure 9. As the operating frequency is increased the gate charge losses will be higher, reducing efficiency (see Efficiency Considerations). The maximum switching frequency is approximately 550kHz.

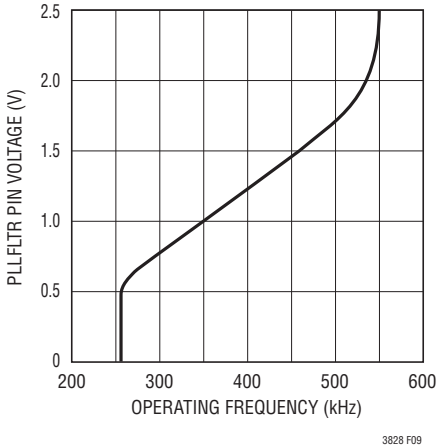


Figure 9. PLLFLTR Pin Voltage vs Frequency

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because

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of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 25% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Selection

Usually, high inductance is preferred for small current ripple and low core loss. Unfortunately, increased inductance requires more turns of wire or small air gap of the inductor, resulting in high copper loss or low saturation current. Once the value of L is known, the actual inductor must be selected. There are two popular types of core material of commercial available inductors.

Ferrite core inductors usually have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. However, ferrite core saturates "hard", which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. One advantage of the LTC3828 is its current mode control that detects and limits cycle-by-cycle peak inductor current. Therefore, accurate and fast protection is achieved if the inductor is saturated in steady state or during transient mode.

Powder iron inductors usually saturate "soft", which means the inductance drops in a linear fashion when the current increases. However, the core loss of the powder iron inductor is usually higher than the ferrite inductor. So design with high switching frequency should pay attention to the inductor core loss too.

Inductor manufacturers usually provide inductance, DCR, (peak) saturation current and (DC) heating current ratings in the inductor data sheet. A good supply design should not exceed the saturation and heating current rating of the inductor.

Power MOSFET and D1 Selection

Two external power MOSFETs must be selected for each controller in the LTC3828: One N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up. Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected ($V_{IN} < 5V$); then, sub-logic level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the Gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

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$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC} - V_{THMIN}} + \frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For $V_{IN} < 12V$ the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} \geq 12V$ the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short circuit when the synchronous switch is on close to 100% of the period.

The term $(1 + \delta)$ is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but $\delta = 0.005/°C$ can be used as an approximation for low voltage MOSFETs.

The Schottky diode D1 shown in Figure 1 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the multiphase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS current requirement. Increasing the output current, drawn from the other out-of-phase controller, will actually decrease the input RMS ripple current from this maximum value (see Figure 3). The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

The type of input capacitor, value and ESR rating have efficiency effects that need to be considered in the selection process. The capacitance value chosen should be sufficient to store adequate charge to keep high peak battery currents down. 20µF to 40µF is usually sufficient for a 25W output supply operating at 260kHz. The ESR of the capacitor is important for capacitor power dissipation as well as overall battery efficiency. All of the power (RMS ripple current • ESR) not only heats up the capacitor but wastes power from the battery.

Medium voltage (20V to 35V) ceramic, tantalum, OS-CON and switcher-rated electrolytic capacitors can be used as input capacitors, but each has drawbacks: ceramic voltage coefficients are very high and may have audible piezoelectric effects; tantalums need to be surge rated; OS-CONs suffer from higher inductance, larger case size and limited surface-mount applicability; electrolytics' higher ESR and dryout possibility require several to be used. Multiphase systems allow the lowest amount of capacitance overall. As little as one 22µF or two to three 10µF ceramic capacitors are an ideal choice in a 20W to 35W power supply due to their extremely low ESR. Even though the capacitance at 20V is substantially below their rating at zero bias, very low ESR loss makes ceramics

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an ideal candidate for highest efficiency battery operated systems. Also consider parallel ceramic and high quality electrolytic capacitors as an effective means of achieving ESR and bulk capacitance goals.

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\,\text{Required}\,I_{RMS} \approx I_{MAX}\frac{\left[V_{OUT}\left(V_{IN}-V_{OUT}\right)\right]^{1/2}}{V_{IN}}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the manufacturer if there is any question.

The benefit of the LTC3828 multiphase clocking can be calculated by using the equation above for the higher power controller and then calculating the loss that would have resulted if both controller channels switched on at the same time. The total RMS power lost is lower when both controllers are operating due to the interleaving of current pulses through the input capacitor's ESR. This is why the input capacitor's requirement calculated above for the worst-case controller is adequate for the dual controller design. Remember that input protection fuse resistance, battery resistance and PC board trace resistance losses are also reduced due to the reduced peak currents in a multiphase system. *The overall benefit of a multiphase design will only be fully realized when the source impedance of the power supply/battery is included in the efficiency testing.* The drains of the two top MOSFETS should be placed within 1cm of each other and share a common C_{IN}(s). Separating the drains and C_{IN} may produce undesirable voltage and current resonances at V_{IN}.

The selection of C_{OUT} is driven by the required output voltage ripple and load transient response. Both the capacitor effective series resistance (ESR) and capacitance determine the output ripple:

$$\Delta V_{OUT} \approx \Delta I_L \bullet \left(ESR + \frac{1}{8fC_{OUT}}\right)$$

where f = operating frequency, C_{OUT} = output capacitance and ΔI_L = ripple current in the inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage.

Usually, ceramic capacitors are used to minimize the output voltage ripple because of their ultralow ESR. Currently, multilayer ceramic capacitors have capacitor values up to hundreds of µF. However, the capacitance of the ceramic capacitors usually decreases with increased DC bias voltage and ambient temperature. In general, X5R or X7R type capacitors are recommended for high performance solutions. The OPTI-LOOP current mode control of LTC3828 provides stable, high performance transient response even with all ceramic output capacitors. Manufactures such as TDK, Taiyo Yuden, Murata and AVX provide high performance ceramic capacitors.

When high capacitance is needed, especially for load transient requirement, low ESR polymerized electrolytic capacitors such as Sanyo POSCAP or Panasonic SP capacitor can be used in parallel with ceramic capacitors. Other high performance electolytic capacitor manufacturers include AVX, KEMET and NEC. With LTC3828, a combination of ceramic and low ESR electrolytic capacitors can provide a low ripple, fast transient, high density and cost-effective solution. Consult manufacturers for specific recommendations.

$INTV_{CC}$ Regulator

An internal P-channel low dropout regulator produces 5V at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the drivers and internal circuitry within the IC. The $INTV_{CC}$ pin regulator can supply a peak current of 50mA and must be bypassed to ground with a minimum of 4.7µF tantalum, 10µF special polymer, or low ESR type electrolytic capacitor. A 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND IC pins is highly recommended. Good

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bypassing is necessary to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between channels.

Higher input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the IC to be exceeded. The system supply current is normally dominated by the gate charge current. Additional external loading of the $INTV_{CC}$ also needs to be taken into account for the power dissipation calculations.

The absolute maximum rating for the $INTV_{CC}$ Pin is 50mA. To prevent maximum junction temperature from being exceeded, the input supply current must be checked operating in continuous mode at maximum V_{IN}.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors, C_B, connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor, C_B, needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate-drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Output Voltage

The output voltages are each set by an external feedback resistive divider carefully placed across the output capacitor. The resultant feedback signal is compared with the internal precision 0.800V voltage reference by the error amplifier. The output voltage is given by the equation:

$$V_{OUT} = 0.8V\left(1+\frac{R2}{R1}\right)$$

where R1 and R2 are defined in Figure 1.

SENSE+/SENSE– Pins

The common mode input range of the current comparator sense pins is from 0V to (1.1)$INTV_{CC}$. Continuous linear operation is guaranteed throughout this range allowing output voltage setting from 0.8V to 7.7V. A differential NPN input stage is biased with internal resistors from an internal 2.4V source as shown in the Functional Diagram. This requires that current either be sourced or sunk from the SENSE pins depending on the output voltage. If the output voltage is below 2.4V current will flow out of both SENSE pins to the main output. The output can be easily preloaded by the V_{OUT} resistive divider to compensate for the current comparator's negative input bias current. The maximum current flowing out of each pair of SENSE pins is:

$$I_{SENSE}^{+} + I_{SENSE}^{-} = (2.4V - V_{OUT})/24k$$

Since V_{OSENSE} is servoed to the 0.8V reference voltage, we can choose R1 in Figure 1 to have a maximum value to absorb this current.

$$R1_{(MAX)} = 24k\left(\frac{0.8V}{2.4V - V_{OUT}}\right)$$

for $V_{OUT} < 2.4V$

Regulating an output voltage of 1.8V, the maximum value of R1 should be 32k. Note that for an output voltage above 2.4V, R1 has no maximum value necessary to absorb the sense currents; however, R1 is still bounded by the V_{OSENSE} feedback current.

RUN and Soft-Start

The LTC3828 RUN pins shut down their respective channels independently. The LTC3828 is put in a low quiescent current state (I_Q < 30µA) if both RUN pin voltages are below 1V. TRCKSS pins are actively pulled to ground in this shutdown state. Once the RUN pin voltages are above 1.5V, the respective channel of the LTC3828 is powered

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up. The LTC3828 has the ability to either soft-start by itself with an external soft-start capacitor or tracking the output of the other channel or supply. When the device is configured to soft-start by itself, an external soft-start capacitor should be connected to the TRCKSS pin. A soft-start current of 1.2µA is to charge the soft-start capacitor C_{SS}. Note that soft-start during this mode is achieved not by limiting the maximum output current of the controller but by controlling the ramp rate of the output voltage. As a matter of fact, current foldback is defeated during soft-start or tracking. During this phase, the LTC3828 is basically ramping the reference voltage until this voltage is 7.5% below the 0.8V reference. The total soft-start time can be estimated as:

$$t_{SOFT\text{-}START} = 0.925 \bullet 0.8V \bullet C_{SS}/1.2\mu A$$

The LTC3828 is designed such that the TRCKSS pin is not actively pulled down if only one of the channels is shut down. In this case, the TRCKSS pin voltage could be higher than 0.8V. If this particular channel is powered up again, the soft-start for this particular channel is provided by an internal soft-start timer about 450µs. The internal soft-start timer will also be in effect if the LTC3828 is trying to track an output supply that is already powered up.

In any case, the force continuous mode is disabled and PGOOD signal is forced low during the first 90% of the soft-start phase. This time can be estimated for external soft-start as:

$$t_{FORCE} = 0.9 \bullet 0.925 \bullet 0.8V \bullet C_{SS}/1.2\mu A$$

For internal soft-start, it will be 450µs.

Fault Conditions: Current Limit and Current Foldback

The current comparators have a maximum sense voltage of 75mV resulting in a maximum MOSFET current of $75mV/R_{SENSE}$. The maximum value of current limit generally occurs with the largest V_{IN} at the highest ambient temperature, conditions that cause the highest power dissipation in the top MOSFET.

Each controller includes current foldback to help further limit load current when the output is shorted to ground. If the output falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 75mV to 25mV. Under short-circuit conditions with very low duty cycles, the controller will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time, $t_{ON(MIN)}$, of each controller (typically 200ns), the input voltage and inductor value:

$$\Delta I_{L(SC)} = t_{ON(MIN)} (V_{IN}/L)$$

The resulting short-circuit current is:

$$I_{SC} = \frac{25mV}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 7.5% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The output of this comparator is only latched by the overvoltage condition itself and will therefore allow a switching regulator system having a poor PC layout to function while the design is being debugged. The bottom MOSFET remains on continuously for as long as the OV condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes. A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

Phase-Locked Loop and Frequency Synchronization

The IC has a phase-locked loop comprised of an internal voltage controlled oscillator and phase detector. This allows the top MOSFET turn-on to be locked to the rising edge of an external source. The frequency range of the voltage controlled oscillator is ±50% around the center

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frequency f_O. A voltage applied to the PLLFLTR pin of 1.2V corresponds to a frequency of approximately 400kHz. The nominal operating frequency range of the IC is 260kHz to 550kHz.

The phase detector used is an edge sensitive digital type which provides zero degrees phase shift between the external and internal oscillators. This type of phase detector will not lock up on input frequencies close to the harmonics of the VCO center frequency. The PLL hold-in range, Δf_H, is equal to the capture range, Δf_C:

$\Delta f_H = \Delta f_C = \pm 0.5\ f_O$ (260kHz-550kHz)

The output of the phase detector is a complementary pair of current sources charging or discharging the external filter network on the PLLFLTR pin.

If the external frequency, f_{PLLIN}, is greater than the oscillator frequency, f_{OSC}, current is sourced continuously, pulling up the PLLFLTR pin. When the external frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLFLTR pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. Thus the voltage on the PLLFLTR pin is adjusted until the phase and frequency of the external and internal oscillators are identical. At this stable operating point the phase comparator output is open and the filter capacitor C_{LP} holds the voltage. The IC's FCB/PLLIN pin must be driven from a low impedance source such as a logic gate located close to the pin. When using multiple ICs for a phase-locked system, the PLLFLTR pin of the master oscillator should be biased at a voltage that will guarantee the slave oscillator(s) ability to lock onto the master's frequency. A DC voltage of 0.7V to 1.7V applied to the master oscillator's PLLFLTR pin is recommended in order to meet this requirement. The resultant operating frequency can range from 300kHz to 500kHz.

The loop filter components (C_{LP}, R_{LP}) smooth out the current pulses from the phase detector and provide a stable input to the voltage controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} =10k and C_{LP} is 0.01µF to 0.1µF.

Minimum On-Time Considerations

Minimum on-time, $t_{ON(MIN)}$, is the smallest time duration that each controller is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for each controller is approximately 120ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 300ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

Voltage Positioning

Voltage positioning can be used to minimize peak-to-peak output voltage excursions under worst-case transient loading conditions. The open-loop DC gain of the control loop is reduced depending upon the maximum load step specifications. Voltage positioning can easily be added to either or both controllers by loading the I_{TH} pin with a resistive divider having a Thevenin equivalent voltage source equal to the midpoint operating voltage range of the error amplifier, or 1.2V (see Figure 10).

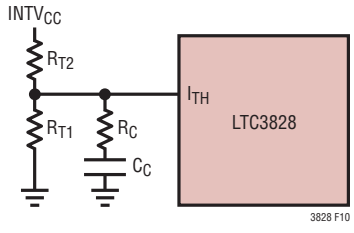

Figure 10. Active Voltage Positioning Applied to the LTC3828

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The resistive load reduces the DC loop gain while maintaining the linear control range of the error amplifier. The maximum output voltage deviation can theoretically be reduced to half or alternatively the amount of output capacitance can be reduced for a particular application. A complete explanation is included in Design Solutions 10. (See www.linear.com)

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

$$\%\text{Efficiency} = 100\% - (L1 + L2 + L3 + ...)$$

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3828 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (V_{IN})^2 \bullet \left(\frac{I_{MAX}}{2}\right)(R_{DR}) \bullet (C_{MILLER})(f)\left(\frac{1}{5V - V_{TH}} + \frac{1}{V_{TH}}\right)$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. The LTC3828 2-phase architecture typically halves this input capacitance requirement over competing solutions. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

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Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in the Figure 15 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

Automotive and Low V_{IN} Considerations

As battery-powered devices go mobile, there is a natural interest in plugging into the cigarette lighter in order to conserve or even recharge battery packs during operation. But before you connect, be advised: you are plugging into the supply from hell. The main power line in an automobile is the source of a number of nasty potential transients, including load-dump, reverse-battery and double-battery.

Load-dump is the result of a loose battery cable. When the cable breaks connection, the field collapse in the alternator can cause a positive spike as high as 60V which takes several hundred milliseconds to decay. Reverse-battery is just what it says, while double-battery is a consequence of tow-truck operators finding that a 24V jump start cranks cold engines faster than 12V.

The network shown in Figure 11a is the most straightforward approach to protect a DC/DC converter from the ravages of an automotive power line. The series diode prevents current from flowing during reverse-battery, while the transient suppressor clamps the input voltage

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during load-dump. Note that the transient suppressor should not conduct during double-battery operation, but must still clamp the input voltage below breakdown of the converter. Although the LTC3828 have a maximum input voltage of 30V, most applications will also be limited to 30V by the MOSFET BVD_{SS}.

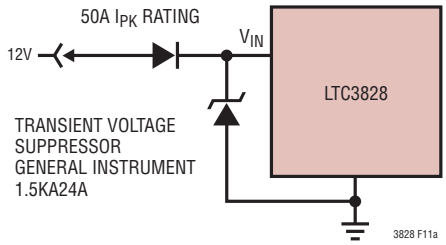

Figure 11a. Automotive Application Protection

For applications where the main input power is 5V, tie the V_{IN}, $INTV_{CC}$ and DRV_{CC} pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 11b to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ regulator and will prevent $INTV_{CC}$ from dropping too low due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic-level devices.

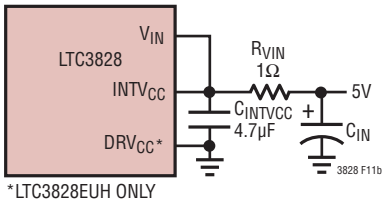

Figure 11b. Setup for a 5V Input

Design Example

As a design example for one channel, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 1.8V, I_{MAX} = 5A and f = 300kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the PLLFLTR pin to a resistive divider from the $INTV_{CC}$ pin, generating 0.7V for 300kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 23% ripple current and a 3.3µH will result in 33%. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.84A, for the 3.3µH value. Increasing the ripple current will also help ensure that the minimum on-time of 100ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(300kHz)} = 273ns$$

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{60mV}{5.84A} \approx 0.01\Omega$$

Since the output voltage is below 2.4V the output resistive divider will need to be sized to not only set the output voltage but also to absorb the SENSE pin's specified input current.

$$R1_{(MAX)} = 24k\left(\frac{0.8V}{2.4V - V_{OUT}}\right)$$

$$= 24k\left(\frac{0.8V}{2.4V - 1.8V}\right) = 32k$$

Choosing 1% resistors: R1 = 25.5k and R2 = 32.4k yields an output voltage of 1.816V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

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$$P_{MAIN} = \frac{1.8V}{22V}(5)^2[1+(0.005)(50°C-25°C)]\bullet$$
$$(0.035\Omega)+(22V)^2\left(\frac{5A}{2}\right)(4\Omega)(215pF)\bullet$$
$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](300kHz)=332mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC}=\frac{25mV}{0.01\Omega}-\frac{1}{2}\left(\frac{120ns(22V)}{3.3\mu H}\right)=2.1A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(20) = 0.1. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC}=\frac{22V-1.8V}{22V}(2.1A)^2(1.125)(0.022\Omega)$$
$$=100mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.67A) = 33mV_{P-P}$$

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 12. The Figure 13 illustrates the current waveforms present in the various branches of the 2-phase synchronous regulators operating in the continuous mode. Check the following in your layout:

1. Are the top N-channel MOSFETs M1 and M3 located within 1cm of each other with a common drain connection at CIN? Do not attempt to split the input decoupling for the two channels as it can cause a large resonant loop.

2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.

3. Do the LTC3828 V_{OSENSE} pins' resistive dividers connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The R2 and R4 connections should not be along the high current input feeds from the input capacitor(s).

4. Are the $SENSE^-$ and $SENSE^+$ leads routed together with minimum PC trace spacing? The filter capacitor between $SENSE^+$ and $SENSE^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.

5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.

6. Keep the switching nodes (SW1, SW2), top gate nodes (TG1, TG2), and boost nodes (BOOST1, BOOST2) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3828 and occupy minimum PC trace area.

7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.