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Low I_Q Synchronous Step-Down Controller

FEATURES

- **Wide Output Voltage Range: 0.8V ≤ V_{OUT} ≤ 10V**
- **Low Operating I_Q: 80µA**
- **OPTI-LOOP® Compensation Minimizes C_{OUT}**
- **±1% Output Voltage Accuracy**
- **Wide V_{IN} Range: 4V to 36V Operation**
- **Phase-Lockable Fixed Frequency 140kHz to 650kHz**
- Dual N-Channel MOSFET Synchronous Drive
- Very Low Dropout Operation: 99% Duty Cycle
- Adjustable Output Voltage Soft-Start or Tracking
- Output Current Foldback Limiting
- Output Overvoltage Protection
- Low Shutdown I_Q: 10µA
- Selectable Continuous, Pulse-Skipping or Burst Mode® Operation at Light Loads
- Small 16-Lead Narrow SSOP or 3mm × 5mm DFN Package

APPLICATIONS

- Automotive Systems
- Telecom Systems
- Battery-Operated Digital Devices
- Distributed DC Power Systems

DESCRIPTION

The LTC®3835-1 is a high performance step-down switching regulator controller that drives an all N-channel synchronous power MOSFET stage. A constant-frequency current mode architecture allows a phase-lockable frequency of up to 650kHz.

The 80µA no-load quiescent current extends operating life in battery powered systems. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. The LTC3835-1 features a precision 0.8V reference and a power good output indicator. The 4V to 36V input supply range encompasses a wide range of battery chemistries.

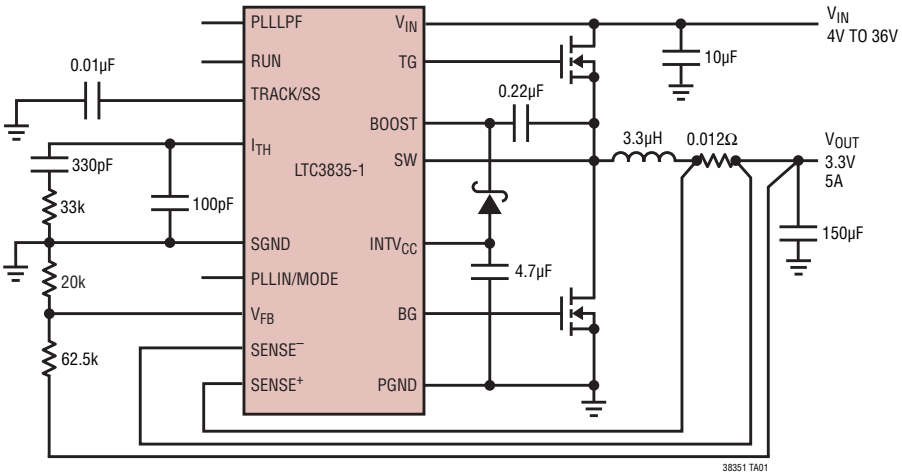
The TRACK/SS pin ramps the output voltage during start-up. Current foldback limits MOSFET heat dissipation during short-circuit conditions.

Comparison of LTC3835 and LTC3835-1

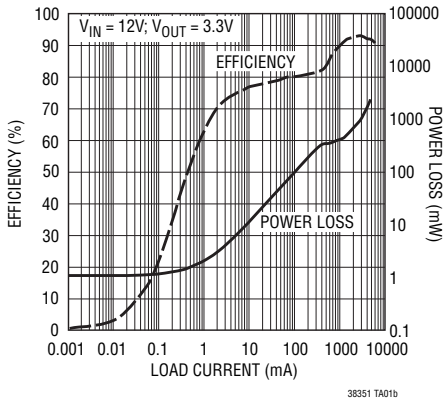
PART #	CLKOUT/ PHASMD	$EXTV_{CC}$	PGOOD	PACKAGES
LTC3835	YES	YES	YES	FE20/4 × 5 QFN
LTC3835-1	NO	NO	NO	GN16/3 × 5 DFN

TYPICAL APPLICATION

High Efficiency Step-Down Converter



Efficiency and Power Loss vs Load Current

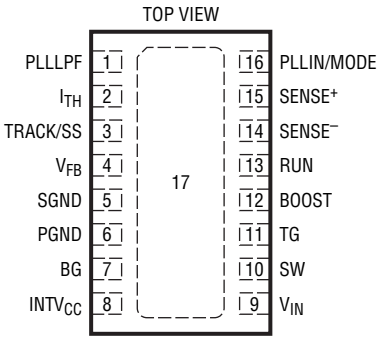


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 36V to –0.3V
Top Side Driver Voltage (BOOST)..... 42V to –0.3V
Switch Voltage (SW) ..... 36V to –5V
$INTV_{CC}$, (BOOST-SW) ..... 8.5V to –0.3V
RUN, TRACK/SS ..... 7V to –0.3V
$SENSE^+$, $SENSE^-$ Voltages ..... 11V to –0.3V
PLLIN/MODE, PLLLPF .....INTVCC to –0.3V
I_{TH}, V_{FB} Voltages ..... 2.7V to –0.3V
Peak Output Current <10µs (TG, BG) 3A

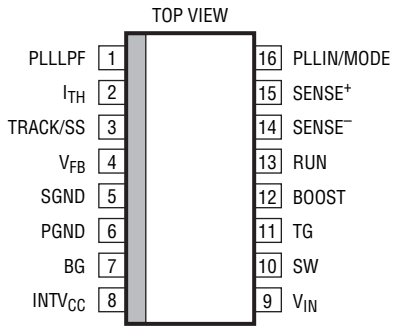
$INTV_{CC}$ Peak Output Current 50mA
Operating Temperature Range (Note 2).... –40°C to 85°C
Junction Temperature (Note 3) ..... 125°C
Storage Temperature Range
GN Package ..... –65°C to 150°C
Storage Temperature Range
DHC Package ..... –65°C to 125°C
Lead Temperature (GN Package, Soldering, 10 sec).... 300°C

PIN CONFIGURATION



DHC PACKAGE
16-Pin (5mm × 3mm) PLASTIC DFN

T_{JMAX} = 125°C, θ_{JA} = 43.5°C/W
EXPOSED PAD (PIN 17) IS SGND
MUST BE SOLDERED TO PCB



GN PACKAGE
16-LEAD PLASTIC SSOP

T_{JMAX} = 150°C, θ_{JA} = 90°C/W

ORDER INFORMATION (Note 2)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3835EDHC-1#PBF	LTC3835EDHC-1#TRPBF	38351	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3835IDHC-1#PBF	LTC3835IDHC-1#TRPBF	38351	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3835EGN-1#PBF	LTC3835EGN-1#TRPBF	38351	16-Lead Plastic SSOP	–40°C to 85°C
LTC3835IGN-1#PBF	LTC3835IGN-1#TRPBF	38351	16-Lead Plastic SSOP	–40°C to 85°C
LEAD BASED FINISH	**TAPE AND REEL**	**PART MARKING***	**PACKAGE DESCRIPTION**	**TEMPERATURE RANGE**
LTC3835EDHC-1	LTC3835EDHC-1#TR	38351	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3835IDHC-1	LTC3835IDHC-1#TR	38351	16-Lead (5mm × 3mm) Plastic DFN	–40°C to 85°C
LTC3835EGN-1	LTC3835EGN-1#TR	38351	16-Lead Plastic SSOP	–40°C to 85°C
LTC3835IGN-1	LTC3835IGN-1#TR	38351	16-Lead Plastic SSOP	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 12V, V_{RUN} = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loop							
V_{FB}	Regulated Feedback Voltage	(Note 4); I_{TH} Voltage = 1.2V	●	0.792	0.800	0.808	V
I_{VFB}	Feedback Current	(Note 4)			–5	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4V to 30V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 2V	 ● ●		 0.1 –0.1	 0.5 –0.5	 % %
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V; Sink/Source 5µA (Note 4)			1.55		mmho
I_Q	Input DC Supply Current Sleep Mode Shutdown	(Note 5) RUN = 5V, V_{FB} = 0.83V (No Load) V_{RUN} = 0V			 80 10	 125 20	 µA µA
UVLO	Undervoltage Lockout	V_{IN} Ramping Down	●		3.5	4	V
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB} Relative to Regulated V_{FB}		8	10	12	%
I_{SENSE}	Sense Pins Total Source Current	V_{SENSE}^- = V_{SENSE}^+ = 0V			–660		µA
DF_{MAX}	Maximum Duty Factor	In Dropout		98	99.4		%
$I_{TRACK/SS}$	Soft-Start Charge Current	V_{TRACK} = 0V		0.75	1.0	1.35	µA
V_{RUN} ON	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising		0.5	0.7	0.9	V
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	V_{FB} = 0.7V, V_{SENSE}^- = 3.3V V_{FB} = 0.7V, V_{SENSE}^- = 3.3V	 ●	90 80	100 100	110 115	mV mV
 TG1, 2 t_r TG1, 2 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 50 50	 90 90	 ns ns
 BG1, 2 t_r BG1, 2 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 40 40	 90 80	 ns ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF			70		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF			70		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			180		ns
$INTV_{CC}$ Linear Regulator							
$V_{INTVCCVIN}$	Internal V_{CC} Voltage	8.5V < V_{IN} < 30V		5.0	5.25	5.5	V
V_{LDOVIN}	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.2	1.0	%
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{PLLLPF} = No Connect		360	400	440	kHz
f_{LOW}	Lowest Frequency	V_{PLLLPF} = 0V		220	250	280	kHz
f_{HIGH}	Highest Frequency	V_{PLLLPF} = $INTV_{CC}$		475	530	580	kHz
$f_{SYNCMIN}$	Minimum Synchronizable Frequency	PLLIN/MODE = External Clock; V_{PLLLPF} = 0V			115	140	kHz
$f_{SYNCMAX}$	Maximum Synchronizable Frequency	PLLIN/MODE = External Clock; V_{PLLLPF} = 2V		650	800		kHz
I_{PLLLPF}	Phase Detector Output Current Sinking Capability Sourcing Capability	 $f_{PLLIN/MODE} < f_{OSC}$ $f_{PLLIN/MODE} > f_{OSC}$			 –5 5		 µA µA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3835E-1 is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3835I-1 is guaranteed to meet performance specificatons over the full –40°C to 85°C operating temperature range.

ELECTRICAL CHARACTERISTICS

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3835GN-1: $T_J = T_A + (P_D \bullet 90°C/W)$
LTC3835EDHC-1: $T_J = T_A + (P_D \bullet 43.5°C/W)$

Note 4: The LTC3835-1 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

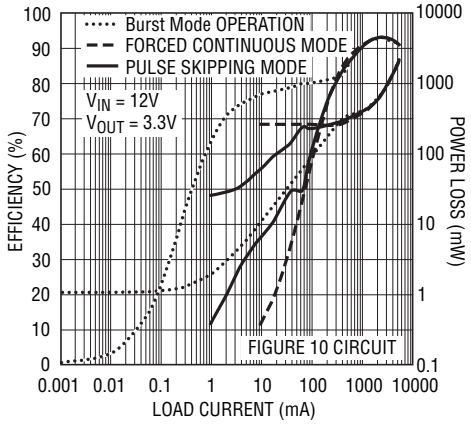
Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

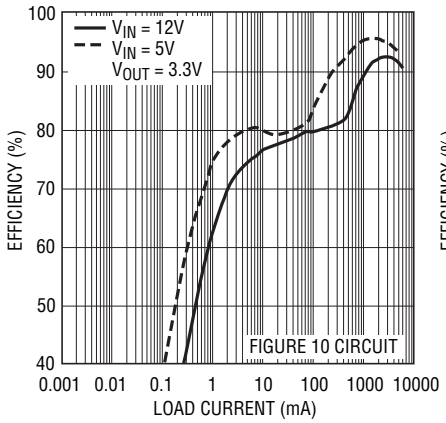
Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

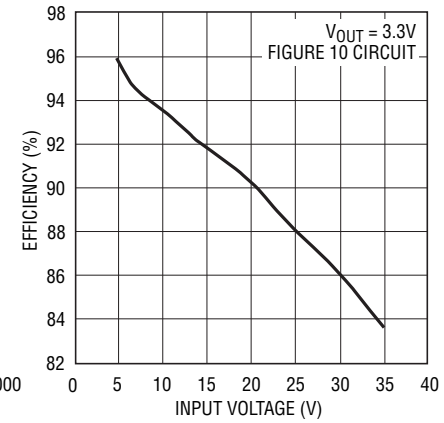
Efficiency and Power Loss vs Output Current



Efficiency vs Load Current



Efficiency vs Input Voltage



Load Step (Burst Mode Operation)

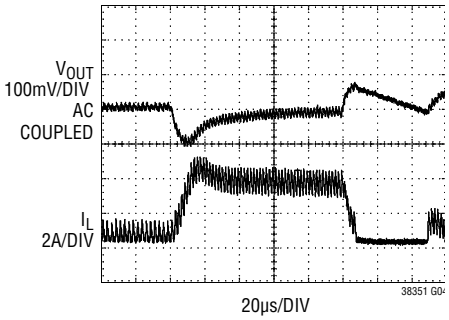


FIGURE 10 CIRCUIT
V_{OUT} = 3.3V

Load Step (Forced Continuous Mode)

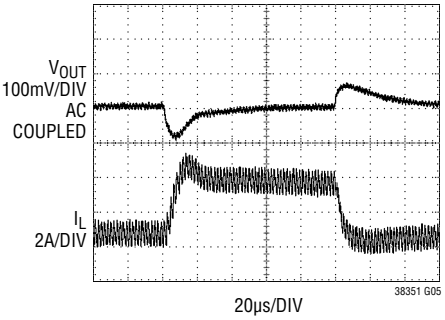


FIGURE 10 CIRCUIT
V_{OUT} = 3.3V

Load Step (Pulse-Skipping Mode)

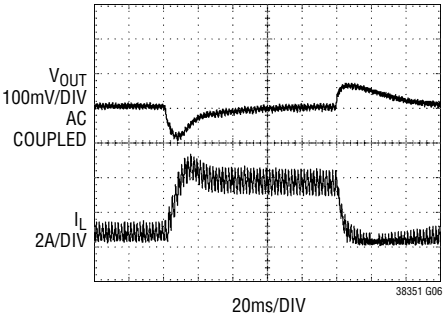


FIGURE 10 CIRCUIT
V_{OUT} = 3.3V

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Inductor Current at Light Load

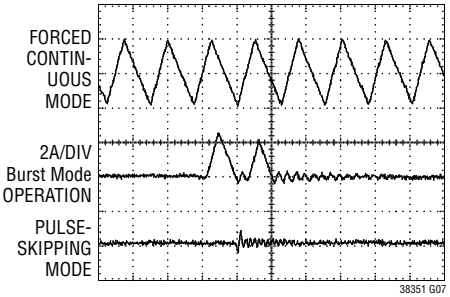


FIGURE 10 CIRCUIT
V_{OUT} = 3.3V
I_{LOAD} = 300µA

Soft Start-Up

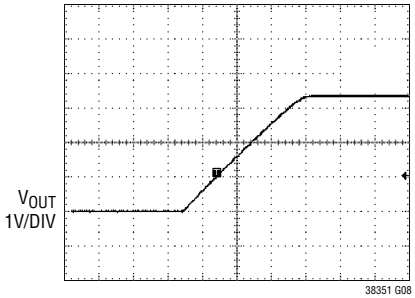


FIGURE 10 CIRCUIT

Tracking Start-Up

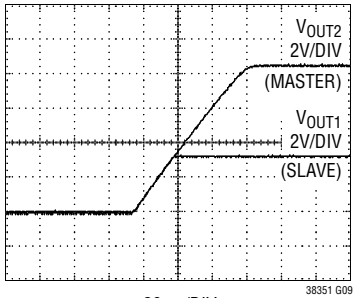
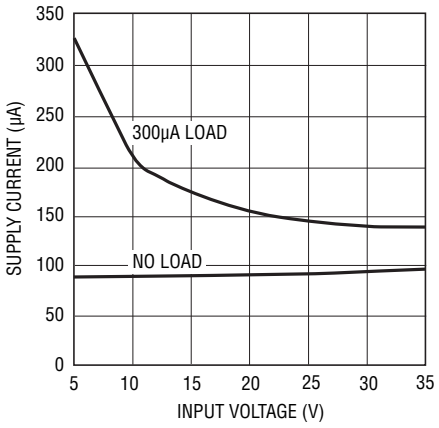
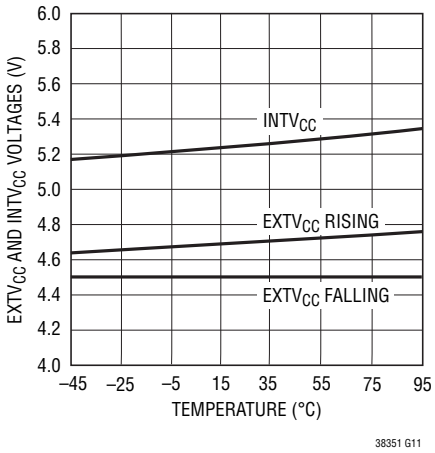


FIGURE 10 CIRCUIT

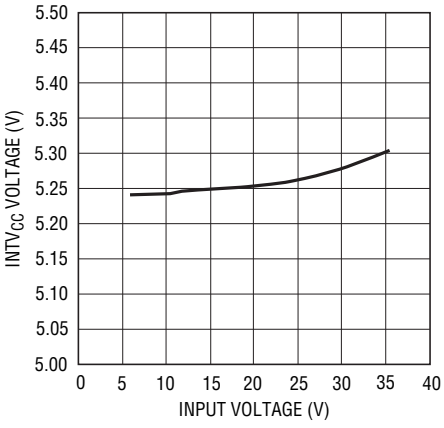
Total Input Supply Current vs Input Voltage



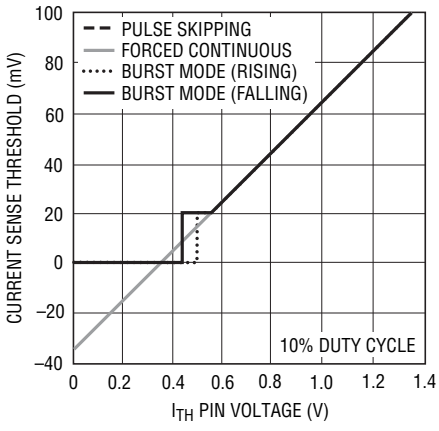
$EXTV_{CC}$ Switchover and $INTV_{CC}$ Voltages vs Temperature



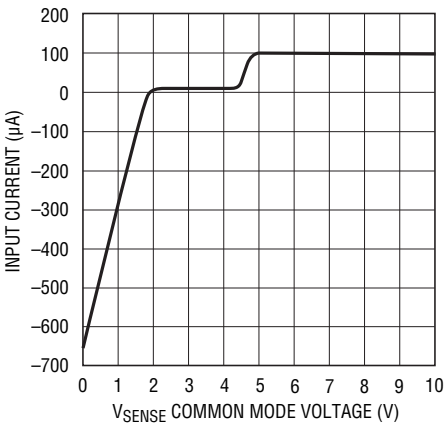
$INTV_{CC}$ Line Regulation



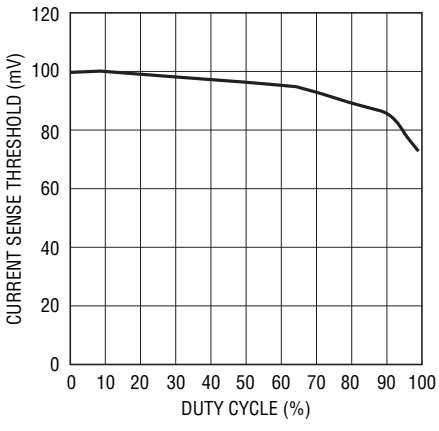
Maximum Current Sense Voltage vs I_{TH} Voltage



Sense Pins Total Input Bias Current

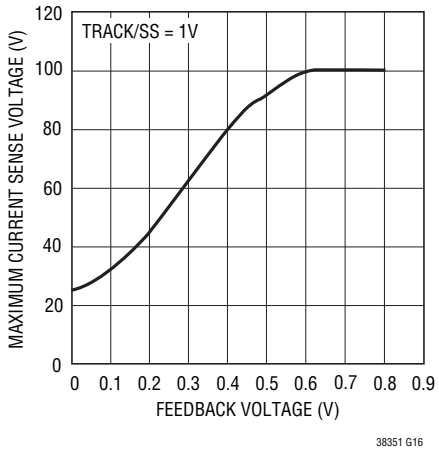


Maximum Current Sense Threshold vs Duty Cycle



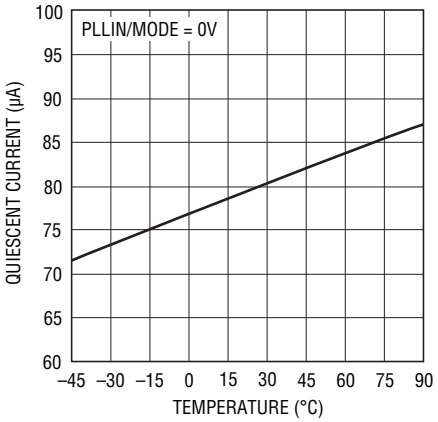
TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

Foldback Current Limit



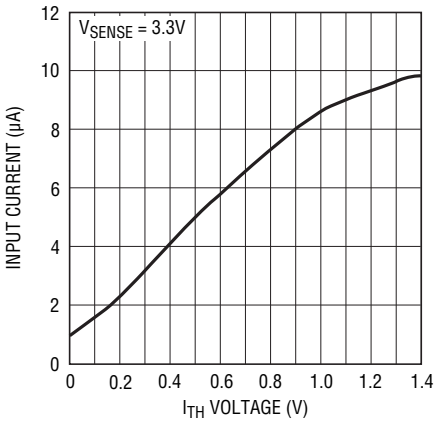
38351 G16

Quiescent Current vs Temperature



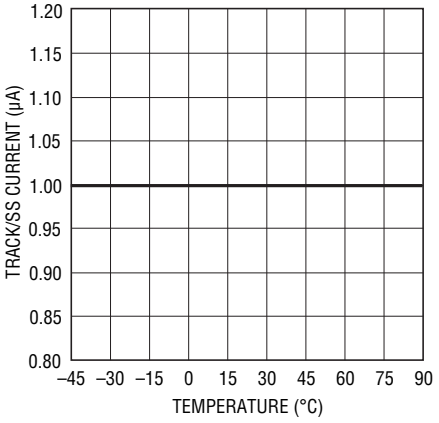
38351 G17

SENSE Pins Total Input Bias Current vs I_{TH}



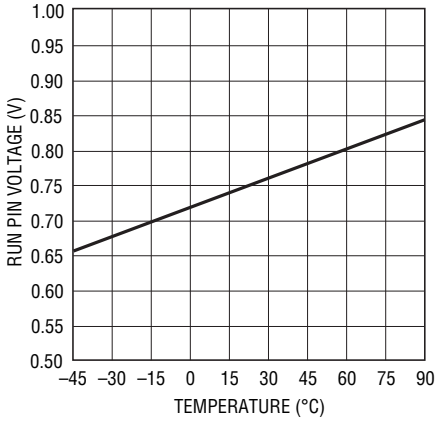
38351 G18

TRACK/SS Pull-Up Current vs Temperature



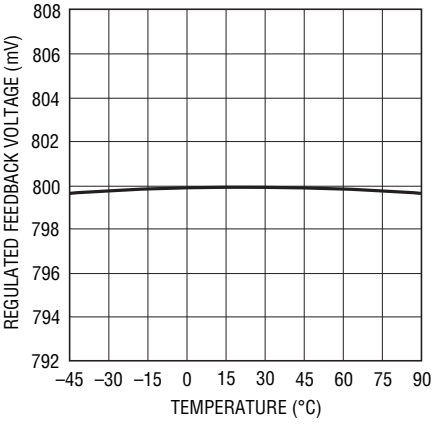
38351 G19

Shutdown (RUN) Threshold vs Temperature



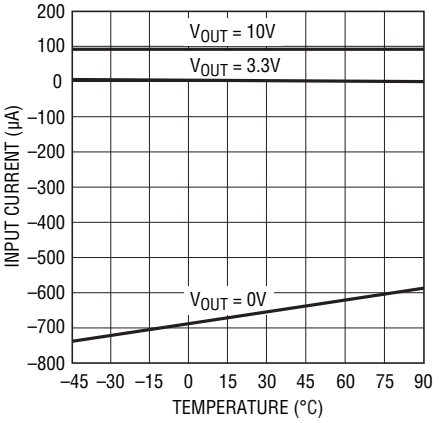
38351 G20

Regulated Feedback Voltage vs Temperature



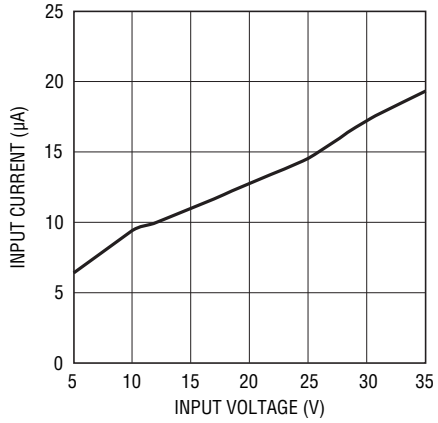
38351 G21

SENSE Pins Total Input Current vs Temperature



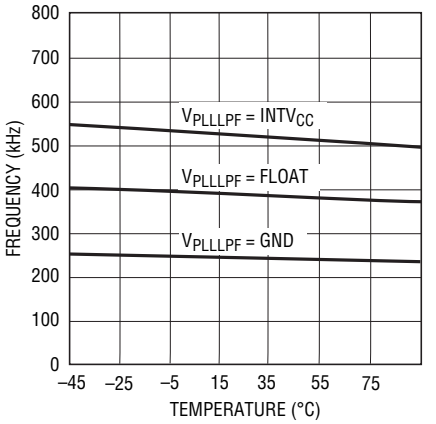
38351 G22

Shutdown Current vs Input Voltage



38351 G23

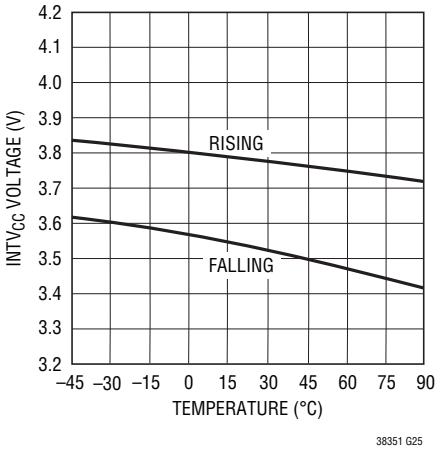
Oscillator Frequency vs Temperature



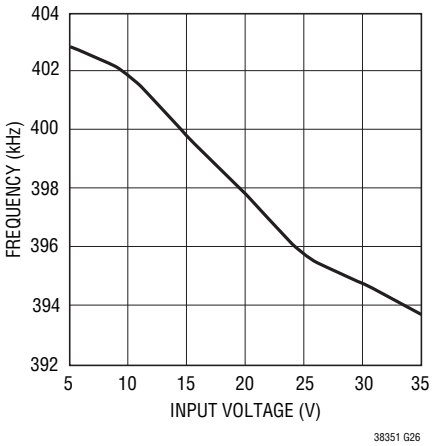
38351 G24

TYPICAL PERFORMANCE CHARACTERISTICS T_A = 25°C, unless otherwise noted.

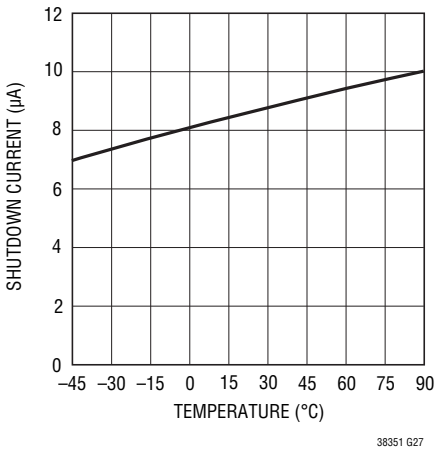
Undervoltage Lockout Threshold vs Temperature



Oscillator Frequency vs Input Voltage



Shutdown Current vs Temperature



PIN FUNCTIONS (DHC Package/GN Package)

PLLLPF (Pin 1/Pin 1): The phase-locked loop's lowpass filter is tied to this pin when synchronizing to an external clock. Alternatively, tie this pin to GND, $INTV_{CC}$ or leave floating to select 250kHz, 530kHz or 400kHz switching frequency.

I_{TH} (Pin 2/Pin 2): Error Amplifier Outputs and Switching Regulator Compensation Points. The current comparator trip point increases with this control voltage.

TRACK/SS (Pin 3/Pin 3): External Tracking and Soft-Start Input. The LTC3835-1 regulates the V_{FB} voltage to the smaller of 0.8V or the voltage on the TRACK/SS pin. A internal 1µA pull-up current source is connected to this pin. A capacitor to ground at this pin sets the ramp time to final regulated output voltage. Alternatively, a resistor divider on another voltage supply connected to this pin allows the LTC3835-1 output to track the other supply during start-up.

V_{FB} (Pin 4/Pin 4): Receives the remotely sensed feedback voltage from an external resistive divider across the output.

SGND (Pin 5/Pin 5): Small-Signal Ground. Must be routed separately from high current grounds to the common (–) terminals of the input capacitor.

PGND (Pin 6/Pin 6): Driver Power Ground. Connects to the source of bottom (synchronous) N-channel MOSFET, anode of the Schottky rectifier and the (–) terminal of C_{IN}.

BG (Pin 7/Pin 7): High Current Gate Drive for Bottom (Synchronous) N-Channel MOSFET. Voltage swing at this pin is from ground to $INTV_{CC}$.

$INTV_{CC}$ (Pin 8/Pin 8): Output of the Internal Linear Low Dropout Regulator. The driver and control circuits are powered from this voltage source. Must be decoupled to power ground with a minimum of 4.7µF tantalum or other low ESR capacitor.

V_{IN} (Pin 9/Pin 9): Main Supply Pin. A bypass capacitor should be tied between this pin and the signal ground pin.

SW (Pin 10/Pin 10): Switch Node Connections to Inductor. Voltage swing at this pin is from a Schottky diode (external) voltage drop below ground to V_{IN}.

TG (Pin 11/Pin 11): High Current Gate Drive for Top N-Channel MOSFET. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ – 0.5V superimposed on the switch node voltage SW.

BOOST (Pin 12/Pin 12): Bootstrapped Supply to the Topside Floating Driver. A capacitor is connected between the BOOST and SW pins and a Schottky diode is tied between the BOOST and $INTV_{CC}$ pins. Voltage swing at the BOOST pin is from $INTV_{CC}$ to (V_{IN} + $INTV_{CC}$).

PIN FUNCTIONS (DHC Package/GN Package)

RUN (Pin 13/Pin 13): Digital Run Control Input for Controller. Forcing this pin below 0.7V shuts down all controller functions, reducing the quiescent current that the LTC3835-1 draws to approximately 10µA.

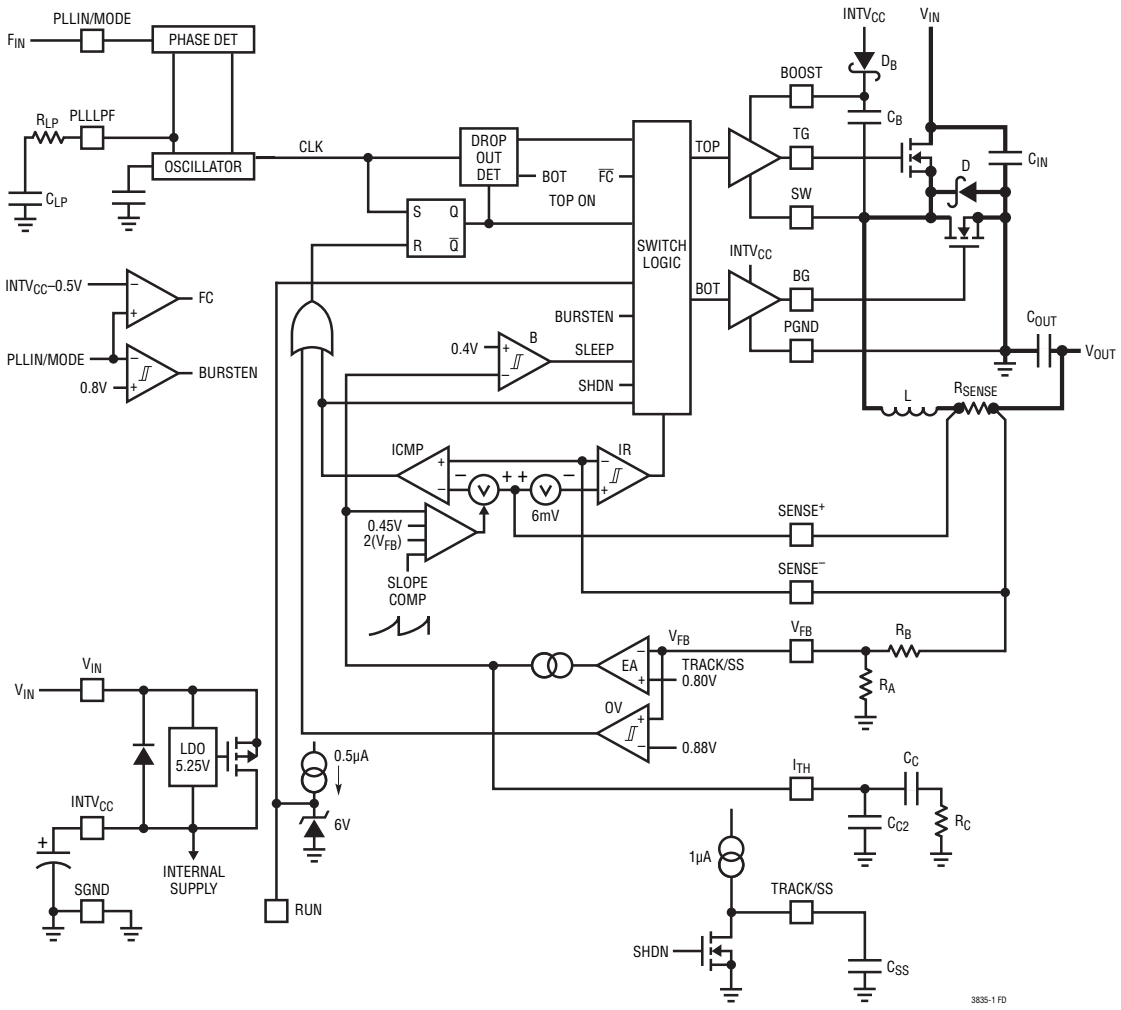
SENSE⁻ (Pin 14/Pin 14): The (–) Input to the Differential Current Comparator.

SENSE⁺ (Pin 15/Pin 15): The (+) Input to the Differential Current Comparator. The I_{TH} pin voltage and controlled offsets between the SENSE⁻ and SENSE⁺ pins in conjunction with R_{SENSE} set the current trip threshold.

PLLIN/MODE (Pin 16/Pin 16): External Synchronization Input to Phase Detector and Forced Continuous Control Input. When an external clock is applied to this pin, the phase-locked loop will force the rising TG signal to be synchronized with the rising edge of the external clock. In this case, an R-C filter must be connected to the PLLLPF pin. When not synchronizing to an external clock, this input determines how the LTC3835-1 operates at light loads. Pulling this pin below 0.7V selects Burst Mode operation. Tying this pin to $INTV_{CC}$ forces continuous inductor current operation. Tying this pin to a voltage greater than 0.9V and less than $INTV_{CC}$ selects pulse-skipping operation.

Exposed Pad (Pin 17, DHC Package): SGND. Must be soldered to PCB.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3835-1 uses a constant-frequency, current mode step-down architecture. During normal operation, each external top MOSFET is turned on when the clock sets the RS latch, and is turned off when the main current comparator, ICMP, resets the RS latch. The peak inductor current at which ICMP trips and resets the latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier EA. The error amplifier compares the output voltage feedback signal at the V_{FB} pin, (which is generated with an external resistor divider connected across the output voltage, V_{OUT}, to ground) to the internal 0.800V reference voltage. When the load current increases, it causes a slight decrease in V_{FB} relative to the reference, which cause the EA to increase the I_{TH} voltage until the average inductor current matches the new load current.

After the top MOSFET is turned off each cycle, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the current comparator IR, or the beginning of the next clock cycle.

$INTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. An internal 5.25V low dropout linear regulator supplies $INTV_{CC}$ power from V_{IN}.

The top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one twelfth of the clock period every tenth cycle to allow C_B to recharge.

Shutdown and Start-Up (RUN and TRACK/SS Pins)

The LTC3835-1 can be shut down using the RUN pin. Pulling this pin below 0.7V shuts down the main control loop for the controller. A low disables the controller and most internal circuits, including the $INTV_{CC}$ regulator, at which time the LTC3835-1 draws only 10µA of quiescent current.

Releasing the RUN pin allows an internal 0.5µA current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum rating of 7V on this pin.

The start-up of the output voltage V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.8V internal reference, the LTC3835-1 regulates the V_{FB} voltage to the TRACK/SS pin voltage instead of the 0.8V reference. This allows the TRACK/SS pin to be used to program a soft-start by connecting an external capacitor from the TRACK/SS pin to SGND. An internal 1µA pull-up current charges this capacitor creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from 0V to 0.8V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value.

Alternatively the TRACK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TRACK/SS pin an external resistor divider from the other supply to ground (see Applications Information section).

When the RUN pin is pulled low to disable the LTC3835-1, or when V_{IN} drops below its undervoltage lockout threshold of 3.5V, the TRACK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, the controller is disabled and the external MOSFETs are held off.

OPERATION (Refer to Functional Diagram)

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping, or Continuous Conduction) (PLLIN/MODE Pin)

The LTC3835-1 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode at low load currents. To select Burst Mode operation, tie the PLLIN/MODE pin to a DC voltage below 0.8V (e.g., SGND). To select forced continuous operation, tie the PLLIN/MODE pin to INTVCC. To select pulse-skipping mode, tie the PLLIN/MODE pin to a DC voltage greater than 0.8V and less than $INTV_{CC}$ – 0.5V.

When the LTC3835-1 is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-tenth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is lower than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.4V, the internal sleep signal goes high (enabling "sleep" mode) and both external MOSFETs are turned off. The I_{TH} pin is then disconnected from the output of the EA and "parked" at 0.425V.

In sleep mode, much of the internal circuitry is turned off, reducing the quiescent current that the LTC3835-1 draws to only 80µA. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the I_{TH} pin is reconnected to the output of the EA, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator.

When the LTC3835-1 is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (IR) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative, thus operating in discontinuous operation.

In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous operation has the advantages of lower output ripple and less interference to audio circuitry. In forced continuous mode, the output ripple is independent of load current.

When the PLLIN/MODE pin is connected for pulse-skipping mode or clocked by an external clock source to use the phase-locked loop (see Frequency Selection and Phase-Locked Loop section), the LTC3835-1 operates in PWM pulse-skipping mode at light loads. In this mode, constant-frequency operation is maintained down to approximately 1% of designed maximum output current. At very light loads, the current comparator ICMP may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Frequency Selection and Phase-Locked Loop (PLLLPF and PLLIN/MODE Pins)

The selection of switching frequency is a tradeoff between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

The switching frequency of the LTC3835-1's controllers can be selected using the PLLLPF pin.

If the PLLIN/MODE pin is not being driven by an external clock source, the PLLLPF pin can be floated, tied to $INTV_{CC}$, or tied to SGND to select 400kHz, 530kHz or 250kHz, respectively.

A phase-locked loop (PLL) is available on the LTC3835-1 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN/MODE pin. In this case, a series R-C should be connected between the PLLLPF pin and SGND to serve as the PLL's loop filter. The LTC3835-1 phase detector adjusts the voltage on the PLLLPF pin to align the turn-on of the external top MOSFET to the rising edge of the synchronizing signal.

OPERATION (Refer to Functional Diagram)

The typical capture range of the LTC3835-1's phase-locked loop is from approximately 115kHz to 800kHz, with a guarantee to be between 140kHz and 650kHz. In other words, the LTC3835-1's PLL is guaranteed to lock to an external clock source whose frequency is between 140kHz and 650kHz.

The typical input clock thresholds on the PLLIN/MODE pin are 1.6V (rising) and 1.2V (falling).

Output Overvoltage Protection

An overvoltage comparator guards against transient overshoots as well as other more serious conditions that may overvoltage the output. When the V_{FB} pin rises to more than 10% higher than its regulation point of 0.800V, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

R_{SENSE} Selection for Output Current

R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold of 100mV/R_{SENSE} and an input common mode range of SGND to 10V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L.

Allowing a margin for variations in the IC and external component values yields:

$$R_{SENSE} = \frac{80mV}{I_{MAX}}$$

When using the controller in very low dropout conditions, the maximum output current level will be reduced due to the internal compensation required to meet stability criterion for buck regulators operating at greater than 50% duty factor. A curve is provided to estimate this reduction in peak output current level depending upon the operating duty factor.

Operating Frequency and Synchronization

The choice of operating frequency, is a trade-off between efficiency and component size. Low frequency operation improves efficiency by reducing MOSFET switching losses, both gate charge loss and transition loss. However, lower frequency operation requires more inductance for a given amount of ripple current.

The internal oscillator of the LTC3835-1 runs at a nominal 400kHz frequency when the PLLLPF pin is left floating and the PLLIN/MODE pin is a DC low or high. Pulling the PLLLPF to $INTV_{CC}$ selects 530kHz operation; pulling the PLLLPF to SGND selects 250kHz operation.

Alternatively, the LTC3835-1 will phase-lock to a clock signal applied to the PLLIN/MODE pin with a frequency between 140kHz and 650kHz (see Phase-Locked Loop and Frequency Synchronization).

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. So why would anyone ever choose to operate at lower frequencies with larger components? The answer is efficiency. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \frac{1}{(f)(L)} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

APPLICATIONS INFORMATION

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.3(I_{MAX})$. The maximum ΔI_L occurs at the maximum input voltage.

The inductor value also has secondary effects. The transition to Burst Mode operation begins when the average inductor current required results in a peak current below 10% of the current limit determined by R_{SENSE}. Lower inductor values (higher ΔI_L) will cause this to occur at lower load currents, which can cause a dip in efficiency in the upper range of low current operation. In Burst Mode operation, lower inductance values will cause the burst frequency to decrease.

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. High efficiency converters generally cannot afford the core loss found in low cost powdered iron cores, forcing the use of more expensive ferrite or molypermalloy cores. Actual core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3835-1: One N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected ($V_{IN} < 5V$); then, sub-logic level threshold MOSFETs ($V_{GS(TH)} < 3V$) should be used. Pay close attention to the BV specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the "ON" resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the Gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

APPLICATIONS INFORMATION

The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER})\bullet\left[\frac{1}{V_{INTVCC}-V_{THMIN}}+\frac{1}{V_{THMIN}}\right](f)$$

$$P_{SYNC} = \frac{V_{IN}-V_{OUT}}{V_{IN}}(I_{MAX})^2(I+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. V_{THMIN} is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diode D1 shown in Figure 8 conducts during the dead-time between the conduction of the two power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead-time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle (V_{OUT})/(V_{IN}). To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN}\ \text{Required}\ I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[(V_{OUT})(V_{IN}-V_{OUT})\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3835-1, ceramic capacitors can also be used for C_{IN}. Always consult the manufacturer if there is any question.

The selection of C_{OUT} is driven by the effective series resistance (ESR). Typically, once the ESR requirement is satisfied, the capacitance is adequate for filtering. The output ripple (ΔV_{OUT}) is approximated by:

$$\Delta V_{OUT} \approx I_{RIPPLE}\left(ESR+\frac{1}{8fC_{OUT}}\right)$$

where f is the operating frequency, C_{OUT} is the output capacitance and I_{RIPPLE} is the ripple current in the inductor. The output ripple is highest at maximum input voltage since I_{RIPPLE} increases with input voltage.

APPLICATIONS INFORMATION

Setting Output Voltage

The LTC3835-1 output voltage is set by an external feedback resistor divider carefully placed across the output, as shown in Figure 1. The regulated output voltage is determined by:

$$V_{OUT} = 0.8V \bullet \left(1 + \frac{R_B}{R_A}\right)$$

To improve the frequency response, a feed-forward capacitor, C_{FF}, may be used. Great care should be taken to route the V_{FB} line away from noise sources, such as the inductor and the SW line.

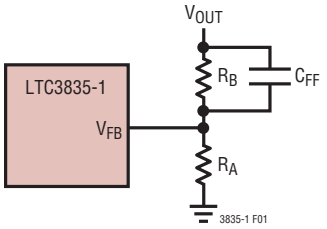


Figure 1. Setting Output Voltage

SENSE+ and SENSE– Pins

The common mode input range of the current comparator is from 0V to 10V. Continuous linear operation is provided throughout this range allowing output voltages from 0.8V to 10V. The input stage of the current comparator requires that current either be sourced or sunk from the SENSE pins depending on the output voltage, as shown in the curve in Figure 2. If the output voltage is below 1.5V, current will flow out of both SENSE pins to the main output. In these cases, the output can be easily pre-loaded by the V_{OUT} resistor divider to compensate for the current comparator's negative input bias current. Since V_{FB} is servoed to the 0.8V reference voltage, R_A in Figure 1 should be chosen to be less than $0.8V/I_{SENSE}$, with I_{SENSE} determined from Figure 2 at the specified output voltage.

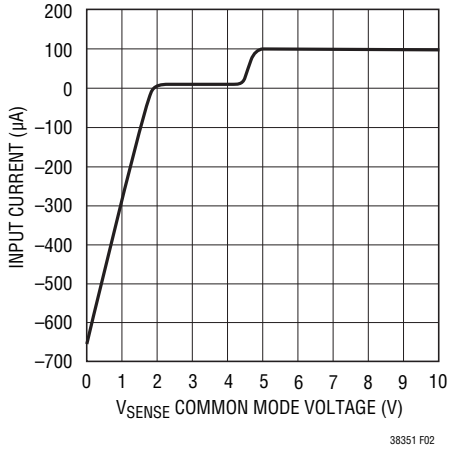


Figure 2. SENSE Pins Input Bias Current vs Common Mode (Output) Voltage

Tracking and Soft-Start (TRACK/SS Pin)

The start-up of V_{OUT} is controlled by the voltage on the TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the internal 0.8V reference, the LTC3835-1 regulates the V_{FB} pin voltage to the voltage on the TRACK/SS pin instead of 0.8V. The TRACK/SS pin can be used to program an external soft-start function or to allow V_{OUT} to "track" another supply during start-up.

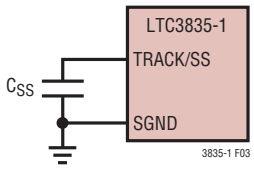


Figure 3. Using the TRACK/SS Pin to Program Soft-Start

Soft-start is enabled by simply connecting a capacitor from the TRACK/SS pin to ground, as shown in Figure 3. An internal 1µA current source charges up the capacitor, providing a linear ramping voltage at the TRACK/SS pin. The LTC3835-1 will regulate the V_{FB} pin (and hence V_{OUT}) according to the voltage on the TRACK/SS pin, allowing V_{OUT} to rise smoothly from 0V to its final regulated value. The total soft-start time will be approximately:

$$t_{SS} = C_{SS} \bullet \frac{0.8V}{1\mu A}$$

APPLICATIONS INFORMATION

Alternatively, the TRACK/SS pin can be used to track two (or more) supplies during start-up, as shown qualitatively in Figures 4a and 4b. To do this, a resistor divider should be connected from the master supply (V_X) to the TRACK/SS pin of the slave supply (V_{OUT}), as shown in Figure 5. During start-up V_{OUT} will track V_X according to the ratio set by the resistor divider:

$$\frac{V_X}{V_{OUT}} = \frac{R_A}{R_{TRACKA}} \bullet \frac{R_{TRACKA} + R_{TRACKB}}{R_A + R_B}$$

For coincident tracking ($V_{OUT} = V_X$ during start-up),

$R_A = R_{TRACKA}$

$R_B = R_{TRACKB}$

$INTV_{CC}$ Regulators

The LTC3835-1 features an internal P-channel low dropout linear regulator (LDO) that supplies power at the $INTV_{CC}$ pin from the V_{IN} supply pin. $INTV_{CC}$ powers the gate drivers and much of the LTC3835-1's internal circuitry. The V_{IN} LDO regulates the voltage at the $INTV_{CC}$ pin to 5.25V. It can supply a peak current of 50mA and must be bypassed to ground with a minimum of 4.7µF tantalum, 10µF special polymer, or low ESR electrolytic capacitor. A ceramic capacitor with a minimum value of 4.7µF can also be used if a 1Ω resistor is added in series with the capacitor. No matter what type of bulk capacitor is used, an additional 1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND IC pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

(4a) Coincident Tracking **(4b) Ratiometric Tracking**

Figure 4. Two Different Modes of Output Voltage Tracking

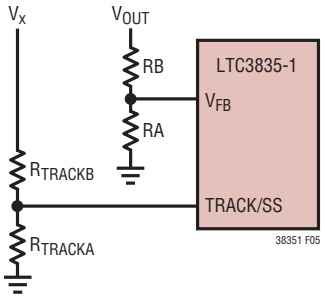


Figure 5. Using the TRACK/SS Pin for Tracking

APPLICATIONS INFORMATION

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3835-1 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, is supplied by the 5.25V V_{IN} LDO. Power dissipation for the IC in this case is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 2 of the Electrical Characteristics. For example, the LTC3835-1 $INTV_{CC}$ current is limited to less than 25mA from a 24V supply when in the GN package:

$T_J = 70°C + (25mA)(24V)(90°C/W) = 125°C$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (PLLIN/MODE = $INTV_{CC}$) at maximum V_{IN}.

Topside MOSFET Driver Supply (C_B, D_B)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFET. Capacitor C_B in the Functional Diagram is charged though external diode D_B from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFET is to be turned on, the driver places the C_B voltage across the gate-source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Fault Conditions: Current Limit and Current Foldback

The LTC3835-1 includes current foldback to help limit load current when the output is shorted to ground. If the output falls below 70% of its nominal output level, then the maximum sense voltage is progressively lowered from 100mV to 30mV. Under short-circuit conditions with very low duty cycles, the LTC3835-1 will begin cycle skipping in order to limit the short-circuit current. In this situation the bottom MOSFET will be dissipating most of the power but less than in normal operation. The short-circuit ripple current is determined by the minimum on-time $t_{ON(MIN)}$ of the LTC3835-1 (≈180ns), the input voltage and inductor value:

$\Delta I_{L(SC)} = t_{ON(MIN)} (V_{IN}/L)$

The resulting short-circuit current is:

$$I_{SC} = \frac{10mV}{R_{SENSE}} - \frac{1}{2}\Delta I_{L(SC)}$$

Fault Conditions: Overvoltage Protection (Crowbar)

The overvoltage crowbar is designed to blow a system input fuse when the output voltage of the regulator rises much higher than nominal levels. The crowbar causes huge currents to flow, that blow the fuse to protect against a shorted top MOSFET if the short occurs while the controller is operating.

A comparator monitors the output for overvoltage conditions. The comparator (OV) detects overvoltage faults greater than 10% above the nominal output voltage. When this condition is sensed, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared. The bottom MOSFET remains on continuously for as long as the OV condition persists; if V_{OUT} returns to a safe level, normal operation automatically resumes. A shorted top MOSFET will result in a high current condition which will open the system fuse. The switching regulator will regulate properly with a leaky top MOSFET by altering the duty cycle to accommodate the leakage.

APPLICATIONS INFORMATION

Phase-Locked Loop and Frequency Synchronization

The LTC3835-1 has a phase-locked loop (PLL) comprised of an internal voltage-controlled oscillator (VCO) and a phase detector. This allows the turn-on of the top MOSFET to be locked to the rising edge of an external clock signal applied to the PLLIN/MODE pin. The phase detector is an edge sensitive digital type that provides zero degrees phase shift between the external and internal oscillators. This type of phase detector does not exhibit false lock to harmonics of the external clock.

The output of the phase detector is a pair of complementary current sources that charge or discharge the external filter network connected to the PLLLPF pin. The relationship between the voltage on the PLLLPF pin and operating frequency, when there is a clock signal applied to PLLIN/MODE, is shown in Figure 6 and specified in the Electrical Characteristics table. Note that the LTC3835-1 can only be synchronized to an external clock whose frequency is within range of the LTC3835-1's internal VCO, which is nominally 115kHz to 800kHz. This is guaranteed to be between 140kHz and 650kHz. A simplified block diagram is shown in Figure 7.

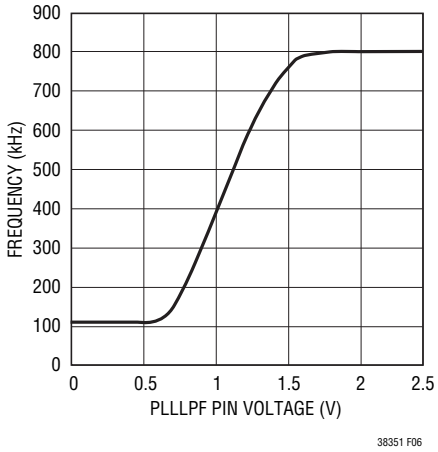


Figure 6. Relationship Between Oscillator Frequency and Voltage at the PLLLPF Pin When Synchronizing to an External Clock

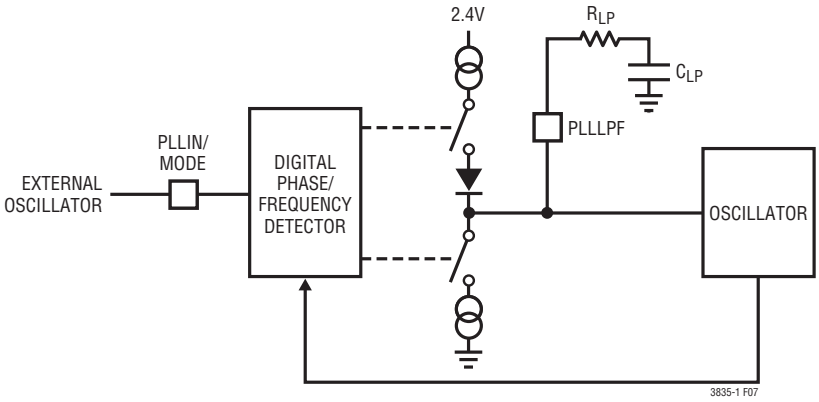


Figure 7. Phase-Locked Loop Block Diagram

APPLICATIONS INFORMATION

If the external clock frequency is greater than the internal oscillator's frequency, f_{OSC}, then current is sourced continuously from the phase detector output, pulling up the PLLLPF pin. When the external clock frequency is less than f_{OSC}, current is sunk continuously, pulling down the PLLLPF pin. If the external and internal frequencies are the same but exhibit a phase difference, the current sources turn on for an amount of time corresponding to the phase difference. The voltage on the PLLLPF pin is adjusted until the phase and frequency of the internal and external oscillators are identical. At the stable operating point, the phase detector output is high impedance and the filter capacitor C_{LP} holds the voltage.

The loop filter components, C_{LP} and R_{LP}, smooth out the current pulses from the phase detector and provide a stable input to the voltage-controlled oscillator. The filter components C_{LP} and R_{LP} determine how fast the loop acquires lock. Typically R_{LP} = 10k and C_{LP} is 2200pF to 0.01µF.

Typically, the external clock (on PLLIN/MODE pin) input high threshold is 1.6V, while the input low threshold is 1.2V.

Table 1 summarizes the different states in which the PLLLPF pin can be used.

Table 1

PLLLPF PIN	PLLIN/MODE PIN	FREQUENCY
0V	DC Voltage	250kHz
Floating	DC Voltage	400kHz
$INTV_{CC}$	DC Voltage	530kHz
RC Loop Filter	Clock Signal	Phase-Locked to External Clock

Minimum On-Time Considerations

Minimum on-time $t_{ON(MIN)}$ is the smallest time duration that the LTC3835-1 is capable of turning on the top MOSFET. It is determined by internal timing delays and the gate charge required to turn on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$t_{ON(MIN)} < \frac{V_{OUT}}{V_{IN}(f)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the ripple voltage and current will increase.

The minimum on-time for the LTC3835-1 is approximately 180ns. However, as the peak sense voltage decreases the minimum on-time gradually increases up to about 200ns. This is of particular concern in forced continuous applications with low ripple current at light loads. If the duty cycle drops below the minimum on-time limit in this situation, a significant amount of cycle skipping can occur with correspondingly larger current and voltage ripple.

APPLICATIONS INFORMATION

Efficiency Considerations

The percent efficiency of a switching regulator is equal to the output power divided by the input power times 100%. It is often useful to analyze individual losses to determine what is limiting the efficiency and which change would produce the most improvement. Percent efficiency can be expressed as:

%Efficiency = 100% – (L1 + L2 + L3 + ...)

where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the circuit produce losses, four main sources usually account for most of the losses in LTC3835-1 circuits: 1) IC V_{IN} current, 2) $INTV_{CC}$ regulator current, 3) I^2R losses, 4) Topside MOSFET transition losses.

1. The V_{IN} current has two components: the first is the DC supply current given in the Electrical Characteristics table, which excludes MOSFET driver and control currents; the second is the current drawn from the 3.3V linear regulator output. V_{IN} current typically results in a small (<0.1%) loss.

2. $INTV_{CC}$ current is the sum of the MOSFET driver and control currents. The MOSFET driver current results from switching the gate capacitance of the power MOSFETs. Each time a MOSFET gate is switched from low to high to low again, a packet of charge dQ moves from $INTV_{CC}$ to ground. The resulting dQ/dt is a current out of $INTV_{CC}$ that is typically much larger than the control circuit current. In continuous mode, $I_{GATECHG} = f(Q_T + Q_B)$, where Q_T and Q_B are the gate charges of the topside and bottom side MOSFETs.

3. I^2R losses are predicted from the DC resistances of the fuse (if used), MOSFET, inductor, current sense resistor, and input and output capacitor ESR. In continuous mode the average output current flows through L and R_{SENSE}, but is "chopped" between the topside MOSFET and the synchronous MOSFET. If the two MOSFETs have approximately the same $R_{DS(ON)}$, then the resistance of one MOSFET can simply be summed with the resistances of L, R_{SENSE} and ESR to obtain I^2R losses. For example, if each $R_{DS(ON)} = 30m\Omega$, $R_L = 50m\Omega$, $R_{SENSE} = 10m\Omega$ and $R_{ESR} = 40m\Omega$ (sum of both input and output capacitance losses), then the total resistance is $130m\Omega$. This results in losses ranging from 3% to 13% as the output current increases from 1A to 5A for a 5V output, or a 4% to 20% loss for a 3.3V output. Efficiency varies as the inverse square of V_{OUT} for the same external components and output power level. The combined effects of increasingly lower output voltages and higher currents required by high performance digital systems is not doubling but quadrupling the importance of loss terms in the switching regulator system!

4. Transition losses apply only to the topside MOSFET(s), and become significant only when operating at high input voltages (typically 15V or greater). Transition losses can be estimated from:

$$\text{Transition Loss} = (1.7)\, V_{IN}^2\, I_{O(MAX)}\, C_{RSS}\, f$$

Other "hidden" losses such as copper trace and internal battery resistances can account for an additional 5% to 10% efficiency degradation in portable systems. It is very important to include these "system" level losses during the design phase. The internal battery and fuse resistance losses can be minimized by making sure that C_{IN} has adequate charge storage and very low ESR at the switching frequency. A 25W supply will typically require a minimum of 20µF to 40µF of capacitance having a maximum of $20m\Omega$ to $50m\Omega$ of ESR. Other losses including Schottky conduction losses during dead-time and inductor core losses generally account for less than 2% total additional loss.

APPLICATIONS INFORMATION

Checking Transient Response

The regulator loop response can be checked by looking at the load current transient response. Switching regulators take several cycles to respond to a step in DC (resistive) load current. When a load step occurs, V_{OUT} shifts by an amount equal to ΔI_{LOAD} (ESR), where ESR is the effective series resistance of C_{OUT}. ΔI_{LOAD} also begins to charge or discharge C_{OUT} generating the feedback error signal that forces the regulator to adapt to the current change and return V_{OUT} to its steady-state value. During this recovery time V_{OUT} can be monitored for excessive overshoot or ringing, which would indicate a stability problem. OPTI-LOOP compensation allows the transient response to be optimized over a wide range of output capacitance and ESR values. *The availability of the I_{TH} pin not only allows optimization of control loop behavior but also provides a DC coupled and AC filtered closed-loop response test point. The DC step, rise time and settling at this test point truly reflects the closed-loop response.* Assuming a predominantly second order system, phase margin and/or damping factor can be estimated using the percentage of overshoot seen at this pin. The bandwidth can also be estimated by examining the rise time at the pin. The I_{TH} external components shown in Figure 10 circuit will provide an adequate starting point for most applications.

The I_{TH} series R_C-C_C filter sets the dominant pole-zero loop compensation. The values can be modified slightly (from 0.5 to 2 times their suggested values) to optimize transient response once the final PC layout is done and the particular output capacitor type and value have been determined. The output capacitors need to be selected because the various types and values determine the loop gain and phase. An output current pulse of 20% to 80% of full-load current having a rise time of 1µs to 10µs will produce output voltage and I_{TH} pin waveforms that will give a sense of the overall loop stability without breaking the feedback loop. Placing a power MOSFET directly across the output capacitor and driving the gate with an appropriate signal generator is a practical way to produce a realistic load step condition. The initial output voltage step resulting from the step change in output current may not be within the bandwidth of the feedback loop, so this signal cannot be used to determine phase margin. This is why it is better to look at the I_{TH} pin signal which is in the feedback loop and is the filtered and compensated control loop response. The gain of the loop will be increased by increasing R_C and the bandwidth of the loop will be increased by decreasing C_C. If R_C is increased by the same factor that C_C is decreased, the zero frequency will be kept the same, thereby keeping the phase shift the same in the most critical frequency range of the feedback loop. The output voltage settling behavior is related to the stability of the closed-loop system and will demonstrate the actual overall supply performance.

A second, more severe transient is caused by switching in loads with large (>1µF) supply bypass capacitors. The discharged bypass capacitors are effectively put in parallel with C_{OUT}, causing a rapid drop in V_{OUT}. No regulator can alter its delivery of current quickly enough to prevent this sudden step change in output voltage if the load switch resistance is low and it is driven quickly. If the ratio of C_{LOAD} to C_{OUT} is greater than 1:50, the switch rise time should be controlled so that the load rise time is limited to approximately 25 • C_{LOAD}. Thus a 10µF capacitor would require a 250µs rise time, limiting the charging current to about 200mA.

APPLICATIONS INFORMATION

Design Example

As a design example, assume V_{IN} = 12V(nominal), V_{IN} = 22V(max), V_{OUT} = 1.8V, I_{MAX} = 5A and f = 250kHz.

The inductance value is chosen first based on a 30% ripple current assumption. The highest value of ripple current occurs at the maximum input voltage. Tie the PLLLPF pin to GND, generating 250kHz operation. The minimum inductance for 30% ripple current is:

$$\Delta I_L = \frac{V_{OUT}}{(f)(L)}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

A 4.7µH inductor will produce 23% ripple current and a 3.3µH will result in 33%. The peak inductor current will be the maximum DC value plus one half the ripple current, or 5.84A, for the 3.3µH value. Increasing the ripple current will also help ensure that the minimum on-time of 180ns is not violated. The minimum on-time occurs at maximum V_{IN}:

$$t_{ON(MIN)} = \frac{V_{OUT}}{V_{IN(MAX)}f} = \frac{1.8V}{22V(250kHz)} = 327ns$$

The R_{SENSE} resistor value can be calculated by using the maximum current sense voltage specification with some accommodation for tolerances:

$$R_{SENSE} \le \frac{80mV}{5.84A} \approx 0.012\Omega$$

Choosing 1% resistors: R1 = 25.5k and R2 = 32.4k yields an output voltage of 1.816V.

The power dissipation on the topside MOSFET can be easily estimated. Choosing a Fairchild FDS6982S dual MOSFET results in: $R_{DS(ON)}$ = 0.035Ω/0.022Ω, C_{MILLER} = 215pF. At maximum input voltage with T(estimated) = 50°C:

$$P_{MAIN} = \frac{1.8V}{22V}(5)^2\left[1+(0.005)(50°C-25°C)\right]\bullet$$
$$(0.035\Omega)+(22V)^2\left(\frac{5A}{2}\right)(4\Omega)(215pF)\bullet$$
$$\left[\frac{1}{5-2.3}+\frac{1}{2.3}\right](300kHz) = 332mW$$

A short-circuit to ground will result in a folded back current of:

$$I_{SC} = \frac{25mV}{0.01\Omega} - \frac{1}{2}\left(\frac{120ns(22V)}{3.3\mu H}\right) = 2.1A$$

with a typical value of $R_{DS(ON)}$ and δ = (0.005/°C)(20) = 0.1. The resulting power dissipated in the bottom MOSFET is:

$$P_{SYNC} = \frac{22V-1.8V}{22V}(2.1A)^2(1.125)(0.022\Omega)$$
$$= 100mW$$

which is less than under full-load conditions.

C_{IN} is chosen for an RMS current rating of at least 3A at temperature assuming only this channel is on. C_{OUT} is chosen with an ESR of 0.02Ω for low output ripple. The output ripple in continuous mode will be highest at the maximum input voltage. The output voltage ripple due to ESR is approximately:

$$V_{ORIPPLE} = R_{ESR}(\Delta I_L) = 0.02\Omega(1.67A) = 33mV_{P-P}$$

APPLICATIONS INFORMATION

PC Board Layout Checklist

When laying out the printed circuit board, the following checklist should be used to ensure proper operation of the IC. These items are also illustrated graphically in the layout diagram of Figure 8. The Figure 9 illustrates the current waveforms present in the various branches of the synchronous regulator operating in the continuous mode. Check the following in your layout:

1. Is the top N-channel MOSFET M1 located within 1cm of C_{IN}?
2. Are the signal and power grounds kept separate? The combined IC signal ground pin and the ground return of C_{INTVCC} must return to the combined C_{OUT} (–) terminals. The path formed by the top N-channel MOSFET, Schottky diode and the C_{IN} capacitor should have short leads and PC trace lengths. The output capacitor (–) terminals should be connected as close as possible to the (–) terminals of the input capacitor by placing the capacitors next to each other and away from the Schottky loop described above.
3. Does the LTC3835-1 V_{FB} pin resistive divider connect to the (+) terminals of C_{OUT}? The resistive divider must be connected between the (+) terminal of C_{OUT} and signal ground. The feedback resistor connections should not be along the high current input feeds from the input capacitor(s).
4. Are the SENSE$^-$ and SENSE$^+$ leads routed together with minimum PC trace spacing? The filter capacitor between SENSE$^+$ and SENSE$^-$ should be as close as possible to the IC. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
5. Is the $INTV_{CC}$ decoupling capacitor connected close to the IC, between the $INTV_{CC}$ and the power ground pins? This capacitor carries the MOSFET drivers current peaks. An additional 1µF ceramic capacitor placed immediately next to the $INTV_{CC}$ and PGND pins can help improve noise performance substantially.
6. Keep the switching node (SW), top gate node (TG), and boost node (BOOST) away from sensitive small-signal nodes, especially from the opposites channel's voltage and current sensing feedback pins. All of these nodes have very large and fast moving signals and therefore should be kept on the "output side" of the LTC3835-1 and occupy minimum PC trace area.
7. Use a modified "star ground" technique: a low impedance, large copper area central grounding point on the same side of the PC board as the input and output capacitors with tie-ins for the bottom of the $INTV_{CC}$ decoupling capacitor, the bottom of the voltage feedback resistive divider and the SGND pin of the IC.

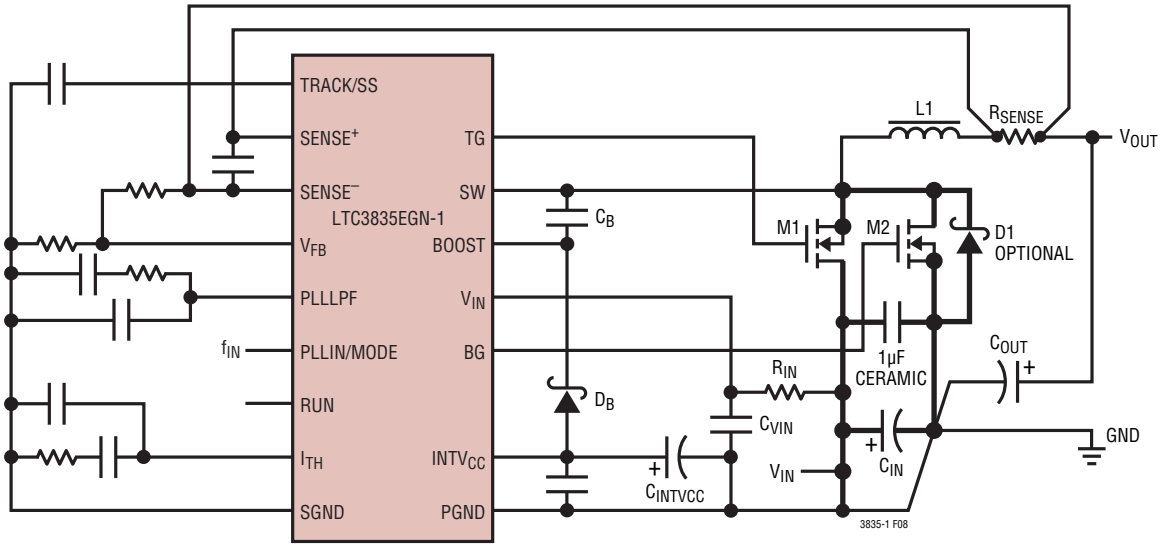


Figure 8. LTC3835-1 Recommended Printed Circuit Layout Diagram

APPLICATIONS INFORMATION

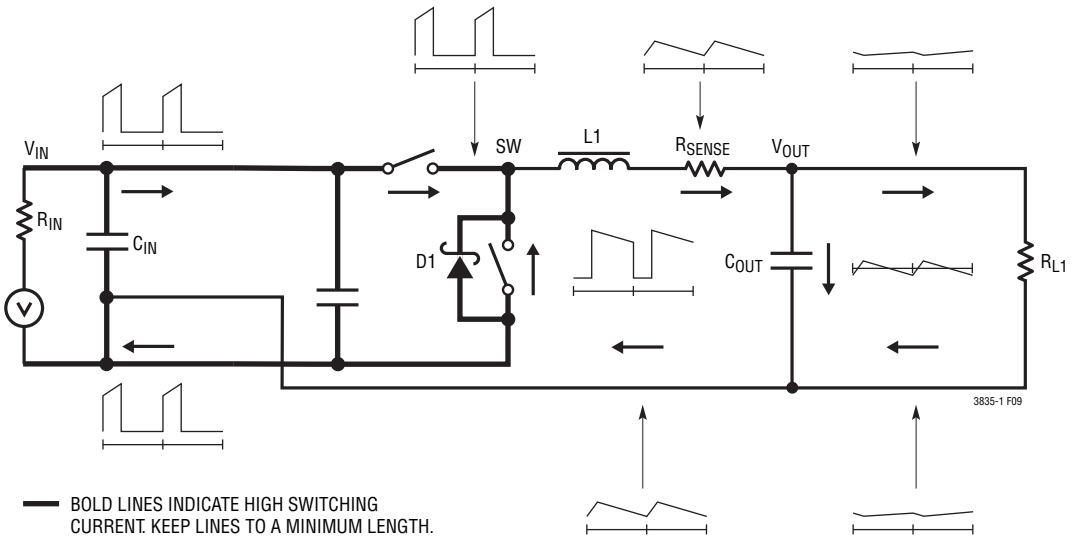


Figure 9. Branch Current Waveforms

PC Board Layout Debugging

It is helpful to use a DC-50MHz current probe to monitor the current in the inductor while testing the circuit. Monitor the output switching node (SW pin) to synchronize the oscilloscope to the internal oscillator and probe the actual output voltage as well. Check for proper performance over the operating voltage and current range expected in the application. The frequency of operation should be maintained over the input voltage range down to dropout and until the output load drops below the low current operation threshold—typically 10% of the maximum designed current level in Burst Mode operation.

The duty cycle percentage should be maintained from cycle to cycle in a well-designed, low noise PCB implementation. Variation in the duty cycle at a subharmonic rate can suggest noise pickup at the current or voltage sensing inputs or inadequate loop compensation. Overcompensation of the loop can be used to tame a poor PC layout if regulator bandwidth optimization is not required.

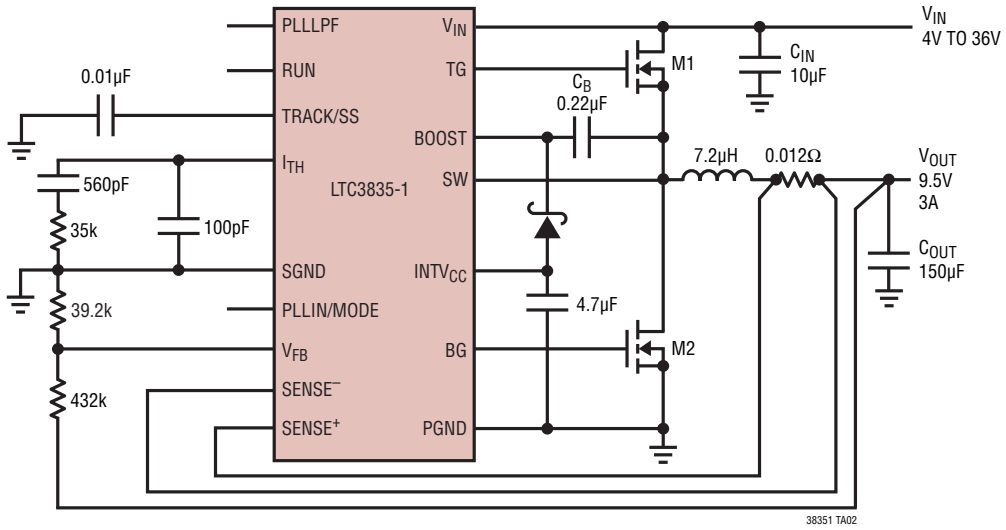
Reduce V_{IN} from its nominal level to verify operation of the regulator in dropout. Check the operation of the undervoltage lockout circuit by further lowering V_{IN} while monitoring the outputs to verify operation.

Investigate whether any problems exist only at higher output currents or only at higher input voltages. If problems coincide with high input voltages and low output currents, look for capacitive coupling between the BOOST, SW, TG, and possibly BG connections and the sensitive voltage and current pins. The capacitor placed across the current sensing pins needs to be placed immediately adjacent to the pins of the IC. This capacitor helps to minimize the effects of differential noise injection due to high frequency capacitive coupling. If problems are encountered with high current output loading at lower input voltages, look for inductive coupling between C_{IN}, Schottky and the top MOSFET components to the sensitive current and voltage sensing traces. In addition, investigate common ground path voltage pickup between these components and the SGND pin of the IC.

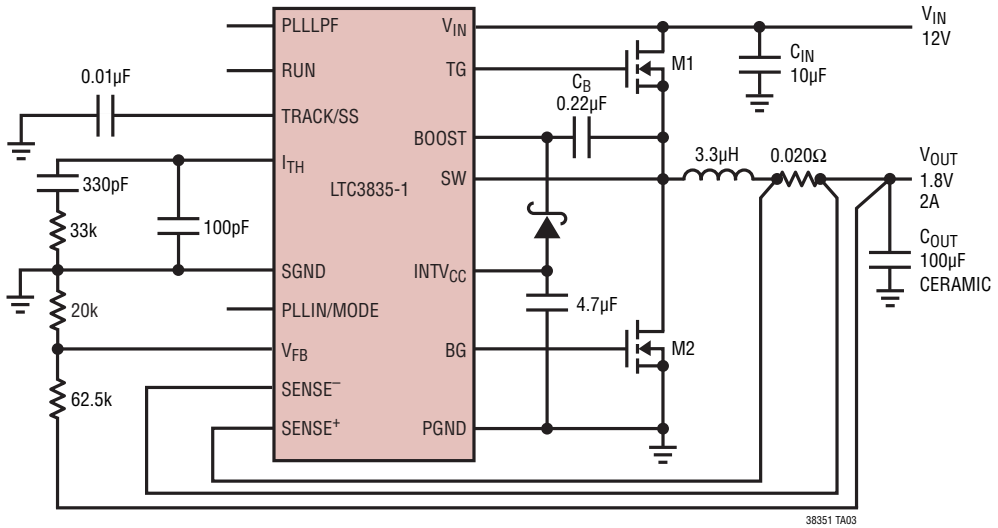
An embarrassing problem, which can be missed in an otherwise properly working switching regulator, results when the current sensing leads are hooked up backwards. The output voltage under this improper hookup will still be maintained but the advantages of current mode control will not be realized. Compensation of the voltage loop will be much more sensitive to component selection. This behavior can be investigated by temporarily shorting out the current sensing resistor—don't worry, the regulator will still maintain control of the output voltage.

TYPICAL APPLICATIONS

High Efficiency 9.5V, 3A Step-Down Converter



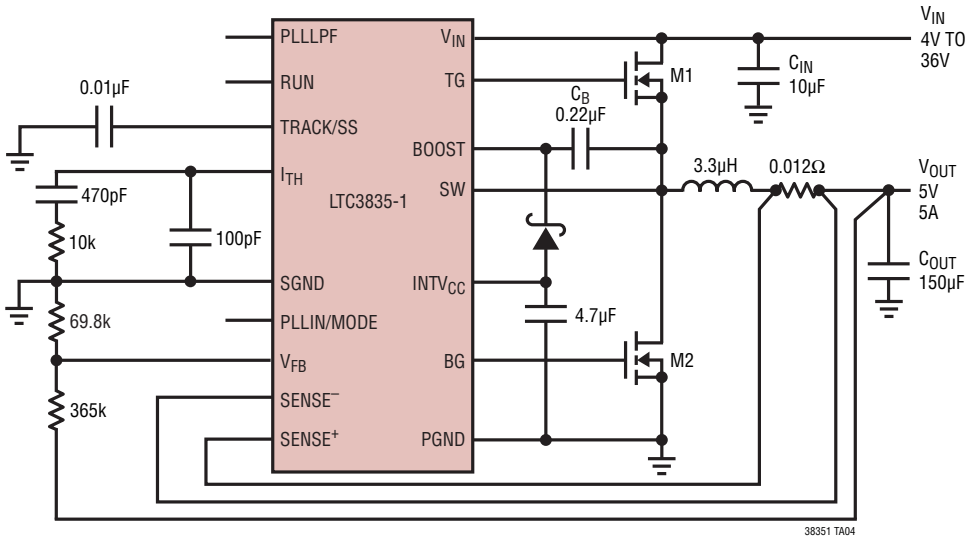
High Efficiency 12V to 1.8V, 2A Step-Down Converter



M1, M2: Si4840DY
L1 TOKO 053LC A915AY-3R3M

TYPICAL APPLICATIONS

High Efficiency 5V, 5A Step-Down Converter



High Efficiency 1.2V, 5A Step-Down Converter