Dual, Fast, Accurate Step-Down DC/DC Controller with Differential Output Sensing

FEATURES

- **Wide V_{IN} Range: 4.5V to 38V, V_{OUT}: 0.6V to 5.5V**
- **±0.67% Output Voltage Accuracy Over Temperature, Differential Output Voltage Sensing, Allowing Up to ±500mV Line Loss at Remote Ground on Channel 1**
- **±1% Output on the Independent 2nd Channel**
- **Controlled On-Time, Valley Current Mode Control**
- **Fast Load Transient Response**
- **Detect Transient (DTR) Reduces V_{OUT} Overshoot**
- **Frequency Programmable from 200kHz to 2MHz, Synchronizable to External Clock**
- **$t_{ON(MIN)}$ = 30ns, $t_{OFF(MIN)}$ = 90ns**
- R_{SENSE} or Inductor DCR Current Sensing
- Overvoltage Protection and Current Limit Foldback
- Power Good Output Voltage Monitor
- Output Voltage Tracking and Adjustable Soft Start-Up
- Thermally Enhanced 38-Pin (5mm × 7mm) QFN and TSSOP packages

APPLICATIONS

- Distributed Power Systems
- Point-of-Load Converters
- Computing Systems
- Data Communication Systems

DESCRIPTION

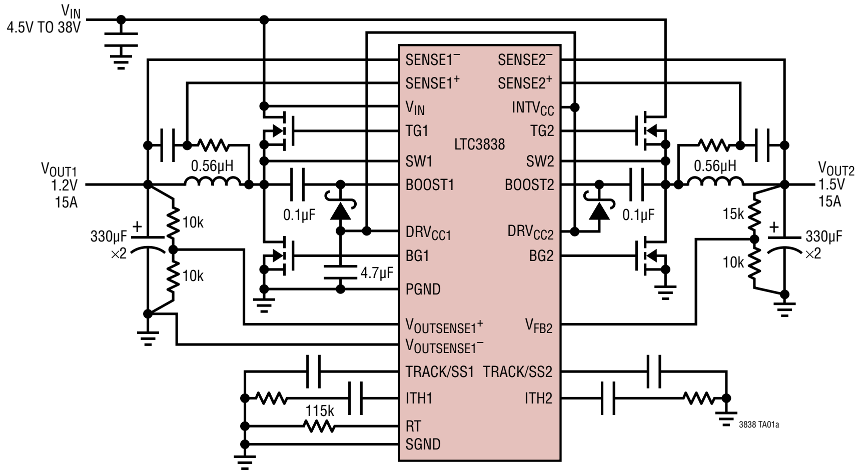
The LTC®3838 is a dual, PolyPhase® synchronous step-down DC/DC switching regulator controller. Two independent channels drive all N-channel power MOSFETs. The controlled on-time, valley current mode control architecture allows for fast transient response and constant frequency switching in steady-state operation, independent of V_{IN}, V_{OUT} and load current. Its load-release transient detection feature significantly reduces overshoot at low output voltages.

Differential output voltage sensing, along with a precision internal reference, offers an accurate ±0.67% output regulation on Channel 1, even if the remote output ground deviates from local ground by ±500mV. The second channel can either provide an independent ±1% output, or together with the first channel of this controller, serve as one of the PolyPhase channels for a single-output voltage.

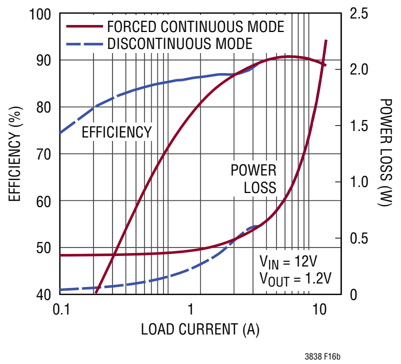
The switching frequency can be programmed from 200kHz to 2MHz with an external resistor, and can be synchronized to an external clock. Very low t_{ON} and t_{OFF} times allow for near 0% and near 100% duty cycles, respectively. Voltage tracking soft start-up and multiple safety features are provided.

TYPICAL APPLICATION

1.2V/1.5V, 15A, 350kHz, DCR Sense, Step-Down Converter (Refer to Figure 16 for Full Design)



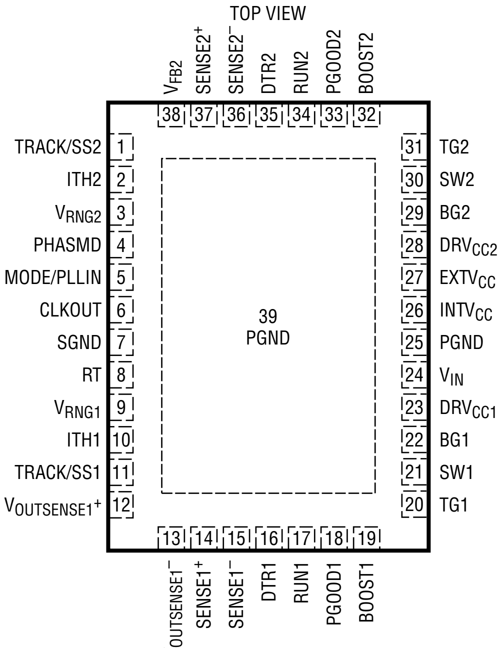
Efficiency/Power Loss



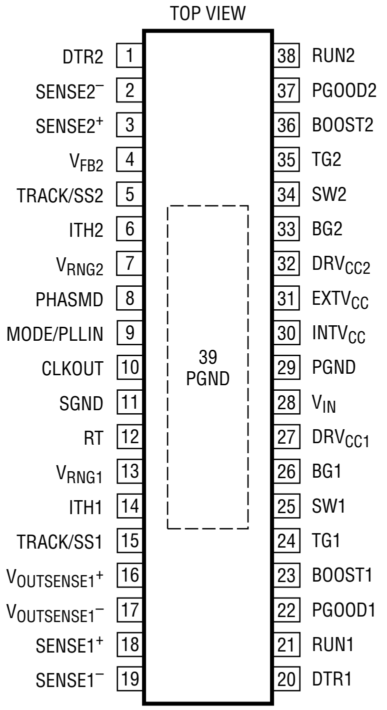
ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{IN} Voltage .... –0.3V to 40V
BOOST1, BOOST2 Voltages .... –0.3V to 46V
SW1, SW2 Voltages .... –5V to 40V
$INTV_{CC}$, DRV_{CC1}, DRV_{CC2}, $EXTV_{CC}$, PGOOD1, PGOOD2, RUN1, RUN2, (BOOST1-SW1), (BOOST2-SW2), MODE/PLLIN Voltages ...... –0.3V to 6V
$V_{OUTSENSE1}^+$, $V_{OUTSENSE1}^-$, SENSE1$^+$, SENSE2$^+$, SENSE1$^-$, SENSE2$^-$ Voltages .... –0.6V to 6V
TRACK/SS1, TRACK/SS2 Voltages .... –0.3V to 5V
DTR1, DTR2, PHASMD, RT, V_{RNG1}, V_{RNG2}, V_{FB2}, ITH1, ITH2 Voltages .... –0.3V to ($INTV_{CC}$ + 0.3V)
Operating Junction Temperature Range (Note 2, 3, 4) .... –40°C to 125°C
Storage Temperature Range .... –65°C to 150°C
Lead Temperature (Soldering, 10 sec)
FE Package .... 300°C

PIN CONFIGURATION



UHF PACKAGE
38-LEAD (5mm × 7mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB



FE PACKAGE
38-LEAD PLASTIC TSSOP
T_{JMAX} = 125°C, θ_{JA} = 28°C/W
EXPOSED PAD (PIN 39) IS PGND, MUST BE SOLDERED TO PCB

Table 1. Comparison of LTC3838 Options

PART NUMBER	DESCRIPTION
LTC3838	±0.67% Differential Output Regulation on Channel 1 ±1% Output Regulation on Channel 2 Separate-Per-Channel Continuous 30mV to 100mV Current Sense Range Controls
LTC3838-1	±0.67% and ±0.75%, Both Differential Output Regulation on Channel 1 and 2 Single-Pin 30mV/60mV Current Sense Range Control, Improved Current Limit Accuracy Than LTC3838
LTC3838-2	±0.67% Differential Output Regulation with Internal Reference on Channel 1 ±4mV Differential Output Regulation with External Reference Voltage on Channel 2 Fixed 30mV Current Sense Range, Improved Current Limit Accuracy Than LTC3838

ORDER INFORMATION

(http://www.linear.com/product/LTC3838#orderinfo)

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3838EUHF#PBF	LTC3838EUHF#TRPBF	3838	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3838IUHF#PBF	LTC3838IUHF#TRPBF	3838	38-Lead (5mm × 7mm) Plastic QFN	–40°C to 125°C
LTC3838EFE#PBF	LTC3838EFE#TRPBF	LTC3838FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3838IFE#PBF	LTC3838IFE#TRPBF	LTC3838FE	38-Lead Plastic TSSOP	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/. Some packages are available in 500 unit reels through designated sales channels with #TRMPBF suffix.

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Operating Range			4.5		38	V
$V_{OUT1,2(REG)}$	Regulated Output Voltage Operating Range	V_{OUT1} Regulated Differentially with Respect to $V_{OUTSENSE1}^-$, V_{OUT2} Regulated with Respect to SGND		0.6		5.5	V
I_Q	Input DC Supply Current						
	Both Channels Enabled	MODE/PLLIN = 0V, No Load			3		mA
	Only One Channel Enabled	RUN1 or RUN2 (But Not Both) = 0V			2		mA
	Shutdown Supply Current	RUN1 = RUN2 = 0V			15		µA
$V_{OUTSENSE1(REG)}$	Regulated Differential Feedback Voltage on Channel 1 ($V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$)	ITH1 = 1.2V (Note 5)					
		T_A = 25°C		0.5985	0.6	0.6015	V
		T_A = 0°C to 85°C	●	0.596	0.6	0.604	V
		T_A = –40°C to 125°C	●	0.594	0.6	0.606	V
	Regulated Differential Feedback Voltage on Channel 1 Over Line, Load and Common Mode	V_{IN} = 4.5V to 38V, ITH1 = 0.5V to 1.9V (Note 5), –0.5V < $V_{OUTSENSE1}^-$ < 0.5V					
		T_A = 0°C to 85°C	●	0.594	0.6	0.606	V
		T_A = –40°C to 125°C	●	0.591	0.6	0.609	V
$V_{FB2(REG)}$	Regulated Feedback Voltage on Channel 2	ITH2 = 1.2V (Note 5)					
		T_A = 25°C		0.597	0.6	0.603	V
		T_A = 0°C to 85°C	●	0.594	0.6	0.606	V
		T_A = –40°C to 125°C	●	0.592	0.6	0.608	V
	Regulated Feedback Voltage on Channel 2 Over Line, Load	V_{IN} = 4.5V to 38V, ITH2 = 0.5V to 1.9V (Note 5)					
		T_A = 0°C to 85°C	●	0.592	0.6	0.608	V
		T_A = –40°C to 125°C	●	0.588	0.6	0.612	V
$I_{VOUTSENSE1^+}$	$V_{OUTSENSE1}^+$ Input Bias Current	$V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$ = 0.6V			±5	±25	nA
$I_{VOUTSENSE1^-}$	$V_{OUTSENSE1}^-$ Input Bias Current	$V_{OUTSENSE1}^+ - V_{OUTSENSE1}^-$ = 0.6V			–25	–50	µA
I_{VFB2}	V_{FB2} Input Bias Current	V_{FB2} = 0.6V			–5	±50	nA
$g_{m(EA)1,2}$	Error Amplifier Transconductance	ITH = 1.2V (Note 5)			1.7		mS
$t_{ON(MIN)1,2}$	Minimum Top Gate On-Time	V_{IN} = 38V, V_{OUT} = 0.6V, R_T = 20k (Note 6)			30		ns
$t_{OFF(MIN)1,2}$	Minimum Top Gate Off-Time	(Note 6)			90		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 15V unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sensing							
$V_{SENSE(MAX)1,2}$	Maximum Valley Current Sense Threshold ($V_{SENSE1,2}^+ – V_{SENSE1,2}^–$)	V_{RNG} = 2V, V_{FB} = 0.57V, $V_{SENSE}^–$ = 2.5V V_{RNG} = 0V, V_{FB} = 0.57V, $V_{SENSE}^–$ = 2.5V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.57V, $V_{SENSE}^–$ = 2.5V	● ● ●	80 21 39	100 30 50	120 40 61	mV mV mV
$V_{SENSE(MIN)1,2}$	Minimum Valley Current Sense Threshold ($V_{SENSE1,2}^+ – V_{SENSE1,2}^–$) (Forced Continuous Mode)	V_{RNG} = 2V, V_{FB} = 0.63V, $V_{SENSE}^–$ = 2.5V V_{RNG} = 0V, V_{FB} = 0.63V, $V_{SENSE}^–$ = 2.5V V_{RNG} = $INTV_{CC}$, V_{FB} = 0.63V, $V_{SENSE}^–$ = 2.5V			–50 –15 –25		mV mV mV
$I_{SENSE1,2}^+$	SENSE1,2$^+$ Pins Input Bias Current	V_{SENSE}^+ = 0.6V V_{SENSE}^+ = 5V			±5 1	±50 ±2	nA µA
$I_{SENSE1,2}^–$	SENSE1,2$^–$ Pins Input Bias Current (Internal 500k Resistor to SGND)	$V_{SENSE}^–$ = 0.6V $V_{SENSE}^–$ = 5V			1.2 10		µA µA
Start-Up and Shutdown							
$V_{RUN1,2}$	RUN Pin On Threshold	$V_{RUN1,2}$ Rising	●	1.1	1.2	1.3	V
	RUN Pin On Hysteresis	$V_{RUN1,2}$ Falling from On Threshold			100		mV
$I_{RUN1,2}$	RUN Pin Pull-Up Current when Off	RUN1,2 = SGND			1.2		µA
	RUN Pin Pull-Up Current Hysteresis	$I_{RUN1,2(HYS)} = I_{RUN1,2(ON)} – I_{RUN1,2(OFF)}$			5		µA
UVLO	$INTV_{CC}$ Undervoltage Lockout	$INTV_{CC}$ Falling $INTV_{CC}$ Rising	● ●	3.3	3.7 4.2	 4.5	V V
$I_{TRACK/SS1,2}$	Soft-Start Pull-Up Current	0V < TRACK/SS1,2 < 0.6V			1		µA
Frequency and Clock Synchronization							
f	Clock Output Frequency (Steady-State Switching Frequency)	R_T = 205k R_T = 80.6k R_T = 18.2k		 450	200 500 2000	 550	kHz kHz kHz
	Channel 2 Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = $INTV_{CC}$			180 180 240		Deg Deg Deg
	CLKOUT Phase (Relative to Channel 1)	PHASMD = SGND PHASMD = Floating PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
$V_{PLLIN(H)}$	Clock Input High Level Into MODE/PLLIN			2			V
$V_{PLLIN(L)}$	Clock Input Low Level Into MODE/PLLIN					0.5	V
$R_{MODE/PLLIN}$	MODE/PLLIN Input DC Resistance	With Respect to SGND			600		kΩ
Gate Drivers							
$R_{TG(UP)1,2}$	TG Driver Pull-Up On Resistance	TG High			2.5		Ω
$R_{TG(DOWN)1,2}$	TG Driver Pull-Down On Resistance	TG Low			1.2		Ω
$R_{BG(UP)1,2}$	BG Driver Pull-Up On Resistance	BG High			2.5		Ω
$R_{BG(DOWN)1,2}$	BG Driver Pull-Down On Resistance	BG Low			0.8		Ω
$t_{D(TG/BG)1,2}$	Top Gate Off to Bottom Gate On Delay Time	(Note 6)			20		ns
$t_{D(BG/TG)1,2}$	Bottom Gate Off to Top Gate On Delay Time	(Note 6)			15		ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at $T_A = 25°C$. $V_{IN} = 15V$ unless otherwise noted (Note 3).

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Internal V_{CC} Regulator							
V_{DRVCC1}	Internally Regulated DRV_{CC1} Voltage	$6V < V_{IN} < 38V$		5.0	5.3	5.6	V
	DRV_{CC1} Load Regulation	I_{DRVCC1} = 0mA to –100mA			–1.5	–3	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Rising		4.4	4.6	4.8	V
	$EXTV_{CC}$ Switchover Hysteresis				200		mV
	$EXTV_{CC}$ to DRV_{CC2} Voltage Drop	V_{EXTVCC} = 5V, I_{DRVCC2} = –100mA			200		mV
PGood Output							
OV	PGOOD Overvoltage Threshold	$V_{FB1,2}$ Rising, with Respect to Regulated Voltage		5	7.5	10	%
UV	PGOOD Undervoltage Threshold	$V_{FB1,2}$ Falling, with Respect to Regulated Voltage		–5	–7.5	–10	%
	PGOOD Threshold Hysteresis	$V_{FB1,2}$ Returning to Reference Voltage			2		%
$V_{PGOOD(L)1,2}$	PGOOD Low Voltage	I_{PGOOD} = 2mA			0.1	0.3	V
$t_{D(PGOOD)1,2}$	Delay from V_{FB} Fault (OV/UV) to PGOOD Falling				50		μs
	Delay from V_{FB} Good to PGOOD Rising				20		μs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The junction temperature (T_J, in °C) is calculated from the ambient temperature (T_A, in °C) and power dissipation (P_D, in Watts) according to the formula:

$$T_J = T_A + (P_D \bullet \theta_{JA})$$

where θ_{JA} (in °C/W) is the package thermal impedance.

Note 3: The LTC3838 is tested under pulsed loading conditions such that $T_J \approx T_A$. The LTC3838E is guaranteed to meet specifications over the 0°C to 85°C operating junction temperature range. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3838I is guaranteed to meet specifications over the –40°C to 125°C operating junction temperature range . Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal impedance and other environmental factors.

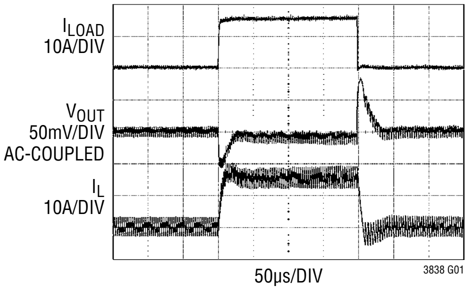
Note 4: This IC includes overtemperature protection that is intended to protect the device during momentary overload conditions. The maximum rated junction temperature will be exceeded when this protection is active. Continuous operation above the specified absolute maximum operating junction temperature may impair device reliability or permanently damage the device.

Note 5: The LTC3838 is tested in a feedback loop that adjusts ($V_{OUTSENSE1}^+ – V_{OUTSENSE1}^–$) or V_{FB2} to achieve specified error amplifier output voltages (ITH1,2).

Note 6: Delay times are measured with top gate (TG) and bottom gate (BG) driving minimum load, and using 50% levels.

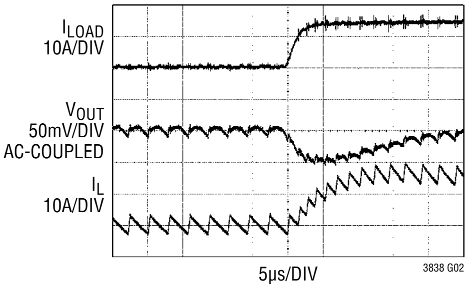
TYPICAL PERFORMANCE CHARACTERISTICS

Transient Response (Forced Continuous Mode)



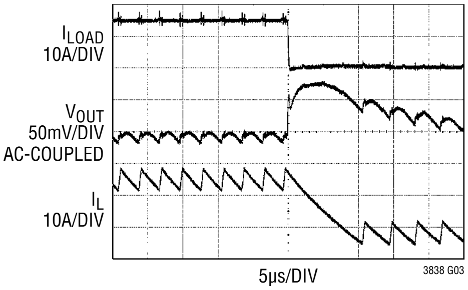
LOAD TRANSIENT = 0A TO 15A TO 0A
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Load Step (Forced Continuous Mode)



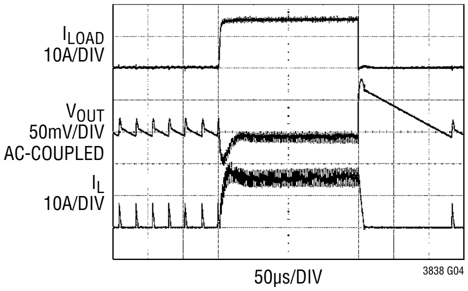
LOAD STEP = 0A TO 15A
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Load Release (Forced Continuous Mode)



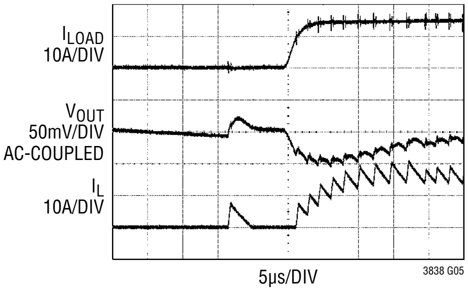
LOAD RELEASE = 15A TO 0A
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Transient Response (Discontinuous Mode)



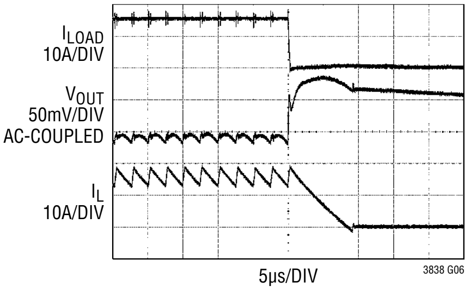
LOAD TRANSIENT = 500mA TO 15A TO 500mA
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Load Step (Discontinuous Mode)



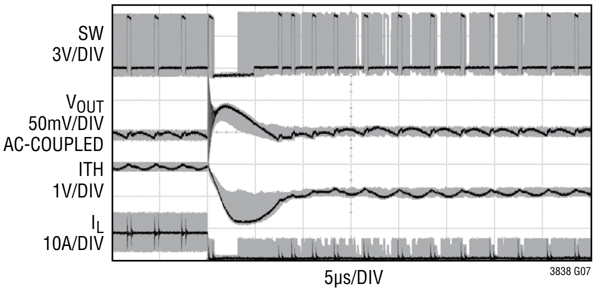
LOAD STEP = 500mA TO 15A
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Load Release (Discontinuous Mode)



LOAD RELEASE = 15A TO 500mA
V_{IN} = 12V
V_{OUT} = 1.2V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

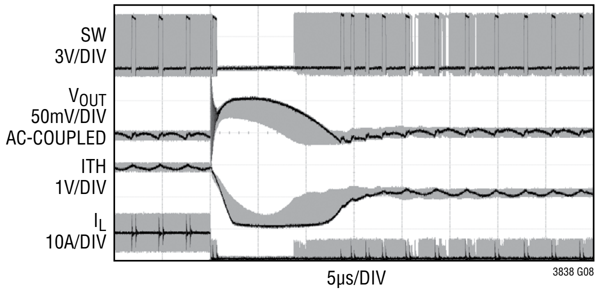
Load Release with Detect Transient (DTR) Feature Enabled



LOAD RELEASE = 15A TO 5A
V_{IN} = 5V
V_{OUT} = 0.6V

FIGURE 17 CIRCUIT, CHANNEL 1 MODIFIED:
R_{FB2} = 0Ω, V_{RNG2} = SGND, C_{ITH1} = 120pF, C_{ITH2} = 0pF,
FROM DTR1 PIN: R_{ITH1} = 46.4k TO SGND, R_{ITH2} = 42.2k TO $INTV_{CC}$

Load Release with Detect Transient (DTR) Feature Disabled

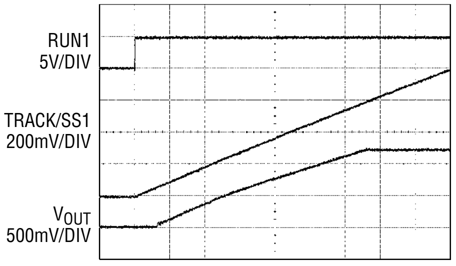


LOAD RELEASE = 15A TO 5A
V_{IN} = 5V
V_{OUT} = 0.6V

FIGURE 17 CIRCUIT, CHANNEL 1 MODIFIED:
R_{FB2} = 0Ω, V_{RNG2} = SGND, C_{ITH1} = 120pF, C_{ITH2} = 0pF,
$R_{ITH1/2}$ = 46.4k TO SGND//42.2k TO $INTV_{CC}$,
CONNECTION FROM $R_{ITH1/2}$ AND C_{ITH1} TO DTR1 PIN REMOVED.
DTR1 PIN TIED TO $INTV_{CC}$

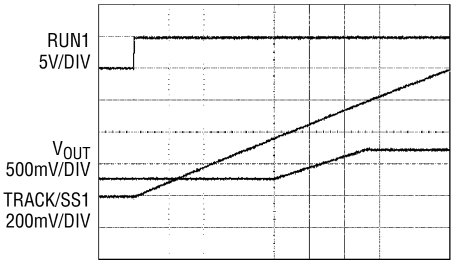
TYPICAL PERFORMANCE CHARACTERISTICS

Regular Soft Start-Up



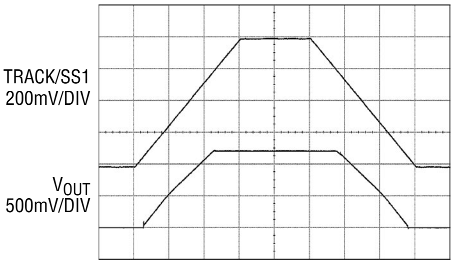
C_{SS} = 10nF 1ms/DIV
V_{IN} = 12V
V_{OUT} = 1.2V
FORCED CONTINUOUS MODE
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Soft Start-Up Into Pre-Biased Output



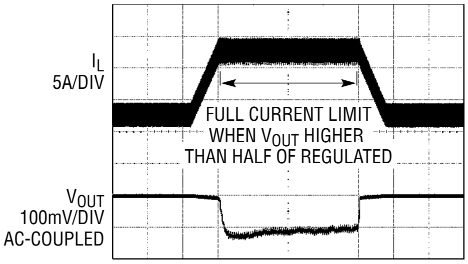
C_{SS} = 10nF 1ms/DIV
V_{IN} = 12V
V_{OUT} = 1.2V
V_{OUT} PRE-BIASED TO 0.75V
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Output Tracking



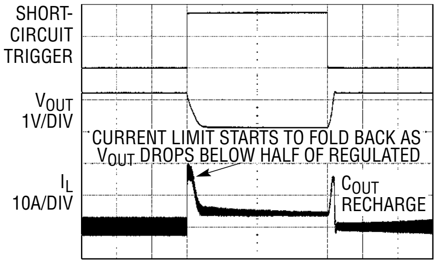
V_{IN} = 12V 10ms/DIV
V_{OUT} = 1.2V
FORCED CONTINUOUS MODE
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Overcurrent Protection



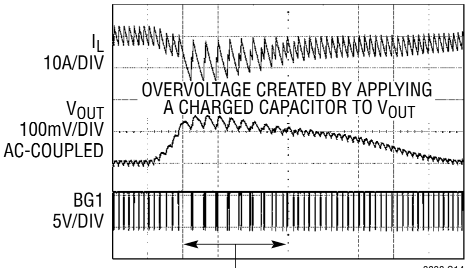
V_{IN} = 12V 5ms/DIV
V_{OUT} = 1.2V
FORCED CONTINUOUS MODE
CURRENT LIMIT = 17A
OVERLOAD = 7.5A TO 17.5A
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

Short-Circuit Protection



V_{IN} = 12V 500μs/DIV
V_{OUT} = 1.2V
I_{LOAD} = 0A
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

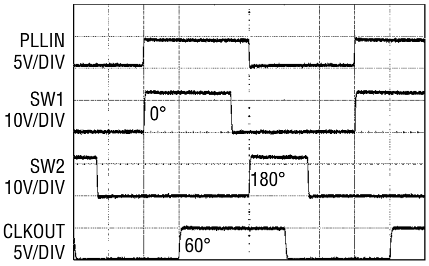
Overvoltage Protection



V_{IN} = 12V 20μs/DIV
V_{OUT} = 1.2V
FORCED CONTINUOUS
MODE
I_{LOAD} = 0A
FIGURE 17 CIRCUIT, CHANNEL 1, V_{RNG1} = SGND

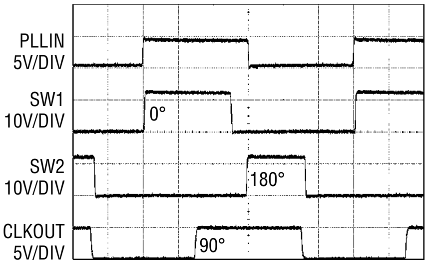
BG STAYS ON UNTIL
V_{OUT} IS PULLED
BELOW OVERVOLTAGE
THRESHOLD

**Phase Relationship:
PHASMD = Ground**



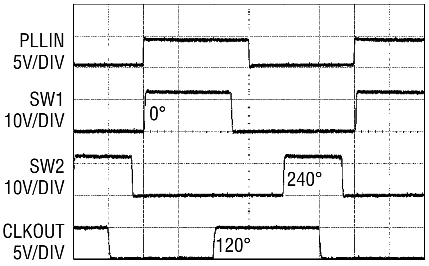
500ns/DIV
FIGURE 19 CIRCUIT
V_{IN} = 12V
V_{OUT1} = 5V, V_{OUT2} = 3.3V
LOAD = 0A
MODE/PLLIN = 333kHz EXTERNAL CLOCK

**Phase Relationship:
PHASMD = Float**



500ns/DIV
FIGURE 19 CIRCUIT
V_{IN} = 12V
V_{OUT1} = 5V, V_{OUT2} = 3.3V
LOAD = 0A
MODE/PLLIN = 333kHz EXTERNAL CLOCK

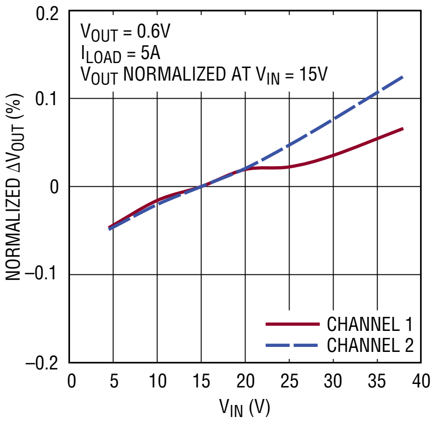
**Phase Relationship:
PHASMD = $INTV_{CC}$**



500ns/DIV
FIGURE 19 CIRCUIT
V_{IN} = 12V
V_{OUT1} = 5V, V_{OUT2} = 3.3V
LOAD = 0A
MODE/PLLIN = 333kHz EXTERNAL CLOCK

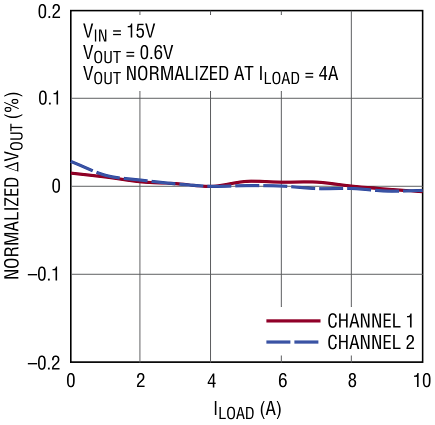
TYPICAL PERFORMANCE CHARACTERISTICS

Output Regulation vs Input Voltage



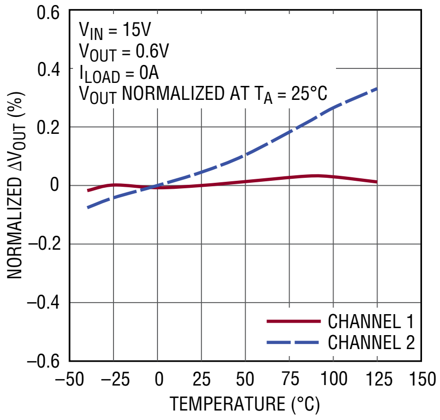
3838 G18

Output Regulation vs Load Current



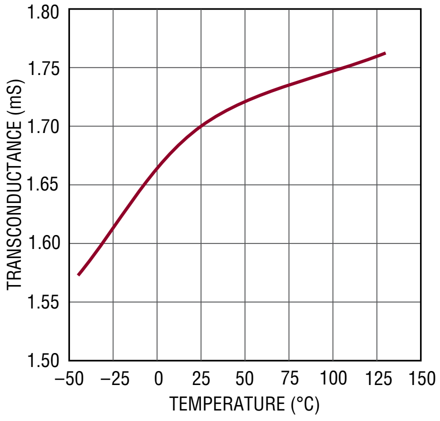
3838 G19

Output Regulation vs Temperature



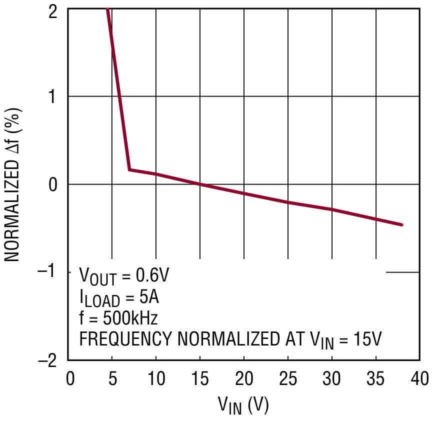
3838 G20

Error Amplifier Transconductance vs Temperature



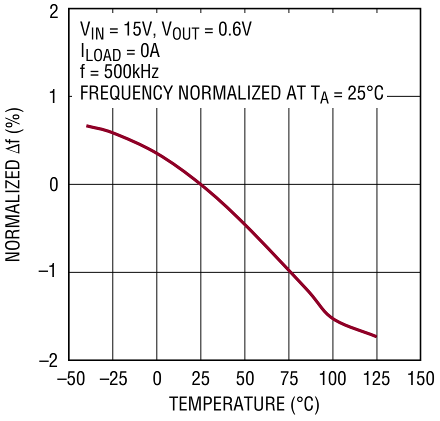
3838 G27

CLKOUT/Switching Frequency vs Input Voltage



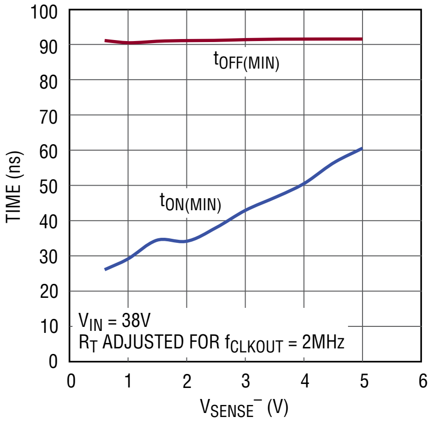
3838 G21

CLKOUT/Switching Frequency vs Temperature



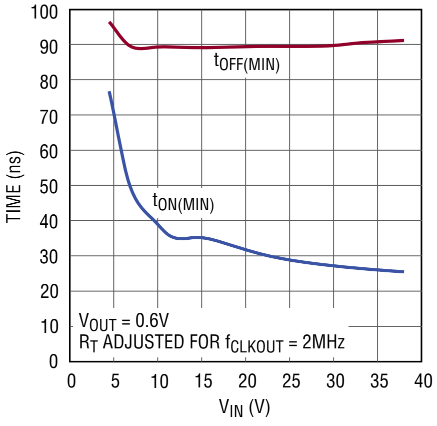
3838 G23

$t_{ON(MIN)}$ and $t_{OFF(MIN)}$ vs V_{OUT} (Voltage on $SENSE^-$ Pin)



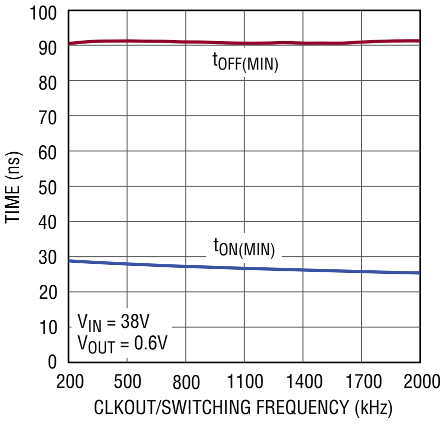
3838 G24

$t_{ON(MIN)}$ and $t_{OFF(MIN)}$ vs Voltage on V_{IN} Pin



3838 G25

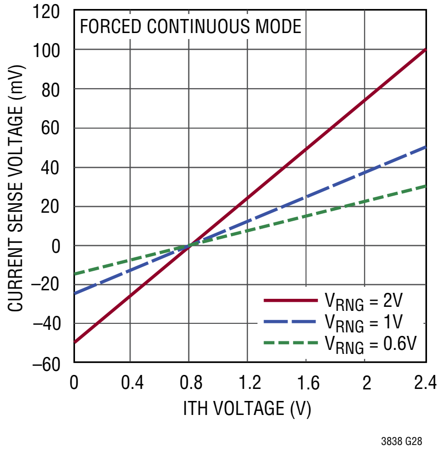
$t_{ON(MIN)}$ and $t_{OFF(MIN)}$ vs Switching Frequency



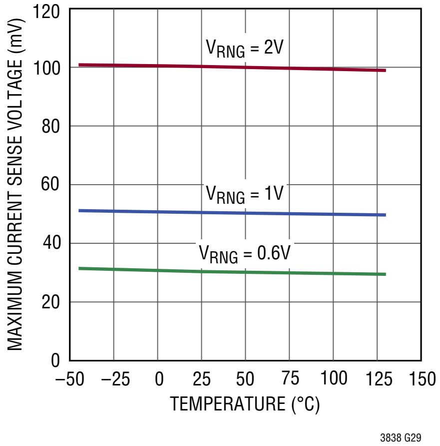
3838 G26

TYPICAL PERFORMANCE CHARACTERISTICS

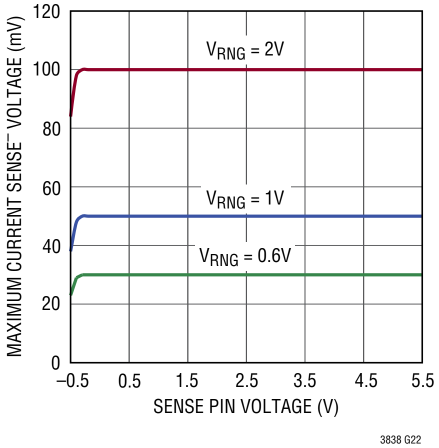
Current Sense Voltage vs ITH Voltage



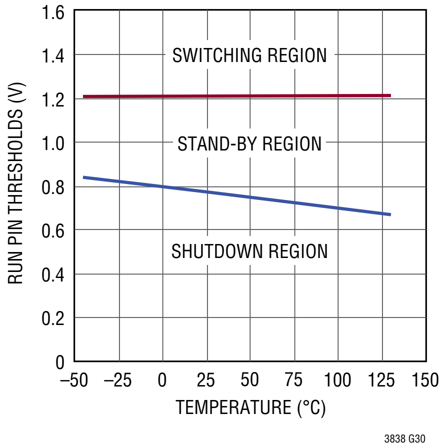
Maximum Current Sense Voltage vs Temperature



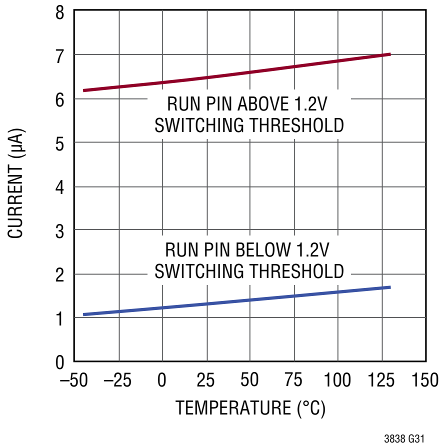
Maximum Current Sense Voltage vs Voltage on SENSE⁻ Pin



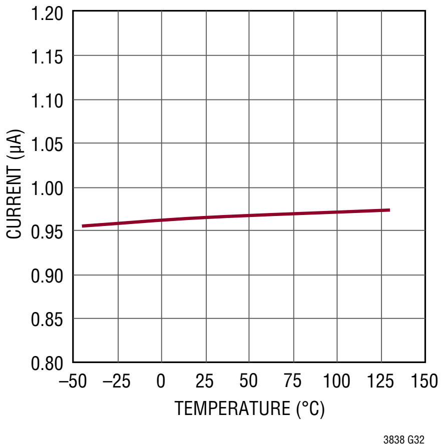
RUN Pin Thresholds vs Temperature



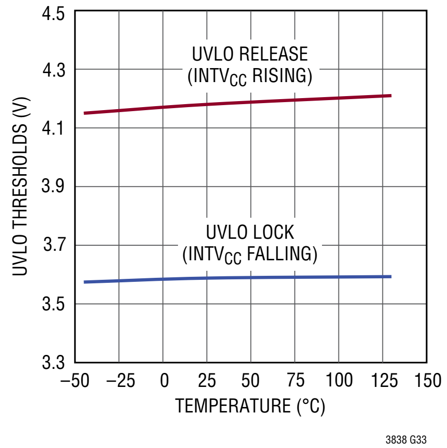
RUN Pull-Up Currents vs Temperature



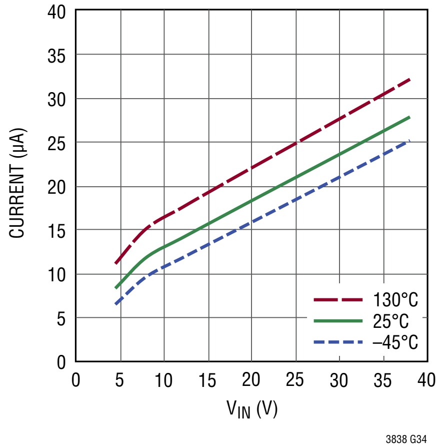
TRACK/SS Pull-Up Currents vs Temperature



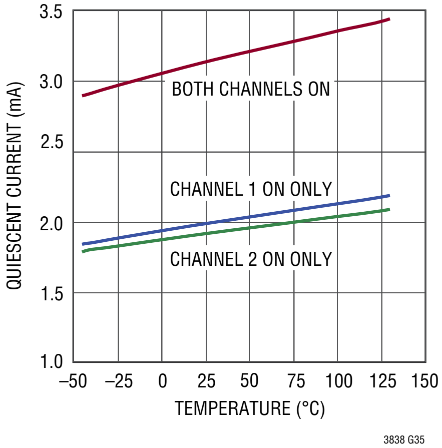
$INTV_{CC}$ Undervoltage Lockout Thresholds vs Temperature



Shutdown Current Into V_{IN} Pin vs Voltage on V_{IN} Pin



Quiescent Current Into V_{IN} Pin vs Temperature



PIN FUNCTIONS (QFN/TSSOP)

PHASMD (Pin 4/Pin 8): Phase Selector Input. This pin determines the relative phases of channels and the CLKOUT signal. With zero phase being defined as the rising edge of TG1: Pulling this pin to SGND locks TG2 to 180°, and CLKOUT to 60°. Connecting this pin to $INTV_{CC}$ locks TG2 to 240° and CLKOUT to 120°. Floating this pin locks TG2 to 180° and CLKOUT to 90°.

MODE/PLLIN (Pin 5/Pin 9): Operation Mode Selection or External Clock Synchronization Input. When this pin is tied to $INTV_{CC}$, forced continuous mode operation is selected. Tying this pin to SGND allows discontinuous mode operation. When an external clock is applied at this pin, both channels operate in forced continuous mode and synchronize to the external clock.

CLKOUT (Pin 6/Pin 10): Clock Output of Internal Clock Generator. Its output level swings between $INTV_{CC}$ and SGND. If clock input is present at the MODE/PLLIN pin, it will be synchronized to the input clock, with phase set by the PHASMD pin. If no clock is present at MODE/PLLIN, its frequency will be set by the RT pin. To synchronize other controllers, it can be connected to their MODE/PLLIN pins.

SGND (Pin 7/Pin 11): Signal Ground. All small-signal analog and compensation components should be connected to this ground. Connect SGND to the exposed pad and PGND pin using a single PCB trace.

RT (Pin 8/Pin 12): Clock Generator Frequency Programming Pin. Connect an external resistor from RT to SGND to program the switching frequency between 200kHz and 2MHz. An external clock applied to MODE/PLLIN should be within ±30% of this programmed frequency to ensure frequency lock. When the RT pin is floating, the frequency is internally set to be slightly under 200kHz.

V_{RNG1}, V_{RNG2} (Pins 9, 3/Pins 13, 7): Current Sense Voltage Range Inputs. When programmed between 0.6V and 2V, the voltage applied to $V_{RNG1,2}$ is twenty times (20×) the maximum sense voltage between $SENSE1,2^+$ and $SENSE1,2^-$, i.e., for either channel, $(V_{SENSE^+} – V_{SENSE^-}) = 0.05 \cdot V_{RNG}$. If a V_{RNG} is tied to SGND, the channel operates with a maximum sense voltage of 30mV, equivalent to a V_{RNG} of 0.6V; If tied to $INTV_{CC}$, a maximum sense voltage of 50mV, equivalent to a V_{RNG} of 1V.

ITH1, ITH2 (Pins 10, 2/Pins 14, 6): Current Control Threshold. This pin is the output of the error amplifier and the switching regulator's compensation point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V, with 0.8V corresponding to zero sense voltage (zero inductor valley current).

TRACK/SS1, TRACK/SS2 (Pins 11, 1/Pins 15, 5): External Tracking and Soft-Start Input. The LTC3838 regulates the feedback voltages $(V_{OUTSENSE1}{}^+ – V_{OUTSENSE1}{}^-)$ and V_{FB2} to the smaller of 0.6V or the voltage on the TRACK/SS1,2 pins respectively. An internal 1μA temperature-independent pull-up current source is connected to each TRACK/SS pin. A capacitor to ground at this pin sets the ramp time to the final regulated output voltage. Alternatively, another voltage supply connected to this pin allows the output to track the other supply during start-up.

$V_{OUTSENSE1}{}^+$ (Pin 12/Pin 16): Differential Output Sense Amplifier (+) Input of Channel 1. Connect this pin to a feedback resistor divider between the positive and negative output capacitor terminals of V_{OUT1}. In nominal operation the LTC3838 will attempt to regulate the differential output voltage V_{OUT1} to 0.6V divided by the feedback resistor divider ratio.

PIN FUNCTIONS (QFN/TSSOP)

$V_{OUTSENSE1}^-$ (Pin 13/Pin 17): Differential Output Sense Amplifier (–) Input of Channel 1. Connect this pin to the negative terminal of the output load capacitor of V_{OUT1}.

SENSE1$^+$, SENSE2$^+$ (Pins 14, 37/Pins 18, 3): Differential Current Sense Comparator (+) Inputs. The ITH pin voltage and controlled offsets between the SENSE$^+$ and SENSE$^-$ pins set the current trip threshold. The comparator can be used for R_{SENSE} sensing or inductor DCR sensing. For R_{SENSE} sensing, Kelvin (4-wire) connect the SENSE$^+$ pin to the (+) terminal of R_{SENSE}. For DCR sensing, tie the SENSE$^+$ pins to the connection between the DCR sense capacitor and sense resistor tied across the inductor.

SENSE1$^-$, SENSE2$^-$ (Pins 15, 36/Pins 19, 2): Differential Current Sense Comparator (–) Input. The comparator can be used for R_{SENSE} sensing or inductor DCR sensing. For R_{SENSE} sensing, Kelvin (4-wire) connect the SENSE$^-$ pin to the (–) terminal of R_{SENSE}. For DCR sensing, tie the SENSE$^-$ pin to the DCR sense capacitor tied to the inductor V_{OUT} node connection. These pins also function as output voltage sense pins for the top MOSFET on-time adjustment. The impedance looking into these pins is different from the SENSE$^+$ pins because there is an additional 500k internal resistor from each of the SENSE$^-$ pins to SGND.

DTR1, DTR2 (Pins 16, 35/Pins 20, 1): Detect Load-Release Transient for Overshoot Reduction. When load current suddenly drops, if voltage on this DTR pin drops below half of $INTV_{CC}$, the bottom gate (BG) could turn off, allowing the inductor current to drop to zero faster, thus reducing the V_{OUT} overshoot. (Refer to Load-Release Transient Detection in the Applications Information section for more details.) An internal 2.5µA current source pulls this pin toward $INTV_{CC}$. To disable the DTR feature, simply tie the DTR pin to $INTV_{CC}$.

RUN1, RUN2 (Pins 17, 34/Pins 21, 38): Run Control Inputs. An internal proportional-to-absolute-temperature (PTAT) pull-up current source (~1.2µA at 25°C) is constantly connected to this pin. Taking both RUN1 and RUN2 pins below a threshold voltage (~0.8V at 25°C) shuts down all bias of $INTV_{CC}$ and DRV_{CC} and places the LTC3838 into micropower shutdown mode. Allowing either RUN pin to rise above this threshold would turn on the internal bias supply and the circuitry for the particular channel. When a RUN pin rises above 1.2V, its corresponding channel's TG and BG drivers are turned on and an additional 5µA temperature-independent pull-up current is connected internally to the RUN pin. Either RUN pin can sink up to 50µA, or be forced no higher than 6V.

PGOOD1, PGOOD2 (Pins 18, 33/Pins 22, 37): Power Good Indicator Outputs. This open-drain logic output is pulled to ground when the output voltage goes out of a ±7.5% window around the regulation point, after a 50µs power-bad-masking delay. Returning to the regulation point, there is a much shorter delay to power good, and a hysteresis of around 2% on both sides of the voltage window.

BOOST1, BOOST2 (Pins 19, 32/Pins 23, 36): Boosted Floating Supplies for Top MOSFET Drivers. The (+) terminal of the bootstrap capacitor, C_B, connects to this pin. The BOOST pins swing by a V_{IN} between a diode drop below DRV_{CC}, or ($DRV_{CC} - V_D$) and ($V_{IN} + DRV_{CC} - V_D$).

TG1, TG2 (Pins 20, 31/Pins 24, 35): Top Gate Driver Outputs. The TG pins drive the gates of the top N-channel power MOSFET with a voltage swing of V_{DRVCC} between SW and BOOST.

PIN FUNCTIONS (QFN/TSSOP)

SW1, SW2 (Pins 21, 30/Pins 25, 34): Switch Node Connection to Inductors. Voltage swings are from a diode voltage below ground to V_{IN}. The (–) terminal of the bootstrap capacitor, C_B, connects to this node.

BG1, BG2 (Pins 22, 29/Pins 26, 33): Bottom Gate Driver Outputs. The BG pins drive the gates of the bottom N-channel power MOSFET between PGND and DRV_{CC}.

DRV_{CC1}, DRV_{CC2} (Pins 23, 28/Pins 27, 32): Supplies of Bottom Gate Drivers. DRV_{CC1} is also the output of an internal 5.3V regulator. DRV_{CC2} is also the output of the $EXTV_{CC}$ switch. Normally the two DRV_{CC} pins are shorted together on the PCB, and decoupled to PGND with a minimum of 4.7µF ceramic capacitor, C_{DRVCC}.

V_{IN} (Pin 24/Pin 28): Input Voltage Supply. The supply voltage can range from 4.5V to 38V. For increased noise immunity decouple this pin to SGND with an RC filter. Voltage at this pin is also used to adjust top gate on-time, therefore it is recommended to tie this pin to the main power input supply through an RC filter.

PGND (Pin 25, Exposed Pad Pin 39/Pin 29, Exposed Pad Pin 39): Power Ground. Connect this pin as close as practical to the source of the bottom N-channel power MOSFET, the (–) terminal of C_{DRVCC} and the (–) terminal of C_{IN}. Connect the exposed pad and PGND pin to SGND pin using a single PCB trace under the IC. The exposed pad must be soldered to the circuit board for electrical and rated thermal performance.

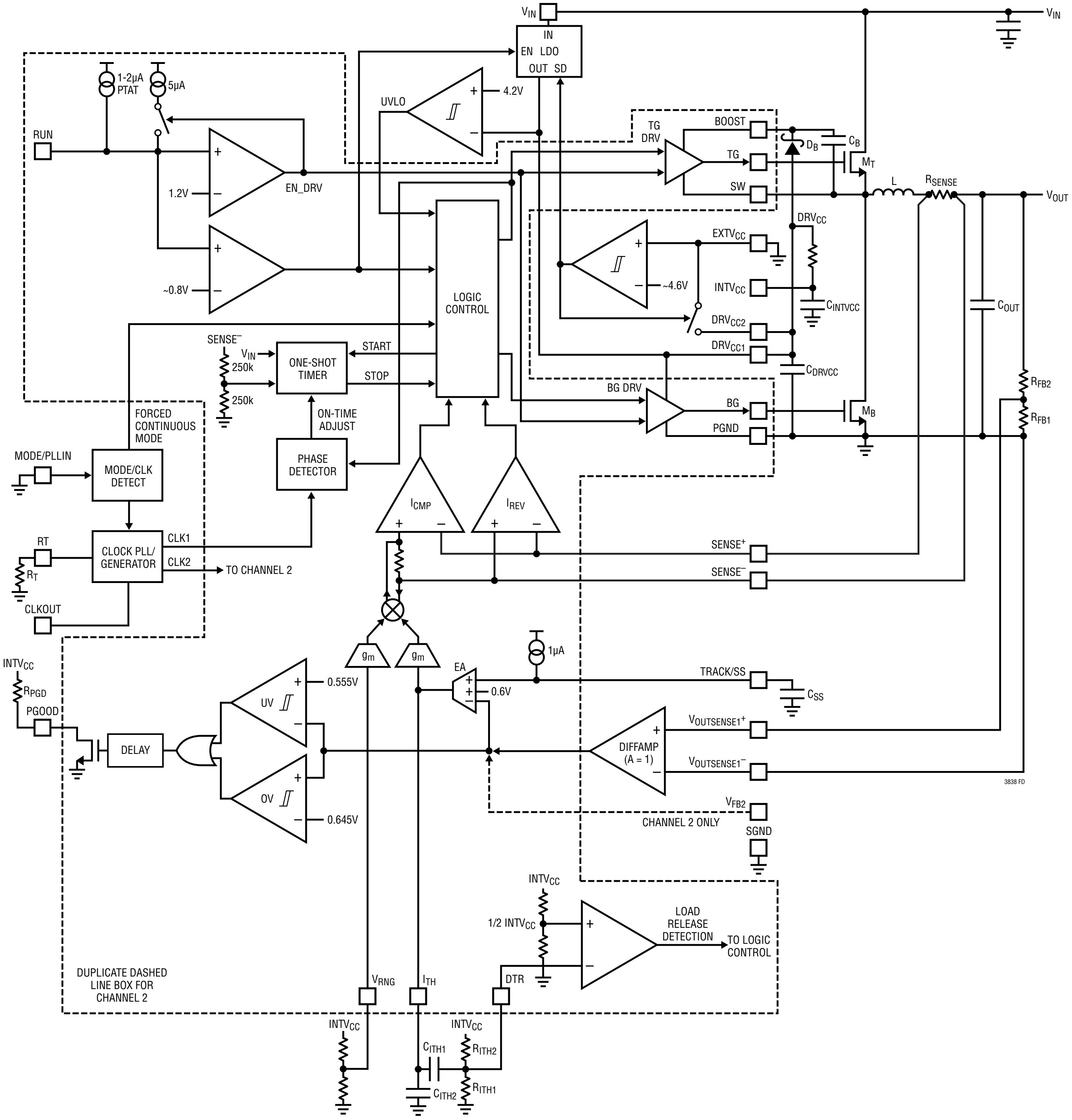
$INTV_{CC}$ (Pin 26/Pin 30): Supply Input for Internal Circuitry (Not Including Gate Drivers). Normally powered from the DRV_{CC} pins through a decoupling RC filter to SGND (typically 2Ω and 1µF).

$EXTV_{CC}$ (Pin 27/Pin 31): External Power Input. When $EXTV_{CC}$ exceeds the switchover voltage (typically 4.6V), an internal switch connects this pin to DRV_{CC2} and shuts down the internal regulator so that $INTV_{CC}$ and gate drivers draw power from $EXTV_{CC}$. The V_{IN} pin still needs to be powered up but draws minimum current.

V_{FB2} (Pin 38/Pin 4): Error Amplifier Feedback Input for Channel 2. This pin connects the error amplifier to an external feedback resistor divider from V_{OUT2}. In nominal operation the LTC3838 will attempt to regulate the V_{OUT2} to 0.6V divided by the feedback resistor divider ratio.

Shorting this pin to $INTV_{CC}$ will disable Channel 2's error amplifier, and internally connect ITH2 to ITH1. (As a result, TRACK/SS2 is no longer functional and PGOOD2 is always pulling low.) By doing so, this part can function as a dual phase, single V_{OUT} step-down controller, and the two channels use a *single* Channel 1's error amplifier for the ITH output and compensation.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3838 is a controlled on-time, valley current mode step-down DC/DC dual controller with two channels operating out of phase. Each channel drives both main and synchronous N-channel MOSFETs. The two channels can be either configured to two independently regulated outputs, or combined into a single output.

The top MOSFET is turned on for a time interval determined by a one-shot timer. The duration of the one-shot timer is controlled to maintain a fixed switching frequency. As the top MOSFET is turned off, the bottom MOSFET is turned on after a small delay. The delay, or dead time, is to avoid both top and bottom MOSFETs being on at the same time, causing shoot-through current from V_{IN} directly to power ground. The next switching cycle is initiated when the current comparator, I_{CMP}, senses that inductor current falls below the trip level set by voltages at the ITH and V_{RNG} pins. The bottom MOSFET is turned off immediately and the top MOSFET on again, restarting the one-shot timer and repeating the cycle. In order to avoid shoot-through current, there is also a small dead-time delay before the top MOSFET turns on. At this moment, the inductor current hits its "valley" and starts to rise again.

Inductor current is determined by sensing the voltage between $SENSE^+$ and $SENSE^-$, either by using an explicit resistor connected in series with the inductor or by implicitly sensing the inductor's DC resistive (DCR) voltage drop through an RC filter connected across the inductor. The trip level of the current comparator, I_{CMP}, is proportional to the voltage at the ITH pin, with a zero-current threshold corresponding to an ITH voltage of around 0.8V.

The error amplifier (EA) adjusts this ITH voltage by comparing the feedback signal to the internal 0.6V reference voltage. On Channel 1, the difference amplifier (DIFFAMP) converts the differential feedback signal ($V_{OUTSENSE1}^+$ – $V_{OUTSENSE1}^-$) to a single-ended input for the EA; Channel 2 uses V_{FB2} directly with respect to SGND. Output voltage is regulated so that the feedback voltage is equal to the internal 0.6V reference. If the load current increases/decreases, it causes a momentary drop/rise in the differential feedback voltage relative to the reference. The EA then moves ITH voltage, or inductor valley current setpoint, higher/lower until the average inductor current again matches the load current, so that the output voltage comes back to the regulated voltage.

The LTC3838 features a detect transient (DTR) pin to detect "load-release", or a transient where the load current suddenly drops, by monitoring the first derivative of the ITH voltage. When detected, the bottom gate (BG) is turned off and inductor current flows through the body diode in the bottom MOSFET, allowing the SW node voltage to drop below PGND by the body diode's forward-conduction voltage. This creates a more negative differential voltage (V_{SW} – V_{OUT}) across the inductor, allowing the inductor current to drop faster to zero, thus creating less overshoot on V_{OUT}. See Load-Release Transient Detection in Applications Information for details.

Differential Output Sensing

This dual controller's first channel features differential output voltage sensing. The output voltage is resistively divided externally to create a feedback voltage for the controller. The internal difference amplifier (DIFFAMP) senses this feedback voltage with respect to the output's remote ground reference to create a differential feedback voltage. This scheme eliminates any ground offsets between local ground and remote output ground, resulting in a more accurate output voltage. Channel 1 allows remote output ground to deviate as much as ±500mV with respect to local ground (SGND).

DRV_{CC}/$EXTV_{CC}$/$INTV_{CC}$ Power

$DRV_{CC1,2}$ are the power for the bottom MOSFET drivers. Normally the two DRV_{CC} pins are shorted together on the PCB, and decoupled to PGND with a minimum 4.7µF ceramic capacitor, C_{DRVCC}. The top MOSFET drivers are biased from the floating bootstrap capacitors ($C_{B1,2}$) which are recharged during each cycle through an external Schottky diode when the top MOSFET turns off and the SW pin swings down.

The DRV_{CC} can be powered on two ways: an internal low-dropout (LDO) linear voltage regulator that is powered

OPERATION (Refer to Functional Diagram)

from V_{IN} and can output 5.3V to DRV_{CC1}. Alternatively, an internal $EXTV_{CC}$ switch (with on-resistance of around 2Ω) can short the $EXTV_{CC}$ pin to DRV_{CC2}.

If the $EXTV_{CC}$ pin is below the $EXTV_{CC}$ switchover voltage (typically 4.6V with 200mV hysteresis, see the Electrical Characteristics Table), then the internal 5.3V LDO is enabled. If the $EXTV_{CC}$ pin is tied to an external voltage source greater than this $EXTV_{CC}$ switchover voltage, then the LDO is shut down and the internal $EXTV_{CC}$ switch shorts the $EXTV_{CC}$ pin to the DRV_{CC2} pin, thereby powering DRV_{CC} and $INTV_{CC}$ with the external voltage source and helping to increase overall efficiency and decrease internal self heating from power dissipated in the LDO. This external power source could be the output of the step-down converter itself (if the output is programmed to higher than the switchover voltage's higher limit, 4.8V). The V_{IN} pin still needs to be powered up but now draws minimum current.

Power for most internal control circuitry other than gate drivers is derived from the $INTV_{CC}$ pin. $INTV_{CC}$ can be powered from the combined DRV_{CC} pins through an external RC filter to SGND to filter out noises due to switching.

Shutdown and Start-Up

Each of the RUN1 and RUN2 pins has an internal proportional-to-absolute-temperature (PTAT) current source (around 1.2µA at 25°C) to pull up the pins. Taking both RUN1 and RUN2 pins below a certain threshold voltage (around 0.8V at 25°C) shuts down all bias of $INTV_{CC}$ and DRV_{CC} and places the LTC3838 into micropower shutdown mode with a minimum I_Q at the V_{IN} pin. The LTC3838's DRV_{CC} (through the internal 5.3V LDO regulator or $EXTV_{CC}$) and the corresponding channel's internal circuitry off $INTV_{CC}$ will be biased up when either or both RUN pins are pulled up above the 0.8V threshold, either by the internal pull-up current or driven directly by external voltage source such as logic gate output.

A channel of the LTC3838 will not start switching until the RUN pin of the respective channel is pulled up to 1.2V. When a RUN pin rises above 1.2V, the corresponding channel's TG and BG drivers are enabled, and TRACK/SS released. An additional 5µA temperature-independent pull-up current is connected internally to the channel's respective RUN pin. To turn off TG, BG and the additional 5µA pull-up current, RUN needs to be pulled down below 1.2V by about 100mV. These built-in current and voltage hystereses prevent false jittery turn-on and turn-off due to noise. Such features on the RUN pins allow input undervoltage lockout (UVLO) to be set up using external voltage dividers from V_{IN}.

The start-up of a channel's output voltage (V_{OUT}) is controlled by the voltage on its TRACK/SS pin. When the voltage on the TRACK/SS pin is less than the 0.6V internal reference, the (differential) feedback voltage is regulated to the TRACK/SS voltage instead of the 0.6V reference. The TRACK/SS pin can be used to program the output voltage soft-start ramp-up time by connecting an external capacitor from a TRACK/SS pin to signal ground. An internal temperature-independent 1µA pull-up current charges this capacitor, creating a voltage ramp on the TRACK/SS pin. As the TRACK/SS voltage rises linearly from ground to 0.6V, the switching starts, V_{OUT} ramps up smoothly to its final value and the feedback voltage to 0.6V. TRACK/SS will keep rising beyond 0.6V, until being clamped to around 3.7V.

Alternatively, the TRACK/SS pin can be used to track an external supply like in a master slave configuration. Typically, this requires connecting a resistor divider from the master supply to the TRACK/SS pin (see the Applications Information section).

TRACK/SS is pulled low internally when the corresponding channel's RUN pin is pulled below the 1.2V threshold (hysteresis applies), or when $INTV_{CC}$ or either of the $DRV_{CC1,2}$ pins drop below their respective undervoltage lockout (UVLO) thresholds.

Light Load Current Operation

If the MODE/PLLIN pin is tied to $INTV_{CC}$ or an external clock is applied to MODE/PLLIN, the LTC3838 will be forced to operate in continuous mode. With load current less than one-half of the full load peak-to-peak ripple, the inductor current valley can drop to zero or become negative. This allows constant-frequency operation but at the cost of low efficiency at light loads.

OPERATION (Refer to Functional Diagram)

If the MODE/PLLIN pin is left open or connected to signal ground, the channel will transition into discontinuous mode operation, where a current reversal comparator (I_{REV}) shuts off the bottom MOSFET (M_B) as the inductor current approaches zero, thus preventing negative inductor current and improving light-load efficiency. In this mode, both switches can remain off for extended periods of time. As the output capacitor discharges by load current and the output voltage droops lower, EA will eventually move the ITH voltage above the zero current level (0.8V) to initiate another switching cycle.

Power Good and Fault Protection

Each PGOOD pin is connected to an internal open-drain N-channel MOSFET. An external resistor or current source can be used to pull this pin up to 6V (e.g., $V_{OUT1,2}$ or DRV_{CC}). Overvoltage or undervoltage comparators (OV, UV) turn on the MOSFET and pull the PGOOD pin low when the feedback voltage is outside the ±7.5% window of the 0.6V reference voltage. The PGOOD pin is also pulled low when the channel's RUN pin is below the 1.2V threshold (hysteresis applies), or in undervoltage lockout (UVLO). Note that feedback voltage of Channel 1 is sensed differentially through $V_{OUTSENSE1}^+$ with respect to $V_{OUTSENSE1}^-$, while Channel 2 is sensed through V_{FB2} with respect to SGND.

When the feedback voltage is within the ±7.5% window, the open-drain NMOS is turned off and the pin is pulled up by the external source. The PGOOD pin will indicate power good immediately after the feedback is within the window. But when a feedback voltage of a channel goes out of the window, there is an internal 50µs delay before its PGOOD is pulled low. In an overvoltage (OV) condition, M_T is turned off and M_B is turned on immediately without delay and held on until the overvoltage condition clears.

Foldback current limiting is provided if the output is below one-half of the regulated voltage, such as being shorted to ground. As the feedback approaches 0V, the internal clamp voltage for the ITH pin drops from 2.4V to around 1.27V, which reduces the inductor valley current level to about 30% of its maximum value. Foldback current limiting is disabled at start-up.

Frequency Selection and External Clock Synchronization

An internal oscillator (clock generator) provides phase-interleaved internal clock signals for individual channels to lock up to. The switching frequency and phase of each switching channel is independently controlled by adjusting the top MOSFET turn-on time (on-time) through the one-shot timer. This is achieved by sensing the phase relationship between a top MOSFET turn-on signal and its internal reference clock through a phase detector, and the time interval of the one-shot timer is adjusted on a cycle-by-cycle basis, so that the rising edge of the top MOSFET turn-on is always trying to synchronize to the internal reference clock signal for the respective channel.

The frequency of the internal oscillator can be programmed from 200kHz to 2MHz by connecting a resistor, R_T, from the RT pin to signal ground (SGND). The RT pin is regulated to 1.2V internally.

For applications with stringent frequency or interference requirements, an external clock source connected to the MODE/PLLIN pin can be used to synchronize the internal clock signals through a clock phase-locked loop (Clock PLL). The LTC3838 operates in forced continuous mode of operation when it is synchronized to the external clock. The external clock frequency has to be within ±30% of the internal oscillator frequency for successful synchronization. The clock input levels should be no less than 2V for "high" and no greater than 0.5V for "low". The MODE/PLLIN pin has an internal 600k pull-down resistor.

Multichip Operations

The PHASMD pin determines the relative phases between the internal reference clock signals for the two channels as well as the CLKOUT signal, as shown in Table 2. The phases tabulated are relative to zero degree (0°) being defined as the rising edge of the internal reference clock signal of Channel 1. The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding either a single high current output, or separate outputs.

OPERATION (Refer to Functional Diagram)

The system can be configured for up to 12-phase operation with a multichip solution. Typical configurations are shown in Table 3 to interleave the phases of the channels.

Table 2

PHASMD	SGND	FLOAT	$INTV_{CC}$
Channel 1	0°	0°	0°
Channel 2	180°	180°	240°
CLKOUT	60°	90°	120°

Table 3

NUMBER OF PHASES	NUMBER OF LTC3838	PIN CONNECTIONS [PIN NAME (CHIP NUMBER)]
2	1	PHASMD(1) = FLOAT or SGND
3	2, or 1 + LTC3833	PHASMD(1) = $INTV_{CC}$ MODE/PLLIN(2) = CLKOUT(1)
4	2	PHASMD(1) = FLOAT PHASMD(2) = FLOAT or SGND MODE/PLLIN(2) = CLKOUT(1)
6	3	PHASMD(1) = SGND PHASMD(2) = SGND MODE/PLLIN(2) = CLKOUT(1) PHASMD(3) = FLOAT or SGND MODE/PLLIN(3) = CLKOUT(2)
12	6	PHASMD(1) = SGND PHASMD(2) = SGND MODE/PLLIN(2) = CLKOUT(1) PHASMD(3) = FLOAT MODE/PLLIN(3) = CLKOUT(2) PHASMD(4) = SGND MODE/PLLIN(4) = CLKOUT(3) PHASMD(5) = SGND MODE/PLLIN(5) = CLKOUT(4) PHASMD(6) = FLOAT or SGND MODE/PLLIN(6) = CLKOUT(5)

Single-Output PolyPhase Configurations

To use LTC3838 for a 2-phase single output step-down controller: Tie the V_{FB2} pin to $INTV_{CC}$, which will disable Channel 2's error amplifier and internally connect ITH2 to ITH1. Tie the compensation R-C components to the ITH1 pin. The ITH2 pin can be either left open or shorted to ITH1 externally. The TRACK/SS2 and PGOOD2 pins become defunct and can be left open. Note that the RUN1, RUN2, DTR1, DTR2, VRNG1 and VRNG2 pins still function for the two channels individually, therefore should be shorted externally for single-output applications. Set PHASMD to SGND or FLOAT so that the two channels are 180° out-of-phase. Efficiency losses may be substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A 2-phase implementation can reduce the input path power loss by up to 75%.

To make a single-output converter of three or more phases, additional LTC3838 or LTC3833 chips can be used. The first chip should be tied the same way as the 2-phase above. If only one more channel of an additional LTC3838 is needed, use Channel 1 for the additional phase:

- Tie the ITH1 pin to the ITH1 pin of the first chip
- Tie the RUN1 pin to the RUN pins of the first chip
- Tie the $V_{OUTSENSE1}^+$ pin to the $V_{OUTSENSE1}^+$ pin of the first chip
- Tie the $V_{OUTSENSE1}^-$ pin to the $V_{OUTSENSE1}^-$ pin of the first chip
- Tie the TRACK/SS1 pin to the TRACK/SS1 pin of the first chip

If both channels are needed, the additional LTC3838 chip should be tied the same way as the first LTC3838 chip to disable the second channel's EA:

- Tie the V_{FB2} pin to the chip's own $INTV_{CC}$
- Tie the ITH1 pin to the ITH1 pin of the first chip
- Tie the RUN pins to the RUN pins of the first chip
- Tie the $V_{OUTSENSE1}^+$ pin to the $V_{OUTSENSE1}^+$ pin of the first chip
- Tie the $V_{OUTSENSE1}^-$ pin to the $V_{OUTSENSE1}^-$ pin of the first chip
- Tie the TRACK/SS1 pin to the TRACK/SS1 pin of the first chip

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Once the required output voltage and operating frequency have been determined, external component selection is driven by load requirement, and begins with the selection of inductors and current sense method (either sense resistors R_{SENSE} or inductor DCR sensing). Next, power MOSFETs are selected. Finally, input and output capacitors are selected.

Output Voltage Programming

As shown in Figure 1, external resistor dividers are used from the regulated outputs to their respective ground references to program the output voltages. On Channel 1, the resistive divider is tapped by the $V_{OUTSENSE1}^+$ pin, and the ground reference is remotely sensed by the $V_{OUTSENSE1}^-$ pin, this voltage is sensed differentially. On Channel 2, the resistive divider is tapped by the V_{FB2} pin, with respect to signal ground at the SGND pin. By regulating the tapped (differential) feedback voltages to the internal reference 0.6V, the resulting output voltages are:

$$V_{OUT1} – V_{OUTSENSE1}^- = 0.6V \bullet (1 + R_{FB2}/R_{FB1})$$

and

$$V_{OUT2} = 0.6V \bullet (1 + R_{FB2}/R_{FB1})$$

For example, if V_{OUT1} is programmed to 5V and the output ground reference is sitting at –0.5V with respect to SGND, then the absolute value of the output will be 4.5V with respect to SGND. The minimum (differential) output voltages are limited to the internal reference 0.6V, and the maximum are 5.5V.

The $V_{OUTSENSE1}^+$ pin is a high impedance pin with no input bias current other than leakage in the nA range. The $V_{OUTSENSE1}^-$ pin has about 30µA of current flowing out of the pin. The V_{FB2} pin is quasi-high impedance pin with minimum bias current out of the pin.

Differential output sensing allows for more accurate output regulation in high power distributed systems having large line losses. Figure 2 illustrates the potential variations in the power and ground lines due to parasitic elements. The variations may be exacerbated in multi-application systems with shared ground planes. Without differential output sensing, these variations directly reflect as an error in the regulated output voltage. The LTC3838 Channel 1's differential output sensing can correct for up to ±500mV of variation in the output's power and ground lines.

The LTC3838 Channel 1's differential output sensing scheme is distinct from conventional schemes where the regulated output and its ground reference are directly sensed with a difference amplifier whose output is then divided down with an external resistor divider and fed into the error amplifier input. This conventional scheme is limited by the common mode input range of the difference amplifier and typically limits differential sensing to the lower range of output voltages.

The LTC3838's Channel 1 allows for seamless differential output sensing by sensing the resistively divided feedback voltage differentially. This allows for differential sensing in the full output range from 0.6V to 5.5V. The difference amplifier (DIFFAMP) has a bandwidth of 8MHz, high

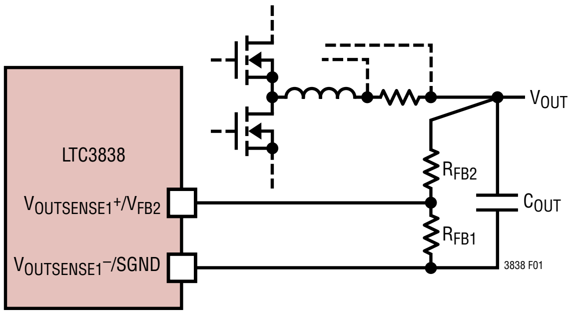

Figure 1. Setting Output Voltage

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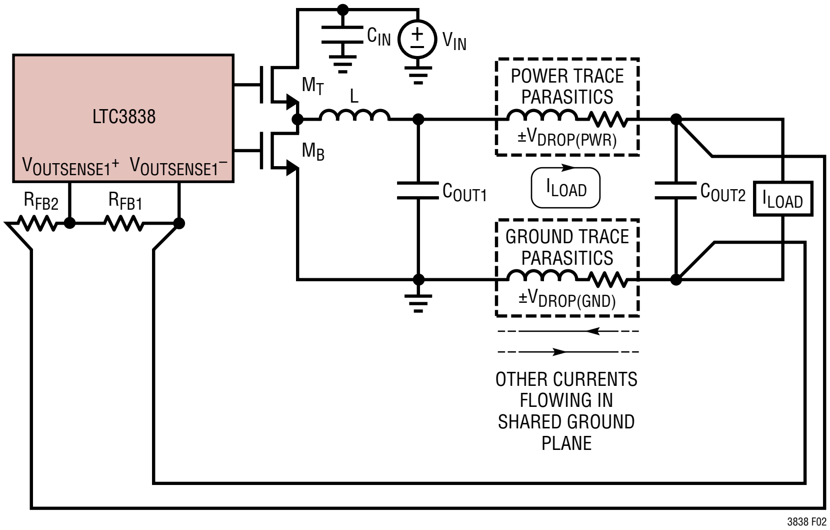

Figure 2. Differential Output Sensing Used to Correct Line Loss Variations in a High Power Distributed System with a Shared Ground Plane

enough so that it will not affect main loop compensation and transient behavior.

To avoid noise coupling into the feedback voltages ($V_{OUTSENSE1}$+ or V_{FB2}), the resistor dividers should be placed close to the $V_{OUTSENSE1}^+$ and $V_{OUTSENSE1}^-$, or V_{FB2} and SGND pins. Remote output and ground traces should be routed together as a differential pair to the remote output. For best accuracy, these traces to the remote output and ground should be connected as close as possible to the desired regulation point.

Switching Frequency Programming

The choice of operating frequency is a trade-off between efficiency and component size. Lowering the operating frequency improves efficiency by reducing MOSFET switching losses but requires larger inductance and/or capacitance to maintain low output ripple voltage. Conversely, raising the operating frequency degrades efficiency but reduces component size.

The switching frequency of the LTC3838 can be programmed from 200kHz to 2MHz by connecting a resistor from the RT pin to signal ground. The value of this resistor can be chosen according to the following formula:

$$R_T\,[k\Omega] = \frac{41550}{f\,[kHz]} - 2.2$$

The overall controller system, including the clock PLL and switching channels, has a synchronization range of no less than ±30% around this programmed frequency. Therefore, during external clock synchronization be sure that the external clock frequency is within this ±30% range of the RT programmed frequency. It is advisable that the RT programmed frequency be equal the external clock for maximum synchronization margin. Refer to the “Phase and Frequency Synchronization” section for more details.

Inductor Value Calculation

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered.

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The inductor value has a direct effect on ripple current. The inductor ripple current ΔI_L decreases with higher inductance or frequency and increases with higher V_{IN}:

$$\Delta I_L = \left(\frac{V_{OUT}}{f \bullet L}\right)\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Accepting larger values of ΔI_L allows the use of low inductances, but results in higher output voltage ripple, higher ESR losses in the output capacitor, and greater core losses. A reasonable starting point for setting ripple current is $\Delta I_L = 0.4 \bullet I_{MAX}$. The maximum ΔI_L occurs at the maximum input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductance should be chosen according to:

$$L = \left(\frac{V_{OUT}}{f \bullet \Delta I_{L(MAX)}}\right)\left(1 - \frac{V_{OUT}}{V_{IN(MAX)}}\right)$$

Inductor Core Selection

Once the value for L is known, the type of inductor must be selected. The two basic types are iron powder and ferrite. The iron powder types have a soft saturation curve which means they do not saturate hard like ferrites do. However, iron powder type inductors have higher core losses. Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation.

Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite core material saturates *hard*, which means that inductance collapses abruptly when the peak design current is exceeded. This results an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

A variety of inductors designed for high current, low voltage applications are available from manufacturers such as Sumida, Panasonic, Coiltronics, Coilcraft, Toko, Vishay, Pulse and Würth.

Current Sense Pins

Inductor current is sensed through voltage between $SENSE^+$ and $SENSE^-$ pins, the inputs of the internal current comparators. The input voltage range of the SENSE pins is –0.5V to 5.5V. Care must be taken not to float these pins during normal operation. The $SENSE^+$ pins are quasi-high impedance inputs. There is no bias current into a $SENSE^+$ pin when its corresponding channel's $SENSE^-$ pin ramps up from below 1.1V and stays below 1.4V. But there is a small (~1µA) current flowing into a $SENSE^+$ pin when its corresponding $SENSE^-$ pin ramps down from 1.4V and stays above 1.1V. Such currents also exist on $SENSE^-$ pins. But in addition, each $SENSE^-$ pin has an internal 500k resistor to SGND. The resulted current (V_{OUT}/500k) will dominate the total current flowing into the $SENSE^-$ pins. $SENSE^+$ and $SENSE^-$ pin currents have to be taken into account when designing either R_{SENSE} or DCR inductor current sensing.

Current Limit Programming

The current sense comparators' maximum trip voltage between $SENSE^+$ and $SENSE^-$ (or "sense voltage"), when ITH is clamped at its maximum 2.4V, is set by the voltage applied to the V_{RNG} pin and is given by:

$$V_{SENSE(MAX)} = 0.05V_{RNG}$$

The valley current mode control loop does not allow the inductor current valley to exceed $0.05V_{RNG}$. In practice, one should allow sufficient margin, to account for tolerance of the parts and external component values. Note that ITH is close to 2.4V when in current limit.

An external resistive divider from $INTV_{CC}$ can be used to set the voltage on a V_{RNG} pin between 0.6V and 2V, resulting in a maximum sense voltage between 30mV and 100mV. Such wide voltage range allows for variety of applications. The V_{RNG} pin can also be tied to either SGND or $INTV_{CC}$ to force internal defaults. When V_{RNG} is tied to SGND, the device has an equivalent V_{RNG} of 0.6V. When the V_{RNG} pin is tied to $INTV_{CC}$, the device has an equivalent V_{RNG} of 1V.

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R_{SENSE} Inductor Current Sensing

The LTC3838 can be configured to sense the inductor currents through either low value series current sensing resistors (R_{SENSE}) or inductor DC resistance (DCR). The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller.

A typical R_{SENSE} inductor current sensing scheme is shown in Figure 3a. The filter components (R_F, C_F) need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair close together and Kelvin (4-wire) connected underneath the sense resistor, as shown in Figure 3b. Sensing current elsewhere can effectively add parasitic inductance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable.

R_{SENSE} is chosen based on the required maximum output current. Given the maximum current, $I_{OUT(MAX)}$, maximum sense voltage, $V_{SENSE(MAX)}$, set by V_{RNG}, and maximum inductor ripple current $\Delta I_{L(MAX)}$, the value of R_{SENSE} can be chosen as:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{OUT(MAX)} - \dfrac{\Delta I_{L(MAX)}}{2}}$$

Conversely, given R_{SENSE} and $I_{OUT(MAX)}$, $V_{SENSE(MAX)}$ and thus V_{RNG} voltage can be determined from the above equation. To ensure the maximum output current, sufficient margin should be built in the calculations to account for variations of LTC3838 under different operating conditions and tolerances of external components.

Because of possible PCB noise in the current sensing loop, the current sensing voltage ripple $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, 10mV of ΔV_{SENSE} is recommended as a conservative number to start with, either for R_{SENSE} or Inductor DCR sensing applications.

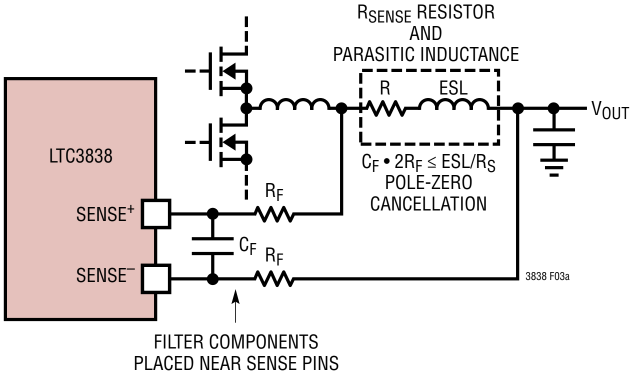

Figure 3a. R_{SENSE} Current Sensing

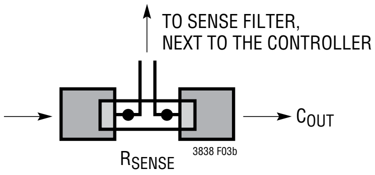

Figure 3b. Sense Lines Placement with Sense Resistor

For today's highest current density solutions the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 2MHz are becoming more common. Under these conditions, the voltage drop across the sense resistor's parasitic inductance becomes more relevant. A small RC filter placed near the IC has been traditionally used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance.

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For example, Figure 4a illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for a 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \bullet \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}}$$

where $V_{ESL(STEP)}$ is the voltage step caused by the ESL and shown in Figure 4a, and t_{ON} and t_{OFF} are top MOSFET on-time and off-time respectively. If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 4b. For applications using low $V_{SENSE(MAX)}$, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{RSENSE}.

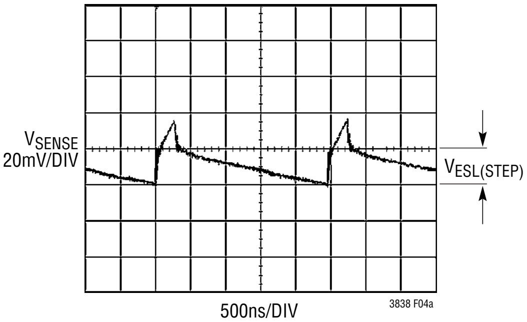

Figure 4a. Voltage Waveform Measured Directly Across the Sense Resistor

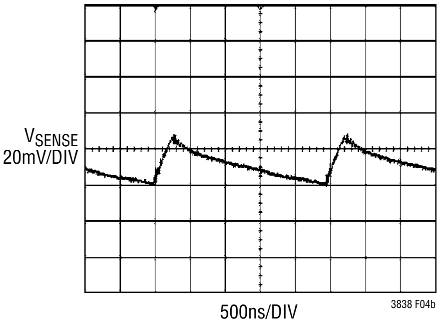

Figure 4b. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω

Note that the SENSE1⁻ and SENSE2⁻ pins are also used for sensing the output voltage for the adjustment of top gate on time, t_{ON}. For this purpose, there is an additional internal 500k resistor from each SENSE⁻ pin to SGND, therefore there is an impedance mismatch with their corresponding SENSE⁺ pins. The voltage drop across the R_F causes an offset in sense voltage. For example, with R_F = 100Ω, at $V_{OUT} = V_{SENSE}^-$ = 5V, the sense-voltage offset $V_{SENSE(OFFSET)} = V_{SENSE}^- \bullet R_F/500k$ = 1mV. Such small offset may seem harmless for current limit, but could be significant for current reversal detection (I_{REV}), causing excess negative inductor current at discontinuous mode. Also, at $V_{SENSE(MAX)}$ = 30mV, a mere 1mV offset will cause a significant shift of zero-current ITH voltage by (2.4V – 0.8V) • 1mV/30mV = 53mV. Too much shift may not allow the output voltage to return to its regulated value after the output is shorted due to ITH foldback. Therefore, when a larger filter resistor R_F value is used, it is recommended to use an *external* 500k resistor from each SENSE⁺ pin to SGND, to balance the *internal* 500k resistor at its corresponding SENSE⁻ pin.

The previous discussion generally applies to high density/high current applications where $I_{OUT(MAX)}$ > 10A and low inductor values are used. For applications where $I_{OUT(MAX)}$

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< 10A, set R_F to 10Ω and C_F to 1000pF. This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin (4-wire) connected to the sense resistor.

DCR Inductor Current Sensing

For applications requiring higher efficiency at high load currents, the LTC3838 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 5. The DCR of the inductor represents the small amount of DC winding resistance, which can be less than 1mΩ for today's low value, high current inductors.

In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

The inductor DCR is sensed by connecting an RC filter across the inductor. This filter typically consists of one or two resistors (R1 and R2) and one capacitor (C1) as shown in Figure 5. If the external (R1||R2) • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the voltage drop across the inductor DCR multiplied by R2/(R1 + R2). Therefore, R2 may be used to scale the voltage across the sense terminals when the DCR is greater than the target sense resistance. With the ability to program current limit through the V_{RNG} pin, R2 may be optional. C1 is usually selected in the range of 0.01μF to 0.47μF. This forces R1||R2 to around 2k to 4k, reducing error that might have been caused by the SENSE pins' input bias currents.

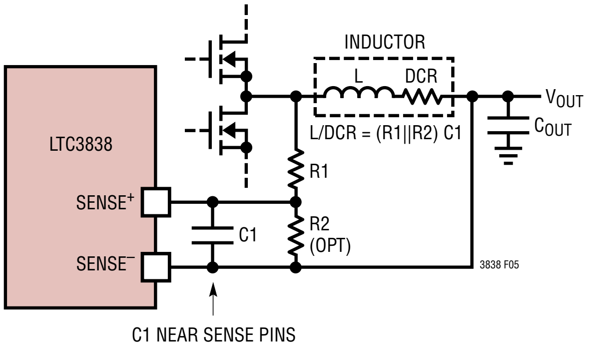

Figure 5. DCR Current Sensing

Resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. Capacitor C1 should be placed close to the IC pins.

The first step in designing DCR current sensing is to determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 25°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for inductor temperature T_L is 100°C. The DCR of the inductor can also be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

From the DCR value, $V_{SENSE(MAX)}$ is easily calculated as:

$$V_{SENSE(MAX)} = DCR_{MAX(25^\circ C)} \cdot \left[1+0.4\%\left(T_{L(MAX)}-25^\circ C\right)\right] \cdot \left(I_{OUT(MAX)}-\frac{\Delta I_L}{2}\right)$$

If $V_{SENSE(MAX)}$ is within the maximum sense voltage (30mV to 100mV) of the LTC3838 as programmed by the V_{RNG} pin, then the RC filter only needs R1. If $V_{SENSE(MAX)}$ is higher, then R2 may be used to scale down the maximum sense voltage so that it falls within range.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}(R1)=\frac{\left(V_{IN(MAX)}-V_{OUT}\right)\bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or R_{SENSE} sensing. Light load power loss can be modestly higher with a DCR network than with a sense resistor due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal-to-noise ratio for the current sense signal, start with a ΔV_{SENSE} of 10mV. For a DCR sensing application, the actual ripple voltage will be determined by:

$$\Delta V_{SENSE}=\frac{V_{IN}-V_{OUT}}{R1\bullet C1}\bullet\frac{V_{OUT}}{V_{IN}\bullet f}$$

Power MOSFET Selection

Two external N-channel power MOSFETs must be selected for each channel of the LTC3838 controller: one for the top (main) switch and one for the bottom (synchronous) switch. The gate drive levels are set by the DRV_{CC} voltage. This voltage is typically 5.3V. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic-level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, Miller capacitance, C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat (or the parameter Q_{GD} if specified on a manufacturer's data sheet), divided by the specified V_{DS} test voltage:

$$C_{MILLER}\cong\frac{Q_{GD}}{V_{DS(TEST)}}$$

When the IC is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$D_{TOP}=\frac{V_{OUT}}{V_{IN}}$$

$$D_{BOT}=1-\frac{V_{OUT}}{V_{IN}}$$

The MOSFET power dissipations at maximum output current are given by:

$$P_{TOP}=D_{TOP}\bullet I_{OUT(MAX)}^{2}\bullet R_{DS(ON)(MAX)}(1+\delta)+V_{IN}^{2}\bullet\left(\frac{I_{OUT(MAX)}}{2}\right)\bullet C_{MILLER}\left[\frac{R_{TG(UP)}}{V_{DRVCC}-V_{MILLER}}+\frac{R_{TG(DOWN)}}{V_{MILLER}}\right]\bullet f$$

$$P_{BOT}=D_{BOT}\bullet I_{OUT(MAX)}^{2}\bullet R_{DS(ON)(MAX)}\bullet(1+\delta)$$

where δ is the temperature dependency of $R_{DS(ON)}$, $R_{TG(UP)}$ is the TG pull-up resistance, and $R_{TG(DOWN)}$ is the TG pull-down resistance. V_{MILLER} is the Miller effect V_{GS} voltage and is taken graphically from the MOSFET's data sheet.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V, the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during short-circuit when the synchronous switch is on close to 100% of the period.

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The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve in the power MOSFET data sheet. For low voltage MOSFETs, 0.5% per degree (°C) can be used to estimate δ as an approximation of percentage change of $R_{DS(ON)}$:

$$\delta = 0.005/°C \cdot (T_J - T_A)$$

where T_J is estimated junction temperature of the MOSFET and T_A is ambient temperature.

C_{IN} Selection

In continuous mode, the source current of the top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. To prevent large voltage transients, a low ESR input capacitor sized for the maximum RMS current must be used. The worst-case RMS current occurs by assuming a single-phase application. The maximum RMS capacitor current is given by:

$$I_{RMS} \cong I_{OUT(MAX)} \cdot \frac{V_{OUT}}{V_{IN}} \cdot \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3838, additional ceramic capacitors should also be used in parallel for C_{IN} close to the IC and power switches to bypass the high frequency switching noises. Typically multiple X5R or X7R ceramic capacitors are put in parallel with either conductive-polymer or aluminum-electrolytic types of bulk capacitors. Because of its low ESR, the ceramic capacitors will take most of the RMS ripple current. Vendors do not consistently specify the ripple current rating for ceramics, but ceramics *could* also fail due to excessive ripple current. Always consult the manufacturer if there is any question.

Figure 6 represents a simplified circuit model for calculating the ripple currents in each of these capacitors. The input inductance (L_{IN}) between the input source and the input of the converter will affect the ripple current through the capacitors. A lower input inductance will result in less ripple current through the input capacitors since more ripple current will now be flowing out of the input source.

For simulations with this model, look at the ripple current during steady-state for the case where one phase is fully loaded and the other was not loaded. This will in *general* be the worst case for ripple current since the ripple current from one phase will not be cancelled by ripple current from the other phase.

Note that the bulk capacitor also has to be chosen for RMS rating with ample margin beyond its RMS current per simulation with the circuit model provided. For a lower V_{IN} range, a conductive-polymer type (such as Sanyo OS-CON) can be used for its higher ripple current rating and lower ESR. For a wide V_{IN} range that also require higher voltage rating, aluminum-electrolytic capacitors are

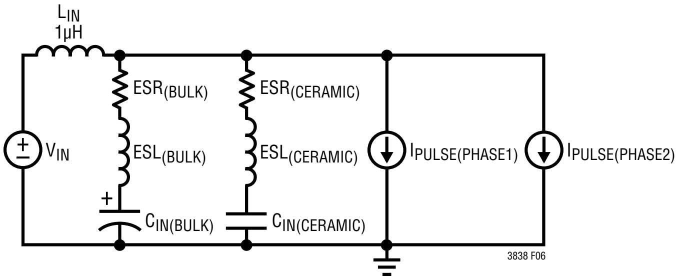

Figure 6. Circuit Model for Input Capacitor Ripple Current Simulation