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Dual, Multiphase Synchronous DC/DC Controller with Differential Remote Sense

FEATURES

- **Dual, 180° Phased Controllers Reduce Required Input Capacitance and Power Supply Induced Noise**
- **High Efficiency: Up to 95%**
- **R_{SENSE} or DCR Current Sensing**
- **Programmable DCR Temperature Compensation**
- **±0.75% 0.6V Output Voltage Accuracy**
- **Phase-Lockable Fixed Frequency 250kHz to 770kHz**
- **True Remote Sensing Differential Amplifier**
- Dual N-Channel MOSFET Synchronous Drive
- Wide V_{IN} Range: 4.5V to 38V
- V_{OUT} Range: 0.6V to 12.5V without Differential Amplifier
- V_{OUT} Range: 0.6V to 3.3V with Differential Amplifier
- Clock Input and Output for Up to 12-Phase Operation
- Adjustable Soft-Start or V_{OUT} Tracking
- Foldback Output Current Limiting
- Output Overvoltage Protection
- 40-Pin (6mm × 6mm) QFN and 38-Lead FE Packages

APPLICATIONS

- Computer Systems
- Telecom Systems
- Industrial and Medical Instruments
- DC Power Distribution Systems

DESCRIPTION

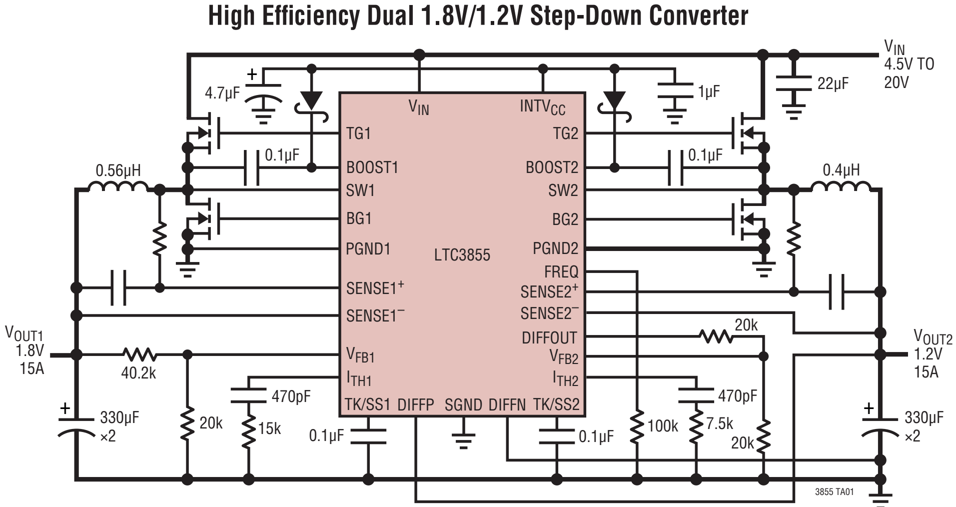
The LTC®3855 is a dual PolyPhase® current mode synchronous step-down switching regulator controller that drives all N-channel power MOSFET stages. It includes a high speed differential remote sense amplifier. The maximum current sense voltage is programmable for either 30mV, 50mV or 75mV, allowing the use of either the inductor DCR or a discrete sense resistor as the sensing element.

The LTC3855 features a precision 0.6V reference and can produce output voltages up to 12.5V. A wide 4.5V to 38V input supply range encompasses most intermediate bus voltages and battery chemistries. Power loss and supply noise are minimized by operating the two controller output stages out of phase. Burst Mode® operation, continuous or pulse-skipping modes are supported.

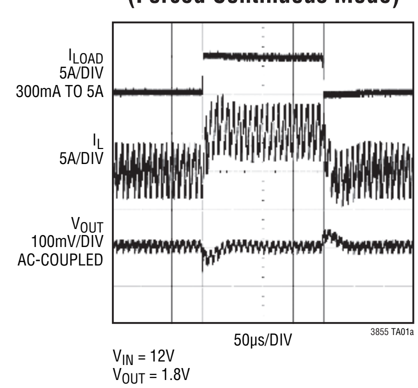
The LTC3855 can be configured for up to 12-phase operation, has DCR temperature compensation, two power good signals and two current limit set pins. The LTC3855 is available in low profile 40-pin 6mm × 6mm QFN and 38-lead exposed pad FE packages.

TYPICAL APPLICATION

High Efficiency Dual 1.8V/1.2V Step-Down Converter



Load Step (Forced Continuous Mode)

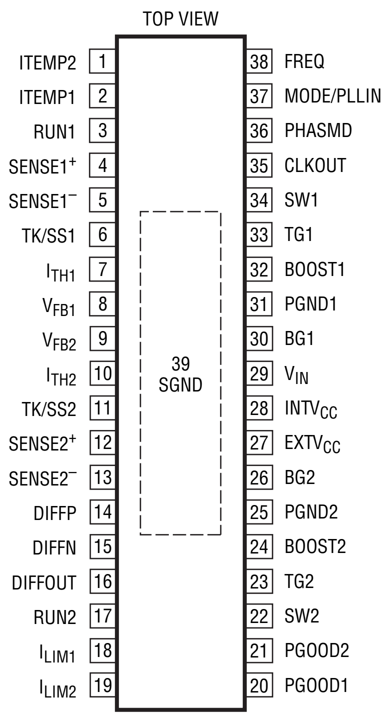


ABSOLUTE MAXIMUM RATINGS

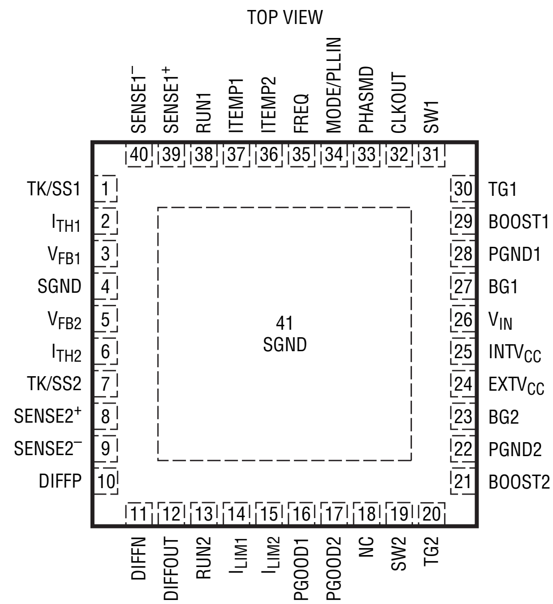
(Note 1)

Input Supply Voltage (V_{IN}) .... –0.3V to 40V
Top Side Driver Voltages
BOOST1, BOOST2 .... –0.3V to 46V
Switch Voltage (SW1, SW2) .... –5V to 40V
$INTV_{CC}$, RUN1, RUN2, PGOOD(s), $EXTV_{CC}$,
(BOOST1-SW1), (BOOST2-SW2) .... –0.3V to 6V
SENSE1$^+$, SENSE2$^+$, SENSE1$^–$,
SENSE2$^–$ Voltages .... –0.3V to 13V
MODE/PLLIN, I_{LIM1}, I_{LIM2}, TK/SS1, TK/SS2, FREQ,
DIFFOUT, PHASMD Voltages .... –0.3V to $INTV_{CC}$
DIFFP, DIFFN .... –0.3V to $INTV_{CC}$
ITEMP1, ITEMP2 Voltages .... –0.3V to $INTV_{CC}$
I_{TH1}, I_{TH2}, V_{FB1}, V_{FB2} Voltages .... –0.3V to $INTV_{CC}$
$INTV_{CC}$ Peak Output Current (Note 8) 100mA
Operating Junction Temperature Range (Notes 2, 3)
LTC3855 .... –40°C to 125°C
Storage Temperature Range .... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
(FE Package) .... 300°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS SGND, MUST BE SOLDERED TO PCB



UJ PACKAGE
40-LEAD (6mm × 6mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 33°C/W
EXPOSED PAD (PIN 41) IS SGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3855EFE#PBF	LTC3855EFE#TRPBF	LTC3855FE	38-Lead Plastic TSSOP	–40°C to 85°C
LTC3855IFE#PBF	LTC3855IFE#TRPBF	LTC3855FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3855EUJ#PBF	LTC3855EUJ#TRPBF	LTC3855UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 85°C
LTC3855IUJ#PBF	LTC3855IUJ#TRPBF	LTC3855UJ	40-Lead (6mm × 6mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range (E-Grade), otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN1,2}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage Range			4.5		38	V
V_{OUT}	Output Voltage Range			0.6		12.5	V
$V_{FB1,2}$	Regulated Feedback Voltage	$I_{TH1,2}$ Voltage = 1.2V (Note 4) $I_{TH1,2}$ Voltage = 1.2V (Note 4), T_A = 125°C	● ●	0.5955 0.594	0.600 0.600	0.6045 0.606	V V
$I_{FB1,2}$	Feedback Current	(Note 4)			–15	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 38V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop; ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
$g_{m1,2}$	Transconductance Amplifier g_m	$I_{TH1,2}$ = 1.2V; Sink/Source 5μA; (Note 4)			2		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) V_{IN} = 15V $V_{RUN1,2}$ = 0V			 3.5 30	 50	 mA μA
DF_{MAX}	Maximum Duty Factor	In Dropout, f_{OSC} = 500kHz		94	95		%
UVLO	Undervoltage Lockout	V_{INTVCC} Ramping Down	●	3.0	3.2	3.4	V
$UVLO_{HYS}$	UVLO Hysteresis				0.6		V
$V_{OVL1,2}$	Feedback Overvoltage Lockout	Measured at $V_{FB1,2}$	●	0.64	0.66	0.68	V
$I_{SENSE1,2}$	Sense Pins Bias Current	(Each Channel); $V_{SENSE1,2}$ = 3.3V	●		±1	±2	μA
$I_{TEMP1,2}$	DCR Tempco Compensation Current	$V_{ITEMP1,2}$ = 0.2V	●	9	10	11	μA
$I_{TK/SS1,2}$	Soft-Start Charge Current	$V_{TK/SS1,2}$ = 0V	●	1	1.2	1.4	μA
$V_{RUN1,2}$	RUN Pin ON Threshold	V_{RUN1}, V_{RUN2} Rising	●	1.1	1.22	1.35	V
$V_{RUN1,2HYS}$	RUN Pin ON Hysteresis				80		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold	$V_{FB1,2}$ = 0.5V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = 0V $V_{FB1,2}$ = 0.5V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = Float $V_{FB1,2}$ = 0.5V, $V_{SENSE1,2}$ = 3.3V, I_{LIM} = $INTV_{CC}$	● ● ●	25 45 68	30 50 75	35 55 82	mV mV mV
TG1, 2 t_r TG1, 2 t_f	TG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns
BG1, 2 t_r BG1, 2 t_f	BG Transition Time: Rise Time Fall Time	(Note 6) C_{LOAD} = 3300pF C_{LOAD} = 3300pF			 25 25		 ns ns

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range (E-Grade), otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN1,2}$ = 5V unless noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			90		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} < 38V		4.8	5	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.5	2	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				200		mV
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		210	250	290	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} ≥ 2.4V		700	770	850	kHz
$R_{MODE/PLLIN}$	MODE/PLLIN Input Resistance				250		kΩ
I_{FREQ}	Frequency Setting Current			9	10	11	μA
CLKOUT	Phase (Relative to Controller 1)	PHASMD = GND PHASMD = Float PHASMD = $INTV_{CC}$			60 90 120		Deg Deg Deg
CLK_{HIGH}	Clock High Output Voltage			4	5		V
CLK_{LOW}	Clock Low Output Voltage				0	0.2	V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.3	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	μA
V_{PG}	PGOOD Trip Level, Either Controller	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %
Differential Amplifier							
A_{DA}	Gain		●	0.998	1	1.002	V/V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100μA				2	mV
$PSRR_{OA}$	Power Supply Rejection Ratio	5V < V_{IN} < 38V			100		dB
I_{CL}	Maximum Output Current			2	3		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300μA		V_{INTVCC} – 1.4	V_{INTVCC} – 1.1		V
GBW	Gain Bandwidth Product	(Note 8)			3		MHz
Slew Rate	Differential Amplifier Slew Rate	(Note 8)			2		V/μs

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range (E-Grade), otherwise specifications are at T_A = 25°C. V_{IN} = 15V, $V_{RUN/SS}$ = 5V unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
On Chip Driver							
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3855E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3855I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature T_A and power dissipation P_D according to the following formulas:

LTC3855UJ: $T_J = T_A + (P_D \bullet 33°C/W)$

LTC3855FE: $T_J = T_A + (P_D \bullet 25°C/W)$

Note 4: The LTC3855 is tested in a feedback loop that servos $V_{ITH1,2}$ to a specified voltage and measures the resultant $V_{FB1,2}$.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See Applications Information.

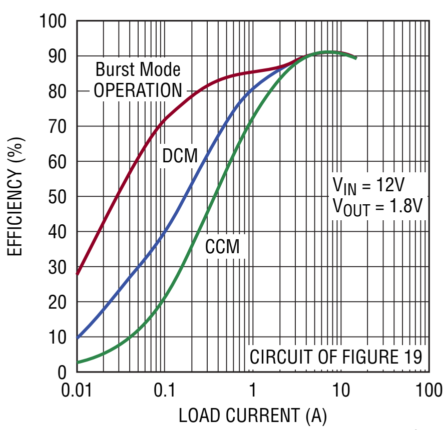
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition is specified for an inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

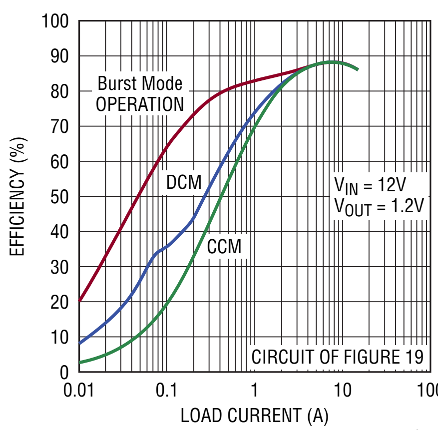
Note 8: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

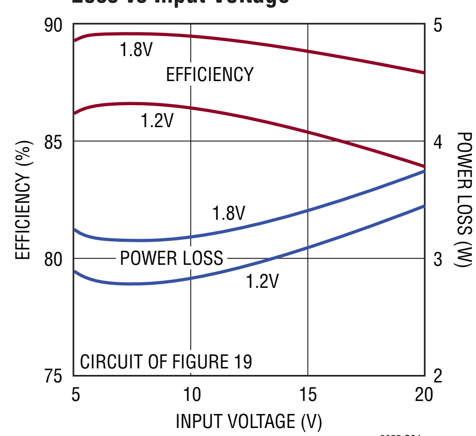
Efficiency vs Output Current and Mode



Efficiency vs Output Current and Mode

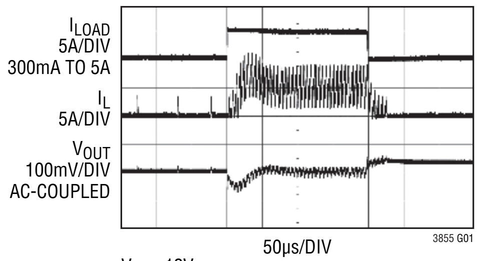


Full Load Efficiency and Power Loss vs Input Voltage



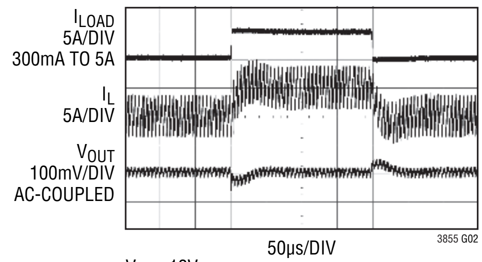
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step (Burst Mode Operation)



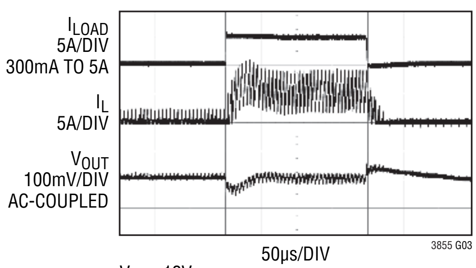
V_{IN} = 12V
V_{OUT} = 1.8V

Load Step (Forced Continuous Mode)



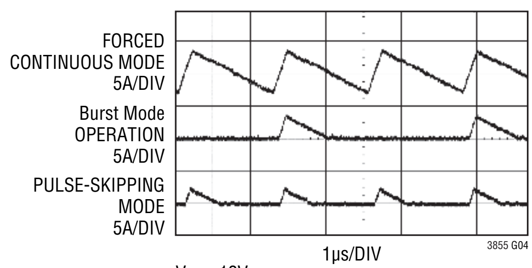
V_{IN} = 12V
V_{OUT} = 1.8V

Load Step (Pulse-Skipping Mode)



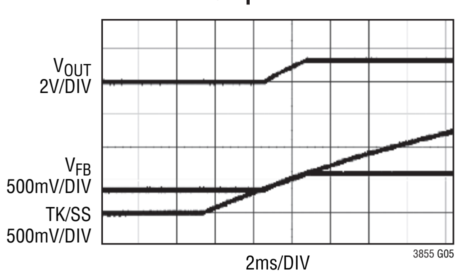
V_{IN} = 12V
V_{OUT} = 1.8V

Inductor Current at Light Load



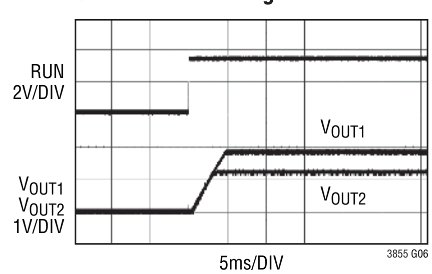
V_{IN} = 12V
V_{OUT} = 1.8V
I_{LOAD} = 400mA

Prebiased Output at 2V



V_{IN} = 12V
V_{OUT} = 3.3V

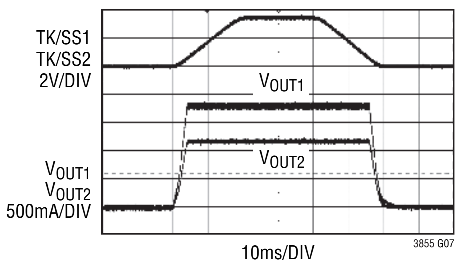
Coincident Tracking



V_{OUT1} = 1.8V, 1.5Ω LOAD
V_{OUT2} = 1.2V, 1Ω LOAD

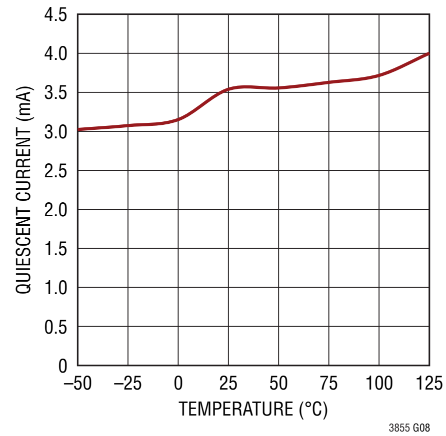
TYPICAL PERFORMANCE CHARACTERISTICS

Tracking Up and Down with External Ramp

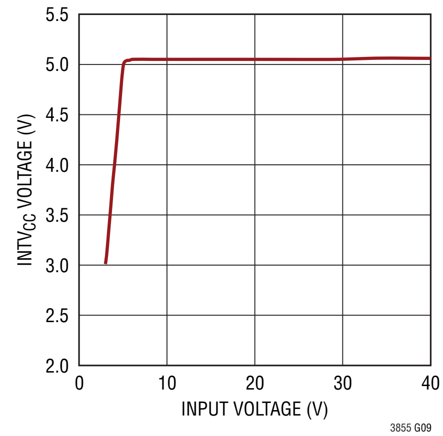


V_{IN} = 12V
V_{OUT1} = 1.8V, 1.5Ω LOAD
V_{OUT2} = 1.2V, 1Ω LOAD

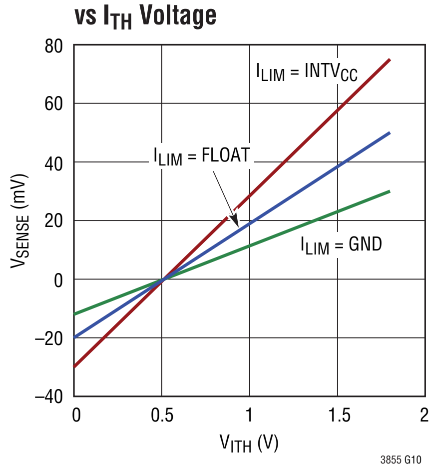
Quiescent Current vs Temperature without $EXTV_{CC}$



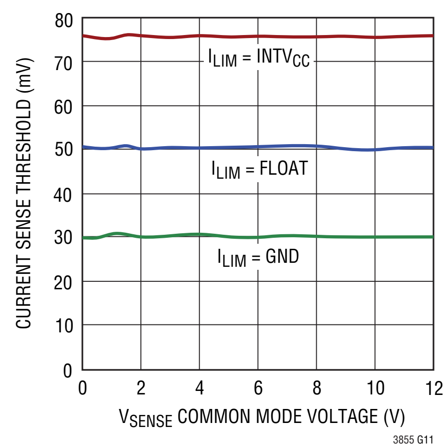
$INTV_{CC}$ Line Regulation



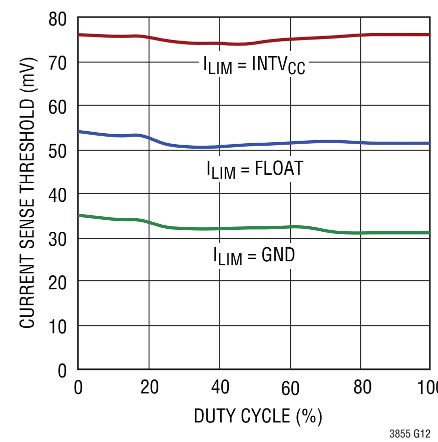
Current Sense Threshold vs I_{TH} Voltage



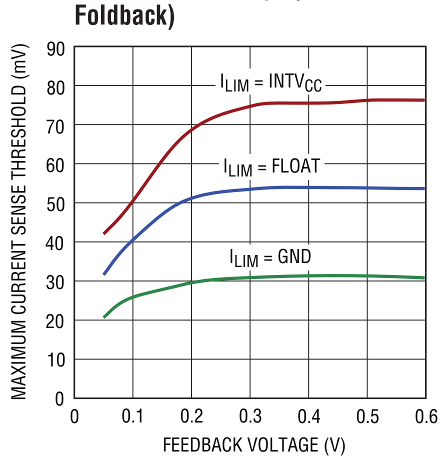
Maximum Current Sense Threshold vs Common Mode Voltage



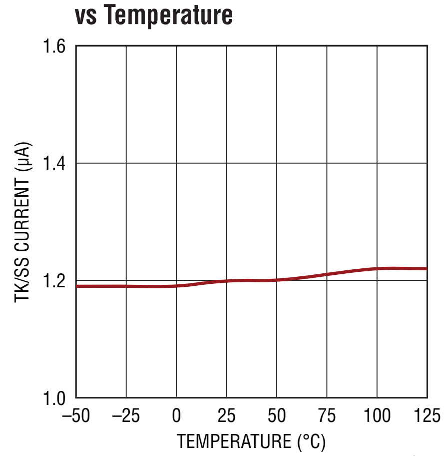
Maximum Current Sense Threshold vs Duty Cycle



Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)

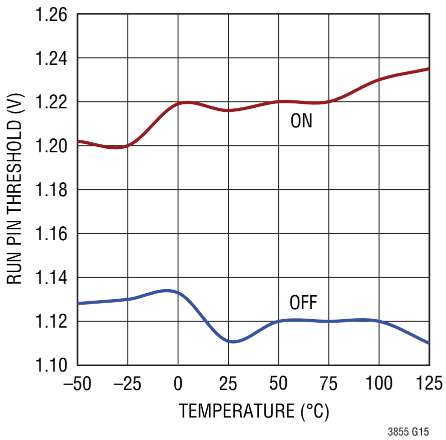


TK/SS Pull-Up Current vs Temperature

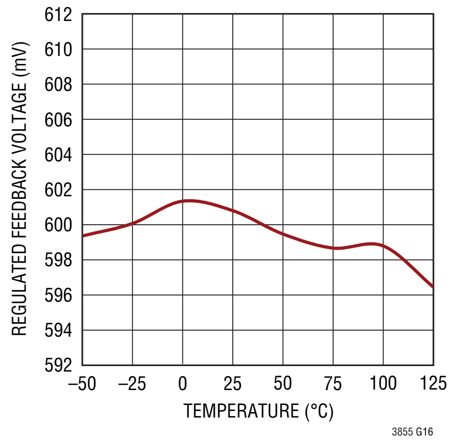


TYPICAL PERFORMANCE CHARACTERISTICS

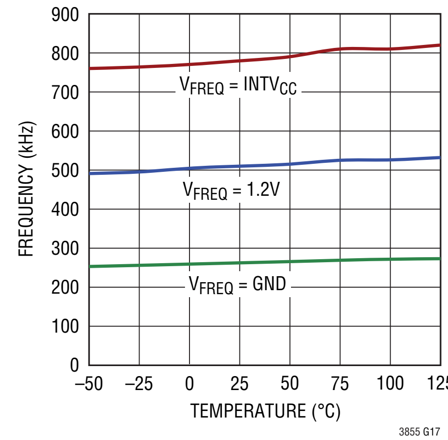
Shutdown (RUN) Threshold vs Temperature



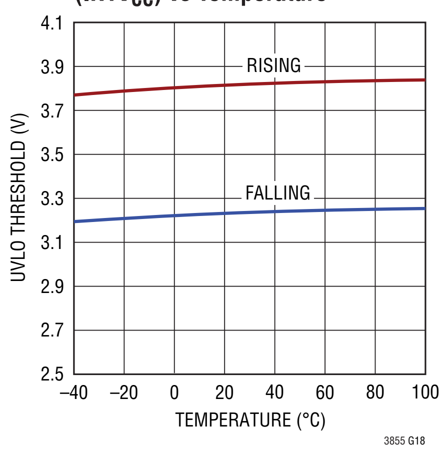
Regulated Feedback Voltage vs Temperature



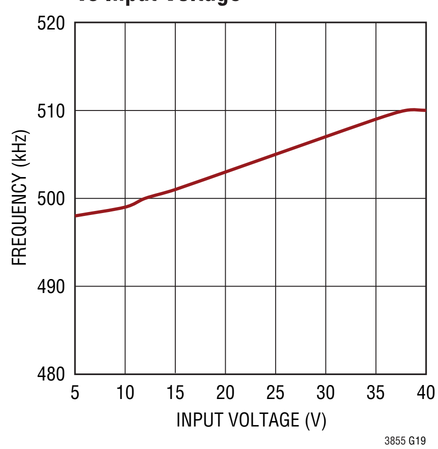
Oscillator Frequency vs Temperature



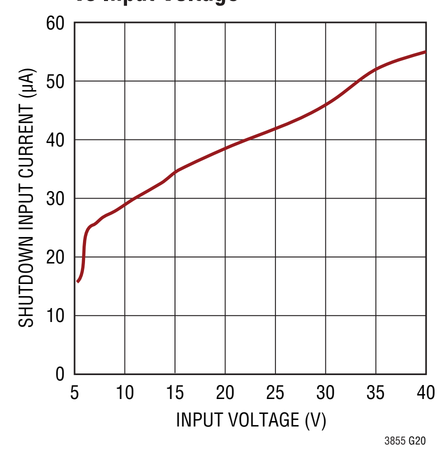
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



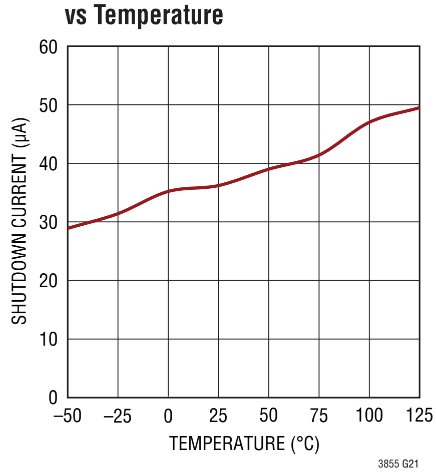
Oscillator Frequency vs Input Voltage



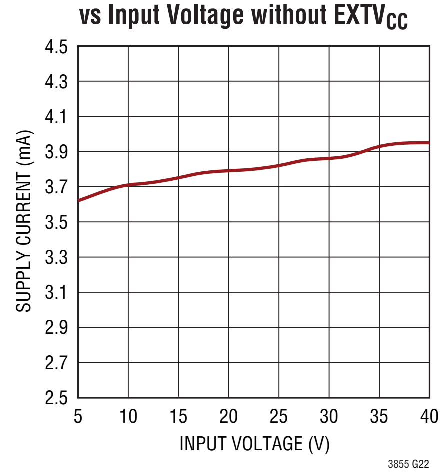
Shutdown Current vs Input Voltage



Shutdown Current vs Temperature



Quiescent Current vs Input Voltage without $EXTV_{CC}$



PIN FUNCTIONS (FE38/UJ40)

ITEMP1, ITEMP2 (Pin 2, Pin 1/Pin 37, Pin 36): Inputs of the temperature sensing comparators. Connect each of these pins to external NTC resistors placed near inductors. Floating these pins disables the DCR temperature compensation function.

RUN1, RUN2 (Pin 3, Pin 17/Pin 38, Pin 13): Run Control Inputs. A voltage above 1.2V on either pin turns on the IC. However, forcing either of these pins below 1.2V causes the IC to shut down the circuitry required for that particular channel. There are 1μA pull-up currents for these pins. Once the Run pin rises above 1.2V, an additional 4.5μA pull-up current is added to the pin.

SENSE1$^+$, SENSE2$^+$ (Pin 4, Pin 12/Pin 39, Pin 8): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

SENSE1$^–$, SENSE2$^–$ (Pin 5, Pin 13/Pin 40, Pin 9): Current Sense Comparator Inputs. The (–) inputs to the current comparators are connected to the outputs.

TK/SS1, TK/SS2 (Pin 6, Pin 11/Pin 1, Pin 7): Output Voltage Tracking and Soft-Start Inputs. When one particular channel is configured to be the master of two channels, a capacitor to ground at this pin sets the ramp rate for the master channel's output voltage. When the channel is configured to be the slave of two channels, the V_{FB} voltage of the master channel is reproduced by a resistor divider and applied to this pin. Internal soft-start currents of 1.2μA are charging these pins.

I_{TH1}, I_{TH2} (Pin 7, Pin 10/Pin 2, Pin 6): Current Control Thresholds and Error Amplifier Compensation Points. Each associated channels' current comparator tripping threshold increases with its I_{TH} control voltage.

V_{FB1}, V_{FB2} (Pin 8, Pin 9/Pin 3, Pin 5): Error Amplifier Feedback Inputs. These pins receive the remotely sensed feedback voltages for each channel from external resistive dividers across the outputs.

DIFFP (Pin 14/Pin 10): Positive Input of Remote Sensing Differential Amplifier. Connect this to the remote load voltage of one of the two channels directly.

DIFFN (Pin 15/Pin 11): Negative Input of Remote Sensing Differential Amplifier. Connect this to the negative terminal of the output capacitors.

DIFFOUT (Pin 16/Pin 12): Output of Remote Sensing Differential Amplifier. Connect this to V_{FB1} or V_{FB2} through a resistive divider.

I_{LIM1}, I_{LIM2} (Pin 18, Pin 19/Pin 14, Pin 15): Current Comparator Sense Voltage Range Inputs. This pin can be tied to SGND, tied to $INTV_{CC}$ or left floating to set the maximum current sense threshold for each comparator.

PGOOD1, PGOOD2 (Pin 20, Pin 21/Pin 16, Pin 17): Power Good Indicator Output for Each Channel. Open drain logic out that is pulled to ground when either channel output exceeds ±10% regulation window, after the internal 20μs power bad mask timer expires.

$EXTV_{CC}$ (Pin 27/Pin 24): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V. Do not exceed 6V on this pin.

$INTV_{CC}$ (Pin 28/Pin 25): Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7μF low ESR tantalum or ceramic capacitor.

V_{IN} (Pin 29/Pin 26): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1μF to 1μF).

BG1, BG2 (Pin 30, Pin 26/Pin 27, Pin 23): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-Channel MOSFETs between PGND and $INTV_{CC}$.

PGND1, PGND2 (Pin 31, Pin 25/Pin 28, Pin 22): Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (–) terminal of C_{VCC} and the (–) terminal of C_{IN}.

PIN FUNCTIONS (FE38/UJ40)

BOOST1, BOOST2 (Pin 32, Pin 24/Pin 29, Pin 21): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to V_{IN} + $INTV_{CC}$.

TG1, TG2 (Pin 33, Pin 23/Pin 30, Pin 20): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch nodes voltages.

SW1, SW2 (Pin 34, Pin 22/Pin 31, Pin 19): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

PHASMD (Pin 36/Pin 33): This pin can be tied to SGND, tied to $INTV_{CC}$ or left floating. This pin determines the relative phases between the internal controllers as well as the phasing of the CLKOUT signal. See Table 1 in the Operation section.

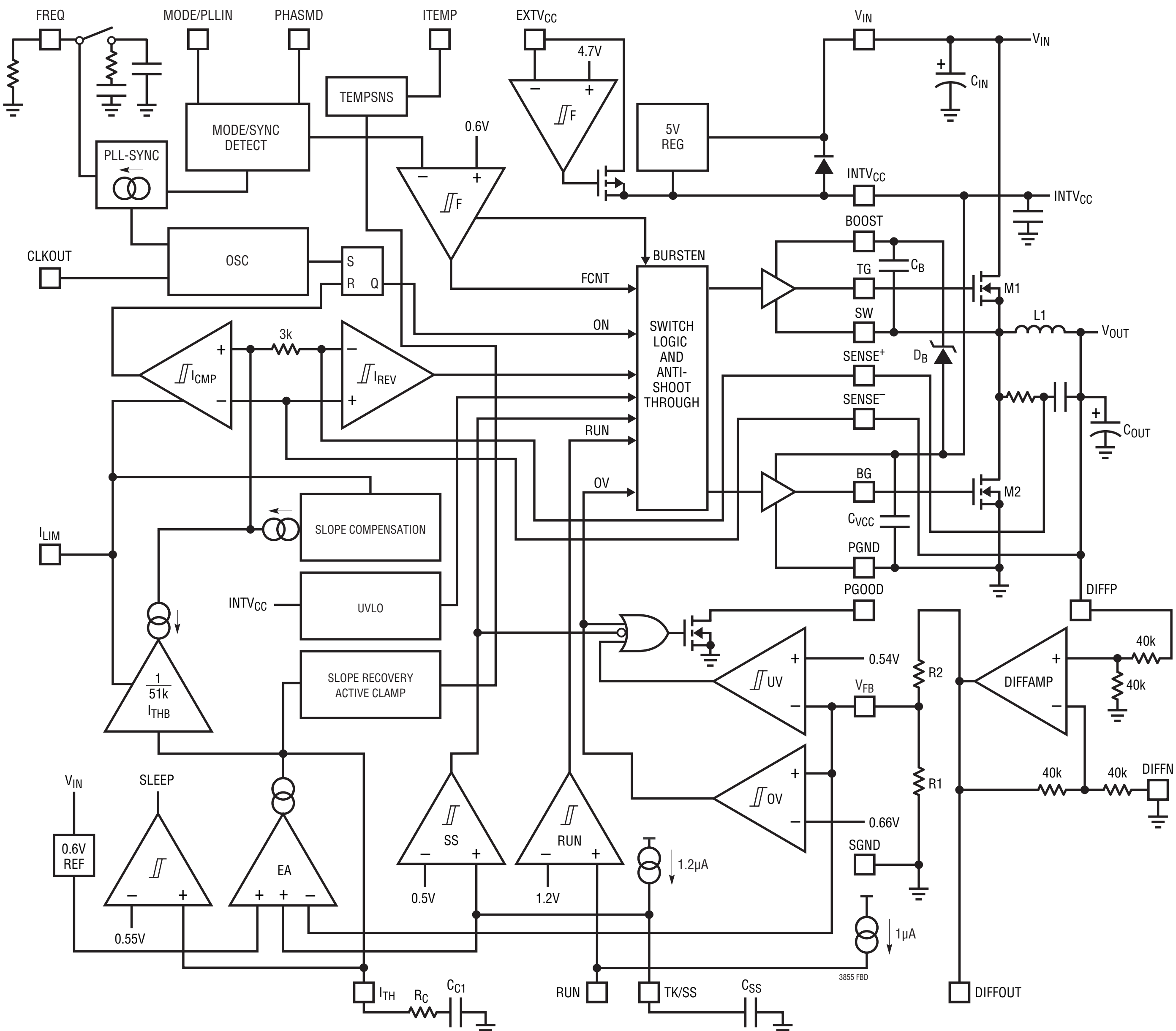
CLKOUT (Pin 35/Pin 32): Clock output with phase changeable by PHASMD to enable usage of multiple LTC3855 in multiphase systems.

MODE/PLLIN (Pin 37/Pin 34): This is a dual purpose pin. When external frequency synchronization is not used, this pin selects the operating mode. The pin can be tied to SGND, tied to $INTV_{CC}$ or left floating. SGND enables forced continuous mode. $INTV_{CC}$ enables pulse-skipping mode. Floating enables Burst Mode operation. For external sync, apply a clock signal to this pin. Both channels will go into forced continuous mode and the internal PLL will synchronize the internal oscillator to the clock. The PLL compensation network is integrated into the IC.

FREQ (Pin 38/Pin 35): There is a precision 10µA current flowing out of this pin. A resistor to ground sets a voltage which in turn programs the frequency. Alternatively, this pin can be driven with a DC voltage to vary the frequency of the internal oscillator.

SGND (Exposed Pad Pin 39/ Pin 4, Exposed Pad Pin 41): Signal Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point. Exposed pad must be soldered to PCB, providing a local ground for the control components of the IC, and be tied to the PGND pin under the IC.

FUNCTIONAL BLOCK DIAGRAM



OPERATION

Main Control Loop

The LTC3855 is a constant-frequency, current mode step-down controller with two channels operating 180 degrees out-of-phase. During normal operation, each top MOSFET is turned on when the clock for that channel sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets the RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of each error amplifier EA. The V_{FB} pin receives the voltage feedback signal, which is compared to the internal reference voltage by the EA. When the load current increases, it causes a slight decrease in V_{FB} relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until the average inductor current matches the new load current. After the top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator I_{REV}, or the beginning of the next cycle.

$INTV_{CC}$/$EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as one of the LTC3855 switching regulator outputs.

Each top MOSFET driver is biased from the floating bootstrap capacitor C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage V_{IN} decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every third cycle to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the drop-out transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN1, RUN2 and TK/SS1, TK/SS2 Pins)

The two channels of the LTC3855 can be independently shut down using the RUN1 and RUN2 pins. Pulling either of these pins below 1.2V shuts down the main control loop for that controller. Pulling both pins low disables both controllers and most internal circuits, including the $INTV_{CC}$ regulator. Releasing either RUN pin allows an internal 1µA current to pull up the pin and enable that controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the Absolute Maximum Rating of 6V on this pin.

The start-up of each controller's output voltage V_{OUT} is controlled by the voltage on the TK/SS1 and TK/SS2 pins. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC3855 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program the soft-start period by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.2µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage V_{OUT} rises smoothly from zero to its final value. Alternatively the TK/SS pin can be used to cause the start-up of V_{OUT} to "track" that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the corresponding RUN pin is pulled low to disable a controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.2V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, both controllers are disabled and the external MOSFETs are held off.

Light Load Current Operation (Burst Mode Operation, Pulse-Skipping, or Continuous Conduction)

The LTC3855 can be enabled to enter high efficiency Burst Mode operation, constant-frequency pulse-skipping mode, or forced continuous conduction mode. To select forced continuous operation, tie the MODE/PLLIN pin to a DC

OPERATION

voltage below 0.6V (e.g., SGND). To select pulse-skipping mode of operation, tie the MODE/PLLIN pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE/PLLIN pin. When a controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-third of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. If the average inductor current is higher than the load current, the error amplifier EA will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops below 0.5V, the internal sleep signal goes high (enabling sleep mode) and both external MOSFETs are turned off.

In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator (I_{REV}) turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE/PLLIN pin is connected to $INTV_{CC}$, the LTC3855 operates in PWM pulse-skipping mode at light loads. At very light loads, the current comparator I_{CMP} may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). The inductor current is not allowed to reverse (discontinuous operation). This mode, like forced continuous operation, exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Multichip Operations (PHASMD and CLKOUT Pins)

The PHASMD pin determines the relative phases between the internal controllers as well as the CLKOUT signal as shown in Table 1. The phases tabulated are relative to zero phase being defined as the rising edge of the clock of phase 1.

Table 1.

PHASMD	GND	FLOAT	INTVcc
Phase1	0°	0°	0°
Phase2	180°	180°	240°
CLKOUT	60°	90°	120°

The CLKOUT signal can be used to synchronize additional power stages in a multiphase power supply solution feeding a single, high current output or separate outputs. Input capacitance ESR requirements and efficiency losses are substantially reduced because the peak current drawn from the input capacitor is effectively divided by the number of phases used and power loss is proportional to the RMS current squared. A two stage, single output voltage implementation can reduce input path power loss by 75% and radically reduce the required RMS current rating of the input capacitor(s).

Single Output Multiphase Operation

The LTC3855 can be used for single output multiphase converters by making these connections

- Tie all of the I_{TH} pins together
- Tie all of the V_{FB} pins together
- Tie all of the TK/SS pins together
- Tie all of the RUN pins together
- Tie all of the ITEMP pins together
- Tie all of the I_{LIM} pins together, or tie the I_{LIM} pins to the same potential

For three or more phases, tie the inputs of the unused differential amplifier(s) to ground. Examples of single output multiphase converters are shown in Figures 20 to 23.

OPERATION

Sensing the Output Voltage with a Differential Amplifier

The LTC3855 includes a low offset, unity gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing the load across the load capacitors directly greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget.

The LTC3855 differential amplifier has a typical output slew rate of 2V/µs. The amplifier is configured for unity gain, meaning that the difference between DIFFP and DIFFN is translated to DIFFOUT, relative to SGND.

Care should be taken to route the DIFFP and DIFFN PCB traces parallel to each other all the way to the terminals of the output capacitor or remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the DIFFP and DIFFN traces should be shielded by a low impedance ground plane to maintain signal integrity.

Inductor DCR Sensing Temperature Compensation and the ITEMP Pins

Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications of high output currents. However the DCR of a copper inductor typically has a positive temperature coefficient. As the temperature of the inductor rises, its DCR value increases. The current limit of the controller is therefore reduced.

LTC3855 offers a method to counter this inaccuracy by allowing the user to place an NTC temperature sensing resistor near the inductor. ITEMP pin, when left floating, is at a voltage around 5V and DCR temperature compensation is disabled. ITEMP pin has a constant 10µA precision current flowing out the pin. By connecting an NTC resistor from ITEMP pin to SGND, the maximum current sense threshold can be varied over temperature according the following equation:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8 - V_{ITEMP}}{1.3}$$

Where:

$V_{SENSEMAX(ADJ)}$ is the maximum adjusted current sense threshold.

$V_{SENSE(MAX)}$ is the maximum current sense threshold specified in the electrical characteristics table. It is typically 75mV, 50mV, or 30mV depending on the setting I_{LIM} pins.

V_{ITEMP} is the voltage of ITEMP pin.

The valid voltage range for DCR temperature compensation on the ITEMP pin is between 0.5V to 0.2V, with 0.5V or above being no DCR temperature correction and 0.2V the maximum correction. However, if the duty cycle of the controller is less than 25%, the ITEMP range is extended from 0.5V to 0V.

An NTC resistor has a negative temperature coefficient, that means that its value decreases as temperature rises. The V_{ITEMP} voltage, therefore, decreases as temperature increases and in turn the $V_{SENSEMAX(ADJ)}$ will increase to compensate the DCR temperature coefficient. The NTC resistor, however, is non-linear and user can linearize its value by building a resistor network with regular resistors. Consult the NTC manufacture datasheets for detailed information.

Another use for the ITEMP pins, in addition to NTC compensated DCR sensing, is adjusting $V_{SENSE(MAX)}$ to values between the nominal values of 30mV, 50mV and 75mV for a more precise current limit. This is done by applying a voltage less than 0.5V to the ITEMP pin. $V_{SENSE(MAX)}$ will be varied per the above equation and the same duty cycle limitations will apply. The current limit can be adjusted using this method either with a sense resistor or DCR sensing.

For more information see the NTC Compensated DCR Sensing paragraph in the Applications Information section.

Frequency Selection and Phase-Locked Loop (FREQ and MODE/PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage. The switching

OPERATION

frequency of the LTC3855's controllers can be selected using the FREQ pin. If the MODE/PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the controller's operating frequency from 250kHz to 770kHz.

There is a precision 10µA current flowing out of the FREQ pin, so the user can program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the application section showing the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is integrated on the LTC3855 to synchronize the internal oscillator to an external clock source that is connected to the MODE/PLLIN pin. The controller is operating in forced continuous mode when it is synchronized.

The PLL loop filter network is integrated inside the LTC3855. The phase-locked loop is capable of locking any frequency within the range of 250kHz to 770kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Power Good (PGOOD Pins)

When V_{FB} pin voltage is not within ±10% of the 0.6V reference voltage, the PGOOD pin is pulled low. The PGOOD pin is also pulled low when the RUN pin is below 1.2V or when the LTC3855 is in the soft-start or tracking phase. The PGOOD pin will flag power good immediately when the V_{FB} pin is within the ±10% of the reference window. However, there is an internal 20µs power bad mask when V_{FB} goes out the ±10% window. Each channel has its own PGOOD and only responds to its own channel signals. The PGOOD pins are allowed to be pulled up by external resistors to sources of up to 6V.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

APPLICATIONS INFORMATION

The Typical Application on the first page is a basic LTC3855 application circuit. LTC3855 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption, and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 30mV, 50mV or 75mV, respectively. The maximum current sense threshold will be adjusted to values between these settings by applying a voltage less than 0.5V to the ITEMP pin. See the Operation section for more details.

Which setting should be used? For the best current limit accuracy, use the 75mV setting. The 30mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. The 50mV setting is a good balance between the two. For single output dual phase applications, use the 50mV or 75mV setting for optimal current sharing.

$SENSE^+$ and $SENSE^-$ Pins

The $SENSE^+$ and $SENSE^-$ pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 12.5V. Both SENSE pins are high impedance inputs with small base currents of

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less than 1µA. When the SENSE pins ramp up from 0V to 1.4V, the small base currents flow out of the SENSE pins. When the SENSE pins ramp down from 12.5V to 1.1V, the small base currents flow into the SENSE pins. The high impedance inputs to the current comparators allow accurate DCR sensing. However, care must be taken not to float these pins during normal operation.

Filter components mutual to the sense lines should be placed close to the LTC3855, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

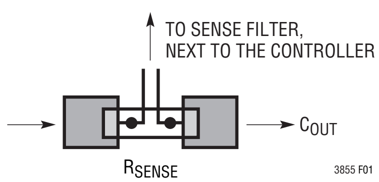


Figure 1. Sense Lines Placement with Sense Resistor

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current.

The current comparator has a maximum threshold $V_{SENSE(MAX)}$ determined by the I_{LIM} setting. The input common mode range of the current comparator is 0V to 12.5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current I_{MAX} equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications, for duty cycles less than 40%.

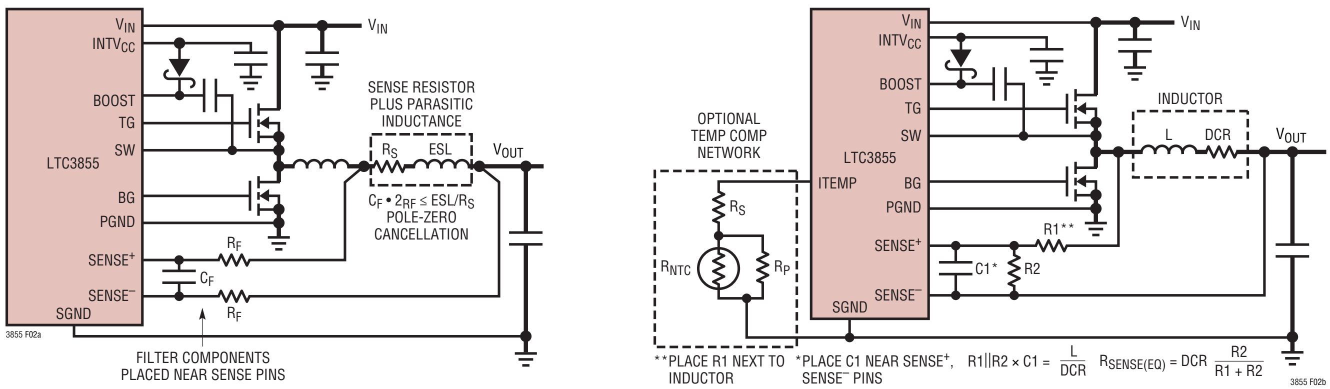
For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628 / LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 2a. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled inthe sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns.

This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 3 illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for the 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}}$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R),

APPLICATIONS INFORMATION



(2a) Using a Resistor to Sense Current

(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

the resulting waveform looks resistive again, as shown in Figure 4. For applications using low maximum sense voltages, check the sense resistor manufacturer's data sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use the equation above to determine the ESL. However, do not over-filter. Keep the RC time constant less than or equal to the inductor time constant to maintain a high enough ripple voltage on V_{RSENSE}.

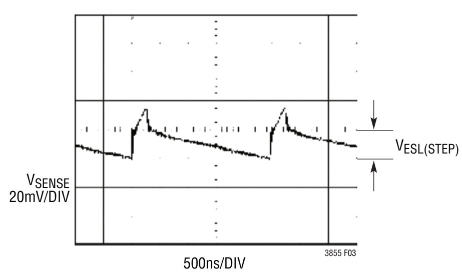


Figure 3. Voltage Waveform Measured Directly Across the Sense Resistor.

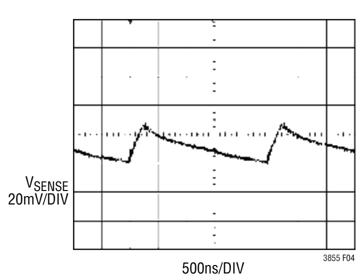


Figure 4. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω.

The above generally applies to high density/high current applications where $I_{(MAX)}$ >10A and low values of inductors are used. For applications where $I_{(MAX)}$ <10A, set R_F to 10 Ohms and C_F to 1000pF. This will provide a good starting point.

The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3855 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing.

If the external R1 || R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not

APPLICATIONS INFORMATION

always the same and varies with temperature; consult the manufacturers' datasheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the Maximum Current Sense Threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (25mV, 45mV, or 68mV, depending on the state of the I_{LIM} pin).

Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C or use LTC3855 DCR temperature compensation function. A conservative value for $T_{L(MAX)}$ is 100°C.

To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{(MAX)} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 0.47µF. This forces R1 || R2 to around 2kΩ, reducing error that might have been caused by the SENSE pins' ±1µA current. $T_{L(MAX)}$ is the maximum inductor temperature.

The equivalent resistance R1 || R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS}\ R1 = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method.

To maintain a good signal to noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV for duty cycles less than 40%. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

NTC Compensated DCR Sensing

For DCR sensing applications where a more accurate current limit is required, a network consisting of an NTC thermistor placed from the ITEMP pin to ground will provide correction of the current limit over temperature. Figure 2b shows this network. Resistors R_S and R_P will linearize the impedance the ITEMP pin sees. To implement NTC compensated DCR sensing, design the DCR sense filter network per the same procedure mentioned in the previous selection, except calculate the divider components using the room temperature value of the DCR. For a single output rail operating from one phase:

1. Set the ITEMP pin resistance to 50k at 25°C. With 10µA flowing out of the ITEMP pin, the voltage on the ITEMP pin will be 0.5V at room temperature. Current limit correction will occur for inductor temperatures greater than 25°C.

2. Calculate the ITEMP pin resistance and the maximum inductor temperature which is typically 100°C. Use the following equations:

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$$R_{ITEMP100C} = \frac{V_{ITEMP100C}}{10\mu A}$$

$$V_{ITEMP100C} = 0.5V - 1.3 \bullet \frac{\frac{I_{MAX} \bullet DCR(MAX) \bullet R2}{R1 + R2} \bullet \frac{(100°C - 25°C) \bullet 0.4}{100}}{V_{SENSE(MAX)}}$$

Calculate the values for R_P and R_S. A simple method is to graph the following R_S versus R_P equations with R_S on the y-axis and R_P on the x-axis.

$R_S = R_{ITEMP25C} - R_{NTC25C} || R_P$

$R_S = R_{ITEMP100C} - R_{NTC100C} || R_P$

Next, find the value of R_P that satisfies both equations which will be the point where the curves intersect. Once R_P is known, solve for R_S.

The resistance of the NTC thermistor can be obtained from the vendor's data sheet either in the form of graphs, tabulated data, or formulas. The approximate value for the NTC thermistor for a given temperature can be calculated from the following equation:

$$R = R_0 \bullet \exp\left(B \bullet \left(\frac{1}{T + 273} - \frac{1}{T_0 + 273}\right)\right)$$

where

R = Resistance at temperature T, which is in degrees C

R_0 = Resistance at temperature T_0, typically 25°C

B = B-constant of the thermistor

Figure 5 shows a typical resistance curve for a 100k thermistor and the ITEMP pin network over temperature.

Starting values for the NTC compensation network are:

- NTC R_0 = 100k
- R_S = 20k
- R_P = 50k

But, the final values should be calculated using the above equations and checked at 25°C and 100°C.

After determining the components for the temperature compensation network, check the results by plotting I_{MAX} versus inductor temperature using the following equations:

$$I_{MAX} = \frac{\frac{V_{SENSEMAX(ADJ)} - \Delta V_{SENSE}}{2}}{DCR(MAX) \text{ at } 25°C \bullet \left(1 + \left(T_{L(MAX)} - 25°C\right) \bullet \frac{0.4}{100}\right)}$$

where

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8V - V_{ITEMP}}{1.3} - A$$

$V_{ITEMP} = 10\mu A \bullet (R_S + R_P || R_{NTC})$

Use typical values for $V_{SENSE(MAX)}$. Subtracting constant A will provide a minimum value for $V_{SENSE(MAX)}$. These values are summarized in Table 2.

Table 2.

I_{LIM}	GND	FLOAT	$INTV_{CC}$
$V_{SENSE(MAX)}$ TYP	30mV	50mV	75mV
A	5mV	5mV	7mV

The resulting current limit should be greater than or equal to I_{MAX} for inductor temperatures between 25°C and 100°C.

Typical values for the NTC compensation network are:

- NTC R_0 = 100k, B-constant = 3000 to 4000
- $R_S \approx$ 20k
- $R_P \approx$ 50k

Generating the I_{MAX} versus inductor temperature curve plot first using the above values as a starting point and then adjusting the R_S and R_P values as necessary is another approach. Figure 6 shows a typical curve of I_{MAX} versus inductor temperature. For PolyPhase applications, tie the ITEMP pins together and calculate for an ITEMP pin current of 10µA • #phases.

The same thermistor network can be used to correct for temperatures less than 25°C. But make sure V_{ITEMP} is

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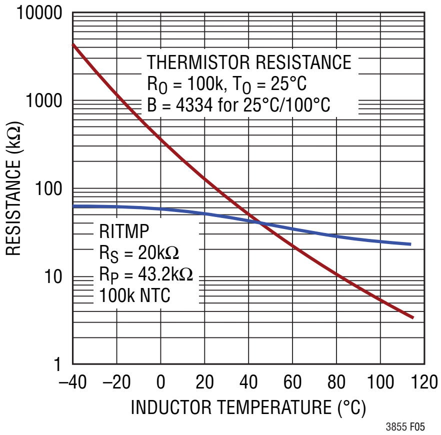


Figure 5. Resistance Versus Temperature for ITEMP Pin Network and the 100k NTC

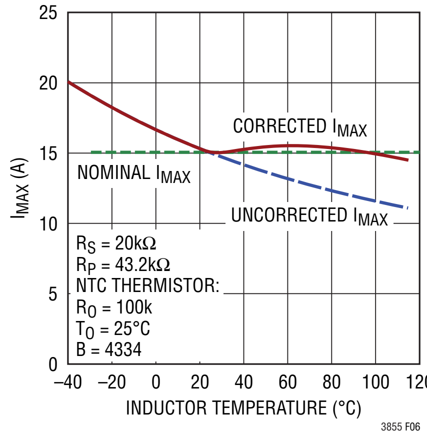


Figure 6. Worst Case I_{MAX} Versus Inductor Temperature Curve with and without NTC Temperature Compensation

greater than 0.2V for duty cycles of 25% or more, otherwise temperature correction may not occur at elevated ambients. For the most accurate temperature detection, place the thermistors next to the inductors as shown in Figure 7. Take care to keep the ITEMP pins away from the switch nodes.

Slope Compensation and Inductor Peak Current

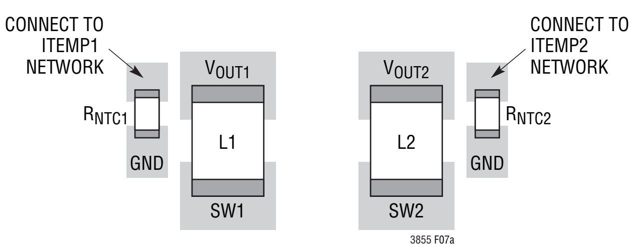
Slope compensation provides stability in constant-frequency architectures by preventing subharmonic oscillations at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles >40%. However, the LTC3855 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

Inductor Value Calculation

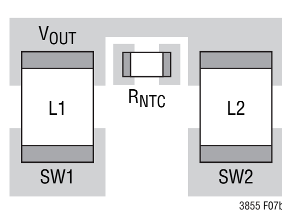
Given the desired input and output voltages, the inductor value and operating frequency f_{OSC} directly determine the inductor's peak-to-peak ripple current:

$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN}}\left(\frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet L}\right)$$

Lower ripple current reduces core losses in the inductor, ESR losses in the output capacitors, and output voltage ripple. Thus, highest efficiency operation is obtained at low frequency with a small ripple current. Achieving this, however, requires a large inductor.



(7a) Dual Output Dual Phase DCR Sensing Application



(7b) Single Output Dual Phase DCR Sensing Application

Figure 7. Thermistor Locations. Place Thermistor Next to Inductor(s) for Accurate Sensing of the Inductor Temperature, but Keep the ITEMP Pins Away from the Switch Nodes and Gate Drive Traces

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A reasonable starting point is to choose a ripple current that is about 40% of $I_{OUT(MAX)}$ for a duty cycle less than 40%. Note that the largest ripple current occurs at the highest input voltage. To guarantee that ripple current does not exceed a specified maximum, the inductor should be chosen according to:

$$L \geq \frac{V_{IN} - V_{OUT}}{f_{OSC} \bullet I_{RIPPLE}} \bullet \frac{V_{OUT}}{V_{IN}}$$

For duty cycles greater than 40%, the 10mV current sense ripple voltage requirement is relaxed because the slope compensation signal aids the signal-to-noise ratio and because a lower limit is placed on the inductor value to avoid subharmonic oscillations. To ensure stability for duty cycles up to the maximum of 95%, use the following equation to find the minimum inductance.

$$L_{MIN} > \frac{V_{OUT}}{f_{SW} \bullet I_{LOAD(MAX)}} \bullet 1.4$$

where

L_{MIN} is in units of µH

f_{SW} is in units of MHz

Inductor Core Selection

Once the inductance value is determined, the type of inductor must be selected. Core loss is independent of core size for a fixed inductor value, but it is very dependent on inductance selected. As inductance increases, core losses go down. Unfortunately, increased inductance requires more turns of wire and therefore copper losses will increase.

Ferrite designs have very low core loss and are preferred at high switching frequencies, so design goals can concentrate on copper loss and preventing saturation. Ferrite core material saturates "hard," which means that inductance collapses abruptly when the peak design current is exceeded. This results in an abrupt increase in inductor ripple current and consequent output voltage ripple. Do not allow the core to saturate!

Power MOSFET and Schottky Diode (Optional) Selection

Two external power MOSFETs must be selected for each controller in the LTC3855: one N-channel MOSFET for the top (main) switch, and one N-channel MOSFET for the bottom (synchronous) switch.

The peak-to-peak drive levels are set by the $INTV_{CC}$ voltage. This voltage is typically 5V during start-up (see $EXTV_{CC}$ Pin Connection). Consequently, logic-level threshold MOSFETs must be used in most applications. The only exception is if low input voltage is expected (V_{IN} < 5V); then, sub-logic level threshold MOSFETs ($V_{GS(TH)}$ < 3V) should be used. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; most of the logic level MOSFETs are limited to 30V or less.

Selection criteria for the power MOSFETs include the on-resistance $R_{DS(ON)}$, Miller capacitance C_{MILLER}, input voltage and maximum output current. Miller capacitance, C_{MILLER}, can be approximated from the gate charge curve usually provided on the MOSFET manufacturers' data sheet. C_{MILLER} is equal to the increase in gate charge along the horizontal axis while the curve is approximately flat divided by the specified change in V_{DS}. This result is then multiplied by the ratio of the application applied V_{DS} to the gate charge curve specified V_{DS}. When the IC is operating in continuous mode the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \frac{V_{IN} - V_{OUT}}{V_{IN}}$$

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The MOSFET power dissipations at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)} + (V_{IN})^2\left(\frac{I_{MAX}}{2}\right)(R_{DR})(C_{MILLER}) \bullet \left[\frac{1}{V_{INTVCC} - V_{TH(MIN)}} + \frac{1}{V_{TH(MIN)}}\right] \bullet f_{OSC}$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}(I_{MAX})^2(1+\delta)R_{DS(ON)}$$

where δ is the temperature dependency of $R_{DS(ON)}$ and R_{DR} (approximately 2Ω) is the effective driver resistance at the MOSFET's Miller threshold voltage. $V_{TH(MIN)}$ is the typical MOSFET minimum threshold voltage.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which are highest at high input voltages. For V_{IN} < 20V the high current efficiency generally improves with larger MOSFETs, while for V_{IN} > 20V the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low or during a short-circuit when the synchronous switch is on close to 100% of the period.

The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs Temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes conduct during the dead time between the conduction of the two power MOSFETs. These prevent the body diodes of the bottom MOSFETs from turning on, storing charge during the dead time and requiring a reverse recovery period that could cost as much as 3% in efficiency at high V_{IN}. A 1A to 3A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition losses due to their larger junction capacitance. A Schottky diode in parallel with the bottom FET may also provide a modest improvement in Burst Mode efficiency.

Soft-Start and Tracking

The LTC3855 has the ability to either soft-start by itself with a capacitor or track the output of another channel or external supply. When one particular channel is configured to soft-start by itself, a capacitor should be connected to its TK/SS pin. This channel is in the shutdown state if its RUN pin voltage is below 1.2V. Its TK/SS pin is actively pulled to ground in this shutdown state.

Once the RUN pin voltage is above 1.2V, the channel powers up. A soft-start current of 1.2µA then starts to charge its soft-start capacitor. Note that soft-start or tracking is achieved not by limiting the maximum output current of the controller but by controlling the output ramp voltage according to the ramp rate on the TK/SS pin. Current foldback is disabled during this phase to ensure smooth soft-start or tracking. The soft-start or tracking range is defined to be the voltage range from 0V to 0.6V on the TK/SS pin. The total soft-start time can be calculated as:

$$t_{SOFTSTART} = 0.6 \bullet \frac{C_{SS}}{1.2\mu A}$$

Regardless of the mode selected by the MODE/PLLIN pin, the regulator will always start in pulse-skipping mode up to TK/SS = 0.5V. Between TK/SS = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TK/SS > 0.54V. The output ripple is minimized during the 40mV forced continuous mode window ensuring a clean PGOOD signal.

When the channel is configured to track another supply, the feedback voltage of the other supply is duplicated by a resistor divider and applied to the TK/SS pin. Therefore, the voltage ramp rate on this pin is determined by the ramp rate of the other supply's voltage. Note that the small soft-start capacitor charging current is always flowing,

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producing a small offset error. To minimize this error, select the tracking resistive divider value to be small enough to make this error negligible.

In order to track down another channel or supply after the soft-start phase expires, the LTC3855 is forced into continuous mode of operation as soon as V_{FB} is below the undervoltage threshold of 0.54V regardless of the setting on the MODE/PLLIN pin. However, the LTC3855 should always be set in force continuous mode tracking down when there is no load. After TK/SS drops below 0.1V, its channel will operate in discontinuous mode.

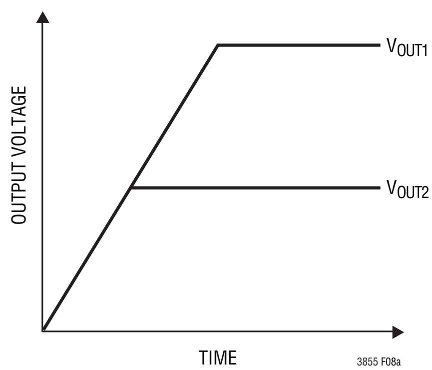
Output Voltage Tracking

The LTC3855 allows the user to program how its output ramps up and down by means of the TK/SS pins. Through these pins, the output can be set up to either coincidentally or ratiometrically track another supply's output, as shown in Figure 8. In the following discussions, V_{OUT1} refers to the LTC3855's output 1 as a master channel and V_{OUT2} refers to the LTC3855's output 2 as a slave channel. In practice, though, either phase can be used as the master.

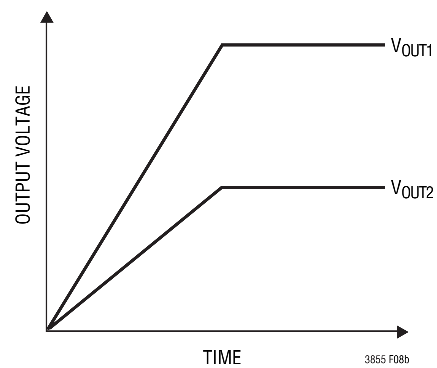
To implement the coincident tracking in Figure 8a, connect an additional resistive divider to V_{OUT1} and connect its midpoint to the TK/SS pin of the slave channel. The ratio of this divider should be the same as that of the slave channel's feedback divider shown in Figure 9a. In this tracking mode, V_{OUT1} must be set higher than V_{OUT2}. To implement the ratiometric tracking in Figure 9b, the ratio of the V_{OUT2} divider should be exactly the same as the master channel's feedback divider shown in Figure 9b. By selecting different resistors, the LTC3855 can achieve different modes of tracking including the two in Figure 8.

So which mode should be programmed? While either mode in Figure 8 satisfies most practical applications, some tradeoffs exist. The ratiometric mode saves a pair of resistors, but the coincident mode offers better output regulation.

When the master channel's output experiences dynamic excursion (under load transient, for example), the slave channel output will be affected as well. For better output regulation, use the coincident tracking mode instead of ratiometric.

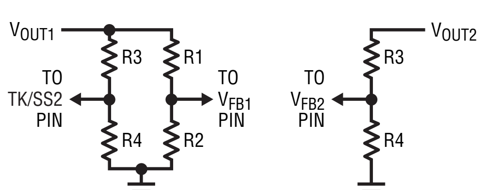


(8a) Coincident Tracking

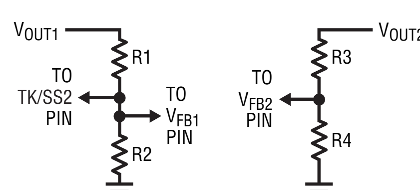


(8b) Ratiometric Tracking

Figure 8. Two Different Modes of Output Voltage Tracking



(9a) Coincident Tracking Setup



(9b) Ratiometric Tracking Setup

Figure 9. Setup for Coincident and Ratiometric Tracking

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$INTV_{CC}$ Regulators and $EXTV_{CC}$

The LTC3855 features a true PMOS LDO that supplies power to $INTV_{CC}$ from the V_{IN} supply. $INTV_{CC}$ powers the gate drivers and much of the LTC3855's internal circuitry. The linear regulator regulates the voltage at the $INTV_{CC}$ pin to 5V when V_{IN} is greater than 5.5V. $EXTV_{CC}$ connects to $INTV_{CC}$ through a P-channel MOSFET and can supply the needed power when its voltage is higher than 4.7V. Each of these can supply a peak current of 100mA and must be bypassed to ground with a minimum of 4.7µF ceramic capacitor or low ESR electrolytic capacitor. No matter what type of bulk capacitor is used, an additional 0.1µF ceramic capacitor placed directly adjacent to the $INTV_{CC}$ and PGND pins is highly recommended. Good bypassing is needed to supply the high transient currents required by the MOSFET gate drivers and to prevent interaction between the channels.

High input voltage applications in which large MOSFETs are being driven at high frequencies may cause the maximum junction temperature rating for the LTC3855 to be exceeded. The $INTV_{CC}$ current, which is dominated by the gate charge current, may be supplied by either the 5V linear regulator or $EXTV_{CC}$. When the voltage on the $EXTV_{CC}$ pin is less than 4.7V, the linear regulator is enabled. Power dissipation for the IC in this case is highest and is equal to $V_{IN} \bullet I_{INTVCC}$. The gate charge current is dependent on operating frequency as discussed in the Efficiency Considerations section. The junction temperature can be estimated by using the equations given in Note 3 of the Electrical Characteristics. For example, the LTC3855 $INTV_{CC}$ current is limited to less than 44mA from a 38V supply in the UJ package and not using the $EXTV_{CC}$ supply:

$$T_J = 70°C + (44mA)(38V)(33°C/W) = 125°C$$

To prevent the maximum junction temperature from being exceeded, the input supply current must be checked while operating in continuous conduction mode (MODE/PLLIN = SGND) at maximum V_{IN}. When the voltage applied to $EXTV_{CC}$ rises above 4.7V, the $INTV_{CC}$ linear regulator is turned off and the $EXTV_{CC}$ is connected to the $INTV_{CC}$. The $EXTV_{CC}$ remains on as long as the voltage applied to $EXTV_{CC}$ remains above 4.5V. Using the $EXTV_{CC}$ allows the MOSFET driver and control power to be derived from one of the LTC3855's switching regulator outputs during normal operation and from the $INTV_{CC}$ when the output is out of regulation (e.g., start-up, short-circuit). If more current is required through the $EXTV_{CC}$ than is specified, an external Schottky diode can be added between the $EXTV_{CC}$ and $INTV_{CC}$ pins. Do not apply more than 6V to the $EXTV_{CC}$ pin and make sure that $EXTV_{CC} < V_{IN}$.

Significant efficiency and thermal gains can be realized by powering $INTV_{CC}$ from the output, since the V_{IN} current resulting from the driver and control currents will be scaled by a factor of (Duty Cycle)/(Switcher Efficiency).

Tying the $EXTV_{CC}$ pin to a 5V supply reduces the junction temperature in the previous example from 125°C to:

$$T_J = 70°C + (44mA)(5V)(33°C/W) = 77°C$$

However, for 3.3V and other low voltage outputs, additional circuitry is required to derive $INTV_{CC}$ power from the output.

The following list summarizes the four possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ left open (or grounded). This will cause $INTV_{CC}$ to be powered from the internal 5V regulator resulting in an efficiency penalty of up to 10% at high input voltages.
2. $EXTV_{CC}$ connected directly to V_{OUT}. This is the normal connection for a 5V regulator and provides the highest efficiency.
3. $EXTV_{CC}$ connected to an external supply. If a 5V external supply is available, it may be used to power $EXTV_{CC}$ providing it is compatible with the MOSFET gate drive requirements.
4. $EXTV_{CC}$ connected to an output-derived boost network. For 3.3V and other low voltage regulators, efficiency gains can still be realized by connecting $EXTV_{CC}$ to an output-derived voltage that has been boosted to greater than 4.7V.

For applications where the main input power is below 5V, tie the V_{IN} and $INTV_{CC}$ pins together and tie the combined pins to the 5V input with a 1Ω or 2.2Ω resistor as shown in Figure 10 to minimize the voltage drop caused by the gate charge current. This will override the $INTV_{CC}$ linear regulator and will prevent $INTV_{CC}$ from dropping too low

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due to the dropout voltage. Make sure the $INTV_{CC}$ voltage is at or exceeds the $R_{DS(ON)}$ test voltage for the MOSFET which is typically 4.5V for logic level devices.

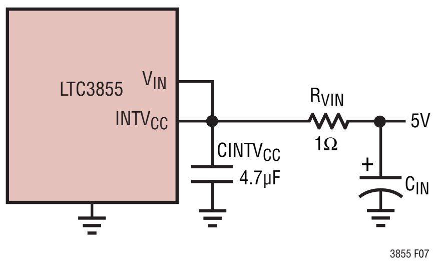

Figure 10. Setup for a 5V Input

Topside MOSFET Driver Supply (C_B, DB)

External bootstrap capacitors C_B connected to the BOOST pins supply the gate drive voltages for the topside MOSFETs. Capacitor C_B in the Functional Diagram is charged though external diode DB from $INTV_{CC}$ when the SW pin is low. When one of the topside MOSFETs is to be turned on, the driver places the C_B voltage across the gate source of the desired MOSFET. This enhances the MOSFET and turns on the topside switch. The switch node voltage, SW, rises to V_{IN} and the BOOST pin follows. With the topside MOSFET on, the boost voltage is above the input supply: $V_{BOOST} = V_{IN} + V_{INTVCC}$. The value of the boost capacitor C_B needs to be 100 times that of the total input capacitance of the topside MOSFET(s). The reverse breakdown of the external Schottky diode must be greater than $V_{IN(MAX)}$. When adjusting the gate drive level, the final arbiter is the total input current for the regulator. If a change is made and the input current decreases, then the efficiency has improved. If there is no change in input current, then there is no change in efficiency.

Undervoltage Lockout

The LTC3855 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.2V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 600mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pins have a precision turn-on reference of 1.2V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.2V. One can program the hysteresis of the run comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.5V.

C_{IN} and C_{OUT} Selection

The selection of C_{IN} is simplified by the 2-phase architecture and its impact on the worst-case RMS current drawn through the input network (battery/fuse/capacitor). It can be shown that the worst-case capacitor RMS current occurs when only one controller is operating. The controller with the highest $(V_{OUT})(I_{OUT})$ product needs to be used in the formula below to determine the maximum RMS capacitor current requirement. Increasing the output current drawn from the other controller will actually decrease the input RMS ripple current from its maximum value. The out-of-phase technique typically reduces the input capacitor's RMS ripple current by a factor of 30% to 70% when compared to a single phase power supply solution.

In continuous mode, the source current of the top MOSFET is a square wave of duty cycle $(V_{OUT})/(V_{IN})$. To prevent large voltage transients, a low ESR capacitor sized for the maximum RMS current of one channel must be used. The maximum RMS capacitor current is given by:

$$C_{IN} \text{ Required } I_{RMS} \approx \frac{I_{MAX}}{V_{IN}}\left[\left(V_{OUT}\right)\left(V_{IN}-V_{OUT}\right)\right]^{1/2}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT}/2$. This simple worst-case condition is commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturers' ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor, or to choose a capacitor rated at a higher temperature than required. Several capacitors may be paralleled to meet size or height requirements in the design. Due to the high operating frequency of the LTC3855, ceramic capacitors