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2-Phase Synchronous Step-Down DC/DC Controller with Diffamp

FEATURES

- **PolyPhase® Controller Reduces Input and Output Capacitance and Power Supply Induced Noise**
- **Wide V_{IN} Range: 4.5V to 38V Operation**
- **±0.75%, 0.6V Reference Voltage Accuracy**
- **High Efficiency: Up to 95%**
- **Programmable Burst Mode® Operation or Stage Shedding™ for Highest Light Load Efficiency**
- **Active Voltage Positioning (AVP)**
- **R_{SENSE} or DCR Current Sensing**
- **Programmable DCR Temperature Compensation**
- **Phase-Lockable Fixed Frequency: 250kHz to 770kHz**
- **True Remote Sense Differential Amplifier**
- **Dual N-Channel MOSFET Synchronous Drive**
- V_{OUT} Range: 0.6V to 5V without Differential Amplifier
- V_{OUT} Range: 0.6V to 3.3V with Differential Amplifier
- Adjustable Soft-Start or V_{OUT} Tracking
- Stackable for Up to 12-Phase Operation
- 32-Pin (5mm × 5mm) QFN and 38-Pin TSSOP Packages

APPLICATIONS

- Telecom and Datacom Systems
- Industrial and Medical Instruments
- DC Power Distribution Systems
- Computer Systems

DESCRIPTION

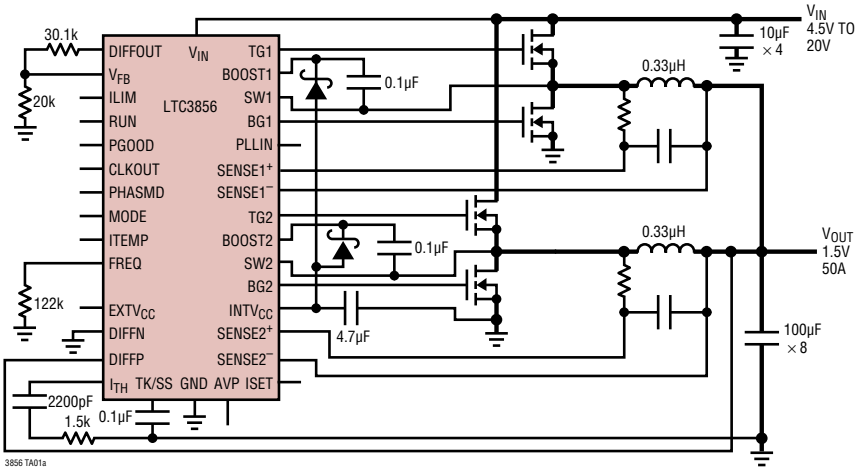
The LTC®3856 is a single output, dual channel PolyPhase synchronous step-down DC/DC controller that drives all N-channel power MOSFET stages. This device includes a high speed differential amplifier for remote output voltage sense. Power loss and supply noise are minimized by operating the two controller output stages out-of-phase and up to 12-phase operation can be achieved.

The LTC3856 monitors the output current by sensing the voltage drop across the output inductor (DCR) or by using a sense resistor. DCR temperature compensation maintains an accurate current sense threshold over a broad temperature range. A constant-frequency, current mode architecture allows a phase-lockable frequency of up to 770kHz.

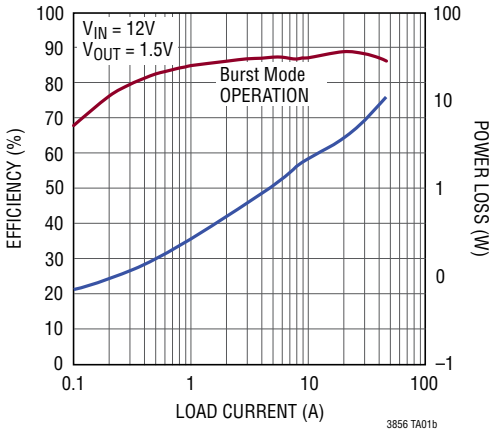
A wide 4.5V to 38V input supply range encompasses most intermediate bus voltages and battery chemistries. Burst Mode operation, continuous or Stage Shedding modes are supported. A TK/SS pin shared by both channels ramps the output voltage during start-up.

TYPICAL APPLICATION

High Efficiency 1.5V/50A Step-Down Converter



Efficiency and Power Loss vs Output Current

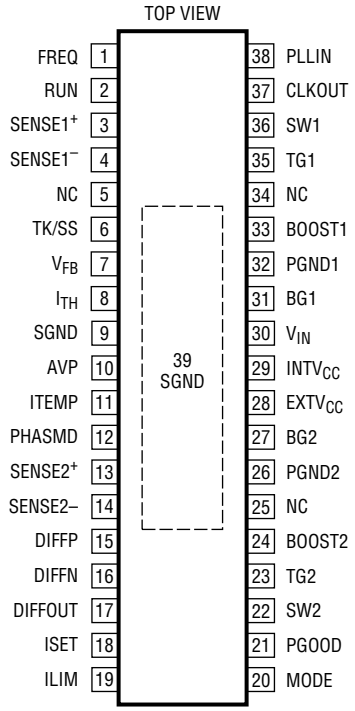


ABSOLUTE MAXIMUM RATINGS (Note 1)

Input Supply Voltage (V_{IN}) ..... 40V to –0.3V
Topside Driver Voltages (BOOSTn) ..... 46V to –0.3V
Switch Voltage (SWn) ..... 40V to –5V
$INTV_{CC}$, RUN, PGOOD, $EXTV_{CC}$,
(BOOSTn – SWn) ..... 6V to –0.3V
SENSEn Voltages ..... 5.5V to –0.3V
MODE, PLLIN, ILIM, TK/SS, AVP,
FREQ, ISET Voltages ..... $INTV_{CC}$ to –0.3V
DIFFP, DIFFN, DIFFOUT, PHASMD,
ITEMP Voltages ..... $INTV_{CC}$ to –0.3V

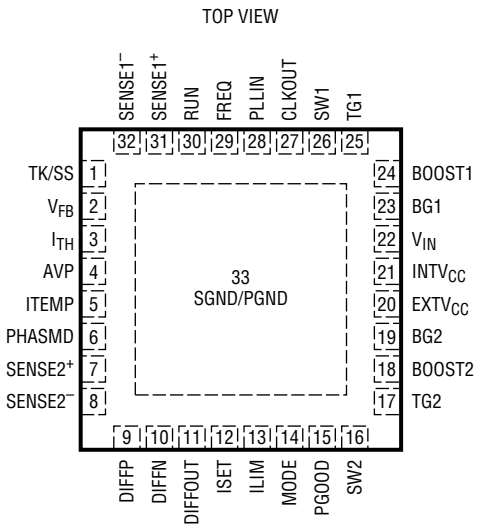
I_{TH}, V_{FB} Voltages ..... $INTV_{CC}$ to –0.3V
$INTV_{CC}$ Peak Output Current 100mA
Operating Junction Temperature Range
(Notes 2, 3) ..... –40°C to 125°C
Storage Temperature Range ..... –65°C to 125°C
Reflow Peak Body Temperature (UH Package) ..... 260°C
Lead Temperature (Soldering, 10 sec.)
FE Package ..... 300°C

PIN CONFIGURATION



FE PACKAGE
38-LEAD PLASTIC TSSOP

T_{JMAX} = 125°C, θ_{JA} = 25°C/W
EXPOSED PAD (PIN 39) IS SGND/PGND, MUST BE SOLDERED TO PCB



UH PACKAGE
32-LEAD (5mm × 5mm) PLASTIC QFN

T_{JMAX} = 125°C, θ_{JA} = 34°C/W
EXPOSED PAD (PIN 33) IS SGND/PGND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC3856EFE#PBF	LTC3856EFE#TRPBF	LTC3856FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3856IFE#PBF	LTC3856IFE#TRPBF	LTC3856FE	38-Lead Plastic TSSOP	–40°C to 125°C
LTC3856EUH#PBF	LTC3856EUH#TRPBF	3856	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C
LTC3856IUH#PBF	LTC3856IUH#TRPBF	3856	32-Lead (5mm × 5mm) Plastic QFN	–40°C to 125°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Main Control Loops							
V_{IN}	Input Voltage			4.5		38	V
V_{OUT}	Output Voltage			0.6		5.0	V
V_{FB}	Regulated Feedback Voltage	I_{TH} Voltage = 1.2V, E-Grade (Note 4) I_{TH} Voltage = 1.2V, I-Grade (Note 4)	● ●	0.5955 0.593	0.600 0.600	0.6045 0.607	V V
I_{FB}	Feedback Current	(Note 4)			–15	–50	nA
$V_{REFLNREG}$	Reference Voltage Line Regulation	V_{IN} = 4.5V to 38V (Note 4)			0.002	0.02	%/V
$V_{LOADREG}$	Output Voltage Load Regulation	(Note 4) Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 0.7V Measured in Servo Loop, ΔI_{TH} Voltage = 1.2V to 1.6V	 ● ●		 0.01 –0.01	 0.1 –0.1	 % %
g_m	Transconductance Amplifier g_m	I_{TH} = 1.2V, Sink/Source 5µA (Note 4)			2.0		mmho
I_Q	Input DC Supply Current Normal Mode Shutdown	(Note 5) V_{IN} = 15V V_{RUN} = 0V			 4.0 40	 70	 mA µA
DF_{MAX}	Maximum Duty Factor	In Dropout; f_{OSC} = 500kHz		93	94		%
UVLO	Undervoltage Lockout	V_{INTVCC} Ramping Down	●	3.0	3.2	3.4	V
UVLO Hyst	UVLO Hysteresis				0.6		V
V_{OVL}	Feedback Overvoltage Lockout	Measured at V_{FB}	●	0.64	0.66	0.68	V
I_{SENSE+}	SENSE+ Pins Bias Current	Each Channel, $V_{SENSE1,2}$ = 3.3V	●		±1	±2	µA
I_{TEMP}	DCR Tempco Compensation Current	V_{ITEMP} = 0.3V	●	9	10	11	µA
$I_{TK/SS}$	Soft-Start Charge Current	$V_{TK/SS}$ = 0V	●	1.0	1.25	1.5	µA
V_{RUN}	RUN Pin On Threshold	V_{RUN} Rising	●	1.1	1.22	1.35	V
V_{RUNHYS}	RUN Pin On Hysteresis				80		mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (E-Grade)	V_{FB} = 0.5V, $V_{SENSE1,2}$ = 3.3V I_{LIM} = 0V I_{LIM} = Float I_{LIM} = $INTV_{CC}$	 ● ● ●	 25 45 68	 30 50 75	 35 55 82	 mV mV mV
$V_{SENSE(MAX)}$	Maximum Current Sense Threshold (I-Grade)	V_{FB} = 0.5V, $V_{SENSE1,2}$ = 3.3V I_{LIM} = 0V I_{LIM} = Float I_{LIM} = $INTV_{CC}$	 ● ● ●	 23 43 66	 30 50 75	 37 57 84	 mV mV mV

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
	TG Transition Time	(Note 6)					
TG1,2 t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
TG1,2 t_f	Fall Time	C_{LOAD} = 3300pF			25		ns
	BG Transition Time	(Note 6)					
BG1,2 t_r	Rise Time	C_{LOAD} = 3300pF			25		ns
BG1,2 t_f	Fall Time	C_{LOAD} = 3300pF			25		ns
TG/BG t_{1D}	Top Gate Off to Bottom Gate On Delay Synchronous Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
BG/TG t_{2D}	Bottom Gate Off to Top Gate On Delay Top Switch-On Delay Time	C_{LOAD} = 3300pF Each Driver			30		ns
$t_{ON(MIN)}$	Minimum On-Time	(Note 7)			90		ns
$INTV_{CC}$ Linear Regulator							
V_{INTVCC}	Internal V_{CC} Voltage	6V < V_{IN} ≤ 38V		4.8	5.0	5.2	V
V_{LDO} INT	$INTV_{CC}$ Load Regulation	I_{CC} = 0mA to 20mA			0.5	2.0	%
V_{EXTVCC}	$EXTV_{CC}$ Switchover Voltage	$EXTV_{CC}$ Ramping Positive	●	4.5	4.7		V
V_{LDO} EXT	$EXTV_{CC}$ Voltage Drop	I_{CC} = 20mA, V_{EXTVCC} = 5V			50	100	mV
V_{LDOHYS}	$EXTV_{CC}$ Hysteresis				200		mV
Oscillator and Phase-Locked Loop							
f_{NOM}	Nominal Frequency	V_{FREQ} = 1.2V		450	500	550	kHz
f_{LOW}	Lowest Frequency	V_{FREQ} = 0V		210	250	290	kHz
f_{HIGH}	Highest Frequency	V_{FREQ} ≥ 2.4V		700	770	850	kHz
R_{MODE}	MODE Input Resistance				250		kΩ
I_{FREQ}	Frequency Setting Output Current			9	10	11	µA
CLKOUT	Phase (Relative to Controller 1)	PHASMD = GND; Non Stage Shedding Mode PHASMD = FLOAT; Non Stage Shedding Mode PHASMD = $INTV_{CC}$; Non Stage Shedding Mode Stage Shedding Mode			60 90 120 180		Deg Deg Deg Deg
CLKHIGH	Clock High Output Voltage			4	5		V
CLKLOW	Clock Low Output Voltage				0	0.2	V
PGOOD Output							
V_{PGL}	PGOOD Voltage Low	I_{PGOOD} = 2mA			0.1	0.2	V
I_{PGOOD}	PGOOD Leakage Current	V_{PGOOD} = 5V				±2	µA
V_{PG}	PGOOD Trip Level, Either Controller	V_{FB} with Respect to Set Output Voltage V_{FB} Ramping Negative V_{FB} Ramping Positive			 –10 10		 % %

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 15V, V_{RUN} = 5V, unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Differential Amplifier							
A_{DA}	Gain	E-Grade I-Grade	● ●	0.998 0.997	1 1	1.002 1.003	V/V V/V
R_{IN}	Input Resistance	Measured at DIFFP Input			80		kΩ
V_{OS}	Input Offset Voltage	V_{DIFFP} = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA				2	mV
PSRR	Power Supply Rejection Ratio	4.5V < V_{IN} < 38V			100		dB
I_{CL}	Maximum Output Current			2	3		mA
$V_{OUT(MAX)}$	Maximum Output Voltage	$I_{DIFFOUT}$ = 300µA		V_{INTVCC} –1.4	V_{INTVCC} –1.1		V
On-Chip Driver							
TG R_{UP}	TG Pull-Up $R_{DS(ON)}$	TG High			2.6		Ω
TG R_{DOWN}	TG Pull-Down $R_{DS(ON)}$	TG Low			1.5		Ω
BG R_{UP}	BG Pull-Up $R_{DS(ON)}$	BG High			2.4		Ω
BG R_{DOWN}	BG Pull-Down $R_{DS(ON)}$	BG Low			1.1		Ω
GBW	Gain-Bandwidth Product	(Note 8)			3		MHz
SR	Slew Rate	(Note 8)			2		V/µs
Stage Shedding Mode							
I_{ISET}	Programmable Stage Shedding Mode Current			6.5	7.5	8.5	µA
AVP (Active Voltage Positioning)							
V_{AVP}	Maximum V_{OUT} with AVP				2.5		V
I_{SINK}	Sink Current of AVP Pin	$SENSE^+$ = 1.2V			250		µA
I_{SOURCE}	Source Current of AVP Pin	$SENSE^+$ = 1.2V			2		mA
V_{AVP}-$V_{O(MAX)}$	Maximum Voltage Drop V_{AVP} to V_O	$SENSE^+$ = 1.2V			120		mV

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTC3856 is tested under pulse load conditions such that $T_J \approx T_A$. The LTC3856E is guaranteed to meet performance specifications from 0°C to 85°C operating junction temperature. Specifications over the –40°C to 125°C operating junction temperature range are assured by design, characterization and correlation with statistical process controls. The LTC3856I is guaranteed to meet performance specifications over the full –40°C to 125°C operating junction temperature range.

Note 3: T_J is calculated from the ambient temperature, T_A, and power dissipation, P_D, according to the following formula:

LTC3856UH: $T_J = T_A + (P_D \bullet 34°C/W)$
LTC3856FE: $T_J = T_A + (P_D \bullet 25°C/W)$

Note 4: The LTC3856 is tested in a feedback loop that servos V_{ITH} to a specified voltage and measures the resultant V_{FB}.

Note 5: Dynamic supply current is higher due to the gate charge being delivered at the switching frequency. See the Applications Information section.

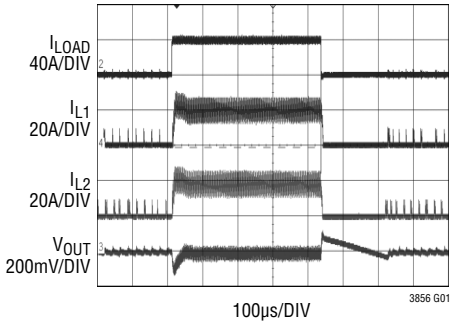
Note 6: Rise and fall times are measured using 10% and 90% levels. Delay times are measured using 50% levels.

Note 7: The minimum on-time condition corresponds to the on inductor peak-to-peak ripple current ≥40% of I_{MAX} (see Minimum On-Time Considerations in the Applications Information section).

Note 8: Guaranteed by design.

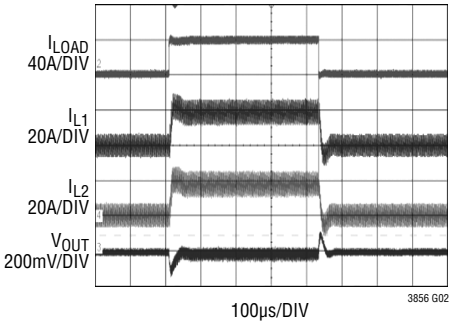
TYPICAL PERFORMANCE CHARACTERISTICS

Load Step: Burst Mode Operation



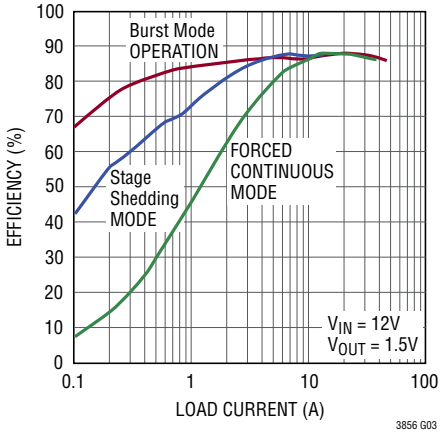
V_{IN} = 12V
V_{OUT} = 1.5V
I_{LOAD} = 1A TO 40A

Load Step: Forced Continuous Mode

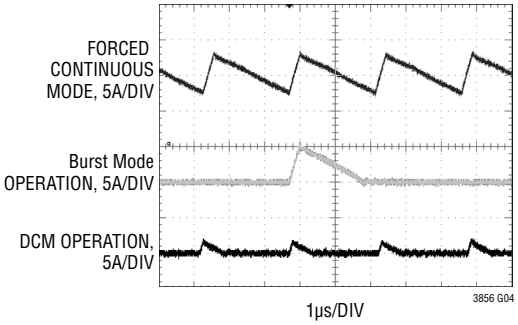


V_{IN} = 12V
V_{OUT} = 1.5V
I_{LOAD} = 1A TO 40A

Efficiency vs Output Current and Mode

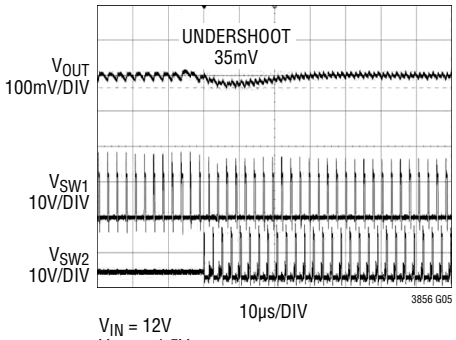


Inductor Current at Light Load



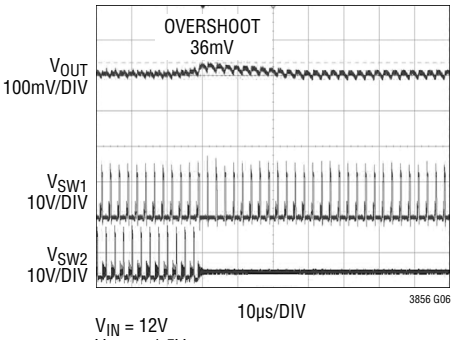
V_{IN} = 12V
V_{OUT} = 1.5V
I_{LOAD} = 400mA

Stage Shedding Transition, 1-Phase to 2-Phase



V_{IN} = 12V
V_{OUT} = 1.5V

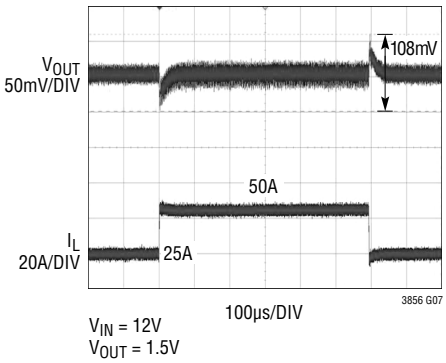
Stage Shedding Transition, 2-Phase to 1-Phase



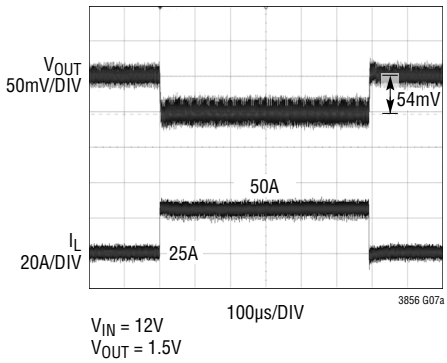
V_{IN} = 12V
V_{OUT} = 1.5V

TYPICAL PERFORMANCE CHARACTERISTICS

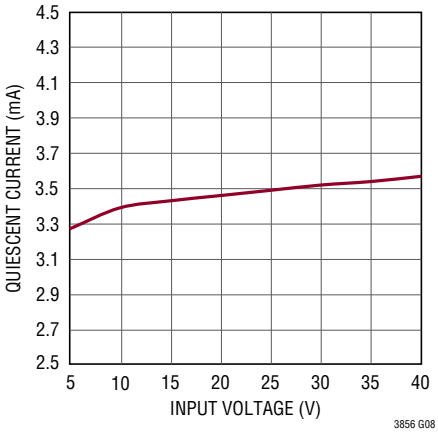
Load Step without AVP



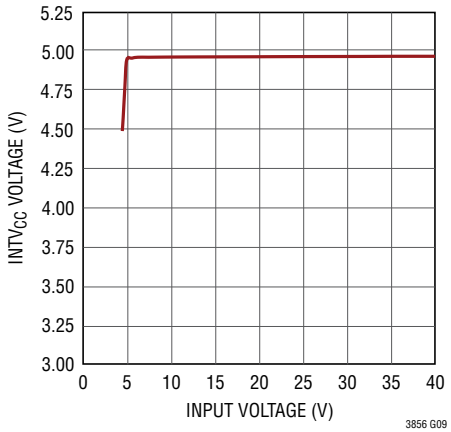
Load Step with AVP



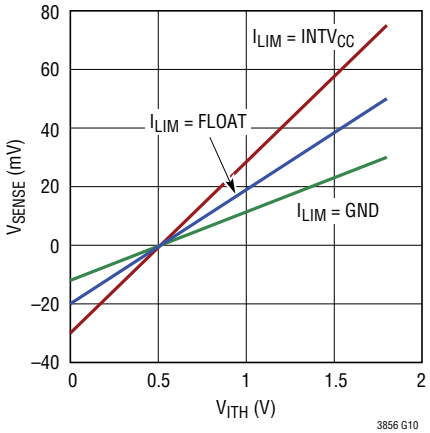
Quiescent Current vs Input Voltage without EXTVCC



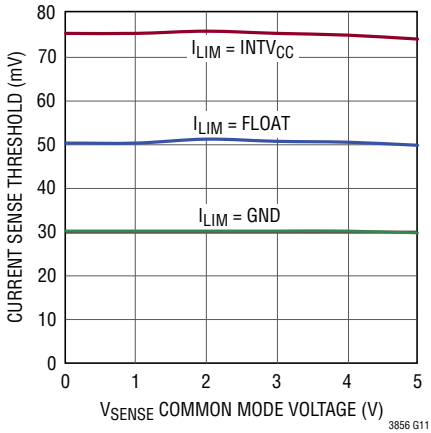
INTVCC Line Regulation



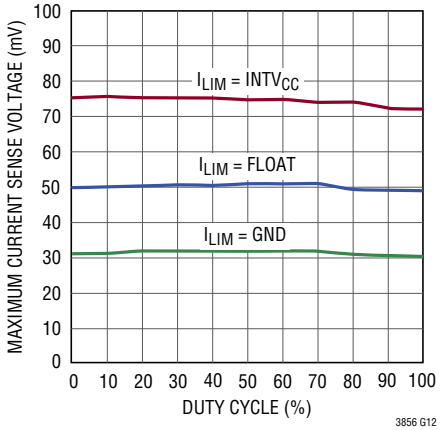
Current Sense Threshold vs ITH Voltage



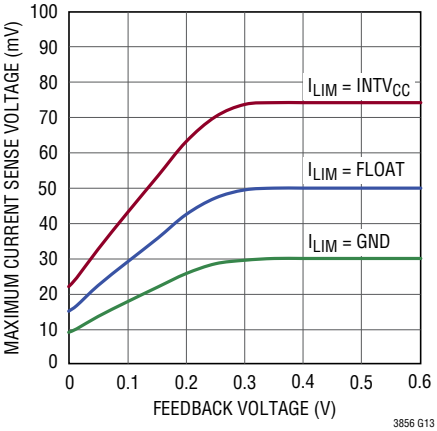
Maximum Current Sense Threshold vs Common Mode Voltage



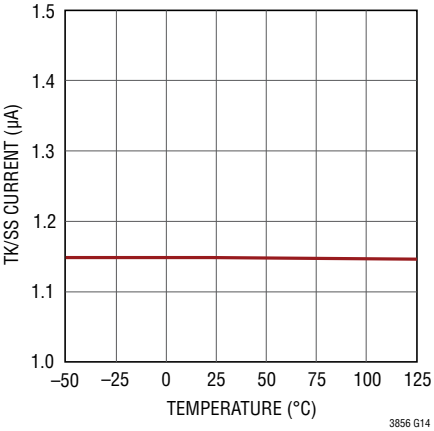
Maximum Current Sense Voltage vs Duty Cycle



Maximum Current Sense Voltage vs Feedback Voltage (Current Foldback)

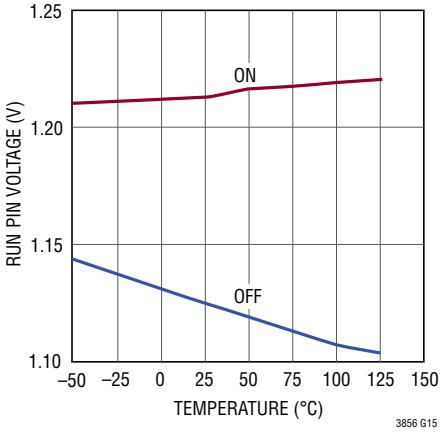


TK/SS Pull-Up Current vs Temperature

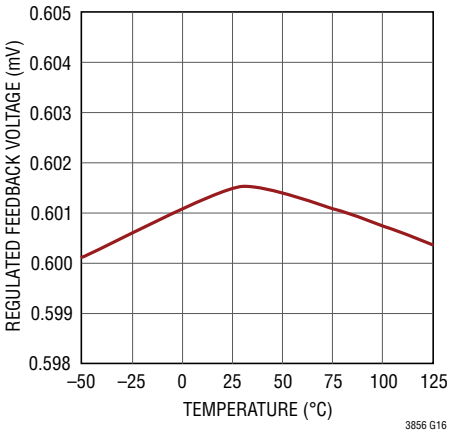


TYPICAL PERFORMANCE CHARACTERISTICS

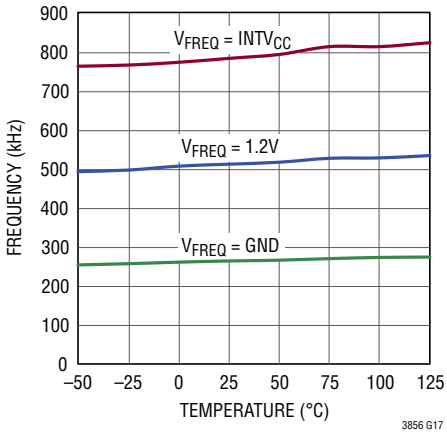
Shutdown (RUN) Threshold vs Temperature



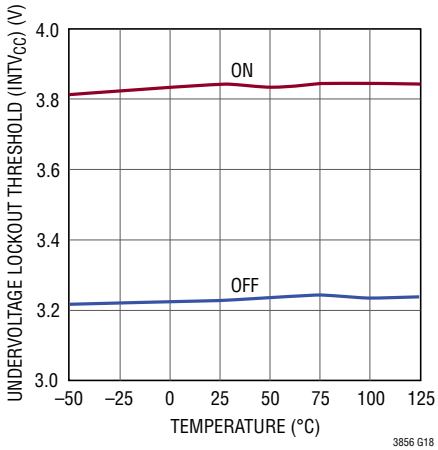
Regulated Feedback Voltage vs Temperature



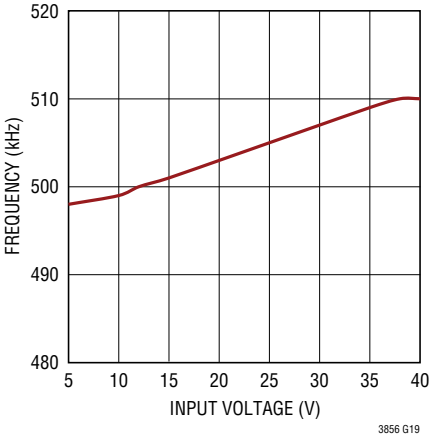
Oscillator Frequency vs Temperature



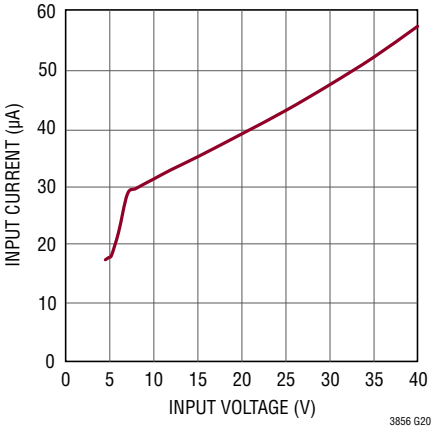
Undervoltage Lockout Threshold ($INTV_{CC}$) vs Temperature



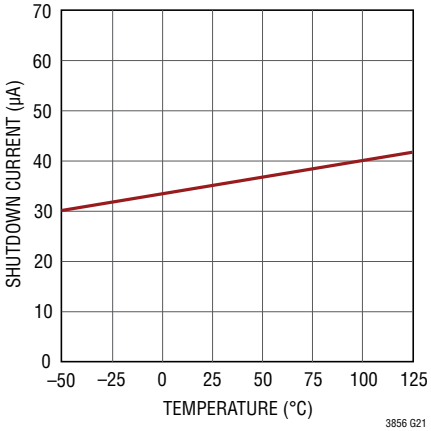
Oscillator Frequency vs Input Voltage



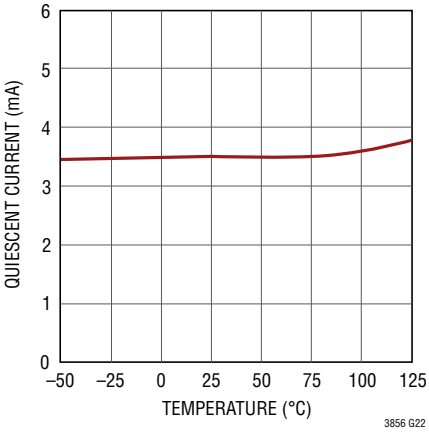
Shutdown Current vs Input Voltage



Shutdown Current vs Temperature



Quiescent Current vs Temperature without $EXTV_{CC}$



PIN FUNCTIONS (TSSOP/QFN)

FREQ (Pin 1/Pin 29): Frequency Setting Pin. A resistor to ground sets the operating frequency of the controller. This pin can also be driven with a DC voltage to vary the frequency of the internal oscillator.

RUN (Pin 2/Pin 30): Run Control Input. A voltage above 1.22V on this pin turns on the IC. There is a 1µA pull-up current for this pin. Once the RUN pin rises above 1.22V, an additional 4.5µA pull-up current is added to the pin.

SENSE1$^+$, SENSE2$^+$ (Pins 3, 13/Pins 31, 7): Current Sense Comparator Inputs. The (+) inputs to the current comparators are normally connected to DCR sensing networks or current sensing resistors.

SENSE1$^-$, SENSE2$^-$ (Pins 4, 14/Pins 32, 8): Current Sense Comparator Inputs. The (–) inputs to the current comparators are connected to the outputs.

NC (Pins 5, 25, 34) TSSOP Package: No Connections.

TK/SS (Pin 6/Pin 1): Output Voltage Tracking and Soft-Start Input. When one particular IC is configured to be the master of two ICs, a capacitor to ground at this pin sets the ramp rate for the master IC's output voltage. When the IC is configured to be the slave of two ICs, the V_{FB} voltage of the master IC is reproduced by a resistor divider and applied to this pin. An internal soft-start current of 1.25µA is charging this pin.

V_{FB} (Pin 7/Pin 2): Error Amplifier Feedback Input. This pin receives the remotely sensed feedback voltage from an external resistive divider.

I_{TH} (Pin 8/Pin 3): Current Control Threshold and Error Amplifier Compensation Point. Each associated channels' current comparator tripping threshold increases with I_{TH} control voltage.

SGND (Pin 9/Pin 33): Signal Ground and Power Ground. All small-signal components and compensation components should connect to this ground, which in turn connects to PGND at one point.

AVP (Pin 10/Pin 4): Active Voltage Positioning Load Slope Programming Pin. A resistor between this pin and the DIFFP pin sets the load slope. The AVP function can only be used with the remote sensing differential amplifier. Float or connect a 1k resistor to DIFFP pin when AVP function is not used.

ITEMP (Pin 11/Pin 5): Input to the Temperature Sensing Circuit. Connect this pin to an external NTC (negative temperature coefficient) resistor placed near the heat source on the PCB board (e.g., inductors) changes the controller's current limit with temperature.

PHASMD (Pin 12/Pin 6): Connect this pin to SGND, $INTV_{CC}$, or float this pin to select the phase of CLKOUT to be 60°, 120° and 90°, respectively.

DIFFP (Pin 15/Pin 9): Positive Input of Remote Sensing Differential Amplifier. Must connect this pin directly to the remote load voltage or local V_{OUT} even when AVP or diffamp is not used.

DIFFN (Pin 16/Pin 10): Negative Input of Remote Sensing Differential Amplifier. Connect this pin to the negative terminal of output load capacitors.

DIFFOUT (Pin 17/Pin 11): Output of Remote Sensing Differential Amplifier. Connect this pin to V_{FB} through a resistive divider.

ISET (Pin 18/Pin 12): Stage Shedding Mode Comparator and Burst Mode Comparator Programming Pin. A resistor to ground programs the threshold of the Stage Shedding mode comparator or Burst Mode comparator threshold and current limit.

I_{LIM} (Pin 19/Pin 13): Current Comparator Sense Voltage Range Input. This pin is to be programmed to SGND, FLOAT or $INTV_{CC}$ to set the maximum current sense threshold to one of three different levels for both comparators.

MODE (Pin 20/Pin 14): Forced Continuous Mode, Burst Mode Operation or Stage Shedding Mode Selection Pin. Connect this pin to SGND to force IC in continuous mode of operation. Connect to $INTV_{CC}$ to enable Stage Shedding mode operation. Leaving the pin floating enables Burst Mode operation.

PGOOD (Pin 21/Pin 15): Power Good Indicator Output. Open-drain logic out that is pulled to ground when the output exceeds the ±10% regulation window, after the internal 20µs power-bad mask timer expires.

PIN FUNCTIONS (TSSOP/QFN)

$EXTV_{CC}$ (Pin 28/Pin 20): External Power Input to an Internal Switch Connected to $INTV_{CC}$. This switch closes and supplies the IC power, bypassing the internal low dropout regulator, whenever $EXTV_{CC}$ is higher than 4.7V. Do not exceed 6V on this pin and ensure $V_{IN} > V_{EXTVCC}$ at all times.

$INTV_{CC}$ (Pin 29/Pin 21): Internal 5V Regulator Output. The control circuits are powered from this voltage. Decouple this pin to PGND with a minimum of 4.7µF low ESR tantalum or ceramic capacitor.

V_{IN} (Pin 30/Pin 22): Main Input Supply. Decouple this pin to PGND with a capacitor (0.1µF to 1µF).

BG1, BG2 (Pins 31, 27/Pins 23, 19): Bottom Gate Driver Outputs. These pins drive the gates of the bottom N-channel MOSFETs between $INTV_{CC}$ and PGND.

PGND1, PGND2 (Pins 32, 26) TSSOP Package: Power Ground Pin. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (–) terminal of CV_{CC} and the (–) terminal of C_{IN}.

BOOST1, BOOST2 (Pins 33, 24/Pins 24, 18): Boosted Floating Driver Supplies. The (+) terminal of the bootstrap capacitors connect to these pins. These pins swing from a diode voltage drop below $INTV_{CC}$ up to $V_{IN} + INTV_{CC}$.

SGND/PGND (Exposed Pad Pin 33) QFN Package: Signal Ground and Power Ground. Connect this pin closely to the sources of the bottom N-channel MOSFETs, the (–) terminal of CV_{CC} and the (–) terminal of C_{IN}. All small-signal components and compensation components should also connect to this ground.

TG1, TG2 (Pins 35, 23/Pins 25, 17): Top Gate Driver Outputs. These are the outputs of floating drivers with a voltage swing equal to $INTV_{CC}$ superimposed on the switch nodes voltages.

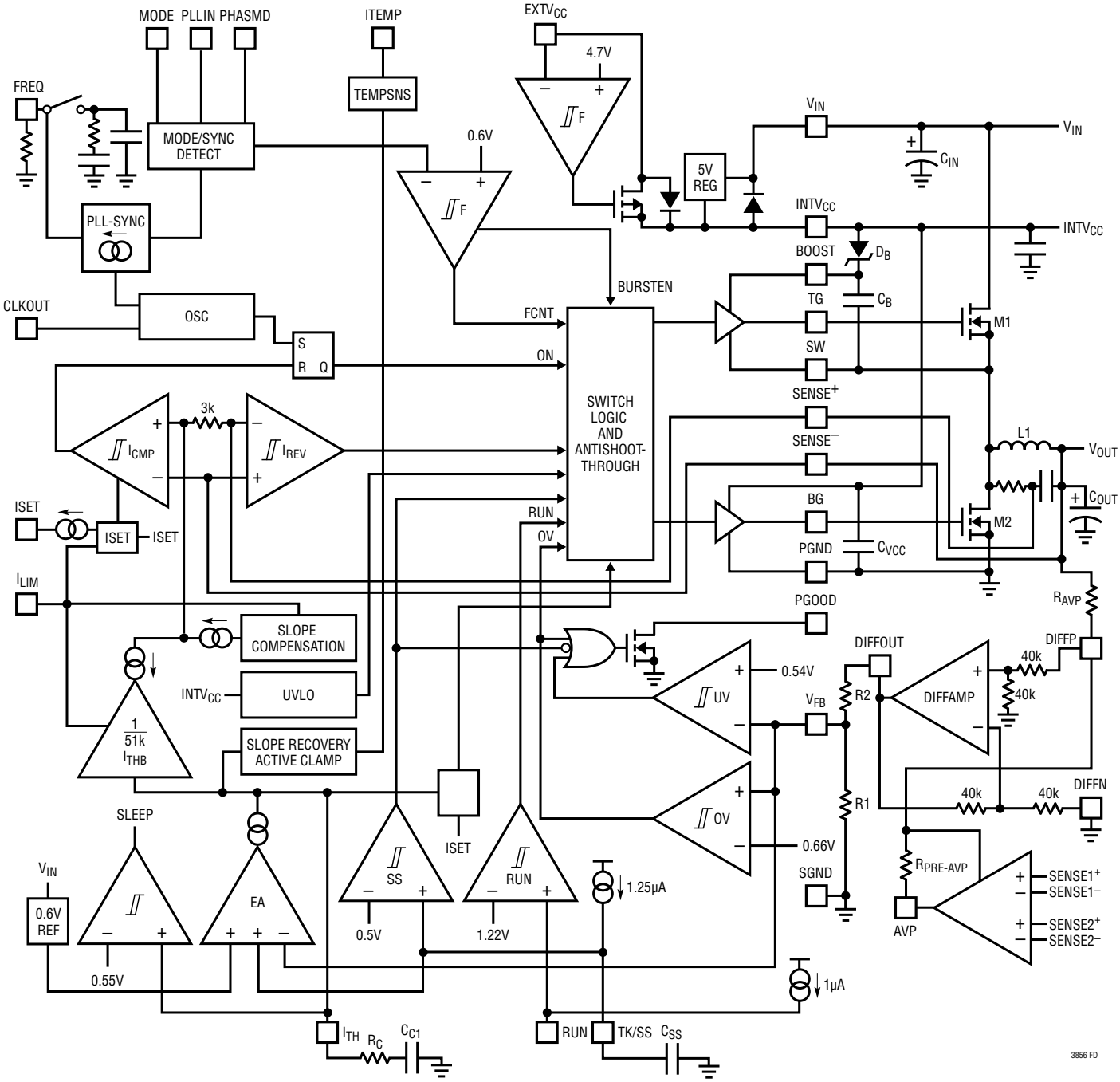
SW1, SW2 (Pins 36, 22/Pins 26, 16): Switch Node Connections to Inductors. Voltage swing at these pins is from a Schottky diode (external) voltage drop below ground to V_{IN}.

CLKOUT (Pin 37/Pin 27): Clock output with phase changeable by PHASMD to enable usage of multiple LTC3856 ICs in multiphase systems.

PLLIN (Pin 38/Pin 28): External Synchronization Pin. A clock on the pin synchronizes the internal oscillator with the clock on this pin.

SGND (Exposed Pad Pin 39) TSSOP Package: The exposed pad must be soldered to PCB ground for electrical connection and rated thermal performance.

FUNCTIONAL DIAGRAM



OPERATION (Refer to Functional Diagram)

Main Control Loop

The LTC3856 uses a constant-frequency, current mode step-down architecture. During normal operation, each top MOSFET is turned on each cycle when the oscillator sets the RS latch, and turned off when the main current comparator, I_{CMP}, resets each RS latch. The peak inductor current at which I_{CMP} resets the RS latch is controlled by the voltage on the I_{TH} pin, which is the output of the error amplifier, EA. The V_{FB} pin receives a portion of output voltage feedback signal via the DIFFOUT pin (if DIFFAMP is used) through the external resistive divider and is compared to the internal reference voltage. When the load current increases, it causes a slight decrease in the V_{FB} pin voltage relative to the 0.6V reference, which in turn causes the I_{TH} voltage to increase until each inductor's average current matches half of the new load current (assuming the two current sensing resistors are equal). In Burst Mode operation, after each top MOSFET has turned off, the bottom MOSFET is turned on until either the inductor current starts to reverse, as indicated by the reverse current comparator, I_{REV}, or the beginning of the next cycle.

The main control loop is shut down by pulling the RUN pin low. Releasing RUN allows an internal 1µA current source to pull up the RUN pin. When the RUN pin reaches 1.22V, the main control loop is enabled and the IC is powered up. When the RUN pin is low, all functions are kept in a controlled state.

$INTV_{CC}/EXTV_{CC}$ Power

Power for the top and bottom MOSFET drivers and most other internal circuitry is derived from the $INTV_{CC}$ pin. When the $EXTV_{CC}$ pin is left open or tied to a voltage less than 4.7V, an internal 5V linear regulator supplies $INTV_{CC}$ power from V_{IN}. If $EXTV_{CC}$ is taken above 4.7V, the 5V regulator is turned off and an internal switch is turned on connecting $EXTV_{CC}$. Using the $EXTV_{CC}$ pin allows the $INTV_{CC}$ power to be derived from a high efficiency external source such as a switching regulator output. Each top MOSFET driver is biased from the floating bootstrap capacitor, C_B, which normally recharges during each off cycle through an external diode when the top MOSFET turns off. If the input voltage, V_{IN}, decreases to a voltage close to V_{OUT}, the loop may enter dropout and attempt to turn on the top MOSFET continuously. The dropout detector detects this and forces the top MOSFET off for about one-twelfth of the clock period plus 100ns every third cycle to allow C_B to recharge. However, it is recommended that a load be present or the IC operates at low frequency during the dropout transition to ensure C_B is recharged.

Shutdown and Start-Up (RUN and TK/SS Pins)

The LTC3856 can be shut down using the RUN pin. Pulling the RUN pin below 1.22V shuts down the main control loop for the controller and most internal circuits, including the $INTV_{CC}$ regulator. Releasing the RUN pin allows an internal 1µA current to pull up the pin and enable the controller. Alternatively, the RUN pin may be externally pulled up or driven directly by logic. Be careful not to exceed the absolute maximum rating of 6V on this pin. The start-up of the controller's output voltage, V_{OUT}, is controlled by the voltage on the TK/SS pin. When the voltage on the TK/SS pin is less than the 0.6V internal reference, the LTC3856 regulates the V_{FB} voltage to the TK/SS pin voltage instead of the 0.6V reference. This allows the TK/SS pin to be used to program a soft-start by connecting an external capacitor from the TK/SS pin to SGND. An internal 1.25µA pull-up current charges this capacitor, creating a voltage ramp on the TK/SS pin. As the TK/SS voltage rises linearly from 0V to 0.6V (and beyond), the output voltage, V_{OUT}, rises smoothly from zero to its final value. Alternatively, the TK/SS pin can be used to cause the start-up of V_{OUT} to track that of another supply. Typically, this requires connecting to the TK/SS pin an external resistor divider from the other supply to ground (see the Applications Information section). When the RUN pin is pulled low to disable the controller, or when $INTV_{CC}$ drops below its undervoltage lockout threshold of 3.2V, the TK/SS pin is pulled low by an internal MOSFET. When in undervoltage lockout, all phases of the controller are disabled and the external MOSFETs are held off.

OPERATION (Refer to Functional Diagram)

Light Load Current Operation (Burst Mode Operation, Stage Shedding or Continuous Conduction)

The LTC3856 can be enabled to enter high efficiency Burst Mode operation, Stage Shedding mode or forced continuous conduction mode. To select forced continuous operation, tie the MODE pin to a DC voltage below 0.6V (e.g., SGND). To select Stage Shedding mode of operation, tie the MODE pin to $INTV_{CC}$. To select Burst Mode operation, float the MODE pin.

When the controller is enabled for Burst Mode operation, the peak current in the inductor is set to approximately one-sixth of the maximum sense voltage even though the voltage on the I_{TH} pin indicates a lower value. The peak current can be programmed by the ISET pin. If the average inductor current is higher than the load current, the error amplifier, EA, will decrease the voltage on the I_{TH} pin. When the I_{TH} voltage drops, the internal sleep signal goes high (enabling sleep mode) and the external MOSFETs are turned off. In sleep mode, the load current is supplied by the output capacitor. As the output voltage decreases, the EA's output begins to rise. When the output voltage drops enough, the sleep signal goes low, and the controller resumes normal operation by turning on the top external MOSFET on the next cycle of the internal oscillator. When a controller is enabled for Burst Mode operation, the inductor current is not allowed to reverse. The reverse current comparator, I_{REV}, turns off the bottom external MOSFET just before the inductor current reaches zero, preventing it from reversing and going negative. Thus, the controller operates in discontinuous operation. In forced continuous operation, the inductor current is allowed to reverse at light loads or under large transient conditions. The peak inductor current is determined by the voltage on the I_{TH} pin, just as in normal operation. In this mode, the efficiency at light loads is lower than in Burst Mode operation. However, continuous mode has the advantages of lower output ripple and less interference with audio circuitry.

When the MODE pin is connected to $INTV_{CC}$, the LTC3856 operates in Stage Shedding mode at light loads. The controller will turn off channel 2 and increase the current gain of the first channel to ensure a smooth transition. The threshold where the controller goes into Stage Shedding mode is where the I_{TH} voltage drops below 0.5V, but it can be programmed by the ISET pin. The inductor current is not allowed to reverse in this mode (discontinuous operation). At very light loads, the current comparator may remain tripped for several cycles and force the external top MOSFET to stay off for the same number of cycles (i.e., skipping pulses). This mode exhibits low output ripple as well as low audio noise and reduced RF interference as compared to Burst Mode operation. It provides a higher low current efficiency than forced continuous mode, but not nearly as high as Burst Mode operation.

Multichip Operations (PHASMD and CLKOUT Pins)

The LTC3856's two channels are 180° out-of-phase, providing multiphase operation. This configuration can provide enough power for most of the high current applications. However, for even higher power applications, the LTC3856 can be configured for PolyPhase and multichip operation. The LTC3856 features PHASMD and CLKOUT pins which enable multiple LTC3856s to operate out-of-phase, as shown in Table 1. The CLKOUT signal is out-of-phase with respect to phase 1 of the controller depending on the PHASMD pin setting. In Stage Shedding mode, however, the CLKOUT signal is 180° out-of-phase with respect to phase 1 of the controller.

Table 1.

PHASMD	GND	FLOAT	$INTV_{CC}$
Phase 1	0°	0°	0°
Phase 2	180°	180°	240°
CLKOUT	60°	90°	120°

Frequency Selection and Phase-Locked Loop (FREQ and PLLIN Pins)

The selection of switching frequency is a trade-off between efficiency and component size. Low frequency operation increases efficiency by reducing MOSFET switching losses, but requires larger inductance and/or capacitance to maintain low output ripple voltage.

If the PLLIN pin is not being driven by an external clock source, the FREQ pin can be used to program the control-

OPERATION (Refer to Functional Diagram)

ler's operating frequency from 250kHz to 770kHz. There is a precision 10µA current flowing out of the FREQ pin enabling the user to program the controller's switching frequency with a single resistor to SGND. A curve is provided later in the Applications Information section showing the relationship between the voltage on the FREQ pin and switching frequency.

A phase-locked loop (PLL) is available on the LTC3856 to synchronize the internal oscillator to an external clock source that is connected to the PLLIN pin. The PLL loop filter network is integrated inside the LTC3856. The phase-locked loop is capable of locking any frequency within the range of 250kHz to 770kHz. The frequency setting resistor should always be present to set the controller's initial switching frequency before locking to the external clock.

Sensing the Output Voltage with a Differential Amplifier

The LTC3856 includes a low offset, unity-gain, high bandwidth differential amplifier for applications that require true remote sensing. Sensing the load across the load capacitors directly greatly benefits regulation in high current, low voltage applications, where board interconnection losses can be a significant portion of the total error budget.

The LTC3856 differential amplifier has a typical output slew rate of 2V/µs. The amplifier is configured for unity gain, meaning that the difference between DIFFP and DIFFN is translated to DIFFOUT, relative to SGND.

Care should be taken to route the DIFFP and DIFFN PCB traces parallel to each other all the way to the terminals of the output capacitor or remote sensing points on the board. In addition, avoid routing these sensitive traces near any high speed switching nodes in the circuit. Ideally, the DIFFP and DIFFN traces should be shielded by a low impedance ground plane to maintain signal integrity.

The maximum output voltage when using the differential amplifier is $INTV_{CC}$ – 1.4V (typically 3.6V). The differential amplifier should not be used above this voltage.

Power Good (PGOOD Pin)

The PGOOD pin is connected to an open drain of an internal N-channel MOSFET. The MOSFET turns on and pulls the PGOOD pin low when either V_{FB} pin voltage is not within ±10% of the 0.6V reference voltage. The PGOOD pin is also pulled low when the RUN pin is below 1.22V or when the LTC3856 is in the soft-start or tracking phase. When the V_{FB} pin voltage is within the ±10% regulation window, the MOSFET is turned off and the pin is allowed to be pulled up by an external resistor to a source of up to 6V. The PGOOD pin will flag power good immediately when V_{FB} is within the regulation window. However, there is an internal 20µs power-bad mask when V_{FB} goes out of the regulation window.

Output Overvoltage Protection

An overvoltage comparator, OV, guards against transient overshoots (>10%) as well as other more serious conditions that may overvoltage the output. In such cases, the top MOSFET is turned off and the bottom MOSFET is turned on until the overvoltage condition is cleared.

Undervoltage Lockout

The LTC3856 has two functions that help protect the controller in case of undervoltage conditions. A precision UVLO comparator constantly monitors the $INTV_{CC}$ voltage to ensure that an adequate gate-drive voltage is present. It locks out the switching action when $INTV_{CC}$ is below 3.2V. To prevent oscillation when there is a disturbance on the $INTV_{CC}$, the UVLO comparator has 600mV of precision hysteresis.

Another way to detect an undervoltage condition is to monitor the V_{IN} supply. Because the RUN pin has a precision turn-on reference of 1.22V, one can use a resistor divider to V_{IN} to turn on the IC when V_{IN} is high enough. An extra 4.5µA of current flows out of the RUN pin once the RUN pin voltage passes 1.22V. The RUN comparator itself has about 80mV of hysteresis. One can program additional hysteresis for the RUN comparator by adjusting the values of the resistive divider. For accurate V_{IN} undervoltage detection, V_{IN} needs to be higher than 4.5V.

APPLICATIONS INFORMATION

The Typical Application on the first page of this data sheet is a basic LTC3856 application circuit. LTC3856 can be configured to use either DCR (inductor resistance) sensing or low value resistor sensing. The choice between the two current sensing schemes is largely a design trade-off between cost, power consumption and accuracy. DCR sensing is becoming popular because it saves expensive current sensing resistors and is more power efficient, especially in high current applications. However, current sensing resistors provide the most accurate current limits for the controller. Other external component selection is driven by the load requirement, and begins with the selection of R_{SENSE} (if R_{SENSE} is used) and inductor value. Next, the power MOSFETs are selected. Finally, input and output capacitors are selected.

Current Limit Programming

The I_{LIM} pin is a tri-level logic input which sets the maximum current limit of the controller. When I_{LIM} is either grounded, floated or tied to $INTV_{CC}$, the typical value for the maximum current sense threshold will be 30mV, 50mV or 75mV, respectively.

Which setting should be used? For the best current limit accuracy, use the 75mV setting. The 30mV setting will allow for the use of very low DCR inductors or sense resistors, but at the expense of current limit accuracy. The 50mV setting is a good balance between the two.

SENSE+ and SENSE– Pins

The SENSE+ and SENSE– pins are the inputs to the current comparators. The common mode input voltage range of the current comparators is 0V to 5V. All SENSE+ pins are high impedance inputs with small currents of less than 1µA. The positive high impedance input to the current comparators allows accurate DCR sensing. All SENSE– pins and DIFFP should be connected directly to V_{OUT} when DCR sensing is used. Care must be taken not to float these pins during normal operation. Filter components mutual to the sense lines should be placed close to the LTC3856, and the sense lines should run close together to a Kelvin connection underneath the current sense element (shown in Figure 1). Sensing current elsewhere can effectively add parasitic inductance and capacitance to the current sense element, degrading the information at the sense terminals and making the programmed current limit unpredictable. If DCR sensing is used (Figure 2b), sense resistor R1 should be placed close to the switching node, to prevent noise from coupling into sensitive small-signal nodes. The capacitor C1 should be placed close to the IC pins.

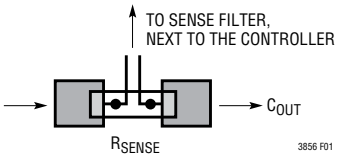
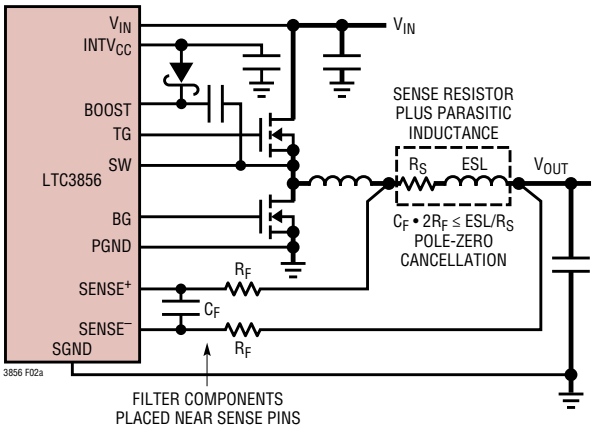
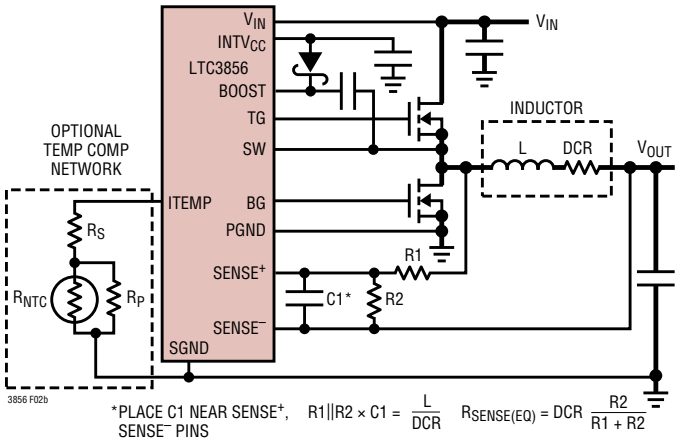


Figure 1. Sense Lines Placement with Sense Resistor



(2a) Using a Resistor to Sense Current



(2b) Using the Inductor DCR to Sense Current

Figure 2. Two Different Methods of Sensing Current

APPLICATIONS INFORMATION

Low Value Resistors Current Sensing

A typical sensing circuit using a discrete resistor is shown in Figure 2a. R_{SENSE} is chosen based on the required output current. The current comparator has a maximum threshold, $V_{SENSE(MAX)}$, determined by the I_{LIM} setting. The input common mode range of the current comparator is 0V to 5V. The current comparator threshold sets the peak of the inductor current, yielding a maximum average output current, I_{MAX}, equal to the peak value less half the peak-to-peak ripple current, ΔI_L. To calculate the sense resistor value, use the equation:

$$R_{SENSE} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

Because of possible PCB noise in the current sensing loop, the AC current sensing ripple of $\Delta V_{SENSE} = \Delta I_L \bullet R_{SENSE}$ also needs to be checked in the design to get a good signal-to-noise ratio. In general, for a reasonably good PCB layout, a 10mV ΔV_{SENSE} voltage is recommended as a conservative number to start with, either for R_{SENSE} or DCR sensing applications. For previous generation current mode controllers, the maximum sense voltage was high enough (e.g., 75mV for the LTC1628/LTC3728 family) that the voltage drop across the parasitic inductance of the sense resistor represented a relatively small error. For today's highest current density solutions, however, the value of the sense resistor can be less than 1mΩ and the peak sense voltage can be as low as 20mV. In addition, inductor ripple currents greater than 50% with operation up to 1MHz are becoming more common. Under these conditions the voltage drop across the sense resistor's parasitic inductance is no longer negligible. A typical sensing circuit using a discrete resistor is shown in Figure 2a. In previous generations of controllers, a small RC filter placed near the IC was commonly used to reduce the effects of capacitive and inductive noise coupled in the sense traces on the PCB. A typical filter consists of two series 10Ω resistors connected to a parallel 1000pF capacitor, resulting in a time constant of 20ns. This same RC filter, with minor modifications, can be used to extract the resistive component of the current sense signal in the presence of parasitic inductance. For example, Figure 3 illustrates the voltage waveform across a 2mΩ sense resistor with a 2010 footprint for the 1.2V/15A converter operating at 100% load. The waveform is the superposition of a purely resistive component and a purely inductive component. It was measured using two scope probes and waveform math to obtain a differential measurement. Based on additional measurements of the inductor ripple current and the on-time and off-time of the top switch, the value of the parasitic inductance was determined to be 0.5nH using the equation:

$$ESL = \frac{V_{ESL(STEP)}}{\Delta I_L} \frac{t_{ON} \bullet t_{OFF}}{t_{ON} + t_{OFF}} \quad (1)$$

If the RC time constant is chosen to be close to the parasitic inductance divided by the sense resistor (L/R), the resulting waveform looks resistive again, as shown in Figure 4. For applications using low maximum sense voltages, check the sense resistor manufacturer's data

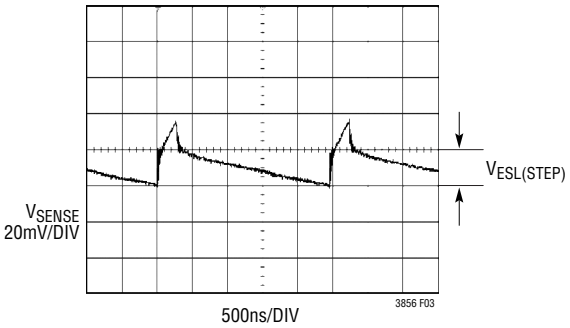


Figure 3. Voltage Waveform Measured Directly Across the Sense Resistor

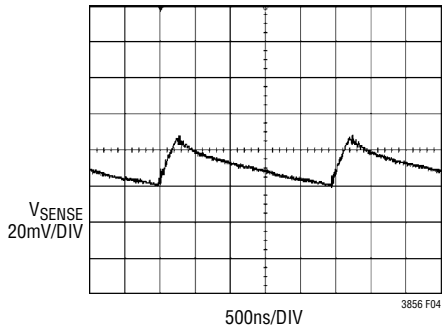


Figure 4. Voltage Waveform Measured After the Sense Resistor Filter. C_F = 1000pF, R_F = 100Ω

APPLICATIONS INFORMATION

sheet for information about parasitic inductance. In the absence of data, measure the voltage drop directly across the sense resistor to extract the magnitude of the ESL step and use Equation 1 to determine the ESL. However, do not overfilter. Keep the RC time constant, less than or equal to the inductor time constant to maintain a high enough ripple voltage of ΔV_{SENSE}. The equation generally applies to high density/high current applications where I_{MAX} > 10A and low values of inductors are used. For applications where I_{MAX} < 10A, set R_F to 10Ω and C_F to 1000pF. This will provide a good starting point. The filter components need to be placed close to the IC. The positive and negative sense traces need to be routed as a differential pair and Kelvin connected to the sense resistor.

Inductor DCR Sensing

For applications requiring the highest possible efficiency at high load currents, the LTC3856 is capable of sensing the voltage drop across the inductor DCR, as shown in Figure 2b. The DCR of the inductor represents the small amount of DC winding resistance of the copper, which can be less than 1mΩ for today's low value, high current inductors. In a high current application requiring such an inductor, conduction loss through a sense resistor would cost several points of efficiency compared to DCR sensing. If the external R1|| R2 • C1 time constant is chosen to be exactly equal to the L/DCR time constant, the voltage drop across the external capacitor is equal to the drop across the inductor DCR multiplied by R2/(R1 + R2). R2 scales the voltage across the sense terminals for applications where the DCR is greater than the target sense resistor value. To properly dimension the external filter components, the DCR of the inductor must be known. It can be measured using a good RLC meter, but the DCR tolerance is not always the same and varies with temperature; consult the manufacturers' data sheets for detailed information.

Using the inductor ripple current value from the Inductor Value Calculation and Output Ripple Current section, the target sense resistor value is:

$$R_{SENSE(EQUIV)} = \frac{V_{SENSE(MAX)}}{I_{(MAX)} + \frac{\Delta I_L}{2}}$$

To ensure that the application will deliver full load current over the full operating temperature range, choose the minimum value for the maximum current sense threshold ($V_{SENSE(MAX)}$) in the Electrical Characteristics table (25mV, 45mV or 68mV, depending on the state of the I_{LIM} pin). Next, determine the DCR of the inductor. Where provided, use the manufacturer's maximum value, usually given at 20°C. Increase this value to account for the temperature coefficient of resistance, which is approximately 0.4%/°C. A conservative value for $T_{L(MAX)}$ is 100°C. To scale the maximum inductor DCR to the desired sense resistor value, use the divider ratio:

$$R_D = \frac{R_{SENSE(EQUIV)}}{DCR_{MAX} \text{ at } T_{L(MAX)}}$$

C1 is usually selected to be in the range of 0.047µF to 0.47µF. This forces R1|| R2 to around 2k, reducing error that might have been caused by the SENSE+ pins' ±1µA current. $T_{L(MAX)}$ is the maximum inductor temperature. The equivalent resistance R1|| R2 is scaled to the room temperature inductance and maximum DCR:

$$R1||R2 = \frac{L}{(DCR \text{ at } 20°C) \bullet C1}$$

The sense resistor values are:

$$R1 = \frac{R1||R2}{R_D}; \quad R2 = \frac{R1 \bullet R_D}{1 - R_D}$$

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The LTC3856 also features a DCR temperature compensation circuit by using a NTC temperature sensor. See the Inductor DCR Sensing Temperature Compensation and the ITEMP Pin section for details.

The maximum power loss in R1 is related to duty cycle, and will occur in continuous mode at the maximum input voltage:

$$P_{LOSS\ R1} = \frac{\left(V_{IN(MAX)} - V_{OUT}\right) \bullet V_{OUT}}{R1}$$

Ensure that R1 has a power rating higher than this value. If high efficiency is necessary at light loads, consider this power loss when deciding whether to use DCR sensing or sense resistors. Light load power loss can be modestly higher with a DCR network than with a sense resistor, due to the extra switching losses incurred through R1. However, DCR sensing eliminates a sense resistor, reduces conduction losses and provides higher efficiency at heavy loads. Peak efficiency is about the same with either method. To maintain a good signal-to-noise ratio for the current sense signal, use a minimum ΔV_{SENSE} of 10mV for duty cycles less than 40%. For a DCR sensing application, the actual ripple voltage will be determined by the equation:

$$\Delta V_{SENSE} = \frac{V_{IN} - V_{OUT}}{R1 \bullet C1} \frac{V_{OUT}}{V_{IN} \bullet f_{OSC}}$$

Inductor DCR Sensing Temperature Compensation and the ITEMP Pin

Inductor DCR current sensing provides a lossless method of sensing the instantaneous current. Therefore, it can provide higher efficiency for applications of high output currents. However, the DCR of the inductor, which is the small amount of DC winding resistance of the copper, typically has a positive temperature coefficient. As the temperature of the inductor rises, its DCR value increases. The current limit of the controller is therefore reduced.

The LTC3856 offers a method to counter this inaccuracy by allowing the user to place an NTC temperature sensing resistor near the inductor to actively correct this error. The ITEMP pin, when left floating, is at a voltage around 5V and DCR temperature compensation is disabled. The ITEMP pin has a constant 10µA precision current flowing out of the pin. By connecting an NTC resistor from the ITEMP pin to SGND, the maximum current sense threshold can be varied over temperature according the following equation:

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8 - V_{ITEMP}}{1.3}$$

where:

$V_{SENSEMAX(ADJ)}$ is the maximum adjusted current sense threshold at temperature.

$V_{SENSE(MAX)}$ is the maximum current sense threshold specified in the Electrical Characteristics table. It is typically 75mV, 50mV or 30mV, depending on the setting I_{LIM} pins.

V_{ITEMP} is the voltage of the ITEMP pin.

The valid voltage range for DCR temperature compensation on the ITEMP pin is between 0.5V to 0.2V, with 0.5V or above being no DCR temperature correction and 0.2V the maximum correction. However, if the duty cycle of the controller is less than 25%, the ITEMP range is extended from 0.5V to 0V.

The NTC resistor has a negative temperature coefficient, meaning its value decreases as temperature rises. The V_{ITEMP} voltage, therefore, decreases as temperature increases and in turn, the $V_{SENSEMAX(ADJ)}$ will increase to compensate the DCR temperature coefficient. The NTC resistor, however, is nonlinear and the user can linearize its value by building a resistor network with regular resistors. Consult the NTC manufacture data sheets for detailed information.

Another use for the ITEMP pins, in addition to NTC compensated DCR sensing, is adjusting $V_{SENSE(MAX)}$ to values between the nominal values of 30mV, 50mV and 75mV for a more precise current limit. This is done by applying a voltage less than 0.5V to the ITEMP pin. $V_{SENSE(MAX)}$ will be varied per the previous equation and the same duty cycle limitations will apply. The current limit can be adjusted using this method either with a sense resistor or DCR sensing.

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NTC Compensated DCR Sensing

For DCR sensing applications where a more accurate current limit is required, a network consisting of an NTC thermistor placed from the ITEMP pin to ground will provide correction of the current limit over temperature. Figure 2b shows this network. Resistors R_S and R_P will linearize the impedance the ITEMP pin sees. To implement NTC compensated DCR sensing, design the DCR sense filter network per the same procedure mentioned in the previous selection, except calculate the divider components using the room temperature value of the DCR. For a typical application:

1. Set the ITEMP pin resistance to 50k at 25°C. With 10µA flowing out of the ITEMP pin, the voltage on the ITEMP pin will be 0.5V at room temperature. Current limit correction will occur for inductor temperatures greater than 25°C.
2. Calculate the ITEMP pin resistance and the maximum inductor temperature, which is typically 100°C. Use the following equations:

$$R_{ITEMP100C} = \frac{V_{ITEMP100C}}{10\mu A}$$

$$V_{ITEMP100C} = 0.5V - 1.3 \bullet \frac{I_{MAX} \bullet DCR_{MAX} \bullet \frac{R2}{R1+R2} \bullet (100°C - 25°C) \bullet \frac{0.4}{100}}{V_{SENSE(MAX)}}$$

Calculate the values for R_P and R_S. A simple method is to graph the following R_S versus R_P equations with R_S on the y-axis and R_P on the x-axis.

$$R_S = R_{ITEMP25C} - R_{NTC25C} || R_P$$

$$R_S = R_{ITEMP100C} - R_{NTC100C} || R_P$$

Next, find the value of R_P that satisfies both equations, which will be the point where the curves intersect. Once R_P is known, solve for R_S.

The resistance of the NTC thermistor can be obtained from the vendor's data sheet either in the form of graphs, tabulated data or formulas. The approximate value for the NTC thermistor for a given temperature can be calculated from the following equation:

$$R = R_0 \bullet \exp\left[B \bullet \left(\frac{1}{T+273} - \frac{1}{T_0+273}\right)\right]$$

Where

R = resistance at temperature T, in degrees C
R_0 = resistance at temperature T_0, typically 25°C
B = B-constant of the thermistor.

Figure 5 shows a typical resistance curve for a 100k thermistor and the ITEMP pin network over temperature.

Starting values for the NTC compensation network are:

- NTC R_0 = 100k
- R_S = 20k
- R_P = 50k

But, the final values should be calculated using the previous equations and checked at 25°C and 100°C.

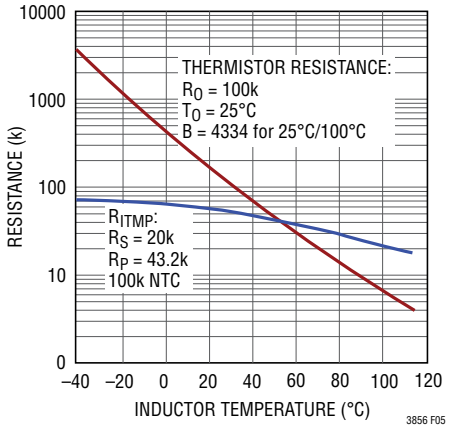

Figure 5. Resistance vs Temperature for the ITEMP Pin Network and the 100k NTC

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After determining the components for the temperature compensation network, check the results by plotting I_{MAX} versus inductor temperature using the following equations:

$$I_{MAX} = \frac{V_{SENSEMAX(ADJ)} - \frac{\Delta V_{SENSE}}{2}}{DCR_{MAX}\ AT\ 25°C \bullet \left[1 + (T_{L(MAX)} - 25°C) \bullet \frac{0.4}{100}\right]}$$

where

$$V_{SENSEMAX(ADJ)} = V_{SENSE(MAX)} \bullet \frac{1.8V - V_{ITMP}}{1.3} - A$$

$$V_{ITMP} = 10\mu A \bullet (R_S + R_P || R_{NTC})$$

Use typical values for $V_{SENSE(MAX)}$. Subtracting constant A will provide a minimum value for $V_{SENSE(MAX)}$. These values are summarized in Table 2.

Table 2. Values for $V_{SENSE(MAX)}$

I_{LIM}	GND	FLOAT	$INTV_{CC}$
$V_{SENSE(MAX)}$ Typ	30mV	50mV	75mV
A	5mV	5mV	7mV

The resulting current limit should be greater than or equal to I_{MAX} for inductor temperatures between 25°C and 100°C.

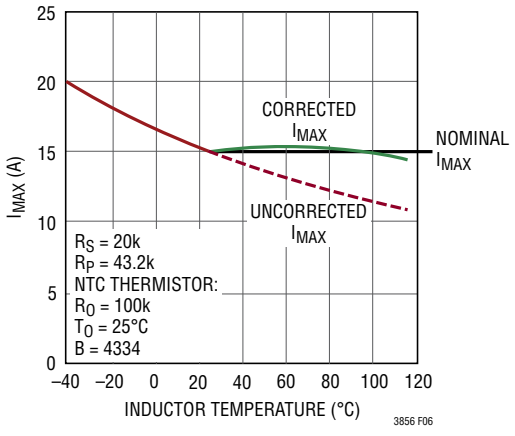

Figure 6. Worst Case I_{MAX} vs Inductor Temperature Curve with and without NTC Temperature Compensation

Typical values for the NTC compensation network are:

- NTC R_0 = 100k, B-constant = 3000 to 4000
- $R_S \approx 20k$
- $R_P \approx 50k$

Another approach for generating the I_{MAX} versus inductor temperature curve plot is to first use the aforementioned values as a starting point and then adjusting the R_S and R_P values as necessary. Figure 6 shows a typical curve of I_{MAX} versus inductor temperature.

The same thermistor network can be used to correct for temperatures less than 25°C. But, ensure that V_{ITEMP} is greater than 0.2V for duty cycles of 25% or more, otherwise temperature correction may not occur at elevated ambients. For the most accurate temperature detection, place the thermistor next to the inductors, as shown in Figure 7. Take care to keep the ITEMP pins away from the switch nodes.

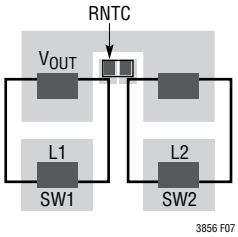

Figure 7. Thermistor Location. Place Thermistor Next to Inductor(s) for Accurate Sensing of the Inductor Temperature, But Keep the ITEMP Pin Away from the Switch Nodes and Gate Drive Traces.

Slope Compensation and Inductor Peak Current

Slope compensation provides stability in constant-frequency, current mode architectures by preventing subharmonic oscillation at high duty cycles. It is accomplished internally by adding a compensating ramp to the inductor current signal at duty cycles in excess of 40%. Normally, this results in a reduction of maximum inductor peak current for duty cycles greater than 40%. However, the LTC3856 uses a scheme that counteracts this compensating ramp, which allows the maximum inductor peak current to remain unaffected throughout all duty cycles.

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Inductor Value Calculation and Output Ripple Current

The operating frequency and inductor selection are interrelated in that higher operating frequencies allow the use of smaller inductor and capacitor values. A higher frequency generally results in lower efficiency because of MOSFET gate charge and transition losses. In addition to this basic trade-off, the effect of inductor value on ripple current and low current operation must also be considered. The PolyPhase approach reduces both input and output ripple currents while optimizing individual output stages to run at a lower fundamental frequency, enhancing efficiency.

The inductor value has a direct effect on ripple current. The inductor ripple current, ΔI_L, per individual section N, decreases with higher inductance or frequency and increases with higher V_{IN} or V_{OUT}:

$$\Delta I_L = \frac{V_{OUT}}{f_{OSC} \bullet L}\left(1-\frac{V_{OUT}}{V_{IN}}\right)$$

where f_{OSC} is the individual output stage operating frequency.

In a PolyPhase converter, the net ripple current seen by the output capacitor is much smaller than the individual inductor ripple currents due to the ripple cancellation. The details on how to calculate the net output ripple current can be found in Application Note 77.

Figure 8 shows the net ripple current seen by the output capacitors for the different phase configurations. The output ripple current is plotted for a fixed output voltage as the duty factor is varied between 10% and 90% on the x-axis. The output ripple current is normalized against the inductor ripple current at zero duty factor. The graph can be used in place of tedious calculations. The zero output ripple current is obtained when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \text{ where } k = 1, 2, ..., N-1$$

Power MOSFET and Schottky Diode (Optional) Selection

At least two external power MOSFETs must be selected for each power stage: One N-channel MOSFET for the top (main) switch and one or more N-channel MOSFET(s) for the bottom (synchronous) switch. The number, type and on-resistance of all MOSFETs selected take into account the voltage step-down ratio as well as the actual position (main or synchronous) in which the MOSFET will be used. A much smaller and much lower input capacitance MOSFET should be used for the top MOSFET in applications that have an output voltage that is less than one-third of the input voltage. In applications where $V_{IN} >> V_{OUT}$, the top MOSFETs' on-resistance is normally less important for overall efficiency than its input capacitance at operating frequencies above 300kHz. MOSFET manufacturers have designed special purpose devices that provide reasonably low on-resistance with significantly reduced input capacitance for the main switch application in switching regulators.

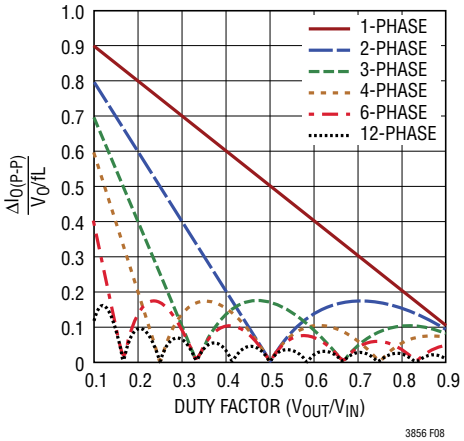

Figure 8. Normalized Peak Output Current vs Duty Factor [$I_{RMS} = 0.3(I_{OP-P})$]

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The peak-to-peak MOSFET gate drive levels are set by the voltage, V_{CC}, requiring the use of logic-level threshold MOSFETs in most applications. Pay close attention to the BV_{DSS} specification for the MOSFETs as well; many of the logic-level MOSFETs are limited to 30V or less. Selection criteria for the power MOSFETs include the on-resistance, $R_{DS(ON)}$, input capacitance, input voltage and maximum output current. MOSFET input capacitance is a combination of several components but can be taken from the typical gate charge curve included on most data sheets (Figure 9). The curve is generated by forcing a constant input current into the gate of a common source, current source loaded stage, then plotting the gate voltage versus time.

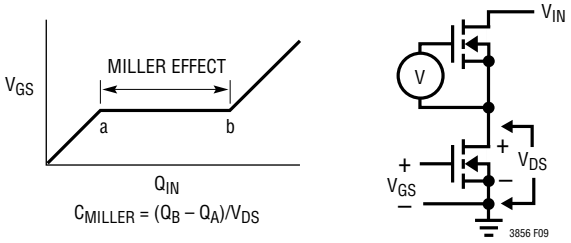

Figure 9. Gate Charge Characteristic

The initial slope is the effect of the gate-to-source and the gate-to-drain capacitance. The flat portion of the curve is the result of the Miller multiplication effect of the drain-to-gate capacitance as the drain drops the voltage across the current source load. The upper sloping line is due to the drain-to-gate accumulation capacitance and the gate-to-source capacitance. The Miller charge (the increase in coulombs on the horizontal axis from a to b while the curve is flat) is specified for a given V_{DS} drain voltage, but can be adjusted for different V_{DS} voltages by multiplying the ratio of the application V_{DS} to the curve specified V_{DS} values. A way to estimate the C_{MILLER} term is to take the change in gate charge from points a and b on a manufacturer's data sheet and divide by the stated V_{DS} voltage specified. C_{MILLER} is the most important selection criteria for determining the transition loss term in the top MOSFET but is not directly specified on MOSFET data sheets. C_{RSS} and C_{OS} are specified sometimes but definitions of these parameters are not included. When the controller is operating in continuous mode, the duty cycles for the top and bottom MOSFETs are given by:

$$\text{Main Switch Duty Cycle} = \frac{V_{OUT}}{V_{IN}}$$

$$\text{Synchronous Switch Duty Cycle} = \left(\frac{V_{IN} - V_{OUT}}{V_{IN}}\right)$$

The power dissipation for the main and synchronous MOSFETs at maximum output current are given by:

$$P_{MAIN} = \frac{V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2 (1+\delta)R_{DS(ON)} +$$

$$(V_{IN})^2\left(\frac{I_{MAX}}{2N}\right)(R_{DR})(C_{MILLER})\bullet$$

$$\left[\frac{1}{V_{CC} - V_{TH(IL)}} + \frac{1}{V_{TH(IL)}}\right]\bullet f$$

$$P_{SYNC} = \frac{V_{IN} - V_{OUT}}{V_{IN}}\left(\frac{I_{MAX}}{N}\right)^2 (1+\delta)R_{DS(ON)}$$

where N is the number of output stages, δ is the temperature dependency of $R_{DS(ON)}$, R_{DR} is the effective top driver resistance (approximately 2Ω at $V_{GS} = V_{MILLER}$), V_{IN} is the drain potential and the change in drain potential in the particular application. $V_{TH(IL)}$ is the data sheet specified typical gate threshold voltage specified in the power MOSFET data sheet at the specified drain current. C_{MILLER} is the calculated capacitance using the gate charge curve from the MOSFET data sheet and the technique just described.

Both MOSFETs have I^2R losses while the topside N-channel equation includes an additional term for transition losses, which peak at the highest input voltage. For $V_{IN} < 20V$, the high current efficiency generally improves with larger MOSFETs, while for $V_{IN} > 20V$, the transition losses rapidly increase to the point that the use of a higher $R_{DS(ON)}$ device with lower C_{MILLER} actually provides higher efficiency. The synchronous MOSFET losses are greatest at high input voltage when the top switch duty factor is low, or during a short-circuit when the synchronous switch is on close to 100% of the period.

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The term (1 + δ) is generally given for a MOSFET in the form of a normalized $R_{DS(ON)}$ vs temperature curve, but δ = 0.005/°C can be used as an approximation for low voltage MOSFETs.

The optional Schottky diodes conduct during the dead time between the conduction of the two large power MOSFETs. This prevents the body diode of the bottom MOSFET from turning on, storing charge during the dead time and requiring a reverse-recovery period which could cost as much as several percent in efficiency. A 2A to 8A Schottky is generally a good compromise for both regions of operation due to the relatively small average current. Larger diodes result in additional transition loss due to their larger junction capacitance. A Schottky diode in parallel with the bottom FET may also provide a modest improvement in Burst Mode efficiency.

C_{IN} and C_{OUT} Selection

In continuous mode, the source current of each top N-channel MOSFET is a square wave of duty cycle V_{OUT}/V_{IN}. A low ESR input capacitor sized for the maximum RMS current must be used. The details of a close form equation can be found in Application Note 77. Figure 10 shows the input capacitor ripple current for different phase configurations with the output voltage fixed and input voltage varied. The input ripple current is normalized against the DC output current. The graph can be used in place of tedious calculations. The minimum input ripple current can be achieved when the product of phase number and output voltage, $N(V_{OUT})$, is approximately equal to the input voltage, V_{IN}, or:

$$\frac{V_{OUT}}{V_{IN}} = \frac{k}{N} \text{ where } k = 1, 2, ..., N-1$$

So, the phase number can be chosen to minimize the input capacitor size for the given input and output voltages. In the graph of Figure 10, the local maximum input RMS capacitor currents are reached when:

$$\frac{V_{OUT}}{V_{IN}} = \frac{2k-1}{N} \text{ where } k = 1, 2, ..., N$$

These worst-case conditions are commonly used for design because even significant deviations do not offer much relief. Note that capacitor manufacturer's ripple current ratings are often based on only 2000 hours of life. This makes it advisable to further derate the capacitor or to choose a capacitor rated at a higher temperature than required. Several capacitors may also be paralleled to meet size or height requirements in the design. Always consult the capacitor manufacturer if there is any question.

The Figure 10 graph shows that the peak RMS input current is reduced linearly, inversely proportional to the number N of stages used. It is important to note that the efficiency loss is proportional to the input RMS current squared and therefore a 3-stage implementation results in 90% less power loss when compared to a single-phase design. Battery/input protection fuse resistance (if used), PC board trace and connector resistance losses are also

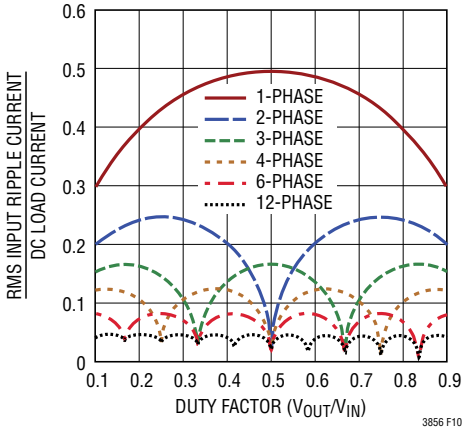

Figure 10. Normalized Input RMS Ripple Current vs Duty Factor for One to Six Output Stages

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reduced by the reduction of the input ripple current in a PolyPhase system. The required amount of input capacitance is further reduced by the factor N, due to the effective increase in the frequency of the current pulses. Ceramic capacitors are becoming very popular for small designs but several cautions should be observed. X7R, X5R and Y5V are examples of a few of the ceramic materials used as the dielectric layer, and these different dielectrics have very different effect on the capacitance value due to the voltage and temperature conditions applied. Physically, if the capacitance value changes due to applied voltage change, there is a concomitant piezo effect which results in radiating sound! A load that draws varying current at an audible rate may cause an attendant varying input voltage on a ceramic capacitor, resulting in an audible signal. A secondary issue relates to the energy flowing back into a ceramic capacitor whose capacitance value is being reduced by the increasing charge. The voltage can increase at a considerably higher rate than the constant current being supplied because the capacitance value is decreasing as the voltage is increasing! Nevertheless, ceramic capacitors, when properly selected and used, can provide the lowest overall loss due to their extremely low ESR.

The selection of C_{OUT} is driven by the required effective series resistance (ESR). Typically once the ESR requirement is satisfied the capacitance is adequate for filtering. The steady-state output ripple (ΔV_{OUT}) is determined by:

$$\Delta V_{OUT} \approx \Delta I_L \left(ESR + \frac{1}{8NfC_{OUT}} \right)$$

where f = operating frequency of each stage, N = the number of output stages, C_{OUT} = output capacitance and ΔI_L = ripple current in each inductor. The output ripple is highest at maximum input voltage since ΔI_L increases with input voltage. The output ripple will be less than 50mV at maximum V_{IN} with $\Delta I_L = 0.4 I_{OUT(MAX)}$ assuming:

C_{OUT} required ESR < N • R_{SENSE}

and

$$C_{OUT} > \frac{1}{(8Nf)(R_{SENSE})}$$

The emergence of very low ESR capacitors in small, surface mount packages makes very small physical implementations possible. The ability to externally compensate the switching regulator loop using the I_{TH} pin allows a much wider selection of output capacitor types. The impedance characteristic of each capacitor type is significantly different than an ideal capacitor and therefore requires accurate modeling or bench evaluation during design. Manufacturers such as Nichicon, Nippon Chemi-Con and Sanyo should be considered for high performance through-hole capacitors. The OS-CON semiconductor dielectric capacitors available from Sanyo and the Panasonic SP surface mount types have a good (ESR)(size) product.

Once the ESR requirement for C_{OUT} has been met, the RMS current rating generally far exceeds the $I_{RIPPLE(P-P)}$ requirement. Ceramic capacitors from AVX, Taiyo Yuden and Murata offer high capacitance value and very low ESR, especially applicable for low output voltage applications.

In surface mount applications, multiple capacitors may have to be paralleled to meet the ESR or RMS current handling requirements of the application. Aluminum electrolytic and dry tantalum capacitors are both available in surface mount configurations. New special polymer surface mount capacitors offer very low ESR also but have much lower capacitive density per unit volume. In the case of tantalum, it is critical that the capacitors are surge tested for use in switching power supplies. Several excellent choices are the AVX TPS, AVX TPSV, the KEMET T510 series of surface mount tantalums or the Panasonic SP series of surface mount special polymer capacitors available in case heights ranging from 2mm to 4mm. Other capacitor types include Sanyo POSCAP, Sanyo OS-CON, Nichicon PL series and Sprague 595D series. Consult the manufacturers for other specific recommendations.

Differential Amplifier

The LTC3856 has a true remote voltage sense capability. The sensing connections should be returned from the load, back to the differential amplifier's inputs through a common, tightly coupled pair of PC traces. The differential amplifier rejects common mode signals capacitively or inductively radiated into the feedback PC traces as well as ground loop disturbances. The differential amplifier output signal is divided by a pair of resistors and is compared with the internal, precision 0.6V voltage reference by the

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error amplifier. The amplifier has an output swing range of 0V to 3.6V. The output uses an NPN emitter follower with 80k feedback resistance.

Active Voltage Positioning (AVP)

In an application, the AVP scheme modifies the regulated output voltage depending on its current loading. AVP can improve overall transient response and save power consumption.

The LTC3856 senses inductor current information by monitoring voltage drops across the sense resistors R_{SENSE} or the DCR sensing network of the two channels. The voltage drops are added together and applied as $V_{PRE-AVP}$ between the AVP and DIFFP pins, which are connected through resistor $R_{PRE-AVP}$. Then $V_{PRE-AVP}$ is scaled through R_{AVP} and added to output voltage as the compensation for the load voltage drop.

Let:

$$\Delta V = V_{SENSE1}^{+} - V_{SENSE1}^{-}$$

$$\Delta V = V_{SENSE2}^{+} - V_{SENSE2}^{-}$$

then:

$$\Delta V_{DIFFP,VOUT} = 2 \bullet \Delta V \left(\frac{R_{AVP}}{R_{PRE-AVP}} \right)$$

The final load slope is defined by the inductor current sense resistors and the two external resistors previously mentioned.

In summary, the load slope is:

$$\left(R_{SENSE} \bullet \frac{R_{AVP}}{R_{PRE-AVP}} \right) V/A$$

The recommended value for R_{AVP} is 90Ω to 100Ω. The maximum output voltage at AVP is 2.5V. Therefore, for outputs higher than 2.5V, the AVP function is not supported. The DIFFP pin, however, should always be connected to the output even when AVP or diffamp functions are not used. When AVP function is not desired, float the AVP pin or connect a resistor between the AVP pin and DIFFP pin. $R_{PRE-AVP}$ on the order of 1kΩ is recommended.

Programmable Stage Shedding Mode

When the MODE pin is tied to $INTV_{CC}$, the LTC3856 enters Stage Shedding mode. This means that the second channel will stop switching when I_{TH} is below a certain programmed threshold. This threshold voltage on I_{TH} is programmed according to the following formula:

$$V_{SHED} = 0.5 + \left(\frac{5}{3} \right) \bullet (0.5 - V_{ISET})$$

The valid range of V_{ISET} is between 0V to 0.5V, where V_{ISET} is the voltage on the ISET pin. There is a precision 7.5µA flowing out of the ISET pin. Connecting a resistor to SGND sets the V_{ISET} voltage. When left floating, V_{ISET} voltage will be at $INTV_{CC}$. The Stage Shedding mode threshold voltage in this case will be 0.5V. There is a 50mV hysteresis for the Stage Shedding mode threshold comparator.

Programmable Burst Mode Operation

When the MODE pin is floating, the LTC3856 enters Burst Mode operation. This means that both channels will stop switching when I_{TH} is below a certain threshold.

The Burst Mode clamp, which sets the current limit when bursting, can be programmed through V_{ISET} according to the following formula:

$$V_{CLAMP} = 0.7 + 0.62\ (0.5 - V_{ISET})$$

The valid range of V_{ISET} is between 0.3V to 0.5V and V_{ISET} is the voltage on the ISET pin. There is a precision 7.5µA flowing out of ISET. Connecting a resistor to SGND sets the V_{ISET} voltage. When left floating, V_{ISET} will be at $INTV_{CC}$. The Burst Mode clamp voltage in this case will be 0.7V. There is a 50mV hysteresis for the Burst Mode comparator.